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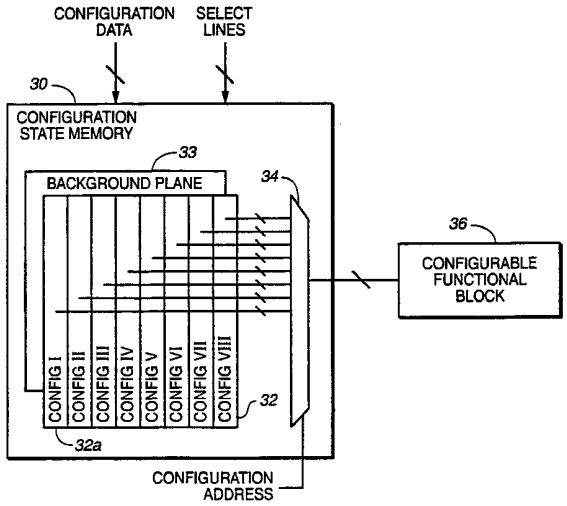
(54) Title: CONFIGURATION STATE MEMORY FOR FUNCTIONAL BLOCKS ON A RECONFIGURABLE CHIP



(57) Abstract: A configuration state memory (30) is associated with a configurable functional block (36) on a reconfigurable chip. The configuration state memory (30) stores more than one configuration (32) for the functional block (36). This allows the functional block (36) to switch configuration without requiring the configuration data (32a) to be loaded from off-chip which would stall the operation of the reconfigurable chip. In a preferred embodiment, the configuration state memory (30) uses a relatively few address bits (34) to produce a relatively broad configuration output to the functional blocks (36). The small number of input address bits allows the configuration state memory to be addressed by relatively small state machine unit.

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CONFIGURATION STATE MEMORY FOR FUNCTIONAL BLOCKS ON A RECONFIGURABLE CHIP

BACKGROUND OF THE INVENTION

The present invention relates to reconfigurable logic chips.

Reconfigurable logic chips, such as field programmable gate arrays (FPGAs) have become increasingly popular. Such chips allow logic to implement different circuits at different times.

FPGAs are being increasingly used because they offer greater flexibility and shorter development cycles than traditional Application Specific Integrated Circuits (ASICs) while providing most of the performance advantages of a dedicated hardware solution.

One growingly popular use of FPGAs is referred to as reconfigurable computing. In reconfigurable computing, hardware logic functions are loaded into the FPGA as needed to implement different sections of a computationally intensive code. By using the FPGAs to do the computational intensive code, advantages are obtained over dedicated processors. Reconfigurable computing is being pursued by university researchers as well as FPGA companies.

Typically, in order to change configurations, FPGAs load new configuration data for different functional units from off-chip. This can be time consuming and may reduce the efficiency of a reconfigurable computing system. It is desired to have an improved reconfigurable chip for reconfigurable computing.

SUMMARY OF THE PRESENT INVENTION

The present invention comprises a configuration state memory for use on a reconfigurable chip. The configuration state memory stores multiple configurations which can be used to configure a functional block unit into a variety of functions. By storing multiple configurations local to the functional block unit in the configuration statement memory, the system of the present invention allows for dynamic switching between different functions in the functional block unit. This improves the efficiency of reconfigurable computing system. Additional configurations need not be loaded from off-chip to switch the function of a functional unit.

In a preferred embodiment, the functional block units have reconfigurable elements within them which are reconfigured by the configuration lines coming from the configuration state memory. The functional block units can implement a variety of functions such as add, shift, subtract, etc.

In one embodiment, the configuration state memory has a relatively few address bits and a greater number of output configuration lines. In one preferred embodiment, the configuration state memory has a three-bit address and a forty-plus bit configuration output. The number of output bits can be varied depending on the complexity of the data path unit. A three-bit address allows for eight different configurations to be stored locally near the functional block units. In one embodiment of the present invention, the memory in the configuration state memory is arranged into a background plane and a foreground plane. The arrangement into the background plane and the foreground plane allows a background plane to be loaded onto the chip without affecting the operation of the configuration state memory.

The configuration state memory may be a part of a control fabric unit. The configuration state memory is addressed by a state machine that allows the addresses for the configuration state memory to be produced locally on the reconfigurable chip. In this way, a configuration of the state machine can address multiple stored data path unit configurations in the configuration state memory. The configuration state memory preferably stores enough configurations for the data path unit that the data in the configuration state memory need not be changed every time the state machine configuration is changed. The state machine can receive inputs from functional block and the CPU on the reconfigurable chip as well as being configured from off-chip. The state machine can be implemented using a reconfigurable programmable sum of products (PSOP) generator.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a diagram that illustrates the arrangement of a configuration state memory and a configurable functional block used in the present invention.

Figure 2A is a diagram that illustrates one arrangement of the configuration state memory used in the present invention.

Figure 2B is a diagram that illustrates one means of implementing a configuration state memory.

Figure 3 is a diagram of a bus data for use in loading a configuration into the configuration state memory.

Figure 4 is a diagram that illustrates a circuit to load a configuration into the configuration state memory for the present invention.

Figure 5 is a diagram of a memory element that can be used in the configuration state memory of the present invention.

Figure 6 is a diagram of a master/slave latch which can be used to implement one of the memory elements of a configuration state memory to allow for the foreground and background planes.

Figure 7 is a diagram of a reconfigurable chip that can use the configuration state memory of the present invention.

Figure 8A is a diagram illustrating a control fabric unit using the configuration state memory of the present invention.

Figure 8B is a diagram of an embodiment where the configuration state memory is part of a second state machine.

Figure 9 is a diagram illustrating a reconfigurable programmable sum of products generator for use in a state machine in a control fabric shown in Figure 8.

Figure 10 is a diagram that illustrates the inner leaving of the programmable sum of products generator and configuration state memory with the data path units.

Figure 11 is a diagram that illustrates a programmable sum of products generator which is used to address multiple configuration state memory.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 shows a system 20 using the configuration state memory 22 of the present invention. The configuration state memory 22 receives a configuration address and produces from the configuration address a relatively large number of configuration bits sent on the configuration lines 24 to the configurable functional block 26. The configuration state memory is preferably local to the configurable functional block.

The configuration state memory stores a number of configurations for the configurable functional block. By changing the configuration address to the configuration state memory, the functions implemented by the configurable functional block (data path unit) 26 can be modified. The configurable functional block operates on data in a data path according to the pre-loaded function. The data is then sent to additional data path functional blocks using the output data path connections 28.

The advantage of the apparatus of system 20 is that the configuration of functional block 26 need not be loaded from off the reconfigurable chip. Configurations are stored in the configuration state memory 22. Since off-chip data access is an execution speed limiting factor of most computing systems, the use of configuration state memory local to the configurable functional blocks can significantly quicken the operation of a reconfigurable computing system.

The configuration state memory (CSM) 22 preferably has a relatively small number of bits used for the configuration address and much greater number of configuration bits sent to the configurable functional block. The number of configuration address bits sent to the control state memory 22 is dependent on how many dynamic configuration planes need to be stored on the chip. In one embodiment, the number of configuration address bits sent to the CSM 22 is ten or less and the number of configuration bits sent to the configurable functional block 24 is twenty or greater. In a preferred embodiment, the number of configuration address bits is three and the number of output configuration bits is forty-plus. Keeping the number of configuration address bits relatively low allows for a relatively small configuration memory and allows a relatively small state machine produce the configuration address.

In one embodiment, the configuration state memory contains four or greater configurations. In a preferred embodiment, eight configurations are addressed by a three-bit configuration address.

Figure 2A shows one implementation of the configuration state memory 30. The configuration state memory 30 includes a number of configurations 32a in a foreground plane 32. Multiplexer 34 selects the configuration to be sent to the configurable functional block 36. In a preferred embodiment, the system additionally has a background plane 33 which stores a backup configuration to switch into the foreground plane. Both the background plane and the foreground plane data is loaded into the configuration state memory using configuration data and select lines, respectively.

Figure 2B illustrates, one way of implementing a configuration state memory by using a number of smaller memory units.

Figures 3-5 illustrate one embodiment of a system for loading configuration data into the configuration state memory. Figure 3 shows a bus data for the main system bus of a reconfigurable chip. The data can include x address bits and y memory element configuration bits, where $x + y = n$, and n is the bus size. In one embodiment, the bus size is one hundred and twenty-eight (128) bits wide, sixteen (16) address bits and one hundred and twelve (112) configuration bits are used.

Figure 4 shows an address decoder 41 that decodes the address to produce the select lines. Memory elements (not shown) are located at the intersection of the select lines and the configuration bits. These memory elements can include the memory elements for the foreground and background plane of the configuration state memory. Figure 5 illustrates the memory element 40 which can be located at the intersection of the select lines and configuration bits lines shown in Figure 4. The memory element produces an output 42 and receives the write select line 44 and configuration data bits line 46. In one embodiment, one plane of the configuration state memory has eight configurations, each configuration using 45 bits.

Figure 6 illustrates one embodiment of a memory element 50 which can implement a foreground plane bit and a background plane bit. During the normal operation of the memory element, the write select I and the write select II sent to the multiplexers 52 and 54 respectively are both low. This causes the values at nodes 56 and 58 to be maintained. Node 58 stores the output value of the memory element. When configuration data is to be written into the memory element, the write select line I goes high. This causes the data on the data input line to be written into node 56, changing the value of the background plane bit. The value in the background bit at node 56 can be written into the foreground plane bit node 58 by selecting the write select line II. The write select I corresponds to one of the write select lines produced by the address decoder. Write select line II can be a signal sent to a whole block of memory elements causing the background plane to be loaded into the foreground plane.

Reset line 60 allows the nodes 56 and 58 to be zeroed. The reset line 60 is preferably connected to a memory element throughout the chip. This allows for asynchrons operation in which storage values are zeroed without requiring values be loaded through the configuration bit lines shown in Figure 4.

Figure 7 illustrates a reconfigurable chip 70 which can use the configuration state memory of the present invention. The reconfigurable chip 70 is connected to an external memory 72. The memory controller 74 allows data from the external memory 72 to be loaded onto bus 76. The DMA controller 78 loads data into the reconfigurable fabric slices 80 as well as the control fabric units 82. The control fabric units 82 contain the configuration state memory units (not shown) of the present invention. The reconfigurable chip 70 also includes a central processing unit (CPU) 84.

One embodiment of a reconfigurable chip for use with the present invention is disclosed in the patent application, "An Integrated Processor And

Programmable Data Path Chip For Reconfigurable Computing", Serial No. 08/884,380, filed June 27, 1998, incorporated herein by reference.

Figure 8A shows the configuration state memory 90 of the present invention used within a controlled fabric unit 92. The control fabric 92 includes a state machine 94 which is adapted to produce the configuration addresses for the configuration state memory 90. In one embodiment, the state machine comprises a reconfigurable programmable sum of products generator 96 and state machine memory 98.

Figure 8B shows multiplexer 130 that has inputs from the output of configuration state memory 132 and from the reconfigurable PSOP 134. Each line of the configuration state memory 132 has a configuration data field 132a, a next address field 132b and a control bit field 132c. The control bit field determines what input is selected by multiplexer 130. When the PSOP state machine input is selected the address from the PSOP state machine is used to select the data to go to the data path unit 138. When the CSM state machine is selected the address in address field 1326 is used as the next address to the control state memory 202. The system of figure 8B thus provides two compatible state machines which can allow a relatively complicated combined state machine to be stored on the reconfigurable chip.

Figure 9 illustrates a reconfigurable programmable sum of products generator. Details of one embodiment of a reconfigurable programmable sum of products generator is given in the patent application, "Reconfigurable Programmable Sum of Products Generator ," corresponding to Attorney Docket No. 032001-036, which is incorporated herein by reference. The control path unit 92 used for one embodiment of the present invention is described in the patent application, "Control Fabric For Enabling Data Path Flow", corresponding to Attorney Docket No 032001-016, which is incorporated herein by reference.

Figure 10 illustrates the interspersing of the reconfigurable programmable sum of products generators used for the state machine units, the control state memories (CSM), and the data path slices. The data path slices include data path units which implement functional blocks in a preferred embodiment of the present invention.

The data path units are interconnected to produce the data path flow for the reconfigurable chip.

Figure 11 is a diagram of an embodiment in which a reconfigurable programmable sum of products generator 100 is connected to provide the configuration address for multiple configuration state memories 102. The state machines include the reconfigurable programmable sum of products generator 100, the state register block 104, and a multiplexer plane 106 which provide the inputs to the reconfigurable programmable sum of products generator. In this embodiment, three address bits are provided to the control state memory 102 where and forty-five configuration line bits are sent to the data path unit 108. Configuration state memory 103 provides fifty-four configuration bits to send to the multiplier 110.

It will be appreciated by those of ordinary skill in the art that the invention can be implemented in other specific forms without departing from the spirit or central character thereof. The presently disclosed embodiments are therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is illustrated by the appended claims rather than the foregoing description, and all changes which come within the meaning and range for equivalence thereof are intended to be embraced herein.

We claim:

1. A reconfigurable logic chip including:

a reconfigurable functional block adapted to be configured into a number of different functions; and

a configuration state memory adapted to store multiple configurations for the reconfigurable functional block, the configuration state memory being local to the reconfigurable functional block.

2. The reconfigurable logic chip of claim 1, wherein the configuration state memory is a part of a control fabric unit for the reconfigurable logic chip.

3. The reconfigurable logic chip of claim 2, wherein the control fabric unit further comprises a state machine unit used to produce the addresses for the configuration state memory.

4. The reconfigurable chip of claim 3, wherein the state machine unit includes a reconfigurable programmable sum of products generator .

5. The reconfigurable logic chip of claim 1, wherein the reconfigurable functional block comprises a data path unit.

6. The reconfigurable logic chip of claim 5, wherein a number of configurable state memories and data path units are arranged in a tile structure.

7. The reconfigurable logic chip of claim 6, wherein the data path units in adjacent tiles are interconnected.

8. The reconfigurable logic chip of claim 1, wherein the address to the configuration state memory has a fewer number of bits than the configuration output of the configuration state memory.

9. The reconfigurable logic chip of claim 8, wherein the configuration state memory configuration addresses are less than ten bits.

10. The reconfigurable logic chip of claim 9, wherein the configuration state memory, the configuration address comprises three-bits.

11. The reconfigurable logic chip of claim 8, wherein the output configuration is greater than twenty-bits.

12. The reconfigurable logic chip of claim 11, wherein the output configuration is greater than forty-bits.

13. The reconfigurable logic chip of claim 1, wherein the configuration state memory stores more than four configurations.

14. The reconfigurable logic chip of claim 13, wherein the configuration state memory stores eight configurations.

15. A reconfigurable logic chip comprising:

a configurable functional unit adapted to operate on input data, the configurable functional unit including reconfigurable elements; and

a control fabric unit adapted to set reconfigurable elements in the configurable functional unit, the control fabric unit including a configuration

memory adapted to store multiple configurations for the configurable functional unit, the configuration state memory being local to the configurable functional unit.

16. The reconfigurable logic chip of claim 15, wherein the control fabric includes a state machine unit.

17. The reconfigurable logic chip of claim 16, wherein the state memory unit includes a reconfigurable programmable sum of products generator .

18. The reconfigurable logic chip of claim 17, wherein the state machine unit further includes a muxing plane connected to the programmable sum of products generator .

19. The reconfigurable logic chip of claim 17, wherein a state register block is operatively connected to the programmable sum of products generator and to the configuration memory.

20. The reconfigurable logic chip of claim 15, wherein the control fabric unit is associated with multiple configurable functional units.

21. The reconfigurable logic chip of claim 15, wherein the configurable functional unit comprises a data path unit.

22. A reconfigurable logic chip including:

a control fabric unit adapted to set reconfigurable elements in at least one configurable functional unit, the control fabric including a state machine unit and at least one configuration memory operably connected to the state machine unit, the configuration memory storing a number of configurations for the

configurable functional unit, wherein the configurable functional unit is adapted to operate on data.

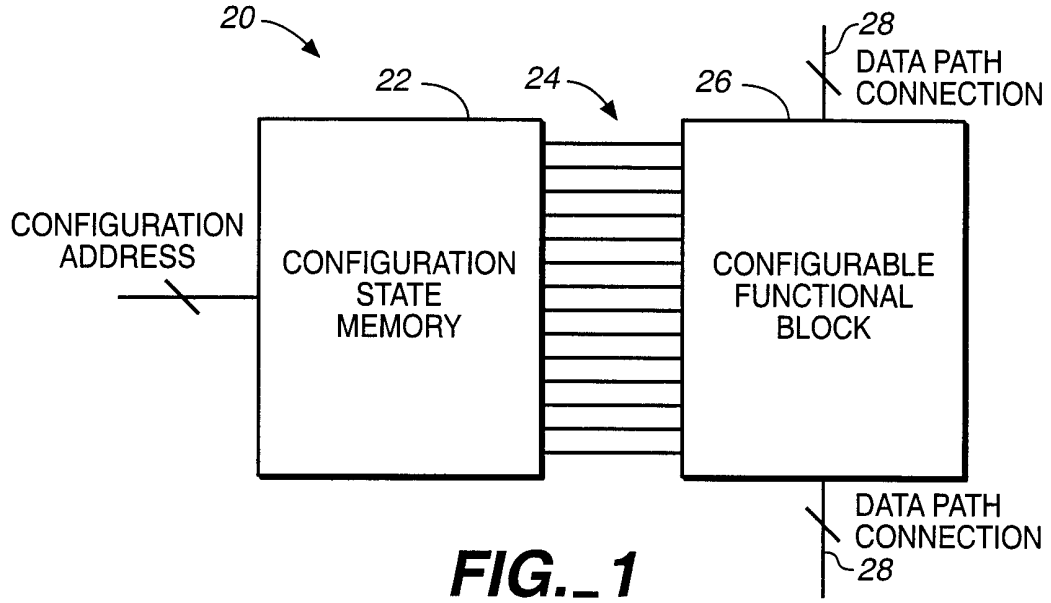
20
22
24
26
28
DATA PATH CONNECTION
CONFIGURATION ADDRESS
CONFIGURATION STATE MEMORY
CONFIGURABLE FUNCTIONAL BLOCK
DATA PATH CONNECTION
28

FIG._1

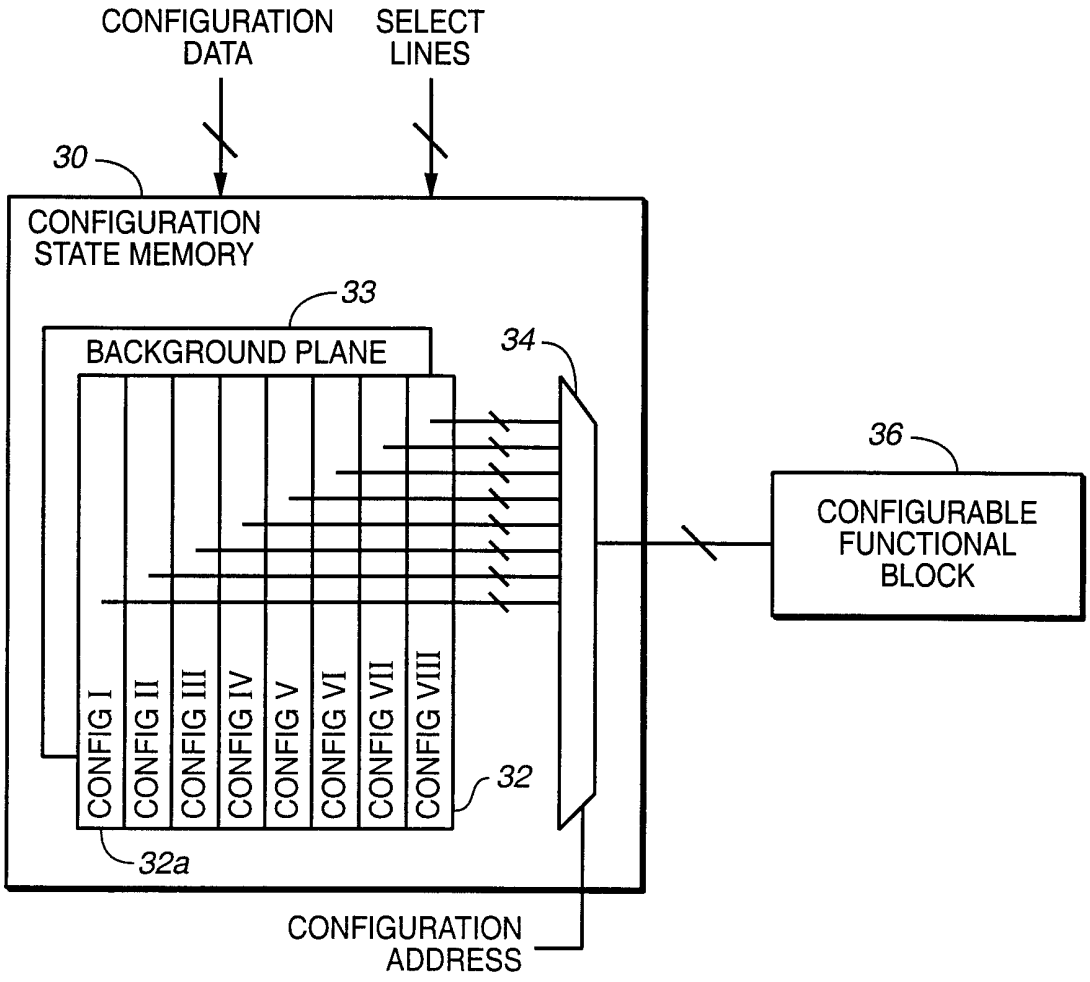
CONFIGURATION DATA
SELECT LINES
30
CONFIGURATION STATE MEMORY
33
BACKGROUND PLANE
34
36
CONFIGURABLE FUNCTIONAL BLOCK
CONFIG I
CONFIG II
CONFIG III
CONFIG IV
CONFIG V
CONFIG VI
CONFIG VII
CONFIG VIII
32
32a
CONFIGURATION ADDRESS

FIG._2A

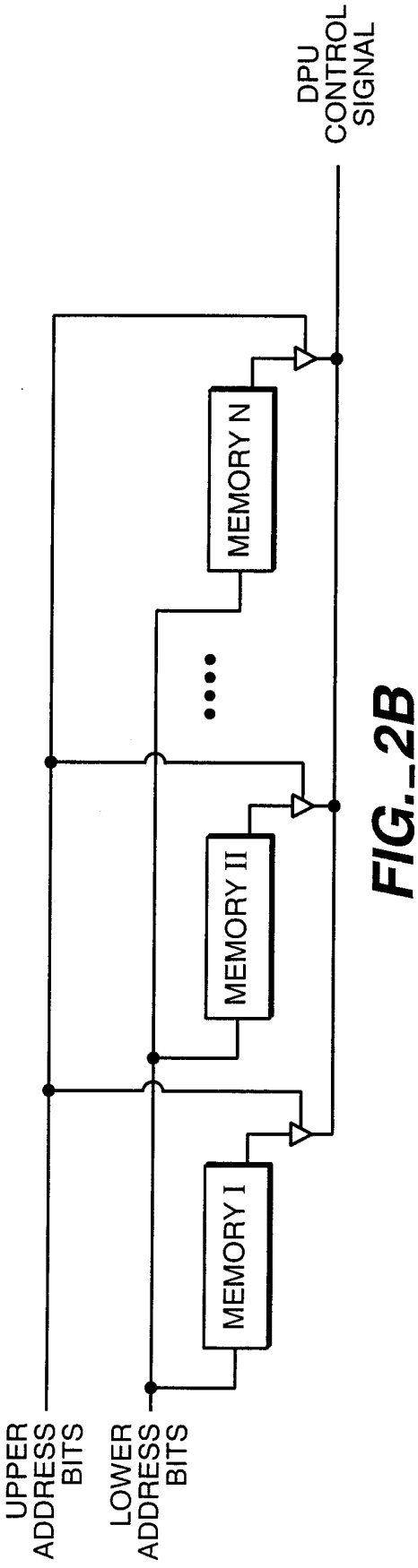

FIG._2B

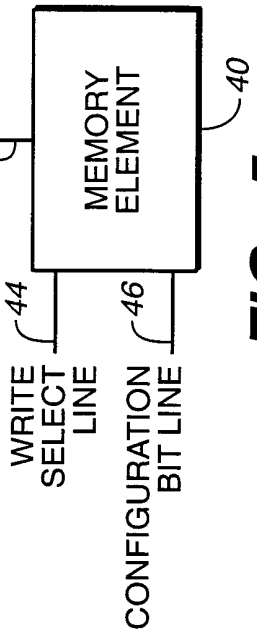

FIG._5

FIG._3

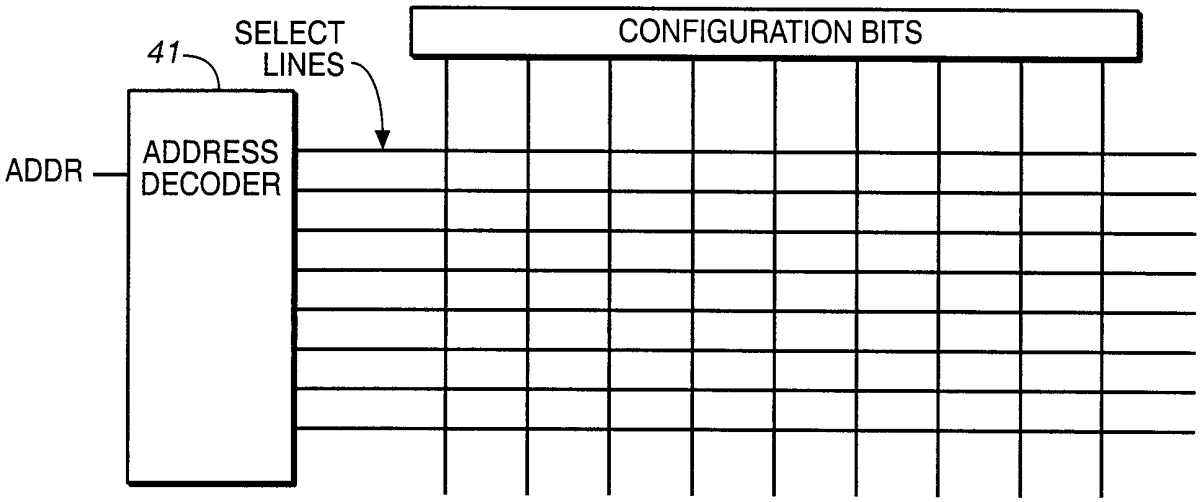
41
SELECT LINES
CONFIGURATION BITS
ADDR
ADDRESS DECODER

FIG._4

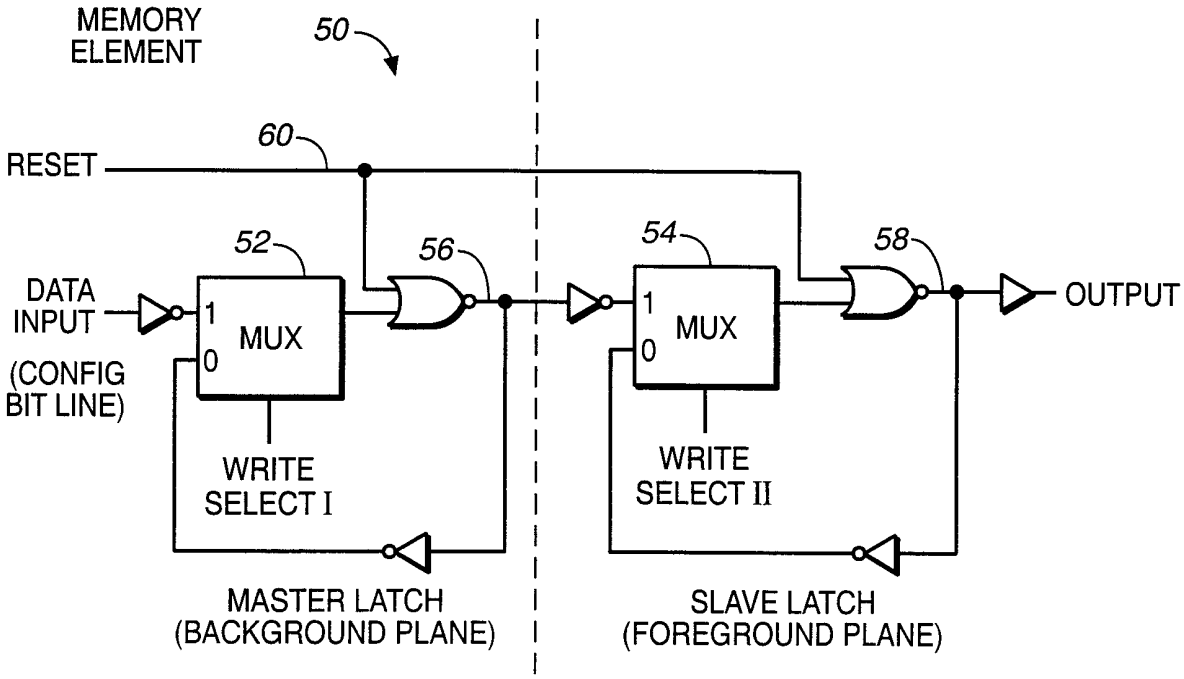
MEMORY ELEMENT
50
60
RESET
52
56
54
58
DATA INPUT
(CONFIG BIT LINE)
1
0
MUX
WRITE SELECT I
MUX
WRITE SELECT II
OUTPUT
MASTER LATCH (BACKGROUND PLANE)
SLAVE LATCH (FOREGROUND PLANE)

FIG._6

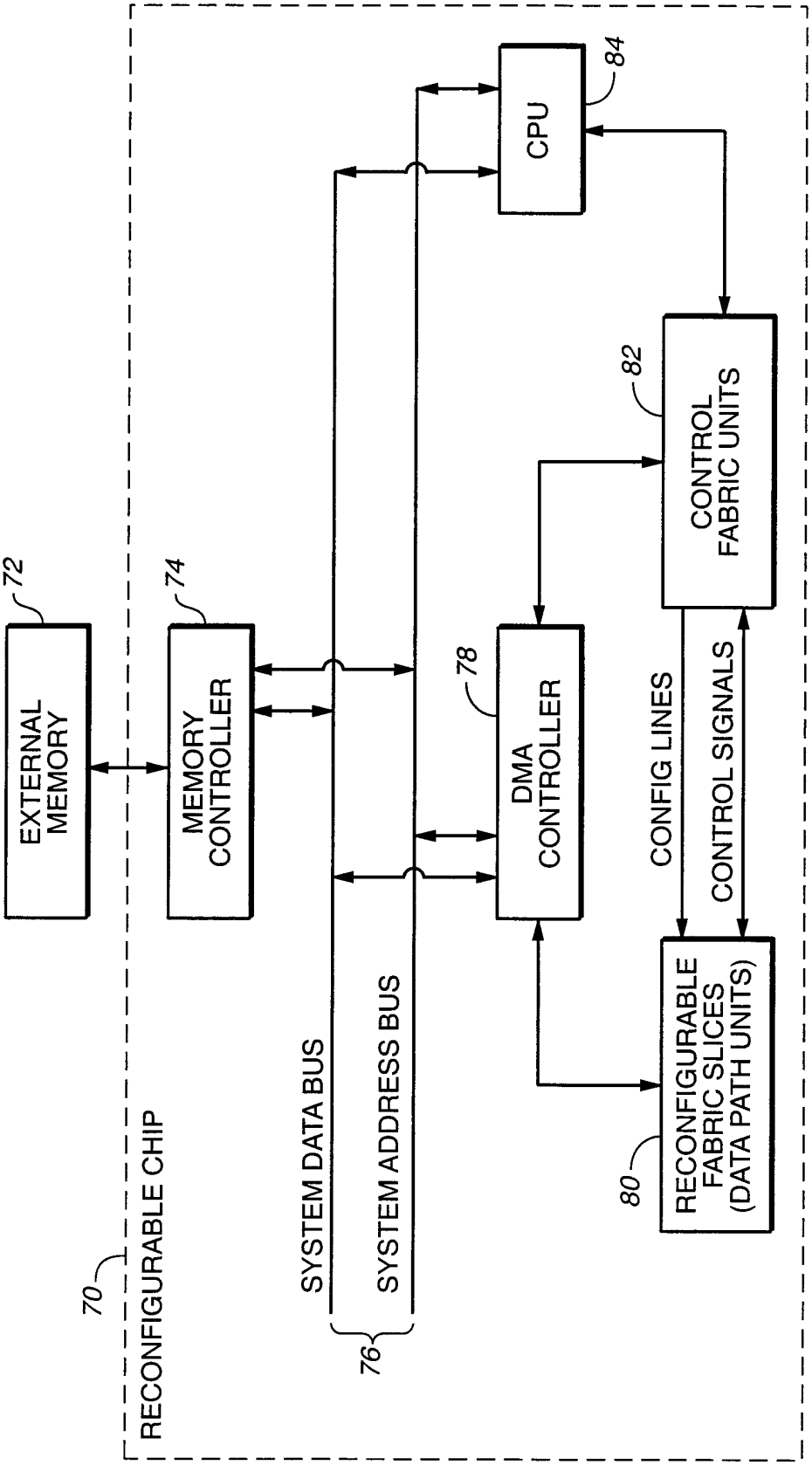
RECONFIGURABLE CHIP
70
EXTERNAL MEMORY
72
MEMORY CONTROLLER
74
SYSTEM DATA BUS
SYSTEM ADDRESS BUS
76
DMA CONTROLLER
78
CPU
84
CONTROL FABRIC UNITS
82
CONFIG LINES
CONTROL SIGNALS
RECONFIGURABLE FABRIC SLICES (DATA PATH UNITS)
80

FIG._7

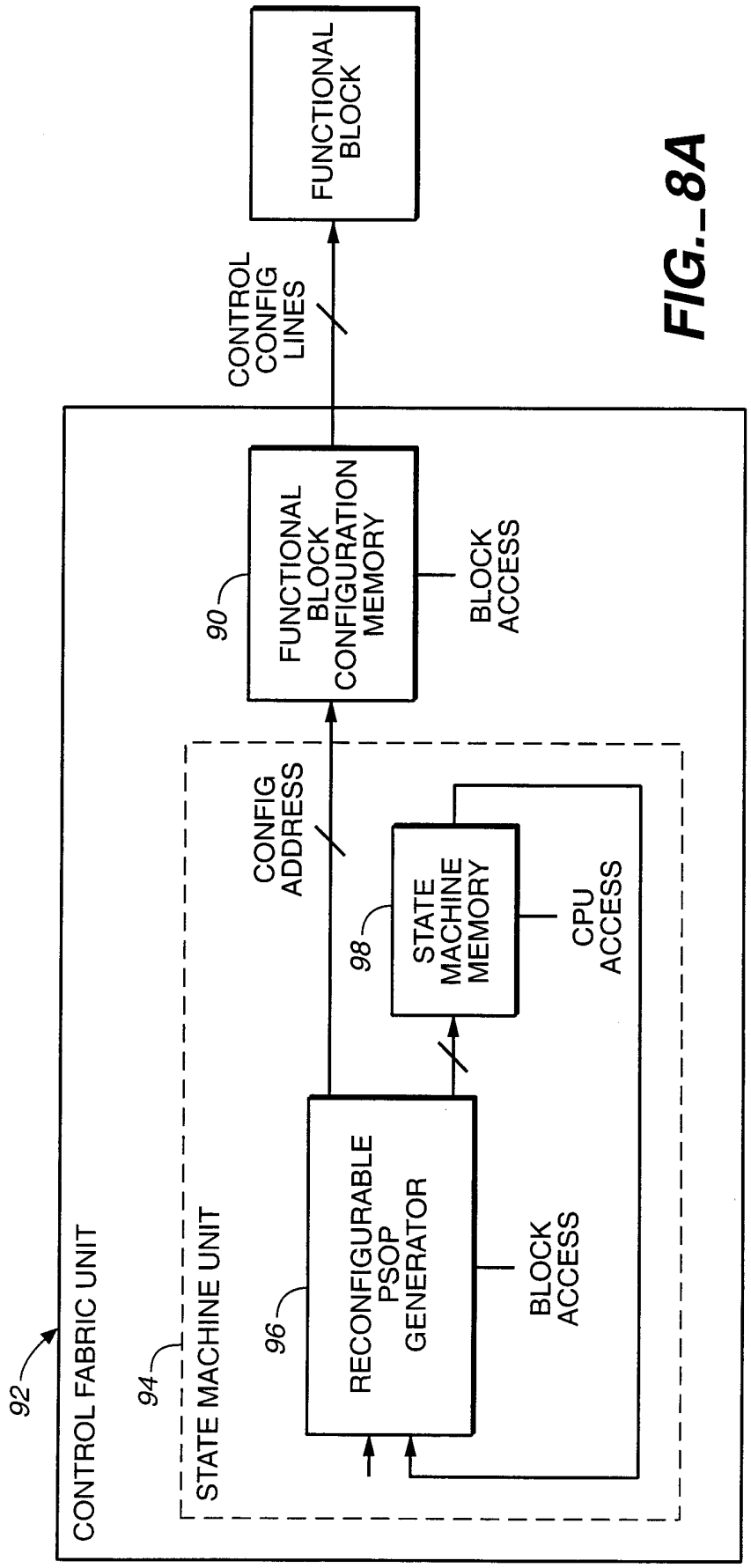
FUNCTIONAL BLOCK
CONTROL CONFIG LINES
FUNCTIONAL BLOCK CONFIGURATION MEMORY
90
BLOCK ACCESS
CONFIG ADDRESS
STATE MACHINE MEMORY
98
CPU ACCESS
RECONFIGURABLE PSOP GENERATOR
96
BLOCK ACCESS
STATE MACHINE UNIT
94
CONTROL FABRIC UNIT
92

FIG._8A

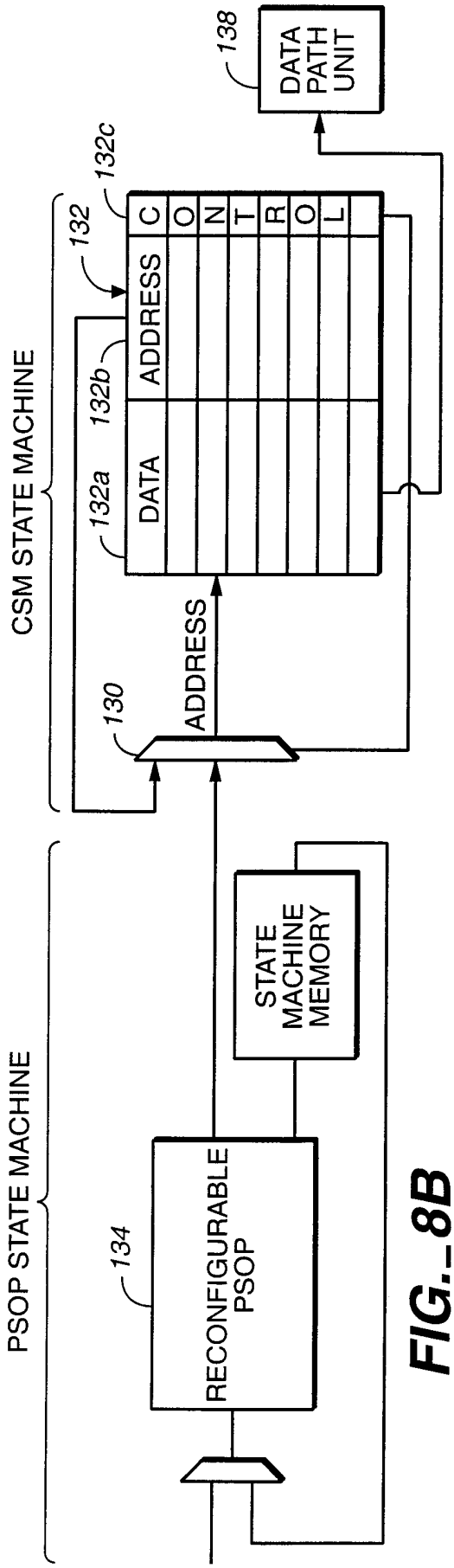
PSOP STATE MACHINE
CSM STATE MACHINE
RECONFIGURABLE PSOP
134
STATE MACHINE MEMORY
130
ADDRESS
132
132a
DATA
132b
ADDRESS
132c
CONTROL
138
DATA PATH UNIT

FIG._8B

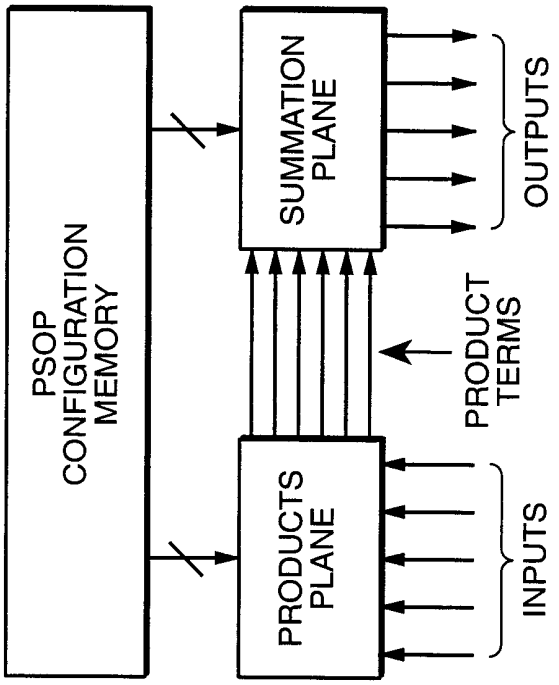
PSOP CONFIGURATION MEMORY
PRODUCTS PLANE
SUMMATION PLANE
PRODUCT TERMS
INPUTS
OUTPUTS

FIG._9

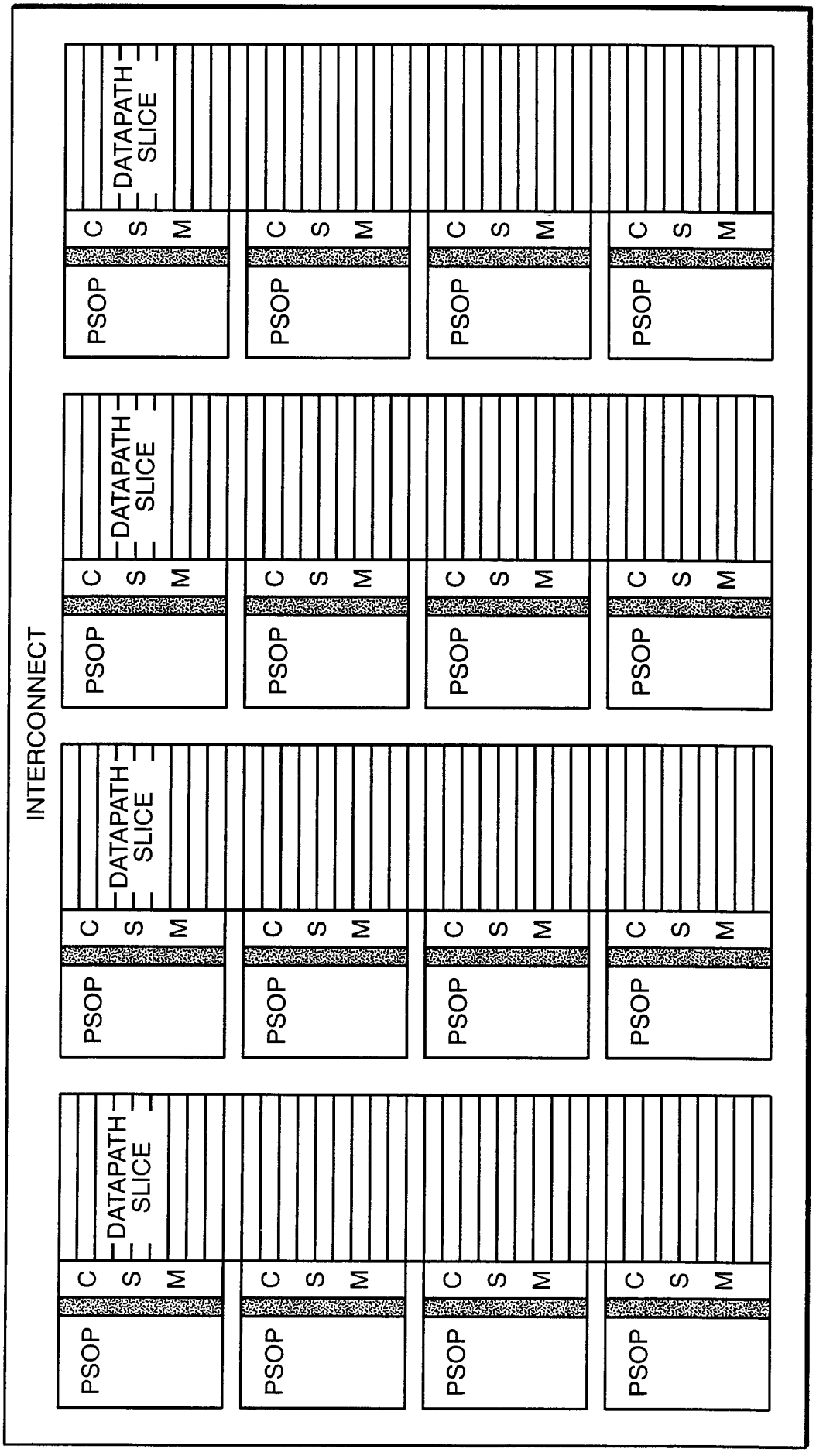

FIG._10

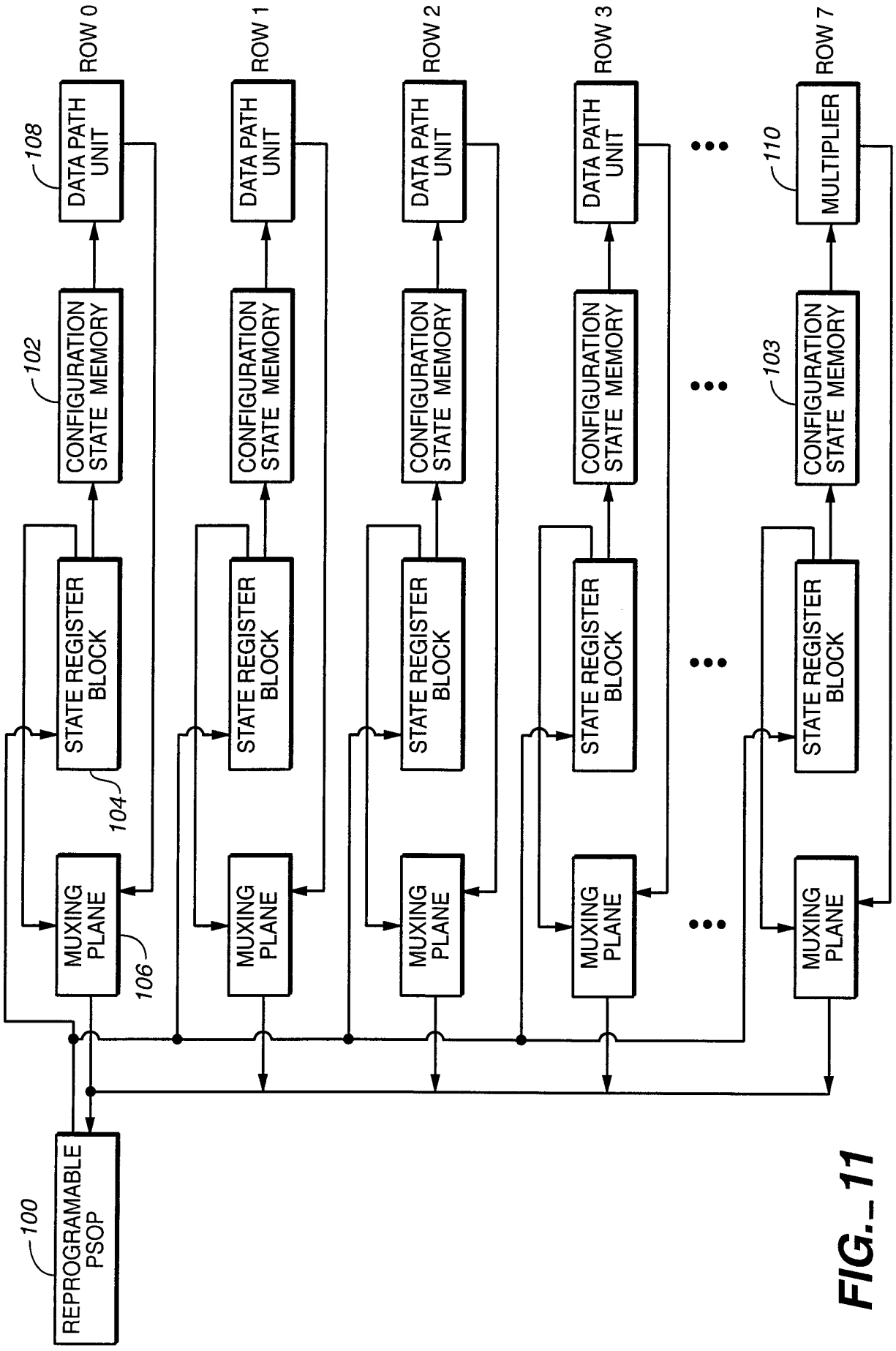
ROW 0
ROW 1
ROW 2
ROW 3
ROW 7
108
DATA PATH UNIT
110
MULTIPLIER
102
CONFIGURATION STATE MEMORY
103
104
STATE REGISTER BLOCK
106
MUXING PLANE
100
REPROGRAMABLE PSOP

FIG._11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/23976

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H03K 19/173
US CL :326/38

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 326/38, 39, 40, 41, 46, 47

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,426,378 A (ONG) 20 June 1995 (20.06.1995), col. 3, line 65 - col. 4, line 52 and fig. 1.	1-2, 5-9, 11-15, 20-21
X,P --- Y,P	US 6,018,559 A (AZEGAMI et al) 25 January 2000 (25.01.2000), col. 24, lines 26-55 and fig. 41.	1-2, 5-9, 11-15, 20-21 --- 3-4, 10, 16-19, 22
Y,P	US 6,005,865 A (LEWIS et al) 21 December 1999 (21.12.1999), col. 8, lines 1-26 fig. 5B.	3-4, 10, 16-19, 22
X,P	US 6,091,263 A (NEW et al) 18 July 2000 (18.07.2000), col. 7, line 42 - col. 9, line 29 and fig. 9.	1-2, 5-9, 11-15, 20-21

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
11 OCTOBER 2000	14 NOV 2000

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/23976

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,796,269 A (NEW) 18 August 1998 (18.08.1998), fig. 1.	1-22
A	US 5,760,602 A (TAN) 02 June 1998 (02.06.1998), fig. 1.	1-22
Y	US 5,550,782 A (CLIFF et al) 27 August 1996 (27.08.1996), col. 13, lines 40-65 and fig. 16A	3-4, 10, 16-19, 22