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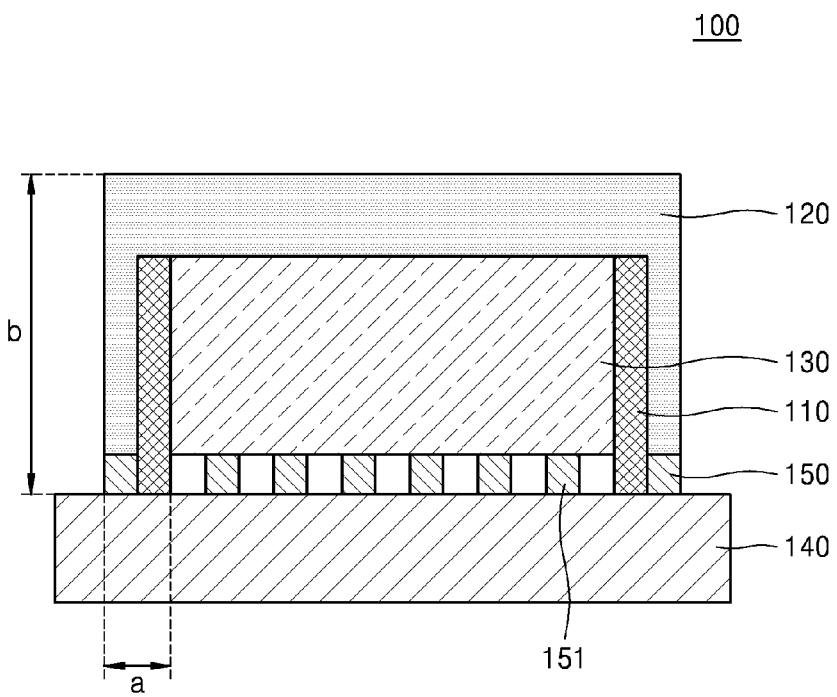
(54) Title: SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING THE SAME



(57) Abstract: A semiconductor package includes a semiconductor chip mounted on a substrate, an insulating layer covering at least a portion of the semiconductor chip and including a thixotropic material or a hot melt material, and a shielding layer covering at least a portion of the semiconductor chip and the insulating layer. A method of manufacturing the semiconductor package includes forming an insulating layer and a shielding layer having a high aspect ratio by using a three-dimensional printer.

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Description

Title of Invention: SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING THE SAME

Technical Field

[1] The present disclosure relates to a semiconductor package and a method of manufacturing the same, and more particularly, to a semiconductor package including an electromagnetic waves shielding member for protecting a semiconductor chip in the semiconductor package from external factors and shielding electromagnetic waves, and a method of manufacturing the same.

Background Art

[2] As the market for electronic products expands, demand for more functionality and smaller portable devices have rapidly increased, and, thus, technology has led to miniaturization and weight reduction of electronic components in the electronic products. In this regard, not only are sizes of the various electronic components reduced, but several discrete semiconductor chips may be put in one semiconductor package. In particular, a semiconductor packages capable of processing high frequency signals should not only be miniaturized but also include various electromagnetic waves shielding structures to alleviate electromagnetic interference or electromagnetic susceptibility.

Disclosure of Invention

Solution to Problem

[3] Provided is a semiconductor package including an electromagnetic wave shielding structure that allows miniaturization and weight reduction of the semiconductor package and also has excellent shielding properties with respect to electromagnetic interference.

[4] Additional aspects will be set forth in part in the description that follows and, in part, will be apparent from the description or may be learned by practice of the presented exemplary embodiments.

Brief Description of Drawings

[5] These and/or other aspects will become apparent and more readily appreciated from the following description of the exemplary embodiments, taken in conjunction with the accompanying drawings in which:

[6] FIG. 1 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[7] FIG. 2A and 2B are views for describing states for a thixotropic material included in a semiconductor package according to an exemplary embodiment;

[8] FIG. 3 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[9] FIG. 4 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[10] FIG. 5 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[11] FIG. 6 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[12] FIG. 7 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[13] FIG. 8 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[14] FIG. 9 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[15] FIG. 10 is a cross-sectional view of a semiconductor package according to an exemplary embodiment;

[16] FIGS. 11A through 11E are views for describing a process of manufacturing a semiconductor package, according to an exemplary embodiment;

[17] FIG. 12 is a perspective view of a three-dimensional (3D) printer for manufacturing a semiconductor package, according to an exemplary embodiment;

[18] FIG. 13 is a conceptual view for describing a 3D printer for manufacturing a semiconductor package, according to an exemplary embodiment;

[19] FIG. 14 is a view for describing an operating method of a 3D printer for manufacturing a semiconductor package, according to an exemplary embodiment;

[20] FIGS. 15A and 15B are views for describing a method of manufacturing a semiconductor package, according to an exemplary embodiment;

[21] FIGS. 16A and 16B are views for describing a method of manufacturing a semiconductor package, according to an exemplary embodiment;

[22] FIG. 17 is a schematic view of a structure of a semiconductor package according to an exemplary embodiment;

[23] FIG. 18 is a view of an electronic system including a semiconductor package, according to an exemplary embodiment; and

[24] FIG. 19 is a schematic perspective view of an electronic device, to which a semiconductor package is applied, according to an exemplary embodiment.

Best Mode for Carrying out the Invention

[25] According to an aspect of an exemplary embodiment, a semiconductor package includes a semiconductor chip mounted on a substrate, and a shielding layer covering

at least a portion of the semiconductor chip, where a thickness of a side surface portion of the shielding layer is less than a height of the side surface portion of the shielding layer.

[26] The semiconductor package may include a multi-chip package.

[27] The thickness of the side surface portion of the shielding layer may be less than one fifth of a height of the shielding layer.

[28] An upper surface of the shielding layer forms an angle of substantially 90° with a side surface of the shielding layer.

[29] The shielding layer may include an edge where an upper surface of the shielding layer and a side surface of the shielding layer contact each other, the edge having a predetermined radius of curvature, and the predetermined radius of curvature may be less than a sum of a thickness of the upper surface of the shielding layer and a thickness of the side surface of the shielding layer.

[30] The semiconductor package may further include, between the semiconductor chip and the shielding layer, an insulating layer including a thixotropic material or a hot melt material.

[31] The thixotropic material may include at least one of composite fine silica, bentonite, fine particles of surface treated calcium carbonate, hydrogenated castor oil, metal soap, aluminum stearate, polyamide wax, oxidized polyethylene, and linseed polymerized oil.

[32] The hot melt material may include at least one of polyurethane, polyurea, polyvinyl chloride, polystyrene, acrylonitrile butadiene styrene, polyamide, acrylic, and poly-butylene terephthalate.

[33] The thixotropic material or the hot melt material may be cured by ultraviolet curing or heat curing.

[34] The shielding layer may be a metallic material.

[35] At least one of the shielding layer and the insulating layer may be formed by three-dimensional printing.

[36] The semiconductor package may include an application processor for use in a mobile phone.

[37] According to an aspect of another exemplary embodiment, a semiconductor package includes a semiconductor chip mounted on a substrate, an insulating layer covering at least a portion of the semiconductor chip and where the insulating layer may be a thixotropic material or a hot melt material, and a shielding layer covering the semi-conductor chip and the insulating layer.

[38] The thixotropic material may include at least one of composite fine silica, bentonite, fine particles of surface treated calcium carbonate, hydrogenated castor oil, metal soap, aluminum stearate, polyamide wax, oxidized polyethylene, and linseed polymerized

oil.

[39] The hot melt material may include at least one of polyurethane, polyurea, polyvinyl chloride, polystyrene, acrylonitrile butadiene styrene, polyamide, acrylic, and poly-butylene terephthalate.

[40] The thixotropic material or the hot melt material may be cured by ultraviolet curing or heat curing.

[41] The shielding layer may include a metallic material.

[42] A sum of a thickness of the insulating layer and a thickness of the shielding layer may be less than a height of the insulating layer.

[43] A sum of a thickness of the insulating layer and a thickness of the shielding layer may be less than one fifth of a height of the insulating layer.

[44] The semiconductor package may include at least one of an application processor, a display driver integrated circuit, a timing controller, and a power module integrated circuit.

[45] At least one of the insulating layer and the shielding layer may be formed by three-dimensional printing.

[46] At least one of the insulating layer and the shielding layer may be formed by a material supply device comprising an opening having same shape as a side surface shape of a corresponding one of the insulating layer and the shielding layer.

[47] The insulating layer covers at least a portion of the semiconductor chip.

[48] The semiconductor chip may include a first semiconductor chip and a second semi-conductor chip, the first semiconductor chip and the second semiconductor chip may be aligned on the substrate, and the insulating layer may be interposed between the first semiconductor chip and the second semiconductor chip.

[49] According to an aspect of another exemplary embodiment, a semiconductor package includes a package substrate connected to a printed circuit board via a connection terminal, a plurality of semiconductor chips stacked on the package substrate in a multi-layer structure, an insulating layer covering at least a portion of the plurality of semiconductor chips, and comprising a thixotropic material or a hot melt material, and a shielding layer covering at least a portion of the plurality of semiconductor chips and the insulating layer, wherein a thickness of a side surface portion of the shielding layer is less than a height of the shielding layer.

[50] Each of the plurality of semiconductor chips may include a through-electrode, and each of the plurality of semiconductor chips is connected to at least another of the plurality of semiconductor chips via the through-electrode.

[51] The semiconductor package may further include wires connecting the plurality of semiconductor chips to the package substrate, wherein the wires are configured to transmit electric signals between the plurality of semiconductor chips and the package

substrate.

[52] The thickness of the side surface portion of the shielding layer may be less than one fifth of the height of the shielding layer.

[53] The thixotropic material may include at least one of composite fine silica, bentonite, fine particles of surface treated calcium carbonate, hydrogenated castor oil, metal soap, aluminum stearate, polyamide wax, oxidized polyethylene, and linseed polymerized oil.

[54] The hot melt material may include at least one of polyurethane, polyurea, polyvinyl chloride, polystyrene, acrylonitrile butadiene styrene, polyamide, acrylic, and poly-butylene terephthalate.

[55] At least one of the insulating layer and the shielding layer is formed by a material supply device comprising an opening having same shape as a side surface shape of a corresponding one of the insulating layer and the shielding layer.

[56] According to an aspect of another exemplary embodiment, a semiconductor package includes a printed circuit board, a first semiconductor package formed on the printed circuit board and including a first package substrate connected to the printed circuit board via a first connection terminal and a first semiconductor chip mounted on the first package substrate, a second semiconductor package formed on the first package substrate and including a second package substrate connected to the first package substrate via a second connection terminal and a plurality of second semiconductor chips stacked on the second package substrate as a multi-layer structure, an insulating layer covering at least a portion of a side surface of the first semiconductor package and a side surface of the second semiconductor package and comprising a thixotropic material or a hot melt material; and a shielding layer covering at least a portion of the side surface of the first semiconductor package and an upper surface and the side surface of the second semiconductor package, wherein a thickness of a side surface portion of the shielding layer is less than a height of the shielding layer.

[57] The semiconductor package may further include wires connecting the plurality of second semiconductor chips to the second package substrate, wherein the wires are configured to transmit electric signals between the plurality of second semiconductor chips and the second package substrate.

[58] According to an aspect of another exemplary embodiment, a method of manufacturing a semiconductor package includes, mounting a semiconductor chip on a substrate, forming an insulating layer covering at least a portion of the semiconductor chip, the insulating layer comprising a thixotropic material or a hot melt material, and forming a shielding layer covering at least a portion of the semiconductor chip and the insulating layer.

[59] The thixotropic material may include at least one of composite fine silica, bentonite,

fine particles of surface treated calcium carbonate, hydrogenated castor oil, metal soap, aluminum stearate, polyamide wax, oxidized polyethylene, and linseed polymerized oil.

[60] The hot melt material may include at least one of polyurethane, polyurea, polyvinyl chloride, polystyrene, acrylonitrile butadiene styrene, polyamide, acrylic, and poly-butylene terephthalate.

[61] The thixotropic material or the hot melt material may be cured by ultraviolet curing or heat curing.

[62] The shielding layer may include a metallic material.

[63] A sum of a thickness of the insulating layer and a thickness of the shielding layer may be less than a height of the insulating layer.

[64] A sum of a thickness of the insulating layer and a thickness of the shielding layer may be less than one fifth of a height of the insulating layer.

[65] At least one of the insulating layer or the shielding layer may be formed by a material supply device comprising an opening having same shape as a side surface shape of a corresponding one of the insulating layer and the shielding layer.

[66] At least one of the shielding layer and the insulating layer may be formed by three-dimensional printing.

[67] According to an aspect of another exemplary embodiment, a mobile phone includes a communication module configured to receive installation data of an application from a server, a memory module configured to store the received installation data of the application, and an application processors configured to install the application on the mobile phone based on the installation data of the application and to execute the installed application on the mobile phone, wherein at least one of the application processor and the memory module includes a semiconductor package including a semiconductor chip mounted on a substrate, and a shielding layer covering the semiconductor chip, wherein a thickness of a side surface portion of the shielding layer is less than a height of the side surface portion of the shielding layer.

[68] The thickness of the side surface portion of the shielding layer may be less than one fifth of the height of the side surface portion of the shielding layer.

[69] The mobile phone may further include an insulating layer including a thixotropic material or a hot melt material, between the semiconductor chip and the shielding layer.

[70] According to an aspect of another exemplary embodiment, a three-dimensional printer includes a chip transportation unit configured to transport a substrate and a semiconductor chip mounted on the substrate in a first direction, a dispensing head unit configured to form a shielding layer and an insulating layer by injecting a shielding material and an insulating material on to an upper surface and a side surface of the

semiconductor chip, respectively, via a dispensing process, and a head transportation unit configured to transport the dispensing head unit in the first direction, a second direction perpendicular to the first direction, and a third direction perpendicular to each of the first direction and the second direction. Each of the shielding material and the insulating material includes a thixotropic material or a hot melt material, and a sum of a thickness of a side surface portion of the shielding layer and a thickness of a side surface portion of the insulating layer is less than a height of the side surface portion of the shielding layer.

[71] The dispensing head unit may include a first injection pump configured to hold the shielding material having a thixotropic or a hot melt property, and a first nozzle configured to form the shielding layer by injecting the shielding material on to the upper surface of the semiconductor chip and coating the upper surface of the semiconductor chip with the shielding material.

[72] The dispensing head unit may include a second injection pump configured to hold the insulating material having a thixotropic or a hot melt property, and a second nozzle configured to form the insulating layer by injecting the insulating material on to the side surface of the semiconductor chip.

[73] The three-dimensional printer may further include a light source configured to cure the shielding material and the insulating material by heat curing or ultraviolet curing.

Mode for the Invention

[74] This application claims the benefit of Korean Patent Application No. 10-2015-0003469, filed on January 9, 2015, and Korean Patent Application No.10-2015-0088717, filed on June 22, 2015 in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

[75] Various embodiments of the disclosure will now be described more fully with reference to the accompanying drawings, in which elements of the various embodiments are shown. The present disclosure may be embodied in many different forms and should not be construed as being limited to the exemplary embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to one of ordinary skill in the art. Like reference numerals refer to like elements throughout. In the drawings, the thicknesses of layers and regions and the sizes of components may be exaggerated for clarity. It should also be understood that detailed drawings showing every detail may not be feasible. Accordingly, when an element is shown, it should be understood that it may be an approximation or an agglomeration. For example, if a contact pad is shown, that contact pad may represent numerous separate contact pads.

[76] It will be understood that when an element, such as a layer, a region, or a substrate, is

referred to as being "on," "connected to" or "coupled to" another element, it may be directly on, connected to, or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly on," "directly connected to" or "directly coupled to" another element or layer, there are no intervening elements or layers present. Other words used to describe the relationship between elements or layers should be interpreted in a like fashion (e.g., "between" versus "directly between," "adjacent" versus "directly adjacent," etc.).

[77] It will be understood that, although the terms first, second, third, etc. may be used to describe various elements, components, regions, layers, and/or sections, these elements, components, regions, layers, and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer, or section from another region, layer, or section. Thus, a first element, component, region, layer, or section discussed below could be termed a second element, component, region, layer, or section without departing from the teachings of exemplary embodiments.

[78] As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising" used herein specify the presence of stated features, integers, steps, operations, members, components, and/or groups thereof, but do not preclude the presence or addition of one or more other features, integers, steps, operations, members, components, and/or groups thereof. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. Expressions such as "at least one of," when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list.

[79] Unless otherwise defined in this disclosure, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which exemplary embodiments belong.

[80] Hereinafter, exemplary embodiments of the present disclosure will be described in detail.

[81] FIG. 1 is a cross-sectional view of a semiconductor package 100 according to an exemplary embodiment. Referring to FIG. 1, the semiconductor package 100 is bonded via contact pads 150 and 151 to an upper surface of a package substrate 140. The contact pad 150 may be formed to ground a semiconductor chip 130, and the contact pad 151 may be formed to ground the semiconductor chip 130 or to transmit a signal. Contact pads may also be referred to as connection terminals.

[82] In the semiconductor package 100, the semiconductor chip 130 and an insulating layer 110 may be disposed on the package substrate 140, and the insulating layer 110

may be disposed to be adjacent to the inner side surfaces of a shielding layer 120 and the contact pads 150. Accordingly, the shielding layer 120 may cover the semiconductor chip 130 and the insulating layer 110. The shielding layer 120 may also be connected to the contact pad 150, and the insulating layer 110 may be formed to separate the semiconductor chip 130 and the contact pad 150 from each other.

[83] As used in this disclosure, "cover" does not necessarily mean just being over something. An object ABC covering an object XYZ may generally mean that the object ABC is adjacent to a surface of the object XYZ, regardless of whether ABC is separated from the object XYZ by space or not. Accordingly, ABC may be said to cover XYZ when ABC is under XYZ, next to XYZ, over XYZ, and any combination of ABC being around XYZ.

[84] The semiconductor package 100 may have, for example, a through silicon via (TSV) structure, a multi-chip package (MCP) structure, or a package on package (PoP) structure. Also, the semiconductor package 100 may be included in an application processor, a display driver integrated circuit (IC), a timing controller, or a power module IC. Also, the semiconductor package 100 may be included in a smart phone, a display apparatus, or a wearable device.

[85] If the semiconductor package 100 is mounted in an electronic device (for example, a cellular phone) including the package substrate 140, electromagnetic waves generated by electronic components in the semiconductor package 100 may cause electromagnetic interference (EMI) with other electronic components mounted in the electronic device. Thus, errors may occur in the electronic device with the semiconductor package 100, and the reliability of the product may deteriorate.

[86] The problems of such errors due to stray electromagnetic waves have become even more serious in the case of the semiconductor package 100 that may have several components operating at high speed. Therefore, the shielding layer 120 may reduce the amount of electromagnetic waves emitted during operation of the semiconductor package 100, as well as reduce interference to the semiconductor chip 130 from electromagnetic waves emitted by other semiconductor packages.

[87] However, thickness of the insulating layer 110 or the shielding layer 120 may lead to inefficient degree of integration in a semiconductor package. A ratio of a semiconductor package's height to its area is called an aspect ratio. Referring to FIG. 1, the aspect ratio of the semiconductor package 100 may be obtained by dividing its height ('b'- height from the package substrate 140) by a sum (distance 'a') of a thickness of a side surface portion of the insulating layer 110 and a thickness of a side surface portion of the shielding layer 120. The aspect ratio (r) may be represented by the following equation.

[88] Aspect ratio (r) = b / a [Equation 1]

[89] Accordingly, a low aspect ratio may be a sign of inefficient usage of vertical space for semiconductor chips and/or too inefficient use of horizontal space on the package substrate 140.

[90] Therefore, various implementations may strive to increase the aspect ratio of the semiconductor package 100 so that the relative area occupied by the semiconductor package 100 on the package substrate 140 may decrease, thus increasing the degree of integration.

[91] The shielding layer 120 may be formed on the semiconductor chip 130 as, for example, a rectangular shape. An upper surface of the shielding layer 120 may be formed to be 90° or substantially 90° with respect to a side surface of the shielding layer 120. However, shapes of the shielding layer 120 are not limited thereto.

[92] According to an exemplary embodiment, the aspect ratio of the semiconductor package 100 may be equal to or greater than 1, and higher aspect ratios of 5 or more may be desirable. To realize this, the insulating layer 110 may be formed by using thixotropic material or hot melt material. The thixotropic material or the hot melt material may be injected as a fluid and then cured (or hardened) by ultraviolet (UV) light or heat. In this way. The thixotropic material or the hot melt material in the insulating layer 110 may comprise a metallic material to help shield against EMI.

[93] Various embodiments of the disclosure may form the insulating layer 110 and/or the shielding layer 120 using three-dimensional (3D) printing. Thus, high expenses related to the manufacturing equipment and the time consumed for the manufacturing process may be reduced. Also, according to an exemplary embodiment, the insulating layer 110 or the shielding layer 120 may be formed by a material supply device including an opening having the same shape as the side surface of the insulating layer 110 or the shielding layer 120.

[94] FIGS. 2A and 2B are views for describing a thixotropic material included in a semiconductor package according to an exemplary embodiment.

[95] Referring to FIG. 2A, the thixotropic material is capable of a phase change, between a gel state and a sol state, due to shear stress. For example, if shear stress is applied to the thixotropic material in a gel state, the thixotropic material is changed to a sol state. For example, if time passes without applying shear stress to the thixotropic material, while the thixtropic material remains in the sol state, the thixotropic material is changed to the gel state again.

[96] Referring to FIG. 2B, if shear stress is applied to the thixotropic material, a viscosity of the thixotropic material becomes low so that the thixotropic material becomes to be in a state which is easily changeable, and if the thixotropic material is left during a time lapse in a state in which the shear stress is dismissed, the thixotropic material becomes to have a high viscosity again and restores its original shape. That is, if the

shear stress is applied to the thixotropic material, a net structure of the thixotropic material is destroyed so that the thixotropic material has a low viscosity, and if the shear stress is dismissed, the thixotropic material restores its net structure so as to have a high viscosity.

[97] For example, referring to first curve ①, when shear stress is applied to the thixotropic material in a sol state, a change of viscosity is little. Referring to second curve ②, when shear stress is applied to the thixotropic material in a gel state, a change of viscosity is great. Also, according to a time lapse Δtime, the thixotropic material may be changed from a state of first curve ① to a state of second curve ②. That is, the viscosity of the thixotropic material may be changed according to a time lapse Δtime and a strength of shear stress.

[98] The thixotropic material may be realized by adding a thixotropic additive to a high viscosity material. For example, the thixotropic material may be realized by adding the materials mentioned in the description of FIG. 1 (for example, composite fine silica, bentonite, fine particles of surface treated calcium carbonate, hydrogenated castor oil, metal soap, aluminum stearate, polyamide wax, oxidized polyethylene, and linseed polymerized oil.

[99] An insulating layer is formed by using a material having a low viscosity, to which shear stress is applied, and the insulating layer may be cured by UV curing or heat curing.

[100] FIG. 3 is a cross-sectional view of a semiconductor package 100a according to an exemplary embodiment. Referring to FIG. 3, the semiconductor package 100a may be mounted on an upper surface of the package substrate 140a via contact pads 150a and 151a. The semiconductor package 100a may comprise a shielding layer 120a covering the semiconductor chip 130a. The semiconductor package 100a may be similar to the semiconductor package 100 of FIG. 1. The aspect ratio for the semiconductor package 100a is shown as: r = b'/a'. Note that there is no insulating layer as in FIG. 1, so the aspect ratio may be bigger than for the semiconductor package of FIG. 1 if the height b' is the same as the height b.

[101] According to an exemplary embodiment, the aspect ratio of the semiconductor package 100a may be equal to or greater than 1, and in various embodiments the aspect ratio of the semiconductor package 100a may be equal to or greater than 5. Accordingly, miniaturization of components may be possible, and so various products that use these components may be made smaller.

[102] FIG. 4 is a cross-sectional view of a semiconductor package 100b according to an exemplary embodiment. Referring to FIG. 4, the semiconductor package 100b may be realized as a PoP structure.

[103] In the semiconductor package 100b, semiconductor chips 131b and 132b and an in-

sulating layer 110b may be disposed on a package substrate 140b, and the insulating layer 110b may be disposed to be adjacent to the inner side surfaces of a shielding layer 120b and the contact pads 150b. Accordingly, the shielding layer 120b may cover the semiconductor chips 131b and 132b and the insulating layer 110b. The package substrate 140b and the semiconductor chip 132b may be connected to each other via contact pads 151b. The semiconductor chip 131b and the semiconductor chip 132b may be connected to each other via contact pads 152b.

[104] According to an exemplary embodiment, the semiconductor chips 131b and 132b may be an application processor, a central processing unit (CPU), a controller, or an application specific integrated circuit (ASIC), which may be used in a mobile phone.

[105] Each of the contact pads 151b and 152b may be used to transmit signals between the semiconductor chips 131b and 132b. Alternatively, any of the contact pads 151b and 152b may be used to ground the semiconductor chips 131b and 132b, respectively.

[106] The insulating layer 110b and the shielding layer 120b of the semiconductor package 100b of the PoP structure may be realized by 3D printing, and thus, EMI shielding is possible on a chip level. Thus, a high aspect ratio of the semiconductor package 100b may be realized, which may contribute to a high integration of the semiconductor package 100b.

[107] The insulating layer 110b may be formed by using a thixotropic material or a hot melt material, like the insulating layer 110 of FIG. 1. The thixotropic material or the hot melt material may be in a fluid state so that it may be easily injected via a dispenser, and then the thixotropic material or the hot melt material may be UV cured or heat cured to harden it. Also, the insulating layer 110b may be a metallic material. The insulating layer 110b may be formed of the metallic material in order to increase the EMI reduction effect.

[108] FIG. 5 is a cross-sectional view of a semiconductor package 100c according to an exemplary embodiment. Referring to FIG. 5, the semiconductor package 100c may be realized as a PoP structure.

[109] In the semiconductor package 100c, semiconductor chips 131c and 132c may be disposed on a package substrate 140c. The package substrate 140c and the semiconductor chip 132c may be connected to each other via contact pads 151c. The semiconductor chips 131c and 132c may be connected to each other via contact pads 152c. Also, a shielding layer 120c may cover the semiconductor chips 131c and 132c.

[110] Each of the contact pads 151c and 152c may be used to transmit signals between the semiconductor chips 131c and 132c. Alternatively, any of the contact pads 151c and 152c may also be used to ground the semiconductor chips 131c and 132c, respectively.

[111] The shielding layer 120c of the semiconductor package 100c of the PoP structure may be realized by 3D printing so that a high aspect ratio of the semiconductor

package 100c can be realized. Thus, EMI shielding is possible on a chip level. The high aspect ratio may contribute to high integration.

[112] FIG. 6 is a cross-sectional view of a semiconductor package 100d according to an exemplary embodiment. Referring to FIG. 6, the semiconductor package 100d may be realized as an MCP structure including the semiconductor chips 131d and 132d.

[113] The semiconductor package 100d may include the semiconductor chip 131d and the semiconductor chip 132d disposed on a substrate 140d. The substrate 140d may be formed based on any one of, for example, a silicon substrate, a ceramic substrate, a printed circuit board (PCB), an organic substrate, and an interposer substrate. The semiconductor chip 131d and the semiconductor chip 132d may be the same type of semiconductor chips, or they may be different types of semiconductor chips. For example, each of the semiconductor chips 131d and 132d may be any one of an application processor, a CPU, a controller, and an ASIC that may be used, for example, in a mobile phone. The semiconductor chip 131d and the semiconductor chip 132d may be on the substrate 140d and may be connected to the substrate 140d via contact pads 151d and contact pads 152d, respectively. Also, a shielding layer 120d may cover the semiconductor chip 131d and the semiconductor chip 132d.

[114] The contact pads 151d and 152d may be used to transmit an electrical signal to the semiconductor chip 131d and the semiconductor chip 132d, respectively. Contact pads 150d may be used to ground the semiconductor chip 131d and the semiconductor chip 132d.

[115] An insulating layer 110d may be disposed on the substrate 140d and disposed to be adjacent to the inner side surfaces of the shielding layer 120d and the contact pads 150d. An insulating layer 112d may be disposed on the substrate 140d to be between the semiconductor chip 131d and the semiconductor chip 132d. The insulating layers 110d and 112d may be formed by using a thixotropic material or a hot melt material, and the thixotropic material or the hot melt material may be UV cured or heat cured.

[116] According to an exemplary embodiment, the aspect ratio of the semiconductor package 100d may be equal to or greater than 1, and in various embodiments the aspect ratio of the semiconductor package 100d may be equal to or greater than 5. The shielding layer 120d of the semiconductor package 100d may be realized by 3D printing so a high aspect ratio of the semiconductor package 100d is realized. Thus, the EMI shielding is possible on a chip level. The high aspect ratio may contribute to high integration.

[117] FIG. 7 is a cross-sectional view of a semiconductor package 100e according to an exemplary embodiment. Referring to FIG. 7, the semiconductor package 100e may be realized as an MCP structure including a plurality of semiconductor chips 131e, 132e, and 133e stacked in a multi-layer structure.

[118] The semiconductor package 100e may include an insulating layer 110e, a shielding layer 120e, the plurality of semiconductor chips 131e, 132e, and 133e, a package substrate 140e, contact pads 151e, and a PCB 160e. The plurality of semiconductor chips 131e, 132e, and 133e may be stacked on the package substrate 140e, and the package substrate 140e may be connected to the PCB 160e via the contact pads 151e. Accordingly, the semiconductor package 100e may be formed as a multi-layer structure. The plurality of semiconductor chips may include the semiconductor chip 131e, the semiconductor chip 132e, and the semiconductor chip 133e. However, the number of semiconductor chips in a stack need not be limited to three, but may be any number suitable for a design or implementation purpose.

[119] According to an exemplary embodiment, the semiconductor chips 131e, 132e, and 133e may be the same type of semiconductor chips. For example, the semiconductor chips 131e, 132e, and 133e may be application processors used in a mobile phone. Each of the semiconductor chips 131e, 132e, and 133e may include through electrodes 153e for exchanging electrical signals with one another.

[120] A first interlayer insulating layer 171e may be interposed between the package substrate 140e and the semiconductor chip 131e. A second interlayer insulating layer 172e may be interposed between the semiconductor chip 131e and the semiconductor chip 132e, and a third interlayer insulating layer 173e may be interposed between the semiconductor chip 132e and the semiconductor chip 133e. Contact pads 152e may be disposed between the package substrate 140e and the semiconductor chips 131e, 132e, and 133e, in order to electrically connect the package substrate 140e and the semiconductor chips 131e, 132e, and 133e.

[121] Contact pads 150e may be used to ground the semiconductor chips 131e, 132e, and 133e. The contact pads 151e may be used to electrically connect the PCB 160e and the package substrate 140e. The contact pads 151e may be formed, for example, by a ball grid array (BGA) method, such as a solder ball. Contact pads 154e may be formed between the package substrate 140e and the contact pads 151e, and may be used to electrically connect between the PCB 160e and the package substrate 140e.

[122] The insulating layer 110e may be disposed on the PCB 160e and adjacent to the inner side surfaces of the shielding layer 120e and the contact pads 150e. The insulating layer 110e may be formed by using a thixotropic material or a hot melt material, like the insulating layer 110 of FIG. 1. Also, the thixotropic material or the hot melt material may be UV cured or heat cured.

[123] The shielding layer 120e may be formed to cover an upper surface of the semiconductor chip 133e disposed on the uppermost level from among the semiconductor chips 131e, 132e, and 133e, and a side surface of the insulating layer 110e. A molding unit 112e may be formed between the semiconductor chips 131e, 132e, and 133e and

the insulating layer 110e, and between the semiconductor chips 131e, 132e, and 133e and the shielding layer 120e. The molding unit 112e may be formed by using an epoxy-based material, a thermosetting material, a thermoplastic material, a UV-processed material, etc. In FIG. 7, an aspect ratio may be the height (b") of the shielding layer 120e divided by the thicknesses (a") of side surface portions of the insulating layer 110e and the shielding layer 120e. When the aspect ratio of the semiconductor package 100e is high, an area occupied by the semiconductor package 100e on the PCB 160e may decrease, and this decrease may increase a degree of integration of the semiconductor package 100e. According to an exemplary embodiment, the aspect ratio of the semiconductor package 100e may be equal to or greater than 1, and in various embodiments the aspect ratio of the semiconductor package 100e may be equal to or greater than 5.

[124] The shielding layer 120e of the semiconductor package 100e of the MCP structure may be realized by 3D printing, and thus, a high aspect ratio of the semiconductor package 100e may be realized. Thus, the EMI shielding is possible on a chip level. The high aspect ratio may contribute to high integration.

[125] While the semiconductor chips 131e, 132e, and 133e may have been described with through electrodes 153e next to the chips, the various embodiments need not be so limited. Various well known methods may be used to interconnect the semiconductor chips 131e, 132e, and 133e to each other as well as to the contact pads 151e. For example, there may be connections from one chip to another through the insulating layers separating the chips.

[126] FIG. 8 is a cross-sectional view of a semiconductor package 100f according to an exemplary embodiment.

[127] Referring to FIG. 8, the semiconductor package 100f may be realized as an MCP structure including the semiconductor chips 131f, 132f, and 133f, which are stacked in a multi-layer structure. A first interlayer insulating layer 171f may be interposed between the package substrate 140f and the semiconductor chip 131f. A second interlayer insulating layer 172f may be interposed between the semiconductor chip 131f and the semiconductor chip 132f, and a third interlayer insulating layer 173f may be interposed between the semiconductor chip 132f and the semiconductor chip 133f.

[128] The semiconductor chip 132f may be electrically connected to and may exchange signals with the package substrate 140f via the wire 181f. Likewise, the semiconductor chip 133f may be electrically connected to and may exchange signals with the package substrate 140f via the wire 182f. The plan areas of the semiconductor chips 131f, 132f, and 133f may be different from one another. The plan area of the semiconductor chip 131f may be greater than the plan area of the semiconductor chip 132f, and the plan area of the semiconductor chip 132f may be greater than the plan area of the semi-

conductor chip 133f. However, the plan areas of the semiconductor chips 131f, 132f, and 133f are not limited thereto.

[129] The semiconductor package 100f may be similar to the semiconductor package 100e, and hence many components that are similar will not be described in detail. The semiconductor package 100f may include an insulating layer 110f, a shielding layer 120f, the semiconductor chips 131f, 132f, and 133f, a package substrate 140f, contact pads 150f, 151f, 154f, and a PCB 160f that are similar to corresponding parts of the semiconductor package 100e.

[130] A molding unit 112f similar to the molding unit 112e may fill the inner space where the semiconductor chips 131f, 132f, and 133f are disposed between the shielding layer 120f and the package substrate 140f. The molding unit 112f may be formed by using an epoxy-based material, a thermosetting material, a thermoplastic material, a UV-processed material, etc.

[131] The semiconductor package 100f of FIG. 8 differs from the semiconductor package 100e of FIG. 7 in that plan areas of the semiconductor chips 131f, 132f, and 133f are different from one another, and the semiconductor chips 132f and 133f are electrically connected to the package substrate 140f via wires 181f and 182f, respectively.

[132] Aside from the wires 181f and 182f, the semiconductor chips 131f, 132f, and 133f may communicate with each other and to the package substrate 140f via various well known methods. For example, there may be connections from one chip to another or to the package substrate 140f through the insulating layers separating them.

[133] FIG. 9 is a cross-sectional view of a semiconductor package 100g according to an exemplary embodiment. Referring to FIG. 9, the semiconductor package 100g may be realized as a PoP structure.

[134] The semiconductor package 100g may include a PCB 160g, a first semiconductor package 131g formed on the PCB 160g, and a second semiconductor package 132g formed on the first semiconductor package 131g.

[135] The first semiconductor package 131g may include a first package substrate 140g, and a semiconductor chip 130g mounted on the first package substrate 140g. The first package substrate 140g may be electrically connected to the PCB 160g via contact pads 151g and 154g. The semiconductor chip 130g may be a microprocessor such as, for example, a CPU, a controller, or an ASIC. According to an exemplary embodiment, the semiconductor chip 130g may be an application processor used in a mobile phone or a smartphone. The semiconductor chip 130g may exchange electrical signals with the PCB 160g and other devices connected to the PCB 160g, via the contact pads 151g.

[136] The second semiconductor package 132g may include a second package substrate 142g, semiconductor chips 135g and 136g mounted on the second package substrate 142g, contact pads 152g and 153g, and wires 181g and 182g. Although it is illustrated

with two semiconductor chips 135g and 136g, it is not limited thereto. Three or more semiconductor chips may be stacked as a multi-layer structure. The semiconductor chips 135g and 136g may be the same type of semiconductor chips. The semiconductor chips 135g and 136g may be, for example, at least one of dynamic random-access memory (DRAM), static random-access memory (SRAM), flash memory, electrically erasable programmable read-only memory (EEPROM), parameter random-access memory (PRAM), magnetoresistive random-access memory (MRAM), and resistive random-access memory (RRAM).

[137] A first interlayer insulating layer 171g may be interposed between the semiconductor chip 135g and the second package substrate 142g, and a second interlayer insulating layer 172g may be interposed between the semiconductor chip 135g and the semiconductor chip 136g. The semiconductor chips 135g and 136g may be electrically connected to the second package substrate 142g via the wire 181g and the wire 182g, respectively.

[138] Contact pads 153g may be used to electrically connect between the first package substrate 140g and the second package substrate 142g. The contact pads 153g may be formed as a ball grid array.

[139] A ground unit 150g may be used to ground the semiconductor chip 130g and the semiconductor chips 135g and 136g.

[140] An insulating layer 110g may be formed adjacent to the first semiconductor package 131g and the second semiconductor package 132g. In detail, the insulating layer 110g may be formed adjacent to the semiconductor chip 130g and the semiconductor chips 135g and 136g, by being adjacent to a side surface of the first package substrate 140g and a side surface of the second package substrate 142g. The insulating layer 110g may be formed by using a thixotropic material or a hot melt material. Also, the thixotropic material or the hot melt material may be UV cured or heat cured.

[141] A shielding layer 120g may be formed to cover an upper surface of the semiconductor chip 136g and outside surface of the insulating layer 110g. A molding unit 112g may be formed between the semiconductor chips 130g, 135g, and 136g and the insulating layer 110g, and between the semiconductor chips 130g, 135g, and 136g and the shielding layer 120g. The molding unit 112g may be formed by using an epoxy-based material, a thermosetting material, a thermoplastic material, a UV-processed material, etc. According to the exemplary embodiment illustrated in FIG. 9, an aspect ratio may be defined as a value obtained by dividing a height (b''') of the shielding layer 120g by a sum of thicknesses (a''') of side surface portions of the insulating layer 110g and the shielding layer 120g. When the aspect ratio of the semiconductor package 100g is high, a relative area occupied by the semiconductor package 100g on the PCB 160g may decrease, and thus, a degree of integration of the semiconductor package

100g may increase.

[142] The shielding layer 120g of the semiconductor package 100g of the PoP structure may be realized by 3D printing, and thus, the high aspect ratio of the semiconductor package 100g may be realized.

[143] FIG. 10 is a cross-sectional view of a semiconductor package 100h according to an exemplary embodiment.

[144] Referring to FIG. 10, the semiconductor package 100h may be realized as a semiconductor package structure in which a semiconductor chip 130h is mounted on a package substrate 140h as a flip-chip structure. The semiconductor package 100h may include an insulating layer 110h, a shielding layer 120h, the semiconductor chip 130h, the package substrate 140h, a contact pads 150h, and a PCB 160h. The semiconductor package 100h illustrated in FIG. 10 differs from the semiconductor package 100e illustrated in FIG. 7 in that one semiconductor chip 130h is mounted in the flip chip structure. Components of the semiconductor package 100h have the same reference numerals as the components of the semiconductor package 100e, with only different English letters attached to the reference numerals, wherein like reference numerals refer to like elements. Thus, their descriptions will be omitted. The components of the semiconductor package 100h which are the same as the components of FIG. 7 will not be described in detail.

[145] The semiconductor chip 130h may be mounted on the package substrate 140h as the flip-chip structure. The semiconductor chip 130h may be electrically connected to the package substrate 140h via contact pads 152h. The package substrate 140h may be electrically connected to the PCB 160h via contact pads 151h. The semiconductor chip 130h may exchange electrical signals with other devices connected to the PCB 160h via the contact pads 151h and 152h. Contact pads 154h may be disposed between the contact pads 151h and the PCB 160h, and may be used to electrically connect between the PCB 160h and the semiconductor chip 130h via the contact pad 151h.

[146] An under-fill member 114h may be formed between a lower surface of the semiconductor chip 130h and an upper surface of the package substrate 140h and between the connection pads 152h.

[147] The insulating layer 110h may be formed of the same material as the insulating layer 110e illustrated in FIG. 7. The shielding layer 120h may be formed as substantially the same structure as the shielding layer 120e illustrated in FIG. 7. According to the present exemplary embodiment illustrated in FIG. 10, an aspect ratio may be defined as a value obtained by dividing a height (b"") of the shielding layer 120h by a sum of thicknesses (a"") of side surface portions of the insulating layer 110h and the shielding layer 120h. When the aspect ratio of the semiconductor package 100h is high, a relative area occupied by the semiconductor package 100h on the PCB 160h may

decrease, and thus, a degree of integration of the semiconductor package 100h may increase.

[148] FIGS. 11A through 11E are views for describing a manufacturing process of a semiconductor package 1000, according to an exemplary embodiment.

[149] Referring to FIG. 11A, contact pads 150d and 151d may be patterned on a substrate 140d. The substrate 140d may have the contact pads 150d and 151d on an upper surface thereof. For example, the contact pads 150d may be for ground, and the contact pads 151d may be for signal or ground. The substrate 140d may be, for example, a double-sided PCB or a multi-layer PCB.

[150] Referring to FIG. 11B, a semiconductor chip 130d may be disposed on the substrate 140d. Recently, demand for more functionality and smaller portable devices have rapidly increased, and, thus, technology has led to miniaturization and weight reduction of electronic components in the electronic products.

[151] For this purpose, there is needed not only technology for reducing the sizes of the separate components, but also a system on chip (SOC) technology is needed to integrate a plurality of separate components into one chip, or a system in package (SIP) technology is needed for integrating a plurality of separate devices into one package.

[152] In the SIP technology that integrates the plurality of separate devices into one package, the number of semiconductor chips may vary according to the purpose of a semiconductor package. The present disclosure does not limit the number of semiconductor chips in a package to a single number. The number of semiconductor chips may depend on various design and implementation criteria.

[153] Referring to FIG. 11C, the insulating layer 110d may be formed, where the insulating layer 110d may be a thixotropic material or a hot melt material. The thixotropic material may include at least one of, for example, composite fine silica, bentonite, fine particles of surface treated calcium carbonate, hydrogenated castor oil, metal soap, aluminum stearate, polyamide wax, oxidized polyethylene, and linseed polymerized oil.

[154] The hot melt material of the insulating layer 110d may include at least one of, for example, polyurethane, polyurea, polyvinyl chloride, polystyrene, acrylonitrile butadiene styrene (ABS), polyamide, acrylic, and polybutylene terephthalate (PBTP).

[155] Referring to FIG. 11D, the shielding layer 120d may be formed to cover the semiconductor chip 130d. The insulating layer 110d may be interposed between the shielding layer 120d and the semiconductor chip 130d. An edge 120edge of the shielding layer 120d, at which an upper surface and a side surface of the shielding layer 120d meet each other, may be at 90° or substantially 90°. However, various embodiments of the disclosure need not be limited so. According to an exemplary embodiment, the edge 120edge of the shielding layer 120d may have a predetermined

radius of curvature.

[156] By forming the shielding layer 120d by using a high index thixotropic material, the shielding layer 120d may be formed by 3D printing, and thus, the edge 120edge of the shielding layer 120d may have a predetermined radius of curvature. A product including any one of the previously described semiconductor packages (100, and 100a through 100h) according to the exemplary embodiments illustrated in FIG. 1 and FIGS. 3 through 10 may be miniaturized and highly integrated. This aspect will be described later with reference to FIGS. 12 through 16.

[157] As illustrated in FIG. 11D, the insulating layer 110d may also be formed on the upper surface of the semiconductor chip 130d. Also, according to another exemplary embodiment, the insulating layer 110d may be formed only on the side surface of the semiconductor chip 130d.

[158] The shielding layer 120 may be formed to reduce EMI due to electromagnetic waves generated by the semiconductor chip 130, and also to reduce EMI on the semiconductor chip 130 by electromagnetic waves generated externally to the semiconductor package 1000.

[159] According to an exemplary embodiment, the insulating layer 110d or the shielding layer 120d may be formed of thixotropic material or hot melt material so that a high aspect ratio is realized by 3D printing illustrated in FIGS. 12 through 16.

[160] FIG. 11E is an enlarged view of the edge portion 120edge of FIG. 11D. Referring to FIG. 11E, an edge 120edge' located at a boundary portion of the shielding layer 120d, at which an upper surface and a side surface of the shielding layer 120d meet each other, may have a radius of curvature 120r, and may have a curvature corresponding to a reciprocal value of the radius of curvature 120r. The radius of curvature 120r may be less than or equal to a thickness 120t of the shielding layer 120d. That is, a maximum value of the radius of curvature 120r may be the same as or less than the thickness 120t of the shielding layer 120d.

[161] According to an exemplary embodiment, the shielding layer 120d is formed by a process in which a high thixotropic material is discharged via a nozzle of a dispenser. Thus, as illustrated in FIG. 11E, the edge 120edge' of the shielding layer 120d may have the predetermined radius of curvature 120r. The method of forming the shielding layer 120d by 3D printing will be described in more detail with reference to FIGS. 12 through 16.

[162] FIG. 12 is a schematic perspective view of a 3D printer 300 that manufactures at least one of the semiconductor packages 100 and 100a through 100h, according to an exemplary embodiment. The 3D printer 300 may form an insulating layer having a high aspect ratio by using a thixotropic material or a hot melt material in each of the semiconductor packages 100 and 100a through 100h. In the illustration of FIG. 12,

components of the 3D printer 300 may be omitted or exaggerated, for convenience of explanation.

[163] Referring to FIG. 12, the 3D printer 300 may include a dispensing head unit 300A, a frame unit 350, a head transportation unit 360, a chip transportation unit 370, and a measuring unit 380. According to an exemplary embodiment, the 3D printer 300 may further include a control unit (not shown) for controlling the dispensing head unit 300A, and the head transportation unit 360 such that the dispensing head unit 300A forms an insulating layer or a shielding layer on a semiconductor chip so that it can have a high aspect ratio.

[164] The frame unit 350 is a fixing unit configured to fix the 3D printer 300, and the dispensing head unit 300A, the head transportation unit 360, the chip transportation unit 370, and the measuring unit 380 may be disposed on the frame unit 350.

[165] The dispensing head unit 300A may dispense appropriate material on to a semiconductor chip in the chip transportation unit 370. The head transportation unit 360 may be connected to the dispensing head unit 300A. The head transportation unit 360 may move the dispensing head unit 300A in a first direction (a direction x), a second direction (a direction y), and a third direction (a direction z). Also, the head transportation unit 360 may rotate the dispensing head unit 300A.

[166] The chip transportation unit 370 may move the semiconductor chip in the second direction (the direction y). The chip transportation unit 370 may move the semiconductor chip, on which the insulating layer and the shielding layer are formed by the dispensing head unit 300A, in the second direction (the direction y), and may move the semiconductor chip, on which the insulating layer and the shielding layer are not yet formed, to be adjacent to the dispensing head unit 300A.

[167] The measuring unit 380 may measure a weight of the semiconductor chip and adjust a location of the semiconductor chip. The measuring unit 380 may include a module for cleansing the nozzles 330 and 332 of the dispensing head unit 300A.

[168] The dispensing head unit 300A may form an insulating layer 210 (refer to FIG. 13) and a shielding layer 220 (refer to FIG. 13) on the semiconductor chip 200. The detailed descriptions will be given with reference to FIG. 13.

[169] FIG. 13 is a view for describing a method of manufacturing at least one of the semiconductor packages 100 and 100a through 100h by using the 3D printer 300 illustrated in FIG. 12, according to an exemplary embodiment. FIG. 13 is a view of the dispensing head unit 300A illustrated in FIG. 12, which is conceptually schematized for convenience of explanation.

[170] Referring to FIG. 13, a contact pad 230 may be connected to a contact pad 240 connected to an internal circuit of a semiconductor chip 200. According to an exemplary embodiment, the contact pad 240 may be a metal ball grid array, which is

solderable. Also, the contact pad 230 may be formed by a high temperature soldering reflow with respect to a circuit pattern formed on a package substrate.

[171] The shielding layer 220 may be formed on an upper surface of the semiconductor chip 200 by injecting shielding material into the injection unit 320 by using the pump structure 310. According to an exemplary embodiment, the shielding material may be thixotropic material or hot melt material. The shielding layer 220 may be formed by a dispensing process in which the shielding material is injected via the injection unit 320, and thus, the shielding layer 220 may have a square shape including an edge having a predetermined radius of curvature (refer to FIG. 11E).

[172] Also, the insulating layer 210 may be formed on a side surface of the semiconductor chip 200 by injecting an insulating material into the injection unit 322 of the pump structure 312. The insulating material may be thixotropic material or hot melt material.

[173] According to an exemplary embodiment, the shielding material and the insulating material may be heat cured or UV cured via a light source 340.

[174] FIG. 14 is a view for describing a method of manufacturing at least one of the semiconductor packages 100 and 100a through 100h by using the 3D printer 300 illustrated in FIG. 12, according to an exemplary embodiment. FIG. 14 is a cross-sectional view for describing in detail an operation of the second pump structure 312 illustrated in FIG. 13.

[175] Referring to FIG. 14, the second pump structure 312 may include an injection unit 322, a pipe 324, an auger pump 326, a rotation ring 328, and a nozzle 332. An insulating material 210' may be loaded in the injection unit 322, and the insulating material 210' may flow into the rotation ring 328 via the pipe 324 by a pressure applied from the outside. The insulating material 210' may be thixotropic material or hot melt material.

[176] The insulating material 210' may flow into an opening in the rotation ring 328, and may form the insulating layer 210 on the side surface of the semiconductor chip 200 via the nozzle 332. The rotation ring 328 may rotate according to a rotational force of the auger pump 326, and may discharge the insulating material in a direction of the nozzle 332 via a pressure generated due to the rotation of the auger pump 326.

[177] According to an exemplary embodiment, shielding material may also be dispensed by a 3D printer 300. The shielding material may be formed of thixotropic material or hot melt material. This aspect will be described in detail with reference to FIGS. 15A to 16.

[178] FIGS. 15A and 15B are views for describing a method of manufacturing at least one of the semiconductor packages 100 and 100a through 100h by using the 3D printer 300 illustrated in FIG. 12, according to an exemplary embodiment. The dispensing head unit 300A (refer to FIG. 12) may include a nozzle 330' and a coating dispenser 334.

[179] Referring to FIG. 15A, an upper surface portion of the semiconductor chip 200 may be coated with thixotropic material or hot melt material via the coating dispenser 334, and a side surface portion of the semiconductor chip 200 may be coated with thixotropic material or hot melt material, by using the nozzle 330'. An edge at which the upper surface portion and the side surface portion of the semiconductor chip 200 meet each other may have a curvature. FIG. 15B is an enlarged view of portion A15 of FIG. 15A.

[180] Referring to FIG. 15B, the side surface portion of the semiconductor chip 200 may be coated with thixotropic material or hot melt material by using the nozzle 330' with an opening 336 at its side surface.

[181] Also, according to an exemplary embodiment, the insulating layer or the shielding layer may be formed by a material supply device including an opening 336 having the same shape as a side surface of the insulating layer or the shielding layer. For example, the opening 336 may have a slit shape. The opening 336 may have various shapes according to necessity. 3D printing may be easily performed on the side surface portion by using the opening 336 of the side surface.

[182] FIGS. 16A and 16B are views for describing a method of manufacturing a semiconductor package, according to an exemplary embodiment. FIGS. 16A and 16B are views of a method of forming thixotropic materials 210a, 210b, 212a, and 212b on semiconductor chips 200a and 200b by using nozzles 330a and 330b of the 3D printer 300 illustrated in FIG. 12.

[183] Referring to FIG. 16A, the nozzle 330a may be used to dispense the thixotropic materials 210a and 212a on the semiconductor chip 200a. For example, the thixotropic material 210a may have low viscosity via a high shear stress, and the thixotropic material 212a may have high viscosity via a low shear stress.

[184] Referring to FIG. 16B, the nozzle 330b may be used to dispense the thixotropic materials 210b and 212b on the semiconductor chip 200b. For example, the thixotropic material 210b may have low viscosity via a high shear stress, and the thixotropic material 212b may have a high viscosity via a low shear stress.

[185] The thixotropic materials 210a, 210b, 212a, and 212b may be formed as layers as illustrated in FIGS. 16A and 16B. Also, the case of FIG. 16B may realize a higher thixotropic property than the case of FIG. 16A. Thus, the case of FIG. 16B may realize a higher aspect ratio than the case of FIG. 16B, due to the higher thixotropic property.

[186] FIG. 17 is a schematic view of a structure of a semiconductor package 1100 according to an exemplary embodiment.

[187] Referring to FIG. 17, the semiconductor package 1100 may include a micro-processing unit 1110, memory module 1120, an interface 1130, a graphic-processing unit 1140, function blocks 1150, and a bus 1160 connecting the micro-processing unit

1110, the memory module 1120, the interface 1130, the graphic-processing unit 1140, and the function blocks 1150. The semiconductor package 1100 may include both the micro-processing unit 1110 and the graphics-processing unit 1140, or the semiconductor package 1100 may include only one of the micro-processing unit 1110 and the graphics-processing unit 1140.

[188] The micro-processing unit 1110 may include a core processor and a level-2 (L2) cache. For example, the micro-processing unit 1110 may include a multiple processing units. Each of the multiple processing units may have the same or different performance. Also, the multiple processing units may be simultaneously active or may be active at different times. The memory module 1120 may comprise one or more memory chips and may store, for example, a process result of the function blocks 1150 under a control of the micro-processing unit 1110. The interface 1130 may allow the semiconductor package 1100 to interface with external devices. For example, the interface 1130 may interface with a camera, a liquid crystal display (LCD), a speaker, etc.

[189] The graphics-processing unit 1140 may perform graphic functions such as, for example, video encoding and decoding or 3D graphics.

[190] The function blocks 1150 may perform various functions. For example, when the semiconductor package 1100 is an AP used in a mobile device, some of the function blocks 1150 may perform communication functions.

[191] The semiconductor package 1100 may be at least one of the semiconductor packages 100 and 100a through 100h described with reference to FIGS. 1 through 10. The micro-processing unit 1110 and/or the graphics-processing unit 1140 may be at least one of the semiconductor chips 130 and 130a through 130h illustrated with reference to FIGS. 1 through 10. The memory module 1120 may be at least one of the semiconductor chips 130 and 130a through 130h illustrated with reference to FIGS. 1 through 10.

[192] The interface 1130 and the function blocks 1150 may correspond to some of the semiconductor chips 130 and 130a through 130h illustrated with reference to FIGS. 1 through 10.

[193] The semiconductor package 1100 may include the micro-processing unit 1110 and/or the graphics-processing unit 1140, together with the memory module 1120. Also, since the semiconductor package 1100 may rapidly discharge EMI generated in the micro-processing unit 1110 and/or the graphics-processing unit 1140 to the outside of the semiconductor package 1100, a partial heat concentration phenomenon which may occur in the semiconductor package 1100 may be prevented. Thus, the operational reliability of the semiconductor package 1100 may be improved and the semiconductor package 1100 may have higher capacity, higher performance, and higher reliability.

[194] FIG. 18 is a view of an electronic system 1200 including a semiconductor package, according to an exemplary embodiment.

[195] Referring to FIG. 18, a micro-processing unit (MPU)/graphics-processing unit (GPU) 1210 may be mounted in the electronic system 1200. The electronic system 1200 may be, for example, a mobile device, a desk top computer, or a server. Also, the electronic system 1200 may further include a memory device 1220, an input/output device 1230, and a display device 1240, which may be electrically connected to a bus 1250. The MPU/GPU 1210 and the memory device 1220 may be at least one of the semiconductor packages 100 and 100a through 100h described with reference to FIGS. 1 through 10.

[196] FIG. 19 is a schematic perspective view of an electronic device including a semiconductor package 1310.

[197] FIG. 19 illustrates an example in which the electronic system 1200 is applied to a mobile phone 1300. According to an exemplary embodiment, the mobile phone 1300 may be a smartphone including a function of installing and executing an application. The mobile phone 1300 may include a communication module for receiving installation data of an application, a memory module for storing the installation data of the application, and an application processor (AP) for installing the application based on the installation data of the application and executing the installed application. The AP may include an MPU or a GPU. The application processor and/or the memory may include the semiconductor package 1310. The semiconductor package 1310 may be at least one of the semiconductor packages 100 and 100a through 100a described with reference to FIGS. 1 through 10.

[198] The mobile phone 1300 may include the semiconductor package 1310, which includes a high performance application processor and a high capacity memory device, while having a high reliability, and thus, the mobile phone 1300 may be miniaturized and may have high performance.

[199] In addition, the electronic system 1200 may be applied to portable laptop computers, MP3 players, navigation devices, solid state disks (SSD), automobiles, or household appliances.

[200] It should be understood that exemplary embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each exemplary embodiment should typically be considered as available for other similar features or aspects in other exemplary embodiments.

[201] While one or more exemplary embodiments have been described with reference to the figures, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and

scope as defined by the following claims.

Claims

[Claim 1] A semiconductor package comprising:
a semiconductor chip mounted on a substrate; and
a shielding layer covering at least a portion of the semiconductor chip,
wherein a thickness of a side surface portion of the shielding layer is less than a height of the side surface portion of the shielding layer.

[Claim 2] The semiconductor package of claim 1, wherein the semiconductor package comprises a multi-chip package.

[Claim 3] The semiconductor package of claim 1, wherein the thickness of the side surface portion of the shielding layer is less than one fifth of a height of the shielding layer.

[Claim 4] The semiconductor package of claim 1, wherein an upper surface of the shielding layer forms an angle of substantially 90° with a side surface of the shielding layer.

[Claim 5] The semiconductor package of claim 1, wherein the shielding layer comprises an edge whereon an upper surface of the shielding layer and a side surface of the shielding layer contact each other, the edge having a predetermined radius of curvature less than a sum of a thickness of the upper surface of the shielding layer and a thickness of the side surface of the shielding layer.

[Claim 6] The semiconductor package of claim 1, further comprising, between the semiconductor chip and the shielding layer, an insulating layer comprising a thixotropic material or a hot melt material.

[Claim 7] The semiconductor package of claim 6, wherein the shielding layer comprises a metallic material.

[Claim 8] The semiconductor package of claim 6, wherein at least one of the shielding layer and the insulating layer is formed by three-dimensional printing.

[Claim 9] A method of manufacturing a semiconductor package, the method comprising:
mounting a semiconductor chip on a substrate;
forming an insulating layer covering at least a portion of the semiconductor chip, the insulating layer comprising a thixotropic material or a hot melt material; and
forming a shielding layer covering at least a portion of the semiconductor chip and the insulating layer.

[Claim 10] The method of claim 9, wherein the thixotropic material or the hot melt

material is cured by ultraviolet curing or heat curing.

[Claim 11] The method of claim 9, wherein the shielding layer comprises a metallic material.

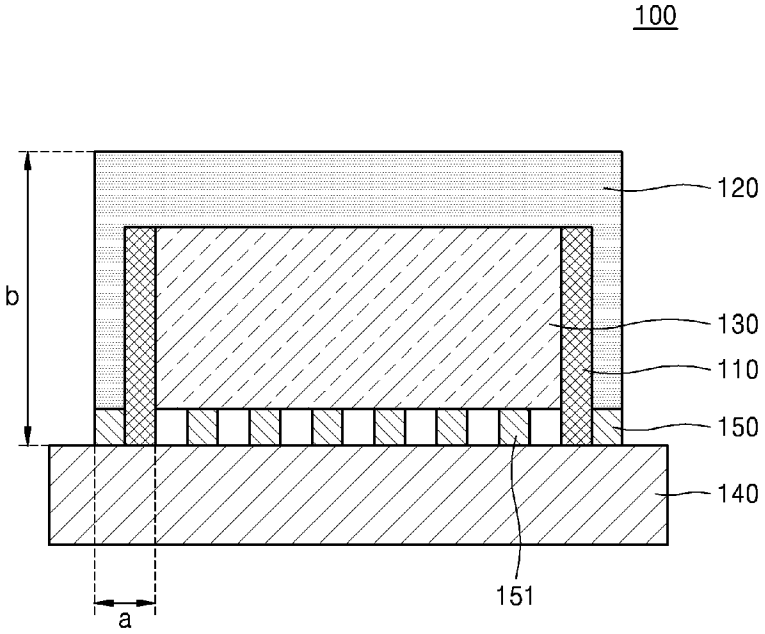
[Claim 12] The method of claim 9, wherein a sum of a thickness of the insulating layer and a thickness of the shielding layer is less than a height of the insulating layer.

[Claim 13] The method of claim 9, wherein a sum of a thickness of the insulating layer and a thickness of the shielding layer is less than one fifth of a height of the insulating layer.

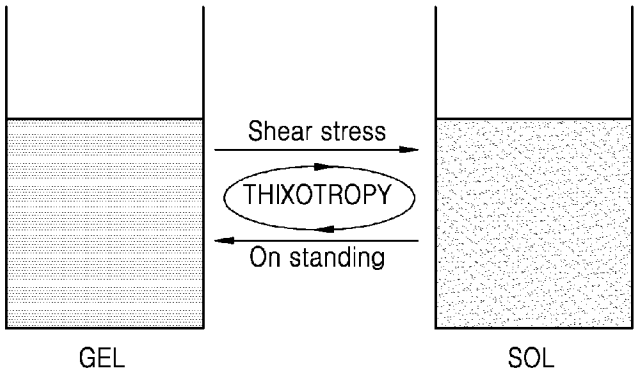
[Claim 14] The method of claim 9, wherein at least one of the insulating layer or the shielding layer is formed by a material supply device comprising an opening having same shape as a side surface shape of a corresponding one of the insulating layer and the shielding layer.

[Claim 15] The method of claim 9, wherein at least one of the shielding layer and the insulating layer is formed by three-dimensional printing.

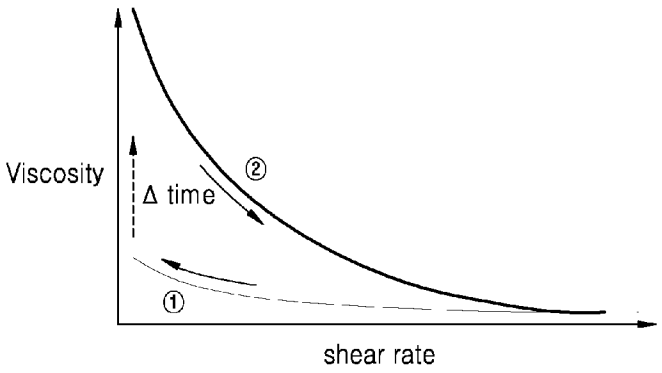
[Fig. 1]


100
120
130
110
150
140
151
b
a

[Fig. 2]

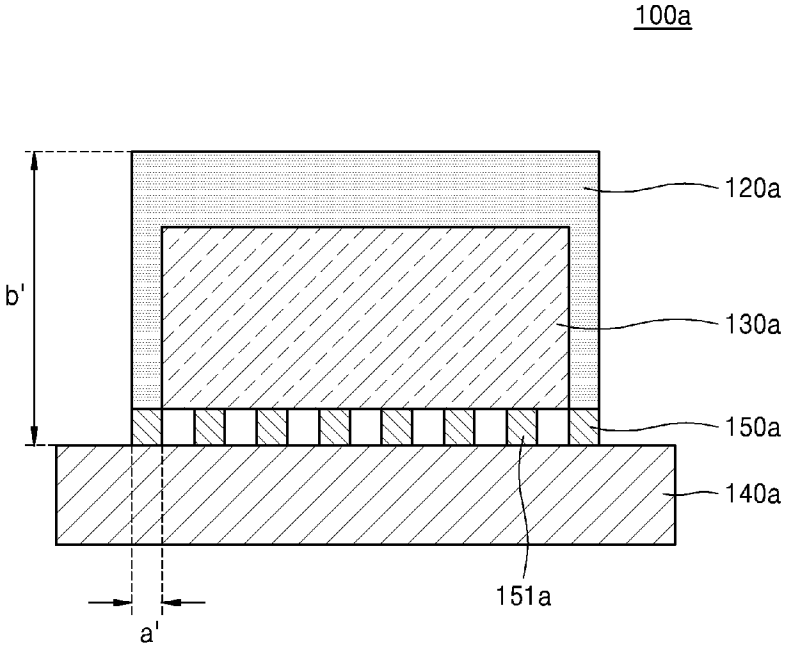

Shear stress
THIXOTROPY
On standing
GEL
SOL

(a)

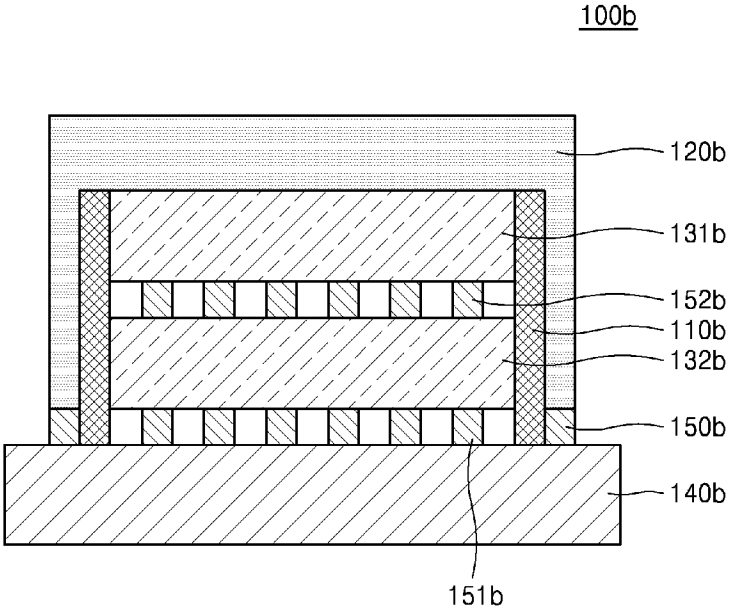

Viscosity
Δ time
②
①
shear rate

(b)

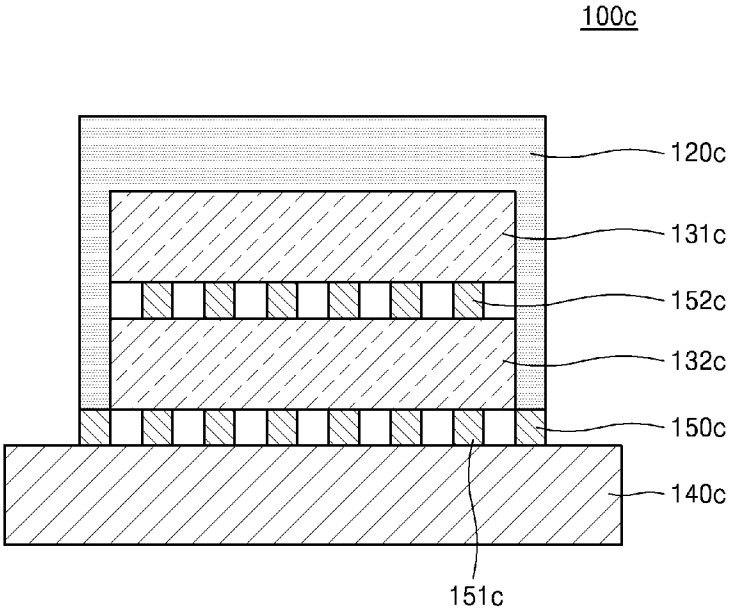
[Fig. 3]



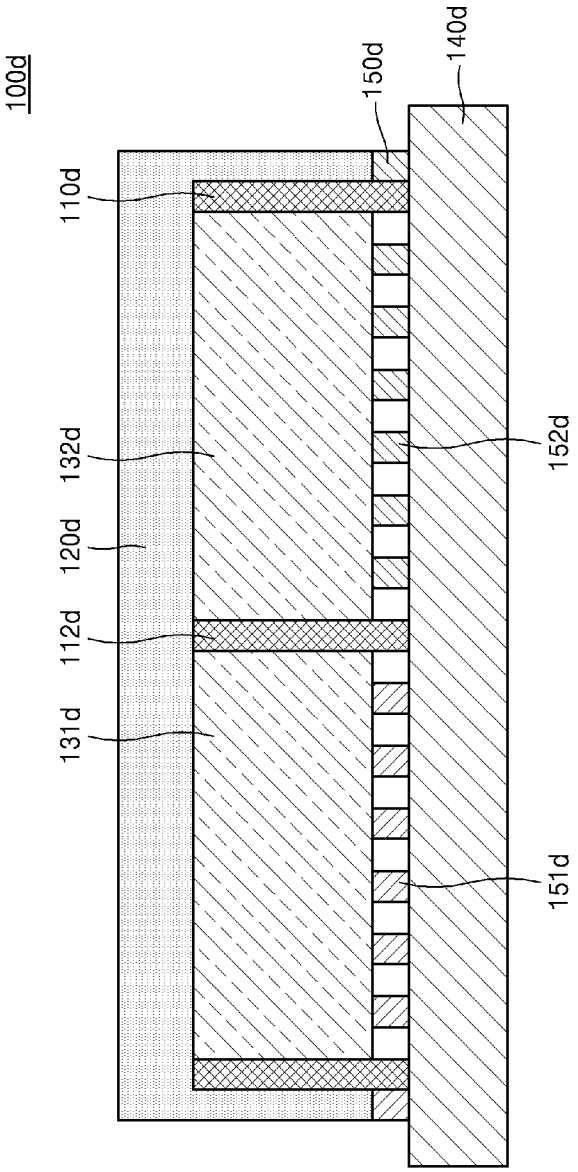
[Fig. 4]



[Fig. 5]



[Fig. 6]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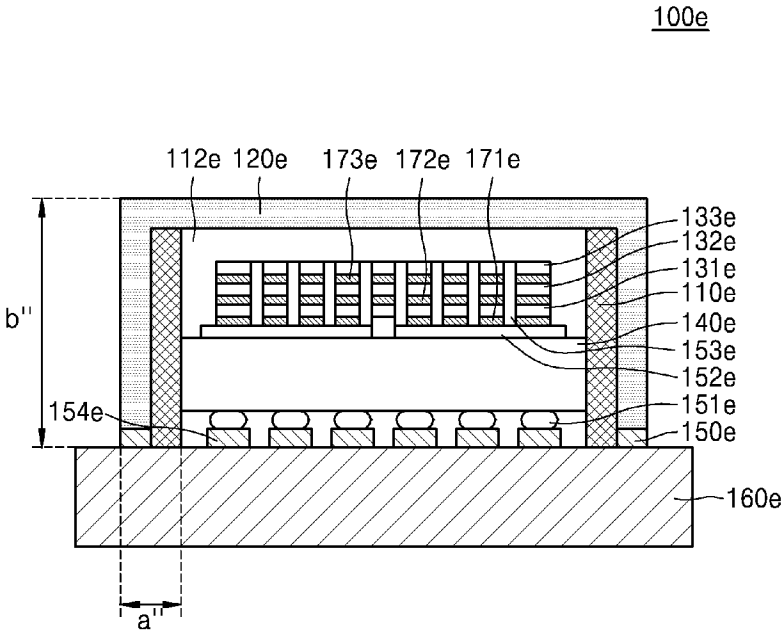
132d
152d
120d
112d
131d
151d

[Fig. 7]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112e 120e 173e 172e 171e
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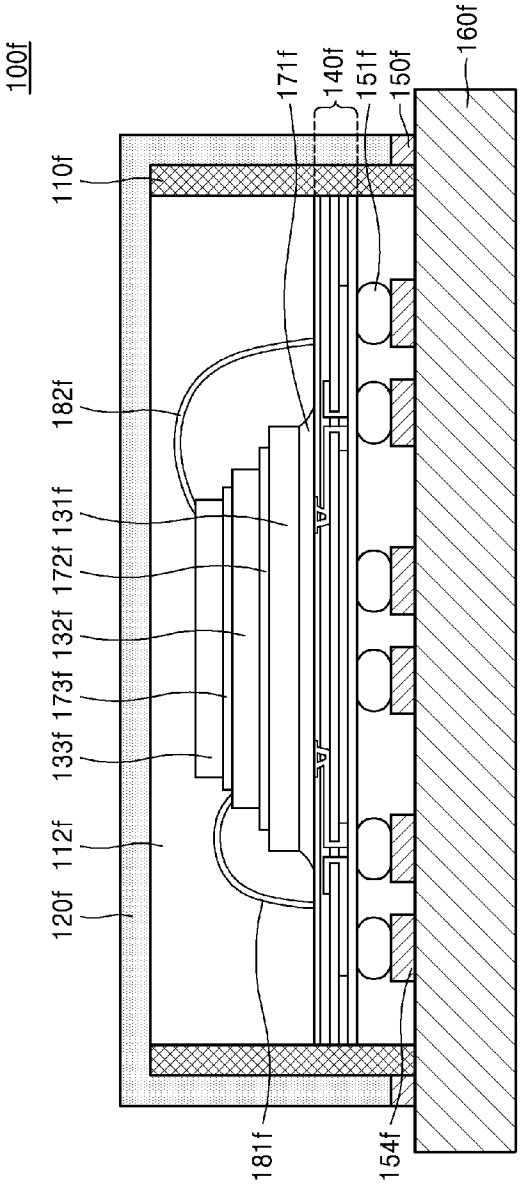
110e
140e
153e
152e
151e
150e
154e
160e
b''
a''

[Fig. 8]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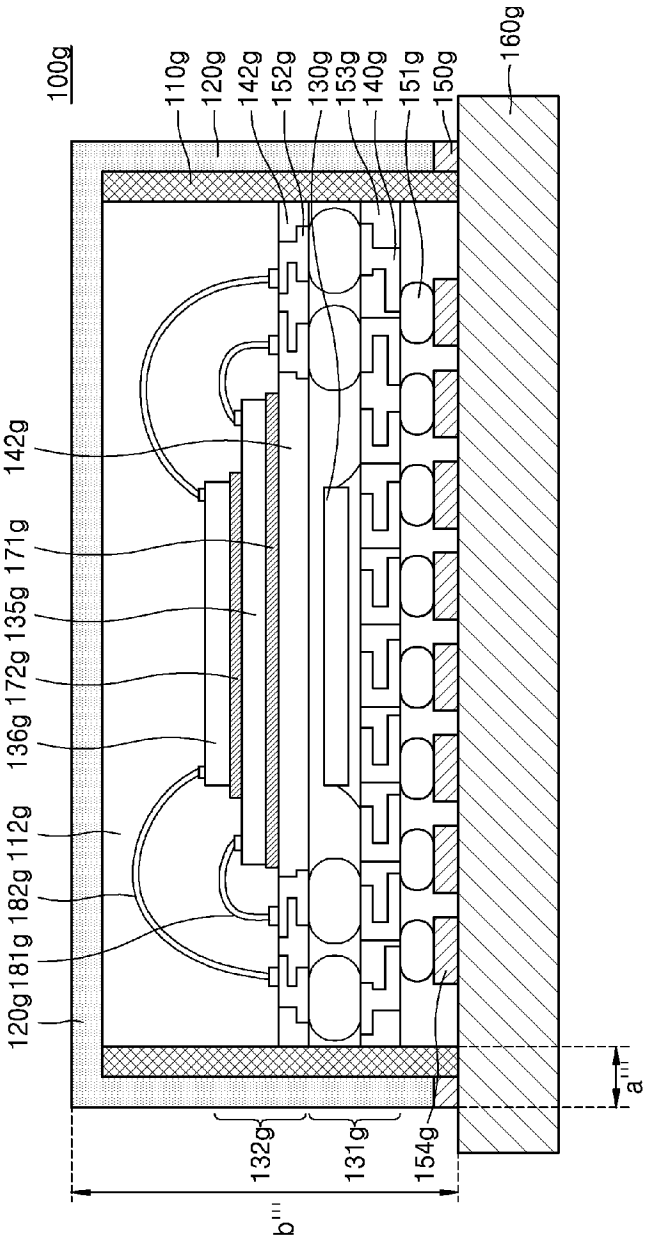
154f

[Fig. 9]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120g
a'''
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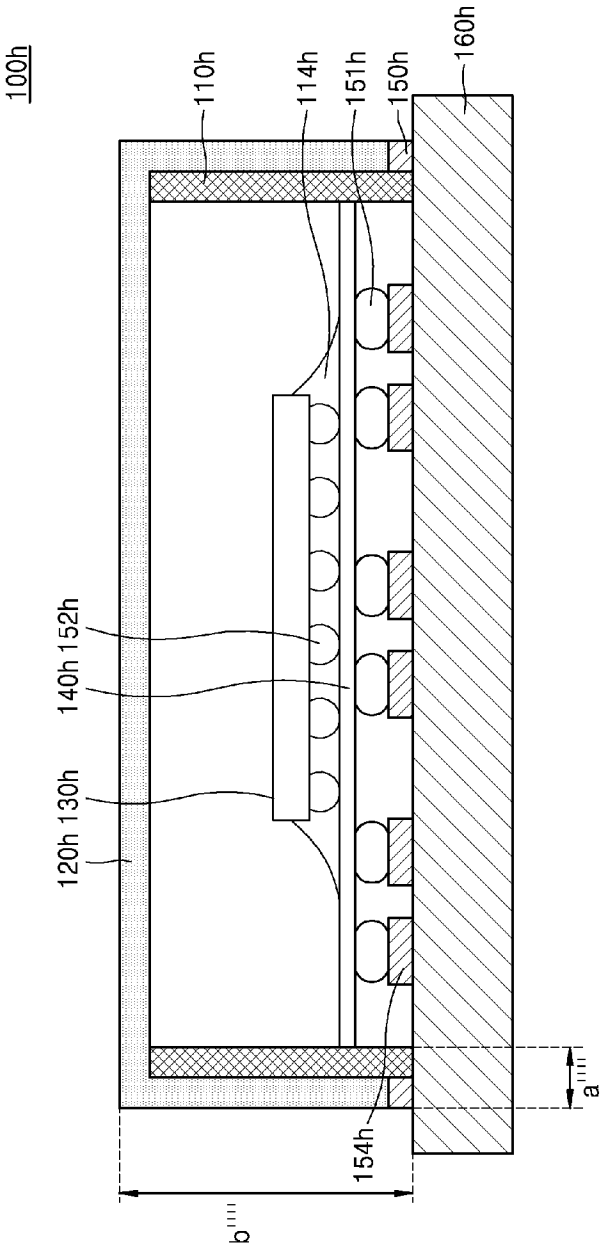
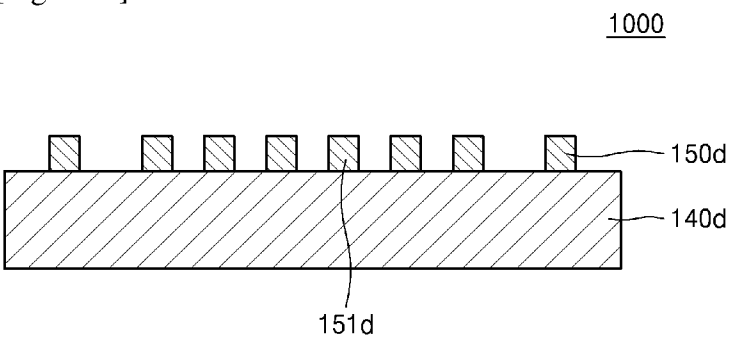
131g
154g
b'''

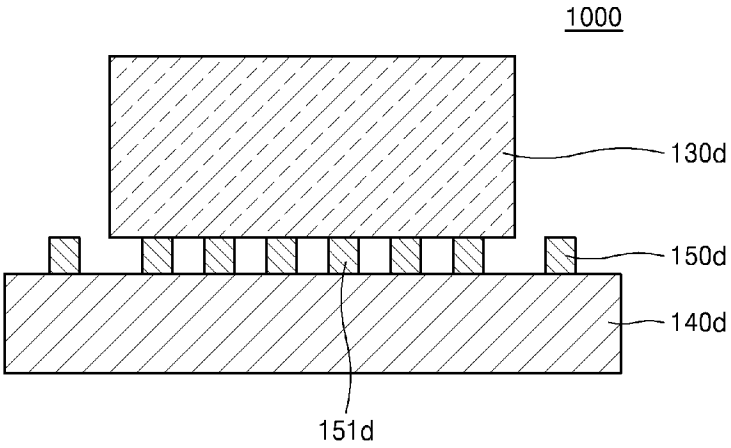
[Fig. 10]



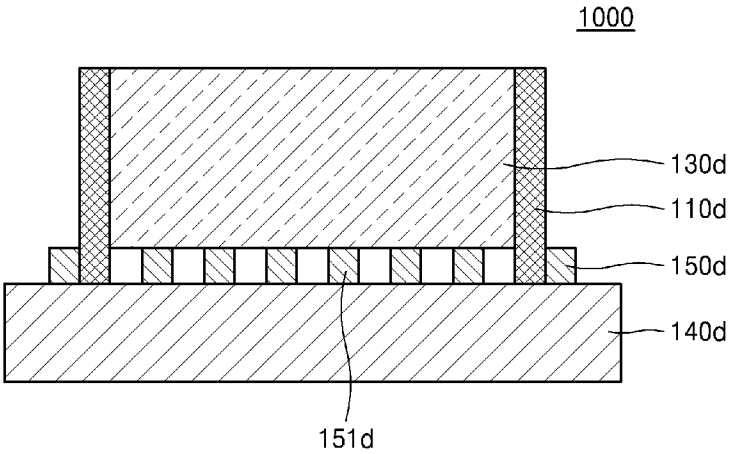
[Fig. 11A]



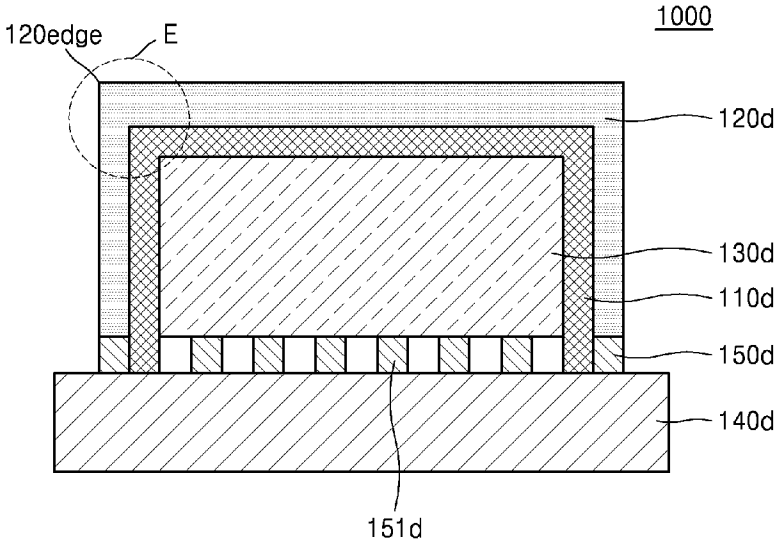
[Fig. 11B]



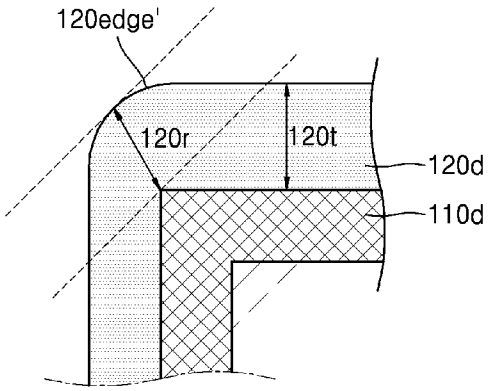
[Fig. 11C]



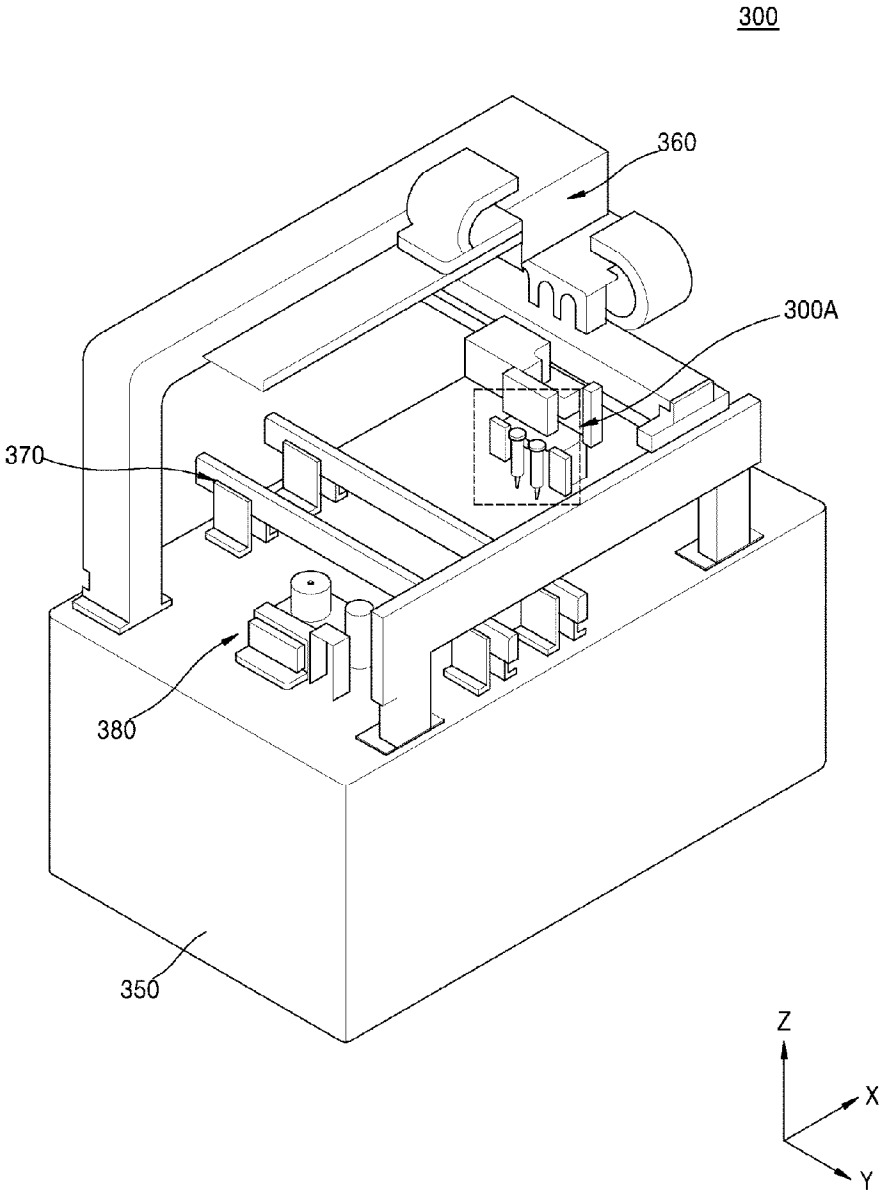
[Fig. 11D]



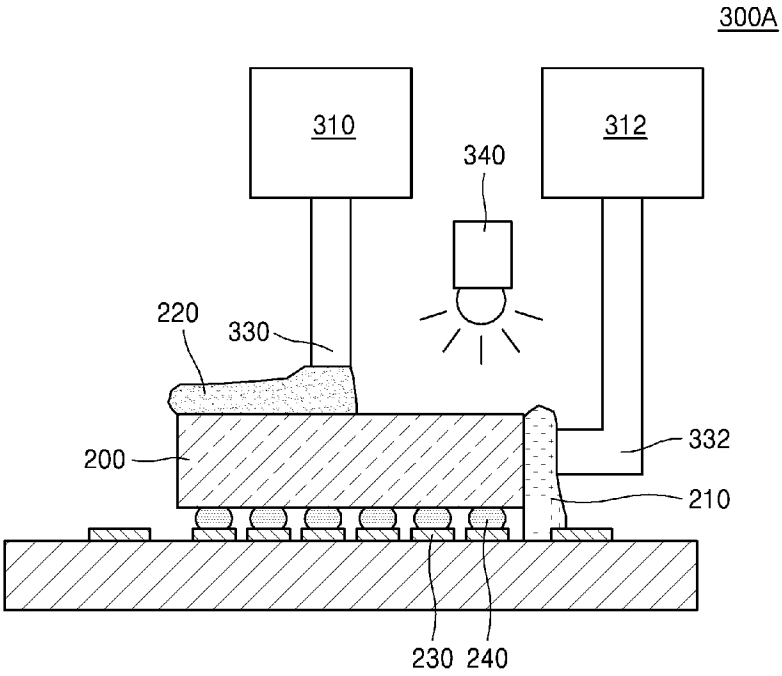
[Fig. 11E]



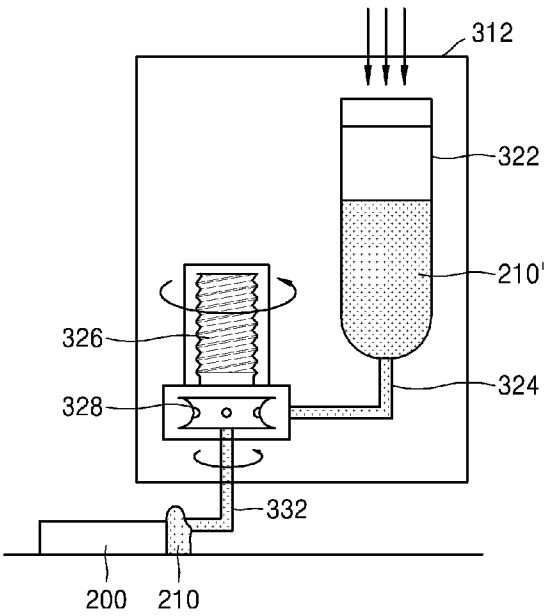
[Fig. 12]



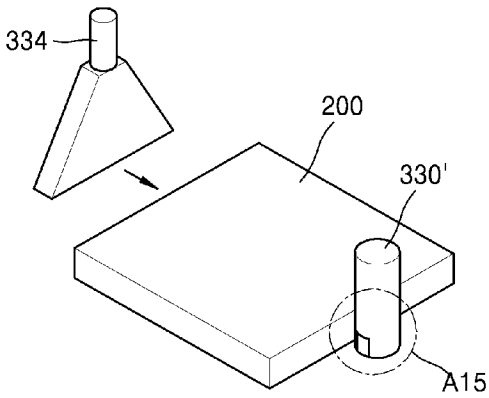
[Fig. 13]



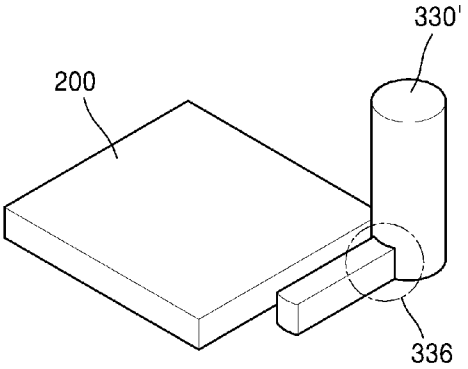
[Fig. 14]



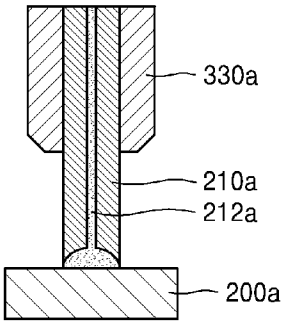
[Fig. 15A]



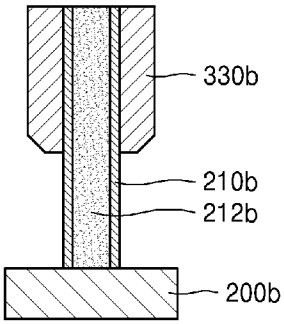
[Fig. 15B]



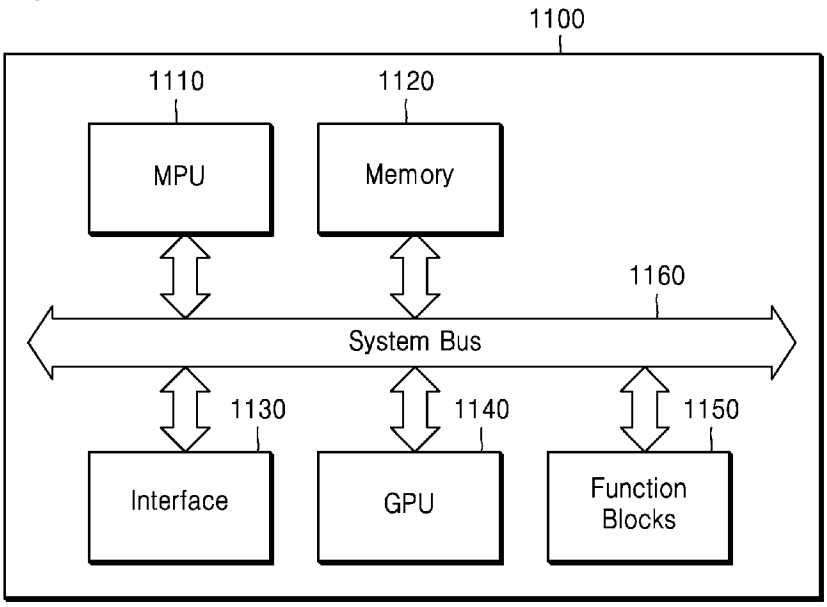
[Fig. 16A]



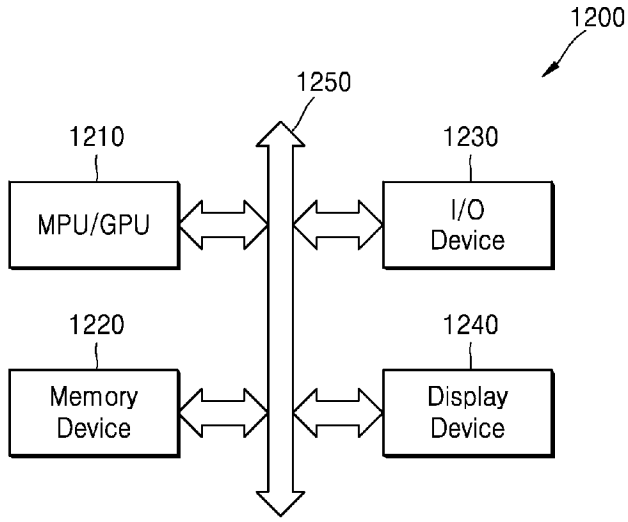
[Fig. 16B]



[Fig. 17]



[Fig. 18]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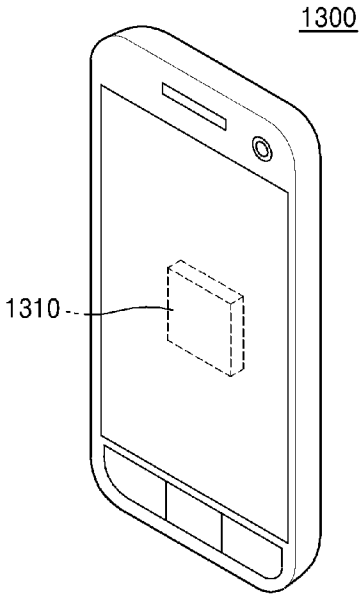
1230
I/O Device
1220
Memory Device
1240
Display Device

[Fig. 19]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INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2016/000013

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/60(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 23/60; B05D 5/12; H01G 9/08; H05K 7/20; H05K 9/00; H01G 4/236; H05K 3/00; H01L 21/78; H01L 23/552

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: package, electromagnetic shielding layer, thixotropic material, three-dimensional printing

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0006408 A1 (KUO-HSIEN LIAO) 13 January 2011 See abstract, paragraphs [0021]-[0029], claim 1 and figures 1A-4.	1-5
Y		6-15
Y	US 2007-0071886 A1 (SAMUEL M. BABB et al.) 29 March 2007 See abstract, paragraphs [0055]-[0060] and figure 1.	6-15
Y	US 2014-0140001 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 22 May 2014 See abstract, paragraph [0037] and claim 16.	8,14-15
A	US 2013-0120903 A1 (YI-HSIU PAN et al.) 16 May 2013 See abstract, paragraphs [0006]-[0011] and figures 7-11.	1-15
A	US 2008-0123316 A1 (RUEI YUEN CHEN et al.) 29 May 2008 See abstract, paragraphs [0005]-[0007] and claim 1.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 April 2016 (18.04.2016)	**18 April 2016 (18.04.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2016/000013

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