(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 February 2008 (07.02.2008)

PCT

(10) International Publication Number
WO 2008/017006 A3

(51) **International Patent Classification:**
***GOIR 31/28* (2006.01)**

(21) **International Application Number:**
PCT/US2007/075020

(22) International Filing Date: 2 August 2007 (02.08.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/821,315	3 August 2006 (03.08.2006)	US
11/774,269	6 July 2007 (06.07.2007)	US

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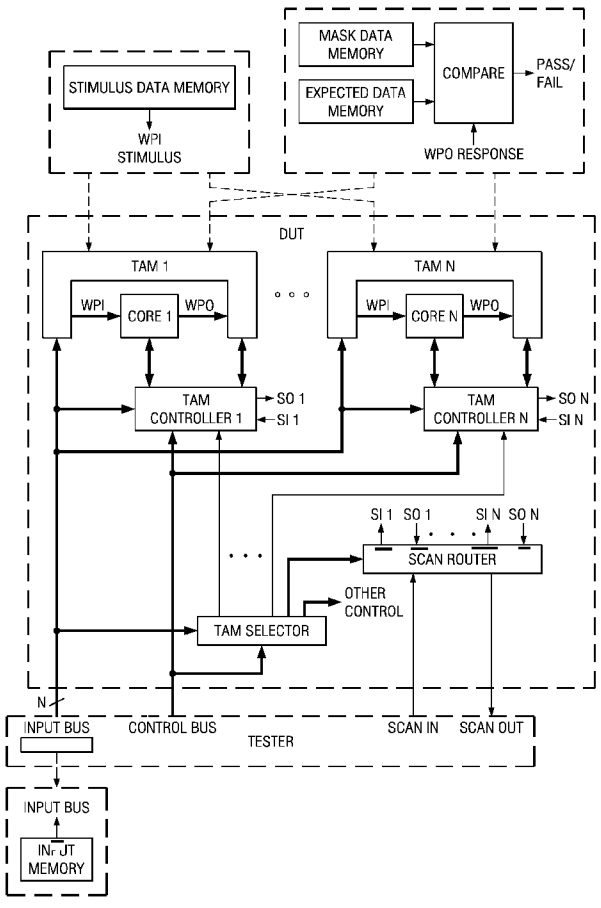
(81) **Designated States** *(unless otherwise indicated, for every kind of national protection available):* AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KR KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available):* ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, **BJ,** CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: DOUBLE DATA RATE TEST INTERFACE AND ARCHITECTURE



(57) Abstract: A device test architecture (702) and a reduced device test interface are provided to enable efficient testing of embedded cores (708) and other circuits within devices. The reduced device test interface is achieved using a double data rate (DDR) signaling technique between the tester (712) and the device. The DDR test interface allows the tester to interface to test circuits within the device, such as IEEE 1500 and/or IEEE 1149.1 test circuits, to provide high test data bandwidth to the test circuits using a minimum of test interface signals. The test architecture includes compare circuits that allow for comparison of test response data to be performed within the device. The test architecture further includes a memory for storing the results of the test response comparisons. The test architecture includes a programmable test controller (706) to allow for various test control operations by simply inputting an instruction to the programmable test controller from the external tester. Additional features and embodiments of the device test architecture and reduced test interface are also disclosed.

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(H))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(Hi))*

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
12 September 2008

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US07/75020

A. CLASSIFICATION OF SUBJECT MATTER
IPC: GOIR 31/28(2006.01)

USPC: 714/726,727
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 714/726,727

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
US PG PUB, JPO, EPO, Derwent, IBM TDB

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Google search, IEEE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,938,225 B2 (Kndu Sandip) 30-Aug-05 Figure 3 Columns 2-3	1-4
X	Double edge triggered devices: Speed and power constraints Hossain et al., A. Circuits and Systems, 1993., ISCAS '93, 1993 IEEE International Symposium on May 1993, Page(s): 1491 -1494, Volume 3	1-4

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cued documents

"A" document defining the general state of the art which is not considered to be of particular relevance

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance, the claimed invention cannot be considered to involve an inventive step when the document is combmed with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 June 2008 (12.06.2008)	01 JUL 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn ISA/US Commissioner for Patents P O Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	Authorized officer Cynthia Britt Telephone No. 571-272-4150

Form PCT/ISA/210 (second sheet) (April 2007)