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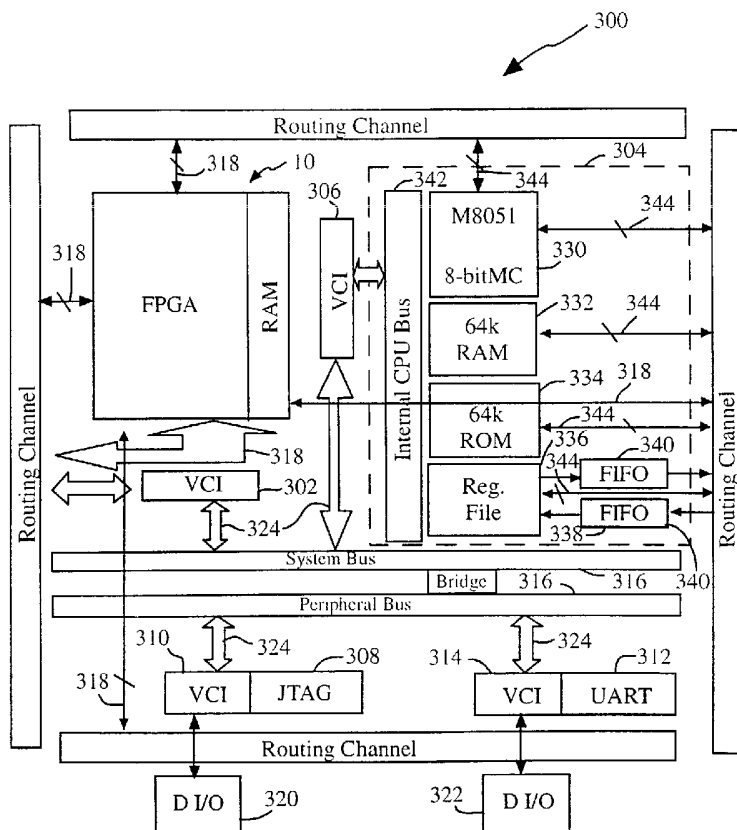
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[Continued on next page]

(54) Title: FIELD PROGRAMMABLE GATE ARRAY AND MICROCONTROLLER SYSTEM-ON-A-CHIP

(57) Abstract: An system-on-a-chip integrated circuit has a field programmable gate array core having logic clusters, static random access memory modules, and routing resources, a field programmable gate array virtual component interface translator having inputs and outputs, wherein the inputs are connected to the field programmable gate array core, a microcontroller, a microcontroller virtual component interface translator having input and outputs, wherein the inputs are connected to the microcontroller, a system bus connected to the outputs of the field programmable gate array virtual component interface translator and also to the outputs of said microcontroller virtual component interface translator, and direct connections between the microcontroller and the routing resources of the field programmable gate array core.



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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 5 970 254 A (WONG DALE ET AL) 19 October 1999 (1999-10-19) abstract; figure 1 column 4, line 32 - line 65 ---	1
A	"MIT PROGRAMMIERBARER LOGIK VERHEIRATED" ELEKTRONIK, FRANZIS VERLAG GMBH. MUNCHEN, DE, vol. 47, no. 7, 31 March 1998 (1998-03-31), page 38 XP000778333 ISSN: 0013-5658 the whole document ---	1
A	DE 198 19 505 A (ALCATEL SA) 4 November 1999 (1999-11-04) column 2, line 56 -column 3, line 50 --- -/--	1

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Patent family members are listed in annex.

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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