



US 20160293706A1

(19) **United States**

(12) **Patent Application Publication**

**Cai et al.**

(10) **Pub. No.: US 2016/0293706 A1**

(43) **Pub. Date: Oct. 6, 2016**

(54) **FINFET SEMICONDUCTOR DEVICES WITH STRESSED CHANNEL REGIONS**

*H01L 29/161* (2006.01)

*H01L 29/78* (2006.01)

(71) Applicants: **GLOBALFOUNDRIES Inc.**, Grand Cayman (KY); **International Business Machines Corporation**, Armonk, NY (US)

(52) **U.S. Cl.**

CPC ..... *H01L 29/1054* (2013.01); *H01L 29/785* (2013.01); *H01L 29/66795* (2013.01); *H01L 29/66545* (2013.01); *H01L 29/161* (2013.01); *H01L 29/7843* (2013.01)

(72) Inventors: **Xiuyu Cai**, Niskayuna, NY (US); **Ruilong Xie**, Niskayuna, NY (US); **Kanguo Cheng**, Schenectady, NY (US); **Ali Khakifirooz**, Mountain View, CA (US); **Ajey P. Jacob**, Watervliet, NY (US); **Witold P. Maszara**, Morgan Hill, CA (US)

(57)

**ABSTRACT**

A FinFET device includes a substrate, a gate structure positioned above the substrate, and sidewall spacers positioned adjacent to the gate structure. An epi semiconductor material is positioned in source and drain regions of the FinFET device and laterally outside of the sidewall spacers. A fin extends laterally under the gate structure and the sidewall spacers in a gate length direction of the FinFET device, wherein the end surfaces of the fin abut and engage the epi semiconductor material. A stressed material is positioned in a channel cavity located below the fin, above the substrate, and laterally between the epi semiconductor material, the stressed material having a top surface that abuts and engages a bottom surface of the fin, a bottom surface that abuts and engages the substrate, and end surfaces that abut and engage the epi semiconductor material.

(21) Appl. No.: **15/186,632**

(22) Filed: **Jun. 20, 2016**

**Related U.S. Application Data**

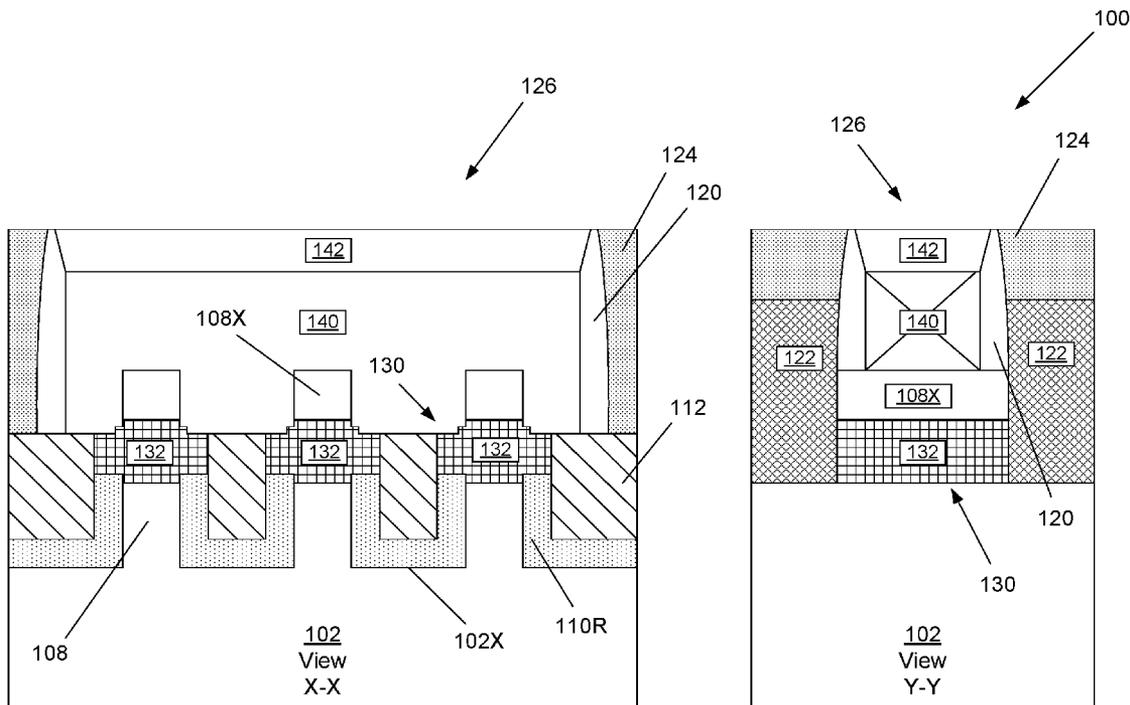
(62) Division of application No. 14/200,737, filed on Mar. 7, 2014, now Pat. No. 9,412,822.

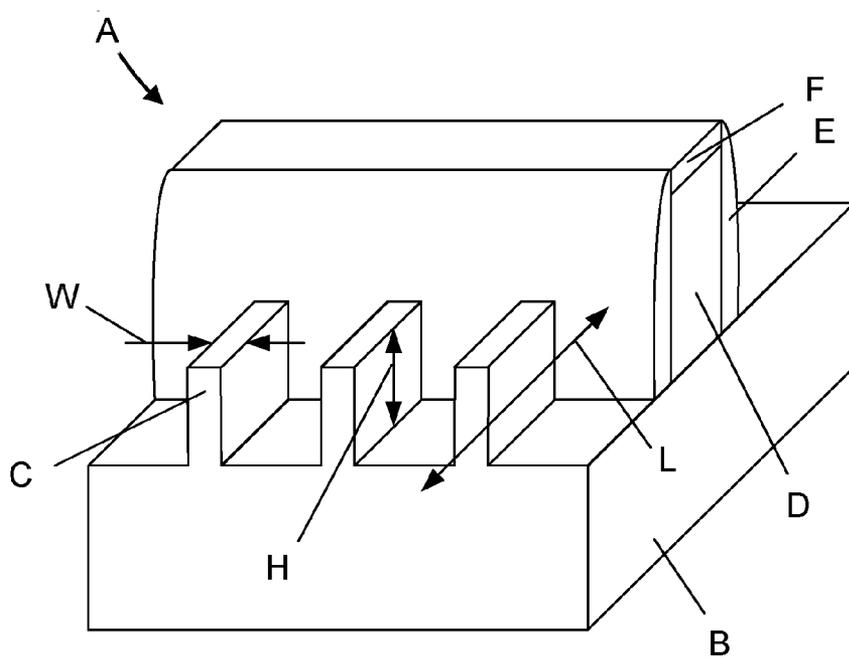
**Publication Classification**

(51) **Int. Cl.**

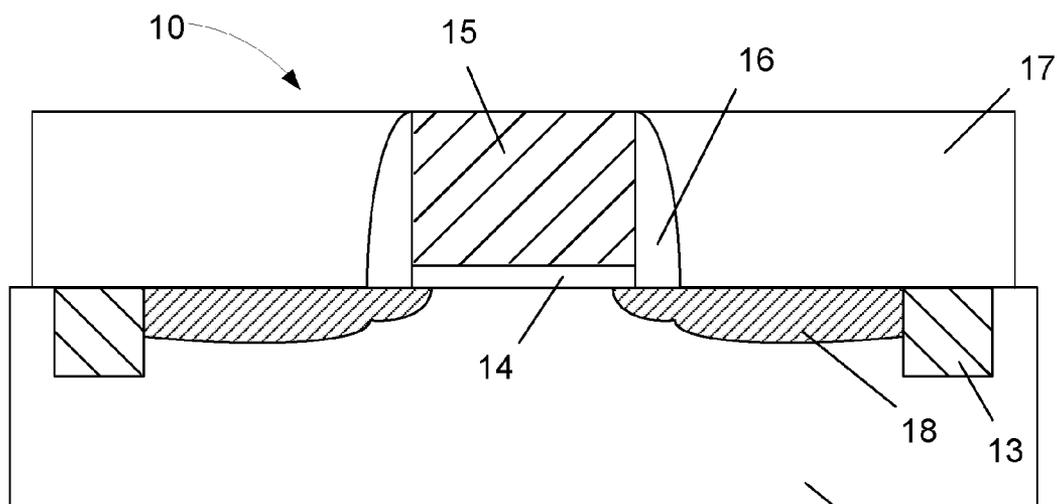
*H01L 29/10* (2006.01)

*H01L 29/66* (2006.01)





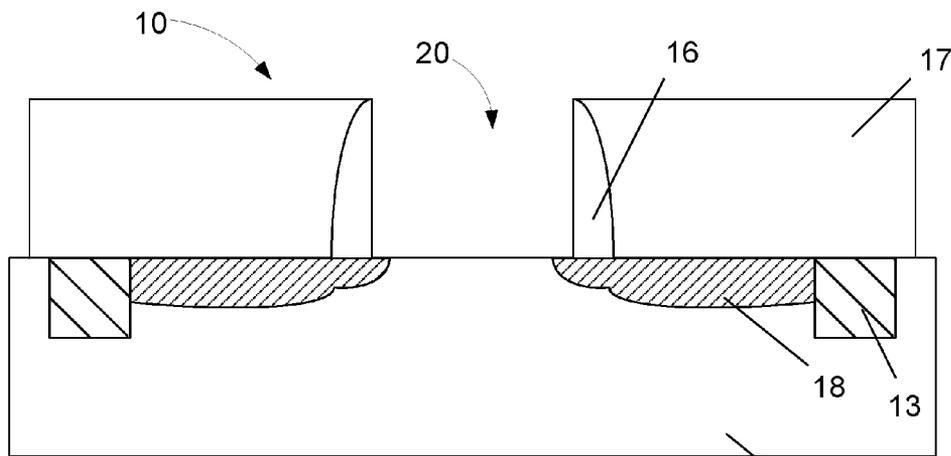
**Figure 1A** (Prior Art)



(Prior Art)

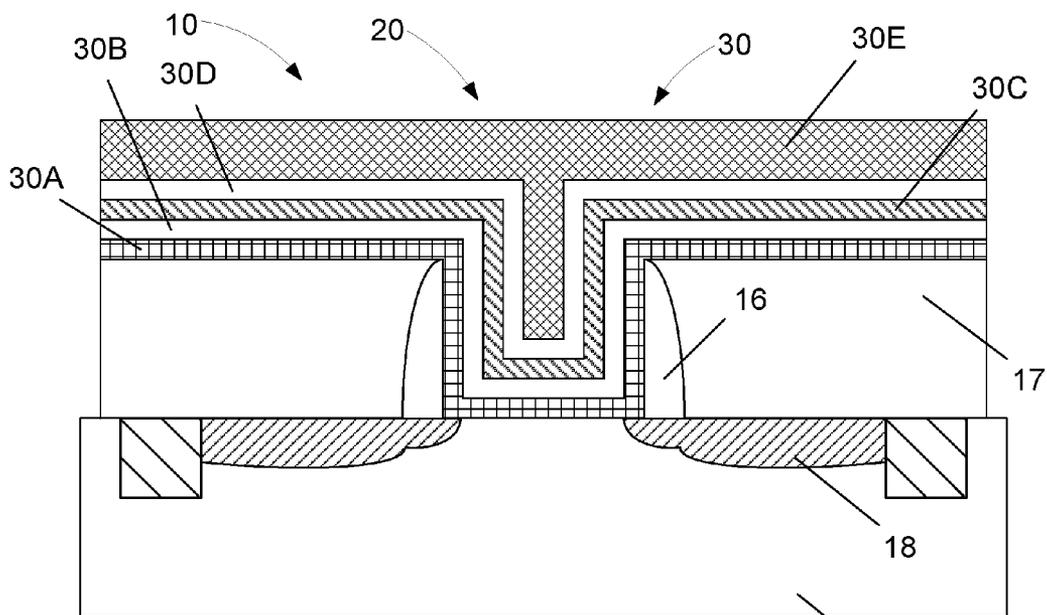
**Figure 1B**

12



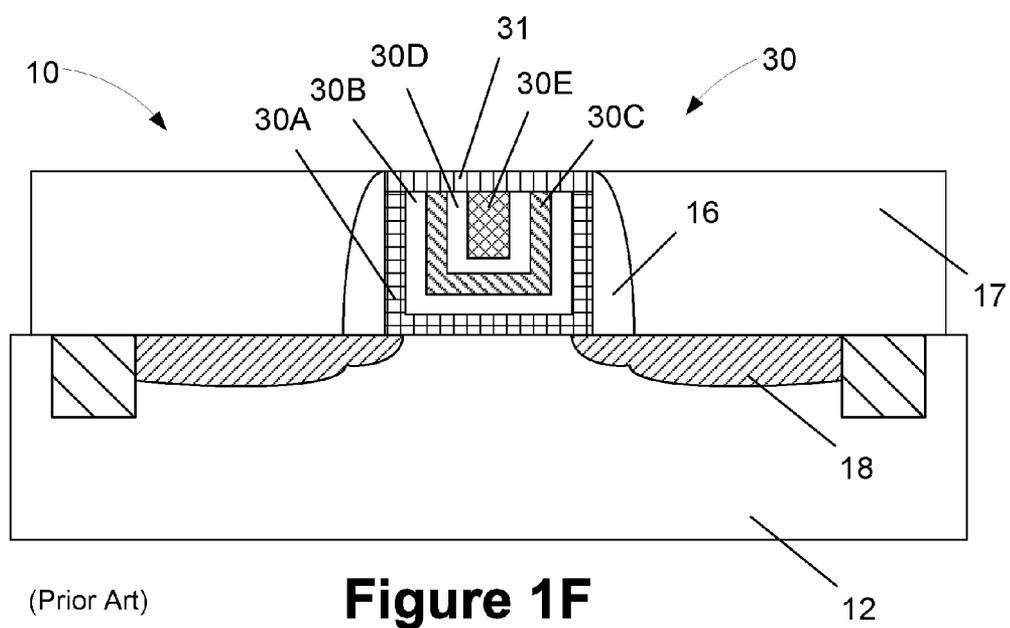
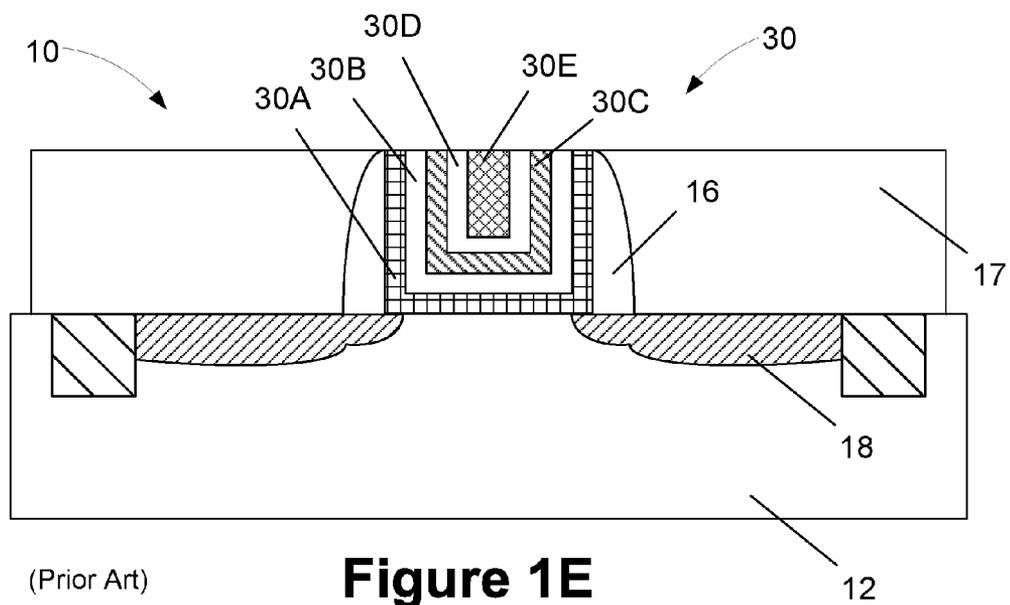
(Prior Art)

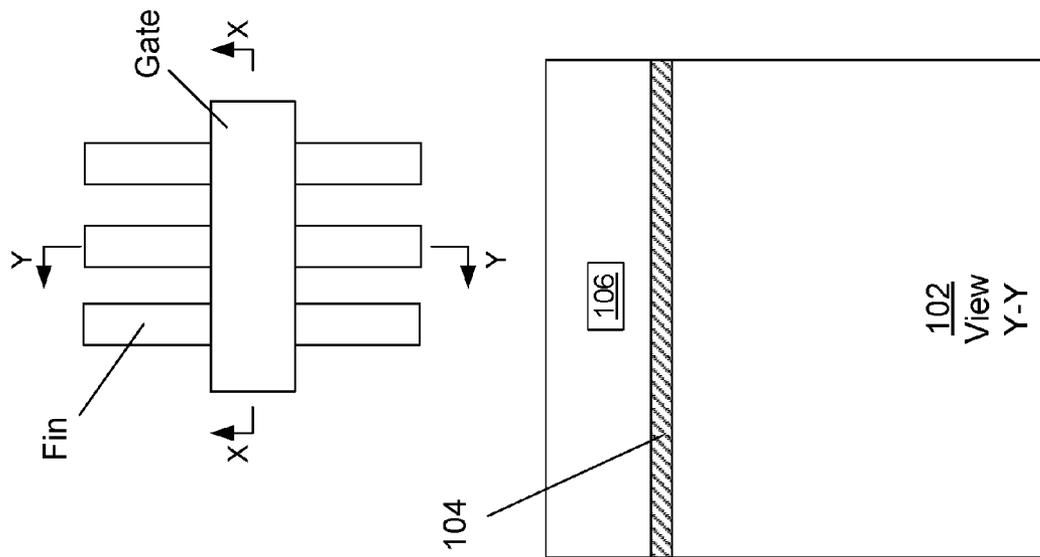
**Figure 1C**



(Prior Art)

**Figure 1D**

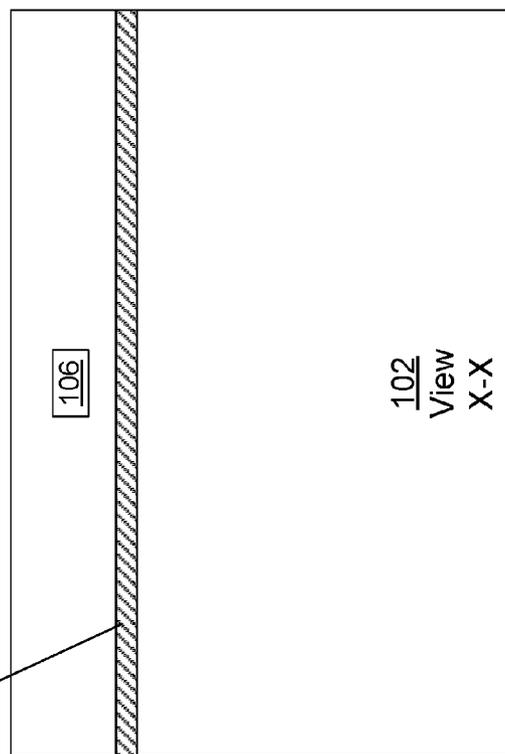




**Figure 2A**

100

104



102  
View  
X-X

100

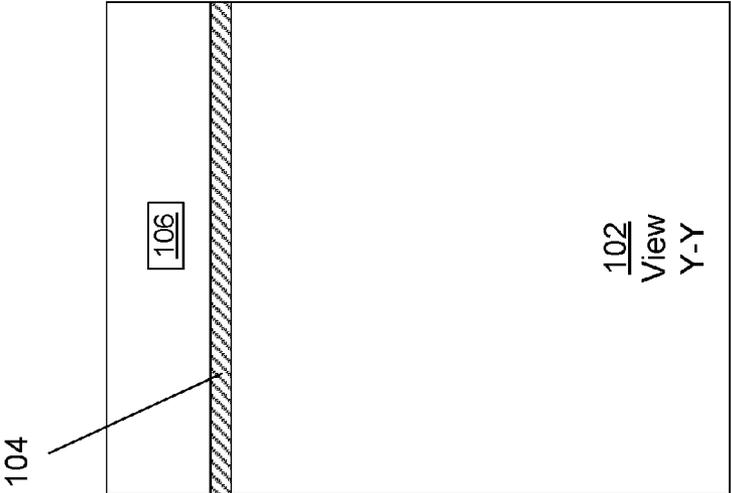
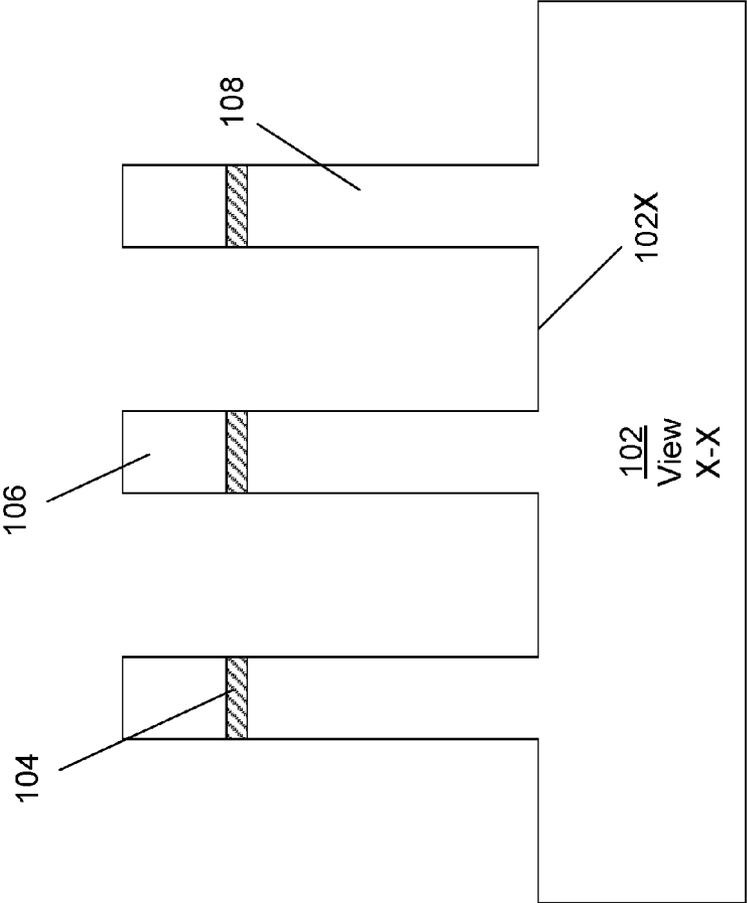
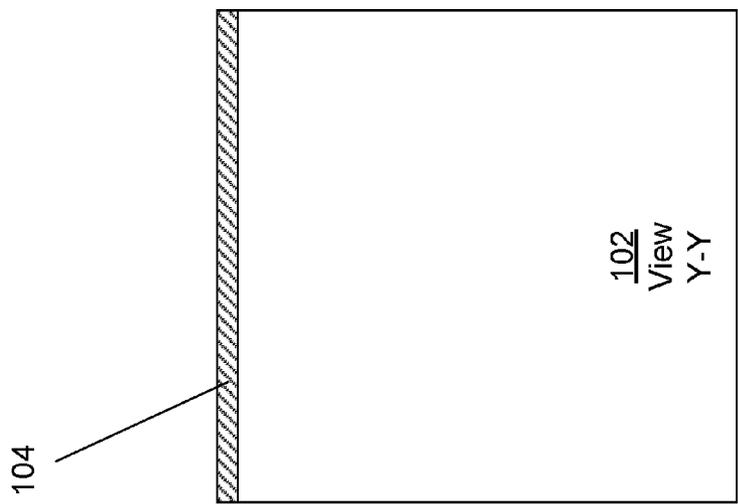


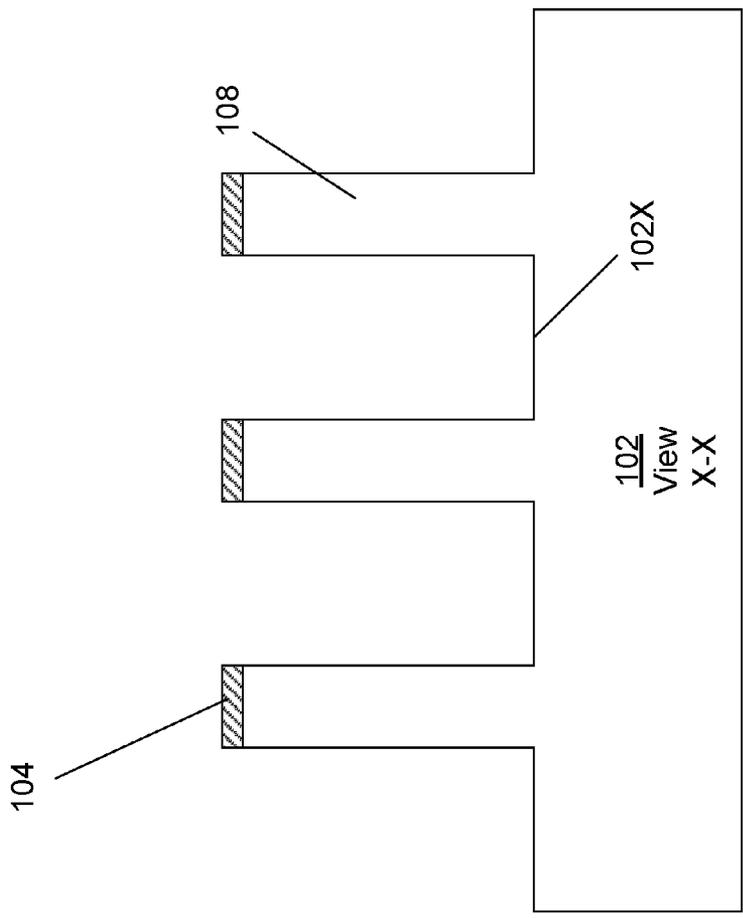
Figure 2B

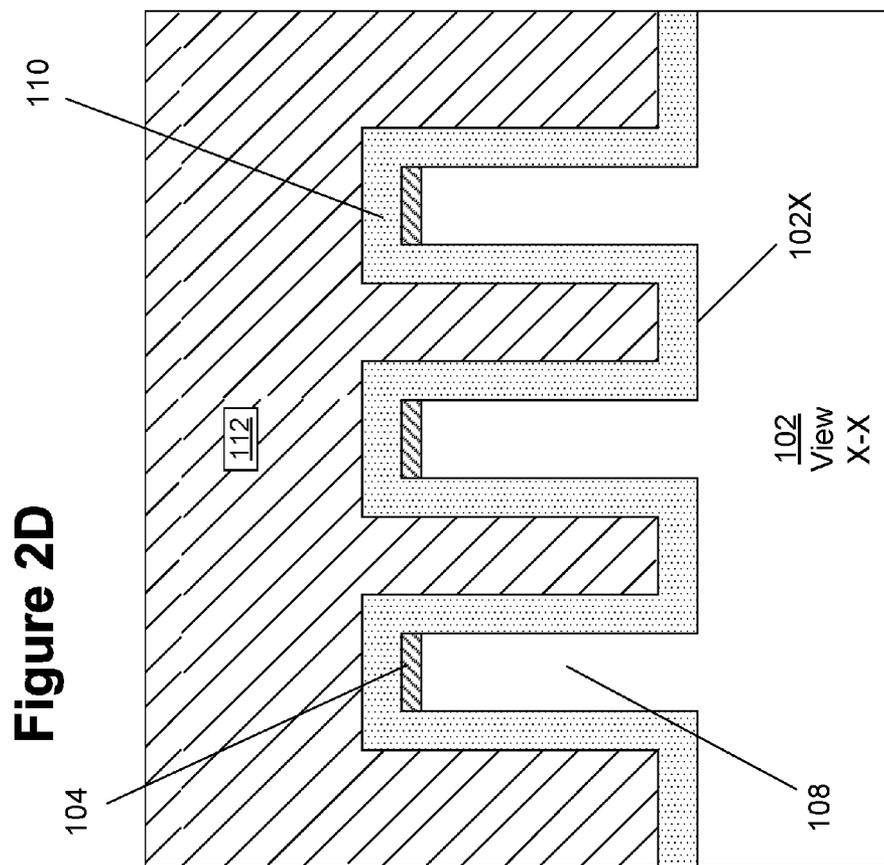
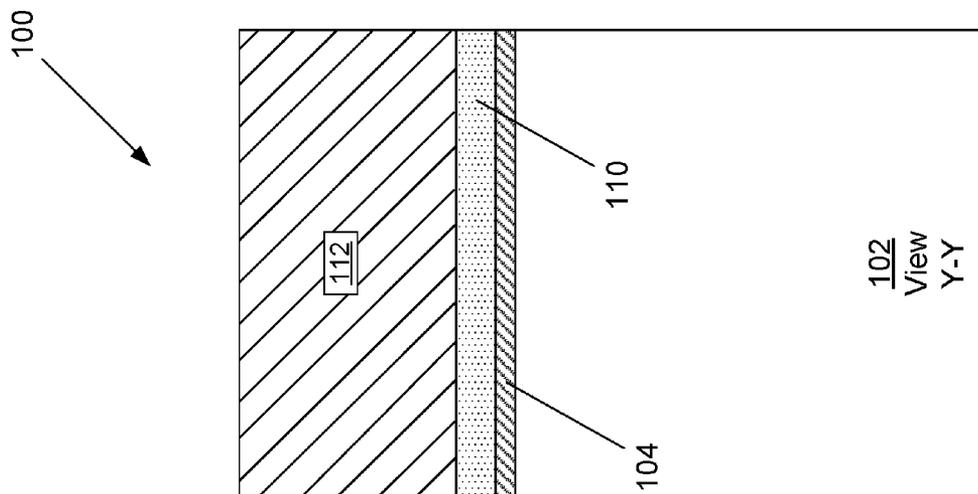


100



**Figure 2C**

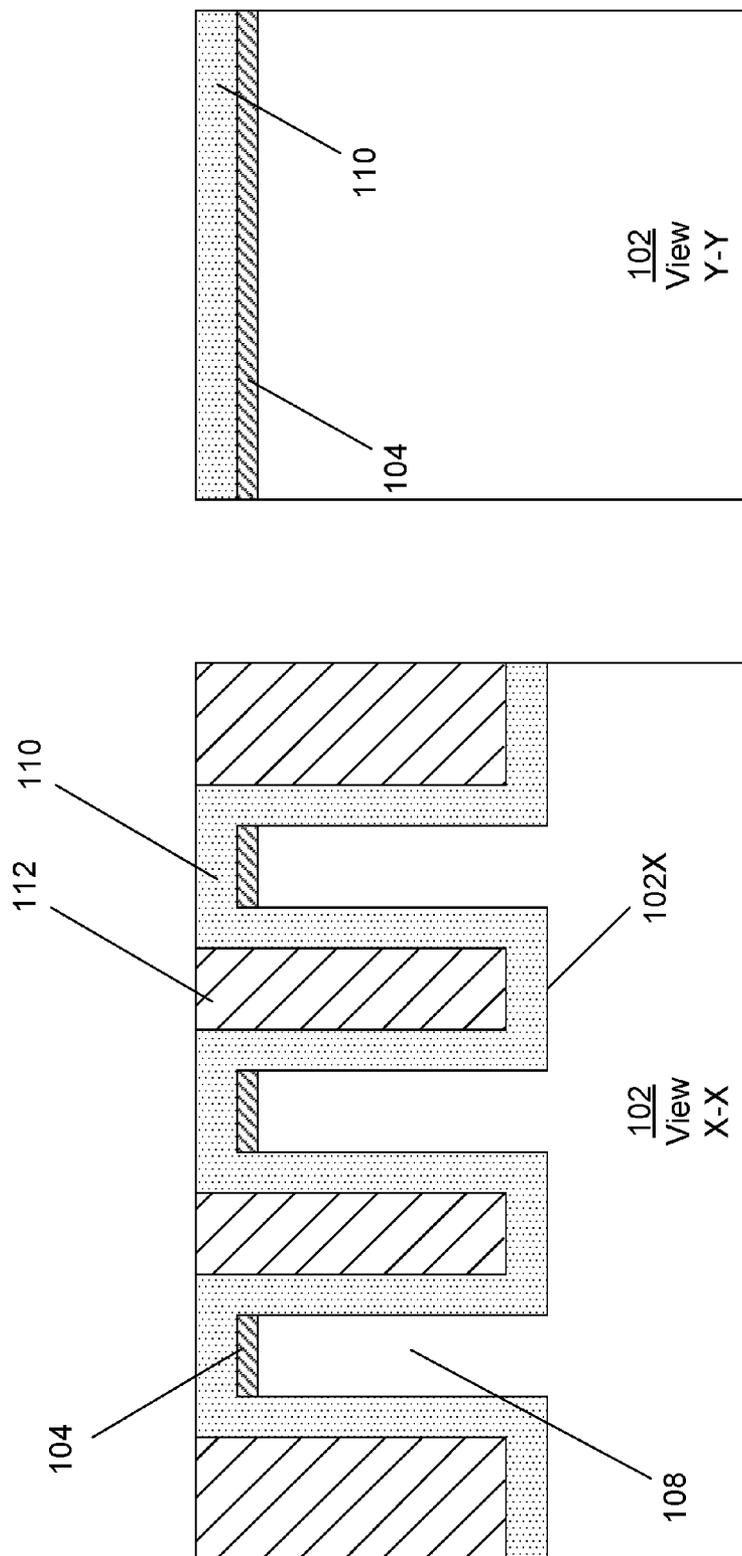




**Figure 2D**

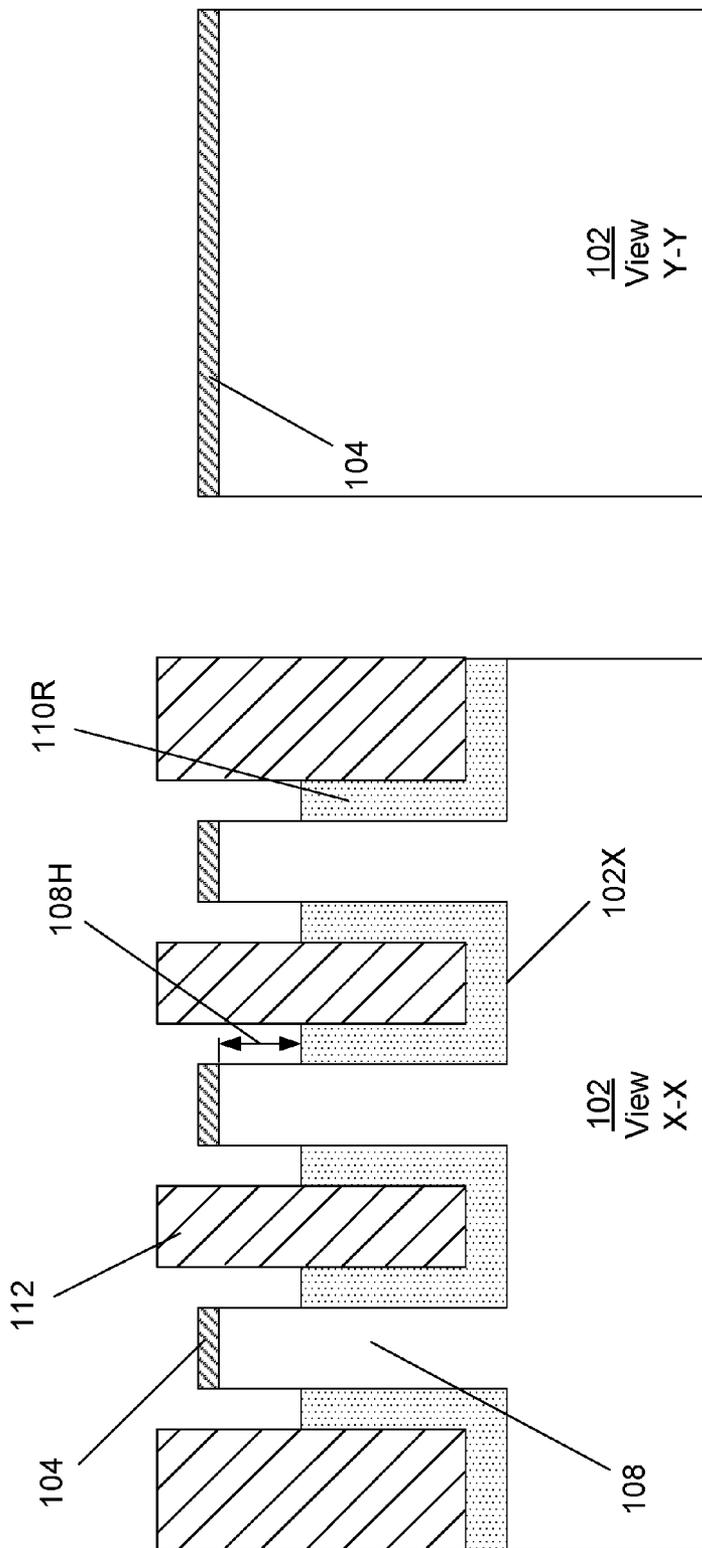
100

**Figure 2E**



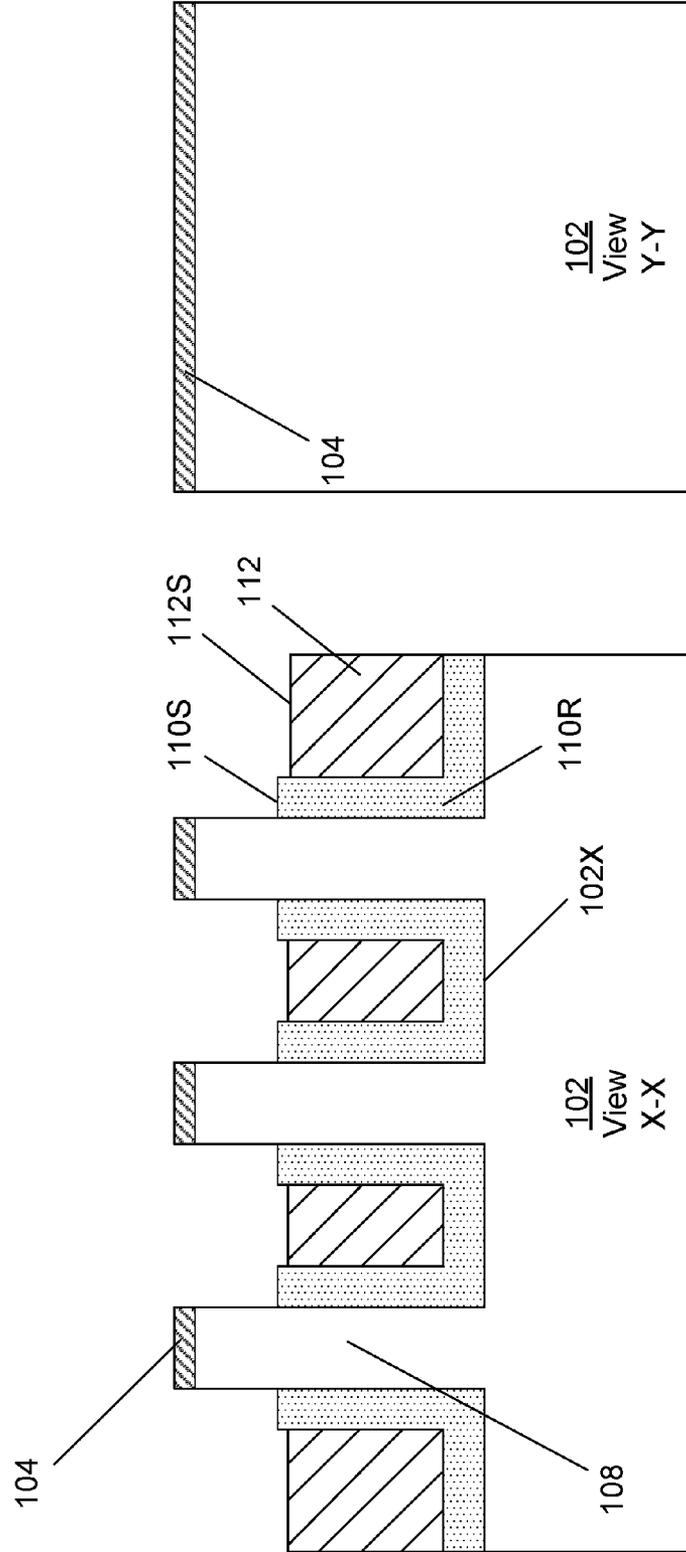
100

**Figure 2F**



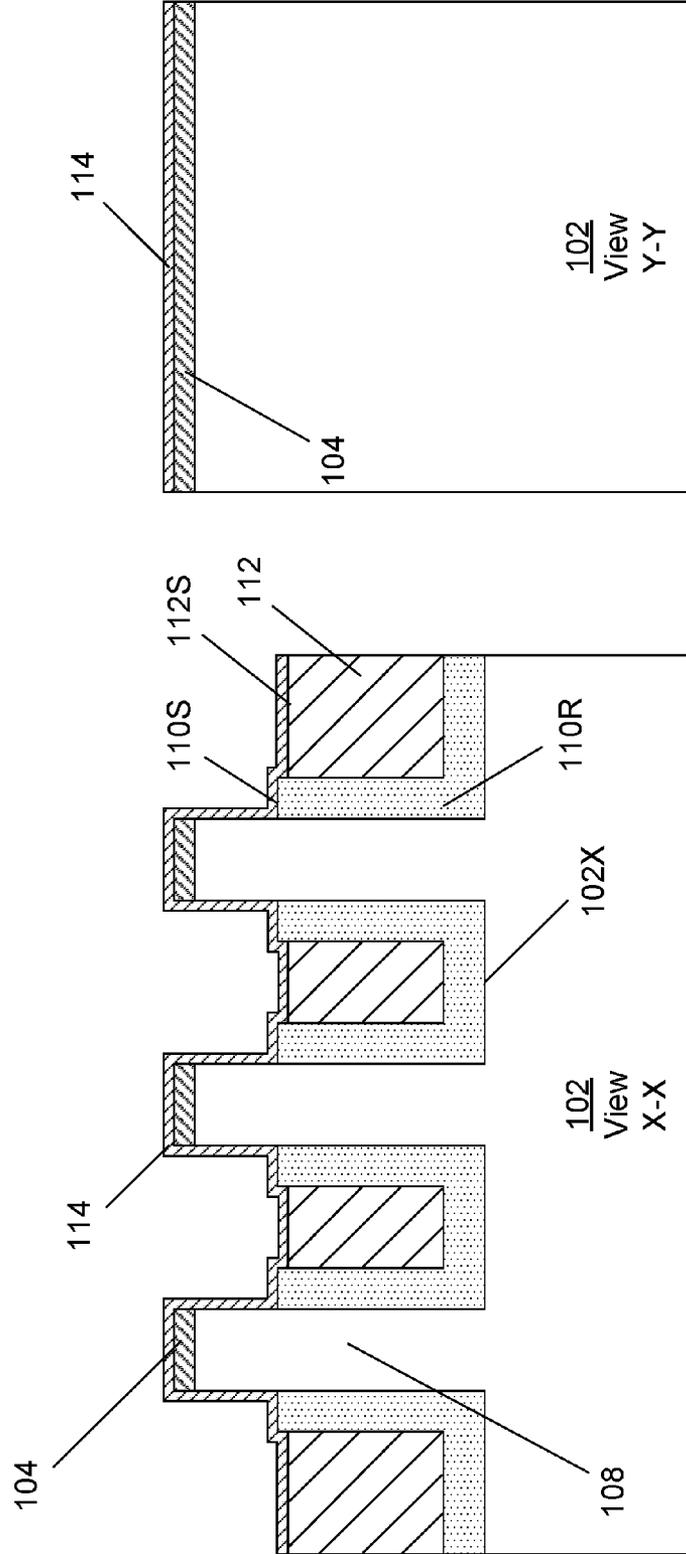
100

**Figure 2G**



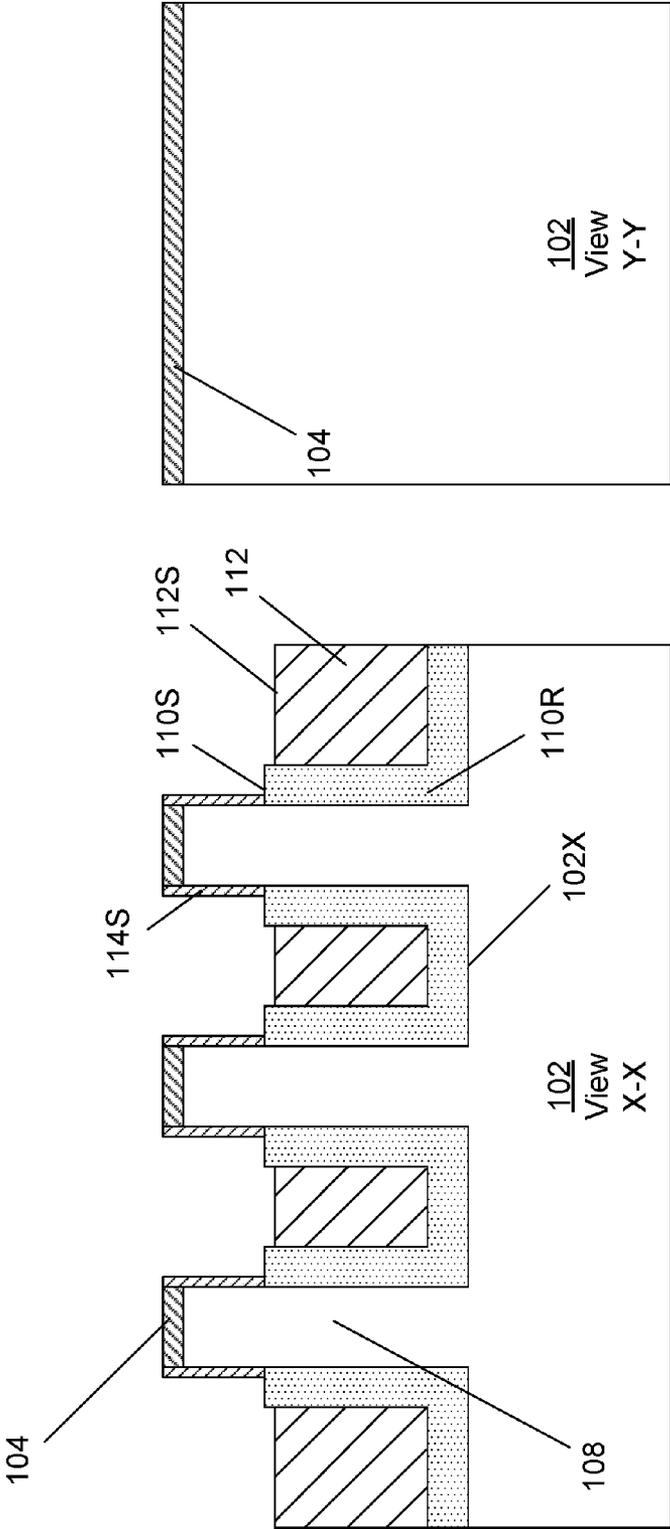
100

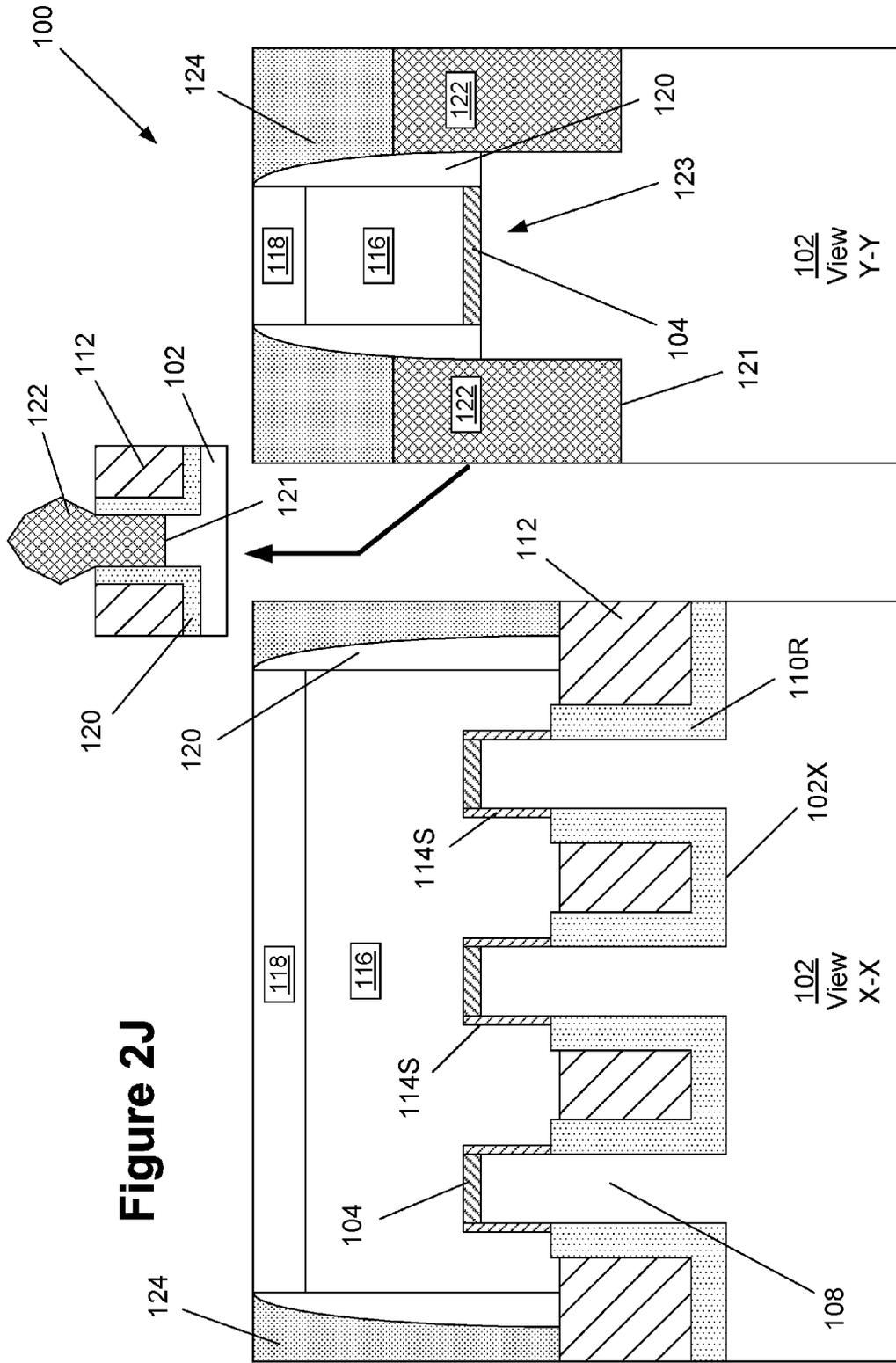
Figure 2H



100

Figure 2I





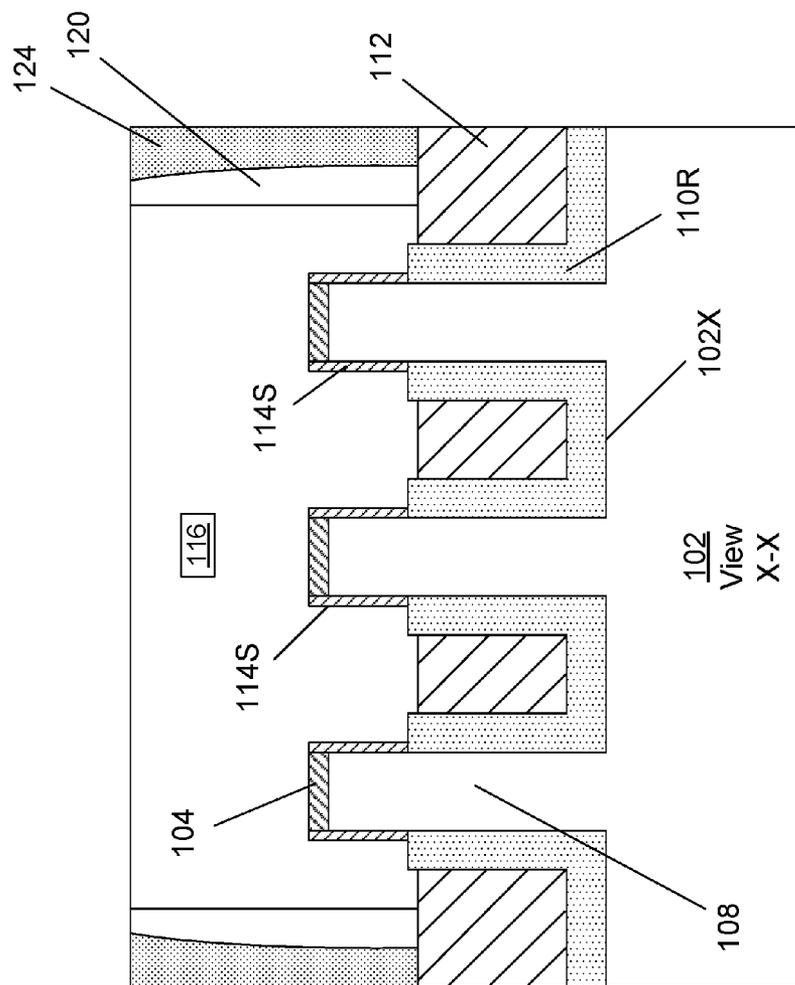
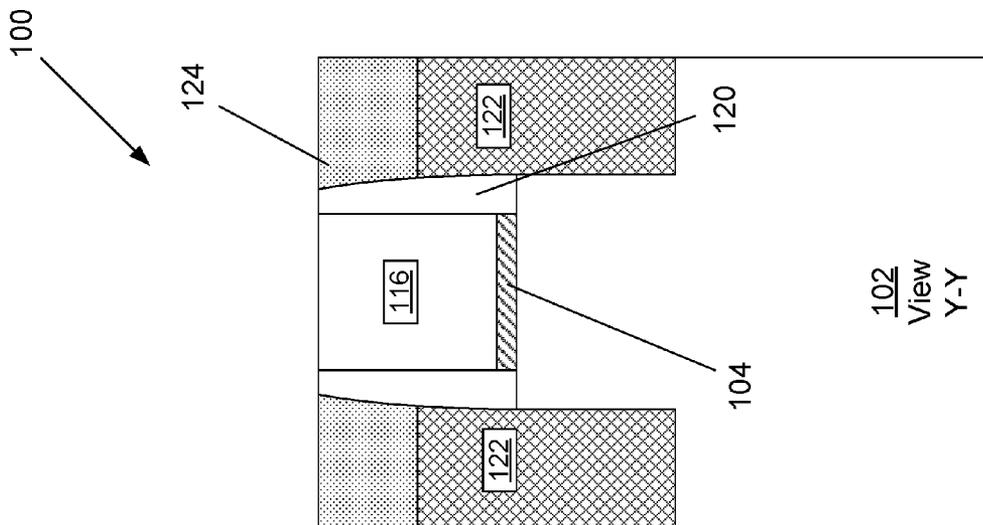
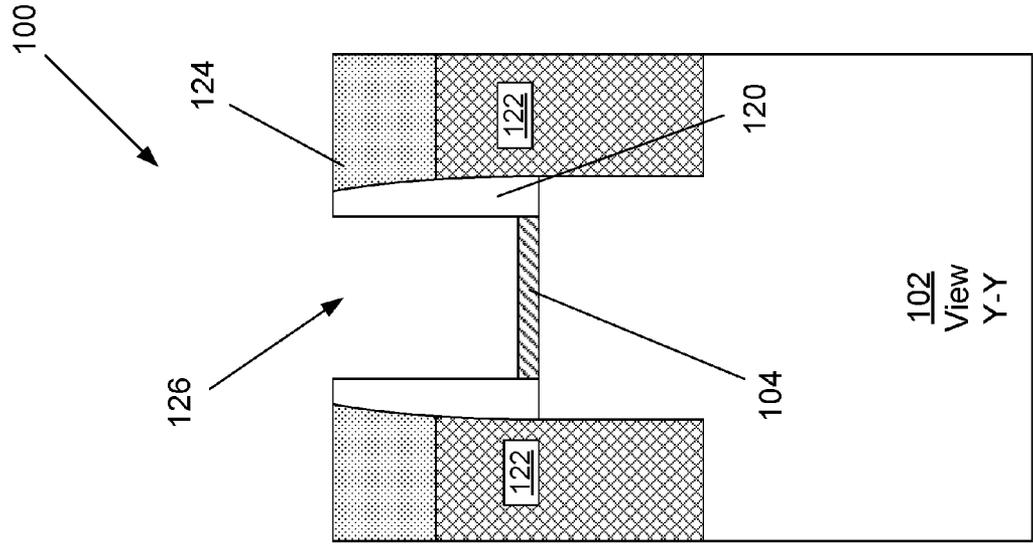
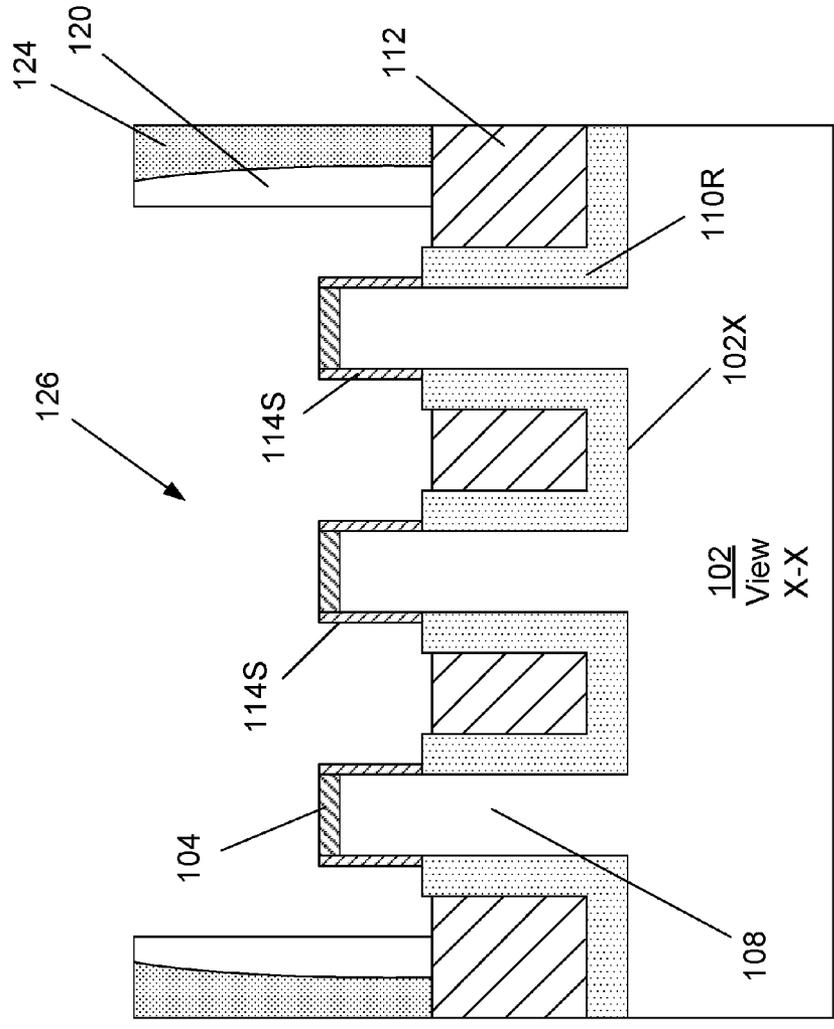
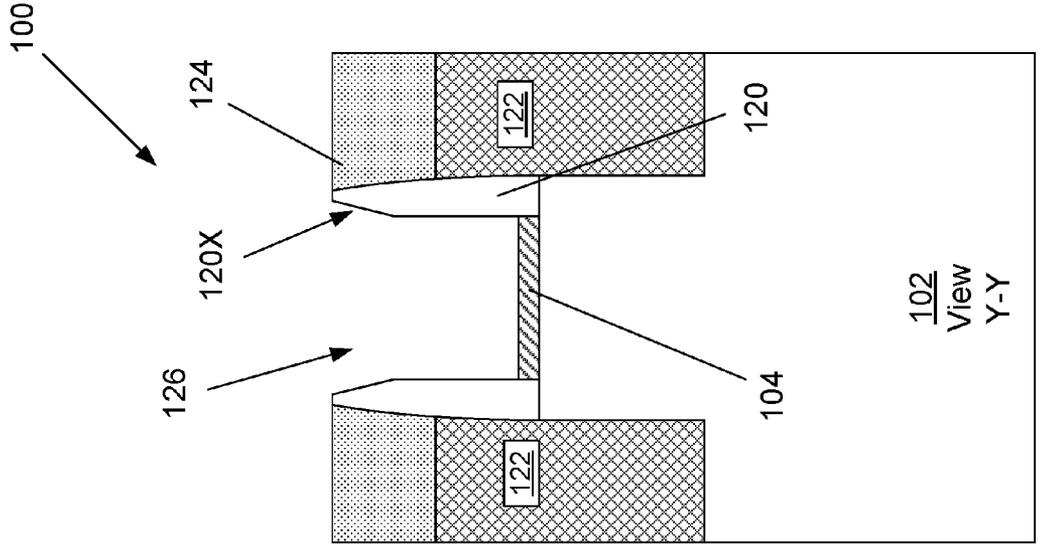


Figure 2K

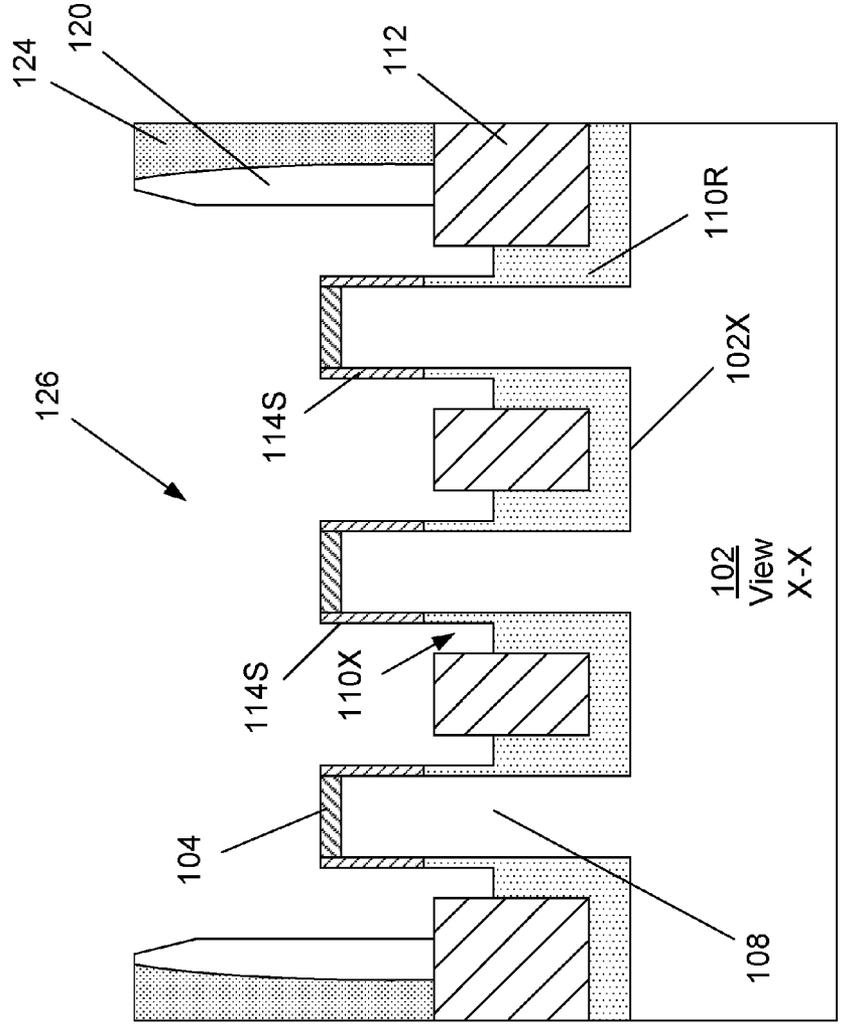


**Figure 2L**





**Figure 2M**



**Figure 2N**

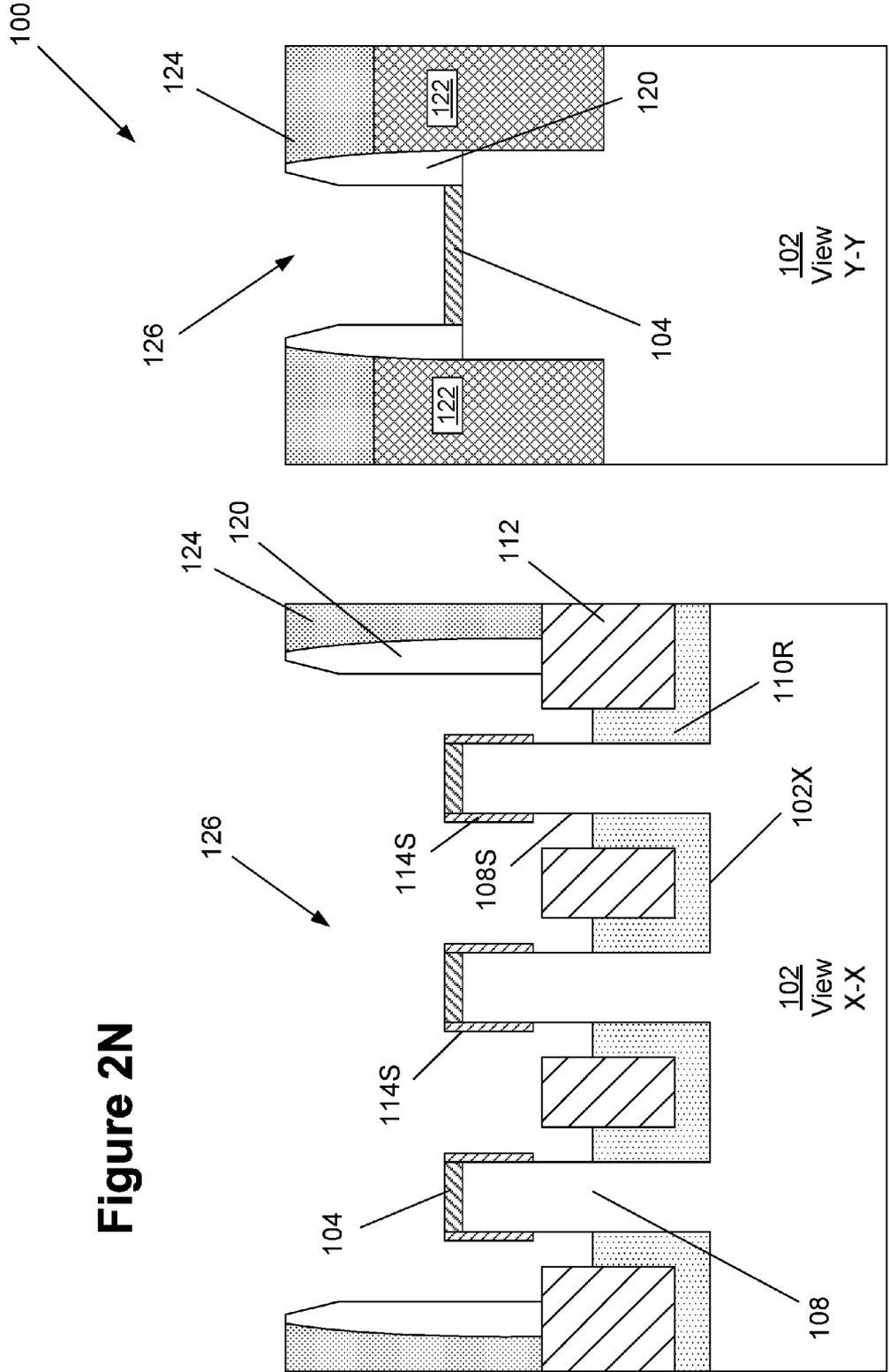


Figure 20

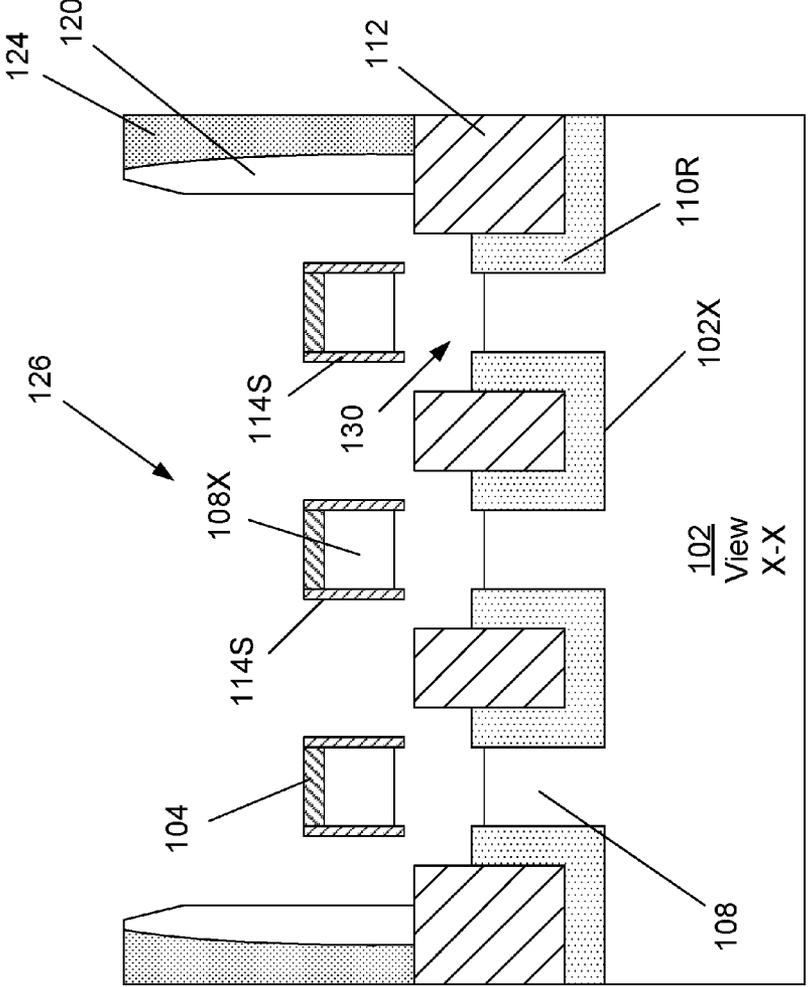
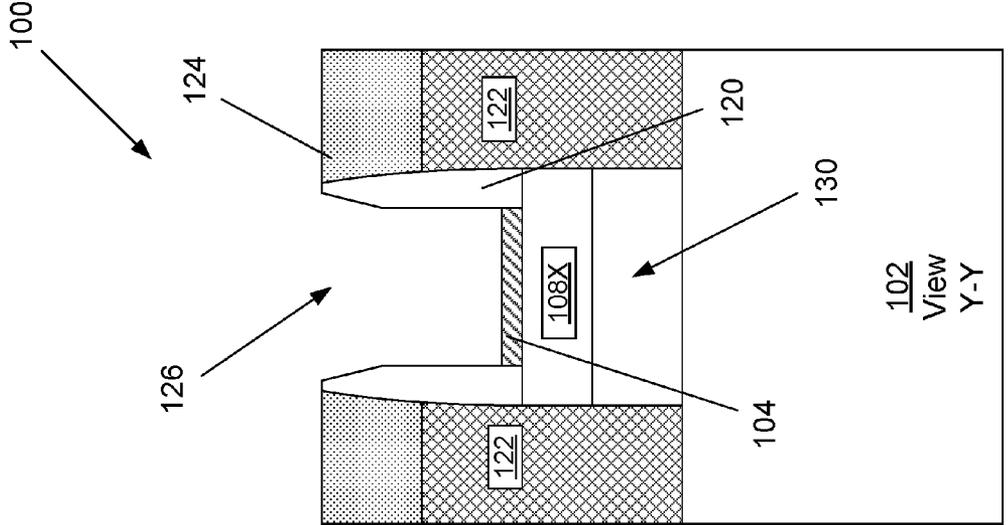
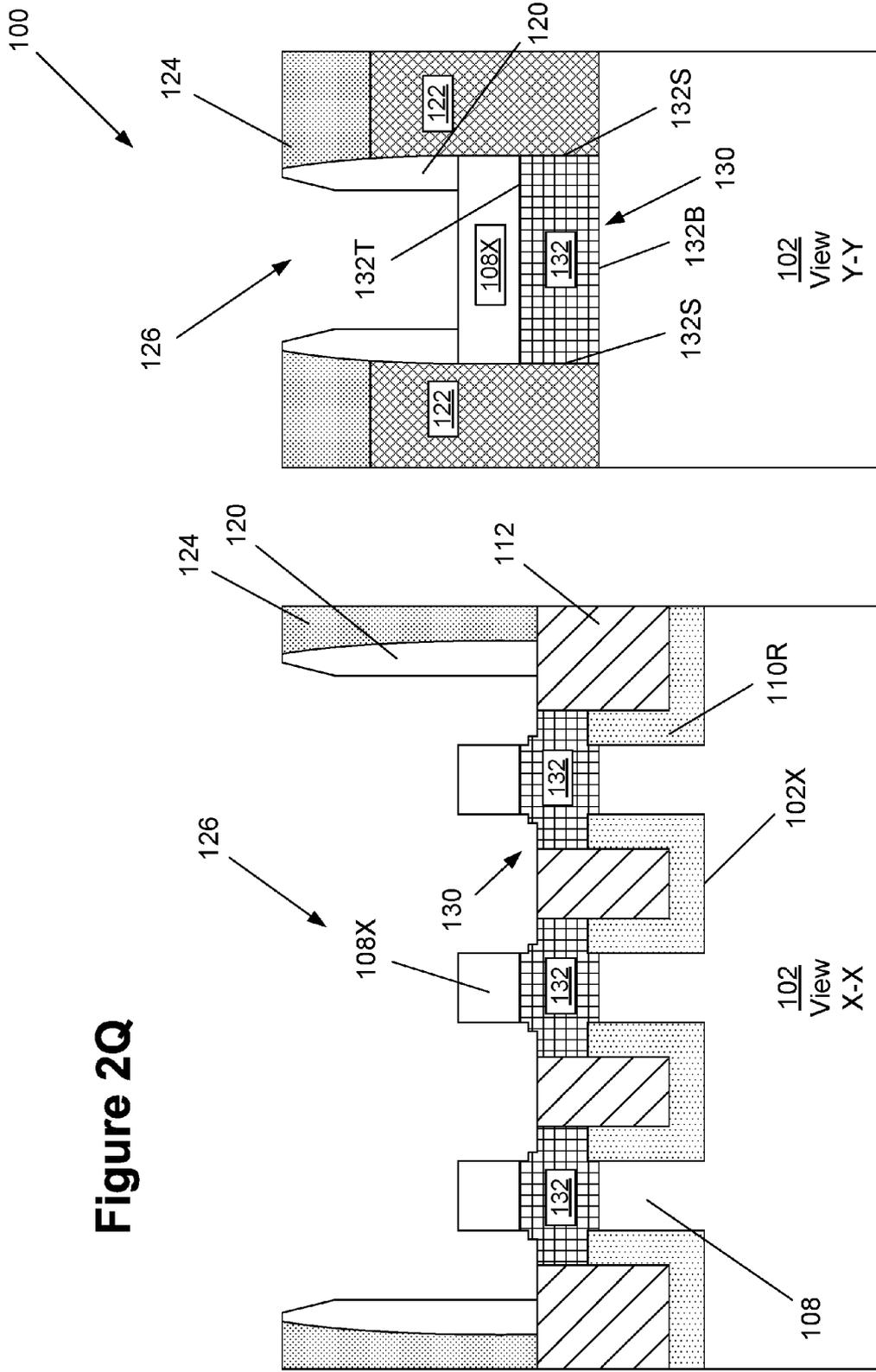
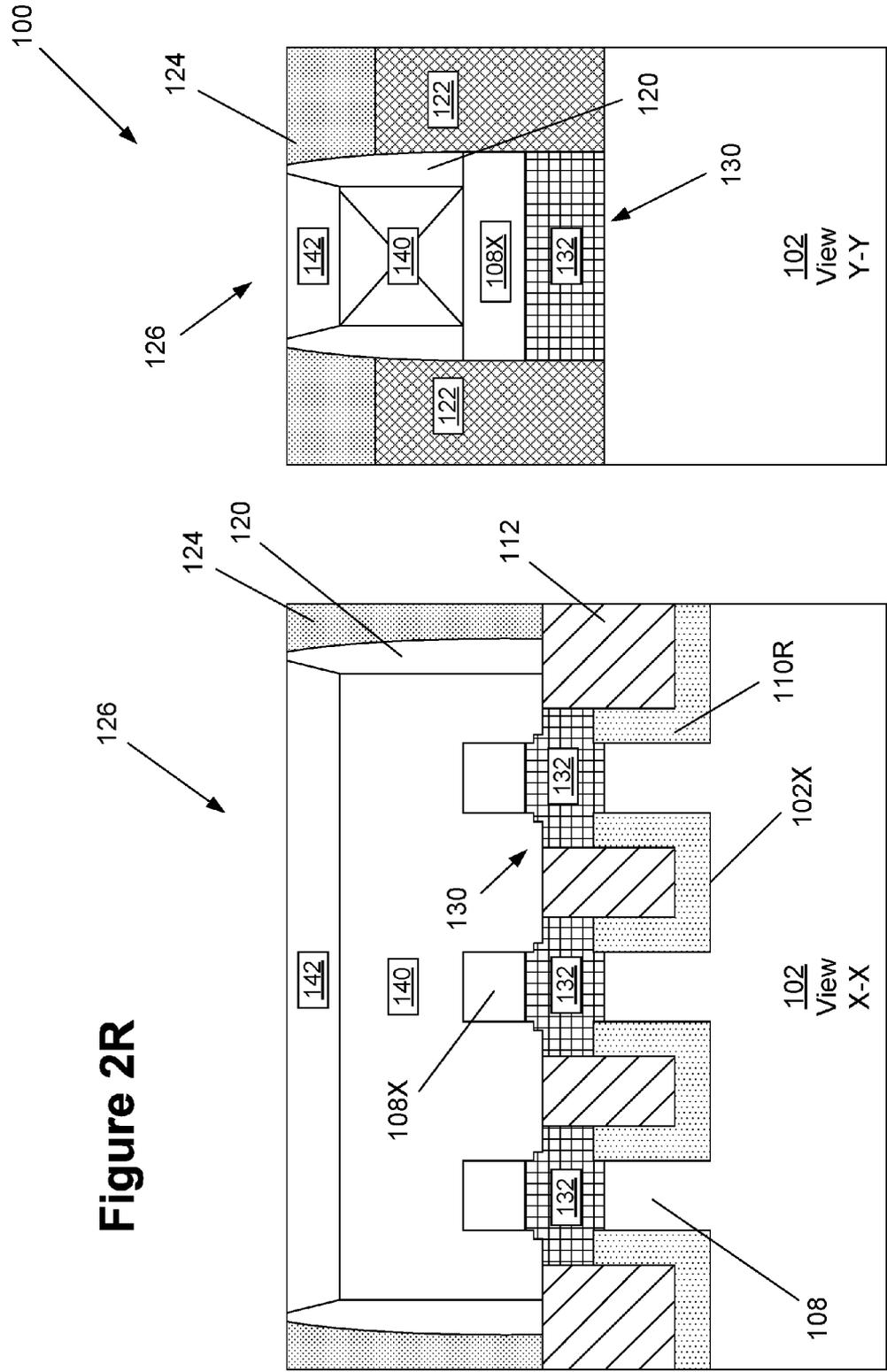




Figure 2Q



**Figure 2R**



## FINFET SEMICONDUCTOR DEVICES WITH STRESSED CHANNEL REGIONS

### BACKGROUND

**[0001]** 1. Field of the Disclosure

**[0002]** Generally, the present disclosure relates to sophisticated integrated circuit devices, and more specifically, to FinFET semiconductor devices having stressed channel regions.

**[0003]** 2. Description of the Related Art

**[0004]** In modern integrated circuits, such as microprocessors, storage devices and the like, a very large number of circuit elements, especially transistors, are provided and operated on a restricted chip area. In integrated circuits fabricated using metal-oxide-semiconductor (MOS) technology, field effect transistors (FETs) (both NMOS and PMOS transistors) are provided that are typically operated in a switching mode. That is, these transistor devices exhibit a highly conductive state (on-state) and a high impedance state (off-state). FETs may take a variety of forms and configurations. For example, among other configurations, FETs may be either so-called planar FET devices or three-dimensional (3D) devices, such as FinFET devices.

**[0005]** A field effect transistor (FET), irrespective of whether an NMOS transistor or a PMOS transistor is considered, and irrespective of whether it is a planar or 3D FinFET device, typically comprises doped source/drain regions that are formed in a semiconductor substrate that are separated by a channel region. A gate insulation layer is positioned above the channel region and a conductive gate electrode is positioned above the gate insulation layer. The gate insulation layer and the gate electrode may sometimes be referred to as the gate structure for the device. By applying an appropriate voltage to the gate electrode, the channel region becomes conductive and current is allowed to flow from the source region to the drain region. In a planar FET device, the gate structure is formed above a substantially planar upper surface of the substrate. In some cases, one or more epitaxial growth processes are performed to form epi semiconductor material in recesses formed in the source/drain regions of the planar FET device. In some cases, the epi material may be formed in the source/drain regions without forming any recesses in the substrate for a planar FET device. The gate structures for such planar FET devices may be manufactured using so-called “gate-first” or “replacement gate” (gate-last) manufacturing techniques.

**[0006]** To improve the operating speed of FETs, and to increase the density of FETs on an integrated circuit device, device designers have greatly reduced the physical size of FETs over the years. More specifically, the channel length of FETs has been significantly decreased, which has resulted in improving the switching speed of FETs. However, decreasing the channel length of a FET also decreases the distance between the source region and the drain region. In some cases, this decrease in the separation between the source and the drain makes it difficult to efficiently inhibit the electrical potential of the source region and the channel from being adversely affected by the electrical potential of the drain. This is sometimes referred to as a so-called short channel effect, wherein the characteristic of the FET as an active switch is degraded.

**[0007]** In contrast to a FET, which has a planar structure, a so-called FinFET device has a three-dimensional (3D) structure. FIG. 1A is a perspective view of an illustrative

prior art FinFET semiconductor device “A” that is formed above a semiconductor substrate B that will be referenced so as to explain, at a very high level, some basic features of a FinFET device. In this example, the FinFET device A includes three illustrative fins C, a gate structure D, sidewall spacers E and a gate cap F. The gate structure D is typically comprised of a layer of insulating material (not separately shown), e.g., a layer of high-k insulating material or silicon dioxide, and one or more conductive material layers (e.g., metal and/or polysilicon) that serve as the gate electrode for the device A. The fins C have a three-dimensional configuration: a height H, a width W and an axial length L. The axial length L corresponds to the direction of current travel in the device A when it is operational. The portions of the fins C covered by the gate structure D is the channel region of the FinFET device A. In a conventional process flow, the portions of the fins C that are positioned outside of the spacers E, i.e., in the source/drain regions of the device A, may be increased in size or even merged together (a situation not shown in FIG. 1A) by performing one or more epitaxial growth processes. The process of increasing the size of or merging the fins C in the source/drain regions of the device A is performed to reduce the resistance of source/drain regions and/or make it easier to establish electrical contact to the source/drain regions. Even if an epi “merger” process is not performed, an epi growth process will typically be performed on the fins C to increase their physical size. In the FinFET device A, the gate structure D may enclose both sides and the upper surface of all or a portion of the fins C to form a tri-gate structure so as to use a channel having a three-dimensional structure instead of a planar structure. In some cases, an insulating cap layer (not shown), e.g., silicon nitride, is positioned at the top of the fins C and the FinFET device only has a dual-gate structure (sidewalls only). The gate structures D for such FinFET devices may be manufactured using so-called “gate-first” or “replacement gate” (gate-last) manufacturing techniques.

**[0008]** Unlike a planar FET, in a FinFET device, a channel is formed perpendicular to a surface of the semiconducting substrate so as to reduce the physical size of the semiconductor device. Also, in a FinFET, the junction capacitance at the drain region of the device is greatly reduced, which tends to significantly reduce short channel effects. When an appropriate voltage is applied to the gate electrode of a FinFET device, the surfaces (and the inner portion near the surface) of the fins C, i.e., the vertically oriented sidewalls and the top upper surface of the fin, form a surface inversion layer or a volume inversion layer that contributes to current conduction. In a FinFET device, the “channel-width” is estimated to be about two times (2×) the vertical fin-height plus the width of the top surface of the fin, i.e., the fin width (for a tri-gate device). Multiple fins can be formed in the same foot-print as that of a planar transistor device. Accordingly, for a given plot space (or foot-print), FinFETs tend to be able to generate significantly higher drive current density than planar transistor devices. Additionally, the leakage current of FinFET devices after the device is turned “OFF” is significantly reduced as compared to the leakage current of planar FETs, due to the superior gate electrostatic control of the “fin” channel on FinFET devices. In short, the 3D structure of a FinFET device is a superior MOSFET structure as compared to that of a planar FET, especially in the 20 nm CMOS technology node and beyond.

**[0009]** For many early device technology generations, the gate structures of most transistor elements (planar or FinFET devices) were comprised of a plurality of silicon-based materials, such as a silicon dioxide and/or silicon oxynitride gate insulation layer, in combination with a polysilicon gate electrode. However, as the channel length of aggressively scaled transistor elements has become increasingly smaller, many newer generation devices employ gate structures that contain alternative materials in an effort to avoid the short channel effects which may be associated with the use of traditional silicon-based materials in reduced channel length transistors. For example, in some aggressively scaled transistor elements, which may have channel lengths on the order of approximately 10-32 nm or less, gate structures that include a so-called high-k dielectric gate insulation layer and one or more metal layers that function as the gate electrode (HK/MG) have been implemented. Such alternative gate structures have been shown to provide significantly enhanced operational characteristics over the heretofore more traditional silicon dioxide/polysilicon gate structure configurations.

**[0010]** Depending on the specific overall device requirements, several different high-k materials—i.e., materials having a dielectric constant, or k-value, of approximately 10 or greater—have been used with varying degrees of success for the gate insulation layer in an HK/MG gate electrode structure. For example, in some transistor element designs, a high-k gate insulation layer may include tantalum oxide ( $\text{Ta}_2\text{O}_5$ ), hafnium oxide ( $\text{HfO}_2$ ), zirconium oxide ( $\text{ZrO}_2$ ), titanium oxide ( $\text{TiO}_2$ ), aluminum oxide ( $\text{Al}_2\text{O}_3$ ), hafnium silicates ( $\text{HfSiO}_x$ ) and the like. Furthermore, one or more non-polysilicon metal gate electrode materials—i.e., a metal gate stack—may be used in HK/MG configurations so as to control the work function of the transistor. These metal gate electrode materials may include, for example, one or more layers of titanium (Ti), titanium nitride (TiN), titanium-aluminum (TiAl), titanium-aluminum-carbon (TiAlC), aluminum (Al), aluminum nitride (AlN), tantalum (Ta), tantalum nitride (TaN), tantalum carbide (TaC), tantalum carbonitride (TaCN), tantalum silicon nitride (TaSiN), tantalum silicide (TaSi) and the like.

**[0011]** One well-known processing method that has been used for forming a transistor with a high-k/metal gate structure is the so-called “gate last” or “replacement gate” technique.

**[0012]** Generally, the replacement gate process may be used when forming either planar devices or 3D devices. FIGS. 1B-1F simplistically illustrate one exemplary prior art method for forming an HK/MG replacement gate structure using a replacement gate technique on a planar transistor device. As shown in FIG. 1B, the process includes the formation of a basic transistor structure above a semiconductor substrate **12** in an active area defined by a shallow trench isolation structure **13**. At the point of fabrication depicted in FIG. 1B, the device **10** includes a sacrificial gate insulation layer **14**, a dummy or sacrificial gate electrode **15**, sidewall spacers **16**, a layer of insulating material **17** and source/drain regions **18** formed in the substrate **12**. The various components and structures of the device **10** may be formed using a variety of different materials and by performing a variety of known techniques. For example, the sacrificial gate insulation layer **14** may be comprised of silicon dioxide, the sacrificial gate electrode **15** may be comprised of polysilicon, the sidewall spacers **16** may be

comprised of silicon nitride and the layer of insulating material **17** may be comprised of silicon dioxide. The source/drain regions **18** may be comprised of implanted dopant materials (N-type dopants for NMOS devices and P-type dopants for PMOS devices) that are implanted into the substrate **12** using known masking and ion implantation techniques. Of course, those skilled in the art will recognize that there are other features of the transistor **10** that are not depicted in the drawings for purposes of clarity. For example, so-called halo implant regions are not depicted in the drawings, as well as various layers or regions of silicon/germanium that are typically found in high performance PMOS transistors. At the point of fabrication depicted in FIG. 1B, the various structures of the device **10** have been formed and a chemical mechanical polishing (CMP) process has been performed to remove any materials above the sacrificial gate electrode **15** (such as a protective cap layer (not shown) comprised of silicon nitride) so that at least the sacrificial gate electrode **15** may be removed.

**[0013]** As shown in FIG. 1C, one or more etching processes are performed to remove the sacrificial gate electrode **15** and the sacrificial gate insulation layer **14** to thereby define a gate cavity **20** where a replacement gate structure will subsequently be formed. Typically, the sacrificial gate insulation layer **14** is removed as part of the replacement gate technique, as depicted herein. However, the sacrificial gate insulation layer **14** may not be removed in all applications. Even in cases where the sacrificial gate insulation layer **14** is intentionally removed, there will typically be a very thin native oxide layer (not shown) that forms on the substrate **12** within the gate cavity **20**.

**[0014]** Next, as shown in FIG. 1D, various layers of material that will constitute a replacement gate structure **30** are formed in the gate cavity **20**. The materials used for the replacement gate structures **30** for NMOS and PMOS devices are typically different. For example, the replacement gate structure **30** for an NMOS device may be comprised of a high-k gate insulation layer **30A**, such as hafnium oxide, having a thickness of approximately 2 nm, a first metal layer **30B** (e.g., a layer of titanium nitride with a thickness of about 1-2 nm), a second metal layer **30C**—a so-called work function adjusting metal layer for the NMOS device—(e.g., a layer of titanium-aluminum or titanium-aluminum-carbon with a thickness of about 5 nm), a third metal layer **30D** (e.g., a layer of titanium nitride with a thickness of about 1-2 nm) and a bulk metal layer **30E**, such as aluminum or tungsten.

**[0015]** Ultimately, as shown in FIG. 1E, one or more CMP processes are performed to remove excess portions of the gate insulation layer **30A**, the first metal layer **30B**, the second metal layer **30C**, the third metal layer **30D** and the bulk metal layer **30E** positioned outside of the gate cavity **20** to thereby define the replacement gate structure **30** for an illustrative NMOS device. Typically, the replacement metal gate structure **30** for a PMOS device does not include as many metal layers as does an NMOS device. For example, the gate structure **30** for a PMOS device may only include the high-k gate insulation layer **30A**, a single layer of titanium nitride—the work function adjusting metal for the PMOS device—having a thickness of about 3-4 nm, and the bulk metal layer **30E**.

**[0016]** FIG. 1F depicts the device **10** after several process operations were performed. First, one or more recess etching processes were performed to remove upper portions of the

various materials within the cavity 20 so as to form a recess within the gate cavity 20. Then, a gate cap layer 31 was formed in the recess above the recessed gate materials. The gate cap layer 31 is typically comprised of silicon nitride and it may be formed by depositing a layer of gate cap material so as to over-fill the recess formed in the gate cavity and thereafter performing a CMP process to remove excess portions of the gate cap material layer positioned above the surface of the layer of insulating material 17. The gate cap layer 31 is formed so as to protect the underlying gate materials during subsequent processing operations.

[0017] Device designers are under constant pressure to increase the operating speed and electrical performance of transistors and integrated circuit products that employ such transistors. Given that the gate length (the distance between the source and drain regions) on modern transistor devices may be approximately 20-50 nm, and that further scaling is anticipated in the future, device designers have employed a variety of techniques in an effort to improve device performance, e.g., the use of high-k dielectrics, the use of metal gate electrode structures, the incorporation of work function metals in the gate electrode structure and the use of channel stress engineering techniques on transistors (create a tensile stress in the channel region for NMOS transistors and create a compressive stress in the channel region for PMOS transistors). Stress engineering techniques typically involve the formation of specifically made silicon nitride layers that are selectively formed above appropriate transistors, i.e., a layer of silicon nitride that is intended to impart a tensile stress in the channel region of a NMOS transistor would only be formed above the NMOS transistors. Such selective formation may be accomplished by masking the PMOS transistors and then blanket depositing the layer of silicon nitride, or by initially blanket depositing the layer of silicon nitride across the entire substrate and then performing an etching process to selectively remove the silicon nitride from above the PMOS transistors. Conversely, for PMOS transistors, a layer of silicon nitride that is intended to impart a compressive stress in the channel region of a PMOS transistor is formed above the PMOS transistors. The techniques employed in forming such nitride layers with the desired tensile or compressive stress are well known to those skilled in the art.

[0018] As noted above, as the channel length of the transistors has decreased, the pitch between adjacent transistors likewise decreases, thereby limiting the area of space between the transistors. For example, current-day transistors may be fabricated with a channel length that ranges from 20-30 nm with a gate pitch that ranges from 50-70 nm, which results in a spacing between the sidewall spacers on adjacent gate structures of about 10-20 nm. Formation of stress-inducing layers in such a small space is very difficult and it can lead to problems, such as the formation of voids, which may limit the effectiveness of such stress-inducing layers.

[0019] The present disclosure is directed to various methods of forming a stressed channel region for a FinFET semiconductor device and the resulting semiconductor device that may avoid, or at least reduce, the effects of one or more of the problems identified above.

#### SUMMARY OF THE DISCLOSURE

[0020] The following presents a simplified summary of the disclosure in order to provide a basic understanding of some

aspects of the subject matter that is described in further detail below. This summary is not an exhaustive overview of the disclosure, nor is it intended to identify key or critical elements of the subject matter disclosed here. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

[0021] Generally, the present disclosure is directed to various methods of forming a stressed channel region for a FinFET semiconductor device and the resulting semiconductor device. In one illustrative embodiment, a FinFET device is disclosed that includes, among other things, a substrate of a first semiconductor material, a gate structure positioned above the substrate, and sidewall spacers positioned adjacent to the gate structure. Additionally, the illustrative FinFET device includes an epi semiconductor material that is positioned in source and drain regions of the FinFET device and laterally outside of the sidewall spacers, wherein the epi semiconductor material includes a second semiconductor material, and a fin that extends laterally under the gate structure and the sidewall spacers in a gate length direction of the FinFET device, wherein the end surfaces of the fin abut and engage the epi semiconductor material. Furthermore, the FinFET device also includes a stressed material positioned in a channel cavity that is located below the fin, above the substrate, and laterally between the epi semiconductor material, wherein the stressed material has a top surface that abuts and engages a bottom surface of the fin, a bottom surface that abuts and engages the substrate, and end surfaces that abut and engage the epi semiconductor material.

[0022] Also disclosed herein is an exemplary FinFET device that includes a lower fin structure that is defined in a substrate, the lower fin structure including a first semiconductor material, and an upper fin structure that is positioned above the lower fin structure, wherein the upper fin structure has opposing end surfaces and a bottom surface that is separated from a top surface of the lower fin structure by a channel cavity that extends in a gate length direction of the FinFET device between source and drain regions thereof, the upper fin structure including a second semiconductor material. Furthermore, the illustrative FinFET device also includes, among other things, a gate structure positioned above and around the upper fin structure, and an epi semiconductor material positioned in each of the source and drain regions of the FinFET device and include a third semiconductor material, wherein the opposing end surfaces of the upper fin structure abut and engage the epi semiconductor material. Additionally, the disclosed FinFET device further includes a stressed material positioned in the channel cavity, the stressed material having a top surface that abuts and engages the bottom surface of the upper fin structure, a bottom surface that abuts and engages the top surface of the lower fin structure, and opposing end surfaces that abut and engage the epi semiconductor material.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The disclosure may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

[0024] FIG. 1A is a perspective view of one illustrative embodiment of a prior art FinFET device;

[0025] FIGS. 1B-1F depict one illustrative prior art method of forming a gate structure of the transistors using a so-called “replacement gate” technique; and

[0026] FIGS. 2A-2R depict various illustrative methods of forming a stressed channel region for a FinFET semiconductor device and the resulting semiconductor device.

[0027] While the subject matter disclosed herein is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention.

#### DETAILED DESCRIPTION

[0028] Various illustrative embodiments of the present subject matter are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers’ specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

[0029] The present subject matter will now be described with reference to the attached figures. Various systems, structures and devices are schematically depicted in the drawings for purposes of explanation only and so as to not obscure the present disclosure with details that are well known to those skilled in the art. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present disclosure. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, i.e., a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, i.e., a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

[0030] Generally, present disclosure relates to various methods of forming a stressed channel region for a FinFET semiconductor device and the resulting semiconductor device. Moreover, as will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to a variety of devices, including, but not limited to, logic devices, memory devices, etc., and the methods disclosed herein may be employed to form N-type or P-type semiconductor devices. The methods and devices disclosed herein may be employed in manufacturing products using a variety of technologies, e.g., NMOS, PMOS, CMOS, etc., and they may be employed in manu-

facturing a variety of different devices, e.g., memory devices, logic devices, ASICs, etc. As will be appreciated by those skilled in the art after a complete reading of the present application, the inventions disclosed herein may be employed in forming integrated circuit products using a variety of so-called 3D devices, such as FinFETs. For purposes of disclosure, reference will be made to an illustrative process flow wherein a single FinFET device **100** is formed. Moreover, the inventions will be disclosed in the context of forming the gate structures using a replacement gate (“gate-last”) processing technique. Of course, the inventions disclosed herein should not be considered to be limited to the illustrative examples depicted and described herein. With reference to the attached figures, various illustrative embodiments of the methods and devices disclosed herein will now be described in more detail.

[0031] In one embodiment, the illustrative device **100** will be formed in and above the semiconductor substrate **102**, having a bulk configuration. The device **100** may be either an NMOS or a PMOS transistor. Additionally, various doped regions, e.g., source/drain regions, halo implant regions, well regions and the like, are not depicted in the attached drawings. The substrate **102** may be made of silicon or it may be made of materials other than silicon. In other embodiments, the device **100** may be formed on a so-called silicon-on-insulator (SOI) substrate, as described more fully below. Thus, the terms “substrate” or “semiconductor substrate” should be understood to cover all semiconducting materials and all forms of such materials.

[0032] The attached drawings present various views of one illustrative embodiment of a FinFET device **100** that may be formed using the methods disclosed herein. FIG. 2A contains a simplistic plan view of the device **100** (in the upper right corner) that depicts the location where various cross-sectional views depicted in the following drawings will be taken. More specifically, the view “X-X” is a cross-sectional view that is taken through the gate structure of the device in the gate-width direction, and the view “Y-Y” is a cross-sectional view that is taken through the long axis of the fins of the device (i.e., in the current transport or gate-length direction of the device). The illustrative FinFET device **100** disclosed herein will be depicted as being comprised of three illustrative fins **108**. However, as will be recognized by those skilled in the art after a complete reading of the present application, the methods and devices disclosed herein may be employed when manufacturing FinFET devices having any number of fins. The various layers of material depicted in the following drawings may be formed by any of a variety of different known techniques, e.g., a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, a thermal growth process, spin-coating techniques, etc. Moreover, as used herein and in the attached claims, the word “adjacent” is to be given a broad interpretation and should be interpreted to cover situations where one feature actually contacts another feature or is in close proximity to that other feature.

[0033] FIG. 2A depicts the device **100** at a point in fabrication wherein several process operations have been performed. First, an etch stop layer **104** was deposited above the substrate **102**. Next, a hard mask layer **106** was deposited above the etch stop layer **104**. In one example, the hard mask layer **106** may be a layer of silicon nitride. In one embodiment, the etch stop layer **104** may be comprised of a high-k material (k value of **10** or greater) such as hafnium oxide.

The thickness of the etch stop layer **104** and the hard mask layer **106** may vary depending upon the particular application.

[0034] FIG. 2B depicts the device **100** after several additional process operations were performed. First, the hard mask layer **106** and the etch stop layer **104** were patterned using traditional photolithography and etching processes. FIG. 2B depicts the device after all photoresist masks were removed. Then, one or more etching processes, e.g., anisotropic etching processes, were performed through the patterned layers **106/104** to define a plurality of trenches **102X** in the substrate **102**. The formation of the trenches **102X** results in the formation of a plurality of initial fin structures **108**. The width and height of the fin structures **108** as well as the depth of the trenches **102X** may vary depending upon the particular application. Additionally, the overall size, shape and configuration of the trenches **102X** and fins **108** may vary depending on the particular application. In the illustrative examples depicted in most of the attached drawings, the fin-formation trenches **102X** and fins **108** are all depicted as having a uniform size and shape. However, such uniformity in the size and shape of the fin-formation trenches **102X** and the fins **108** is not required to practice at least some aspects of the inventions disclosed herein. In the attached figures, the fin-formation trenches **102X** are depicted as having been formed by performing an anisotropic etching process that results in the fin-formation trenches **102X** having a schematically depicted, generally rectangular configuration. In an actual real-world device, the sidewalls of the fin-formation trenches **102X** may be somewhat inwardly tapered, although that configuration is not depicted in the attached drawings. In some cases, the fin-formation trenches **102X** may have a reentrant profile (not shown) near the bottom of the fin-formation trenches **102X**. To the extent the fin-formation trenches **102X** are formed by performing a wet etching process, the fin-formation trenches **102X** may tend to have a more rounded configuration or non-linear configuration as compared to the generally rectangular configuration of the fin-formation trenches **102X** that are formed by performing an anisotropic etching process. Thus, the size and configuration of the fin-formation trenches **102X**, and the manner in which they are made, as well as the general configuration of the fins **108**, should not be considered a limitation of the present invention. For ease of disclosure, only the substantially rectangular fin-formation trenches **102X** and fins **108** will be depicted in the subsequent drawings.

[0035] FIG. 2C depicts the device **100** after the hard mask layer **106** was removed from the device selectively relative to the etch stop layer **104**.

[0036] FIG. 2D depicts the device after several process operations were performed. First, a liner layer **110** was formed on the device by performing a conformal deposition process. In one illustrative embodiment, the liner layer **110** may be a layer of silicon nitride that has a thickness of about 5-10 nm. Next, a layer of insulating material **112** was blanket-deposited on the device **100**. In one illustrative example, the layer of insulating material **112** may be a layer of silicon dioxide, an oxygen-rich silicon dioxide, etc., and it may be formed by performing a chemical vapor deposition (CVD) process.

[0037] FIG. 2E depicts the device **100** after a chemical mechanical polishing (CMP) process was performed using the liner layer **110** as a polish stop layer.

[0038] FIG. 2F depicts the device **100** after a recess etching process was performed to recess the liner layer **110** relative to the surrounding materials. This recessing process exposes the desired final height **108H** of the fin **108**.

[0039] FIG. 2G depicts the device **100** after a recess etching process was performed to recess the layer of insulating material **112** relative to the surrounding materials. This recessing process should be performed such that the recessed surface **112S** of the layer of insulating material **112** is positioned below the level of the upper surface **110S** of the recessed liner layer **110R**. The difference in the height of the surfaces **110S** and **112S** may vary depending upon the particular application, e.g., 1-3 nm.

[0040] FIG. 2H depicts the device **100** after another etch stop layer **114** was deposited by performing a conformal deposition process, such as an ALD process. The etch stop layer **114** may be made of the same materials as that of the etch stop layer **104**, although such a situation may not be required in all applications. The etch stop layer **114** may be relatively thin, e.g., 2-3 nm.

[0041] FIG. 2I depicts the device **100** after a timed, anisotropic etching process was performed to remove the horizontally positioned portions of the etch stop layer **114**. The etching process results in the formation of protective sidewall spacers **114S** on the sidewalls of the fins **108**.

[0042] FIG. 2J depicts the device **100** after several process operations were performed. First, an illustrative sacrificial gate structure **116**, gate cap layer **118** and sidewall spacers **120** were formed on the device **100**. In this example, the sacrificial gate structure **116** includes a dummy or sacrificial gate electrode comprised of, for example, polysilicon or amorphous silicon. The gate cap layer **118** and the sidewall spacers **120** may be comprised of a material such as silicon nitride. The gate structure **116** and the gate cap layer **118** may be formed by depositing the appropriate layer of material on the device and thereafter patterning those materials using traditional photolithography and etching techniques. The etch stop layer **104** may be used as an etch stop during the gate patterning techniques. After gate patterning is done, exposed portions of the etch stop layer **104** may be removed. Then the sidewall spacers **120** may be formed adjacent the gate structure **116**. The spacers **120** may be formed by depositing a layer of spacer material and thereafter performing an anisotropic etching process. After the spacers **120** were formed, an etching process was performed to remove the portions of the fins **108** in the areas laterally outside of the spacers **120**, i.e., in the source/drain regions of the device. This forms a fin cavity **121** in the source/drain regions of the device **100**. The depth of the fin cavity **121** may vary depending upon the particular application.

[0043] With continuing reference to FIG. 2J, the next process operation involves formation of an epi semiconductor material **122** in the fin cavity **121**. In one illustrative embodiment, the epi semiconductor material **122** may be formed with either a tensile or compressive stress depending upon the type of device (N or P) under construction. In that illustrative situation, the epi semiconductor material **122** imparts a desired stress on the materials in the channel region **123** of the device **100**. The epi semiconductor material **122** may be made by performing a traditional epitaxial deposition process. In one illustrative embodiment, the epi semiconductor material **122** may be made of silicon/germanium ( $S_xGe_{1-x}$ ), where the concentration of the germanium may also vary depending upon the particular application.

FIG. 2J contains a simplistic insert drawing showing one example of a cross-sectional configuration of the epi semiconductor material **122** in the source/drain regions of the device, i.e., laterally outside of the spacers **120**. The insert drawing is a cross-sectional view taken through the source/drain region of the device in the gate width direction of the device. The faceted shape of the epi semiconductor material **122** is due to the crystallographic structure of the substrate **102**, as well as the orientation of the long axis of the fins **108** on the substrate **102**. Of course, the epi semiconductor material **122** in the source/drain regions of the device may have a cross-sectional configuration other than the faceted configuration depicted in FIG. 2J.

[0044] While still referring to FIG. 2J, the next operation involves the formation of a layer of insulating material **124** that was blanket-deposited on the device **100**. In one illustrative example, the layer of insulating material **112** may be a layer of silicon dioxide, an oxygen-rich silicon dioxide, etc., and it may be formed by performing a chemical vapor deposition (CVD) process. Thereafter, a chemical mechanical polishing (CMP) process was performed using the gate cap layer **118** as a polish stop layer.

[0045] FIG. 2K depicts the device **100** after a CMP process was performed to remove the gate cap layer **118** and thereby expose the sacrificial gate structure **116** for removal.

[0046] FIG. 2L depicts the device **100** after one or more etching processes were performed to remove the sacrificial gate structure **116** and thereby define a replacement gate cavity **126** where a replacement gate structure will eventually be formed for the device **100**. During this etching process, the etch stop layer **104** within the gate cavity **126** may serve as an etch stop layer.

[0047] FIG. 2M depicts the device **100** after an anisotropic etching process was performed to remove portions **120X** of the silicon nitride spacers **120** and portions **110X** of the silicon nitride liner layer **110**. By removing portions of the spacers **120**, the opening of the replacement gate cavity **126** is effectively widened thereby making filling of the gate cavity **126** easier.

[0048] FIG. 2N depicts the device **100** after an isotropic etching process was performed to remove any residual portions of the silicon nitride liner layer **110**. This etching process exposes portions of the sidewalls **108S** of the initial fin structures **108** for further processing.

[0049] FIG. 2O depicts the device **100** after an isotropic etching process was performed through the replacement gate cavity **126** to remove the portions of the initial fin structures **108** that are not protected by the etch stop layers **104**, **114** and liner layer **110R**. This results in the formation of a channel cavity **130** for each of the fins **108** and defines the final fins **108X** for the device. This etching process is also selective relative to the epi semiconductor material **122**. The final fins **108X** are anchored to the substrate **102** by the epi semiconductor material **122**.

[0050] FIG. 2P depicts the device **100** after the channel cavity **130** was substantially filled with a stressed material **132**. The stressed material **132** may be formed with either a tensile or compressive stress depending upon the type of device (N or P) under construction, and it may be formed with any desired magnitude of stress, e.g., 0.7-3 GPa (tensile or compressive). In one illustrative example, the stressed material **132** may be a layer of a nitride material, an oxide material or a metal-containing material that is formed by a traditional deposition process, such as silicon nitride, silicon

dioxide or a metal oxide. In another embodiment, the stressed material **132** may be an epi semiconductor material, such as silicon/germanium ( $S_xGe_{1-x}$ ), where the concentration of the germanium may also vary depending upon the particular application. In both embodiments, the stressed material **132** may be formed so as to overfill the channel cavity **130** and an anisotropic etch-back process may then be performed to remove the desired amounts of the stressed material **132** such that the post-etch configuration of the stressed material **132** is substantially as depicted in FIG. 2P.

[0051] With continuing reference to FIG. 2P, according to one illustrative aspect of the various inventions disclosed herein, the stressed material **132** has a top surface **132T** that abuts and engages the bottom surface of the final fin structure **108X** and a bottom surface **132B** that abuts and engages a portion of the substrate **102**. The stressed material **132** also has side surfaces **132W** that are substantially parallel to the long axis of the gate structure of the device (they run in the gate width direction) that abut and engage the epi semiconductor material **122**. The stressed material **132** also has side surfaces **132L** that are substantially parallel to the long axis of the final fin structure **108X** (they run in the gate length direction) that abut and engage the layer of insulating material **112**.

[0052] As will be appreciated by those skilled in the art, the presently disclosed inventions also provide device designers with greater flexibility in manufacturing CMOS-based integrated circuit devices. For example, in some applications, the structure depicted in FIG. 2P may actually represent two devices, an NMOS device comprised of the center fin and the leftmost fin, while the rightmost fin is for a PMOS device. In this example, the depicted stressed material **132** may be tailored for the NMOS device, i.e., it may be formed with a tensile stress. Thereafter, a masking layer **129** (shown in dashed lines in FIG. 2P only) may be formed to mask the NMOS device. At that point, the previously formed tensile-stressed material **132** under the right fin **108X** may be removed from the channel cavity by performing an isotropic etching process. Thereafter, with the masking layer **129** still in position, another stressed material (not shown) tailored for the PMOS device, i.e., it may be formed with a compressive stress, may be formed in the channel cavity **130**. Thereafter, the masking layer **129** may be removed. Thus, the stressed material that is formed in the channel cavities as described herein may be tailored for either NMOS or PMOS devices in CMOS applications.

[0053] FIG. 2Q depicts the device **100** after one or more etching processes were performed to remove any residual portions of the etch stop layers **104**, **114** so as to thereby clear the final fin structure **108X** of any unwanted materials.

[0054] FIG. 2R depicts the device **100** after several process operations were performed. First, several known processing operations were performed to form a schematically depicted replacement gate structure **140** in the gate cavity **126**. The replacement gate structure **140** depicted herein is intended to be representative in nature of any type of gate structure that may be employed in manufacturing integrated circuit products using so-called gate-last (replacement-gate) manufacturing techniques. The replacement gate structure **140** typically comprises a high-k (k value greater than 10) gate insulation layer (not individually shown), such as hafnium oxide, one or more metal layers (not individually shown) (e.g., layers of titanium nitride or TiAlC depending upon the type of transistor device being manufactured), and

a bulk conductive material layer (not individually shown), such as tungsten or aluminum. After the various layers of material that will be present in the replacement gate structure **140** are sequentially deposited in the gate cavity **126**, one or more CMP processes are performed to remove excess portions of the gate materials positioned outside of the gate cavity **126** and above the layer of insulating material **124**, as described in the background section of this application. Then, one or more etching processes were performed to remove upper portions of the various materials within the cavity **126** so as to form the replacement gate structure **140** and to form a recess above the replacement gate structure **140**. Then, a gate cap **142** was formed in the recess above the recessed gate materials. The gate cap **142** is typically comprised of silicon nitride and it may be formed by depositing a layer of gate cap material so as to over-fill the recess formed in the gate cavity **126** above the replacement gate structure **140** and thereafter performing a CMP process to remove excess portions of the gate cap material layer positioned above the surface of the layer of insulating material **124**. The gate cap **142** is formed so as to protect the underlying gate materials during subsequent processing operations. At this point, traditional manufacturing operations may be performed to complete the fabrication of the illustrative FinFET device **100**, e.g., contact formation, formation of metallization layers, etc.

[0055] The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Note that the use of terms, such as “first,” “second,” “third” or “fourth” to describe various processes or structures in this specification and in the attached claims is only used as a shorthand reference to such steps/structures and does not necessarily imply that such steps/structures are performed/formed in that ordered sequence. Of course, depending upon the exact claim language, an ordered sequence of such processes may or may not be required. Accordingly, the protection sought herein is as set forth in the claims below.

What is claimed:

1. A FinFET device, comprising:

a substrate comprising a first semiconductor material;  
 a gate structure positioned above said substrate;  
 sidewall spacers positioned adjacent to said gate structure;  
 an epi semiconductor material positioned in source and drain regions of said FinFET device and laterally outside of said sidewall spacers, said epi semiconductor material comprising a second semiconductor material;  
 a fin extending laterally under said gate structure and said sidewall spacers in a gate length direction of said FinFET device, wherein end surfaces of said fin abut and engage said epi semiconductor material; and  
 a stressed material positioned in a channel cavity that is located below said fin, above said substrate, and laterally between said epi semiconductor material, said stressed material having a top surface that abuts and

engages a bottom surface of said fin, a bottom surface that abuts and engages said substrate, and end surfaces that abut and engage said epi semiconductor material.

2. The FinFET device of claim 1, wherein said stressed material comprises a stressed semiconductor material.

3. The FinFET device of claim 1, wherein said stressed material comprises one of a nitride material, an oxide material, and a metal-containing material.

4. The FinFET device of claim 1, wherein said stressed material is one of a tensile-stressed material and a compressive-stressed material.

5. The FinFET device of claim 1, wherein said substrate is silicon and said epi semiconductor material is silicon/germanium.

6. The FinFET device of claim 1, wherein said fin comprises said first semiconductor material.

7. The FinFET device of claim 1, wherein said first semiconductor material is different from said second semiconductor material.

8. The FinFET device of claim 1, wherein said gate structure comprises a gate insulation layer comprising a high-k insulating material and a gate electrode comprising at least one layer of metal.

9. A FinFET device, comprising:

a lower fin structure defined in a substrate, said lower fin structure comprising a first semiconductor material;

an upper fin structure positioned above said lower fin structure, wherein said upper fin structure has opposing end surfaces and a bottom surface that is separated from a top surface of said lower fin structure by a channel cavity that extends in a gate length direction of said FinFET device between source and drain regions thereof, said upper fin structure comprising a second semiconductor material;

a gate structure positioned above and around said upper fin structure;

an epi semiconductor material positioned in each of said source and drain regions of said FinFET device and comprising a third semiconductor material, wherein said opposing end surfaces of said upper fin structure abut and engage said epi semiconductor material; and

a stressed material positioned in said channel cavity, said stressed material having a top surface that abuts and engages said bottom surface of said upper fin structure, a bottom surface that abuts and engages said top surface of said lower fin structure, and opposing end surfaces that abut and engage said epi semiconductor material.

10. The FinFET device of claim 9, further comprising sidewall spacers positioned adjacent to said gate structure, wherein said upper fin structure and said stressed material extend laterally under said sidewall spacers, and wherein said epi semiconductor material is positioned laterally adjacent to and outside of said sidewall spacers.

11. The FinFET device of claim 9, wherein said stressed material comprises a stressed semiconductor material.

12. The FinFET device of claim 9, wherein said stressed material comprises one of a nitride material, an oxide material, and a metal-containing material.

13. The FinFET device of claim 9, wherein said stressed material is one of a tensile-stressed material and a compressive-stressed material.

14. The FinFET device of claim 9, wherein said first semiconductor material is silicon and said third semiconductor material is silicon/germanium.

15. The FinFET device of claim 9, wherein said first and second semiconductor materials are a same semiconductor material.

16. The FinFET device of claim 9, wherein said first semiconductor material is different from said third semiconductor material.

17. The FinFET device of claim 9, wherein said gate structure comprises a gate insulation layer comprising a high-k insulating material and a gate electrode comprising at least one layer of metal.

\* \* \* \* \*