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(54) Title: MICROSTRIP PHASE SHIFTING REFLECT ARRAY ANTENNA		
(57) Abstract		
<p>A circularly polarized reflect array antenna having a plurality of antenna elements, where each antenna element has an electrically conductive patch, at least two electrically conductive stubs positioned along the periphery of the patch, and at least two switches each operable to connect or disconnect the patch to one of the at least two stubs.</p> <div data-bbox="858 1258 1308 1850" data-label="Diagram"> </div>		

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MICROSTRIP PHASE SHIFTING
REFLECT ARRAY ANTENNA

BACKGROUND OF THE INVENTION

Many radar, electronic warfare and communication systems require a circularly polarized antenna with high gain and low axial ratio. Conventional mechanically scanned reflector antennas can meet these specifications. However, they are bulky, difficult to install, and subject to performance degradation in winds. Planar phased arrays may also be employed in these applications. However, these antennas are costly because of the large number of expensive GaAs Monolithic microwave integrated circuit components, including an amplifier and phase shifter at each array element as well as a feed manifold and complex packaging. Furthermore, attempts to feed each microstrip element from a common input/output port becomes impractical due to the high losses incurred in the long microstrip transmission lines, especially in large arrays.

Conventional microstrip reflect array antennas use an array of microstrip antennas as collecting and radiating elements. Conventional reflect array antennas use either delay lines of fixed lengths connected to each microstrip radiator to produced a fixed beam or use an electronic phase shifter connected to each microstrip radiator to produce an electronically scanning beam. These conventional reflect array antennas are not desirable because the fixed beam reflect arrays suffer from gain ripple over the reflect array operating bandwidth, and the electronically scanned reflect array suffer from high cost and high loss phase shifters.

In U.S. Patent No. 4,053,895 entitled "Electronically Scanned Microstrip Antenna Array" issued to Malagisi on October 11, 1977, antennas having at least two pairs of diametrically opposed short circuit shunt switches placed at different angles around the periphery of a microstrip disk is described. Phase shifting of the circularly polarized reflect array elements is achieved by varying the angular position of the short-circuit plane created by diametrically opposed pairs of diode shunt switches. This antenna is of limited utility because of the complicated labor intensive manufacturing process required to connect the shunt switches and their bias network between the microstrip disk and ground.

It is also known that any desired phase variation across a circularly polarized array can be achieved by mechanically rotating the individual circularly polarized array elements. Miniature mechanical motors or rotators have been used to rotate each array element to the appropriate angular orientation. However, the use of such mechanical rotation devices and the controllers introduce mechanical reliability problems. Further, the manufacturing process of such antennas are labor intensive and costly.

SUMMARY OF THE INVENTION

It has been recognized that it is desirable to provide a high performance circularly polarized beam scanning array antenna that is low in cost and easy to manufacture.

In one aspect of the invention, an antenna array element has an electrically conductive patch, at least two electrically conductive stubs positioned along the periphery of the patch, and at least two switches each operable to connect or disconnect the patch to one of the at least two stubs.

In another aspect of the invention, an antenna includes an array of electrically conductive patches arranged in a predetermined generally equally spaced pattern on a first surface of a substantially flat substrate, at least two electrically conductive stubs positioned along the periphery of each of the patches, and at least two switches coupled between each patch and the at least two stubs. A controller is coupled to each of the at least two switches operable to connect or disconnect a selected one of the at least two stubs to each patch.

In another aspect of the present invention, a method of electronically phase shifting array elements in a reflect array antenna includes the steps of generating and directing energy toward N sets of patches disposed on a substantially flat surface and arranged in a predetermined pattern thereon, selectively connecting patches, for each of N sets of patches, to a different stub out of N stubs arranged along half of the periphery of each patch, thereby applying a phase shift to the energy, reradiating into space.

In yet another aspect of the present invention, a method of electronically phase shifting array elements in a reflect array antenna includes the steps of generating and directing energy toward N sets of patches disposed on a substantially flat surface and arranged in a predetermined pattern thereon, selectively connecting patches, for each of N sets of patches, to a different pair of diametrically opposed stubs out of N pairs of diametrically opposed stubs arranged along the periphery of each patch, thereby phase shifting the energy, and reradiating the energy into space.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference may be made to the accompanying drawings, in which:

5 FIGURE 1 is a schematic representation of the array element constructed according to an embodiment of the present invention;

10 FIGURE 2A is a perspective view of a microstrip phase shifting reflect array antenna shown with an offset feed horn constructed according to an embodiment of the present invention;

15 FIGURE 2B is an enlarged view of an inset shown in FIGURE 2A showing the array elements of the antenna and the phase state and rotation angles thereof constructed according to an embodiment of the present invention;

 FIGURE 3 is a cross-sectional view of an embodiment of an array element constructed according to the teachings of the present invention;

20 FIGURE 4 is a cross-sectional view of another embodiment of an array element constructed according to the teachings of the present invention;

 FIGURE 5 is a cross-sectional view of another embodiment of an array element constructed according to the teachings of the present invention; and

25 FIGURE 6 is a cross-sectional view of yet another embodiment of an array element constructed according to the teachings of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIGURE 1, a detailed schematic representation of an array element 10 for a microstrip phase shifting reflect array antenna constructed according to the teachings of the present invention is shown. Array element 10 includes an electrically conductive microstrip patch 12, which is preferably circular in shape. Arranged radially around patch 12 are a plurality of stubs 14 also constructed of an electrically conductive material. Each stub 14 is coupled to the periphery or edge of microstrip patch 12 by a low loss switch 16, such as a diode (shown), transistor, micromechanical switch, electromechanical switch and the like. When forward biased, the diode switch connects the respective stub 14 to microstrip patch 12; when reverse biased, the diode switch disconnects the respective stub 14 from microstrip patch 12. At any one instant during the operation of the antenna, switch controllers 18 generate and send control signals to switches 16 so that only two diametrically opposed stubs are connected to each microstrip patch 12 with the rest disconnected therefrom. Therefore, depending on which two diametrically opposed stubs are connected to patch 12, a rotational effect and electronic phase shift is achieved. Although FIGURE 1 is shown with only two stubs coupled to controller 18 for the sake of clarity and simplicity, it may be understood that all the radial stubs are coupled to controller 18, which controls the connectivity thereof to the microstrip patch.

Referring to FIGURES 2A and 2B, a microstrip phase shifting reflect array antenna 20 constructed in accordance with the teachings of the present invention is shown. Antenna 20 may include a substantially flat dielectric substrate 22 upon which a plurality of array elements 24 are disposed in a regular and repeating pattern. As shown in FIGURES 2A and 2B, array elements 24 are arranged in

rows and columns on disk 22, but may be arranged in other random or concentric patterns in accordance with array antenna theory. A feed horn 26 is located above disk 22, either offset (as shown) or centered, over the plurality of array elements 24. Array elements 24 may be etched on a ceramic filled PTFE substrate, which may be supported and strengthened by a thicker flat panel 28. Although antenna 20 is shown on a substantially flat substrate, the invention contemplates substrates that may be curved or conformed to some physical contour due to installation requirements or space limitations. The variation in the substrate plane geometry, the spherical wave front from the feed and to steer the beam may be corrected by modifying the phase shift state of array elements 24. Furthermore, the substrate may be fabricated in sections and then assembled on site to increase the portability of the antenna and facilitate its installation and deployment.

In FIGURE 2B, a portion of the plurality of array elements 24 is shown to demonstrate the phase states and respective rotation angles for a LHCP (left hand circularly polarized) Ku-Band reflect array. As shown in FIGURE 1, array element 10 includes 16 stubs and thus eight different rotation angles which correspond to eight phase states. This configuration is equivalent to a three-bit phase shifter. TABLES A and B below list the angular stub positions required for a three-bit and four-bit microstrip phase shifting reflect array antenna with diametrically located stubs.

3-Bit Phase Shift (degrees)	Rotation of Diametrically Located Stubs for RHCP (degrees)	
	Stub 1	Stub 2
0	0	180
45	22.5	202.5
90	45	225
135	67.5	247.5
180	90	270
225	112.5	292.5
270	135	325
315	157.5	347.5

TABLE A

4-Bit Phase Shift (degrees)	Rotation of Diametrically Located Stubs for RHCP (degrees)	
	Stub 1	Stub 2
0	0	180
22.5	11.25	191.25
45	22.5	202.5
67.5	33.75	213.75
90	45	225
112.5	56.25	236.25
135	67.5	247.5
157.5	78.75	258.75
180	90	270
202.5	101.25	281.25
225	112.5	292.5
247.5	123.75	303.75
270	135	315
292.5	146.25	326.25
315	157.5	337.5
337.5	168.75	348.75

TABLE B

A more efficient array element configuration requires only one stub connection at each rotational angle. Therefore, only one stub rather than two diametrically opposed stubs connected to patch 22 at any one instant has the same effect. This characteristic may be utilized advantageously to reduce the fabrication cost and complexity or to increase the robustness and reliability of the antenna. For each phase state, one stub and its

connection may fail without adversely impacting the antenna operation. For example referring to FIGURE 1, if all stubs in set B fail, the remaining stubs in set A will still enable array element 10 to function. TABLES C and D below list the angular stub positions for a three-bit and four-bit microstrip phase shifting reflect array antenna with single stubs, respectively.

3-Bit Phase Shift (degrees)	Single Stub (degrees)
0	0 or 180
45	22.5 or 202.5
90	45 or 225
135	67.5 or 247.5
180	90 or 270
225	12.5 or 292.5
270	135 or 325
315	157.5 or 347.5

TABLE C

5		4-Bit Phase Shift (degrees)	Single Stub (degrees)
		0	0 or 180
		22.5	11.25 or 191.25
		45	22.5 or 202.5
		67.5	33.75 or 213.75
10		90	45 or 225
		112.5	56.25 or 236.25
		135	67.5 or 247.5
		157.5	78.75 or 258.75
		180	90 or 270
15		202.5	101.25 or 281.25
		225	112.5 or 292.5
		247.5	123.75 or 303.75
		270	135 or 315
		292.5	146.25 or 326.25
20		315	157.5 or 337.5
		337.5	168.75 or 348.75

TABLE D

25 Alternatively, phase shifting may also be accomplished by selectively connecting every other stub arranged around the patch thereto.

30 FIGURE 3 is a cross-sectional view of one embodiment of an array element 30 according to the teachings of the present invention. Array element 30 includes a microstrip patch 32, a plurality of radial stubs 34 and respective switches 36 fabricated or mounted on a first side of a dielectric substrate with at least a top layer 40 and a bottom layer 42. An electrical reference or ground plane 35 38 may be sandwiched between dielectric layers 40 and 42

and coupled to the center of microstrip patch 32 by via 48. Stubs 34 may be coupled to switch control transmission lines 46 disposed on a second side of the dielectric substrate by DC vias 44. Switch control transmission lines 46 are coupled to one or more switch controllers 18, which may be mounted on the surface of bottom dielectric layer 42.

Microstrip phase shifting reflect array antenna 20 containing array element 30 may be constructed using conventional circuit board fabrication processes. For example, vias 44 and 48 may be formed in copper clad ceramic filled PTFE substrates, and array element patches 32 and stubs 34 may be formed by etching the copper cladding. Array element patches 32 may be of a shape other than circular. Switches 36 and switch controllers 18 may then be mounted on the dielectric substrate using standard chip on board or surface mount techniques.

Referring to FIGURE 4, a cross-sectional view of another embodiment of an array element 60 is shown. Array element 60 includes a microstrip patch 62 disposed on a top side of a dielectric substrate 70. A plurality of radial stubs 64 are disposed on a bottom side of a second dielectric substrate 72 which is bonded or coupled to dielectric substrate 70 with a ground reference plane 68 disposed therebetween. Switches 66 are coupled to stubs and switch control transmission lines 64 and also to RF vias 74 leading to the periphery of microstrip patch 62. In this embodiment, because microstrip patches 62 and stubs 64 are disposed on different sides of the multi-layer dielectric substrate, the array elements can be placed closer together to increase the compactness of the antenna. Further, this configuration also reduces reflections from and coupling with the stubs. The stubs may also be fabricated in stripline to reduce coupling with the DC layers.

FIGURE 5 is a cross-sectional view of yet another embodiment of an array element 80 constructed on a semiconductor and dielectric or semiconductor substrate 102 and 104 according to the teachings of the present invention. Array element 80 includes a microstrip patch 82 and its stubs 84 formed on the surface of semiconductor substrate 102. Semiconductor substrate 102 may be silicon, gallium arsenide, or like materials. Between the edge of microstrip patch 82 and stubs 84, a plurality of PIN junction switch 86 or PN junction switch 87 are formed on the surface of semiconductor substrate 102. The fabrication of PIN or PN junctions employs conventional or known semiconductor processes such as epitaxial growth, ion implantation, diffusion and the like and therefore is not described in detail herein. PIN junction switch 86 includes a p-type region 91, an intrinsic region 93, and an n-type region 95. PN junction switch 87 includes an n+ region 90, an n-type region 92, and a p-type region 94. Accordingly, semiconductor substrate 102 may be of a p-type material with intrinsic region 93 and n-type regions 90, 92 and 95 implanted, grown or otherwise formed therein; alternatively, semiconductor substrate 102 may be of an n-type material with intrinsic region 93 and p-type regions 91 and 94 implanted, grown or otherwise formed therein.

Microstrip patch 82 is coupled to a ground or reference plane 100 sandwiched between semiconductor substrate 102 and dielectric or semiconductor substrate 104. The switch controllers 18 and switch control transmission lines 86 may be mounted and formed on the surface of the dielectric or semiconductor substrate 104. Vias 106 couple switch control transmission lines 86 to radial stubs 84 for conveying DC control signals from the switch controllers to radial stubs 84. The center of microstrip patch 82 is coupled to ground plane 100 by via 108.

Referring to yet another embodiment of an array element 120 shown in FIGURE 6. Array element 120 is also constructed on a semiconductor substrate 132 and a dielectric substrate 134 with a ground plane 130 sandwiched therebetween. A microstrip patch 122 is disposed on the surface of semiconductor substrate 132 and its center is coupled to ground plane 130 by via 140. PIN junction switches 126 are formed at the periphery of microstrip patch 122 between microstrip patch 122 and an intermediate plane 125. PIN junction switches 126 includes a p-type region 127 disposed immediately below the periphery of the microstrip patch 122, an n-type region 129 disposed above intermediate plane 125, and an intrinsic region 123 disposed therebetween. Radial stubs and switch control transmission lines 124 are formed on the surface of dielectric substrate 134, and switch controllers 18 may be mounted on the same surface. Radial stubs 124 are coupled to intermediate plane 125 and PIN junction switch 126 by DC vias 128. This configuration allows array elements 120 to be placed more closely together compared with the embodiment shown in FIGURE 5.

Constructed in this manner, the switches, whether they be diodes, transistors, PIN junctions, PN junctions, or any low loss switch, are biased appropriately to either connect or disconnect the radial stubs from the periphery of the microstrip patches to effect beam scanning.

The reflect array antenna of the present invention is more reliable than conventional reflect arrays or phased arrays. Given that a conventional 4-Bit delay line phase shifter and a microstrip phase shifting reflect array antenna use the same type of switches, and

$$N = 2^B \quad (1)$$

where N is the number of states and B is the number of bits. Then an array element with orthogonal stubs will have 2N diodes. The number of diodes in a delay line phase shifter is given by

$$MB \quad (2)$$

5 where M is the number of diodes per bit and B is the number of bits. If p is the probability of failure for a single diode then the probability of success for the antenna is given by

$$P_{MDPSA} = \frac{N-1}{N} + \frac{1}{N}(1-p)^2 \cong 1 - \frac{2p}{N} \quad (3)$$

and the probability of failure is

$$P_{MDPSA}^F \approx \frac{2p}{N} \quad (4)$$

10 Similarly, the probability of success for the delay line phase shifter is given by

$$P_{DL} = (1-p)^{MB} \quad (5)$$

and the delay line phase shifter probability of failure is

$$P_{DL}^F = MBp \quad (6)$$

15 The increased failure rate of the delay line phase shifter over the microstrip phase shifting reflect array antenna is given by

$$\frac{P_{DL}^F}{P_{MDPSA}^F} \cong \frac{MBp}{\left(\frac{2p}{N}\right)} = \frac{MBN}{2} = \frac{M}{2} N \log_2 N \quad (7)$$

Therefore, for a conventional 4-Bit delay line phase shifter with $M=4$ and a microstrip phase shifting reflect array antenna with orthogonal stubs and $N=16$, the antenna is at least 128 times more reliable. Furthermore, since the microstrip phase shifting reflect array elements do not have amplifiers at each element, they generate much less heat, therefore, do not suffer the damaging effects associated with high temperature thermal cycling. Finally, the phase shifting reflect array has no moving parts. For these reasons the microstrip phase shifting reflect array should exhibit higher electrical and mechanical reliability than phased array or mechanically steered antennas.

Although several embodiments of the present invention and its advantages have been described in detail, it should be understood that various mutations, changes, substitutions, transformations, modifications, variations, and alterations can be made therein without departing from the teachings of the present invention, the spirit and scope of the invention being set forth by the appended claims.

WHAT IS CLAIMED IS:

1. An antenna element comprising:
an electrically conductive patch;
5 at least two electrically conductive stubs disposed generally orthogonally with respect to the periphery of the patch;
at least one switch operable to connect or disconnect the patch to a selected one of the at least two stubs;
10 a dielectric substrate having a first surface and a second surface;
the patch being disposed on the first surface;
the at least two switches being disposed on the first surface; and
15 the at least two stubs being disposed on the first surface;
switch control lines disposed on the second surface of the dielectric substrate; and
a least two DC vias through the dielectric substrate operable to couple the at least two stubs to the switch control lines.
20
2. The antenna element, as set forth in claim 1, further comprising an electrical reference plane coupled to
25 each patch.
3. The antenna element, as set forth in claim 1, wherein the patch is a circular disk.
- 30 4. The antenna element, as set forth in claim 1, wherein each of the at least two switches comprises a diode coupled between the periphery of the patch and one end of a stub.

5 5. The antenna element, as set forth in claim 1,
wherein the at least two stubs comprise at least two pairs
of diametrically positioned electrically conductive stubs
radially arranged around the periphery of the patch, each
stub having a first end disposed adjacent to the periphery
of the patch and a second end disposed remotely from the
patch, and the at least two switches comprise at least two
pairs of switches operable to connect or disconnect the
periphery of the patch to the first ends of one selected
10 pair of stubs to electronically rotate the patch.

6. The antenna element, as set forth in claim 1,
wherein the at least two stubs and switches comprises:
2N stubs radially arranged and equally spaced along
15 the periphery of the patch; and
N switches each operable to connect and disconnect the
patch to one of N stubs arranged equally spaced along the
periphery of only half of the patch to electronically
rotate the patch.

20 7. The antenna element, as set forth in claim 1,
wherein the at least two stubs comprise eight pairs of
diametrically opposed stubs arranged radially and equally
spaced along the periphery of the patch, and the at least
25 one switch comprises eight switches, each switch operable
to coupled one selected stub of a pair of diametrically
opposed stubs.

8. The antenna element, as set forth in claim 1, wherein the at least two stubs and switches comprise:

N pairs of diametrically opposed stubs arranged radially and equally spaced along the periphery of the patch; and

N switches operable to connect or disconnect one selected stub of each pair of diametrically opposed stubs to electronically rotate the patch.

9. An antenna element comprising:

an electrically conductive patch;

at least two electrically conductive stubs disposed
generally orthogonally with respect to the periphery of the
patch;

at least one switch operable to connect or disconnect
the patch to a selected one of the at least two stubs;

a dielectric substrate having a first surface and a
second surface;

the patch being disposed on the first surface;

the at least two switches being disposed on the second
surface;

the at least two stubs being disposed on the second
surface; and

at least two RF vias through the dielectric substrate
operable to couple the patch to the at least two switches.

10. The antenna element, as set forth in claim 9,
further comprising switch control lines disposed on the
second surface of the dielectric substrate coupled to the
at least two stubs.

11. An antenna element comprising:

an electrically conductive patch;

at least two electrically conductive stubs disposed generally orthogonally with respect to the periphery of the patch;

at least one switch operable to connect or disconnect the patch to a selected one of the at least two stubs;

a semiconductor substrate having a first surface and a second surface;

the patch being disposed on the first surface;

the at least two stubs being disposed on the first surface; and

at least two p-n junction switches defined in the first surface of the semiconductor substrate between the periphery of the patch and the at least two stubs.

12. The antenna element, as set forth in claim 11, further comprising:

a dielectric substrate having a first surface and a second surface;

switch control lines disposed on the second surface of the semiconductor dielectric substrate; and

at least two DC vias through the semiconductor substrate and dielectric substrates operable to couple the at least two stubs to the switch control lines.

13. The antenna element, as set forth in claim 12, further comprising switch control lines disposed at the interface between the second surface of the semiconductor substrate and the first surface of the dielectric substrate, and the switch control lines being coupled to the PIN junctions and the at least two stubs by the at least two RF vias.

14. An antenna element comprising:

an electrically conductive patch;

at least two electrically conductive stubs disposed
generally orthogonally with respect to the periphery of the
patch;

at least one switch operable to connect or disconnect
the patch to a selected one of the at least two stubs;

a semiconductor substrate having a first surface and
a second surface;

the patch being disposed on the first surface;

the at least two stubs being disposed on the first
surface; and

at least two PIN junctions defined in the first
surface of the semiconductor substrate between the
periphery of the patch and the at least two stubs.

15. The antenna element, as set forth in claim 14,
further comprising:

a dielectric substrate having a first surface and a
second surface;

switch control lines disposed on the second surface of
the dielectric substrate; and

a least two DC vias through the semiconductor and
dielectric substrates operable to couple the at least two
stubs to the switch control lines.

16. An antenna element comprising:

an electrically conductive patch;

at least two electrically conductive stubs disposed generally orthogonally with respect to the periphery of the patch;

at least one switch operable to connect or disconnect the patch to a selected one of the at least two stubs;

an electrical reference plane coupled to each patch;

a semiconductor substrate having a first surface and a second surface;

a dielectric substrate having a first surface and a second surface, the electrical reference plane being disposed between the second surface of the semiconductor substrate and the first surface of the dielectric substrate;

the patch being disposed on the first surface of the semiconductor substrate;

the at least two stubs being disposed on the second surface of the dielectric substrate;

at least two PIN junctions defined in the semiconductor substrate between the periphery of the patch and the at least two stubs; and

at least two RF vias through the dielectric substrate operable to couple the at least two PIN junctions to the at least two stubs disposed on the second surface of the dielectric substrate.

17. An antenna comprising:

an array of electrically conductive patches arranged in a predetermined pattern on a first surface of a substrate having a first surface and a second surface, and wherein all patches, the switches and stubs are disposed on the first surface of the substrate;

at least two electrically conductive stubs positioned generally orthogonally with respect to the periphery of each of the patches;

at least two switches disposed between each patch and the at least two stubs; and

a controller coupled to each of the at least two switches operable to connect or disconnect a selected one of the at least two stubs to each patch to electronically phase shift the patches;

switch control lines disposed on the second surface of the substrate; and

a least two DC vias through the substrate operable to couple the stubs to the switch control lines.

18. The antenna, as set forth in claim 17, further comprising an electrical reference plane coupled to each patch.

19. The antenna, as set forth in claim 17, wherein the substrate is substantially flat and comprises at least one dielectric substrate disposed adjacent the electrical reference plane.

20. The antenna, as set forth in claim 17, wherein each patch is a circular disk.

21. The antenna, as set forth in claim 17, wherein each of the at least two switches comprises a diode coupled between the periphery of the patch and one end of a stub.

22. The antenna, as set forth in claim 17, wherein the at least two stubs comprise at least two pairs of diametrically positioned electrically conductive stubs positioned radially around the periphery of the patch, and the at least two switches comprise at least two pairs of switches operable to connect or disconnect the periphery of the patch to one selected pair of diametrically opposed stubs.

23. The antenna, as set forth in claim 17, wherein each patch is dissected into two halves and the at least two stubs comprise eight stubs arranged along the periphery of only one half of the patch.

24. The antenna, as set forth in claim 17, wherein the at least two stubs comprise eight pairs of diametrically opposed stubs arranged along the periphery of the patch.

25. The antenna, as set forth in claim 17, wherein the substrate comprises a dielectric substrate.

26. The antenna, as set forth in claim 17, wherein the substrate comprises a dielectric substrate having a first surface and a second surface, and wherein the patches are disposed on the first surface of the dielectric substrate, and the switches and stubs are disposed on the second surface of the dielectric substrate.

27. The antenna, as set forth in claim 26, further comprising RF vias through the dielectric substrate operable to couple the patches to the switches.

28. The antenna, as set forth in claim 27, further comprising switch control lines disposed on the second surface of the dielectric substrate coupled to the stubs.

5 29. The antenna, as set forth in claim 17, wherein the substrate comprises a semiconductor substrate having a first surface and a second surface, the patches and the stubs being disposed on the first surface of the semiconductor substrate, and at least two p-n junction
10 switches defined in the first surface of the semiconductor substrate between the periphery of the patch and the stubs.

 30. The antenna, as set forth in claim 29, wherein the substrate further comprises a dielectric substrate
15 disposed adjacent to the semiconductor substrate, the dielectric substrate having a first surface adjacent to the second surface of the semiconductor substrate and a second surface, the antenna further comprising:

 switch control lines disposed on the second surface of
20 the dielectric substrate; and

 a least two DC vias through the semiconductor and dielectric substrates operable to couple the stubs to the switch control lines.

25 31. The antenna, as set forth in claim 17, wherein the substrate further comprises a dielectric substrate disposed adjacent to the semiconductor substrate, the dielectric substrate having a first surface adjacent to the second surface of the semiconductor substrate and a second
30 surface, the patches, the stubs being disposed on the first surface, and the PIN junctions being defined in the first surface of the semiconductor substrate between the periphery of the patches and the stubs.

32. The antenna, as set forth in claim 31, further comprising:

switch control lines disposed on the second surface of the dielectric substrate; and

5 a least two DC vias through the semiconductor and dielectric substrates operable to couple the stubs to the switch control lines.

33. The antenna, as set forth in claim 17, wherein
10 the substrate further comprises a dielectric substrate disposed adjacent to the semiconductor substrate, the dielectric substrate having a first surface adjacent to the second surface of the semiconductor substrate and a second surface, the electrical reference plane being disposed
15 between the second surface of the semiconductor substrate and the first surface of the dielectric substrate, the patches being disposed on the first surface of the semiconductor substrate, the stubs being disposed on the second surface of the dielectric substrate, the PIN
20 junctions being defined in the semiconductor substrate between the periphery of the patch and the stubs, and RF vias through the dielectric substrate operable to couple the PIN junctions to the stubs disposed on the second surface of the dielectric substrate.

25

34. The antenna, as set forth in claim 33, further comprising switch control lines disposed at the interface between the second surface of the semiconductor substrate and the first surface of the dielectric substrate, and the
30 switch control lines being coupled to the PIN junctions and the at least two stubs by the RF vias.

35. The antenna, as set forth in claim 17, wherein the array of patches are divided into N sets of patches, the patches of each set being arranged in a predetermined pattern on the substantially flat substrate, each patch having N pairs of diametrically opposed stubs arranged substantially equally spaced along the periphery thereof, and the patches in each N set of patches each having a different pair of the N pairs of diametrically opposed stubs selectively coupled to the patch by the switches.

FIG. 2B

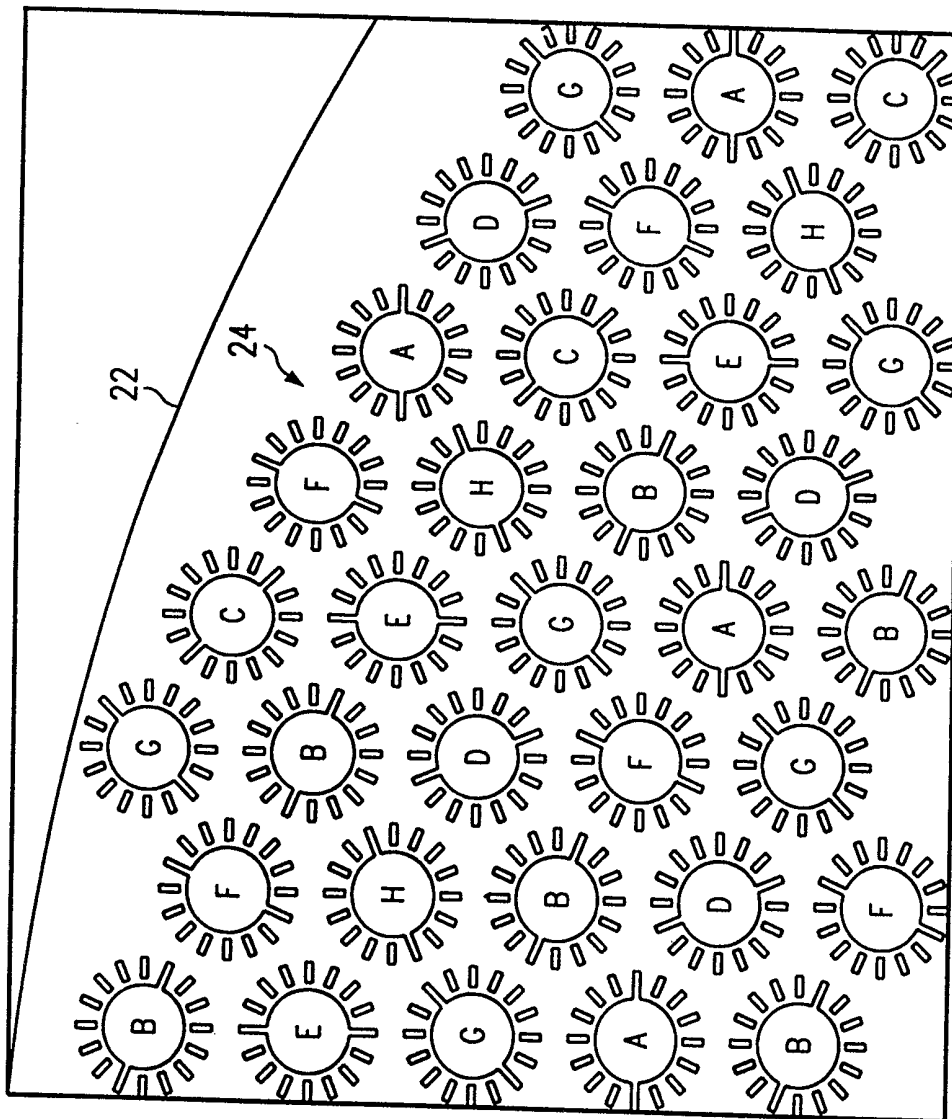
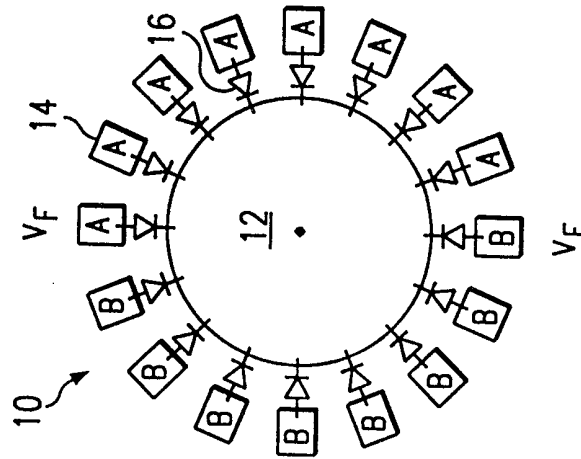
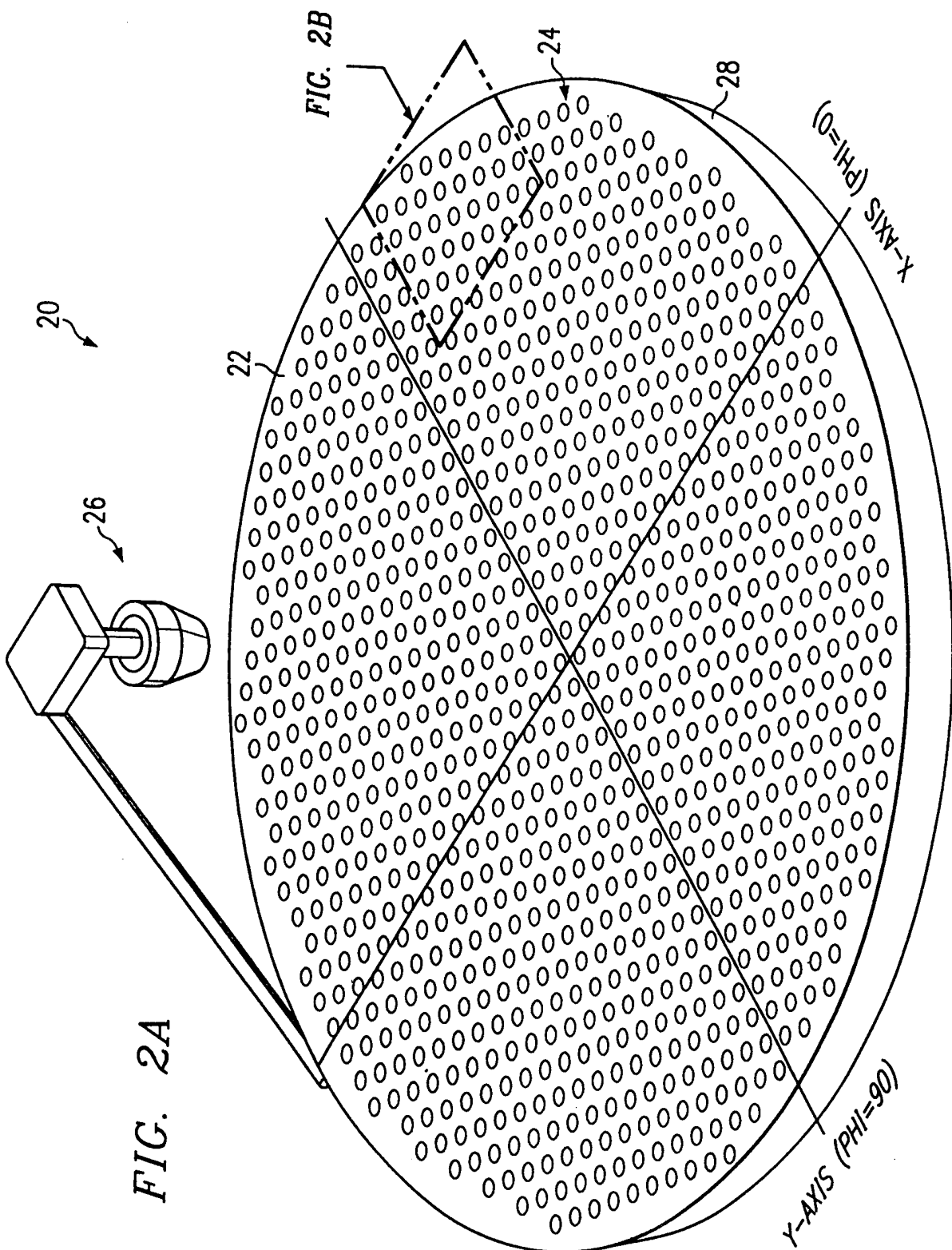
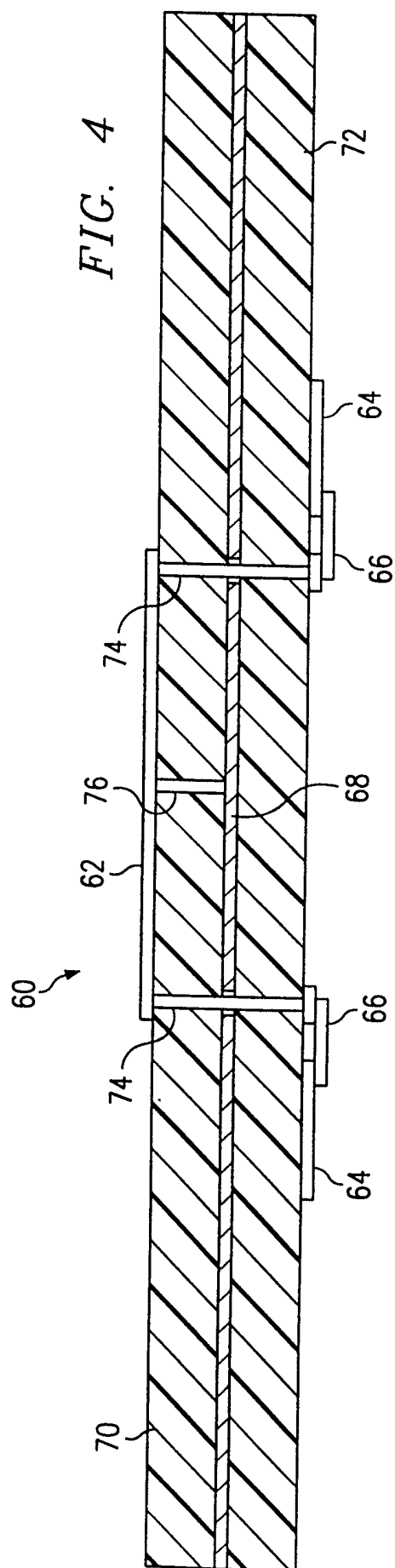
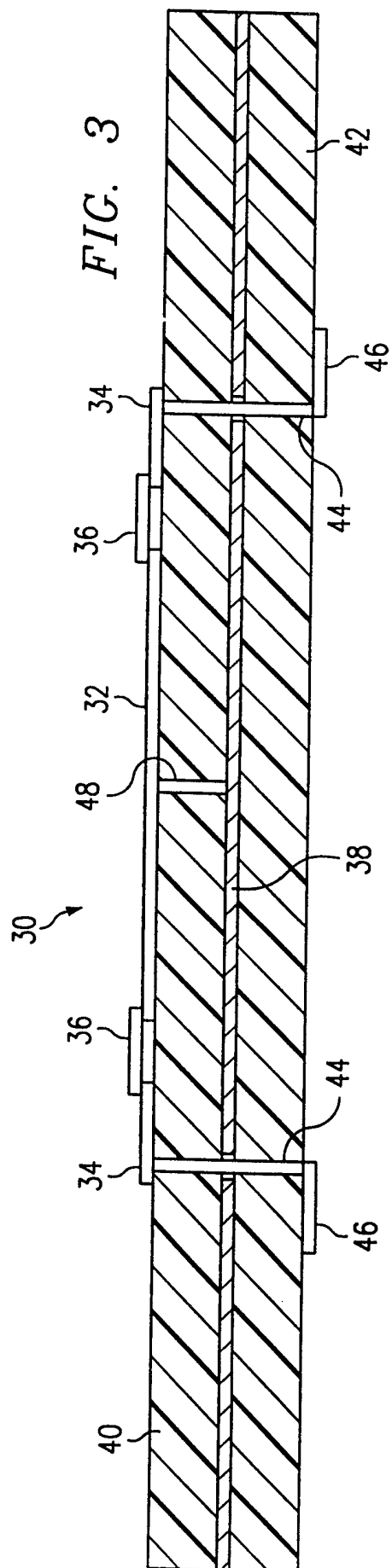


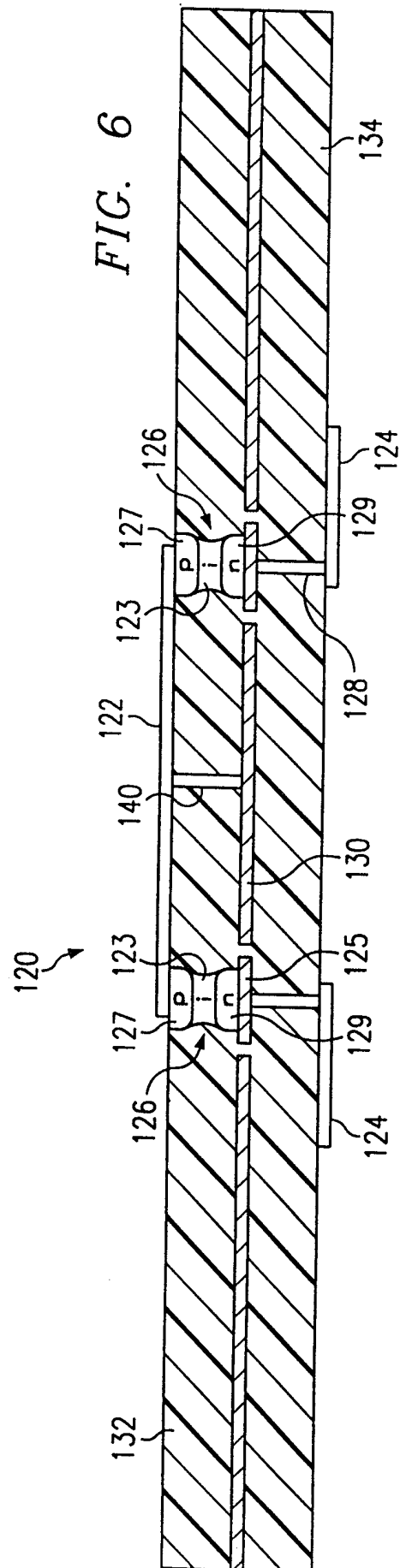
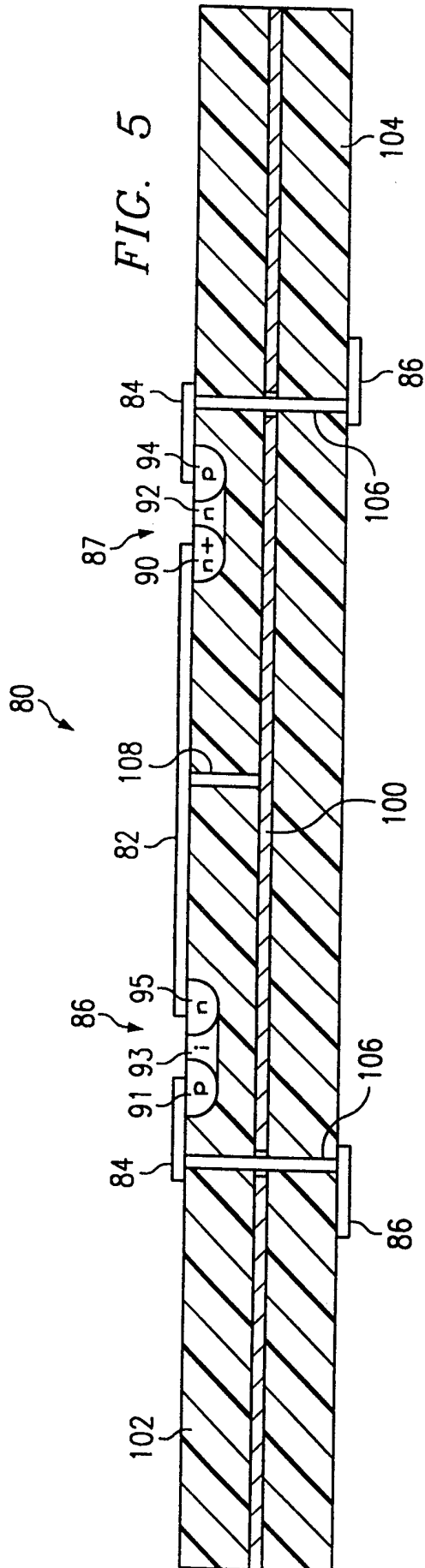
FIG. 1



A	PHASE STATE = 0°,	ROTATION ANGLE = 0°	E	PHASE STATE = 180°,	ROTATION ANGLE = -90°
B	PHASE STATE = 45°,	ROTATION ANGLE = -22.5°	F	PHASE STATE = 225°,	ROTATION ANGLE = -112.5°
C	PHASE STATE = 90°,	ROTATION ANGLE = -45°	G	PHASE STATE = 270°,	ROTATION ANGLE = -135°
D	PHASE STATE = 135°,	ROTATION ANGLE = -67.5°	H	PHASE STATE = 315°,	ROTATION ANGLE = -157.5°







INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 99/25036

A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H01Q3/26		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) IPC 7 H01Q		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4 053 895 A (MALAGISI CARMEN S) 11 October 1977 (1977-10-11) cited in the application the whole document ---	1-35
Y	EP 0 296 838 A (TEXAS INSTRUMENTS INC) 28 December 1988 (1988-12-28) page 6, line 27 -page 6, line 47; figure 5A ---	1-35
A	PATENT ABSTRACTS OF JAPAN vol. 014, no. 041 (E-0879), 25 January 1990 (1990-01-25) & JP 01 274505 A (MITSUBISHI ELECTRIC CORP), 2 November 1989 (1989-11-02) abstract --- <div style="text-align: right;">-/--</div>	1-35
<div style="display: flex; justify-content: space-between;"> <input checked="" type="checkbox"/> Further documents are listed in the continuation of box C. <input checked="" type="checkbox"/> Patent family members are listed in annex. </div>		
Special categories of cited documents :		
<div style="display: flex; justify-content: space-between;"> <div style="width: 45%;"> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> </div> <div style="width: 45%;"> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&" document member of the same patent family</p> </div> </div>		
Date of the actual completion of the international search <div style="text-align: center; font-weight: bold;">12 January 2000</div>		Date of mailing of the international search report <div style="text-align: center; font-weight: bold;">19/01/2000</div>
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer <div style="text-align: center; font-weight: bold;">Villafuerte Abrego</div>

INTERNATIONAL SEARCH REPORT

Inter nal Application No

PCT/US 99/25036

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 682 382 A (DISYS CORP) 15 November 1995 (1995-11-15) the whole document ---	1-35
A	US 5 309 163 A (NGAN YIU C ET AL) 3 May 1994 (1994-05-03) the whole document -----	1-35

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