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(54) **FINFET SEMICONDUCTOR DEVICE WITH ISOLATED CHANNEL REGIONS**

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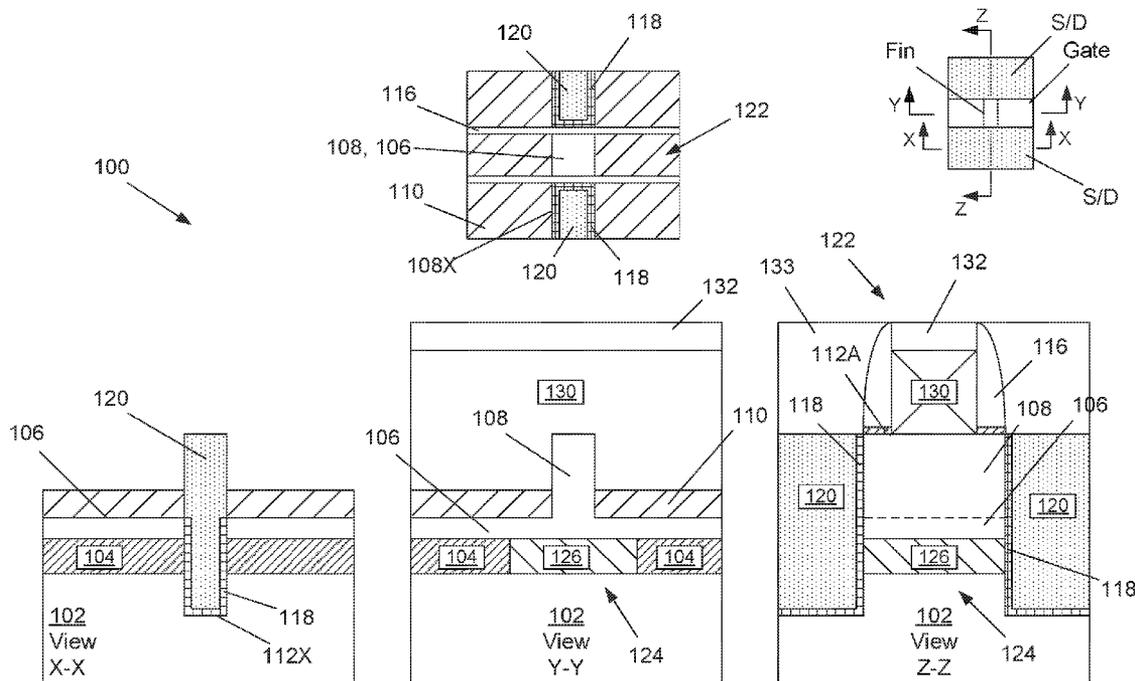
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(57) **ABSTRACT**

A FinFET device includes a fin structure positioned in the channel region of the device and a gate structure positioned above the fin structure, wherein the fin structure includes a portion of a semiconductor substrate and an epi semiconductor material positioned vertically above the portion of the semiconductor substrate. Sidewall spacers are positioned adjacent the gate structure and a fin cavity is positioned in source/drain regions of the device, wherein the fin structure has edges in a gate width direction that are substantially self-aligned with the sidewall spacers and the semiconductor substrate defines the bottom of the fin cavity. A silicon etch stop layer is positioned on and in contact with the edges of the fin structure and within the fin cavity, and a stressed semiconductor material is positioned on and in contact with the silicon etch stop layer and at least partially within the fin cavity.



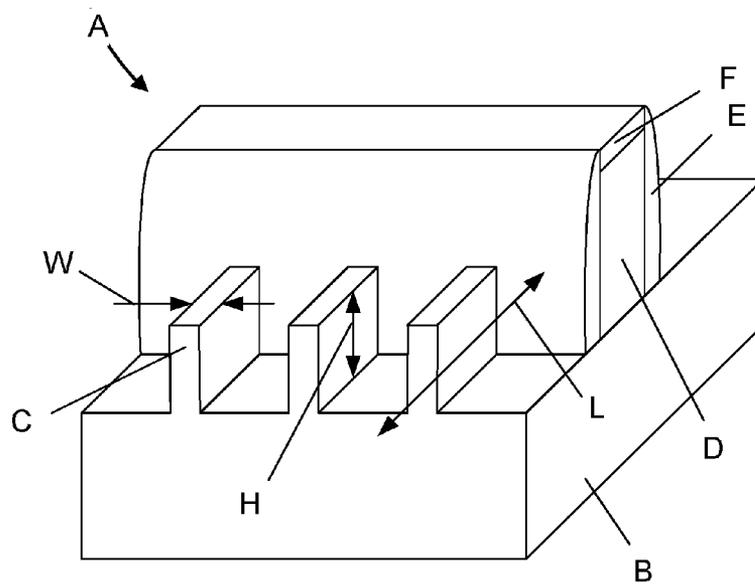
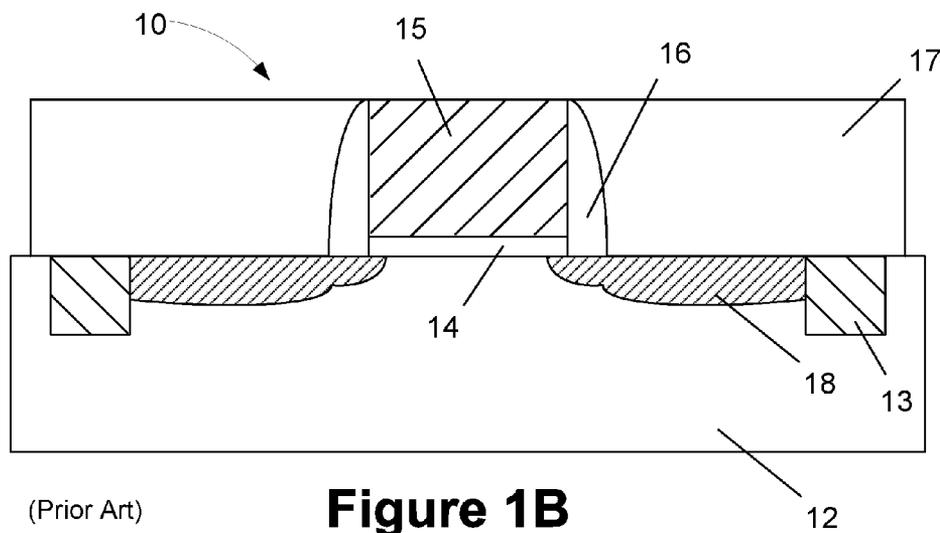


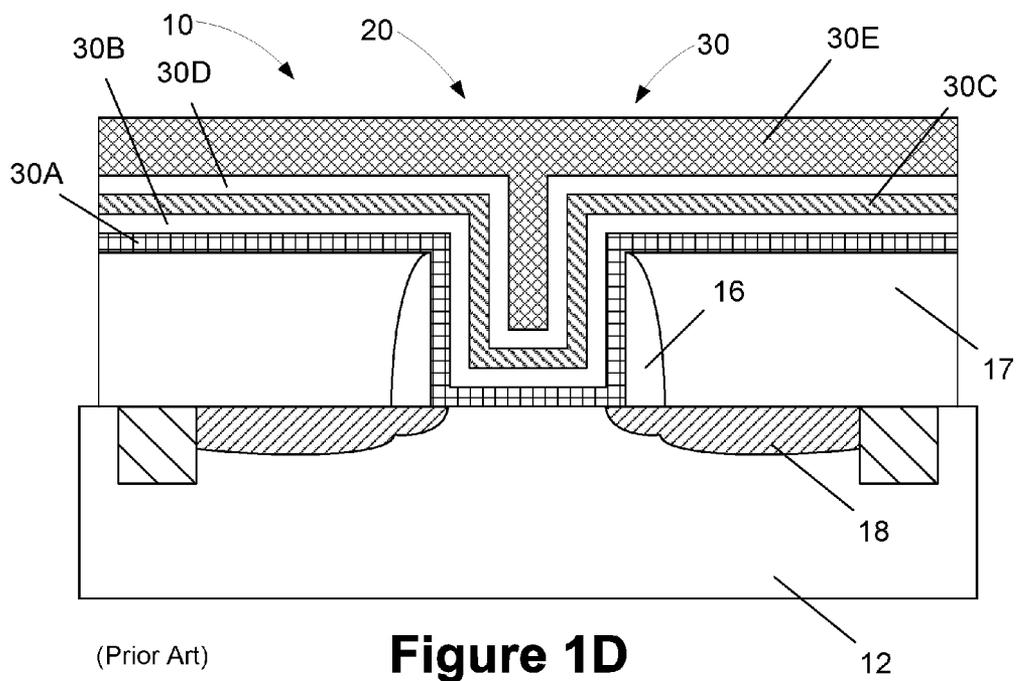
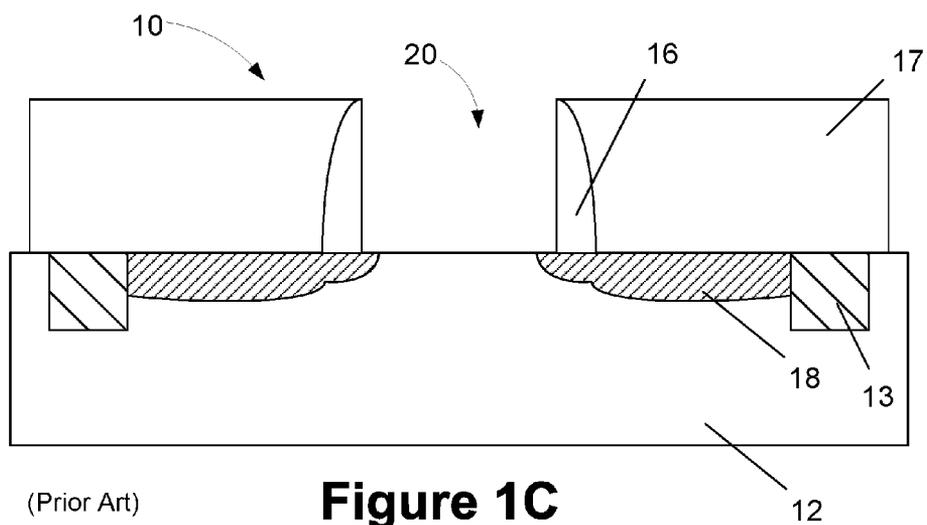
Figure 1A (Prior Art)



(Prior Art)

Figure 1B

12



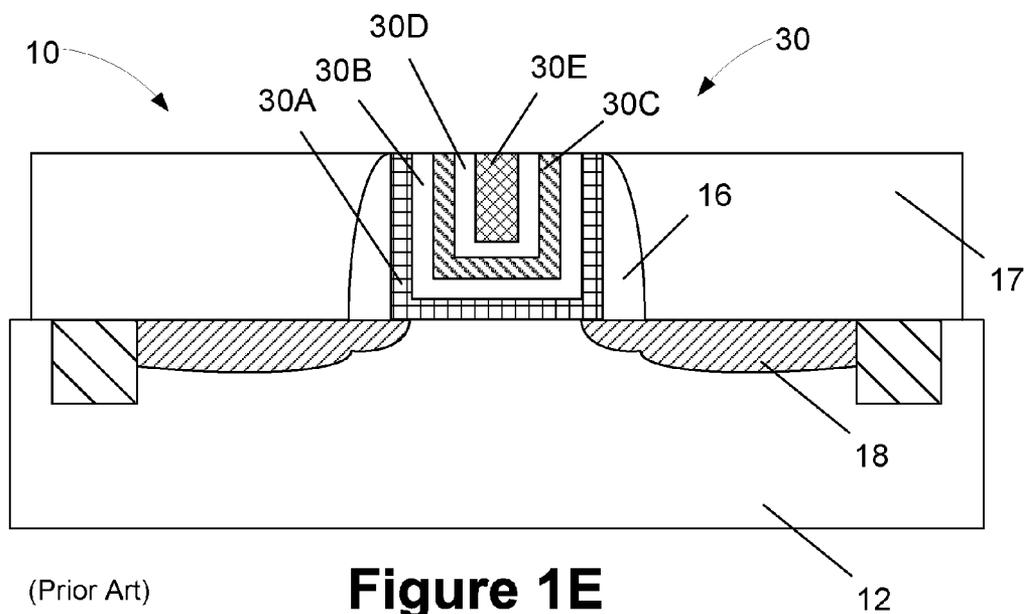


Figure 1E

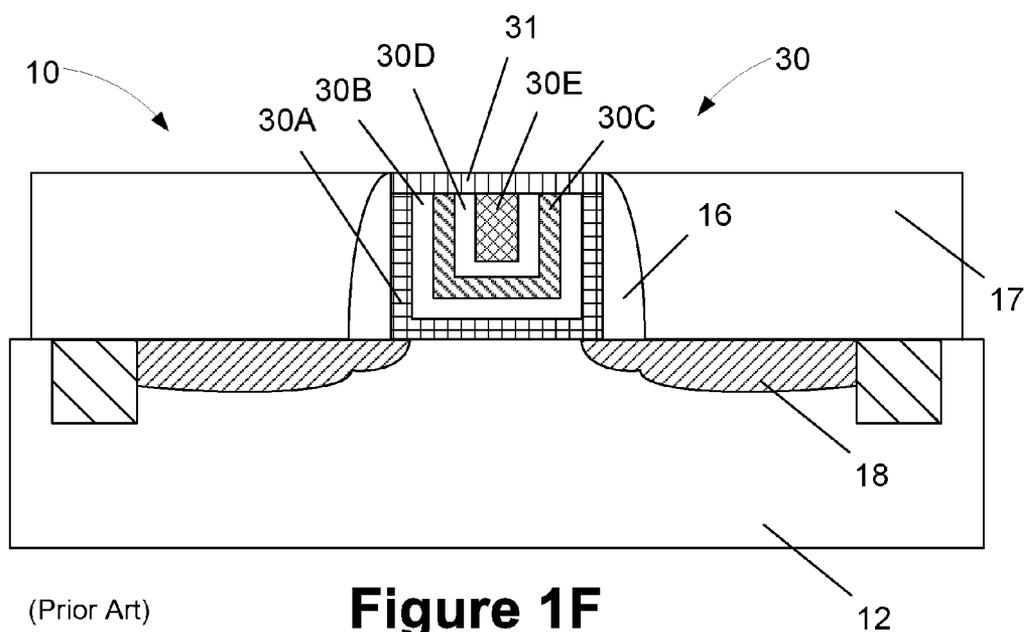


Figure 1F

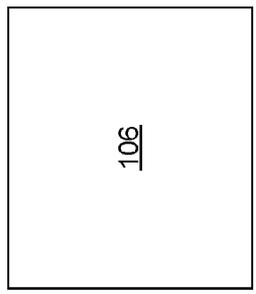
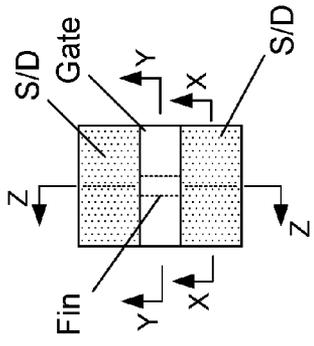
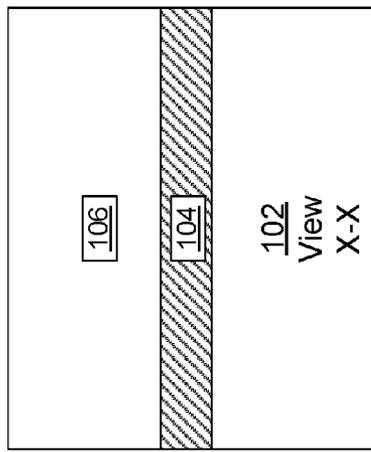
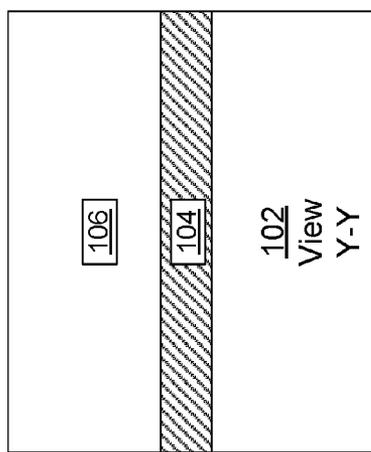
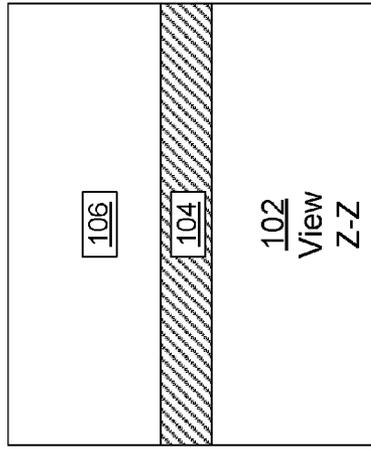
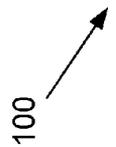


Figure 2A



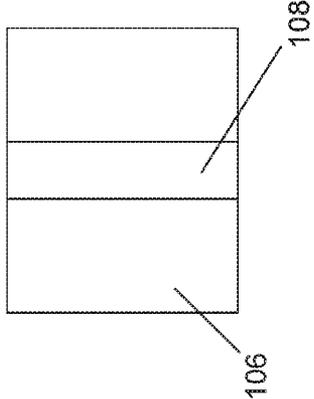
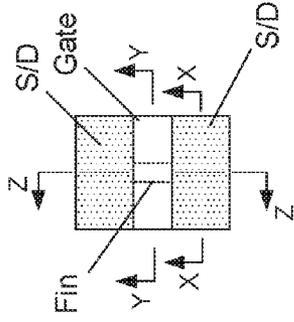
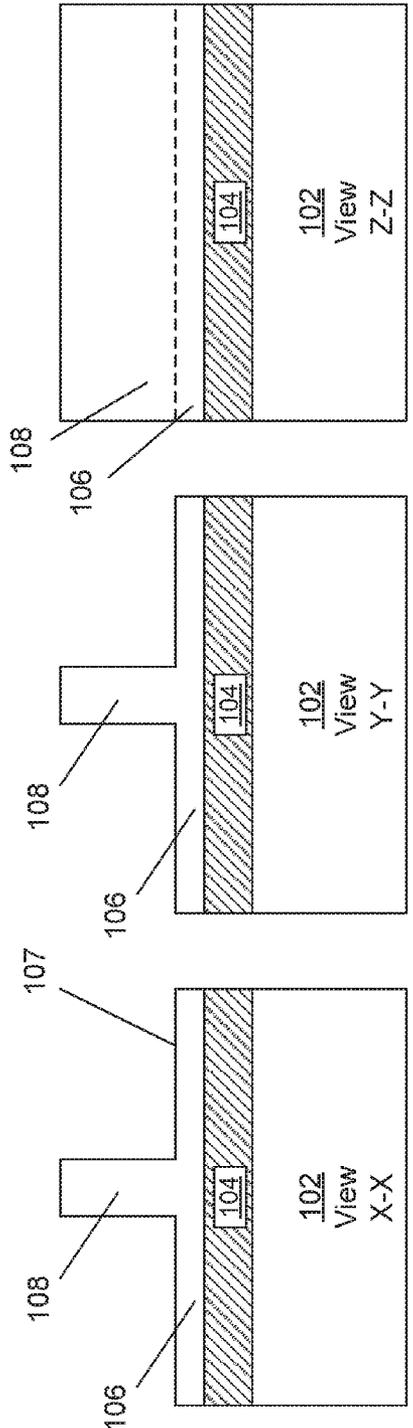
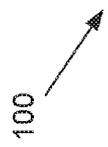


Figure 2B



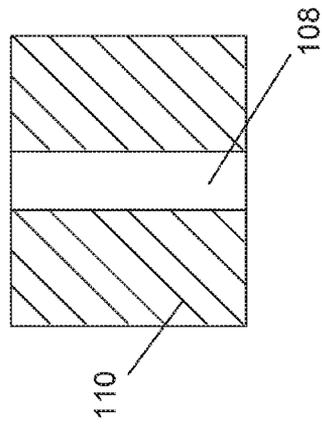
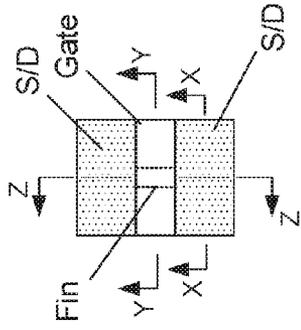
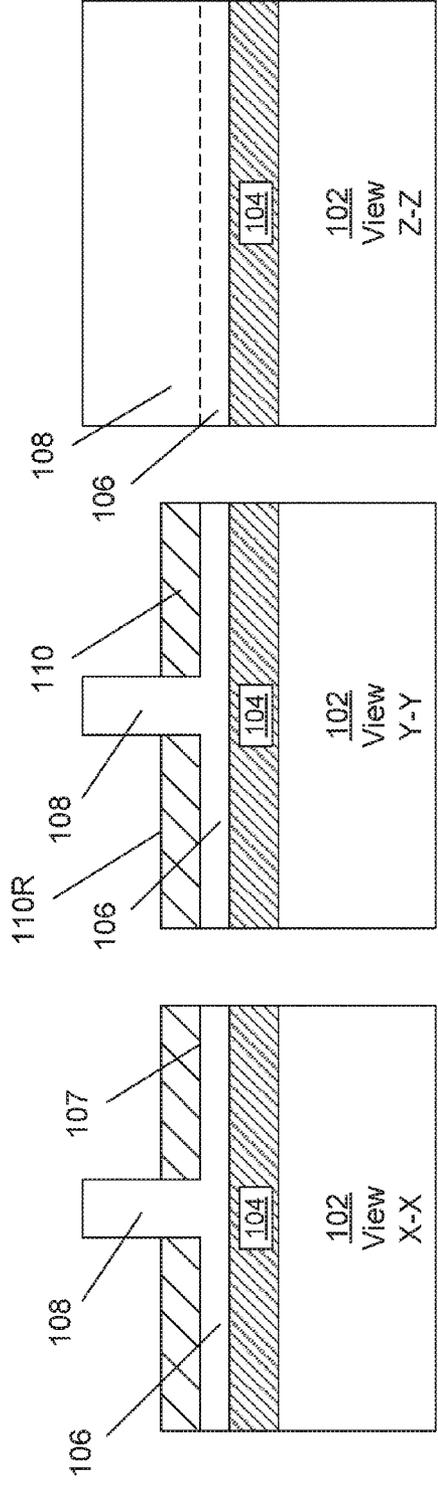
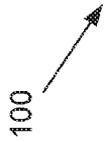
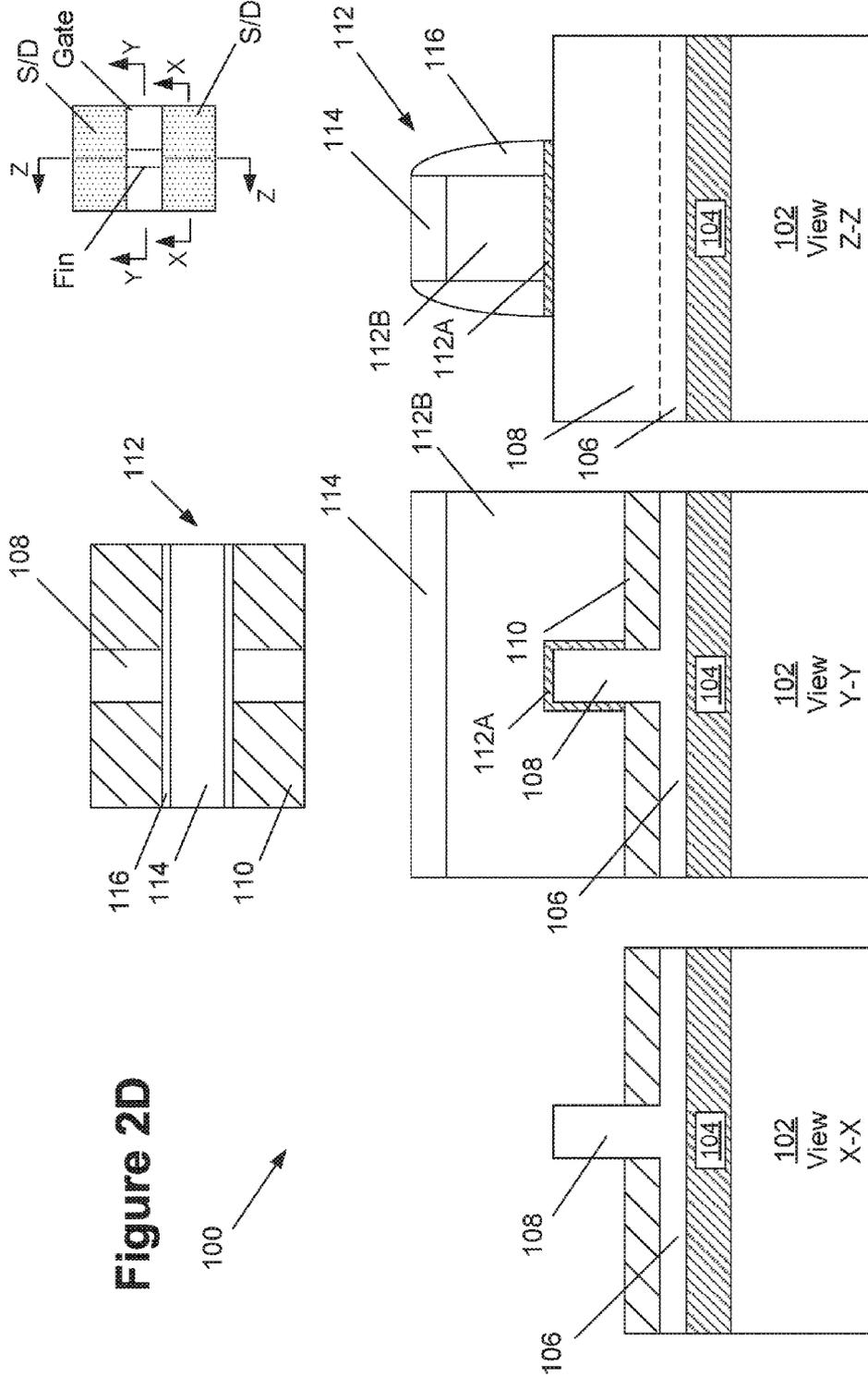
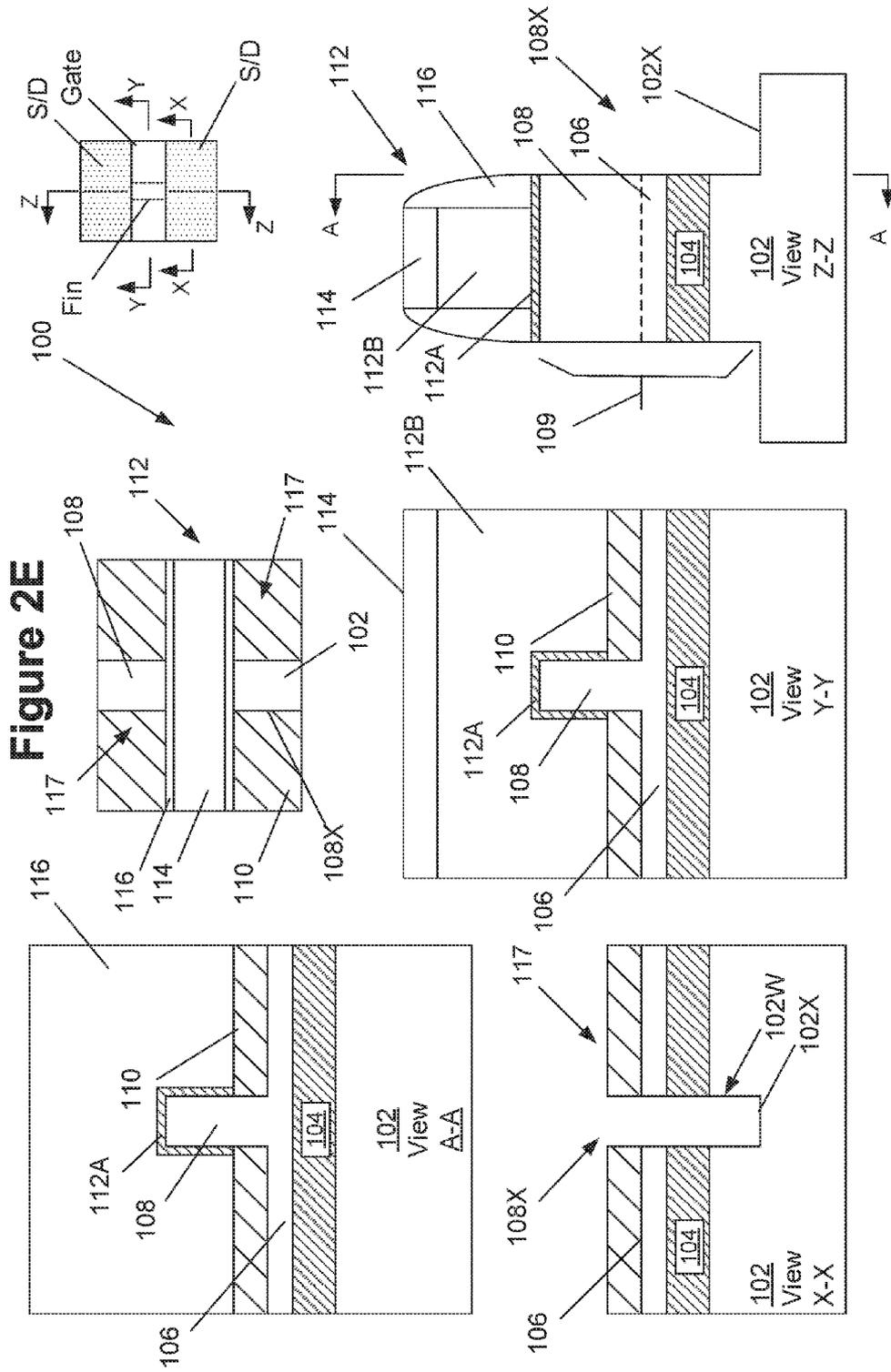
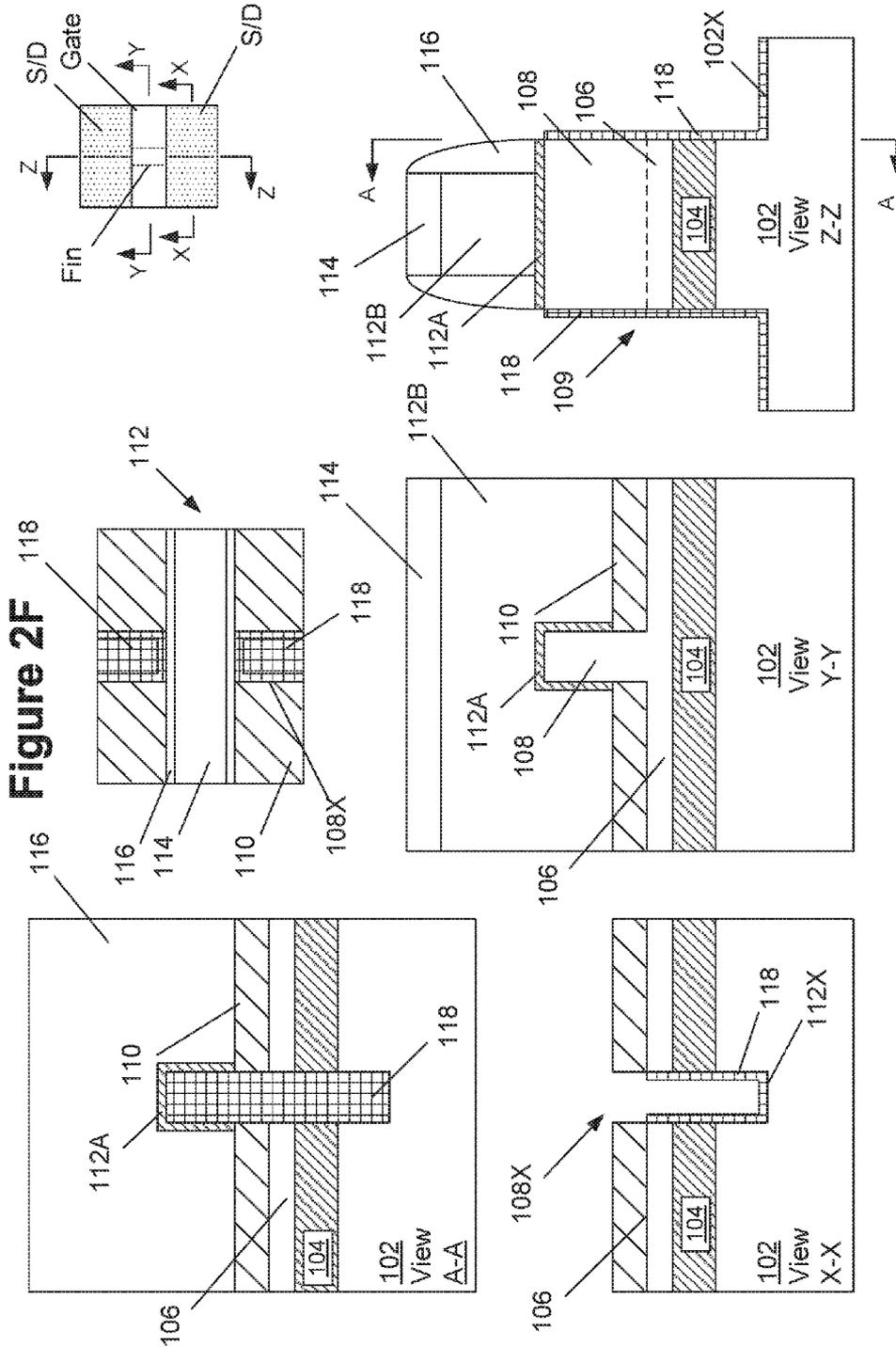


Figure 2C









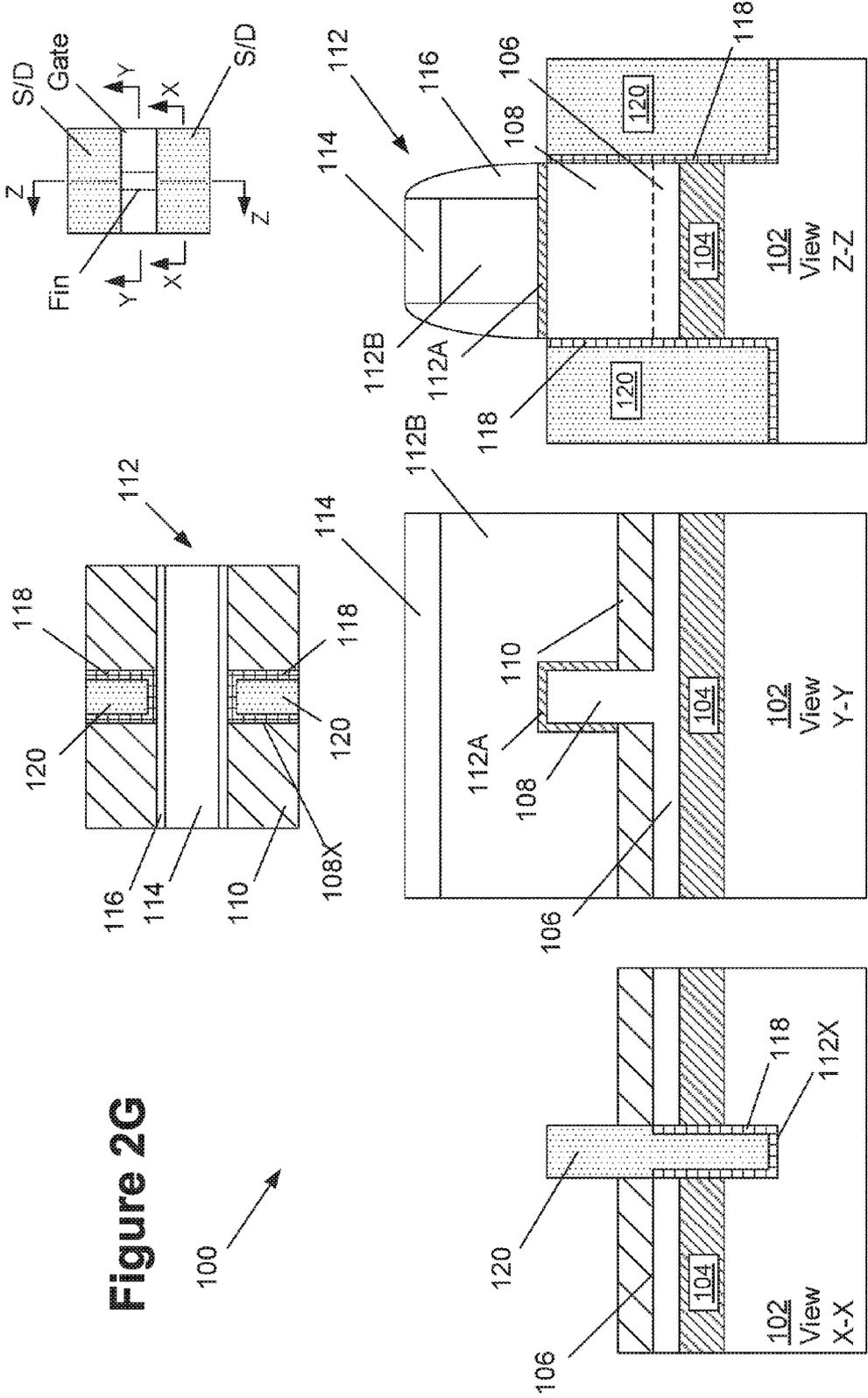
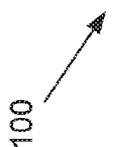
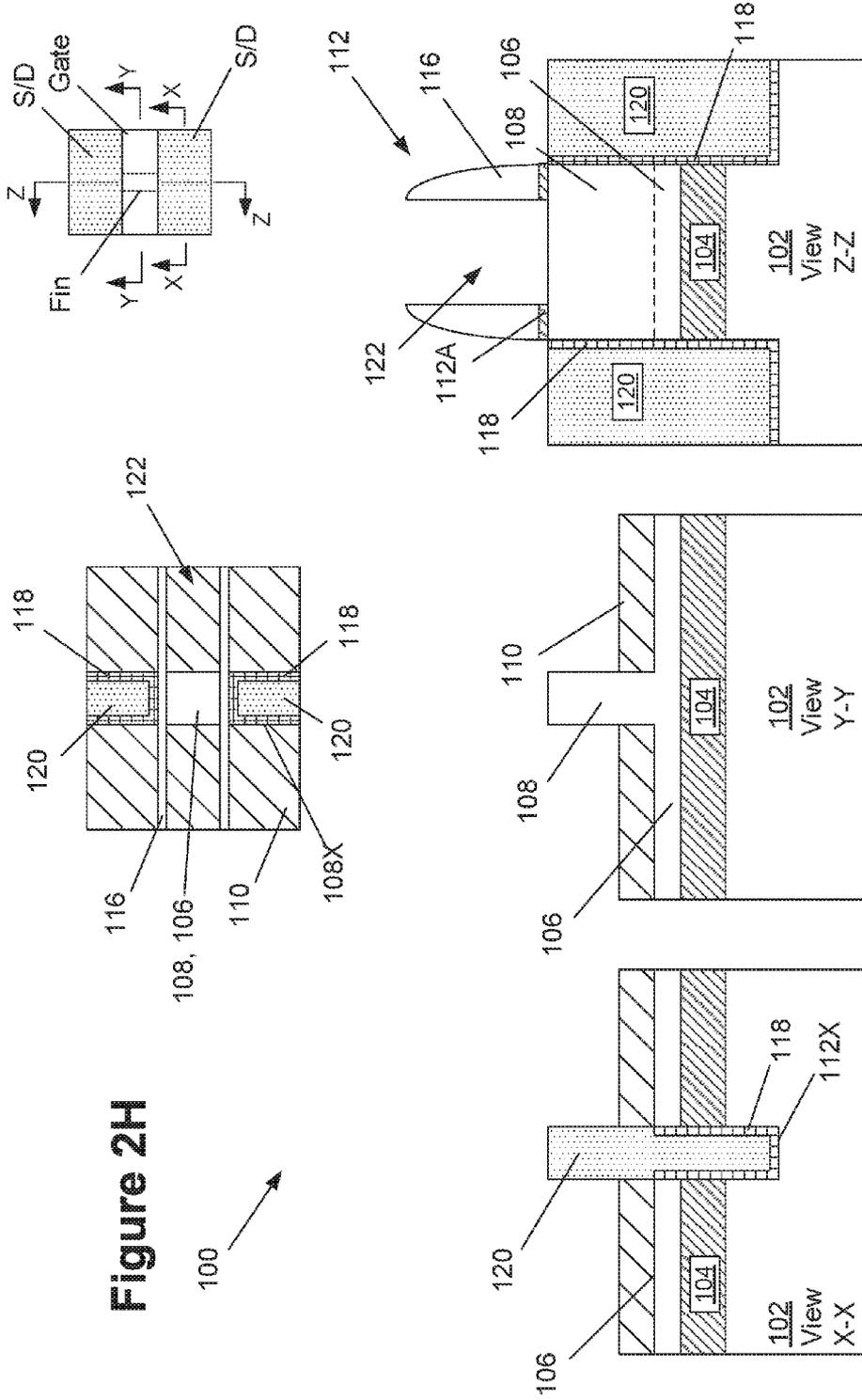


Figure 2G





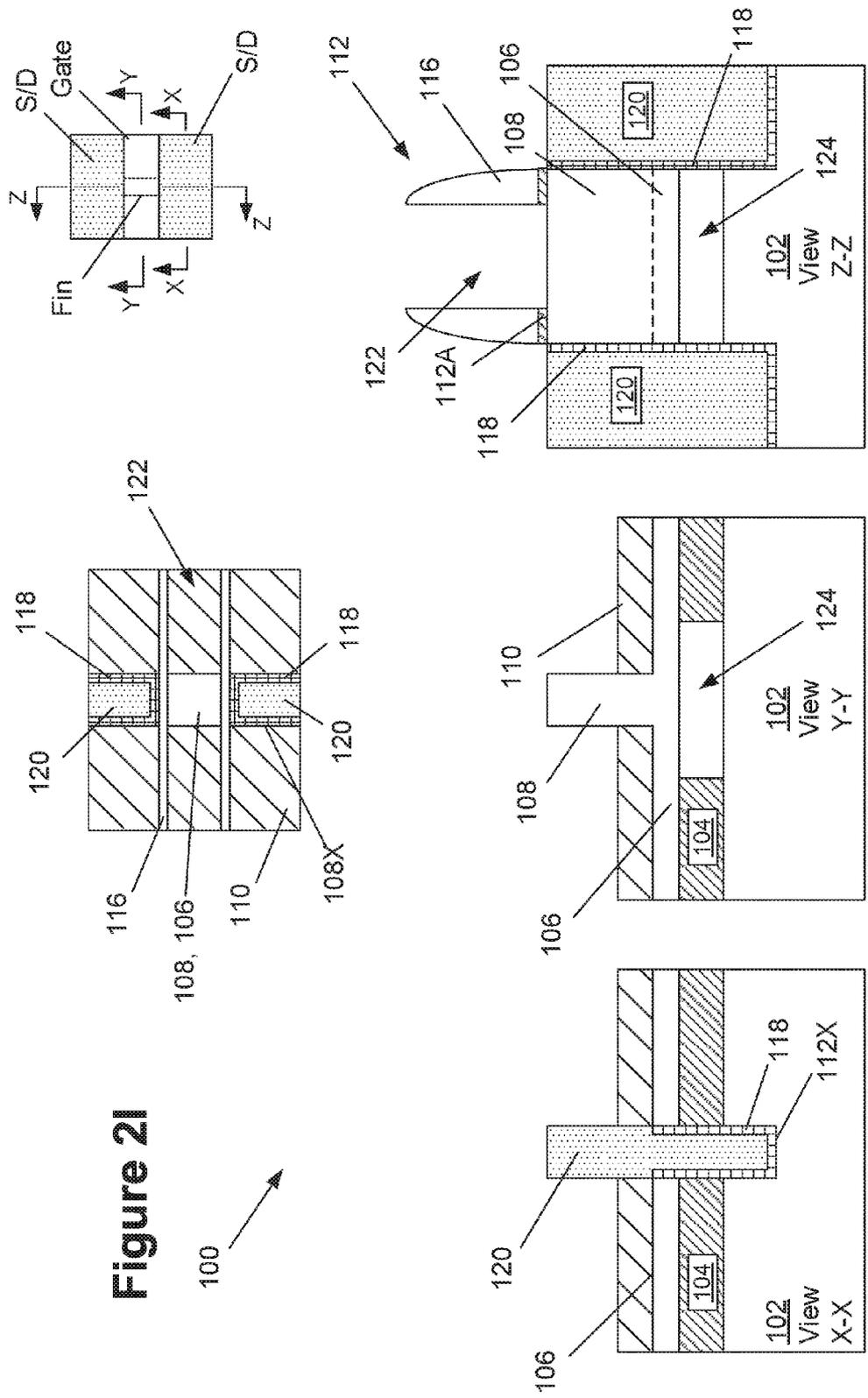
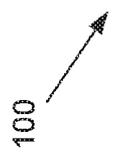
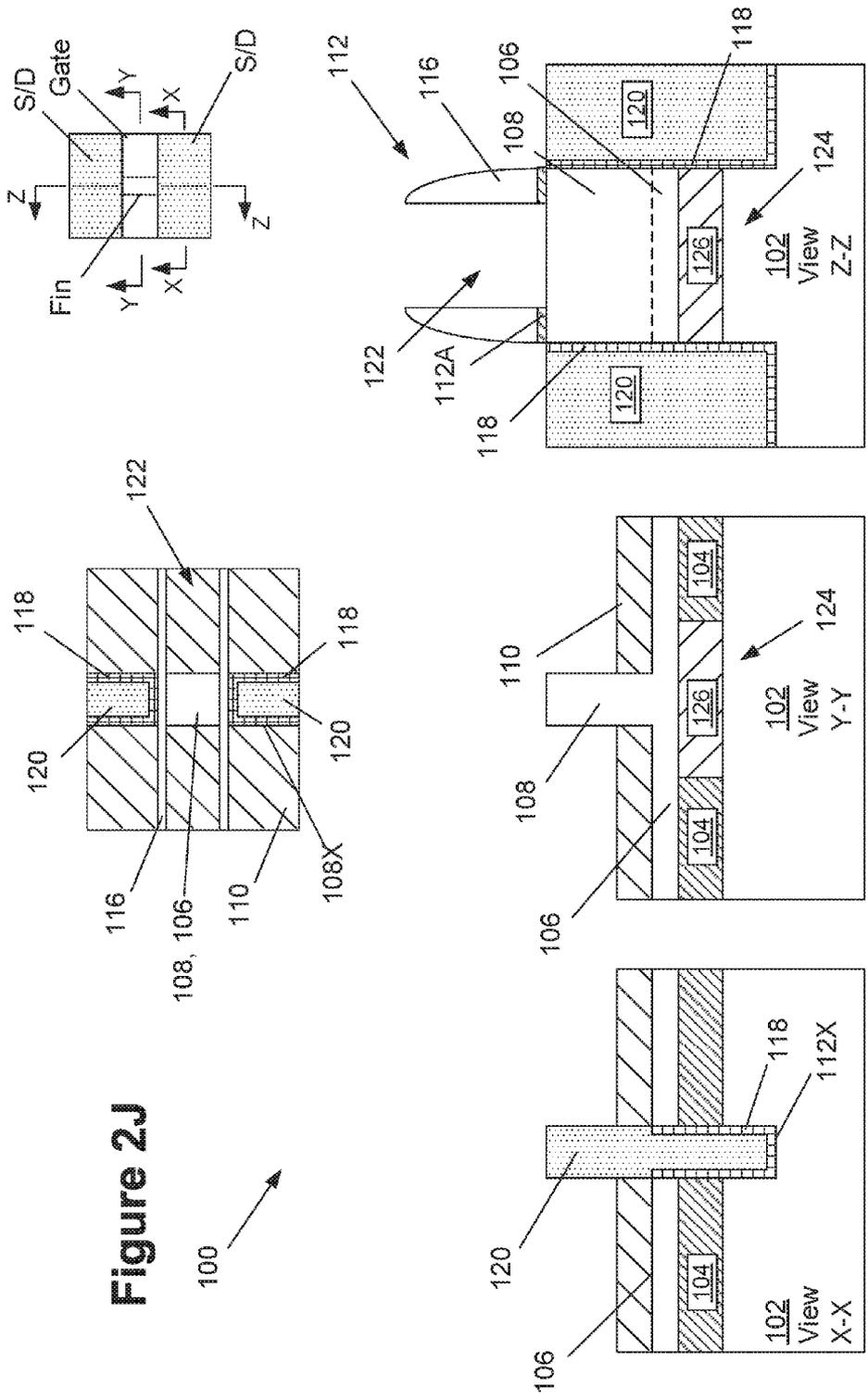


Figure 2I





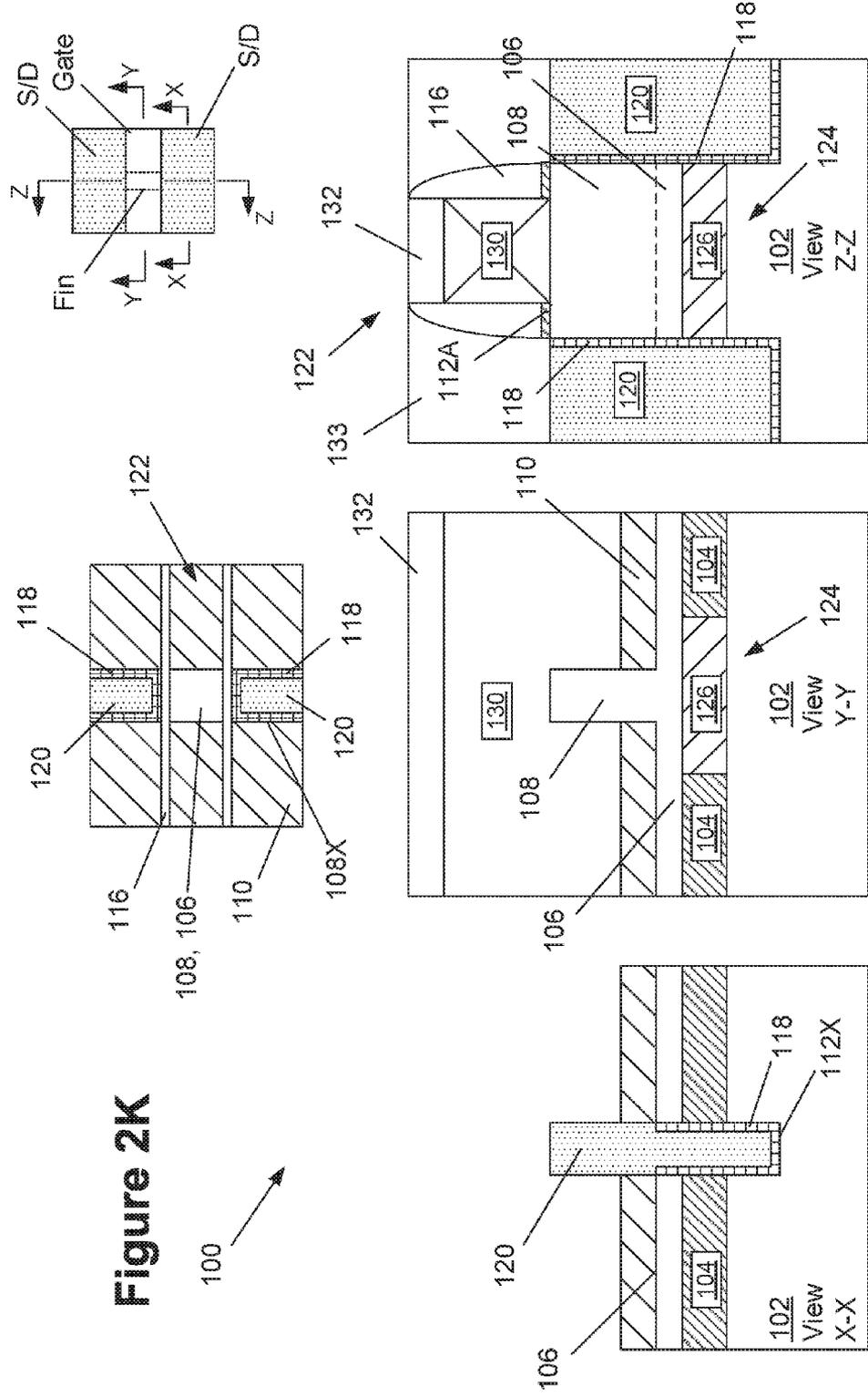
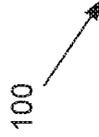


Figure 2K



FINFET SEMICONDUCTOR DEVICE WITH ISOLATED CHANNEL REGIONS

BACKGROUND

[0001] 1. Field of the Disclosure

[0002] Generally, the present disclosure relates to the fabrication of integrated circuits, and, more particularly, to various methods of forming an isolated channel region for a FinFET semiconductor device and the resulting semiconductor device.

[0003] 2. Description of the Related Art

[0004] In modern integrated circuits, such as microprocessors, storage devices and the like, a very large number of circuit elements, especially transistors, are provided and operated on a restricted chip area. In integrated circuits fabricated using metal-oxide-semiconductor (MOS) technology, field effect transistors (FETs) (both NMOS and PMOS transistors) are provided that are typically operated in a switching mode. That is, these transistor devices exhibit a highly conductive state (on-state) and a high impedance state (off-state). FETs may take a variety of forms and configurations. For example, among other configurations, FETs may be either so-called planar FET devices or three-dimensional (3D) devices, such as FinFET devices.

[0005] A field effect transistor (FET), irrespective of whether an NMOS transistor or a

[0006] PMOS transistor is considered, and irrespective of whether it is a planar or 3D FinFET device, typically comprises doped source/drain regions that are formed in a semiconductor substrate that are separated by a channel region. A gate insulation layer is positioned above the channel region and a conductive gate electrode is positioned above the gate insulation layer. The gate insulation layer and the gate electrode may sometimes be referred to as the gate structure for the device. By applying an appropriate voltage to the gate electrode, the channel region becomes conductive and current is allowed to flow from the source region to the drain region. In a planar FET device, the gate structure is formed above a substantially planar upper surface of the substrate. In some cases, one or more epitaxial growth processes are performed to form epi semiconductor material in recesses formed in the source/drain regions of the planar FET device. In some cases, the epi material may be formed in the source/drain regions without forming any recesses in the substrate for a planar FET device. The gate structures for such planar FET devices may be manufactured using so-called “gate-first” or “replacement gate” (gate-last) manufacturing techniques.

[0007] To improve the operating speed of FETs, and to increase the density of FETs on an integrated circuit device, device designers have greatly reduced the physical size of FETs over the years. More specifically, the channel length of FETs has been significantly decreased, which has resulted in improving the switching speed of FETs. However, decreasing the channel length of a FET also decreases the distance between the source region and the drain region. In some cases, this decrease in the separation between the source and the drain makes it difficult to efficiently inhibit the electrical potential of the source region and the channel from being adversely affected by the electrical potential of the drain. This is sometimes referred to as a so-called short channel effect, wherein the characteristic of the FET as an active switch is degraded.

[0008] In contrast to a FET, which has a planar structure, a so-called FinFET device has a three-dimensional (3D) struc-

ture. FIG. 1A is a perspective view of an illustrative prior art FinFET semiconductor device “A” that is formed above a semiconductor substrate B that will be referenced so as to explain, at a very high level, some basic features of a FinFET device. In this example, the FinFET device A includes three illustrative fins C, a gate structure D, sidewall spacers E and a gate cap F. The gate structure D is typically comprised of a layer of insulating material (not separately shown), e.g., a layer of high-k insulating material or silicon dioxide, and one or more conductive material layers (e.g., metal and/or polysilicon) that serve as the gate electrode for the device A. The fins C have a three-dimensional configuration: a height H, a width W and an axial length L. The axial length L corresponds to the direction of current travel in the device A when it is operational. The portions of the fins C covered by the gate structure D is the channel region of the FinFET device A. In a conventional process flow, the portions of the fins C that are positioned outside of the spacers E, i.e., in the source/drain regions of the device A, may be increased in size or even merged together (a situation not shown in FIG. 1A) by performing one or more epitaxial growth processes. The process of increasing the size of or merging the fins C in the source/drain regions of the device A is performed to reduce the resistance of source/drain regions and/or make it easier to establish electrical contact to the source/drain regions. Even if an epi “merger” process is not performed, an epi growth process will typically be performed on the fins C to increase their physical size. In the FinFET device A, the gate structure D may enclose both sides and the upper surface of all or a portion of the fins C to form a tri-gate structure so as to use a channel having a three-dimensional structure instead of a planar structure. In some cases, an insulating cap layer (not shown), e.g., silicon nitride, is positioned at the top of the fins C and the FinFET device only has a dual-gate structure (sidewalls only). The gate structures D for such FinFET devices may be manufactured using so-called “gate-first” or “replacement gate” (gate-last) manufacturing techniques.

[0009] Unlike a planar FET, in a FinFET device, a channel is formed perpendicular to a surface of the semiconducting substrate so as to reduce the physical size of the semiconductor device. Also, in a FinFET, the junction capacitance at the drain region of the device is greatly reduced, which tends to significantly reduce short channel effects. When an appropriate voltage is applied to the gate electrode of a FinFET device, the surfaces (and the inner portion near the surface) of the fins C, i.e., the vertically oriented sidewalls and the top upper surface of the fin, form a surface inversion layer or a volume inversion layer that contributes to current conduction. In a FinFET device, the “channel-width” is estimated to be about two times (2x) the vertical fin-height plus the width of the top surface of the fin, i.e., the fin width (for a tri-gate device). Multiple fins can be formed in the same foot-print as that of a planar transistor device. Accordingly, for a given plot space (or foot-print), FinFETs tend to be able to generate significantly higher drive current density than planar transistor devices. Additionally, the leakage current of FinFET devices after the device is turned “OFF” is significantly reduced as compared to the leakage current of planar FETs, due to the superior gate electrostatic control of the “fin” channel on FinFET devices. In short, the 3D structure of a FinFET device is a superior MOSFET structure as compared to that of a planar FET, especially in the 20 nm CMOS technology node and beyond.

[0010] For many early device technology generations, the gate structures of most transistor elements (planar or FinFET devices) were comprised of a plurality of silicon-based materials, such as a silicon dioxide and/or silicon oxynitride gate insulation layer, in combination with a polysilicon gate electrode. However, as the channel length of aggressively scaled transistor elements has become increasingly smaller, many newer generation devices employ gate structures that contain alternative materials in an effort to avoid the short channel effects which may be associated with the use of traditional silicon-based materials in reduced channel length transistors. For example, in some aggressively scaled transistor elements, which may have channel lengths on the order of approximately 10-32 nm or less, gate structures that include a so-called high-k dielectric gate insulation layer and one or more metal layers that function as the gate electrode (HK/MG) have been implemented. Such alternative gate structures have been shown to provide significantly enhanced operational characteristics over the heretofore more traditional silicon dioxide/polysilicon gate structure configurations.

[0011] Depending on the specific overall device requirements, several different high-k materials—i.e., materials having a dielectric constant, or k-value, of approximately 10 or greater—have been used with varying degrees of success for the gate insulation layer in an HK/MG gate electrode structure. For example, in some transistor element designs, a high-k gate insulation layer may include tantalum oxide (Ta_2O_5), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), titanium oxide (TiO_2), aluminum oxide (Al_2O_3), hafnium silicates (HfSiO_x) and the like. Furthermore, one or more non-polysilicon metal gate electrode materials—i.e., a metal gate stack—may be used in HK/MG configurations so as to control the work function of the transistor. These metal gate electrode materials may include, for example, one or more layers of titanium (Ti), titanium nitride (TiN), titanium-aluminum (TiAl), titanium-aluminum-carbon (TiAlC), aluminum (Al), aluminum nitride (AlN), tantalum (Ta), tantalum nitride (TaN), tantalum carbide (TaC), tantalum carbonitride (TaCN), tantalum silicon nitride (TaSiN), tantalum silicide (TaSi) and the like.

[0012] One well-known processing method that has been used for forming a transistor with a high-k/metal gate structure is the so-called “gate-last” or “replacement gate” technique. The replacement gate process may be used when forming planar devices or 3D devices. FIGS. 1B-1F simplistically depict one illustrative prior art method for forming an HK/MG replacement gate structure using a replacement gate technique on a planar transistor device. As shown in FIG. 1B, the process includes the formation of a basic transistor structure above a semiconductor substrate **12** in an active area defined by a shallow trench isolation structure **13**. At the point of fabrication depicted in FIG. 1B, the device **10** includes a sacrificial gate insulation layer **14**, a dummy or sacrificial gate electrode **15**, sidewall spacers **16**, a layer of insulating material **17** and source/drain regions **18** formed in the substrate **12**. The various components and structures of the device **10** may be formed using a variety of different materials and by performing a variety of known techniques. For example, the sacrificial gate insulation layer **14** may be comprised of silicon dioxide, the sacrificial gate electrode **15** may be comprised of polysilicon, the sidewall spacers **16** may be comprised of silicon nitride and the layer of insulating material **17** may be comprised of silicon dioxide. The source/drain regions **18** may be comprised of implanted dopant materials

(N-type dopants for NMOS devices and P-type dopants for PMOS devices) that are implanted into the substrate **12** using known masking and ion implantation techniques. Of course, those skilled in the art will recognize that there are other features of the transistor **10** that are not depicted in the drawings for purposes of clarity. For example, so-called halo implant regions are not depicted in the drawings, as well as various layers or regions of silicon/germanium that are typically found in high performance PMOS transistors. At the point of fabrication depicted in FIG. 1B, the various structures of the device **10** have been formed and a chemical mechanical polishing (CMP) process has been performed to remove any materials above the sacrificial gate electrode **15** (such as a protective cap layer (not shown) comprised of silicon nitride) so that at least the sacrificial gate electrode **15** may be removed.

[0013] As shown in FIG. 1C, one or more etching processes are performed to remove the sacrificial gate electrode **15** and the sacrificial gate insulation layer **14** to thereby define a gate cavity **20** where a replacement gate structure will subsequently be formed. Typically, the sacrificial gate insulation layer **14** is removed as part of the replacement gate technique, as depicted herein. However, the sacrificial gate insulation layer **14** may not be removed in all applications. Even in cases where the sacrificial gate insulation layer **14** is intentionally removed, there will typically be a very thin native oxide layer (not shown) that forms on the substrate **12** within the gate cavity **20**.

[0014] Next, as shown in FIG. 1D, various layers of material that will constitute a replacement gate structure **30** are formed in the gate cavity **20**. The materials used for the replacement gate structures **30** for NMOS and PMOS devices are typically different. For example, the replacement gate structure **30** for an NMOS device may be comprised of a high-k gate insulation layer **30A**, such as hafnium oxide, having a thickness of approximately 2 nm, a first metal layer **30B** (e.g., a layer of titanium nitride with a thickness of about 1-2 nm), a second metal layer **30C**—a so-called work function adjusting metal layer for the NMOS device—(e.g., a layer of titanium-aluminum or titanium-aluminum-carbon with a thickness of about 5 nm), a third metal layer **30D** (e.g., a layer of titanium nitride with a thickness of about 1-2 nm) and a bulk metal layer **30E**, such as aluminum or tungsten.

[0015] Ultimately, as shown in FIG. 1E, one or more CMP processes are performed to remove excess portions of the gate insulation layer **30A**, the first metal layer **30B**, the second metal layer **30C**, the third metal layer **30D** and the bulk metal layer **30E** positioned outside of the gate cavity **20** to thereby define the replacement gate structure **30** for an illustrative NMOS device. Typically, the replacement metal gate structure **30** for a PMOS device does not include as many metal layers as does an NMOS device. For example, the gate structure **30** for a PMOS device may only include the high-k gate insulation layer **30A**, a single layer of titanium nitride—the work function adjusting metal for the PMOS device—having a thickness of about 3-4 nm, and the bulk metal layer **30E**.

[0016] FIG. 1F depicts the device **10** after several process operations were performed. First, one or more recess etching processes were performed to remove upper portions of the various materials within the cavity **20** so as to form a recess within the gate cavity **20**. Then, a gate cap layer **31** was formed in the recess above the recessed gate materials. The gate cap layer **31** is typically comprised of silicon nitride and it may be formed by depositing a layer of gate cap material so

as to over-fill the recess formed in the gate cavity and thereafter performing a CMP process to remove excess portions of the gate cap material layer positioned above the surface of the layer of insulating material 17. The gate cap layer 31 is formed so as to protect the underlying gate materials during subsequent processing operations.

[0017] Device manufacturers are under constant pressure to produce integrated circuit products with increased performance and lower production costs relative to previous device generations. Thus, device designers spend a great amount of time and effort to maximize device performance while seeking ways to reduce manufacturing costs and improve manufacturing reliability. As it relates to 3D devices, device designers have spent many years and employed a variety of techniques in an effort to improve the performance capability and reliability of such devices. Device designers are currently investigating using alternative semiconductor materials, such as so-called III-V materials, to manufacture FinFET devices which are intended to enhance the performance capabilities of such devices, e.g., to enable low-voltage operation. Device designers are also contemplating ways to form isolation regions under the channel region of a 3D device to improve device performance. What is desired is a reliable and repeatable methodology for forming an isolation region under the channel region of a FinFET device.

[0018] The present disclosure is directed to various methods of forming an isolated channel region for a FinFET semiconductor device and the resulting semiconductor device that may avoid, or at least reduce, the effects of one or more of the problems identified above.

SUMMARY OF THE DISCLOSURE

[0019] The following presents a simplified summary of the disclosure in order to provide a basic understanding of some aspects of the subject matter that is described in further detail below. This summary is not an exhaustive overview of the disclosure, nor is it intended to identify key or critical elements of the subject matter disclosed here. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is discussed later.

[0020] Generally, the present disclosure is directed to various methods of forming an isolated channel region for a FinFET semiconductor device and the resulting semiconductor device. One exemplary embodiment of a FinFET device disclosed herein includes a fin structure positioned in a channel region of the FinFET device, wherein the fin structure includes a portion of a semiconductor substrate and an epi semiconductor material positioned vertically above the portion of the semiconductor substrate. The exemplary FinFET device also includes, among other things, a gate structure positioned above the fin structure in the channel region of the FinFET device and sidewall spacers positioned adjacent the gate structure, wherein the fin structure has edges in a gate width direction of the FinFET device that are substantially self-aligned with the sidewall spacers. Furthermore, a fin cavity is positioned in source/drain regions of the FinFET device, wherein the semiconductor substrate defines the bottom of the fin cavity. Additionally, the disclosed FinFET device includes a silicon etch stop layer positioned on and in contact with the edges of the fin structure and within the fin cavity, and a stressed semiconductor material positioned on and in contact with the silicon etch stop layer and at least partially within the fin cavity.

[0021] Another illustrative FinFET device of the present disclosure includes, among other things, a fin structure positioned in a channel region of the FinFET device, wherein the fin structure includes a portion of a semiconductor substrate and an epi semiconductor material positioned vertically above the portion of the semiconductor substrate. The disclosed FinFET device also includes a gate structure positioned above the fin structure in the channel region of the FinFET device, wherein the gate structure includes a gate insulation layer and a gate electrode, the gate insulation layer including a high-k insulating material and the gate electrode including at least one layer of metal. Additionally, sidewall spacers are positioned adjacent the gate structure, wherein the fin structure has edges in a gate width direction of the FinFET device that are substantially self-aligned with the sidewall spacers, and a fin cavity is positioned in source/drain regions of the FinFET device, wherein the semiconductor substrate defines a bottom of the fin cavity. Moreover, the illustrative FinFET device further includes a silicon etch stop layer positioned on and in contact with the edges of the fin structure, on the bottom of the fin cavity, and on sidewalls of the fin cavity, and a stressed semiconductor material is positioned on and in contact with the silicon etch stop layer and at least partially within the fin cavity.

[0022] In yet a further exemplary embodiment, a FinFET device is disclosed herein that includes a fin structure positioned in a channel region of the FinFET device, wherein the fin structure includes a portion of a semiconductor substrate and an epi semiconductor material positioned vertically above the portion of the semiconductor substrate. Additionally, the exemplary FinFET device includes a gate structure positioned above the fin structure in the channel region of the FinFET device, and sidewall spacers positioned adjacent the gate structure, wherein the fin structure has edges in a gate width direction of the FinFET device that are substantially self-aligned with the sidewall spacers. Also included in the disclosed FinFET device is a fin cavity that is positioned in source/drain regions of the FinFET device, wherein the semiconductor substrate defines a bottom of the fin cavity. Furthermore, a silicon etch stop layer is positioned on and in contact with the edges of the fin structure, on the bottom of the fin cavity, and on sidewalls of the fin cavity, wherein the silicon etch stop layer covers the semiconductor substrate portion of the fin structure and the epi semiconductor material of the fin structure along at least the edges of the fin structure. Moreover, a stressed semiconductor material is positioned on and in contact with the silicon etch stop layer and at least partially within the fin cavity, wherein the stressed semiconductor material comprises silicon-germanium ($\text{Si}_x\text{Ge}_{1-x}$).

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The disclosure may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

[0024] FIG. 1A is a perspective view of one illustrative embodiment of a prior art FinFET device;

[0025] FIGS. 1B-1F depict one illustrative prior art method of forming a gate structure of transistors using a so-called "replacement gate" technique; and

[0026] FIGS. 2A-2K depict various illustrative methods disclosed herein of forming an isolated channel region for a FinFET semiconductor device and the resulting semiconductor device.

[0027] While the subject matter disclosed herein is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention.

DETAILED DESCRIPTION

[0028] Various illustrative embodiments of the present subject matter are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

[0029] The present subject matter will now be described with reference to the attached figures. Various systems, structures and devices are schematically depicted in the drawings for purposes of explanation only and so as to not obscure the present disclosure with details that are well known to those skilled in the art. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present disclosure. The words and phrases used herein should be understood and interpreted to have a meaning consistent with the understanding of those words and phrases by those skilled in the relevant art. No special definition of a term or phrase, i.e., a definition that is different from the ordinary and customary meaning as understood by those skilled in the art, is intended to be implied by consistent usage of the term or phrase herein. To the extent that a term or phrase is intended to have a special meaning, i.e., a meaning other than that understood by skilled artisans, such a special definition will be expressly set forth in the specification in a definitional manner that directly and unequivocally provides the special definition for the term or phrase.

[0030] The present disclosure generally relates to various methods of forming an isolated channel region for a FinFET semiconductor device and the resulting semiconductor device. Moreover, as will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to a variety of devices, including, but not limited to, logic devices, memory devices, etc., and the methods disclosed herein may be employed to form N-type or P-type semiconductor devices. The methods and devices disclosed herein may be employed in manufacturing products using a variety of technologies, e.g., NMOS, PMOS, CMOS, etc., and they may be employed in manufacturing a variety of different devices, e.g., memory devices, logic devices, ASICs, etc. As will be appreciated by those skilled in the art after a complete reading of the present application, the inventions disclosed herein may be employed in forming integrated circuit products using a variety of so-called 3D devices, such as FinFETs. For purposes of disclosure, reference will be made to an illustrative process flow wherein a single FinFET device **100** is formed. Moreover, the

inventions will be disclosed in the context of forming the gate structures using a replacement gate ("gate-last") processing technique. Of course, the inventions disclosed herein should not be considered to be limited to the illustrative examples depicted and described herein. With reference to the attached figures, various illustrative embodiments of the methods and devices disclosed herein will now be described in more detail.

[0031] In one embodiment, the illustrative device **100** will be formed in and above the semiconductor substrate **102**, having a bulk configuration. The device **100** may be either an NMOS or a PMOS transistor. Additionally, various doped regions, e.g., source/drain regions, halo implant regions, well regions and the like, are not depicted in the attached drawings. The substrate **102** may be made of silicon or it may be made of materials other than silicon.

[0032] In other embodiments, the device **100** may be formed on a so-called silicon-on-insulator (SOI) substrate, as described more fully below. Thus, the terms "substrate" or "semiconductor substrate" should be understood to cover all semiconducting materials and all forms of such materials.

[0033] The attached drawings present various views of one illustrative embodiment of a FinFET device **100** that may be formed using the methods disclosed herein. The drawings also include a simplistic plan view of the device **100** (in the upper right corner) that depicts the location where various cross-sectional views depicted in the following drawings will be taken. More specifically, the view "X-X" is a cross-sectional view that is taken through the source/drain (S/D) regions of the device (i.e., along the gate width direction of the device **100**). The view "Y-Y" is a cross-sectional view that is taken through the gate structure of the device in the gate-width direction. The view Z-Z is a cross-sectional view that is taken through the long axis of the fins **106** of the device (i.e., in the current transport or gate-length direction of the device). The drawings also include a reduced-size plan view of the device **100**.

[0034] FIG. 2A depicts the device **100** at a point in fabrication wherein several process operations have been performed. First, a first layer of epi semiconductor material **104** is deposited on the surface of the bulk semiconductor substrate **102**. In one example, the first layer of epi semiconductor material **104** may be a layer of silicon-germanium ($\text{Si}_x\text{Ge}_{1-x}$). The thickness of the first epi semiconductor material **104** may vary depending upon the particular application. In one illustrative embodiment, the layer of epi semiconductor material **104** may have a thickness of about 5-15 nm. The first epi semiconductor material **104** may be formed using any of a variety of different traditional epitaxial deposition processes. Thereafter, a second layer of epi semiconductor material **106** is deposited on the surface of the first epi semiconductor material **104**. In one example, the second layer of epi semiconductor material **106** may be a layer of silicon. The thickness of the second epi semiconductor material **106** may vary depending upon the particular application. In one illustrative embodiment, the second epi semiconductor material **106** may have a thickness of about 20-45 nm. The second epi semiconductor material **106** may be formed using any of a variety of different traditional epitaxial deposition processes.

[0035] FIG. 2B depicts the device **100** after one or more first etching processes, e.g., anisotropic etching processes, were performed on the second layer of epi semiconductor material **106** through a patterned mask layer (not shown) to define a plurality of initial trenches **107** in the second layer of epi semiconductor material **106**. The formation of the

trenches 107 results in the formation of an initial fin structure 108 comprised of a portion of the second layer of epi semiconductor material 106. The width and height of the fin structure 108 as well as the depth of the trenches 107 may vary depending upon the particular application.

[0036] FIG. 2C depicts the device 100 after several process operations were performed. First, the trenches 107 were overfilled with an insulating material 110. The layer of insulating material 110 discussed herein may be comprised of a variety of different materials, such as, for example, silicon dioxide, an oxygen-rich silicon dioxide, etc., or multiple layers thereof, etc., and it may be formed by performing a variety of techniques, e.g., chemical vapor deposition (CVD), etc. Although not depicted, if desired, a chemical mechanical polishing (CMP) process may be performed on the layer of insulating material 110 to planarize its upper surface with that of the patterned mask layer 106. Then, a recess etching process was performed to recess the layer of insulating material 110 to a desired height such that the desired amount of the initial fin structure 108 is exposed above the recessed surface 110R of the layer of insulating material 110.

[0037] FIG. 2D depicts the device 100 after an illustrative sacrificial gate structure 112, gate cap layer 114 and sidewall spacers 116 have been formed on the device 100. The sacrificial gate structure 112 includes a sacrificial gate insulation layer 112A and a dummy or sacrificial gate electrode 112B. Also depicted is an illustrative gate cap 114 and sidewall spacers 116. The various components and structures of the device 100 may be formed using a variety of different materials and by performing a variety of known techniques. For example, the sacrificial gate insulation layer 112A may be comprised of silicon dioxide and the sacrificial gate electrode 112B may be comprised of polysilicon or amorphous silicon. The various layers of material depicted in FIG. 2D, as well as the layers of material described below, may be formed by any of a variety of different known techniques, e.g., a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, a thermal growth process, spin-coating techniques, etc. Moreover, as used herein and in the attached claims, the word "adjacent" is to be given a broad interpretation and should be interpreted to cover situations where one feature actually contacts another feature or is in close proximity to that other feature. The gate cap layer 114 and the sidewall spacers 116 may be comprised of a material such as silicon nitride and they may be formed using traditional techniques. For example, the sidewall spacers 116 may be formed by depositing a layer of spacer material, e.g., silicon nitride, and thereafter performing an anisotropic etching process on the layer of spacer material so as to result in the spacers 116.

[0038] FIG. 2E depicts the device 100 after one or more etching processes were performed to form trenches 102X in the substrate 102. The depth of the trench 102X into the substrate 102 may vary depending upon the application. These etching processes result in the removal of the exposed portions of the second epi material 106 and the first epi material 104 in the areas laterally outside of the spacers 116, i.e., the source/drain regions 117, and in the formation of a fin cavity 108X in the source/drain regions 117. More specifically, these etching processes result in the formation of edges 109 of the fin structure in the gate width direction of the device 100 (i.e., into and out of the plane of the drawing page). As depicted, the exposed edges 109 of the fin structure are substantially self-aligned with the spacers 116. Note that the exposed edges of the fin structure include a portion of the

substrate 102, the first epi semiconductor material 104 and the second epi semiconductor material 106. Also note that a portion of the substrate 102 defines a bottom surface of the fin cavity 108X in the source/drain regions of the device 100, and that the sidewalls of the fin cavity 108X are comprised of a portion of the substrate 102, the first epi material 104 and the second epi material 106. FIG. 2E contains a cross-sectional view "A-A" that is taken at the outer edge of the spacers 116 looking back toward the spacer 116. In one illustrative embodiment, the etching processes that result in the structure depicted in FIG. 2E are anisotropic etching processes that result in the etched structures being approximately self-aligned with respect to the sidewall spacers 116.

[0039] FIG. 2F depicts the device after an epitaxially formed etch stop layer 118 has been formed on and in contact with the exposed edges 109 of the fin structure, i.e., on the exposed surfaces of the second epi material 106, the first epi material 104 and the substrate 102. The etch stop layer 118 is also formed on and in contact with the semiconductor materials that are exposed within the fin cavity 108X. In one illustrative embodiment, the etch stop layer 118 may be comprised of silicon and it may have a thickness that falls within the range of about 3-10 nm.

[0040] FIG. 2G depicts the device 100 after a stressed epi semiconductor material 120 was formed on and in contact with the etch stop layer 118. The stressed epi semiconductor material 120 may be formed with either a tensile or compressive stress depending upon the type of device (N or P) under construction. The purpose of the stressed epi semiconductor material 120 is to impart a desired stress on the materials in the channel region of the device 100. The stressed epi semiconductor material 120 may be made by performing a traditional epitaxial deposition process. In one illustrative embodiment, the stressed epi semiconductor material 120 may be made of silicon-germanium (S_xGe_{1-x}), where the concentration of the germanium may also vary depending upon the particular application.

[0041] FIG. 2H depicts the device 100 after one or more etching processes were performed to remove the gate cap layer 114 and the sacrificial gate structure 112 and thereby result in the formation of a replacement gate cavity 122 where a replacement gate structure will eventually be formed. As will be appreciated by those skilled in the art after a complete reading of the present application, there are several potential process flows to arrive at the point of processing depicted in FIG. 2H wherein the replacement gate cavity 122 has been created. Thus, the exact process flow that may be used to arrive at the structure depicted in FIG. 2H may vary depending upon the particular application. For example, in some applications, a layer of insulating material (not shown) may be deposited above the epi semiconductor material 120 and one or more CMP processes may be formed to effectively remove the gate cap layer 114 so as to expose the sacrificial gate electrode.

[0042] FIG. 2I depicts the device after an isotropic etching process was performed through the replacement gate cavity 122 to remove the underlying portions of the first epi semiconductor material 104 selectively relative to the substrate 102 and the second epi semiconductor material 106. This results in the formation of a channel cavity 124 under the channel region of the device 100. Importantly, the etch stop layer 118 protects the stressed epi semiconductor material 120 during this etching process. Absent the presence of the etch stop layer 118, there may be unwanted consumption of

the stressed epi semiconductor material **120**, which might tend to reduce or eliminate any desired stresses that are intended to be imparted to the channel region of the device due to the formation of the stressed epi semiconductor material **120**.

[0043] FIG. 2J depict the device **100** after the channel cavity **124** was substantially filled with an insulating material **126**, such as silicon dioxide. The insulating material **126** may be formed by performing an ALD deposition process.

[0044] FIG. 2K depicts the device after several process operations were performed. First, several known processing operations were performed to form a schematically depicted replacement gate structure **130** in the gate cavity **122**. The replacement gate structure **130** depicted herein is intended to be representative in nature of any type of gate structure that may be employed in manufacturing integrated circuit products using so-called gate-last (replacement gate) manufacturing techniques. The replacement gate structure **130** typically comprises a high-k (k value greater than 10) gate insulation layer (not individually shown), such as hafnium oxide, one or more metal layers (not individually shown) (e.g., layers of titanium nitride or TiAlC depending upon the type of transistor device being manufactured), and a bulk conductive material layer (not individually shown), such as tungsten or aluminum. Typically, a layer of insulating material **133** (only shown in view Z-Z) is deposited above the device **100**. Thereafter, the various layers of material that will be present in the replacement gate structure **130** are sequentially deposited in the gate cavity **122** and one or more CMP processes are performed to remove excess portions of the gate materials positioned outside of the gate cavity **122**, as described in the background section of this application. Then, one or more etching processes were performed to remove upper portions of the various materials within the cavity **122** so as to form the replacement gate structure **130** and to form a recess above the replacement gate structure **130**. Then, a gate cap **132** was formed in the recess above the recessed gate materials. The gate cap **132** is typically comprised of silicon nitride and it may be formed by depositing a layer of gate cap material so as to over-fill the recess formed in the gate cavity **122** above the replacement gate structure **130** and thereafter performing a CMP process to remove excess portions of the gate cap material layer positioned above the surface of the layer of insulating material **133**. The gate cap **132** is formed so as to protect the underlying gate materials during subsequent processing operations. At this point, traditional manufacturing operations may be performed to complete the fabrication of the illustrative FinFET device **100**, e.g., contact formation, formation of metallization layers, etc.

[0045] The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Note that the use of terms, such as "first," "second," "third" or "fourth" to describe various processes or structures in this specification and in the attached claims is only used as a shorthand reference to such steps/structures and does not necessarily imply

that such steps/structures are performed/formed in that ordered sequence. Of course, depending upon the exact claim language, an ordered sequence of such processes may or may not be required. Accordingly, the protection sought herein is as set forth in the claims below.

What is claimed:

1. A FinFET device, comprising:

- a fin structure positioned in a channel region of said FinFET device, wherein said fin structure comprises:
 - a portion of a semiconductor substrate; and
 - an epi semiconductor material positioned vertically above said portion of said semiconductor substrate;
- a gate structure positioned above said fin structure in said channel region of said FinFET device;
- sidewall spacers positioned adjacent said gate structure, wherein said fin structure has edges in a gate width direction of said FinFET device that are substantially self-aligned with said sidewall spacers;
- a fin cavity positioned in source/drain regions of said FinFET device, wherein said semiconductor substrate defines a bottom of said fin cavity;
- a silicon etch stop layer positioned on and in contact with said edges of said fin structure and within said fin cavity; and
- a stressed semiconductor material positioned on and in contact with said silicon etch stop layer and at least partially within said fin cavity.

2. The FinFET device of claim 1, wherein said silicon etch stop layer is positioned on said bottom of said fin cavity and on sidewalls of said fin cavity.

3. The FinFET device of claim 1, wherein said stressed semiconductor material is silicon-germanium ($\text{Si}_x\text{Ge}_{1-x}$).

4. The FinFET device of claim 1, wherein said gate structure comprises a gate insulation layer and a gate electrode positioned on said gate insulation layer, said gate insulation layer comprising a high-k insulating material and said gate electrode comprising at least one layer of metal.

5. The FinFET device of claim 1, further comprising a gate cap layer positioned above said gate structure.

6. The FinFET device of claim 5, wherein said sidewall spacers are positioned adjacent and laterally confine said gate cap layer.

7. The FinFET device of claim 1, wherein said silicon etch stop layer covers said semiconductor substrate portion of said fin structure and said epi semiconductor material of said fin structure along at least said edges of said fin structure.

8. A FinFET device, comprising:

- a fin structure positioned in a channel region of said FinFET device, wherein said fin structure comprises:
 - a portion of a semiconductor substrate; and
 - an epi semiconductor material positioned vertically above said portion of said semiconductor substrate;
- a gate structure positioned above said fin structure in said channel region of said FinFET device, wherein said gate structure comprises a gate insulation layer and a gate electrode, said gate insulation layer comprising a high-k insulating material and said gate electrode comprising at least one layer of metal;
- sidewall spacers positioned adjacent said gate structure, wherein said fin structure has edges in a gate width direction of said FinFET device that are substantially self-aligned with said sidewall spacers;

a fin cavity positioned in source/drain regions of said FinFET device, wherein said semiconductor substrate defines a bottom of said fin cavity;
 a silicon etch stop layer positioned on and in contact with said edges of said fin structure, on said bottom of said fin cavity, and on sidewalls of said fin cavity; and
 a stressed semiconductor material positioned on and in contact with said silicon etch stop layer and at least partially within said fin cavity.

9. The FinFET device of claim 8, wherein said high-k insulating material has a dielectric constant of approximately 10 or greater and said at least one layer of metal comprises a plurality of metal layers.

10. The FinFET device of claim 8, wherein said gate electrode further comprises a layer of conductive material positioned above said at least one layer of metal.

11. The FinFET device of claim 8, further comprising a gate cap layer positioned above said gate structure, wherein said sidewall spacers are positioned adjacent and laterally confine said gate cap layer.

12. The FinFET device of claim 8, wherein said silicon etch stop layer covers said semiconductor substrate portion of said fin structure and said epi semiconductor material of said fin structure along sidewalls and said edges of said fin structure.

13. A FinFET device, comprising:

a fin structure positioned in a channel region of said FinFET device, wherein said fin structure comprises:
 a portion of a semiconductor substrate;
 an epi semiconductor material positioned vertically above said portion of said semiconductor substrate;
 a gate structure positioned above said fin structure in said channel region of said FinFET device;
 sidewall spacers positioned adjacent said gate structure, wherein said fin structure has edges in a gate width direction of said FinFET device that are substantially self-aligned with said sidewall spacers;

a fin cavity positioned in source/drain regions of said FinFET device, wherein said semiconductor substrate defines a bottom of said fin cavity;

a silicon etch stop layer positioned on and in contact with said edges of said fin structure, on said bottom of said fin cavity, and on sidewalls of said fin cavity, said silicon etch stop layer covering said semiconductor substrate portion of said fin structure and said epi semiconductor material of said fin structure along at least said edges of said fin structure; and

a stressed semiconductor material positioned on and in contact with said silicon etch stop layer and at least partially within said fin cavity, said stressed semiconductor material comprising silicon-germanium ($\text{Si}_x\text{Ge}_{1-x}$).

14. The FinFET device of claim 13, wherein said gate structure comprises a gate insulation layer and a gate electrode positioned on said gate insulation layer.

15. The FinFET device of claim 14, wherein said gate insulation layer comprises a high-k insulating material, and wherein said gate electrode comprises at least one layer of metal.

16. The FinFET device of claim 15, wherein said high-k insulating material has a dielectric constant of approximately 10 or greater.

17. The FinFET device of claim 15, wherein said at least one layer of metal comprises a plurality of metal layers.

18. The FinFET device of claim 15, wherein said gate electrode further comprises a layer of conductive material positioned above said at least one layer of metal.

19. The FinFET device of claim 13, further comprising a gate cap layer positioned above said gate structure, wherein said sidewall spacers are positioned adjacent and laterally confine said gate cap layer.

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