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Dorsman et al.

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[54] **WARP LETOFF CONTROL SYSTEM**

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[73] Assignee: **North American Rockwell Corporation,** El Segundo, Calif.

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[52] **U.S. Cl.**..... **235/151.32,** 235/151.3, 226/30, 73/462

[51] **Int. Cl.** **G06m 1/272,** B65h 59/02

[58] **Field of Search**..... 235/151.3, 151.32; 226/30; 318/445, 467; 73/462

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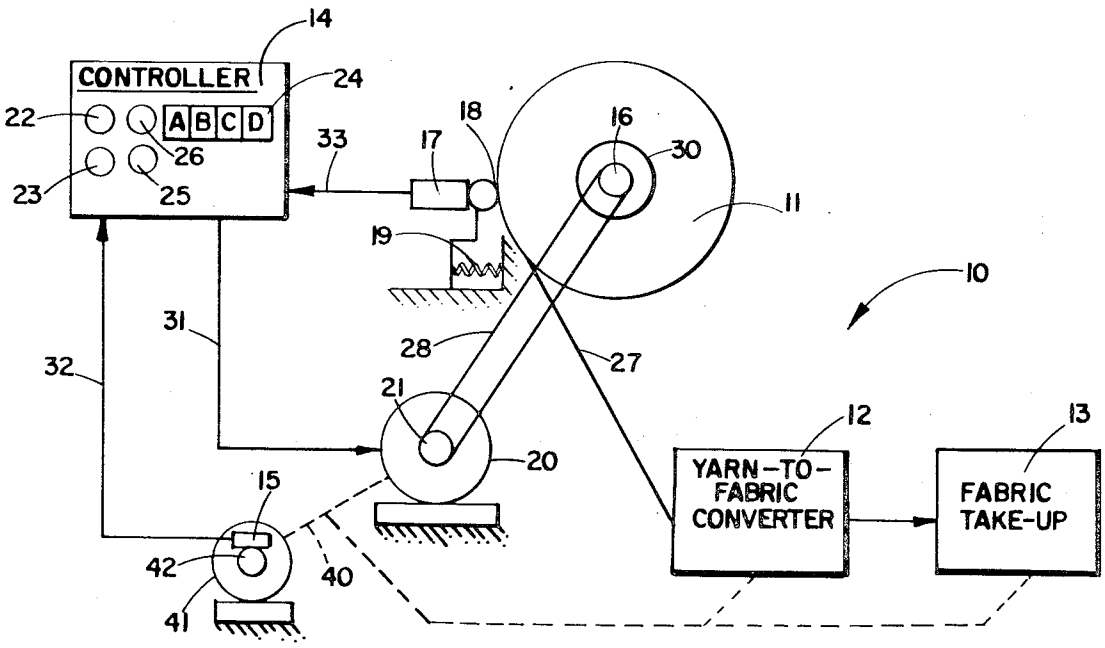
[57] **ABSTRACT**

A control system using electronic components to detect and control the operation of a knitting machine. The control system operates to reliably control the length of yarn which is "let off" or removed from a warp (yarn supply) in accordance with the operation of the knitting machine.

20 Claims, 4 Drawing Figures



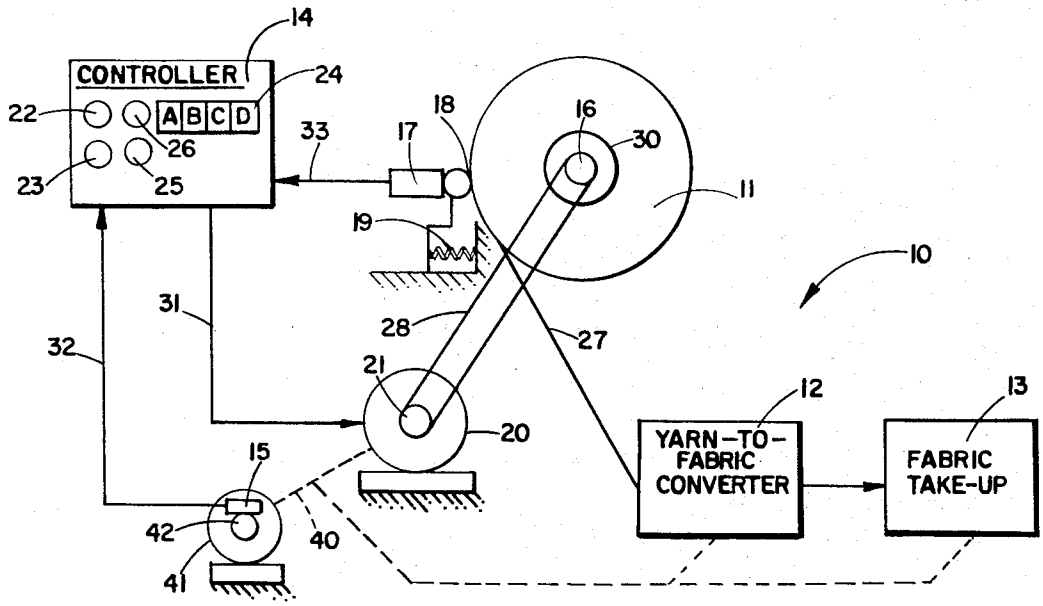

14
CONTROLLER
24
22
A B C D
26
23
25
33
18
17
16
30
11
19
10
31
28
27
32
21
12
13
YARN-TO-FABRIC CONVERTER
FABRIC TAKE-UP
20
15
42
40
41

FIG. 1

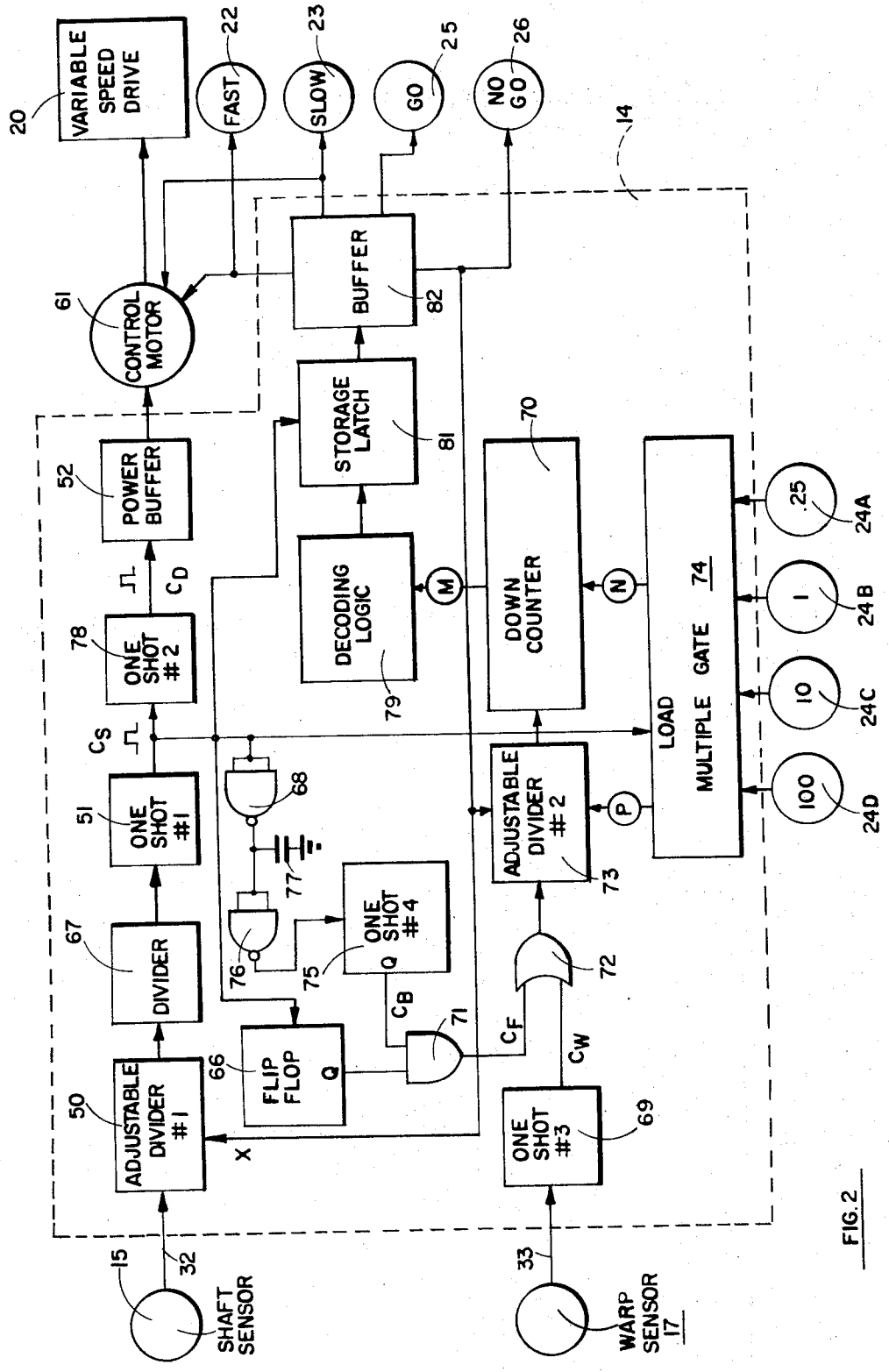

VARIABLE SPEED DRIVE
20
FAST
22
SLOW
23
GO
25
NO GO
26
14
BUFFER
82
CONTROL MOTOR
61
STORAGE LATCH
81
DECODING LOGIC
79
DOWN COUNTER
70
MULTIPLE GATE
74
LOAD
.25
24A
1
24B
10
24C
100
24D
POWER BUFFER
52
ONE SHOT #2
78
ONE SHOT #1
51
DIVIDER
67
ADJUSTABLE DIVIDER #1
50
ADJUSTABLE DIVIDER #2
73
FLIP FLOP
66
ONE SHOT #4
ONE SHOT #3
69
68
76
75
77
71
72
M
N
P
Q
X
C_D
C_S
C_B
C_F
C_W
15
32
SHAFT SENSOR
33
WARP SENSOR
17

FIG. 2

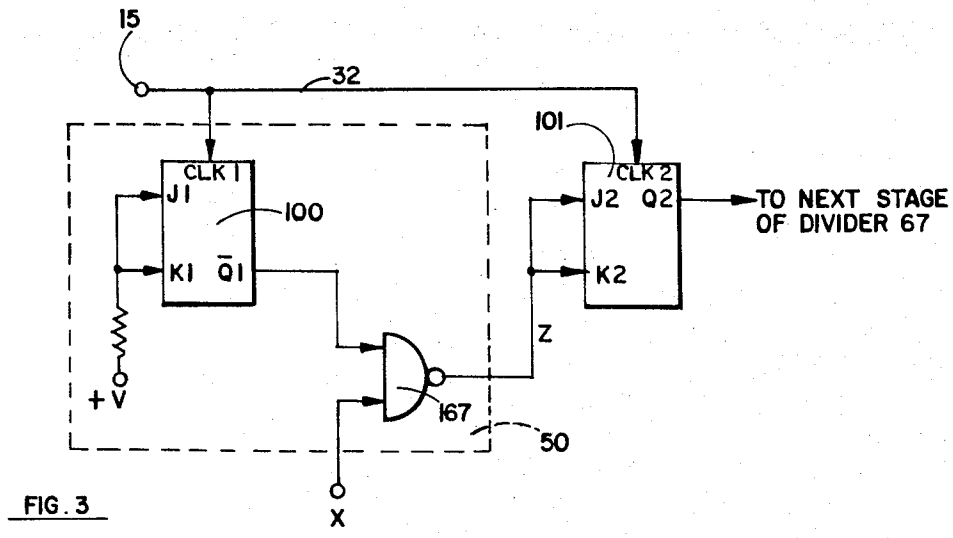

15
32
101
CLK 1
J1
100
K1 Q1
+V
CLK 2
J2 Q2
TO NEXT STAGE
OF DIVIDER 67
K2
Z
167
50
X

FIG. 3

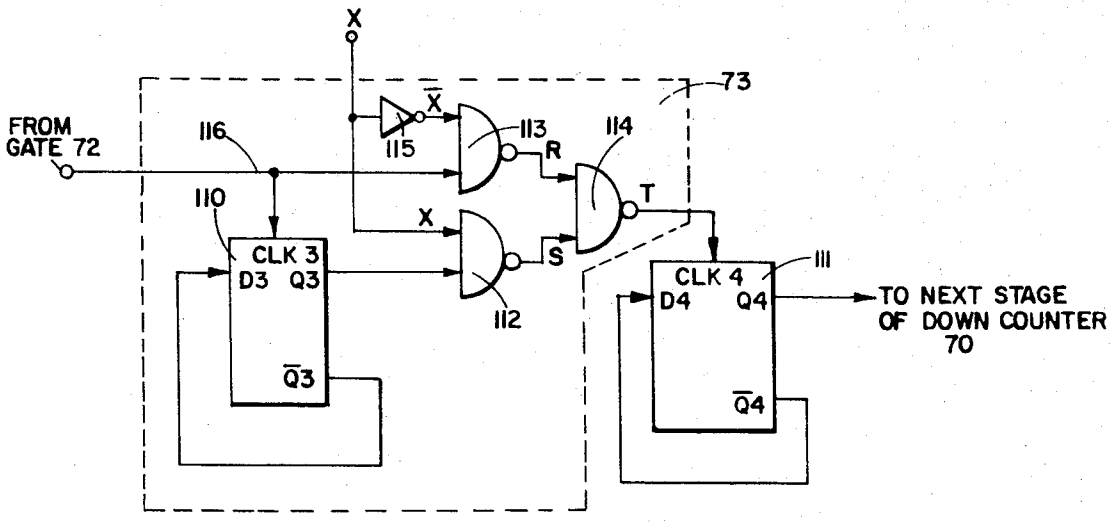

X
73
FROM
GATE 72
116
115
113
R
114
T
110
X
S
CLK 3
D3 Q3
112
111
CLK 4
D4 Q4
TO NEXT STAGE
OF DOWN COUNTER
70
Q3
Q4

FIG. 4

WARP LETOFF CONTROL SYSTEM

BACKGROUND

There are several types of knitting machines available and known to the art. One of these machines is known as the warp knitting machine. This type of knitting machine is capable of turning out fabrics, laces and other involved and intricate textiles in a variety of weights, textures and patterns. The modern warp knitting machine, in a functional sense, consists of three principal assemblies: (1) the yarn (or warp) letoff system, (2) yarn-to-fabric converter, and (3) fabric takeup system.

Briefly, these assemblies serve the functions noted hereinafter. The warp letoff system consists of the mechanism which is necessary to provide multiple yarns (warp), which are prewound on cylindrical beams, to the yarn-to-fabric converter at a specified rate and under controlled tension. The yarn-to-fabric converter includes the needles, guides, sinker bars and the like as well as any other mechanisms required to provide complex, synchronized, and interacting movement of these elements, to effect the knitting process. This assembly, operating on the multiple yarn strands from the warp letoff system, performs the looping and interfacing functions prescribed by the design specification in order to produce the finished fabric or textile. The fabric takeup assembly draws off the finished fabric or textile from the yarn-to-fabric converter at a prescribed rate and winds it onto a suitable form.

The warp letoff system is the portion of the knitting machine which is concerned with the subject invention. The overall function of the warp letoff system is to supply yarn to the needles, via the guide bars, at a rate commensurate with and determined by the stitch construction in accordance with known industry standards. This rate is a variable and is dictated by a manual "runner length" setting. In most embodiments, this setting is expressed in units, e.g. inches, of yarn per machine cycle and provides a control input to the warp letoff control system. Other control parameters are supplied to the warp letoff control system as defined hereinafter. These inputs operate to establish the actual yarn letoff from the warp or beam within a defined accuracy limit.

In the past, a mechanical letoff control system has been utilized with satisfactory efficiency. However, this mechanical control system, while functional, is quite bulky and expensive. The subject invention provides a fully automatic, electronically operated, letoff control system which is less expensive than the mechanical device as well as being substantially smaller in size and weight. In addition, the electronic control system exhibits greater reliability and accuracy in the control operation and is much easier to set up to the desired runner length.

SUMMARY OF THE INVENTION

The control system which forms the subject of this invention includes an electronic circuit which operates upon input signals supplied thereto. Input signals representative of the desired "runner length" (i.e. length of yarn supplied by the warp) are supplied to the control system. Also, input signals representative of the drive shaft rotation and signals representative of the linear velocity of the yarn are supplied to the control system. The shaft signal is representative of the rotational speed of the drive shaft which is substantially constant,

but may assume one or more prescribed speeds under program control. The warp signal represents the linear speed at the periphery of the warp and varies as the diameter of the warp is reduced when yarn is removed from the beam if the beam rotational velocity is not increased to compensate for the removal. The circuit operates upon the input signals and provides output signals representative of the relationships between these input signals. Output signals are supplied to a variable drive system and to output control indicators. The variable drive means causes the beam speed to vary (e.g. increase) as a function of the variation (e.g. decrease) in diameter of the warp on the beam whereby the "runner length" is maintained substantially constant.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic representation of a knitting machine including the control circuit of the instant invention.

FIG. 2 is a block diagram of the circuit which forms the instant invention.

FIGS. 3 and 4 are more detailed logic diagrams of portions of the circuit shown in FIG. 2.

BRIEF DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following description, similar elements in the several drawings bear similar reference numerals.

Referring now to FIG. 1, there is shown a diagrammatic representation of a knitting machine and an associated warp letoff controller which forms the subject invention. In particular, the knitting machine is shown generally at **10.** Warp (or coil yarn) is prewound on a suitable cylindrical shaft or beam **30.** Attached to shaft **30** is a suitable pulley or sheave **16** which is coupled to sheave **21** via a suitable coupling mechanism **28.** Coupling mechanism **28** may represent a suitable drive element such as a gear train, chain, belt or the like. Sheave **21** is attached to the shaft of variable speed drive **20.** Variable speed drive **20** may be any suitable type of variable speed drive such as a friction drive (commonly known as a Floyd drive), hydrostatic drives and/or variable speed belt drives. These type of drives are known in the art.

The yarn from warp **11** is supplied to yarn-to-fabric converter **12** wherein the knitting process is performed. The fabric produced by converter **12** is supplied to fabric takeup **13** which may include a suitable roller or the like. Thus, knitting mechanism **10** operates such that variable speed drive **20** drives beam **30** via the coupling apparatus including coupler **28** whereby yarn **27** is supplied to converter **12.** Fabric from converter **12** is stored on takeup **13.** Variable speed drive **20** is driven by main drive means **41** which may be any suitable prime mover which is synchronous with the yarn-to-fabric converter drive. Drive means **41** is connected to variable speed drive **20,** converter **12** and take-up **13** by a suitable mechanical linkage **40.**

Controller **14** is utilized in order to assure proper operation of the knitting mechanism. That is, the length of the runner of yarn **27** supplied to converter **12** is controlled by controller **14** to a relatively accurate dimension. In particular, sensor **15,** which may be a photoelectric, magnetic or the like sensor, detects the angular velocity or rotational speed of shaft **42** of drive means **41.** A signal representative of the speed of shaft **42** is supplied to controller **14** via line **32.** In addition,

roller 18 is driven by the outer circumference of warp 11. Roller 18 is held in contact with the surface of warp 11 by means of a suitable arrangement suggested by spring 19 which biases roller 18 against warp 11. This construction arrangement is, of course, only illustrative and is not intended to be limitative of the invention. Sensor 17 which may also be a photoelectric, electromagnetic or the like sensor similar to sensor 15, detects the rotational velocity of roller 18 which is proportional to the peripheral velocity of warp 11 and, thus, the linear velocity of yarn 27. Sensor 17 supplies signals representative of this speed characteristic to controller 14 along line 33.

A plurality of switches 24, which may be rotary switches, pushbutton switches or the like, are utilized to manually set in the length of runner which is to be taken from warp 11. The number of switches 24, in the preferred embodiment, is four but a different number of these switches may be utilized as required by the specific configuration of the circuit.

Controller 14, as will be seen hereinafter, operates upon the signals supplied by sensors 15 and 17 as a function of the signal inserted via switches 24. Controller 14 produces a signal representative of this relationship and supplies the signal along line 31 to variable drive means 20. The signal on line 31 is effectively operative to alter, if necessary, the rotational speed of variable speed device 20 to produce a runner letoff within the prescribed dimensional limits from warp 11.

Controller 14 includes indicator lights 22 and 23 which, respectively, indicate whether the variable speed drive 20 is currently operating "fast" or "slow" relative to the ideal speed condition. Also, indicator lights 25 and 26 are utilized to indicate whether the runner letoff is within prescribed dimensional limitations, e.g. within one inch of the desired length. Thus, the operator can determine whether or not the system is operating within limits and, if not, whether the system is correcting in the appropriate manner.

Referring now to FIG. 2, there is shown a block diagram of the control circuit for the instant invention. Shaft sensor 15 (which may be any suitable type of sensing apparatus) is connected via line 32 to the input of adjustable divider 50. Line 32 may comprise a shielded cable wherein the shield is connected to ground. Divider 50 may be of any conventional design and is shown in greater detail in FIG. 3. Generally, however, in this application divider 50 selectively produces output signals of one half or one times the frequency of the signals supplied by sensor 15. Adjustable divider 50 is controlled, in part, by signal X described hereinafter. The output of adjustable divider 50 is connected to conventional divider 67. In this embodiment divider 67 divides by a factor of 32. Thus, the frequency of the signal produced by sensor 15 is divided by 32 or 64 in accordance with the condition of adjustable divider 50.

One output of divider 67 is connected to an input of one shot circuit 51. One shot 51 is of conventional design and is known in the art. The output of one shot 51 is connected to an input of one shot 78. The output of one shot 78 is connected to an input of buffer 52. One shot 78 and buffer 52 are of conventional design.

The above noted output of one shot 51 (labelled C_S) is also connected to one input of flip-flop 66. Also, the C_S signal is supplied to storage latch 81 and multiple gate 74 described hereinafter. Signal C_S is further applied to an input of gate 68. The output of gate 68 is connected to a load consisting of capacitor 77 which is referenced to ground and to an input of gate 76. The output of gate 76 is connected to an input of one shot 75. The Q output of one shot 75 and the Q output of flip-flop 66 are connected to separate inputs of AND gate 71.

Sensor 17 is connected via line 33 to an input of one shot 69. The output terminal of one shot 69 is connected to one input terminal of gate 72 and supplies the signal C_W. The output of gate 71 is also connected to an input of gate 72 and supplies the signal C_F. The output of gate 72 is connected to an input of adjustable divider 73 which is shown in detail in FIG. 4. The function of adjustable divider 73 is similar to the function of adjustable divider 50 and is controlled, in part, by the signal X produced by buffer 82 as described hereinafter.

The output of adjustable divider 73 is connected to an input of down counter or divider 70. The inputs of divider 70 and adjustable divider 73 are connected to outputs of multiple gate 74 via lines P and N. Lines P and N represent the appropriate number of lead lines to transfer the pertinent information. The inputs of gate 74 are connected to switches 24A through 24D to receive signals therefrom. The outputs of divider 70 are connected to decoding logic circuit 79 which produces an output signal representative of the signals supplied thereto. The outputs of logic circuit 79 are connected to storage latch 81 which (when enabled by signal C_S) provides a suitable signal at an input to buffer 82.

Two of the output terminals of buffer 82 are connected to indicators 25 and 26 discussed relative to FIG. 1. In addition, other output terminals of buffer 82 are connected to control motor 63 (which may be a stepper motor) and to indicators 22 and 23. Control motor 61 is connected to control operation of variable speed drive 20.

In the operation of the circuit, concurrent reference is made to all of the figures. Switches 24A through 24D are utilized to manually set into the control system, signals representative of the desired length of the runner letoff yarn. For example, switch 24A controls the runner letoff dimensions in terms of approximately one quarter of an inch. Similarly, switches 24B, 24C and 24D control the runner letoff dimension in terms of 1, 10 and 100 inches, respectively. Of course, the specific letoff dimensions recited above are not fixed and can be adjusted to the individual utilization of the device. Moreover, the dimensions may not be in inches but may be in meters or the like.

The signals representative of the settings of switches 24A through 24D are applied to multiple gate 74. The signals supplied by switches 24A through 24D essentially provide information to gate 74. With the application of the enable signal C_S (described hereinafter), gate 74 is enabled and the data information supplied by switches 24A through 24D is transferred to adjustable divider 73 and countdown divider 70, along lines P and N, respectively. Of course, the actual circuitry of gate 74 may be included in the divider networks in some configurations. In that case, switches 24A through 24D would be connected directly to the divider/gate circuit. Moreover, as noted supra, switches 24A through 24D need not be limited in number to four but may be any number greater than or less than the four illustrated.

One input to the system is supplied through the switch controls.

Shaft sensor **15**, shown best in FIG. **1**, is arranged adjacent to shaft **42** which forms a portion of the machine drive train. Shaft **42** may be located at the main drive motor **41** or at any other proportionally synchronized part of the machine drive train where uniform operation of the machine is produced. A pulse train representative of the rotation of shaft **42** is supplied along line **32** to adjustable divider **50** which is described relative to FIG. **3**. Divider **50** produces output signals representative of the input signals supplied thereto. As suggested supra, depending upon the condition of the signal X, divider **50** supplies to divider **67** output signals equal in frequency to the input signal train or one half that frequency. The half frequency (i.e. divide-by-two) state of divider **50** is the normal state while the divide-by-one state is the excess error i.e. "fast" or "slow" run state.

The output signal from divider **67** is supplied to one shot **51** to represent another count function of the input signal. For example, the signal supplied to one shot **51** represents every sixty-fourth input signal (in the "normal" state). This count function is related to the machine operation cycle and permits greater control accuracy. In response to the input signal from divider **67**, one shot **51** produces output signal C_S. . As suggested supra, the leading edge of signal C_S is supplied to and enables multiple gate **74** such that the information applied to the gate from switches **24A** through **24D** is transferred to and stored in divider **70**. In addition, signal C_S is supplied to storage latch **81** to enable this circuit whereby the signals supplied thereto from decoding logic circuit **79** are also determined on the leading edge of the signal C_S. The signals generated by storage latch **81** are applied to buffer **82**. In accordance with the signal conditions presented at the decoding logic (see Table I) the indicators **22** or **23** and **25** or **26** are illuminated. Also, a signal of appropriate polarity is supplied to control motor **61** whereby the motor can, when enabled, selectively affect the operation of variable speed drive **20**.

The trailing edge of the C_S signal is used to initiate operation of one shot **78**, flip-flop **66** and, via gates **68** and **76**, one shot **75**. When one shot **78** is operated, the shaped and stretched signal C_D is applied to buffer **52**. This signal is operated upon and amplified by buffer **52** and then supplied to control motor **61**. The signal from buffer **52** essentially enables control motor **61** which is then rendered operative in accordance with the signals supplied by buffer **82**. That is, the signals from buffer **82** are continuously supplied to control motor **61**. However, control motor **61** is not rendered operative until signal C_D is supplied to buffer **52**. At that time, control motor **61** affects the operation of variable speed drive **20**. Consequently, variable speed drive **20** will increase (or decrease) the rotational speed of shaft **16** (see FIG. **1**) as determined by decoding logic circuit **79**, described hereinafter.

In addition, the trailing edge of signal C_S is supplied to gate **68**. Gate **68** is connected in the logical NAND configuration and, via capacitor **77**, controls the input of gate **76**. Gate **76** is also connected in the logical NAND configuration but does not react to an output signal from gate **68** until the switching threshold of gate **76** has been achieved. That is, while capacitor **77** is charging to the switching threshold voltage of gate **76**, there is no change in the operation of gate **76**. In effect, gates **68** and **76** provide a delay in the application of the trailing edge of signal C_S to the input of one shot **75**.

Also, the trailing edge of the C_S signal is effective to cause flip-flop **66** to change operating state. The Q output of flip-flop **66** is supplied to an input of AND gate **71**. The Q output or signal C_B of one shot **75** is supplied to another input of AND gate **71**. In essence, the purpose of gates **68** and **76** in delaying the operation of one shot **75** is to assure that the operation of flip-flop **66** has "settled" and that a transient condition is not inadvertently established or detected. When the Q signal from flip-flop **66** and the C_B signal from one shot **75** are simultaneously of predetermined levels, for example, both positive or true, gate **71** produces an output signal C_F which is supplied to adjustable divider **73** via gate **72**. Conversely, if one of the signals Q or C_B is not of the prescribed level, an output signal C_F is not produced by gate **71**. Since a pulse is produced at the Q output only for every second signal C_S, signal C_F is supplied to adjustable divider **73** (via gate **72**) only on every other clock pulse, i.e. signal C_S. Thus, the count-down signal normally supplied by warp sensor **17** to decoding logic **79** via adjustable divider **73** and down counter **70** is adjusted (i.e. increased by one count) during alternate C_S signals. The purpose of this operation is discussed hereinafter.

Warp sensor **17** produces a pulse train which is representative of the linear velocity of the yarn, and more particularly the rotational speed at the periphery of the warp. Obviously, as yarn is withdrawn from the beam, the circumference of the warp will decrease whereby shorter runner lengths will be produced for a given number of revolutions of the beam. Consequently, the signals from warp sensor **17** are utilized to provide an indication of this instantaneous condition so that a modification in the speed of shaft **16** can be made, if required.

Warp sensor **17** supplies signals representative of the yarn velocity to one shot **69** via line **33**. These signals, in effect, relate to the tangential speed of the yarn on beam **11**. Output signal C_W from one shot **69** is supplied to a second input of previously described OR gate **72**. The output of OR gate **72** is connected to an input of adjustable divider **73** described hereinafter relative to FIG. **4**. For each pulse detected by warp sensor **17**, a C_W pulse is supplied via gate **72** to alter the status of adjustable divider **73**. That is, the status or "count" installed in adjustable divider **73** and down counter **70**, in response to the settings of switches **24A** through **24D**, is altered by each signal supplied via gate **72**. In particular, the signals supplied via gate **72** cause the combination of adjustable divider **73** and down counter **70** to be counted down rom the preset count, established by the switches, toward a condition of all zeroes or beyond. The instantaneous count condition is supplied to decoding logic circuit **79** by interface line M. This count condition is continuously changing and decoding logic circuit **79** is continually supplying an appropriate signal to storage latch **81**.

In effect, the preset count inserted into down counter **70** represents the runner length which is desired to be obtained from the warp. The runner length is a function of the speed of rotation, the number of rotations and the diameter of the warp. Consequently, by taking the signals from warp sensor **17** and counting down the signal condition in down counter **70**, decoding logic cir-

cuitry **79** can, in effect, establish the length of yarn removed from the beam during a definable time period. This time period is a function of the clock signal C_S. Consequently, as the diameter and the circumference of the warp are reduced as the yarn is removed therefrom, the frequency of the pulses produced by sensor **17** decreases. That is, the tangential speed of the warp decreases whereby the sensor operation decreases. As this pulse frequency decreases, down counter **70** is counted down to a different number between the clock pulse produced by one shot **51** which, essentially, reloads down counter **70** from multiple gate **74** and samples decoding logic **79.** Consequently, decoding logic **79** interprets a number which is different from the prescribed number and produces a signal wherein the runner length is indicated to be in error.

The signal produced by decoding logic **79** is applied via storage latch **81** and buffer **82** to control motor **61.** Control motor **61** is activated by a pulse from buffer **52** (i.e. signal C_D) and steps or moves in a direction dictated by the signal from buffer **82.** The activation of motor **61** causes variable speed drive **20** to be altered so that the shaft **16** is driven at a different rotational speed. In a simplified analogy concept, activation of control motor **61** may be considered as changing the gear ratio of variable speed drive **20.** That is, since warp sensor **17** through the countdown procedure essentially measures a given distance or length of yarn which is removed from the warp, the same number of counts should, ideally, be produced for each runner in order to maintain the runner length within the prescribed limits of accuracy. However, inasmuch as the diameter of the warp is being continuously reduced as yarn is removed therefrom, the number of rotations of roller **18,** and, thus, the number of signals produced by sensor **17** is reduced for each rotation of the warp beam. Therefore, in order to make the appropriate adjustment in the system wherein sensor **17** produces a substantially constant number of pulses between clock pulses C_S, the speed of shaft **16** must be increased. The speed of shaft **16** is increased by adjusting variable speed drive **20** in accordance with the signal supplied to control motor **61** via buffer **82.**

As suggested supra, signal X is also produced by buffer **82** is conjunction with the "no-go" signal indicated by indicator lamp **26.** This condition is an error condition which is beyond the acceptable limits for the specific knitting machine wherein a rapid correction operation is desirable. Essentially, the X signal is supplied to adjustable dividers **50** and **73** to alter the operation thereof from a divide-by-two to a divide-by-one operation. In essence, this speeds up the operation of the system by a factor of two. That is, the signals supplied to one shot **51** are divided only by the factor inserted by divider **67.** (See FIG. **3** and related description). Similarly, the signals supplied to decoding logic **79** are divided only by down counter **70.** (see FIG. **4** and related description). Typically, the signal C_S produced by one shot **51** would be on every **64**th pulse produced by shaft sensor **15.** However, in response to the error condition of signal X, the signal C_S is produced on every **32**nd pulse. Thus, the sampling rate is twice the normal rate whereby control motor **61** is stepped at twice the normal rate. Consequently, the control system can achieve the desired rate of speed more rapidly than in the normal condition.

The signals exhibited in Table I relative to each of the count positions **0-15** represents the signal condition at the output of down counter **70** and adjustable divider **73.** These signals are supplied and operated upon by decoding logic **79** wherein a representative signal is supplied to storage latch **81,** and, in response to clock signal C_S, to buffer **82.** As long as the signals are between counts **4** and **11,** as noted supra, the machine is in the "go" condition and indicator **25** is operated. In addition, if the signal supplied is between counts **4** and **7,** the machine is running somewhat slow wherein indicator **23** will be operated. Conversely, if the signal is between counts **8** and **11,** the machine is running somewhat fast and indicator **22** will be operated. When the appropriate signal is supplied from buffer **82** to control motor **61,** control motor **61** is stepped an appropriate number of steps in response to the signal from power buffer **52.** Of course, if the signal is represented by counts **0-3** or **12–15,** a "no-go" condition exists and the "no-go" indicator **26** is operated along with the appropriate fast or slow indicator.

Moreover, signal X or X is generated by buffer **82** is accordance with the signal supplied thereto. If the signal from decoding logic is in the count positions **4–11,** signal X is produced while signal X is produced when the decoding signal is in count positions **0-3** and/or **12–15.** As discussed supra, signal X causes a speed up operation wherein the machine attempts to approach the appropriate operating condition in a rapid operating mode by adjusting the operation of dividers **50** and **70.**

In the so-called "normal" operating condition, warp sensor **17** supplies signals via one shot **69** and gate **72** to the down counter circuit comprising down counter **70** and adjustable divider **73.** These signals are supplied at the rate wherein, ideally, seven counts are produced from gate **72** between consecutive clock pulses C_S. However, in order to avoid a static or deadband condition, the circuit comprising flip-flop **66** and one shot **75** periodically produces an additional pulse C_F which is supplied to the countdown system.

The foregoing description of the operation of the circuit describes a typical operation. That is, in this type of operation, when the "all-zeroes" condition is reached in down counter **70,** the system does not produce an error signal and the system is in a prescribed running condition. At the "all-zeroes" condition, i.e. count **7** in Table I, a "dead-band" running state is achieved and motor **61** is not activated. However, it is sometimes more desirable to have a "hunting" type of operation by the system in order to prevent the system from establishing a set position and incurring excessive backlash or the like when an error is to be corrected. Consequently, in a preferred embodiment of the invention, flip-flop **66** and one shot **75** operate to selectively produce signal C_F from AND gate **71** on alternate clock signals C_S. As noted supra, the signal C_F is transferred via Or gate **72** to adjustable divider **73** to insert an additional count into the down counter operation. That is, in addition to the normally occurring signals C_W from one shot **69,** signal C_F is inserted into the count down procedure. Thus, instead of the down counter being affected only by the C_W signals, an additional pulse (in effect $C_W + 1$) is counted by down counter **70** on alternate sampling times by clock pulse C_S.

As is seen in Table I reproduced below, in the standard operation, signals C_W are effective to count down from the initial condition count (O) to the "all-zeroes" condition count(7). If the machine is operating more slowly than is desirable, then the counting from count 0 will not reach count 7 between consecutive clock signals C_S. If the machine is operating more rapidly than is desired, then the count will go beyond the all zeroes condition for each alternate clock pulse C_S.

In normal operation, the count detected by down counter **70** between consecutive clock pulses will be, initially, a seven count and then an eight count operation. Thus, the signals supplied to decoding logic **79** will alternately be the count (7) or count (8) signals which are applied to the remainder of the circuit and operated upon. Consequently, for each clock pulse C_S supplied by signal C_F, the oscillation noted above is maintained even though the warp continues to rotate at a seven count rate. It should be noted that the drive motor is alternately driven one step fast, then one step slow even though there may be no change in warp **17.** This operation is possible inasmuch as enough backlash exists in motor **61** to prevent changes in speed of warp **71** for alternate fast and slow pulses. If the alternate pulse is not supplied, motor **61** would be driven several pulses in one direction in overcoming the backlash thereby causing warp **17** to change speed (e.g. faster). Consequently, several reverse pulses would be required to overcome the motor backlash before the warp could be again slowed to the proper rate. The average speed attained will be 7.5 counts, which is too fast by a half count as is seen in Table I.

TABLE I

DOWN COUNTER TRUTH TABLE

	L	K	J	I	H	G	F	E	D	C	B	A	COUNT		
DOWN COUNT ↓	0	0	0	0	0	0	0	0	0	1	1	1	0		NO-GO=X
	0	0	0	0	0	0	0	0	0	1	1	0	1		
	0	0	0	0	0	0	0	0	0	1	0	1	2		
	0	0	0	0	0	0	0	0	0	1	0	0	3		
	0	0	0	0	0	0	0	0	0	0	1	1	4		
	0	0	0	0	0	0	0	0	0	0	1	0	5		
	0	0	0	0	0	0	0	0	0	0	0	1	6	SLOW	
	0	0	0	0	0	0	0	0	0	0	0	0	7	↕	GO =$\bar{X}$
	1	1	1	0	0	1	1	0	0	1	1	1	8		
	1	1	1	0	0	1	1	0	0	1	1	0	9	FAST	
	1	1	1	0	0	1	1	0	0	1	0	1	10		
	1	1	1	0	0	1	1	0	0	1	0	0	11		
	1	1	1	0	0	1	1	0	0	0	1	1	12		
	1	1	1	0	0	1	1	0	0	0	1	0	13		NO-GO=X
	1	1	1	0	0	1	1	0	0	0	0	1	14		
	1	1	1	0	0	1	1	0	0	0	0	0	15		

which generates a signal C_D, control motor **61** will receive an operational signal from buffer **82.** Control motor **61** will alternately be stepped forward and stepped backward an amount indicated by the count (7) and count (8) signals relative to the normal position. This operation will cause variable speed drive **20** to alternately speed up and slow down wherein a hunting type condition exists. As a result, the system operates at a rate equivalent to a seven count, but appears to operate on 7.5 counts, for an ideal operating condition. This type of operation avoids any problems of backlash or the like which could occur in the event that a static or dead-band operating condition were permitted.

In other words, if the added alternate count is not supplied, the controller would tend to cause the warp rate to be 7.5 counts rather than 7. That is, if the input switch is initially set to count (7), and the warp actually rotates at a rate equivalent to seven counts, the count would reach the all-zero condition. This condition would cause decoding logic **79** to indicate a "slow" condition and the warp would speed up until a rate equivalent to eight counts results wherein a "fast" condition is indicated by decoding logic **79.** Now the warp rotational rate is slowed down until the desired seven count rate is obtained. However, this will again cause a speed-up of warp rotation since a "slow" condition is indicated. It can be seen that the actual rate then will oscillate between seven and eight counts for an average rate of 7.5 counts.

When the additional alternate count is externally

The logic equations for the operation of the circuit are suggested in Table II reproduced infra. The letter designations relate to the bit positions of the signals as produced by down counter **70.** It is readily apparent that the slow and fast signals are readily ascertained, for example, by detecting and/or observing the most significant bit at each clock pulse. The other logic equations are relatively self-evident.

TABLE II

LOGIC EQUATIONS

$\text{SLOW} = \bar{L}\, C_S$

$\text{FAST} = L\, C_S$

$\text{GO} = \bar{C}\,\bar{D}\,\bar{E}\,\bar{F}\,\bar{G}\,\bar{H}\,\bar{I}\,J\,\bar{K} + C\,\bar{D}\,\bar{E}\,F\,G\,\bar{H}\,\bar{I}\,J\,K = \bar{X}$

$\text{NO GO} = \overline{GO} = X$

In order to better understand the operation of the adjustable dividers, adjustable divider **50** is shown in FIG. **3.** Referring to FIG. **3,** shaft sensor **15** is shown connected via line **32** to the clock input terminal of J-K flip-flops **100** and **101.** The J1 and K1 inputs of flip-flop **100** are connected to and constantly receive a +V signal which is equivalent to a high input signal. As is well known in the operation of J-K flip flops, when both of the input signals are high, a clock signal will cause toggle operation wherein the output signal levels are reversed. Conversely, when both of the inputs are low level signals, no change in the output signal levels will occur in response to the application of a clock signal. Therefore, flip-flop **100** will change state with the application of each clock signal on line **32.** If it is initially assumed that the $\overline{Q1}$ signal is a low level signal, a clock

pulse will cause flip-flop **100** to change states wherein the $\overline{Q1}$ signal switches to the high level. The flip-flop will remain in this condition until the next clock pulse wherein the $\overline{Q1}$ output signal will switch to the low level. This signal reversing operation will continue so that flip-flop **100** produces output signals at one half the frequency rate of the input signals at line **32.** Clearly, with the application of high level input signals at the J2 and K2 inputs, flip-flop **101** will operate in the same fashion.

However, the signals to the J2, K2 inputs of flip-flop **101** are controlled by gate **67** which produces the output signal Z. Moreover, the operating condition of gate **67** is, in part at least, controlled by input signal X noted supra. That is, if it is initially assumed that the proper operating or normal condition of the system exists, the signal X is a continuous high level signal which is supplied to one input of gate **67.** This signal, in effect, enables gate **67** wherein the output signal Z is an inverse function of signal $\overline{Q1}$ applied to another input of gate **67.** That is, signal Z will have the same frequency but opposite polarity of signal $\overline{Q1}$. Consequently, the J2, K2 input terminals will receive high level signals for fifty percent of the operating time and low level signals for the remaining time. Thus, it is seen that when signal Z is high, a clock pulse will produce, for example, a high level output signal at Q2. However, since signal Z is one half the frequency of the clock pulse, signal Z will be a low level signal upon application of the next clock signal. As noted supra, flip-flop **101** will not change state when both input signals are low. Consequently, output signal Q2 remains a high level signal. In the meantime, signal Z switches to the high level before the next clock signal wherein the next clock signal will effect a change in the output conditions of flip-flop **101.** Therefore, on the third clock signal, output signal Q2 switches to the low level and remains low until the fifth clock signal is produced concurrently with a high level signal Z to permit changes in the output signal Q2 in response to a clock signal. Clearly, signal Q2 is one half the frequency of signal Z and, thus, one quarter the frequency of the clock signal.

Conversely, if signal X is a low level signal indicating an abnormal operating condition, the output signal produced by gate **67** is clamped in the high level. Thus, signal $\overline{Q1}$ has no effect on the operation of gate **67** and/or flip-flop **101.** Inasmuch as signal Z remains at the high level, flip-flop **101** is now in condition to change output signal states upon application of each clock signal. Thus, the condition described supra relative to flip-flop **100** applies to flip-flop **101** wherein the frequency of signal Q2 is one half the clock signal frequency. Thus, depending upon the condition of signal X, adjustable divider **50** may be considered as having a divide-by-one or a divide-by-two function. The operation of adjustable divider **50** is reflected in the operation of divider **67.**

Referring now to FIG. **4,** there is shown a logic diagram of adjustable divider **73.** The divider circuit is shown, generally, in the dashed outline. The output signal from gate **72** (see FIG. **2**) is supplied to the clock terminal CLK **3** of D-type flip-flop **110.** In addition, this signal is supplied to one input of NAND gate **113.** Another input of gate **113** receives the signal $\overline{X}$ from the output of inverter **115** which is connected to receive the signal X from buffer **82** as shown in FIG. **2.** Signal X is also supplied to an input terminal of NAND gate **112.** The other input of gate **112** is connected to output terminal Q3 of flip-flop **110.** Output terminal of $\overline{Q3}$ flip-flop **110** is connected to input terminal D3 thereof.

The output terminals of gates **113** and **112** (i.e. R and S, respectively) are connected to input terminals of NAND gate **114.** Output terminal T of gate **114** is connected to the clock CLK **4** terminal of D-type flip-flop **111.** Output terminal $\overline{Q4}$ of flip-flop **111** is returned to input terminal D4 thereof. Output terminal Q4 of flip-flop **111** is connected to further stages of down counter **70** (see FIG. **2**).

In considering the operation of the circuit, signal X is normally a high level or positive signal when the system is operating within the prescribed operational limits. This high level signal is supplied to gate **112** and is inverted by inverter **115** wherein a low level signal is supplied to gate **113.** Since NAND gates require all positive input signals to produce a negative or low level output signal, the output signal at terminal R (hereinafter, signal R) of gate **113** is clamped at the high level in response to the low level signal $\overline{X}$. Therefore, regardless of the signal condition on line **116** from gate **72,** signal R is a high level signal.

A D-type flip-flop operates such that the signal applied at the D input is, upon application of a clock signal, transferred to the Q output terminal of this flip-flop. In addition, the $\overline{Q}$ output signal will be of the opposite level from the Q signal. Consequently, with the configuration shown, having signal $\overline{Q3}$ returned to input terminal D3, the signal level at terminal Q3 will switch upon application of each clock signal along line **116.** This operation produces signals Q3 having one half the frequency of the signals on line **116.**

These alternating signals Q3 are supplied to gate **112** along with the positive X signal. When signal Q3 is positive signal S at the output of gate **112** is negative and vice versa. That is, the positive signal X essentially enables gate **112** which is then controlled by signal Q3. Inasmuch as signal R has been defined as clamped at the high level, signal S similarly controls the operation of gate **114** and, thus, signal T at the output of gate **114.** It is clear that signal T has a frequency which is the same as the signal Q3 which is one half the frequency of the signal supplied on line **116.** The similarity in circuit configurations of flip-flops **110** and **111** is readily apparent. Consequently, the operation of flip-flop **111** is substantially the same wherein output signal Q4 is one half the frequency of the clock signal T. As a result, signal Q4 is equal to one fourth the frequency of the signal supplied on line **116** when signal X is positive and indicative of "normal" operation.

However, when abnormal operation is detected, signal X changes to the low level and is supplied to gate **112.** In addition, inverter **115** supplies the high level signal $\overline{X}$ to gate **113.** Now gate **112** is clamped by the low level input signal and produces a high level output signal S. Consequently, regardless of the operation of signals on line **116** or the operation of flip-flop **110,** gate **112** produces a constant high level output signal S. On the contrary, signal R produced by gate **113** is a direct function of and the same frequency as the signal produced on line **116.** That is, if a high level signal is produced on line **116,** gate **113** produces a low level signal R. Conversely, a low level signal on line **116** produces a high level signal R from gate **113.**

Again, gate **114** is, essentially, enabled by the high level input signal S and produces high or low level out-

put signals which are of opposite polarity to but of the same frequency as signal R. Therefore, the signals applied to clock input CLK 4 of flip-flop **111** are of the same frequency as the signals supplied on line **116.** Consequently, with the operation of gate **111,** output signals Q4 are of one half the frequency of the signals on line **116.** Therefore, in accordance with the level of signal X, signals Q4 are one half or one fourth the frequency of the signals on line **116.** Inasmuch as flip-flop **111** may be considered to be the first stage in down counter **70,** flip-flop **110** and, thus, adjustable divider **73** may be considered to have a divide-by-one or a divide-by-two function.

Thus, there is shown and described an electronic warp letoff controller system. This controller is especially designed for use with warp knitting machines. However, the controller system may find many other useful applications. Furthermore, the controller shown and described herein represents a preferred embodiment of the instant invention. Many of the detailed showings are for illustrative purposes and are not intended to be limitative of the invention. Those skilled in the art may devise modifications which may be made to this system but which fall within the purview of the inventive concepts shown and disclosed. The figures and the description related thereto are not intended to, in any way, limit the scope of the invention. Rather, the scope of the invention is limited only by the claims appended hereto.

Having thus described a preferred embodiment of the invention, what is claimed is:

1. In combination,
- first input means for supplying a predetermined input signal,
- second input means for supplying a regularly recurring input signal,
- third input means for supplying an input signal having a variable frequency rate,
- logic means for receiving the input signals from said first, second and third input means and for producing an output signal representative of a relationship between said input signals from said first and third input means as a function of the input signals from said second input means, and
- utilization means connected to receive said output signal from said logic means.

2. The combination recited in claim **1** wherein said utilization means includes a variable speed drive device which has the speed thereof controlled as a function of said output signal from said logic means.

3. The combination recited in claim **1** including counter means connected to receive said input signals from said first and third input means and to supply signals to said logic means.

4. The combination recited in claim **3** including pulse shaping means connected between said third input means and said counter means.

5. The combination recited in claim **4** including control means for selectively supplying some of said regularly recurring input signals from said second input means to said counter means to affect the count relationship between said input signals supplied to said counter means by said first and third input means.

6. The combination recited in claim **5** wherein said control means includes at least one bistable means for supplying a signal to said counter means in response to alternate ones of said regularly recurring input signals supplied by said second input means, and
- pulse delay means for controlling the application of the signal from said bistable means to said counter means as a function of said regularly recurring signals supplied by said second input means.

7. The combination recited in claim **6** wherein said pulse delay means includes a pair of logic gates connected in series,
- energy storage means connected between said pair of logic gates whereby the second logic gate is triggered only after the first logic gate has been triggered and caused sufficient energy to be stored in said energy storage means to trigger said second logic gate,
- one-shot circuit means connected to said second logic gate to receive signals therefrom and to produce an output signal of predetermined length in response to a signal from said second logic gate, and
- an AND gate connected to receive signals from said bistable means and said one shot circuit means and to supply a signal to said counter means upon the concurrent application of prescribed signals, thereby to selectively insert a count signal into said counter means in addition to the variable frequency signals from said third input means.

8. The combination recited in claim **1** wherein said first input means includes manually controlled switches.

9. The combination recited in claim **1** wherein said second and third input means include sensors for detecting motion of separate devices.

10. The combination recited in claim **1** including pulse shaping means for supplying control signals to said logic means in response to said regularly recurring signals from said second input means.

11. The combination recited in claim **1** including buffer means connected between said logic means and said utilization means,
- said second input means connected to supply said regularly recurring signals to said buffer means such that said buffer means supplies signals from said logic means to said utilization means only in response to a signal from said second input means.

12. The combination recited in claim **1** including first and second adjustable divider means connected to receive signals from said first and second input means respectively, and
- said means connecting said logic means to said first and second adjustable divider means to selectively adjust the dividing rate thereof.

13. The combination recited in claim **1** wherein said logic means includes counter means connected to receive said predetermined input signal from said first input means to establish an initial signal condition in said counter means and to receive said variable frequency input signal from said third input means to alter said initial signal condition in said counter means,
- decoding means for detecting the signal conditions at said counter means and producing an output signal representative of said signal condition,
- output buffer means for selectively transferring the output signal from said decoding means to said utilization means in response to a signal from said second input means.

14. The combination recited in claim **13** including

pulse shaping means connected to receive said regularly recurring signals from said second input means, and

means connecting said output buffer means to said pulse shaping means and to said counter means whereby the operation of said counter means and said pulse shaping means is selectively and concurrently altered by a prescribed signal from said output buffer means.

15. The combination recited in claim **1** including buffer gate means connected between said first input means and said logic means,

said buffer gate means being selectively rendered operative in response to a signal produced by said second input means.

16. The combination recited in claim **1** wherein said first input means comprises a plurality of manually controlled switches associated with a knitting machine and said predetermined input signal represents a desired yarn length to be used in the knitting machine operation,

said second input means comprises means for detecting the operation of a direct drive means whereby the speed of the knitting machine operation is detected,

said third input means comprises means for detecting the operation of the yarn supply wherein the variation in speed of the yarn supply is detected, and

said utilization means includes a variable speed drive means for selectively altering the speed of said yarn supply whereby a prescribed relation between the yarn supply and the knitting machine operation is retained.

17. A control system comprising

first sensor means for producing signals representative of motion of a first device,

second sensor means for producing signals representative of motion of a second device,

input means for producing a signal representative of a predetermined value,

first counter means for selectively receiving signals in parallel from said input means in response to a signal from said first sensor means,

said first counter means further receiving signals in series from said second sensor means,

decoding means connected to receive signals from said first counter means which signals are representative of a relationship between the signals supplied to said first counter means in series and in parallel,

output means, and

control means connected to receive signals from said decoding means and to drive said output means in accordance with the signals from said decoding means in response to a signal from said first sensor means.

18. The control system recited in claim **17** including circuit means connected to periodically produce an output signal as a function of signals from said first sensor means and to supply said output signal to said first counter means in addition to signals supplied to said first counter means by said second sensor means.

19. The control system recited in claim **17** including second counter means connected to receive signals from said first sensor means, said first and second counter means each including at least one portion thereof which can selectively vary the counting operation of the respective counters.

20. The control system recited in claim **17** wherein each said portion of said first and second counter means is connected to receive a signal from said decoding means which selectively and concurrently changes the counting operation of the counters.

* * * * *

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,781,532 Dated 12/25/73

Inventor(s) Adrian K. Dorsman and Clark F. Adams

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 6, line 54, change "down rom" to --down from--.

Column 8, line 22, change "X" (second occurrence) to --$\bar{X}$--,

line 25, change "X" (first occurrence) to --$\bar{X}$--.

Signed and sealed this 23rd day of April 1974.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents