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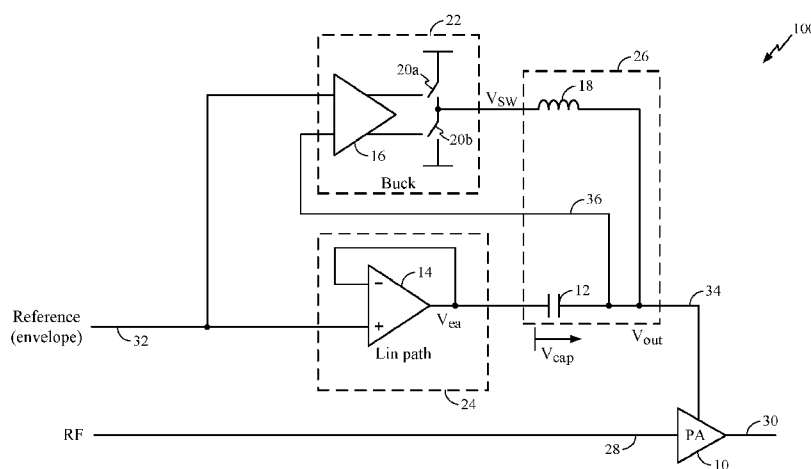
(54) **Title:** CONTROLLED START-UP OF BUCK ENABLED ENVELOPE TRACKING MODULATOR

FIG. 1

(57) **Abstract:** An envelope tracking modulator, comprising a switching amplifier, a correction amplifier, and a combiner for combining the outputs of the switching amplifier and the correction amplifier, to generate as an output an envelope tracked supply voltage tracking a reference signal, further including a boost capacitor for boosting the voltage available at the output, wherein during a start-up phase the increase in voltage across the capacitor is controlled.

CONTROLLED START-UP OF BUCK ENABLED ENVELOPE TRACKING MODULATOR

CROSS REFERENCE TO RELATED APPLICATIONS:

This application claims priority to GB Application No. 1509186.1, filed May 28,
5 2015.

BACKGROUND TO THE INVENTION:

Field of the Invention:

The invention relates to envelope tracking power supplies, and particularly but
not exclusively to envelope tracking power supplies for providing a power supply to a
10 power amplifier of a radio frequency system.

Description of the Related Art:

FIG. 1 illustrates an exemplary envelope tracking (ET) power supply stage 100 for a
power amplifier (PA) 10.

The PA 10 receives a radio frequency (RF) input signal on line 28 and generates
15 an amplified RF output signal on line 30 under the control of a power supply voltage on
line 34 generated by the power supply stage 100.

The power supply stage 100 receives a reference input signal on line 32 and
generates the supply voltage V_{out} on the line 34. The reference signal on line 32 may be
the envelope of the RF signal to be amplified on line 28.

20 The power supply stage 100 includes a switching stage 22, a correction stage
24, and a combiner 26. The combiner includes an inductor 18 and a capacitor 12.

The switching stage 22 includes a buck amplifier 16 which receives the
reference signal on line 32 and drives a pair of switches 20a, 20b in dependence
thereon. The switch 20a is connected to a supply voltage (such as a battery voltage) and
25 the switch 20b is connected to electrical ground. A switching voltage V_{sw} is formed at
the output of the switching stage 22 by switching these two switches 20a, 20b under the
control of the buck amplifier 16. The output of the switching stage 22 is connected to a
first terminal of the inductor 18.

The correction stage 24 includes a linear amplifier 14 which receives the reference signal on line 32 as one input and receives its output as a second input. The linear amplifier 14 generates an output voltage V_{ea} which is a correction to be applied to the output of the switching stage 22. The output of the correction stage 14 is connected
5 to a first terminal of the capacitor 12.

The combiner 26 comprises the capacitor 12 and the inductor 18, and second terminals of each of the inductor 18 and the capacitor 12 are connected together and form the output voltage V_{out} of the supply stage on line 34.

The second terminal of the capacitor 12 is connected to a further input of the
10 buck amplifier 16.

A voltage V_{cap} is developed across the capacitor 12, being the difference between the correction voltage V_{ea} at the output of the linear amplifier 14 and the output voltage V_{out} .

In operation, the output voltage V_{out} is increased by an amount equal to the
15 voltage V_{cap} across the capacitor 12. The output voltage V_{out} is equal to the voltage at the output of the linear amplifier 14, V_{ea} , plus the voltage across the capacitor 12, V_{cap} .

The connection of line 36 from the second terminal of the capacitor 12 to the second input of the buck amplifier 16 permits the voltage V_{cap} across the capacitor 12 to be set by comparing it in the buck amplifier 16 with the reference voltage).

20 The output V_{out} is dictated by the envelope voltage. With any voltage across capacitor, the same voltage is provided on V_{out} .

At start-up, the power supply modulator 100 needs to start-up and reach normal operational status as quickly as possible. In normal operation, a voltage is established across the capacitor 12 which allows the ET modulator output to exceed the battery
25 voltage for short time periods. The capacitor 12 thus needs to be fully charged up during the start-up period. However during the start-up period the ET modulator must draw a limited amount of current.

There is thus a conflict during start-up between the need to charge up capacitor 12 and the need to ensure that a limited amount of current is drawn, i.e. that the
30 capacitor 12 draws a limited amount of current.

It is an aim of the invention to provide an improved circuit.

SUMMARY OF THE INVENTION:

There is disclosed an envelope tracking modulator, comprising a switching amplifier, a correction amplifier, and a combiner for combining the outputs of the switching amplifier and the correction amplifier, to generate as an output an envelope tracked supply voltage tracking a reference signal, further including a boost capacitor for boosting the voltage available at the output, wherein during a start-up phase the increase in voltage across the capacitor is controlled.

After the start-up phase, the voltage across the capacitor may be fully established.

10 The envelope tracking modulator may further comprise a ramp generator which generates a ramp signal which extends from zero volts to a desired capacitor voltage over a period of time which corresponds to the start-up phase, wherein the ramp generator is used to attenuate the voltage generated across the capacitor in the start-up phase. The switching amplifier and the correction amplifier may both receive an envelope of an input signal to be amplified, and wherein the ramp generator controls the application of the envelope signal to the correction amplifier. The switching stage may receive a signal indicative of the voltage of the output. The switching amplifier may control a switching stage in dependence on a difference between the reference signal and the signal indicative of the voltage at the output.

20 The switching amplifier and the correction amplifier may each receive a signal indicative of the voltage to be established across the capacitor and the correction amplifier receives an envelope of an input signal to be amplified, wherein the ramp generator controls the application of the signal indicative of the voltage to be established across the capacitor and the envelope signal to the switching and correction stages. The switching stage may receive a signal indicative of the voltage across the capacitor.

There is also provided a method in an envelope tracking modulator, comprising a switching amplifier, a correction amplifier, and a combiner for combining the outputs of the switching amplifier and the correction amplifier, to generate as an output an envelope tracked supply voltage tracking a reference signal, the method comprising

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boosting the voltage available at the output, and controlling the increase in voltage across the capacitor during a start-up phase.

BRIEF DESCRIPTION OF THE FIGURES:

The invention is described by way of reference to the accompanying figures, in
5 which:

FIG. 1 illustrates an exemplary envelope tracking modulator;

FIGS. 2(a) to 2(d) illustrate the signals and control of the signals at various points in an envelope tracking modulator improved in accordance with the invention;

FIG. 3 illustrates an improved envelope tracking modulator including circuitry
10 for implementing the improvements of the invention; and

FIG. 4 illustrates an alternative improved envelope tracking modulator including circuitry for implementing the improvements of the invention.

DESCRIPTION OF PREFERRED EMBODIMENTS:

The invention is described in the context of exemplary implementations. The
15 invention is not limited to such exemplary implementations and is more broadly applicable. The invention is not limited to any detail of any exemplary implementation unless explicitly stated.

The invention allows a soft start by controlling a ramp rate. This control prevents an abrupt start which would draw current too quickly. Advantageously the
20 invention allows fast start-up while controlling the current drawn by the capacitor 12.

The voltage across the capacitor 12 is ramped up during a preamble of a start-up produce, and the current drawn is therefore controlled during this start-up procedure.

With reference to **FIG. 1**, at the commencement of start-up there is zero volts across the capacitor 12. As start-up commences, the power supply is started quickly, and
25 the power supply is ready to transmit any signal having a peak voltage below the battery voltage, minus a small voltage to give the linear stage some headroom.

For WiFi signals, the first part of a transmitted signal after power-up is the preamble, and is of low amplitude compared with the payload. Therefore the transmission of the signal can commence before the capacitor 12 is fully charged, and

the preamble period used to fully charge the capacitor. This allows the capacitor to be charged without any penalty in the performance of the transmitter.

FIGS. 2(a) to 2(d) show exemplary signalling and signal levels in accordance with the invention. In the figure, **FIG. 2(a)** shows an exemplary output voltage waveform corresponding to V_{out} , **FIG. 2(b)** shows an exemplary mode select signal, which indicates selection of the power supply, **FIG. 2(c)** illustrates the voltage V_{cap} across the capacitor 12, and **FIG. 2(d)** illustrates the maximum available ET voltage.

In an ideal implementation the maximum available ET voltage is the battery voltage V_{bat} plus the voltage across the capacitor 12, V_{cap} .

In practice, this overall available voltage is reduced by a saturation voltage, V_{sat} , such that the maximum available ET voltage is $V_{bat}-V_{sat}+V_{cap}$. For the purposes of simplicity of explanation the saturation voltage is not referred to in the following, but it will be understood that it is present and reduces the maximum available voltage.

The power supply stage 100 switches from an inactive state to an active state responsive to a mode select signal switching from a low level to a high level at time t_0 , as shown in **FIG. 2(b)**.

Shortly after time t_0 , at time t_1 , the linear regulator 14 is switched on and the power supply starts up. The battery voltage V_{bat} is fully available.

Immediately on start-up at time t_1 , the maximum available voltage at the output is V_1 as shown in **FIG. 2(d)**. V_1 is the battery voltage for the purposes of illustration in the figure.

From time t_1 the capacitor 12 then charges up as shown in **FIG. 2(c)**. As the capacitor 12 charges up the maximum available voltage at the output increases from V_1 . Thus as shown in **FIG. 2(d)**, as the capacitor voltage V_{cap} increases from time t_1 , there is a corresponding increase in the available voltage at the output.

At time t_2 the capacitor is fully charged at a voltage level V_C . The maximum available voltage at the output is V_2 , where $V_2 > V_1$, as shown in **FIG. 2(d)**. The maximum available output voltage is thus the battery voltage plus the capacitor voltage: $V_1 + V_C$.

FIG. 2(c) shows the voltage across the capacitor increasing from zero volts to V_C between times t_1 and t_2 .

As shown in **FIG. 2(a)**, between times t_1 and t_2 the output voltage comprises only the preamble signal, which has no large voltages present, and the voltage V_1 is sufficient to amplify the low amplitudes within this signal, which is sufficient to amplify the amplitudes in the payload following the preamble.

5 After time t_2 , the capacitor remains charged up while the power supply stage is operational, with the maximum available output voltage during this time being V_2 .

The power supply stage 100 switches from an active state to an inactive state responsive to a mode select signal switching from a high level to a low level at time t_3 , as shown in **FIG. 2(b)**.

10 At time t_4 the power supply stage 100 switches off, and the linear regulator 14 switches off, and the maximum available voltage at the output drops to V_3 as a result of the battery being switched off, where $V_3 = V_2 - V_1$.

From time t_4 the capacitor then discharges, until at time t_5 the maximum available output voltage is zero volts, with the capacitor fully discharged. The available
15 output voltage between times t_4 and t_5 is only associated with the voltage remaining in the capacitor as it is discharged. As shown in **FIG. 2(c)**, between times t_4 and t_5 the voltage across the capacitor 12 drops from V_c to zero volts. During this time, as denoted in **FIG. 2(a)**, there is no output signal and therefore the output voltage available is unimportant.

20 The ET modulator switches from an inactive to an active state responsive to a mode select signal switching from a low level to a high level at time t_6 , as shown in **FIG. 2(b)**.

The ET modulator then starts-up again at subsequent time t_7 , and the maximum available output voltage then again becomes V_1 . Again, the maximum available output
25 voltage then increases to V_2 at a time t_8 , and remains at this level whilst the ET modulator is switched on. The maximum available output voltage is thus the battery voltage plus the capacitor voltage.

Similarly between times t_7 and t_8 the voltage across the capacitor increases from zero volts to V_c as shown in **FIG. 2(c)**, and during this time period the output signal
30 comprises only a preamble as shown in **FIG. 2(a)**: the available output voltage is sufficient in this time period.

The power supply stage switches from an active state to an inactive state responsive to a mode select signal switching from a high level to a low level at time t_9 , as shown in **FIG. 2(b)**.

At a subsequent time t_{10} the power supply stage is switched off, and as before
 5 the maximum available output voltage drops immediately to V_3 . After time t_{10} the maximum available output voltage is ramped down to decrease toward zero volts, as the voltage across the capacitor is ramped down from V_c toward zero volts.

However in this instance, at a time t_{11} , before the maximum available output voltage has reduced to zero volts, the ET modulator is switched on. The power supply
 10 stage switches from an inactive to an active state responsive to a mode select signal switching from a low level to a high level at time t_{11} , as shown in **FIG. 2(b)**.

At time t_{12} , the power supply stage starts up again, but the maximum available output voltage has only reduced to a level V_4 at this time, and not reached zero volts, as the voltage across the capacitor has decreased to a level V_{c1} , not zero volts.

At time t_{12} , the maximum available output voltage immediately becomes V_5 ,
 15 where $V_5 = V_4 + V_1$. After time t_{12} the maximum available output voltage then increases, until at time t_{13} it reaches V_2 .

The time elapsed between t_{12} and t_{13} will be less than the time elapsed between t_1 and t_2 (or t_7 and t_8) because the maximum available output voltage is ramping up from
 20 V_4 rather than zero volts in this instance.

Between time instances t_{12} and t_{13} , the voltage across the capacitor ramps up from V_{c1} to V_c as shown in **FIG. 2(c)**, and as shown in **FIG. 2(a)** only a preamble is provided at the output voltage.

Thus it can be seen that there is a provided a technique during power-up where
 25 the increases of the voltage across the capacitor is controlled, in order to control the current drawn by the capacitor, such that the full voltage due to the capacitor is not available during power-up. During this power-up phase the signal for which the power supply is needed does not need the full power supply range. After power-up the full voltage associated with the capacitor is available, and the power supply delivered can be
 30 adjusted accordingly to a level in order to deal with large amplitude signals.

FIG. 3 illustrates an exemplary circuit utilising the soft start technique principle illustrated with respect to **FIGS. 2(a) to 2(d)**. Where elements correspond to elements of **FIG. 1**, like reference numerals are used.

The circuit of **FIG. 1** as shown in **FIG. 3** is modified to additionally include a digital-to-analogue converter (DAC) 50 and an amplifier 52. The DAC 50 provides a first input for the amplifier 52 on a line 51, and the second input of the amplifier 52 is provided by the reference signal on line 32. The amplifier 52 then generates one input to the linear correction amplifier 14, rather than this input being provided directly by the reference signal on line 32 as in **FIG. 1**. The other input to the amplifier 14 is fed back from its output as in **FIG. 1**.

A signal of the same shape as **FIG. 2(c)** is applied by the DAC 50 to the amplifier 52 on line 51. The signal from the DAC 50 to the amplifier 52 on line 51 is thus controlled to ramp up consistent with the ramp of the signal in **FIG. 2(c)** between times t_1 and t_2 . Thus between times t_1 and t_2 the DAC applies a ramp from level 0V to V_C (the capacitor voltage) to the amplifier 52. The amplifier 52 adds this to the reference signal on line 32, and the output of the amplifier provided to the linear amplifier 14 thus has the increasing ramp applied to it. The output of the amplifier 14 thus ramps up in accordance with the ramp shape of **FIG. 2(c)**.

The output of the amplifier 52 follows the reference signal but in a ramped fashion. The ramped signal is provided to the linear amplifier 14.

The voltage V_{ea} thus ramps up, and the voltage across the capacitor 12 ramps up from 0V to V_C .

The mode select signal is provided as a control signal on line 54 to the DAC 50. Thus the signal of **FIG. 2(b)** is applied to the DAC 50 on line 54.

As in **FIG. 1**, the switching stage 22 receives an input, at a second input to the buck amplifier 16, from the second terminal of the capacitor 12. The buck amplifier 16 thus controls the switches 20a, 20b in dependence on a difference between the reference signal on line 32 and the feedback signal from the capacitor on line 36.

The DAC converter 50 provides an input to the linear amplifier 14 of the correction stage 24 via the amplifier 52. The DAC is controlled to generate a ramp signal such that the output of the correction amplifier 14 ramps up during start up.

The switching stage 22 determines the minimum value of the envelope $V_{\min}$, based on an analysis of the envelope signal on line 32. The buck amplifier 16 then subtracts the voltage V_{ea} , which is the minimum voltage the linear path can provide, from this envelope minimum. The voltage V_{ea} is the linear path envelope offset value,
 5 which is applied to the linear path.

The net effect is that the envelope appears at the voltage supply stage output, and internal circuits use knowledge of the envelope minimum value to optimise their operating points.

The arrangement of **FIG. 3** assumes unity gain throughout, and no gain or offset
 10 adjustment.

Another example implementation is shown in **FIG. 4**. Elements in **FIG. 4** that correspond to elements in previous figures are identified by the same reference numerals.

The arrangement of **FIG. 4** includes the switching stage 22 including the
 15 switching amplifier 16, and switches 20a, 20b. Also included in the arrangement of **FIG. 4** is the correction stage 24 including the linear amplifier 14. The combiner 26 is provided, including the inductor 18 and the capacitor 12, respectively having their first terminals connected to the outputs of the switching stage 22 and the correction stage 24, and generating the output voltage V_{out} on line 34.

20 A capacitor voltage demand control signal V_{CAP_DEM} is provided on a signal line 81. A buck path gain/offset trim amplifier 68 and a linear path gain/offset trim amplifier 70 each receive the signal on line 81 as an input. A buck path DAC 64 and a linear path DAC 66 each respectively receive the outputs of the amplifiers 68 and 70.

A baseband envelope DAC 72 receives the envelope signal on line 32.

25 The buck amplifier 16 receives as an inverting input the output of the DAC 64. The non-inverting input of the buck amplifier 16 is received from an output of an amplifier 74. The amplifier 74 has inputs connected to the first and second terminals of the capacitor 74, and thus generates an output to the buck amplifier which is based on the voltage across the capacitor 12.

The linear amplifier 14 receives as an inverting input the output of the DAC 66. The non-inverting input of the linear amplifier 14 is provided by the output of the DAC 72.

The DAC 64 sets the voltage across the capacitor 12. The DAC 66 sets the linear
5 path offset voltage consistent with the DAC 50 in **FIG. 3**.

It is important the gain (i.e. step-size) in the two signals from the DACs 64 and 66 is accurately matched. The same operation is applied to both DACs at the same time without multiplication. This is an aspect that makes implementation easier, with variable gain step.

10 The two ramp-ups from the DACs 64 and 66 need to be the same so there is no error, then the ramp rate controls how much current the capacitor 12 consumes. The ramp is dictated by knowing what current is allowed.

As shown in FIG. 4, each DAC 64, 66 and 72 receives the control signal 54 of FIG. 3.

15 The ramp-up is acceptable and does not affect operation of the circuit, because a pre-amble signal is being transmitted in this period, and this preamble signal does not need a large voltage.

The invention has been described by way of example with reference to particular implementations. The invention is not limited to the details of any such implementation.
20 The invention may utilise different aspects of different described implementation in isolation or in combination.

CLAIMS:

1. An envelope tracking modulator, comprising a switching amplifier, a correction amplifier, and a combiner for combining the outputs of the switching amplifier and the correction amplifier, to generate as an output an envelope tracked supply voltage tracking a reference signal, further including a boost capacitor for boosting the voltage available at the output, wherein during a start-up phase the increase in voltage across the capacitor is controlled.
2. The envelope tracking modulator of claim 1 wherein after the start-up phase, the voltage across the capacitor is fully established.
3. The envelope tracking modulator of claim 1 further comprising a ramp generator which generates a ramp signal which extends from zero volts to a desired capacitor voltage over a period of time which corresponds to the start-up phase, wherein the ramp generator is used to attenuate the voltage generated across the capacitor in the start-up phase.
4. The envelope tracking modulator of claim 3 wherein the switching amplifier and the correction amplifier both receive an envelope of an input signal to be amplified, and wherein the ramp generator controls the application of the envelope signal to the correction amplifier.
5. The envelope tracking modulator of claim 4 wherein the switching stage receives a signal indicative of the voltage of the output.
6. The envelope modulator of claim 5 wherein the switching amplifier controls a switching stage in dependence on a difference between the reference signal and the signal indicative of the voltage at the output.
7. The envelop tracking modulator of claim 3 wherein the switching amplifier and the correction amplifier each receive a signal indicative of the voltage to be established across the capacitor and the correction amplifier receives an envelope of an input signal to be amplified, wherein the ramp generator controls the application of the signal

indicative of the voltage to be established across the capacitor and the envelope signal to the switching and correction stages.

8. The envelope tracking stage of claim 7 wherein the switching stage receives a
5 signal indicative of the voltage across the capacitor.

9. A method in an envelope tracking modulator, comprising a switching amplifier,
a correction amplifier, and a combiner for combining the outputs of the switching
amplifier and the correction amplifier, to generate as an output an envelope tracked
10 supply voltage tracking a reference signal, the method comprising boosting the voltage
available at the output, and controlling the increase in voltage across the capacitor
during a start-up phase.

10. The method of claim 9 wherein after the start-up phase, the voltage across the
15 capacitor is fully established.

11. The method of claim 8 or claim 9 further comprising a ramp generator the
method further including generating a ramp signal which extends from zero volts to a
desired capacitor voltage over a period of time which corresponds to the start-up phase,
20 to attenuate the voltage generated across the capacitor in the start-up phase.

12. The method of claim 11 comprising receiving an envelope of an input signal to
be amplified at the switching amplifier and the correction amplifier, and controlling the
application of the envelope signal to the correction amplifier using the ramp signal.
25

13. The method of claim 12 further comprising receiving a signal indicative of the
voltage of the output at switching stage.

14. The method of claim 13 wherein further comprising controlling a switching
30 stage in dependence on a difference between the reference signal and the signal
indicative of the voltage at the output.

15. The method of claim 11 wherein the switching amplifier and the correction
amplifier each receive a signal indicative of the voltage to be established across the

capacitor and the correction amplifier receives an envelope of an input signal to be amplified, wherein there is controlled the application of the signal indicative of the voltage to be established across the capacitor and the envelope signal to the switching and correction stages.

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16. The method of claim 15 wherein the switching stage receives a signal indicative of the voltage across the capacitor.

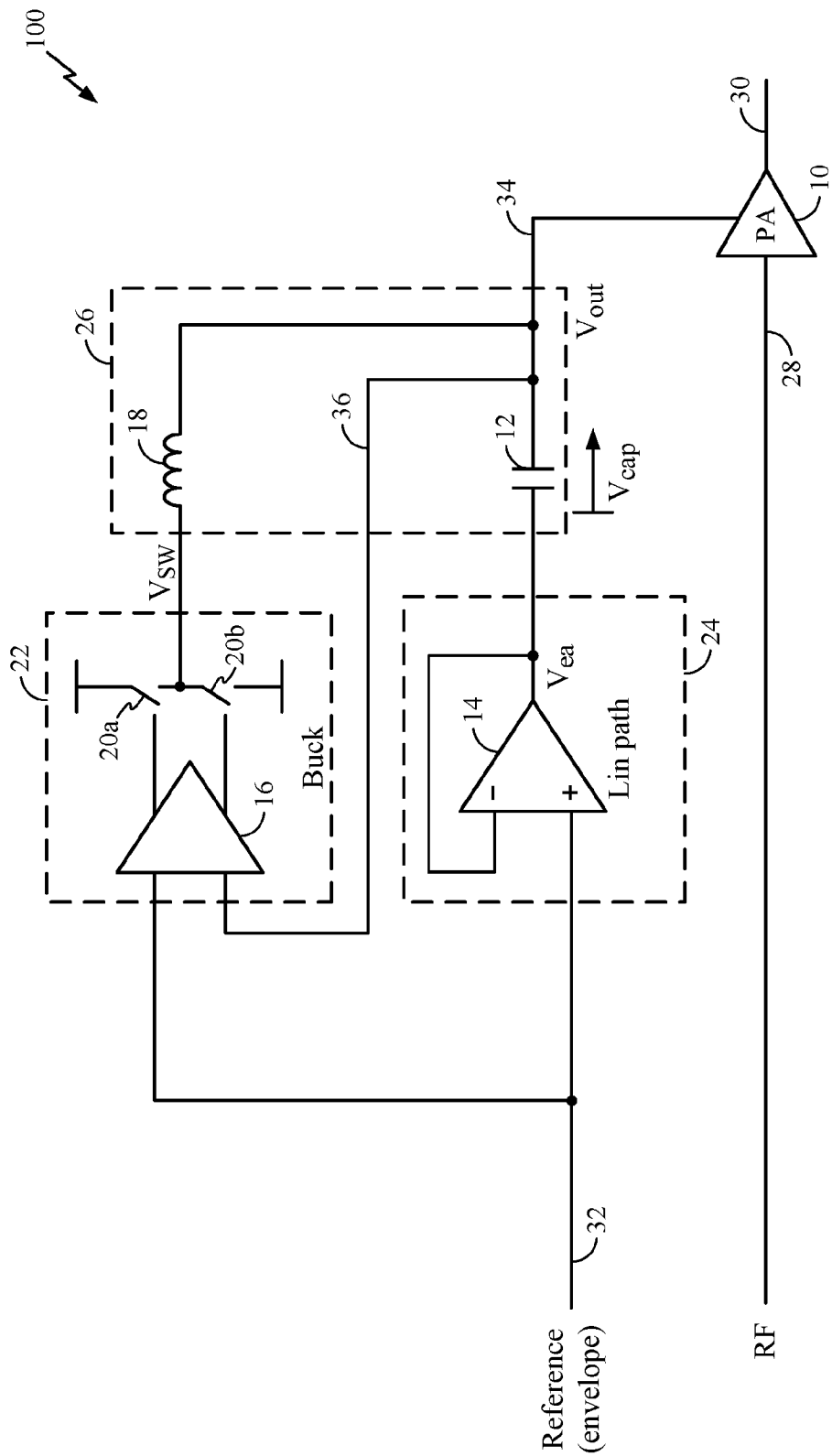
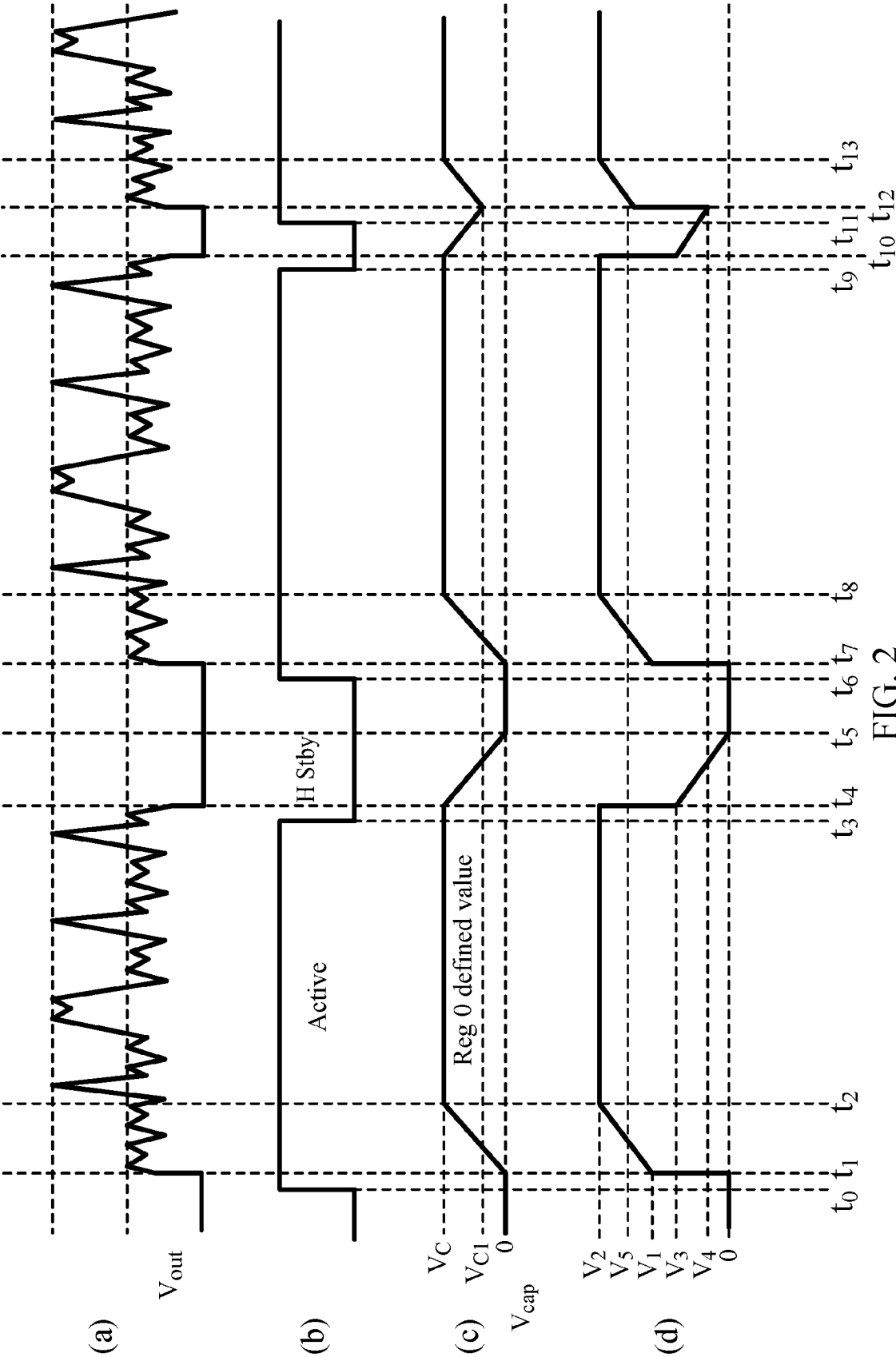


FIG. 1



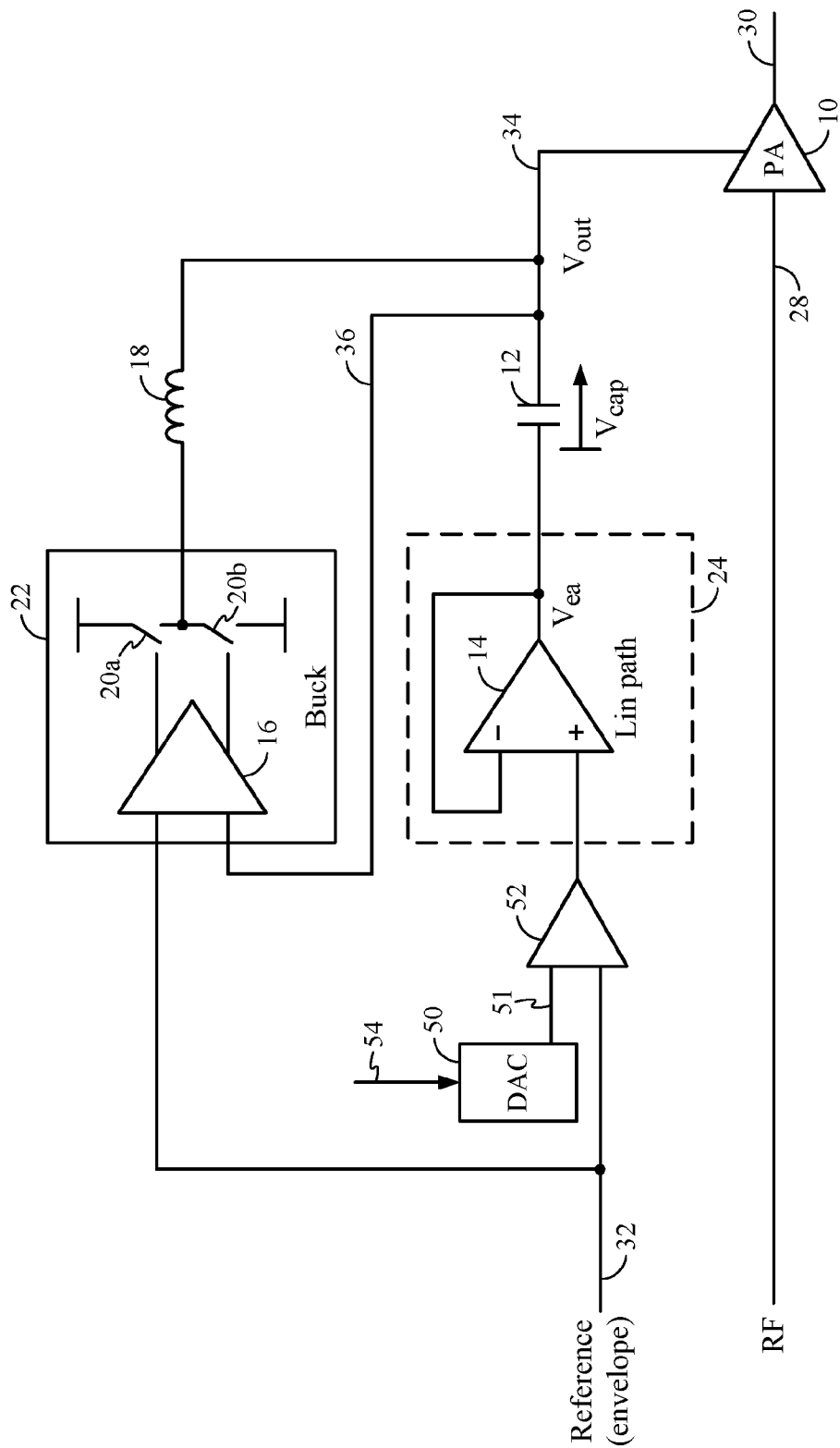


FIG. 3

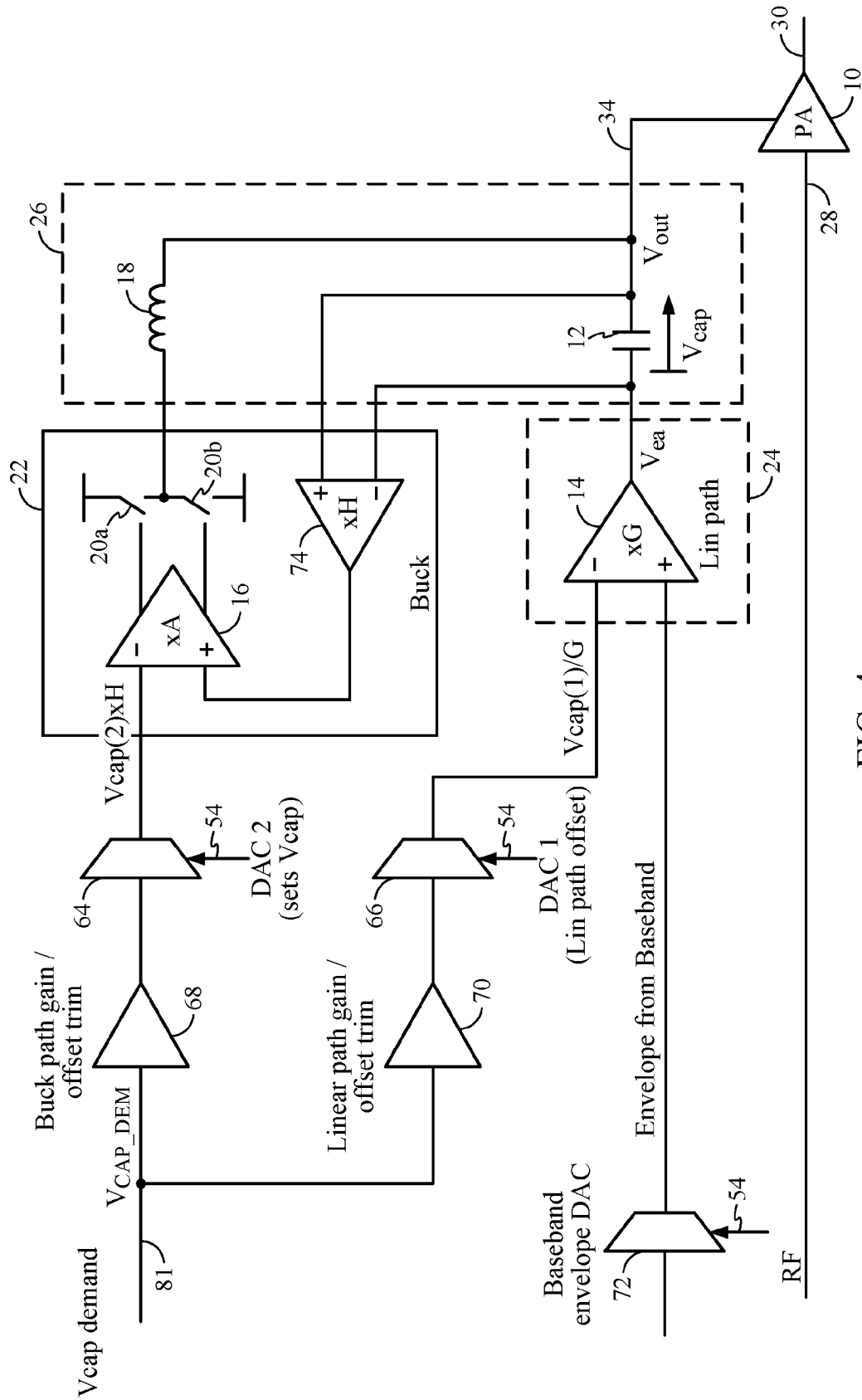


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2016/031989

A. CLASSIFICATION OF SUBJECT MATTER

INV. H03F1/02 H03F3/217
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/194274 A1 (FOWERS PAUL [GB] ET AL) 2 August 2012 (2012-08-02)	1,9
Y	abstract; figure 5	2-8, 10-16
Y	----- US 2013/249505 A1 (BROWN JAMES E C [US] ET AL) 26 September 2013 (2013-09-26) paragraph [0036]; figure 2	2-8, 10-16
A	----- GB 2 345 212 A (MOTOROLA INC [US]) 28 June 2000 (2000-06-28) page 12, lines 14-24; figures 3,11	1-16

☐

Further documents are listed in the continuation of Box C.

☒

See patent family annex.

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Date of the actual completion of the international search

11 July 2016

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012194274 A1	02-08-2012	CN 102629854 A	08-08-2012
		CN 105281688 A	27-01-2016
		EP 2671320 A1	11-12-2013
		JP 5469257 B2	16-04-2014
		JP 2013511242 A	28-03-2013
		TW 201234771 A	16-08-2012
		US 2012194274 A1	02-08-2012
		WO 2012104038 A1	09-08-2012

US 2013249505 A1	26-09-2013	EP 2992599 A1	09-03-2016
		KR 20160003202 A	08-01-2016
		US 2013249505 A1	26-09-2013
		WO 2014178976 A1	06-11-2014

GB 2345212 A	28-06-2000	NONE	
