(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
06 October 2022 (06.10.2022)

WIPO | PCT

(10) International Publication Number
WO 2022/212596 A1

(51) International Patent Classification:
H01L 23/00 (2006.01)

(21) International Application Number:
PCT/US2022/022677

(22) International Filing Date:
30 March 2022 (30.03.2022)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/168,988 31 March 2021 (31.03.2021) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: DIRECT BONDING METHODS AND STRUCTURES

(57) Abstract: Disclosed herein are methods for direct bonding. In some embodiments, a direct bonding method comprises preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element; and after the preparing, providing a protective layer over the prepared first bonding surface of the first element, the protective layer having a thickness less than 3 microns.

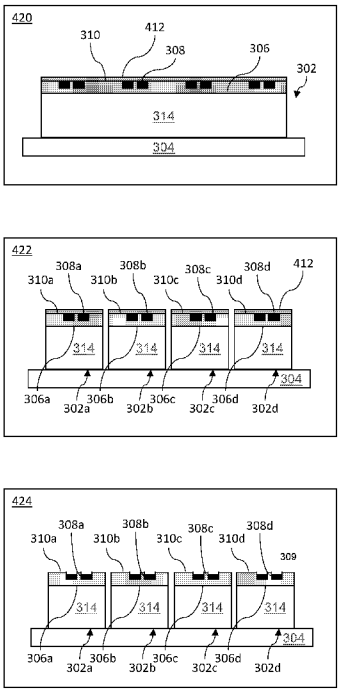


FIG. 4

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[Continued on next page]

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

DIRECT BONDING METHODS AND STRUCTURES

INCORPORATION BY REFERENCE TO ANY PRIORITY APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 63/168988, entitled "DIRECT BONDING METHODS AND STRUCTURES," filed on March 31, 2021, the entirety of which is hereby incorporated by reference herein.

BACKGROUND

Field

[0002] The field relates to direct bonding methods and structures.

Description of the Related Art

[0003] Semiconductor elements, such as semiconductor wafers or integrated device dies, can be stacked and directly bonded to one another without an adhesive. For example, in some hybrid direct bonded structures, non-conductive field regions of the elements can be directly bonded to one another, and corresponding conductive contact structures can be directly bonded to one another. In some applications, it can be challenging to protect the contact pads before bonding. Accordingly, there remains a continuing need for improved contact structures for direct bonding.

SUMMARY

[0004] In one embodiment, a bonding method can include: preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element; and after the preparing, providing a protective layer over the prepared first bonding surface of the first element, the protective layer having a thickness less than 3 microns.

[0005] In some embodiments, preparing the first bonding surface comprises activating the first bonding surface. In some embodiments, activating the first bonding surface comprises plasma activating the first bonding surface. In some embodiments, plasma activating the first bonding surface comprises exposing the first bonding surface to a nitrogen-containing plasma. In some embodiments, the thickness of the protective layer is less than 2 microns. In some embodiments, the thickness of the protective layer is less than 0.25 microns. In some embodiments, the thickness of the protective layer is in a range of 0.05 microns to 2 microns. In some embodiments, the thickness of the protective layer is in a range of 0.1 microns to 0.25 microns. In some embodiments, the protective layer comprises an organic

layer. In some embodiments, the protective layer comprises a hydrophobic coating and/or a hydrophilic coating. In some embodiments, the protective layer comprises a photoresist. In some embodiments, providing the protective layer comprises blanket depositing the protective layer over the first bonding surface. In some embodiments, the bonding method includes removing the blanket deposited protective layer using a reactive ion etching (RIE) process. In some embodiments, the bonding method includes, before the removing, cleaning particles from the first element. In some embodiments, the bonding method includes, before providing the protective layer, selectively providing a passivation layer over a plurality of contact pads, and wherein providing the protective layer comprises providing the protective layer over the passivation layer. In some embodiments, providing the protective layer comprises selectively providing the protective layer over conductive contact pads of the first bonding surface. In some embodiments, the first bonding surface includes a plurality of contact pads, the contact pads protruding above a first non-conductive region of the first bonding surface, wherein providing the protective layer comprises providing the protective layer over at least the protruding contact pads. In some embodiments, providing the protective layer comprises blanket depositing the protective layer over the first bonding surface. In some embodiments, the bonding method includes planarizing the first element such that the plurality of contact pads are flush with or recessed below the first non-conductive region. In some embodiments, the first bonding surface includes a first plurality of conductive contact pads and a first non-conductive bonding region, the first plurality of conductive contact pads recessed below the first non-conductive bonding region. In some embodiments, the first plurality of conductive contact pads are recessed below the first non-conductive bonding region by no more than 10 nm. In some embodiments, a variation in recess depth of the first plurality of contact pads across the first element is less than 25%. In some embodiments, the variation in recess depth of the first plurality of contact pads across the first element is less than 10%. In some embodiments, the variation in recess depth of the first plurality of contact pads across the first element is less than 5%. In some embodiments, the bonding method includes comprising removing the protective layer. In some embodiments, the first element comprises a wafer, the method further comprising, before removing the protective layer, singulating the wafer to form a plurality of singulated elements. In some embodiments, the bonding method includes, after removing the protective layer, directly bonding the first bonding surface of the first element to

the second bonding surface of the second element without an intervening adhesive. In some embodiments, the first bonding surface comprises a first plurality of conductive contact pads and a first non-conductive bonding region, wherein the second bonding surface comprises a second plurality of conductive contact pads and a second non-conductive bonding region, and wherein directly bonding comprise hybrid direct bonding, including directly bonding the first and second pluralities of conductive contact pads to one another without an adhesive and directly bonding the first and second non-conductive bonding regions to one another without an adhesive. In some embodiments, the first non-conductive bonding region comprises a silicon-containing dielectric layer. In some embodiments, the bonding method includes activating the second bonding surface before directly bonding. In some embodiments, preparing the first bonding surface and providing the protective layer are performed in a first facility, and wherein directly bonding is performed at a second facility that is in a different location from the first facility. In some embodiments, directly bonding is performed more than twenty-four (24) hours after activating the first bonding layer.

[0006] In another embodiment, a bonding method includes: preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element; after the preparing, selectively providing a passivation layer over a plurality of contact pads of the first bonding surface; and after providing the passivation layer, providing the protective layer over the passivation layer.

[0007] In some embodiments, providing the protective layer comprises blanket depositing the protective layer over the first bonding surface. In some embodiments, the protective layer has a thickness less than 3 microns. In some embodiments, the thickness of the protective layer is less than 2 microns. In some embodiments, the thickness of the protective layer is less than 0.25 microns. In some embodiments, the thickness of the protective layer is in a range of 0.05 microns to 2 microns. In some embodiments, the thickness of the protective layer is in a range of 0.1 microns to 0.25 microns. In some embodiments, the protective layer comprises an organic layer. In some embodiments, the protective layer comprises a hydrophobic coating and/or a hydrophilic coating. In some embodiments, the method can include removing the protective layer. In some embodiments, the first element comprises a wafer, the method further comprising, before removing the protective layer, singulating the wafer to form a plurality of singulated elements. In some embodiments, the

method can include, after removing the protective layer, directly bonding the first bonding surface of the first element to the second bonding surface of the second element without an intervening adhesive. In some embodiments, the first plurality of conductive contact pads are recessed below a first non-conductive bonding region of the first bonding surface. In some embodiments, the first plurality of conductive contact pads are recessed below the first non-conductive bonding region by no more than 10 nm. In some embodiments, a variation in recess depth of the first plurality of contact pads is less than 25%. In some embodiments, the variation in recess depth of the first plurality of contact pads is less than 10%, for example, less than 5%.

[0008] In another embodiment, a bonding method can include: preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element; and after the preparing, selectively providing a protective layer over a plurality of contact pads of the first bonding surface.

[0009] In some embodiments, the first bonding surface further includes a first non-conductive material, wherein no protective layer is provided over an entirety of the first non-conductive material. In some embodiments, the protective layer has a thickness less than 3 microns. In some embodiments, the thickness of the protective layer is less than 2 microns. In some embodiments, the thickness of the protective layer is less than 0.25 microns. In some embodiments, the thickness of the protective layer is in a range of 0.05 microns to 2 microns. In some embodiments, the thickness of the protective layer is in a range of 0.1 microns to 0.25 microns. In some embodiments, the protective layer comprises an organic layer. In some embodiments, the protective layer comprises a hydrophobic coating and/or a hydrophilic coating. In some embodiments, the method can include providing a passivation layer comprising oxidizing surfaces of the contact pads. In some embodiments, the method can include removing the protective layer. In some embodiments, the first element comprises a wafer, the method further comprising, before removing the protective layer, singulating the wafer to form a plurality of singulated elements. In some embodiments, the method can include, after removing the protective layer, directly bonding the first bonding surface of the first element to the second bonding surface of the second element without an intervening adhesive.

[0010] In another embodiment, a bonding method can include: preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second

element, the first bonding surface including a first non-conductive region and a first plurality of contact pads protruding above the first non-conductive region; and after the preparing, providing a protective layer over at least the first plurality of contact pads.

[0011] In some embodiments, providing the protective layer comprises blanket depositing the protective layer over the first bonding surface. In some embodiments, the method can include planarizing the first element such that the first plurality of contact pads are recessed below the first non-conductive region. In some embodiments, the method can include removing the protective material.

[0012] In another embodiment, a bonding method can include: preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element; and after the preparing, selectively providing a passivation layer over a plurality of contact pads of the first bonding surface.

[0013] In some embodiments, providing the passivation layer comprising oxidizing surfaces of the contact pads. In some embodiments, the method can include singulating the first element with the passivation layer over the plurality of contact pads, wherein the passivation layer is exposed at an upper surface of the element during the singulating.

[0014] In some embodiments, a semiconductor element comprises: a device region; a bonding layer over the device region, the bonding layer having a bonding surface prepared for direct hybrid bonding to a second element; and a protective layer over at least a portion of the prepared first bonding surface, the protective layer having a thickness less than 3 microns. In some embodiments, the protective layer comprises a photoresist. In some embodiments, the semiconductor element is in wafer form. In some embodiments, the thickness of the protective layer is in a range of 0.05 microns to 2 microns. In some embodiments, the bonding layer comprises a plurality of conductive contact pads and a non-conductive bonding region. In some embodiments, the semiconductor element further comprises a passivation layer over the plurality of conductive contact pads between the plurality of contact pads and the protective layer. In some embodiments, the protective layer is selectively provided over the plurality of conductive contact pads. In some embodiments, the plurality of conductive contact pads protrudes above the bonding layer. In some embodiments, the plurality of conductive contact pads is recessed below an upper surface of the bonding layer. In some embodiments, the protective layer is blanket deposited over the bonding surface.

[0015] In some embodiments, a semiconductor element comprises: a device region; a bonding layer over the device region, the bonding layer having a bonding surface prepared for direct hybrid bonding to a second element and including a plurality of conductive contact pads and a non-conductive bonding region, the plurality of conductive contact pads each having a recess depth by which the conductive contact pads are recessed below the bonding surface, wherein a variation in recess depth of the plurality of contact pads is less than 25%. In some embodiments, the variation in recess depth of the plurality of conductive contact pads is less than 10%. In some embodiments, the variation in recess depth of the plurality of conductive contact pads is in a range of 0.5% to 10%, or in a range of 0.1% to 5%.

[0016] In some embodiments, a semiconductor element comprises: a device region; a bonding layer over the device region, the bonding layer having a bonding surface prepared for direct hybrid bonding; and a conductive layer exposed at a portion of the prepared bonding surface, the conductive layer having a recess variation less than 5 nm within the bonding surface of the device. In some embodiments, the recess variation is less than 3 nm within the bonding surface of the device. In some embodiments, the recess variation is less than 2 nm within the bonding surface of the device. In some embodiments, the recess variation is less than 1 nm within the bonding surface of the device. In some embodiments, the recess variation is between 0.5 nm and 5 nm within the bonding surface of the device. In some embodiments, the conductive layer includes a plurality of conductive contact pads, the plurality of conductive contact pads each having a recess depth by which they are recessed below the bonding surface. In some embodiments, the bonding layer includes a non-conductive layer in which the conductive layer is at least partially embedded. In some embodiments, the non-conductive layer is polished.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] These and other features, aspects, and advantages of the disclosure are described with reference to drawings of certain embodiments, which are intended to illustrate, but not to limit, the present disclosure. It will be understood that the accompanying drawings, which are incorporated in and constitute a part of this specification, are for the purpose of illustrating concepts disclosed herein and may not be to scale.

[0018] FIGS. 1a-1b schematically illustrate a direct bonding process according to some embodiments.

[0019] FIG. 2 is a diagram plotting maximum recess distances from a bonding plane versus temperature, for different thicknesses of a thermally expanding metal contact.

[0020] FIG. 3 is a diagram showing an example process for protecting a surface of a semiconductor element during processing according to some embodiments.

[0021] FIG. 4 is a diagram showing an example process for protecting a surface of a semiconductor element during processing according to some embodiments.

[0022] FIG. 5 is a diagram showing an example process for protecting a surface of a semiconductor element during processing according to some embodiments.

[0023] FIG. 6 is a diagram showing an example process for protecting a surface of a semiconductor element during processing according to some embodiments.

[0024] FIG. 7 is a diagram showing an example process for protecting a surface of a semiconductor element during processing according to some embodiments.

DETAILED DESCRIPTION

[0025] Various embodiments disclosed herein relate to directly bonded structures in which two elements can be directly bonded to one another without an intervening adhesive. FIGS. 1a and 1b schematically illustrate a process for forming a directly bonded structure without intervening adhesive according to some embodiments. In FIGS. 1a and 1b, a directly bonded structure 100 comprises two elements 102 and 104 that can be directly bonded to one another without an intervening adhesive. Two or more semiconductor elements (such as integrated device dies, wafers, etc.) 102 and 104 may be stacked on or bonded to one another to form a bonded structure 100. Conductive contact pads 106a of a first element 102 may be electrically connected to corresponding conductive contact pads 106b of a second element 104. Any suitable number of elements can be stacked in the bonded structure 100. For example, a third element (not shown) can be stacked on the second element 104, a fourth element (not shown) can be stacked on the third element, and so forth. Additionally or alternatively, one or more additional elements (not shown) can be stacked laterally adjacent one another along the first element 102. In some embodiments, the laterally stacked additional element may be smaller than the second element. In some embodiments, the laterally stacked additional element may be two times smaller than the second element.

[0026] In some embodiments, the elements 102 and 104 are directly bonded to one another without an adhesive. In various embodiments, a non-conductive or dielectric material can serve as a first bonding layer 108a of the first element 102 which can be directly bonded to a corresponding non-conductive or dielectric field region serving as a second bonding layer 108b of the second element 104 without an adhesive. The non-conductive bonding layers 108a and 108b can be disposed on respective front sides 114a and 114b of device portions 110a and 110b, such as a semiconductor (*e.g.*, silicon) portion of the elements 2, 3. Active devices and/or circuitry can be patterned and/or otherwise disposed in or on the device portions 110a and 110b. Active devices and/or circuitry can be disposed at or near the front sides 114a and 114b of the device portions 110a and 110b, and/or at or near opposite backsides 116a and 116b of the device portions 110a and 110b. The non-conductive material can be referred to as a non-conductive bonding region or bonding layer 108a of the first element 102. In some embodiments, the non-conductive bonding layer 108a of the first element 102 can be directly bonded to the corresponding non-conductive bonding layer 108b of the second element 104 using dielectric-to-dielectric bonding techniques. For example, non-conductive or dielectric-to-dielectric bonds may be formed without an adhesive using the direct bonding techniques disclosed at least in U.S. Patent Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes. It should be appreciated that in various embodiments, the bonding layers 108a and/or 108b can comprise a non-conductive material such as a dielectric material, such as silicon oxide, or an undoped semiconductor material, such as undoped silicon.

[0027] In various embodiments, direct hybrid bonds can be formed without an intervening adhesive. For example, dielectric bonding surfaces 112a and 112b can be polished to a high degree of smoothness. The bonding surfaces 112a and 112b can be cleaned and exposed to a plasma and/or etchants to activate the surfaces 112a and 112b. In some embodiments, the surfaces 112a and 112b can be terminated with a species after activation or during activation (*e.g.*, during the plasma and/or etch processes). Without being limited by theory, in some embodiments, the activation process can be performed to break chemical bonds at the bonding surface 112a and 112b, and the termination process can provide additional chemical species at the bonding surface 112a and 112b that improves the bonding energy during direct bonding. In some embodiments, the activation and termination are provided in

the same step, *e.g.*, a plasma to activate and terminate the surfaces 112a and 112b. In other embodiments, the bonding surface 112a and 112b can be terminated in a separate treatment to provide the additional species for direct bonding. In various embodiments, the terminating species can comprise nitrogen. Further, in some embodiments, the bonding surfaces 112a and 112b can be exposed to fluorine. For example, there may be one or multiple fluorine peaks near layer and/or bonding interface 118. Thus, in the directly bonded structure 100, the bonding interface 118 between two non-conductive materials (*e.g.*, the bonding layers 108a and 108b) can comprise a very smooth interface with higher nitrogen content and/or fluorine peaks at the bonding interface 118. Additional examples of activation and/or termination treatments may be found throughout U.S. Patent Nos. 9,564,414; 9,391,143; and 10,434,749, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

[0028] In various embodiments, conductive contact pads 106a of the first element 102 can also be directly bonded to corresponding conductive contact pads 106b of the second element 104. For example, a hybrid bonding technique can be used to provide conductor-to-conductor direct bonds along the bond interface 118 that includes covalently direct bonded non-conductive-to-non-conductive (*e.g.*, dielectric-to-dielectric) surfaces, prepared as described above. In various embodiments, the conductor-to-conductor (*e.g.*, contact pad 106a to contact pad 106b) direct bonds and the dielectric-to-dielectric hybrid bonds can be formed using the direct bonding techniques disclosed at least in U.S. Patent Nos. 9,716,033 and 9,852,988, the entire contents of each of which are incorporated by reference herein in their entirety and for all purposes.

[0029] For example, non-conductive (*e.g.*, dielectric) bonding surfaces 112a, 112b can be prepared and directly bonded to one another without an intervening adhesive as explained above. Conductive contact pads 106a and 106b (which may be surrounded by non-conductive dielectric field regions within the bonding layers 108a, 108b) may also directly bond to one another without an intervening adhesive. In some embodiments, the respective contact pads 106a and 106b can be recessed below exterior (*e.g.*, upper) surfaces 112a and 112b of the dielectric field or non-conductive bonding layers 108a and 108b, for example, recessed by less than 30 nm, less than 20 nm, less than 15 nm, or less than 10 nm, for example, recessed in a range of 2 nm to 20 nm, or in a range of 4 nm to 10 nm. In various embodiments,

prior to direct bonding, the recesses in the opposing elements can be sized such that the total gap between opposing contact pads is less than 15 nm, or less than 10 nm. The non-conductive bonding layers 108a and 108b can be directly bonded to one another without an adhesive at room temperature in some embodiments and, subsequently, the bonded structure 100 can be annealed. Upon annealing, the contact pads 106a and 106b can expand and contact one another to form a metal-to-metal direct bond. Beneficially, the use of Direct Bond Interconnect, or DBI®, techniques commercially available from Xperi of San Jose, CA, can enable high density of pads 106a and 106b to be connected across the direct bond interface 118 (e.g., small or fine pitches for regular arrays). In some embodiments, the pitch of the bonding pads 106a and 106b, or conductive traces embedded in the bonding surface of one of the bonded elements, may be less than 40 microns or less than 10 microns or even less than 2 microns. For some applications, the ratio of the pitch of the bonding pads 106a and 106b to one of the dimensions (*e.g.*, a diameter) of the bonding pad is less than 5, or less than 3 and sometimes desirably less than 2. In other applications, the width of the conductive traces embedded in the bonding surface of one of the bonded elements may range between 0.3 to 20 microns, *e.g.*, in a range of 0.3 to 3 microns. In various embodiments, the contact pads 106a and 106b and/or traces can comprise copper, although other metals may be suitable.

[0030] Thus, in direct bonding processes, a first element 102 can be directly bonded to a second element 104 without an intervening adhesive. In some arrangements, the first element 102 can comprise a singulated element, such as a singulated integrated device die. In other arrangements, as shown in FIGS. 1a-1b, the first element 102 can comprise a carrier or substrate (*e.g.*, a wafer) that includes a plurality (*e.g.*, tens, hundreds, or more) of device regions that, when singulated, form a plurality of integrated device dies. Similarly, the second element 104 can comprise a singulated element, such as a singulated integrated device die, as shown in FIGS. 1a-1a. In other arrangements, the second element 104 can comprise a carrier or substrate (*e.g.*, a wafer). The embodiments disclosed herein can accordingly apply to wafer-to-wafer, die-to-die, or die-to-wafer bonding processes.

[0031] As explained herein, the first and second elements 102 and 104 can be directly bonded to one another without an adhesive, which is different from a deposition process. In one application, a width of the first element 102 in the bonded structure is similar to a width of the second element 104. In some other embodiments, a width of the first element

102 in the bonded structure 100 is different from a width of the second element 104. Similarly, the width or area of the larger element in the bonded structure may be at least 10% larger than the width or area of the smaller element. The first and second elements 102 and 104 can accordingly comprise non-deposited elements. Further, directly bonded structures 100, unlike deposited layers, can include a defect region along the bond interface 118 in which nanometer-scale voids (nanovoids) are present. The nanovoids may be formed due to activation of the bonding surfaces 112a and 112b (e.g., exposure to a plasma). As explained above, the bond interface 118 can include concentration of materials from the activation and/or last chemical treatment processes. For example, in embodiments that utilize a nitrogen plasma for activation, a nitrogen peak can be formed at the bond interface 118. In embodiments that utilize an oxygen plasma for activation, an oxygen peak can be formed at the bond interface 118. In some embodiments, the bond interface 118 can comprise silicon oxynitride, silicon oxycarbonitride, or silicon carbonitride. As explained herein, the direct bond can comprise a covalent bond, which is stronger than van Der Waals bonds. The bonding layers 108a and 108b can also comprise polished surfaces that are planarized to a high degree of smoothness.

[0032] In various embodiments, the metal-to-metal bonds between the contact pads 106a and 106b can be joined such that copper grains grow into each other across the bond interface 118. In some embodiments, the copper can have grains oriented along the 111 crystal plane for improved copper diffusion across the bond interface 118. The bond interface 118 can extend substantially entirely to at least a portion of the bonded contact pads 106a and 106b, such that there is substantially no gap between the non-conductive bonding layers 108a and 108b at or near the bonded contact pads 106a and 106b. In some embodiments, a barrier layer may be provided under the contact pads 106a and 106b (*e.g.*, which may include copper). In other embodiments, however, there may be no barrier layer under the contact pads 106a and 106b, for example, as described in U.S. Patent No. 11,195,748, which is incorporated by reference herein in its entirety and for all purposes.

[0033] Beneficially, the use of the hybrid bonding techniques described herein can enable extremely fine pitch between adjacent contact pads 106a and 106b, and/or small pad sizes. For example, in various embodiments, the pitch p (i.e., the distance from edge-to-edge or center-to-center, as shown in Figure 1a) between adjacent pads 106a (or 106b) can be in a range of 0.5 microns to 50 microns, in a range of 0.75 microns to 25 microns, in a range of 1

micron to 25 microns, in a range of 1 micron to 10 microns, or in a range of 1 micron to 5 microns. Further, a major lateral dimension (*e.g.*, a pad diameter) can be small as well, *e.g.*, in a range of 0.25 microns to 30 microns, in a range of 0.25 microns to 5 microns, or in a range of 0.5 microns to 5 microns.

[0034] In various embodiments, the second element 104 can comprise a singulated device die, and the first element 102 can comprise a wafer. In other embodiments, both elements 102 and 104 can comprise a singulated device die. In such an embodiment, the second element 104 may be initially provided in wafer form or larger substrate and singulated to form the singulated first element 104. However, the singulation process and/or other processing steps may produce debris that can contaminate the planar bonding surface, which can leave voids and/or defects when two elements are bonded. Accordingly, prior to singulation, a protective layer can be provided over the bonding surface before activation and direct bonding in order to prevent debris from contaminating the bonding surface. The protective layer can comprise an organic or inorganic layer (*e.g.*, a photoresist) that is deposited onto the bonding surface (for example, by spin coating, atomic layer deposition, vapor coating, and so forth). Additional details of the protective layer may be found throughout U.S. Patent No. 10,714,449, the entire contents of which are incorporated by reference herein in their entirety and for all purposes. The wafer containing the first element can be singulated using any suitable method. The protective layer over the bonding surface can beneficially protect the bonding surface from debris. Before direct bonding, the protective layer can be removed from the bonding surface with a cleaning agent, for example with a suitable solvent, such as an alkaline solution or other suitable cleaning agent as recommended by the supplier of the protective layer. The protective layer cleaning agent can be selected such that it does not substantially roughen the smooth bonding surface of the bonding layer and does not substantially etch or contaminate the metal of the contact pad to increase the recess of the pad metal after subsequent cleaning operations. An excessive pad recess may form a recess that is too deep, which may prevent (or reduce the strength of) pad-to-pad bonding at the appropriate annealing conditions (*e.g.*, annealing temperature and times). The cleaning agent can be applied by a fan spray of the liquid cleaning agent or other known methods. For example, the cleaned bonding surface can be ashed (*e.g.*, using an oxygen plasma) and cleaned with

deionized water (DIW). In some embodiments, the cleaned element can be activated before direct bonding.

[0035] It can be important to protect the metallic contact pads so that the pads are not excessively recessed below the non-conductive bonding region. Excessive pad recesses may be problematic for hybrid bonding device fabrication. For example, the increased pad recesses can form a large gap between opposing pads, such that the annealing temperature is raised in order to form electrical contact between the pads. The larger the recess, the higher the bonding temperature used for the opposing conductive features to contact and form an electrical connection. Various embodiments disclosed herein can form a reliable metal-to-metal direct bond interface below about 200°C, preferably below about 180°C, and even more preferably below about 150 °C. In various embodiments, a prebond metal recess can be less than 10 nm, for example, in a range of 1 to 5 nm/μm for metallic structures less than about 4 μm in width. For a through-silicon via (TSV), the prebond metal recess can be between 15 and 4100 nm, for example in a range of about 0.2 to 4 nm/μm depth, depending on the depth of the TSV and the bonding temperature. Typically, chemical mechanical polishing can result in pads with recesses of about 0.5 nm to about 100 nm. In some embodiments, after a CMP step, the pads 106a or 106b may be protruded. The height of the protruded pads 106a or 106b with respect to the bonding surface 112a or 112b may be in a range from about 0.5 nm to about 20 nm, depending on the process specifications.

[0036] Accordingly, various embodiments disclosed herein can beneficially reduce the recess depths structures that are to be hybrid direct bonded. Moreover, various embodiments can reduce within-wafer and wafer-to-wafer variability of recesses. Providing reduced and/or consistent recesses can enable the formation of very reliable metal-to-metal direct bonds at comparatively lower anneal temperatures (*e.g.*, less than 275 °C, preferably less than 200°C, more preferably below about 180°C, even more preferably below about 150 °C) for micron scale and submicron features. The thermal budget and/or cost of fabrication can also be reduced for the fabrication of direct hybrid bonded devices.

[0037] Figure 2 illustrates a chart showing anneal temperatures for copper pad recesses for pads with different thicknesses. As shown, increasing recess depth utilizes higher anneal temperatures, which increases the thermal budget for the direct bonding process. Further, degradation of the copper pads can increase the recess and, accordingly, increase the

anneal temperature for the opposing copper pads to partially or fully contact each other to form a metallurgical bond. A metallurgical bond may be formed, for example, according to the methods, structures, and apparatuses disclosed in U.S. Patent No. 11,011,494, which is incorporated by reference herein in its entirety and for all purposes.

[0038] Various embodiments disclosed herein can utilize a thin protective layer over the bonding surface to protect the bonding surface and the semiconductor element, for example, during a singulation or dicing process. FIG. 3 shows a typical process that uses a thick protective coating or layer (*e.g.*, greater than 3 microns thick). At block 320, a protective coating 312 is applied over a bonding surface 310 of a semiconductor element 302 having a non-conductive region 306 and conductive contact regions 308 which on top of a semiconductor region 314 (*e.g.*, a device portion) and affixed on a dicing tape 304. The semiconductor region 314 can comprise a device portion having active circuitry patterned therein. The protective coating 312 may be applied by spin coating for example. In some embodiments, the protective coating 312 may comprise, for example, a polymer such as a photoresist. In some embodiments, the material used for the protective coating 312 may include a solvent. To remove the solvent in the protective coating 312, the semiconductor element 302 is typically baked at 135°C for about 180s to harden the protective coating 312 (e.g., photoresist) and ensure good adhesion between the protective coating 312 and the semiconductor element 302 beneath. The protective coating 312 can be deposited over the semiconductor element 302, and at block 322, the semiconductor element 302 can be singulated to form singulated elements 302a-302d having non-conductive regions 306a-306d and conductive contact regions 308a-308d. At block 324, the protective coating 312 can be removed.

[0039] The process depicted in FIG. 3 can work well for interconnect processes that use ball grid arrays, controlled collapse chip connection (C4), and so forth, which use surfaces with relatively large topographic features (for example, a typical C4 process may use solder spheres that are several microns to tens of microns in diameter). However, when used in direct bonding processes, the cleaning fluid used to remove the protective layer 312 may unacceptably increase a recess 309 of the copper pads used in direct bonding. For example, the relatively thick coating can have longer coating removal times (for example, from about 300 seconds to about 1200 seconds) and longer exposure to the cleaning medium which can

lead to a higher degree of recess 309. Non-uniform removal of the protective coating 312 across the substrate can also cause an increase in the recess non-uniformity across the semiconductor element 302. There can also be a center to edge variation in the cleaned substrate, as well as greater wafer to wafer variation. In some processes, for example direct bonding, it is important that the recess of all the pads in a die be substantially uniform. For example, various embodiments disclosed herein (*e.g.*, embodiments of FIGS. 4-7) can beneficially ensure that the recess variation among the pads of the die is less than 25%, less than 10%, less than 5%, less than 2%, or less than 1%, or less than about 0.5%. In various embodiments, the recess variation among the pads of the due can be in a range of 0.1% to 10%, in a range of 0.1% to 5%, or in a range of 0.5% to 5%. The recess variation can be less than 5 nm, less than 3 nm, less than 2 nm, or less than 1 nm, for example in a range of 0.5 nm to 5 nm in some embodiments. In some arrangements, the recess variation can comprise a maximum difference between recess depths among the plurality of conductive contact features. In some arrangements, the recess variation can comprise an average difference between recess depths among the plurality of conductive contact features. Residue management may also be challenging, as the thick protective coating 312 may result in a relatively large amount of residue, which may be difficult to fully remove from the semiconductor elements 302a-302d. Additionally, higher baking temperatures may make it more difficult to strip the protective layer 312 from the semiconductor elements 302a-302d. Additionally, at higher temperatures the protective layer 312 may react with metallic pads 308a-308d, and such a reaction may tend to roughen the metallic bonding pads 308a-308d and increase the recess of the metallic bonding pads 308a-308d.

[0040] In some embodiments, for the traditional thick resist and high baking temperature approach, the recess of pads 308a-308d may range from about 60 nm to about 200 nm or more for a 2 micrometer thick metal pad, for example. After the solvent cleaning step to remove the protective layer 312, some of the pads 308a-308d disposed at various portions of the bonding surface 310 may be clean, for example, after 180s, while pads at other portions of the bonding surface 310 may still be contaminated with the hard baked protective layer 312. Additional cleaning times of, for example, 180s or longer, may be used to strip the protective layer from the surface of pads 308a-308d or the bonding surface 310. Thus, some clean pads may be exposed to solvent action for a significant additional time. Depending on the

dissolution or loss of pad material during the protective layer 312 removal, large variations in recess may be formed within a given die and/or between dies located at different portions of the substrate 314, for example dies located at the center and those disposed close the edge of the substrate 314. The recess variation (i.e., the maximum difference between recess depths from the bonding surface 310 for any two pads) in pads within any given die may vary by an amount greater than 10 nm, *e.g.*, 15 nm or greater. These large variations in recess 309 within a given die and across the substrate 314 can be problematic, because a higher bonding temperature may be needed to form adequate metal-to-metal bonds in the bonded substrates 100 of Fig. 1b for pads with deeper recesses, as shown in FIG. 2.

[0041] Accordingly, in various embodiments, as shown in FIG. 4 in block 420, a thinner protective coating 412 can instead be applied over the bonding surface 310 of the semiconductor element 302, for example by spin coating, atomic layer deposition, or vapor coating. The thin protective coating can have a thickness of less than 3 microns, less than 2 microns, less than 0.25 microns, or less than 0.1 microns. For example, in various embodiments, the thickness of the protective coating can be in a range of 0.05 microns to 2 microns, or in a range of 0.1 microns to 0.25 microns. The thin protective coating can comprise, for example, an organic layer in some embodiments. The thin protective layer may be baked at a temperature lower than 130°C and preferably at a temperature lower than 110°C and even lower than 70°C. For example, the protective layer can comprise a hydrophobic coating and/or a hydrophilic coating or combination of both. In some embodiments, the protective layer can comprise a photoresist. In the embodiment of FIG. 4, the protective layer can be blanket deposited across the semiconductor element, including over contact pads 308 and over non-conductive bonding region(s) 306. Advantageously, the thinner protective layer can have less variance in coating thickness compared to a thicker layer.

[0042] In various embodiments, the bonding surface can be prepared for direct bonding prior to providing the protective layer 312. For example, the bonding surface can be planarized before providing the protective layer 312. In some embodiments, the bonding surface can be activated before providing the protective layer 312. Activating the first bonding surface can comprise plasma activating the first bonding surface. Plasma activating the first bonding surface can comprise exposing the first bonding surface to a nitrogen-containing plasma. In other embodiments, the bonding surface of the semiconductor element 302 to be

singulated may be briefly exposed to oxygen plasma (ashing), to form a very thin oxide (for example, a few nanometers thick) on the surface of the pads 308, before applying the protective layer 312.

[0043] The semiconductor element 302 can remain covered with the protective layer 312 for any suitable time period. For example, in some embodiments, the semiconductor element 302 can be prepared for direct bonding and coated with the protective layer 312, and subsequently stored and/or transported to a different location or facility. In some cases, the protected semiconductor element 302 can remain protected by the protective layer 312 for a period greater than 24 hours, or for a period of a week or longer, or a month or longer. As shown in block 422, prior to removal of the protective layer 312, the semiconductor element may be singulated into a plurality of semiconductor elements having bonding surfaces 310a-310d, non-conductive regions 306a-306d and conductive contact regions 308a-308d. At block 424, the protective layer 312 can be removed in any suitable manner before direct bonding. For example, the protective layer 312 can be removed with any suitable cleaning process. In some embodiments, a first cleaning process can utilize a highly alkaline solution, for example dilute tetramethylammonium hydroxide, or other suitable solvents recommended by the supplier of the protective layer (such as blends of polygycols, or a modified ketone, for example) to strip the protective coating 412. The modified ketone can have minimal interaction with a dicing tape (unlike acetone, which may readily attack the dicing tape) and/or the metal of the contact pads 306a and 306b. In one embodiment, when the protective layer is a photoresist material, the coated photoresist protective layer may be exposed to UV light to degrade the resist layer, thus reducing the cleaning times to strip the protective layer from the bonding surface of the semiconductor element. Advantageously, the protective layer 312 may be removed more quickly (e.g., in about 60 s or less) than a thick protective layer as depicted in FIG. 3. Overstripping times can also be significantly shorter, for example less than 30 seconds, less than 20 seconds, or less than 15 seconds, whereas overstripping times for thicker layers can often exceed 1 minute, 2 minutes, or more. Additionally, less debris may remain.

[0044] In some embodiments, a second cleaning process can additionally or alternatively be used. For example, the second cleaning process can be used for cleaning dicing particles and other debris from dies and dicing sheet. In this example, the first cleaning step may strip the protective layer 312 from the bonding surface of the semiconductor element and

the second cleaning step may comprise a cleaning solution tailored to remove unwanted organic materials and unwanted particulates from the plurality of semiconductor elements and the dicing lanes of the dicing tape. In this embodiment, the first cleaning step may comprise a dry process, for example applying oxygen plasma to strip the very thin organic protective layer from the surface of the singulated semiconductor elements. In some embodiments, the second cleaning step may comprise a wet cleaning solution. In such cleaning steps, a suitable solvent containing a suitable surfactant or particulate removing agent may be used to clean the ashed surface of the semiconductor element. The cleaning step is typically followed by a deionized (DI) water rinse and drying step.

[0045] Beneficially, the thin protective coating can utilize a cleaning fluid, as explained above, that is more amenable to the materials used in the semiconductor element. The shorter duration of the removal process and overall cleaning times can beneficially reduce the degree to which the copper pads are degraded by the cleaning process, as compared to processes using a thicker protection layer and longer cleaning processes. The embodiment of FIG. 4 can accordingly provide shallower recesses 309 and more consistent recess depths (i.e., less recess variation), which can improve direct bond reliability in hybrid bonded structures. In some embodiments, no two pads may have a difference in recess depths of greater than 5 nm, greater than 3 nm, greater than 1 nm, or greater than 0.5 nm. The recess variation among the pads of the die is less than 25%, less than 10%, less than 5%, less than 2%, or less than 1%, or less than about 0.5%. In various embodiments, the recess variation among the pads of the due can be in a range of 0.1% to 10%, in a range of 0.1% to 5%, or in a range of 0.5% to 5%. The recess variation can be less than 5 nm, less than 3 nm, less than 2 nm, or less than 1 nm, for example in a range of 0.5 nm to 5 nm in some embodiments. In some arrangements, the recess variation can comprise a maximum difference between recess depths among the plurality of conductive contact features. In some arrangements, the recess variation can comprise an average difference between recess depths among the plurality of conductive contact features.

[0046] FIG. 5 illustrates another example process 500 in which a thin protective layer 512 is provided over a passivation layer 514 according to some embodiments. At step 520, a passivation layer 514 can be selectively provided over the contact pads 308. For example, a wet chemical process and/or a plasma process can be used to selectively oxidize

the contact pads 308. In some embodiments, a few monolayers of a metal complexing agent such as benzotriazole or a similar compound may be selectively coated on the contact pads 308 by known methods.

[0047] At step 522, a thin protective layer 512 (e.g., a protective layer less than about 2 μm thick, and preferably less than about 0.2 μm thick) can be provided over the pads 308 and the non-conductive bonding region 306 of the element. In the illustrated embodiment, the protective layer 512 is blanket deposited over the element. At step 524, the element 302 can be singulated, and, at step 526, the protective layer 512 can be removed as explained above. In some embodiments, the protective layer may be striped in less than about three minutes At step 528, the passivation layer 514 can be selectively removed from the contact pads 308 by a wet etch, a foaming gas, or other suitable means. Additional cleaning may be performed for particle management.

[0048] FIG. 6 illustrates another example process 600 according to some embodiments, in which the contact pads 308 protrude above the non-conductive bonding material 306 before application of the protective layer 612. As shown in block 620, the contact pads 308 may protrude above the bonding surface 310 of the non-conductive bonding material 306 (for example, if the non-conductive bonding material 306 has been etched previously or as the result of a chemical-mechanical-polished or CMP process). At block 622, a protective layer 612 (which may be the same as the protective layer 412) can be provided over the protruding contact pads 308 and the non-conductive bonding material 306, and the element 302 can be singulated. At block 624, the protective layer 612 can be removed. In some embodiments, at block 624, removing the protective layer 612 also causes some removal of the surface of the contact pads 308, reducing the protrusion of the contact pads 308 above the surface of the non-conductive bonding material 306. At block 626, the bonding surface can be planarized (for example, by a chemical-mechanical-polishing or CMP process) such that the contact pads 308 are recessed relative to the surface of the non-conductive bonding material 306. Pad recess may also be controlled by managing the copper/oxygen interaction. In other embodiments, after stripping the protective layer 612, unwanted protrusion on the pads 308 may be removed by cleaning the bonding surface 310 and pads 308 with a dilute pad cleaning agent to form a known or desired recess in the pads 308. The cleaning may form a known recess without degrading the bonding surface 310 or the bonding surface of the recessed pads.

For example, the cleaning agent may not result in significant roughening of the bonding surface 310 or the pads 308 and may not result in the formation of unwanted particulates on the bonding surfaces that could impair direct between opposing substrates without adhesive material.

[0049] FIG. 7 illustrates an example process 700 according to some embodiments, in which a protective coating is selectively provided over the contact pads, as opposed to being deposited as a blanket coating. At block 720, a passivation layer 714 (which may be similar to or the same as passivation layer 514) can be applied on the pads 308, and a protective layer 712 can be applied over the passivation layer 714. In some embodiments, only a passivation layer 714 may be selectively applied to protect the pads without the use of a protective layer 712, which can reduce recess variation and recess increases due to removal of the protective layer 712. Thus, no organic blanket layer may be provided over the entire surface of the semiconductor element. In some embodiments, therefore, the passivation layer 714 can serve as the protective layer to protect the pads during singulation, such that a separate protective layer 712 may not be applied. The passivation layer 714 can be provided to oxidize the pads, which can resist cleaning chemicals better than copper. At block 722, the element 302 can be diced while maintaining a wet surface. After dicing, the element 302 can be cleaned, for example, using water and surfactants. The passivation layer on the pad can be removed using any suitable method. For example, the passivation layer can be removed using a dilute acid or base solution, and/or by an oxidizer/caustic to remove the hydrophobic coated region without substantially attacking the copper pads.

[0050] In some embodiments, reactive ion etching (RIE) can be used to remove the thin protective coating.

[0051] In some embodiments, a saw can be used to singulate the element. In other embodiments, RIE can be used to singulate the semiconductor element into a plurality of singulated device dies. In such embodiments, the protective layer can be provided to a thickness of approximately 1 micron, *e.g.*, in a range of 1 micron to 3 microns. The RIE process may be used to singulate the element, and the protective layer can protect the pads during RIE. The RIE process, however, may reduce the thickness of the protective layer sufficiently such that a subsequent cleaning process can be used to remove the remaining thin protective layer without causing an excessively large recess. At block 724, the protective layer

712, if present, can be removed and, at block 726, the passivation layer 714 can be removed to expose the surface of the conductive contact regions 308a-d.

[0052] In some embodiments, conductive pads 308 having varying dimensions may be formed in dielectric layer 306 and the conductive pads 308 may have exposed bonding surfaces. For example, the various conductive features within a die may comprise pads with a width of 2 to 4 microns, 5 to 8 microns, or 10 to 15 microns. Conductive pads may be arranged in arrays having defined pitches. In some embodiments, the pitch of smaller pads may be smaller than the pitch of larger pads. Advantageously, the methods described herein can result in recesses formed on the various pads with varying width and pitch being the same or similar. For example, the variation in recess induced by protective layer coating, singulation, protective layer stripping, and other surface preparation steps may be less than about 3 nm across a given die, for example, less than 2 nm or less than 1 nm across a die. In some embodiments, the recess variation across a die can be in a range of 0.3 nm to 3 nm, in a range of 0.5 nm to 3 nm, or in a range of 1 nm to 3 nm. With the shallow recess and small variation in recess across the die, a bonded structure (such as the bonded structure 100) can be formed at a comparatively lower temperature compared to dies with deeper recesses and/or large variation in recesses with a given die. With the lower temperature bonding operation, dies having larger differences in thermal expansion may be directly bonded without an adhesive layer. For example, the thermal expansion of semiconductor element 104 may be different from that of semiconductor element 102. As just one example, in some embodiments, the difference between the thermal expansion of the bonded semiconductor elements 102 and 104 may be at least 10%.

[0053] Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise," "comprising," "include," "including" and the like are to be construed in an inclusive sense, as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to." The word "coupled," as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Likewise, the word "connected," as generally used herein, refers to two or more elements that may be either directly connected, or connected by way of one or more intermediate elements. Additionally, the words "herein," "above," "below," and words of similar import, when used in this application, shall refer to this application as a whole and not to any particular portions of this application. Moreover, as used

herein, when a first element is described as being "on" or "over" a second element, the first element may be directly on or over the second element, such that the first and second elements directly contact, or the first element may be indirectly on or over the second element such that one or more elements intervene between the first and second elements. Where the context permits, words in the above Detailed Description using the singular or plural number may also include the plural or singular number respectively. The word "or" in reference to a list of two or more items, that word covers all of the following interpretations of the word: any of the items in the list, all of the items in the list, and any combination of the items in the list.

[0054] Moreover, conditional language used herein, such as, among others, "can," "could," "might," "may," "e.g.," "for example," "such as" and the like, unless specifically stated otherwise, or otherwise understood within the context as used, is generally intended to convey that certain embodiments include, while other embodiments do not include, certain features, elements and/or states. Thus, such conditional language is not generally intended to imply that features, elements and/or states are in any way required for one or more embodiments.

[0055] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the disclosure. Indeed, the novel apparatus, methods, and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the disclosure. For example, while blocks are presented in a given arrangement, alternative embodiments may perform similar functionalities with different components and/or circuit topologies, and some blocks may be deleted, moved, added, subdivided, combined, and/or modified. Each of these blocks may be implemented in a variety of different ways. Any suitable combination of the elements and acts of the various embodiments described above can be combined to provide further embodiments. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the disclosure.

WHAT IS CLAIMED IS:

1. A bonding method comprising:

preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element; and

after the preparing, providing a protective layer over at least a portion of the prepared first bonding surface of the first element, the protective layer having a thickness less than 3 microns.

2. The bonding method of Claim 1, wherein preparing the first bonding surface comprises activating the first bonding surface.

3. The bonding method of Claim 2, wherein activating the first bonding surface comprises plasma activating the first bonding surface.

4. The bonding method of Claim 3, wherein plasma activating the first bonding surface comprises exposing the first bonding surface to a nitrogen-containing plasma.

5. The bonding method of any one of Claims 1 to 4, wherein the thickness of the protective layer is less than 2 microns.

6. The bonding method of Claim 5, wherein the thickness of the protective layer is less than 0.25 microns.

7. The bonding method of Claim 5, wherein the thickness of the protective layer is in a range of 0.05 microns to 2 microns.

8. The bonding method of Claim 5, wherein the thickness of the protective layer is in a range of 0.1 microns to 0.25 microns.

9. The bonding method of any one of Claims 1 to 8, wherein the protective layer comprises an organic layer.

10. The bonding method of any one of Claims 1 to 9, wherein the protective layer comprises a hydrophobic coating and/or a hydrophilic coating.

11. The bonding method of any one of Claims 1 to 10, wherein the protective layer comprises a photoresist.

12. The bonding method of any one of Claims 1 to 10, wherein providing the protective layer comprises blanket depositing the protective layer over the first bonding surface.

13. The bonding method of Claim 12, further comprising removing the blanket deposited protective layer using a reactive ion etching (RIE) process.

14. The bonding method of Claim 13, further comprising, before the removing, cleaning particles from the first element.

15. The bonding method of any one of Claims 1 to 14, further comprising, before providing the protective layer, selectively providing a passivation layer over a plurality of contact pads, and wherein providing the protective layer comprises providing the protective layer over the passivation layer.

16. The bonding method of any one of Claims 1 to 10, wherein providing the protective layer comprises selectively providing the protective layer over conductive contact pads of the first bonding surface.

17. The bonding method of any one of Claims 1 to 16, wherein the first bonding surface includes a plurality of contact pads, the contact pads protruding above a first non-conductive region of the first bonding surface, wherein providing the protective layer comprises providing the protective layer over at least the protruding contact pads.

18. The bonding method of Claim 17, wherein providing the protective layer comprises blanket depositing the protective layer over the first bonding surface.

19. The bonding method of Claim 17 or 18, further comprising planarizing the first element such that the plurality of contact pads are flush with or recessed below the first non-conductive region.

20. The bonding method of any one of Claims 1 to 19, wherein the first bonding surface includes a first plurality of conductive contact pads and a first non-conductive bonding region, the first plurality of conductive contact pads recessed below the first non-conductive bonding region.

21. The bonding method of Claim 20, wherein the first plurality of conductive contact pads are recessed below the first non-conductive bonding region by no more than 10 nm.

22. The bonding method of Claim 20 or 21, wherein a variation in recess depth of the first plurality of contact pads across the first element is less than 25%.

23. The bonding method of Claim 22, wherein the variation in recess depth of the first plurality of contact pads across the first element is less than 10%.

24. The bonding method of any one of Claims 1 to 19, further comprising removing the protective layer.

25. The bonding method of Claim 24, wherein the first element comprises a wafer, the method further comprising, before removing the protective layer, singulating the wafer to form a plurality of singulated elements.

26. The bonding method of Claim 24 or 25, further comprising, after removing the protective layer, directly bonding the first bonding surface of the first element to the second bonding surface of the second element without an intervening adhesive.

27. The bonding method of Claim 26, wherein the first bonding surface comprises a first plurality of conductive contact pads and a first non-conductive bonding region, wherein the second bonding surface comprises a second plurality of conductive contact pads and a second non-conductive bonding region, and wherein directly bonding comprise hybrid direct bonding, including directly bonding the first and second pluralities of conductive contact pads to one another without an adhesive and directly bonding the first and second non-conductive bonding regions to one another without an adhesive.

28. The bonding method of Claim 27, wherein the first non-conductive bonding region comprises a silicon-containing dielectric layer.

29. The bonding method of any one of Claims 26 to 28, further comprising activating the second bonding surface before directly bonding.

30. The bonding method of any one of Claims 26 to 29, wherein preparing the first bonding surface and providing the protective layer are performed in a first facility, and wherein directly bonding is performed at a second facility that is in a different location from the first facility.

31. The bonding method of any one of Claims 26 to 30, wherein directly bonding is performed more than twenty-four (24) hours after activating the first bonding layer.

32. A bonding method comprising:

preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element;

after preparing the first bonding surface of the first element, selectively providing a passivation layer over a first plurality of contact pads of the first bonding surface; and

after providing the passivation layer, providing a protective layer over the passivation layer.

33. The bonding method of Claim 32, wherein providing the protective layer comprises blanket depositing the protective layer over the first bonding surface.

34. The bonding method of Claim 32 or 33, wherein the protective layer has a thickness less than 3 microns.

35. The bonding method of Claim 34, wherein the thickness of the protective layer is less than 2 microns.

36. The bonding method of Claim 35, wherein the thickness of the protective layer is less than 0.25 microns.

37. The bonding method of Claim 35, wherein the thickness of the protective layer is in a range of 0.05 microns to 2 microns.

38. The bonding method of Claim 35, wherein the thickness of the protective layer is in a range of 0.1 microns to 0.25 microns.

39. The bonding method of any one of Claims 32 to 38, wherein the protective layer comprises an organic layer.

40. The bonding method of any one of Claims 32 to 39, wherein the protective layer comprises a hydrophobic coating and/or a hydrophilic coating.

41. The bonding method of any one of Claims 32 to 40, further comprising removing the protective layer.

42. The bonding method of Claim 41, wherein the first element comprises a wafer, the method further comprising, before removing the protective layer, singulating the wafer to form a plurality of singulated elements.

43. The bonding method of Claim 41 or 42, further comprising, after removing the protective layer, directly bonding the first bonding surface of the first element to the second bonding surface of the second element without an intervening adhesive.

44. The bonding method of any one of Claims 32 to 43, wherein the first plurality of contact pads are recessed below a first non-conductive bonding region of the first bonding surface.

45. The bonding method of Claim 44, wherein the first plurality of contact pads are recessed below the first non-conductive bonding region by no more than 10 nm.

46. The bonding method of Claim 44 or 45, wherein a variation in recess depth of the first plurality of contact pads is less than 25%.

47. The bonding method of Claim 46, wherein the variation in recess depth of the first plurality of contact pads is less than 10%.

48. A bonding method comprising:

preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element; and

after the preparing, selectively providing a protective layer over a plurality of contact pads of the first bonding surface.

49. The bonding method of Claim 48, wherein the first bonding surface further includes a first non-conductive material, wherein no protective layer is provided over an entirety of the first non-conductive material.

50. The bonding method of Claim 48 or 49, wherein the protective layer has a thickness less than 3 microns.

51. The bonding method of Claim 50, wherein the thickness of the protective layer is less than 2 microns.

52. The bonding method of Claim 50, wherein the thickness of the protective layer is less than 0.25 microns.

53. The bonding method of Claim 50, wherein the thickness of the protective layer is in a range of 0.05 microns to 2 microns.

54. The bonding method of Claim 50, wherein the thickness of the protective layer is in a range of 0.1 microns to 0.25 microns.

55. The bonding method of any one of Claims 48 to 54, wherein the protective layer comprises an organic layer.

56. The bonding method of any one of Claims 48 to 55, wherein the protective layer comprises a hydrophobic coating and/or a hydrophilic coating.

57. The bonding method of any one of Claims 48 to 56, further comprising providing a passivation layer comprising oxidizing surfaces of the contact pads.

58. The bonding method of any one of Claims 48 to 57, further comprising removing the protective layer.

59. The bonding method of Claim 58, wherein the first element comprises a wafer, the method further comprising, before removing the protective layer, singulating the wafer to form a plurality of singulated elements.

60. The bonding method of Claim 58 or 59, further comprising, after removing the protective layer, directly bonding the first bonding surface of the first element to the second bonding surface of the second element without an intervening adhesive.

61. A bonding method comprising:

preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element, the first bonding surface including a first non-conductive region and a first plurality of contact pads protruding above the first non-conductive region; and

after the preparing, providing a protective layer over at least the first plurality of contact pads.

62. The bonding method of Claim 61, wherein providing the protective layer comprises blanket depositing the protective layer over the first bonding surface.

63. The bonding method of Claim 61 or 62, further comprising planarizing the first element such that the first plurality of contact pads are recessed below the first non-conductive region.

64. The bonding method of any one of Claims 61 to 63, further comprising removing the protective layer.

65. A bonding method comprising:

preparing a first bonding surface of a first element for direct bonding to a second bonding surface of a second element; and

after the preparing, selectively providing a passivation layer over a plurality of contact pads of the first bonding surface.

66. The bonding method of Claim 65, wherein providing the passivation layer comprising oxidizing surfaces of the contact pads.

67. The bonding method of Claim 65, further comprising singulating the first element with the passivation layer over the plurality of contact pads, wherein the passivation layer is exposed at an upper surface of the element during the singulating.

68. A semiconductor element comprising:

a device region;

a bonding layer over the device region, the bonding layer having a first bonding surface prepared for direct hybrid bonding to a second element; and

a protective layer over at least a portion of the prepared first bonding surface, the protective layer having a thickness less than 3 microns.

69. The semiconductor element of Claim 68, wherein the protective layer comprises a photoresist.

70. The semiconductor element of Claim 68, wherein the semiconductor element is in wafer form.

71. The semiconductor element of Claim 68, wherein the thickness of the protective layer is in a range of 0.05 microns to 2 microns.

72. The semiconductor element of Claim 68, wherein the bonding layer comprises a plurality of conductive contact pads and a non-conductive bonding region.

73. The semiconductor element of Claim 72, further comprising a passivation layer over the plurality of conductive contact pads between the plurality of contact pads and the protective layer.

74. The semiconductor element of Claim 72, wherein the protective layer is selectively provided over the plurality of conductive contact pads.

75. The semiconductor element of Claim 72, wherein the plurality of conductive contact pads protrude above the bonding layer.

76. The semiconductor element of Claim 72, wherein the plurality of conductive contact pads are recessed below an upper surface of the bonding layer.

77. The semiconductor element of Claim 68, wherein the protective layer is blanket deposited over the bonding surface.

78. A semiconductor element comprising:

a device region;

a bonding layer over the device region, the bonding layer having a bonding surface prepared for direct hybrid bonding to a second element and including a plurality of conductive contact pads and a non-conductive bonding region, the plurality of conductive contact pads each having a recess depth by which the conductive contact pads are recessed below the bonding surface,

wherein a variation in recess depth of the plurality of contact pads is less than 25%.

79. The semiconductor element of Claim 78, wherein the variation in recess depth of the plurality of conductive contact pads is less than 10%.

80. The semiconductor element of Claim 78, wherein the variation in recess depth of the plurality of conductive contact pads is in a range of 0.5% to 10%.

81. A semiconductor element comprising:

a device region; and

a bonding layer over the device region, the bonding layer having a bonding surface prepared for direct hybrid bonding and including a conductive layer exposed at a portion of the prepared bonding surface, the conductive layer having a recess variation less than 5 nm within the bonding surface of the device.

82. The semiconductor element of Claim 81, wherein the recess variation is less than 3 nm within the bonding surface of the device.

83. The semiconductor element of Claim 81, wherein the recess variation is less than 2 nm within the bonding surface of the device.

84. The semiconductor element of Claim 83, wherein the recess variation is less than 1 nm within the bonding surface of the device.

85. The semiconductor element of Claim 81, wherein the recess variation is between 0.5 nm and 5 nm within the bonding surface of the device.

86. The semiconductor element of Claim 81, wherein the conductive layer includes a plurality of conductive contact pads, the plurality of conductive contact pads each having a recess depth by which they are recessed below the bonding surface, the recess variation comprising a maximum difference between recess depths for the plurality of conductive contact pads.

87. The semiconductor element of Claim 81, wherein the bonding layer includes a non-conductive layer in which the conductive layer is at least partially embedded.

88. The semiconductor element of Claim 87, wherein the non-conductive layer is polished.

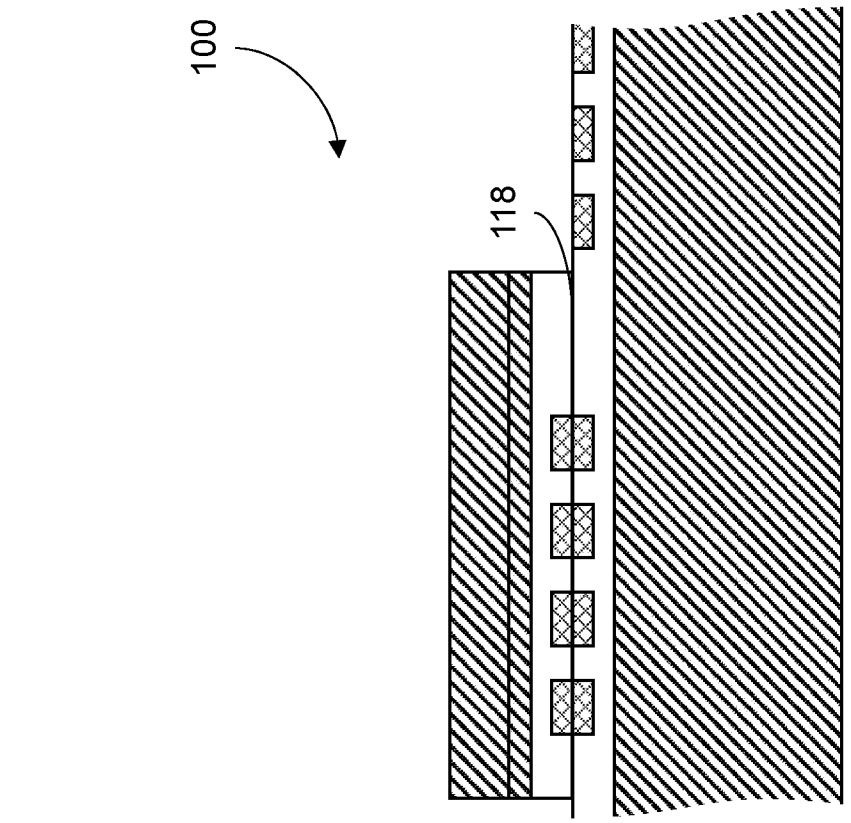

100
118

Fig. 1b

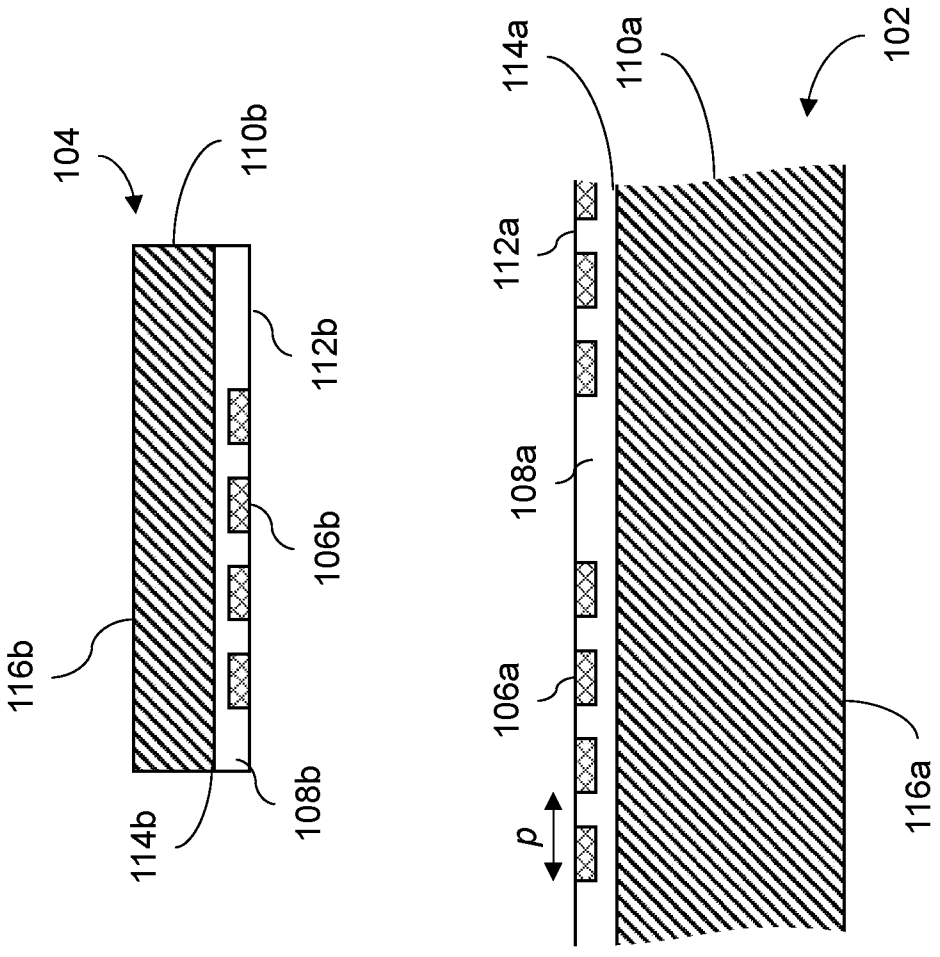

104
110b
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116b
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102
114a
110a
112a
108a
106a
p
116a

Fig. 1a

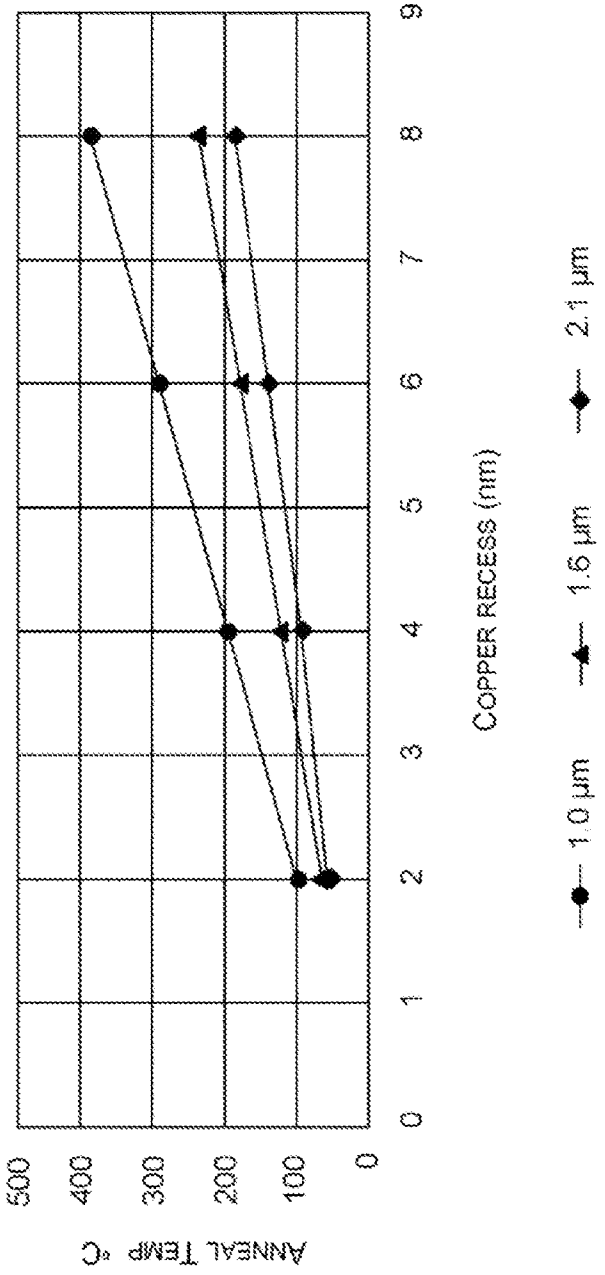
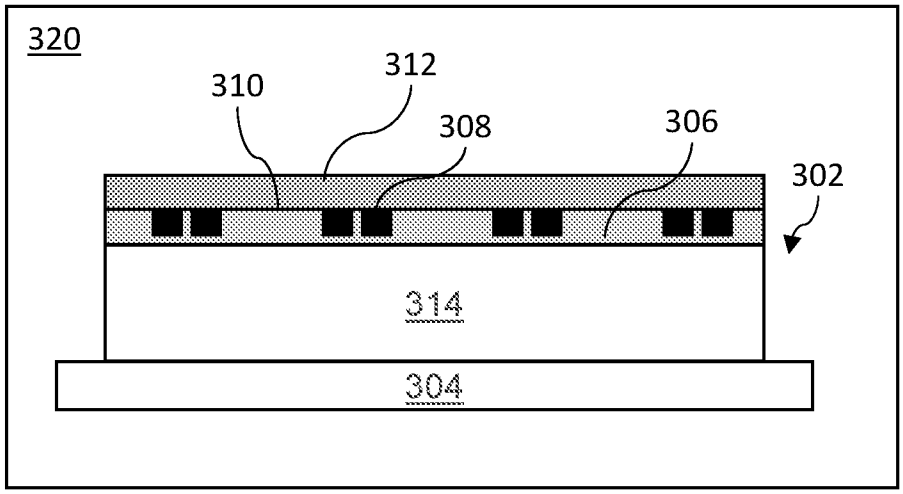
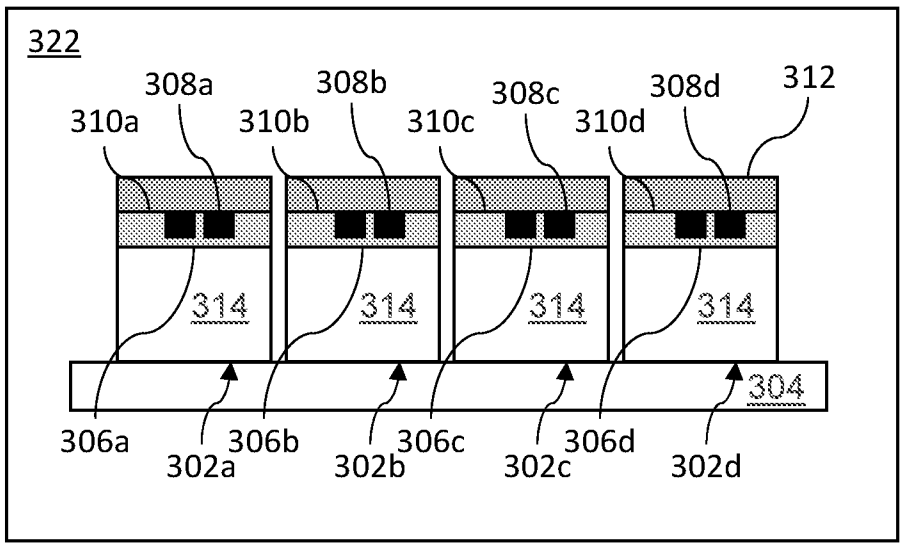

ANNEAL TEMP °C
500
400
300
200
100
0
0
1
2
3
4
5
6
7
8
9
COPPER RECESS (nm)
1.0 µm
1.6 µm
2.1 µm

Fig. 2


320
310
312
308
306
302
314
304


322
308a
308b
308c
308d
312
310a
310b
310c
310d
314
304
306a
306b
306c
306d
302a
302b
302c
302d

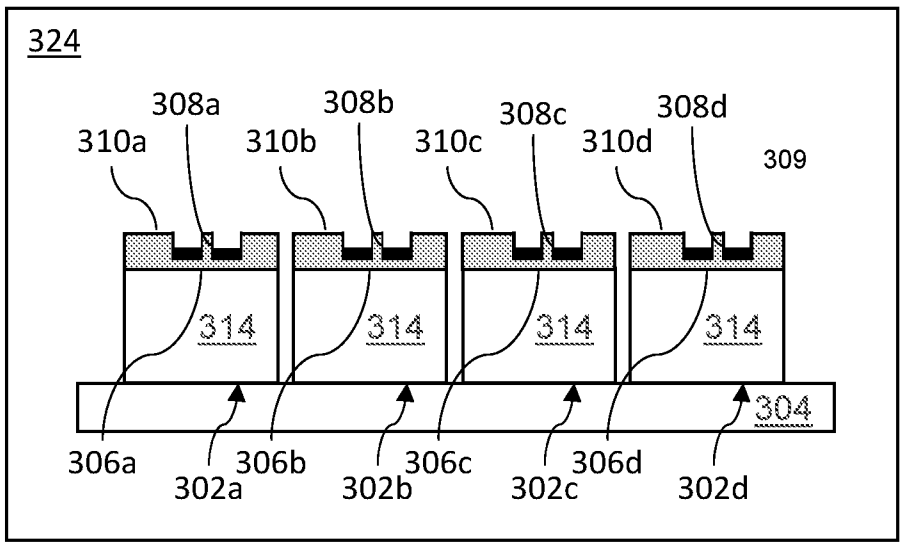

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308c
308d
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310d
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306b
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302b
302c
302d

FIG. 3

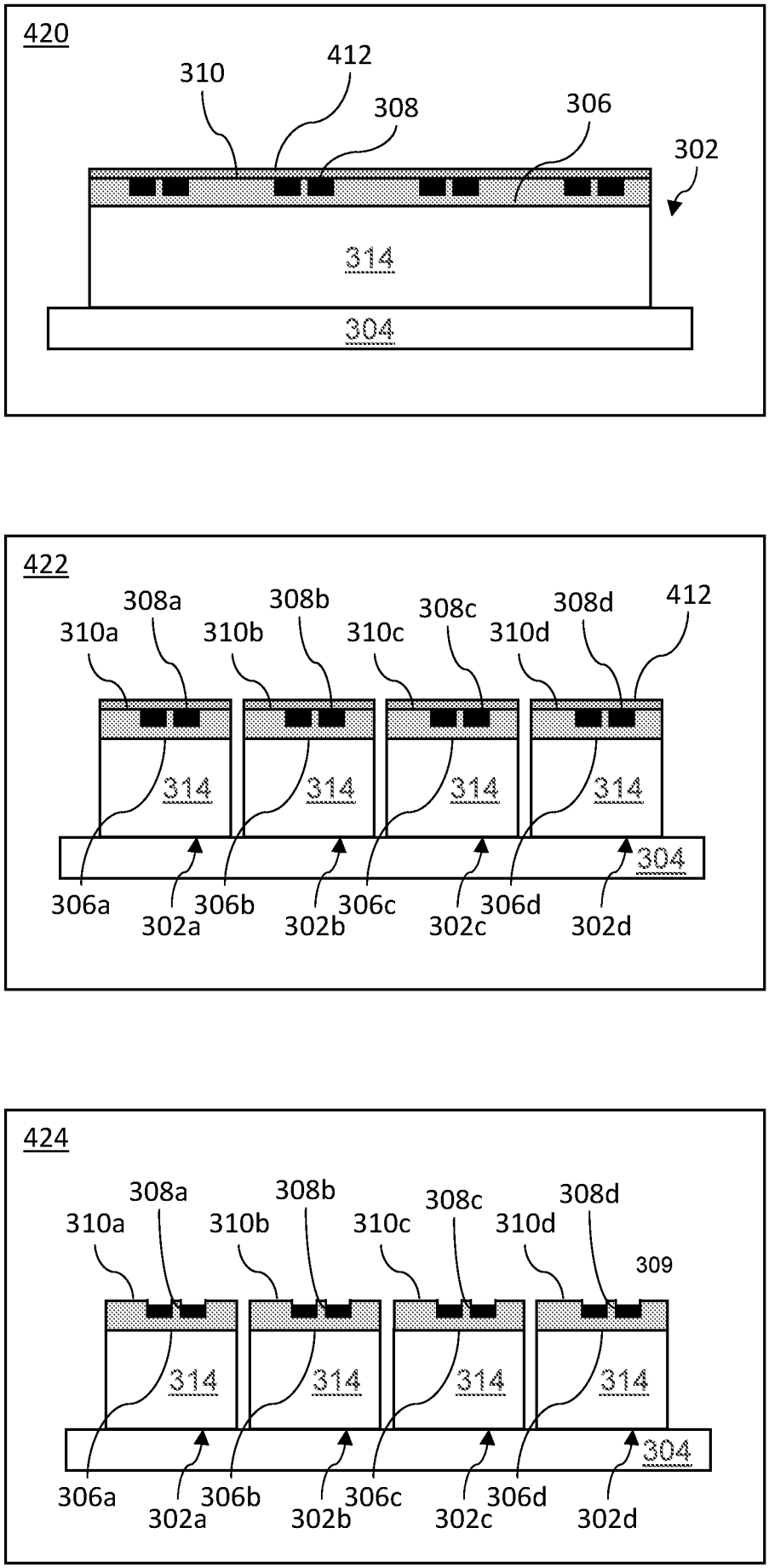

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308a
308b
308c
308d
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304
306a
306b
306c
306d
302a
302b
302c
302d
424
308a
308b
308c
308d
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302b
302c
302d

FIG. 4

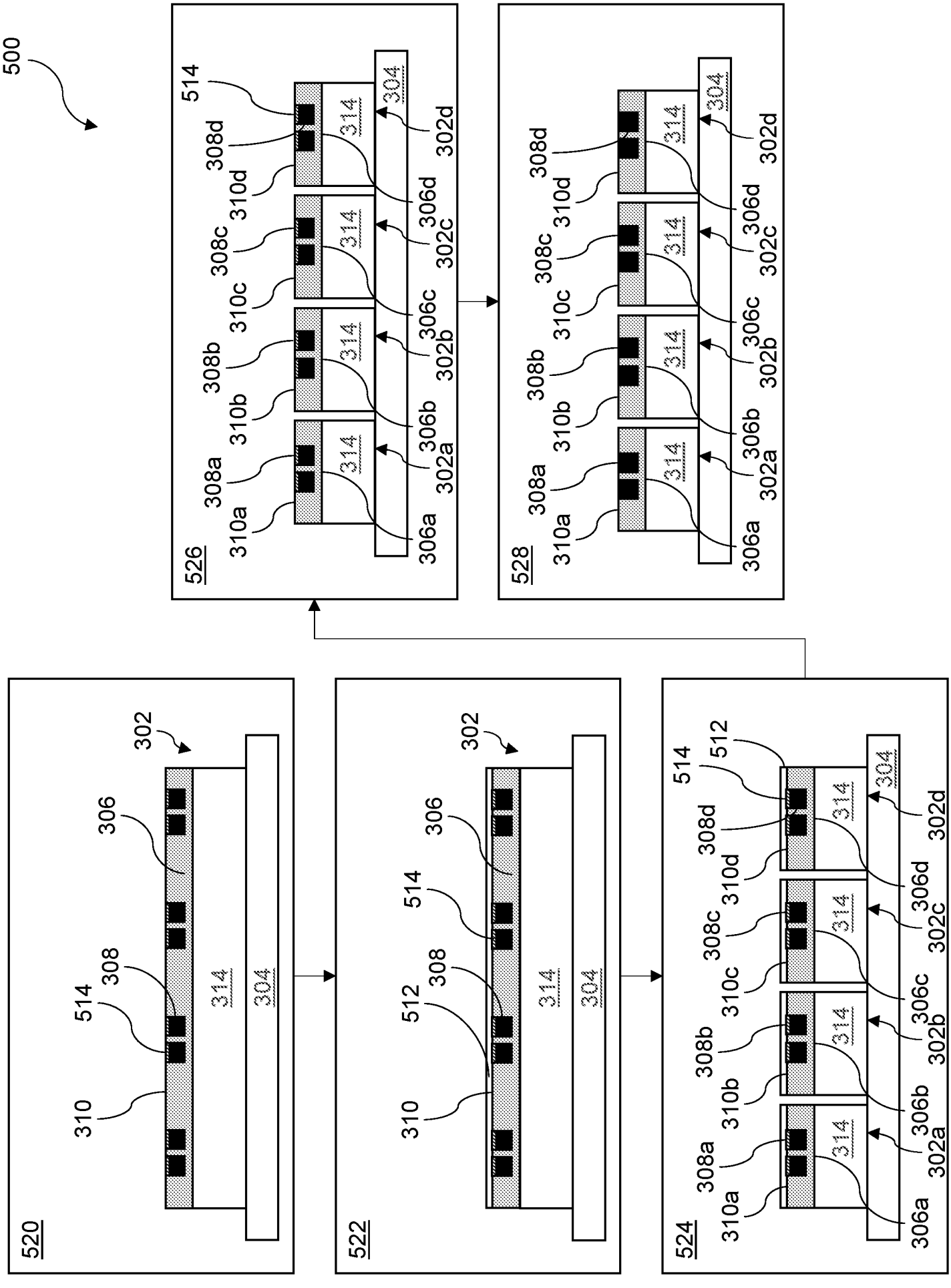

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302a
302b
302c
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308d
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310b
310c
310d

Fig. 5

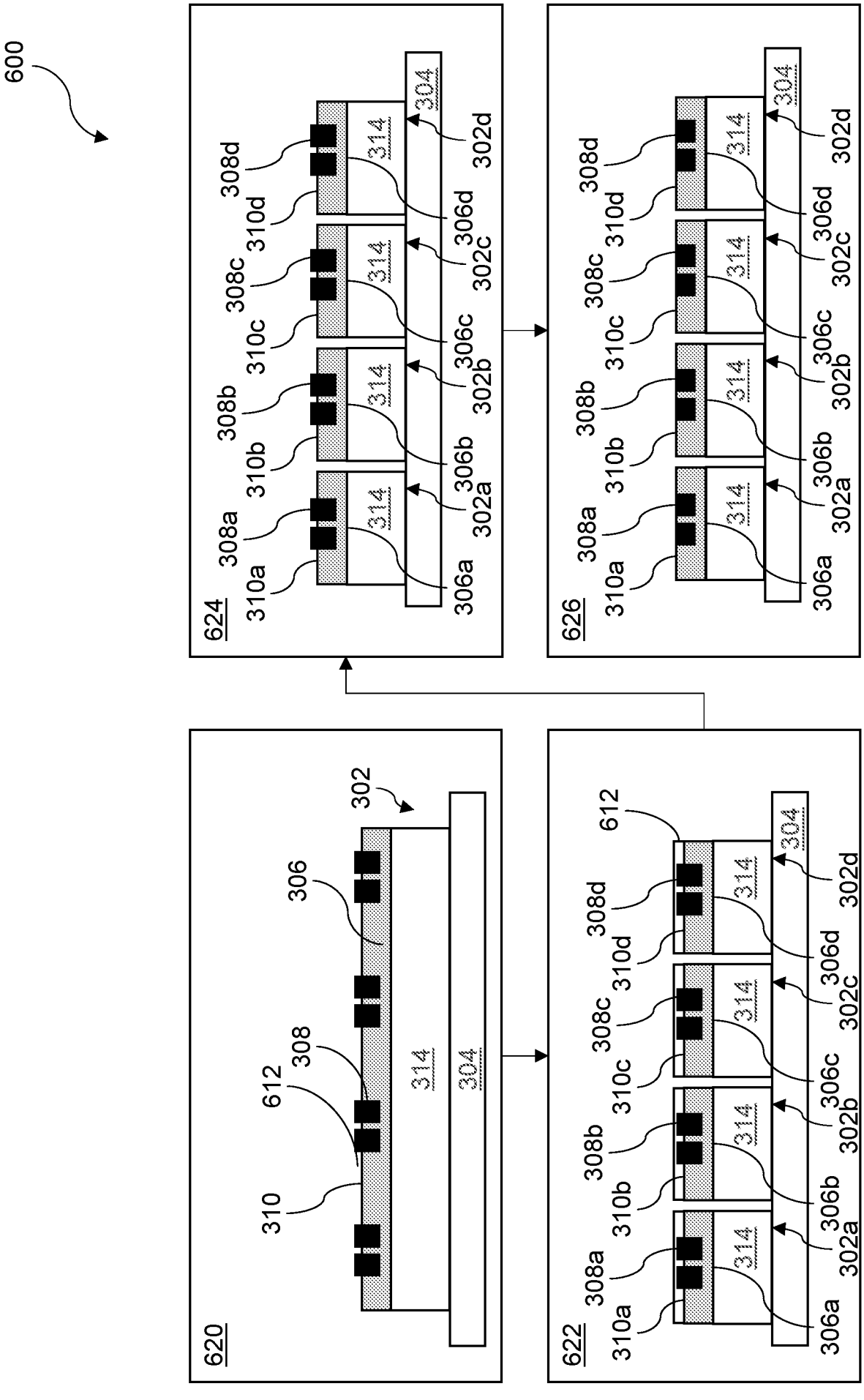

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302a
302b
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308d
310a
310b
310c
310d

Fig. 6

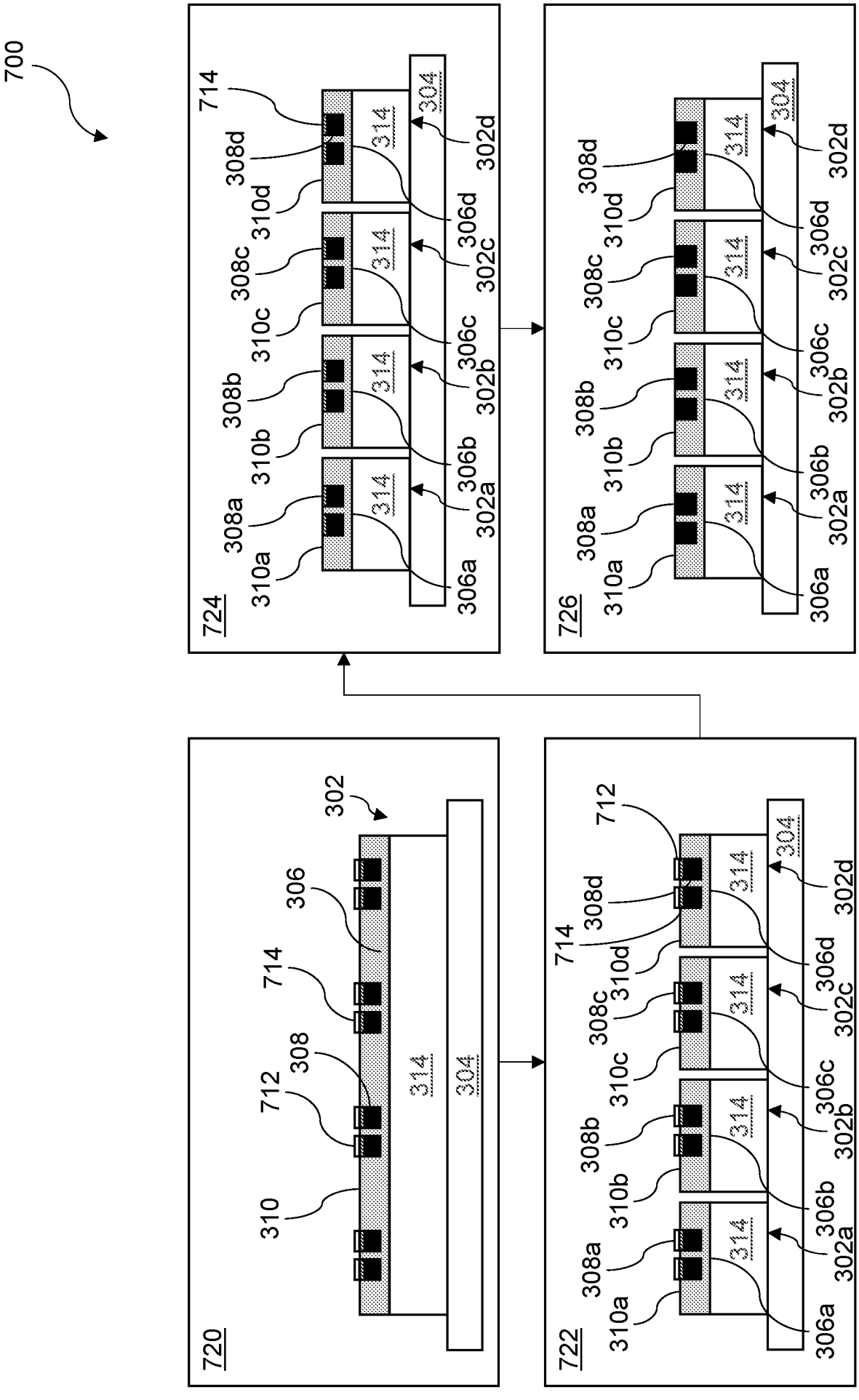

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306a
306b
306c
306d
308a
308b
308c
308d
310a
310b
310c
310d

Fig. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2022/022677

A. CLASSIFICATION OF SUBJECT MATTER

H01L 23/00(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/00(2006.01); H01L 21/20(2006.01); H01L 21/50(2006.01); H01L 21/78(2006.01); H01L 25/00(2006.01); H01L 25/065(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: direct-bonding, plasma-activating, protection, passivation, recess

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2019-0326252 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 24 October 2019 (2019-10-24) Paragraphs 8-93; claims 1-28; and figures 1-3.	48-49,61-63,78-88
Y		1-8,32-38,50-54,65-77
Y	US 2014-0011324 A1 (PING-YIN LIU et al.) 09 January 2014 (2014-01-09) Paragraphs 24-27; and figure 3.	1-8,32-38,50-54,65-77
Y	US 2019-0252364 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 15 August 2019 (2019-08-15) Paragraph 66; and figures 1A-1C.	4
A	US 2018-0308819 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 25 October 2018 (2018-10-25) The entire document.	1-8,32-38,48-54,61-63,65-88

☑ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 July 2022	**25 July 2022**

Name and mailing address of the ISA/KR	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2022/022677

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2011-0010740 A (COMMISSARIAT A L`ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES) 07 February 2011 (2011-02-07) The entire document.	1-8,32-38,48-54,61-63,65-88

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2022/022677

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☑ Claims Nos.: **13, 14, 18, 21, 23, 25, 27, 28, 42, 45, 47, 59**
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

Claims 13, 14, 18, 21, 23, 25, 27, 28, 42, 45, 47, 59 are not clear because they refer to multiple dependent claims, which do not comply with PCT Rule 6.4(a).

3. ☑ Claims Nos.: **9-12, 15-17, 19, 20, 22, 24, 26, 29-31, 39-41, 43, 44, 46, 55-58, 60, 64**
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2022/022677

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/US2022/022677

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