(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
22 May 2025 (22.05.2025)

WIPO | PCT

(10) International Publication Number
WO 2025/106982 A1

(51) International Patent Classification:
H04N 23/23 (2023.01) *H04N 23/20* (2023.01)
H04N 23/52 (2023.01) *G03B 17/55* (2021.01)

(21) International Application Number:
PCT/US2024/056402

(22) International Filing Date:
18 November 2024 (18.11.2024)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
63/600,323 17 November 2023 (17.11.2023) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report (Art. 21(3))*

(54) Title: CRYOGENIC THERMAL IMAGER

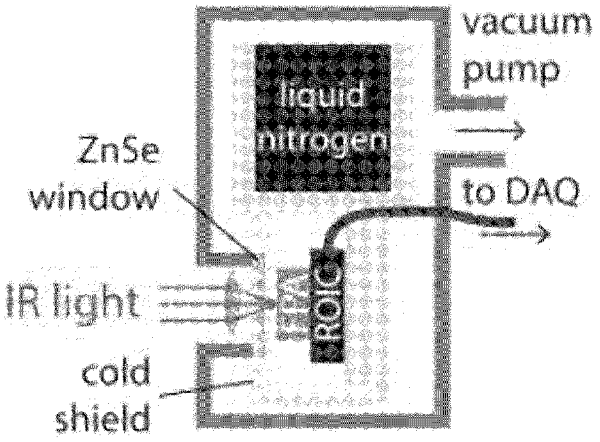

FIG. 1B

(57) Abstract: A high-speed global-shutter thermal imaging system includes a cryostat, the cryostat including a store of coolant and a detector assembly, a vacuum pump, and an output channel to a analog-to-digital converter (ADC).

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CRYOGENIC THERMAL IMAGER

CROSS-REFERENCE TO RELATED APPLICATION

[001] The present application claims priority benefit of U.S. Provisional Application No. 63/600,323, filed November 17, 2023, which is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

[002] In general the present invention relates to imaging, and more particularly to a cryogenic thermal imager.

[003] In general, high-speed thermal imaging is an essential tool for many industrial and scientific applications. However, while complex thermal phenomena can occur on the microsecond timescales, even the fastest commercial thermal cameras can generally acquire only thousands of frames per second. Previous demonstrations at visible wavelengths using specialized burst image sensors have achieved millions of frames per second, but these speeds have generally remained inaccessible for thermal infrared imaging. This limitation comes from the fact that high-performance photodetectors for mid- and long-wavelength infrared (IR) must be constructed from low-bandgap semiconductors, and these devices must operate at very low temperatures. Thus, thermal IR imaging is not compatible with integrated silicon

photodetectors, and cryogenic operation presents practical challenges for scaling up nonintegrated implementations.

SUMMARY OF THE INVENTION

[004] The following presents a simplified summary of the innovation in order to provide a basic understanding of some aspects of the invention. This summary is not an extensive overview of the invention. It is intended to neither identify key or critical elements of the invention nor delineate the scope of the invention. Its sole purpose is to present some concepts of the invention in a simplified form as a prelude to the more detailed description that is presented later.

[005] In an aspect, the present invention features system including a cryostat, the cryostat including a store of coolant and a detector assembly, a vacuum pump, and an output channel to a analog-to-digital converter (ADC).

[006] In another aspect, the present invention features a system including a cryostat, the cryostat including a store of liquid nitrogen and a detector assembly positioned within the cryostat behind an Zinc selenide (ZnSe) window, a vacuum pump, and an output channel to a analog-to-digital converter (ADC).

[007] Embodiments may have one or more of the following advantages.

[008] The system is designed for cryogenic operation at liquid nitrogen temperatures, and it achieves a maximum burst-mode frame rate of five million frames per second, which is the fastest demonstrated imaging array for mid/long-wavelength infrared.

[009] The system is a high-speed global-shutter thermal imaging system with a 24V ×24H pixel HgCdTe infrared focal plane array (FPA) detector and a custom CMOS readout integrated circuit (ROIC), including a 768-frame on-chip analog burst memory bank.

Each pixel contains a buffered current injection circuit and a background current reduction circuit.

[0010] The high-speed global-shutter burst-mode thermal imaging system is optimized for mid- and long- wavelength infrared light (3–10 μm). This is made possible by pairing a custom CMOS readout integrated circuit (ROIC) with a mercury cadmium telluride (MCT or HgCdTe) photodiode array.

[0011] The system achieves thermal imaging burst frame rates as fast as five million frames per second, storing a maximum of 768 frames (153.6 μs at five million frames per second).

[0012] These and other advantages of the invention will be further understood and appreciated by those skilled in the art by reference to the following written specification, claims and appended drawings.

BRIEF DESCRIPTION OF DRAWINGS

[0013] FIGs. 1A, 1B and 1C illustrate an exemplary high-speed global-shutter burst-mode thermal imaging system.

[0014] FIGs. 2A, 2B, 2C, 2D, 2E and 2F illustrate exemplary diagrams of a readout integrated circuit (ROIC).

[0015] FIGs. 3A, 3B and 3C illustrate dark current subtraction.

[0016] FIG. 4 illustrates an exemplary experimental cryostat setup.

[0017] FIG. 5A is an exemplary graph.

[0018] FIG. 5B illustrates experimental responses.

[0019] FIGs 6A and 6B illustrate spatio-temporal infrared imaging at five million frames per second.

[0020] FIG. 6C illustrates image frames before and after a laser line was revealed.

[0021] FIG. 6D illustrates a leading edge of the revealed laser line moving at 79.5 μm/μs.

[0022] FIG. 7 is a table.

[0023] FIG. 8 is a table.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[0024] It is to be understood that the specific devices and processes illustrated in the attached drawings and described in the following specification are exemplary embodiments of the inventive concepts defined in the appended claims. Hence, specific dimensions and other physical characteristics relating to the embodiments disclosed herein are not to be considered as limiting, unless the claims expressly state otherwise.

[0025] The present invention described herein is a high-speed global-shutter burst-mode thermal imaging system which is optimized for mid- and long-wavelength infrared light (3–10 μm). This is made possible by pairing a custom complementary metal-oxide semiconductor (CMOS) readout integrated circuit (ROIC) with a mercury cadmium telluride (MCT or HgCdTe) photodiode array. The thermal imaging system achieves thermal imaging burst frame rates as fast as five million frames per second, storing a maximum of 768 frames (153.6 μs at five million frames per second).

[0026] The focal plane array (FPA) has a 24 × 24 pixel array at a 30-micron pitch in a common-cathode arrangement. The pixel pitch is close to the diffraction-limited resolution for the Long-Wave Infrared (LWIR) focusing optics, and the FPA and ROIC memory bank are sized to capture dynamic failure events within solid materials, such as transient shear band formation.

[0027] HgCdTe photodetectors can have excellent infrared sensitivity, but their small bandgap means that active cooling is needed to optimize the noise and dark current. Thus, the imaging system is designed to operate within a liquid nitrogen cryostat, at approximately −196 °C (77 °K). To minimize wiring overhead

and parasitic capacitances, the imaging system is designed with CMOS ROIC to interface directly with the FPA inside the cryostat.

[0028] In general, a cryostat is a vacuum insulated sample environment that uses liquid cryogens, such as nitrogen or helium, or a mechanical cooler to cool the temperature of a sample.

[0029] Referring now to FIGs. 1A, 1B and 1C, an exemplary high-speed global-shutter burst-mode thermal imaging system illustrated. FIG. 1A illustrates an exemplary die photo of the custom cryogenic CMOS ROIC for infrared imaging. FIG. 1B is an illustration of the imaging system 10. An infrared FPA is bump-bonded to the ROIC, and the detector assembly is positioned within a liquid nitrogen cryostat behind an optical window. FIG. 1C illustrates an architectural diagram of the signal paths within the ROIC supporting high speed burst imaging.

[0030] The CMOS ROIC has an architecture to support image acquisition at millions of frames per second. To directly digitize five million frames per second for all 576 pixels would imply a digitization bandwidth of 2.9 GS/s, but since the ROIC is positioned within a cryostat, there are constraints on the system's size, wiring, bandwidth, and power dissipation. Therefore, instead of real-time digitization, the ROIC is designed with on-chip analog burst memory banks. A simplified illustration of the overall ROIC data path is shown in FIG. 1C, and an illustration of the acquisition sequence is shown in FIG. 3A. The photocurrent from each pixel is amplified, and bursts of samples are written in parallel to the capacitive memory banks. The stored frames are later read out serially from the chip at a reduced speed. Compared to the on-chip real-time burst write speed, the readout is serialized and time-stretched by several orders of magnitude.

[0031] In FIGs. 2A, 2B, 2C, 2D, 2E and 2F, exemplary diagrams of the ROIC are illustrated. More specifically, FIG. 2A illustrates a pixel cell schematic and FIG. 2B illustrates a pixel layout, including the flip-chip photodiode contact pad. The ROIC has 576 pixel amplifiers. FIG. 2C illustrates a memory cell schematic and FIG. 2D illustrates a memory cell layout. The ROIC has a total of 442,368 memory cells to support up to 768 frame burst captures. FIG. 2E is a schematic of the amplifier used in pixels and FIG. 2F illustrates simulated memory cell leakage from room temperature (300 °K) to liquid nitrogen temperature (77 °K).

[0032] FIGs. 3A, 3B and 3C illustrate dark current subtraction. More specifically, FIG. 3A illustrates a summary of the overall timing for burst acquisition and serialized readout. FIG. 3B illustrates how the preamplifier is placed in feedback to memorize the dark current in the learning phase. FIG. 3C illustrates how the subtraction circuit removes dark current and ambient background signal.

[0033] Each pixel in the ROIC contains an integrating preamplifier, dark current subtraction circuit and output buffer as shown in FIG. 2A. One benefit of the hybrid FPA/ROIC assembly is that we can achieve a high optical fill factor while still having area within each pixel for signal conditioning circuits.

[0034] The photocurrent is acquired with a high-speed buffered direct injection (BDI) circuit, which buffers the photocurrent during the brief exposure time and regulates the photodiode anode to maintain a constant reverse bias (typically 50 mV). The amplifier is implemented with a folded structure as shown in FIG. 2E. The common-mode voltage is held above 1.5 V in order to keep M1 in saturation while the signal current is integrated onto C_{int}. The source follower is designed to buffer the integrated voltage into the pixel's burst memory cells, with a bandwidth >50 MHz.

The BDI current buffer has a bandwidth >200 MHz and consumes 216 μW, while the source follower takes 35 μW in each pixel.

[0035] Even at low temperatures, HgCdTe photodiodes can have relatively large reverse leakage currents, and their dark current can vary significantly as a function of temperature, experimental conditions, and device variation. To help tolerate this leakage current, the ROIC implements an adaptive subtraction circuit, which "memorizes" the experimental dark current in each pixel in the moments before the signal acquisition. The system is designed to acquire burst videos of brief transient high-temperature events, and thus the time shortly before the burst capture can provide an useful quiescent background.

[0036] Initially, V_{sub} = 0, both M2 and M3 [FIG. 2A] are off, and I_{pixel} is dominated by the dark current (I_{dark}). During the background learning phase, φ_{sub} = 1, and the pixel current is directed to charge up a small capacitor (C_{sub} = 193 f_F), whose voltage increases until I_{sub} = I_{dark} . M3 is maintained in the linear region, serving as a degeneration resistance on M2 , and the bias value of V_a determines the upper limit of the subtraction current range. Dummy switches are used to minimize the charge injection on C_{sub}. Since the transient burst capture lasts less than 160 μs, and the ROIC is operated at cryogenic temperature, the leakage from C_{sub} is not significant.

[0037] When the pixel transitions to its active phase [φ_{sub} = 0, FIG. 3B], V_{sub} stays unchanged, and I_{sub} continues to represent the memorized dark current. During burst image acquisition, I_{signal} thus represents changes in the photodiode currents compared to the memorized background current (I_{signal} = I_{pixel} – I_{sub}), which can help to increase the useful dynamic range. An experimental measurement of the input-referred signals from one pixel with/without the background subtraction is shown in FIG. 3C, as a function of reverse bias voltage.

[0038] Based on the FPA pixel area, optical magnification, and models of the 3–10 μm thermal emissions, the integration capacitor was selected to be Cint = 750 fF. The pixel integration time (shutter speed) per frame is programmable, with typical values of 75–125 ns. At the end of each integration period, the integrated output voltage from each pixel is sampled into the memory bank. No mechanical shutter is required during the recording.

[0039] The on-chip frame memory is implemented as a series of capacitor banks as shown in FIG. 2C. Each memory cell has C_{mem} = 32.6 f_F plus switches and logic within 6.61 μm × 6.1 μm, and there are 768 cells available for each pixel. Thick-oxide devices were used as switches to minimize leakage, while dummy switches were implemented to reduce the charge injection. Despite the small capacitances, the low-temperature operation mitigates concerns about charge leakage. Representative leakage simulations are presented in FIG. 2F, showing that while the leakage would be significant at room temperature, at liquid nitrogen temperatures the leakage is dramatically reduced. After an experimental burst capture, the memory bank can be read out in a few seconds.

[0040] One potential source of readout error comes from the large size of the overall memory bank, where the parasitic capacitances in the wiring could cause charge sharing issues during readout that decrease the dynamic range and SNR. To reduce charge sharing effects, the ROIC has voltage buffers in the readout paths. Adding buffers to every single memory cell would have cost too much area and power, so output buffers are instead shared by sets of 64 memory cells.

[0041] The memory can be used in groups of 1, 4, 8, or 16 cells per sample, yielding a storage capacity of 768, 192, 96, or 48 frames. In addition to reducing charge sharing effects, grouped memory cells can also improve the kTC noise. However, at

77 °K, the 1/f noise is comparable to the kTC noise, and thus improvements from combining memory cells can be marginal. Before its output from the ROIC, the readout signal is buffered to fully differential to suppress interference and ground loops between the cryostat and the data acquisition system.

[0042] In FIG. 4, an exemplary experimental cryostat setup is illustrated. Inside a liquid nitrogen cryostat, the FPA+ROIC detector assembly is mounted behind an optical window. Outside the cryostat is an accompanying data acquisition board with an ADC and FPGA.

[0043] The ROIC has a total area of 26 mm^2 , and at its peak activity level it dissipates 0.25 W while bursting at five million frames per second. The 24 × 24 pixel array has a pitch of 30 µm and occupies 0.54 mm^2 , while the large memory banks occupy 18.7 mm^2 . The FPA is indium bump-bonded to the ROIC, and the ROIC is wire-bonded to a ceramic pin grid array (CPGA) package in a cavity-down configuration.

[0044] The backside of the ceramic package is placed in contact with the cold finger of the liquid nitrogen cryostat. A cold shield is also positioned around the detector, reducing the background thermal noise from the directions other than the cryostat’s optical window. The assembly is mounted on the backside of a circuit board inside the cryostat, with an opening for optical access. Power, control, and signal lines are routed out of the vacuum chamber through custom cables. Outside the cryostat, a room-temperature data acquisition board hosts an ADC and FPGA with an USB 3.0 interface. System control and acquisition are managed through a Python environment. With a readout speed of 250 000 samples/sec, the full burst frame bank can be digitized in less than 1.8 s. At 77 °K, the measured memory cell leakage over this time is < 0.01% FS.

[0045] FIG. 5A is an exemplary graph illustrating temperature sensitivity of one pixel, measured with a black-body source. FIG. 5B illustrates experimental responses to transient 1–10 µs optical pulses from a TTL-modulated infrared laser diode.

[0046] The ROIC has an analog conversion gain of 0.21µV/e and a maximum capacity of 2800 ke. In FIG. 5A, we characterized the image sensor's temperature response with an infrared black-body reference, with a target emissivity of 0.95. A liquid-cooled aperture was installed in front of the target, and the temperature of the target ranged from 100 °C to 500 °C, corresponding to 3.75–7.77 µm peak emission wavelengths. It is worth noting that the exact curvature of the response is a complex function of the focusing optics and detector responsivity, and these measurements were made with a simple two-lens configuration that was not optimized for chromatic aberration.

[0047] A first experimental demonstration of high-speed transient IR capture is presented in FIG. 5B. An infrared laser diode was modulated with TTL logic, while the ROIC performed a burst acquisition at 5 m frames per second. The measured turn-on time of the laser pulse is less than 1 µs, and the system can easily resolve optical pulses between 10 and 1 µs.

[0048] FIGs 6A and 6B illustrate spatio-temporal infrared imaging at five million frames per second. A chopper wheel was spinning at 200 cycles/sec, periodically revealing an IR laser line on the imager. In FIG. 6C, image frames before and after the laser line was revealed. In FIG. 6D, leading edge of the revealed laser line was moving at 79.5 µm/µs.

[0049] We pointed a static line-profile IR laser module at the FPA through the cryostat window, and modulated the light path with an optical chopper. With the chopper rotating at 200 Hz, the 2.5-inch radius blades are expected to be traveling at 79.8

μm/μs. Burst image sequences measured the IR laser line emerging from behind the chopper blade at 79.5 μm/μs.

[0050] A comparison with state-of-the-art high-speed IR imagers is shown in Table I in FIG. 7, and a performance summary is shown in Table II in FIG. 8. This work is the fastest demonstrated MWIR/LWIR imaging array, with a uniquely designed burst-capture CMOS ROIC co-located with a cryogenic FPA. Extending MWIR/LWIR thermal imaging to MHz frame rates with this high-speed infrared detector and its custom ROIC offers new opportunities to understand forces at the microscale and to design new materials.

[0051] In summary, the high-speed global-shutter thermal imaging system with 24V × 24H resolution supports burst capture of up to 768 frames at up to five million frames per second.

[0052] In the foregoing description, it will be readily appreciated by those skilled in the art that modifications may be made to the invention without departing from the concepts disclosed herein. Such modifications are to be considered as included in the following claims, unless the claims by their language expressly state otherwise.

WHAT IS CLAIMED IS:

1. A system comprising:

a cryostat, the cryostat comprising a store of coolant and a detector assembly;

a vacuum pump; and

an output channel to a analog-to-digital converter (ADC).

2. The system of claim 1 wherein the coolant is liquid nitrogen.

3. The system of claim 1 wherein the detector assembly is positioned within the cryostat behind an optical window.

4. The system of claim 3 wherein the optical window comprises Zinc selenide (ZnSe).

5. The system of claim 3 wherein the detector assembly comprises an infrared focal-plane array (FPA) bump-bonded to a readout integrated circuit (ROIC).

6. The system of claim 3 wherein the readout integrated circuit comprises:

a pixel amplifier/integrator; and

analog burst memory banks.

7. The system of claim 6 wherein the amplifier/integrator is implemented with a folded structure.

8. The system of claim 6 wherein the analog memory banks are implemented as a series of capacitor banks.

9. The system of claim 8 wherein a photocurrent from each pixel

received from the infrared focal-plane array (FPA) is amplified and bursts of samples are written in parallel to the analog memory banks.

10. A system comprising:

a cryostat, the cryostat comprising a store of liquid nitrogen and a detector assembly positioned within the cryostat behind an Zinc selenide (ZnSe) window;

a vacuum pump; and

an output channel to a analog-to-digital converter (ADC).

11. The system of claim 10 wherein the detector assembly comprises an infrared focal-plane array (FPA) bump-bonded to a readout integrated circuit (ROIC).

12. The system of claim 10 wherein the readout integrated circuit comprises:

a pixel amplifier/integrator; and

analog burst memory banks.

13. The system of claim 12 wherein the amplifier/integrator is implemented with a folded structure.

14. The system of claim 12 wherein the analog memory banks are implemented as a series of capacitor banks.

15. The system of claim 14 wherein a photocurrent from each pixel received from the infrared focal-plane array (FPA) is amplified and bursts of samples are written in parallel to the analog memory banks.

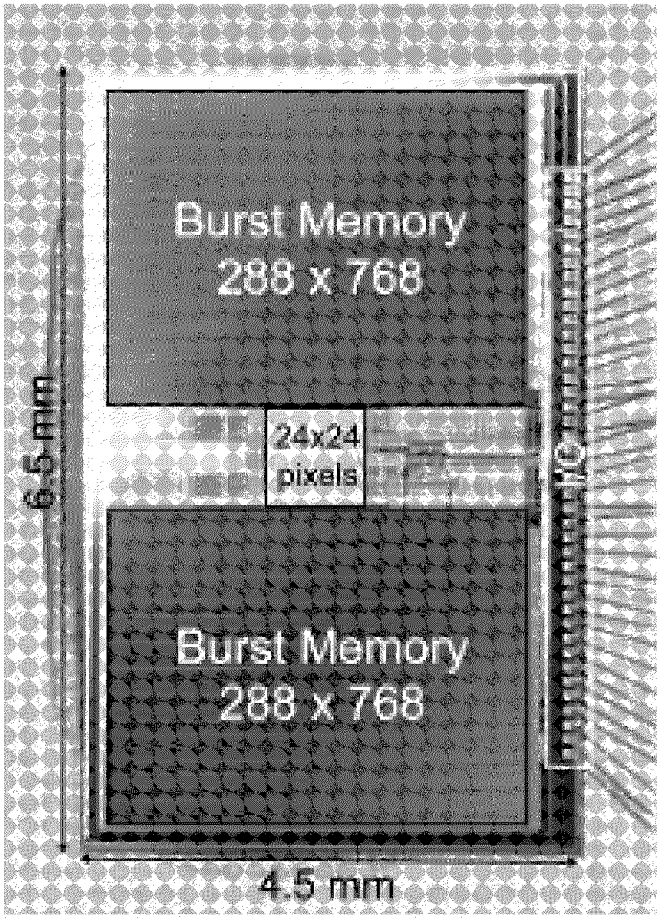
Burst Memory
288 x 768
24x24
pixels
Burst Memory
288 x 768
6.5 mm
4.5 mm

FIG. 1A

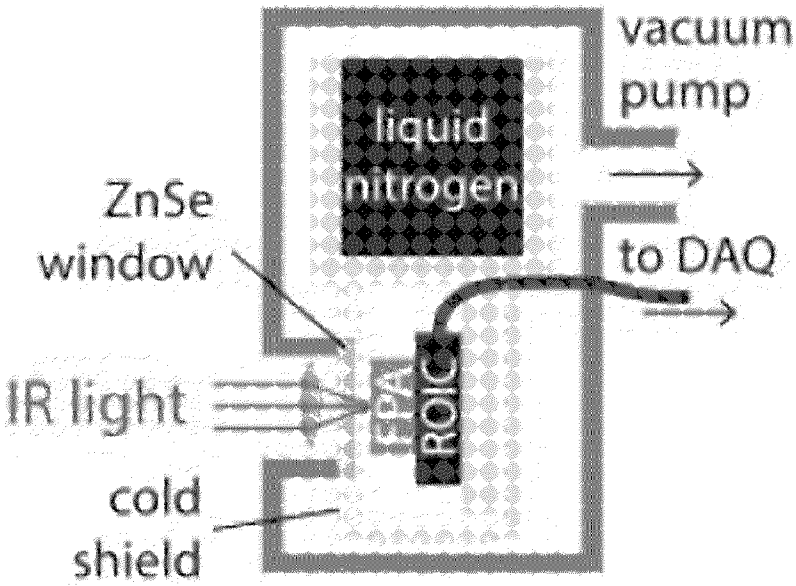
vacuum
pump
liquid
nitrogen
ZnSe
window
to DAQ
IR light
FPA
ROIC
cold
shield

FIG. 1B

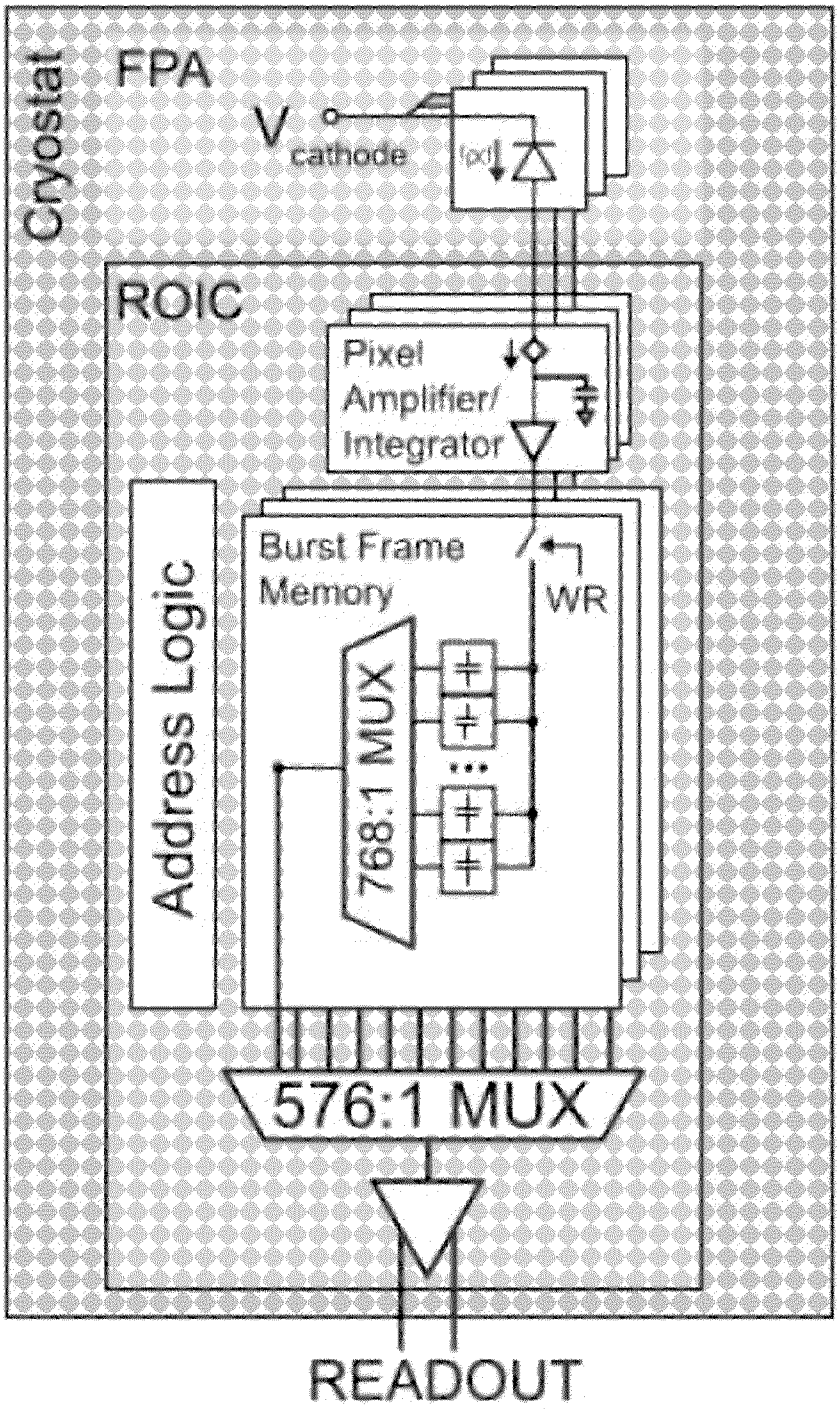
Cryostat
FPA
V
cathode
I(x,t)
ROIC
Pixel
Amplifier/
Integrator
Address Logic
Burst Frame
Memory
WR
768:1 MUX
576:1 MUX
READOUT

FIG. 1C

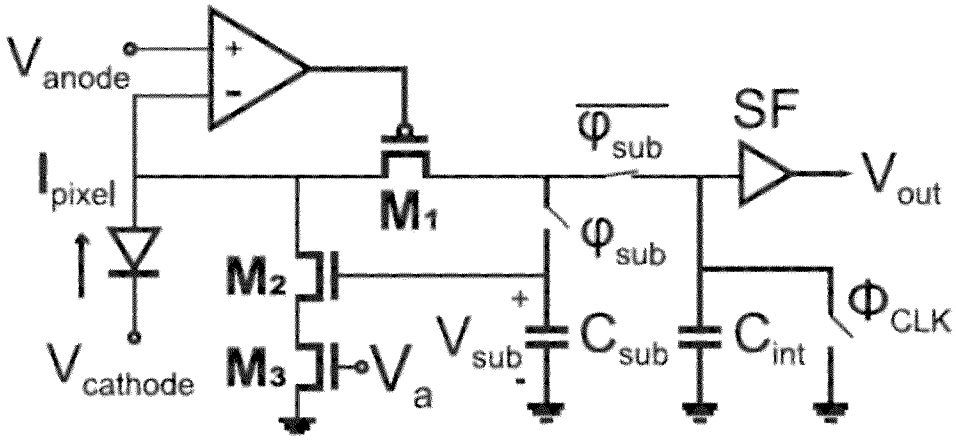
V anode
+
-
I pixel
M1
φ sub
SF
V out
φ sub
M2
Φ CLK
+
V sub
C sub
C int
V cathode
M3
V a
-

FIG. 2A

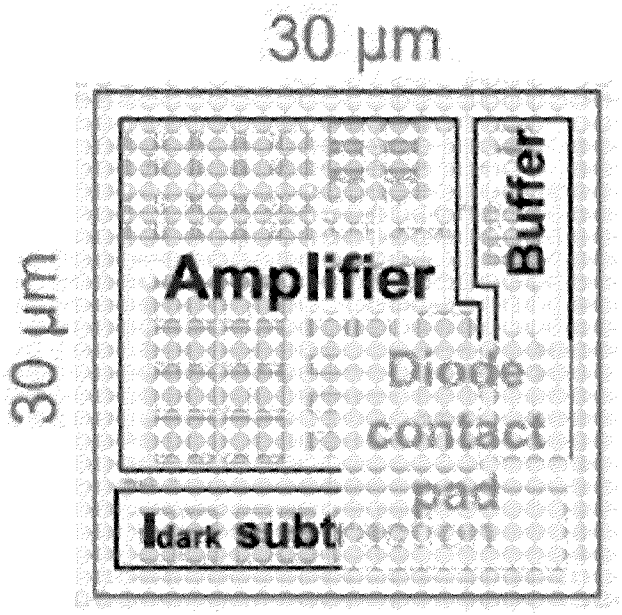
30 µm
30 µm
Amplifier
Buffer
Diode
contact
pad
Idark subt

FIG. 2B

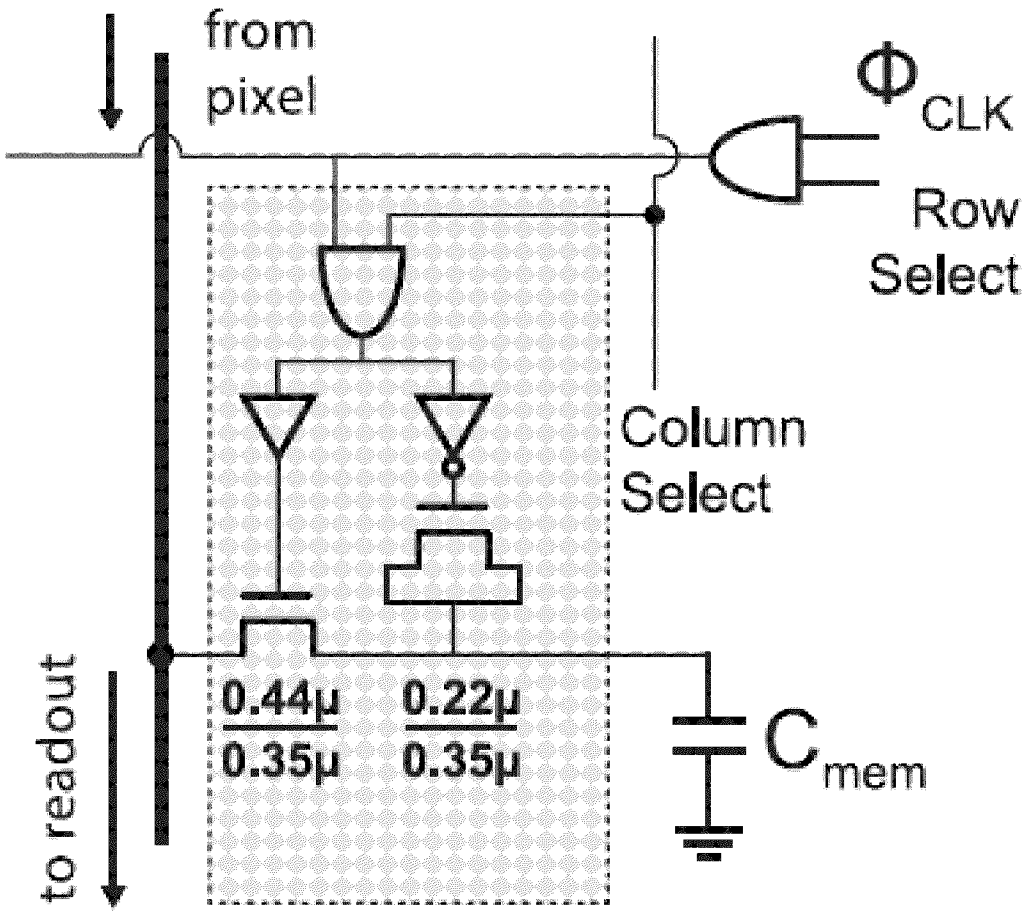
from
pixel
Φ CLK
Row
Select
Column
Select
0.44µ
0.35µ
0.22µ
0.35µ
C mem
to readout

FIG. 2C

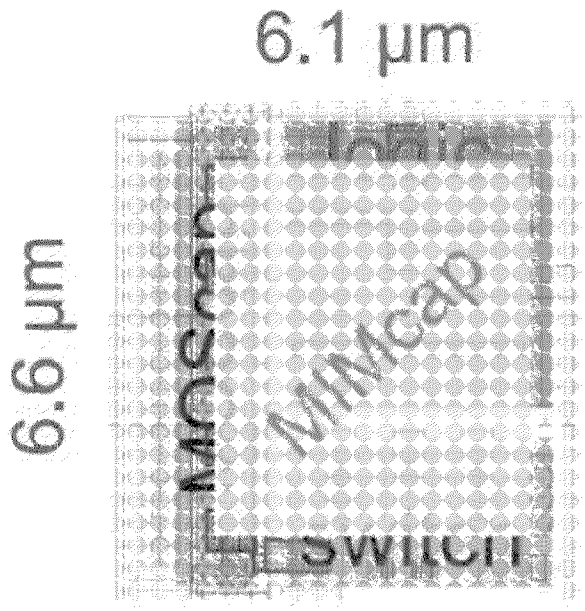
6.1 µm
6.6 µm
MoCap
MiMCap
SWITCH

FIG. 2D

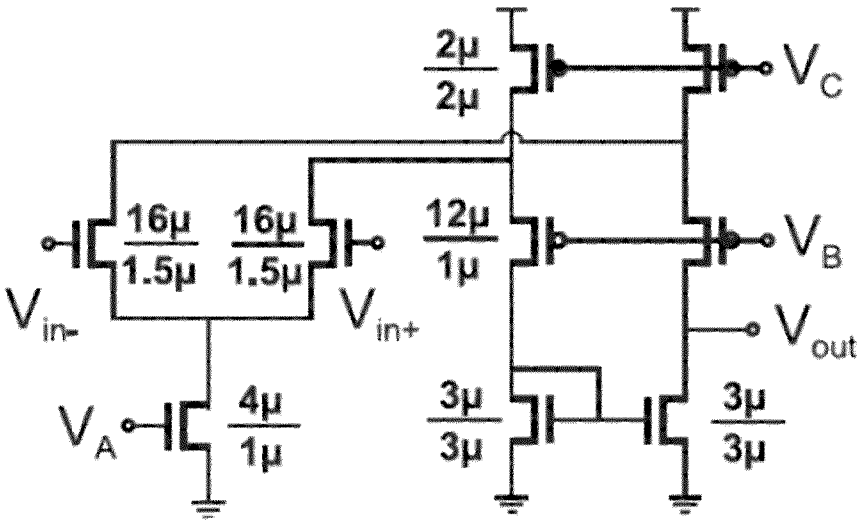
2µ
2µ
V_C
16µ
1.5µ
16µ
1.5µ
12µ
1µ
V_B
V_{in-}
V_{in+}
V_{out}
V_A
4µ
1µ
3µ
3µ
3µ
3µ

FIG. 2E

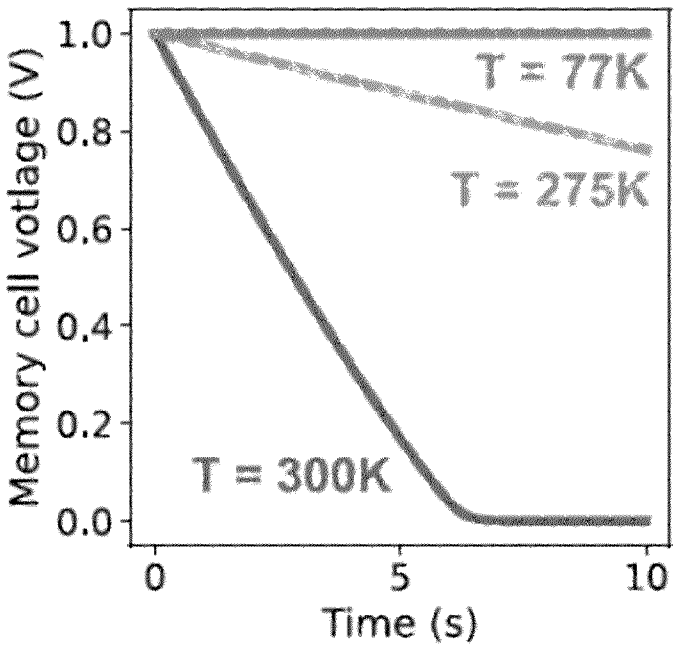
Memory cell voltage (V)
1.0
0.8
0.6
0.4
0.2
0.0
T = 77K
T = 275K
T = 300K
0
5
10
Time (s)

FIG. 2F

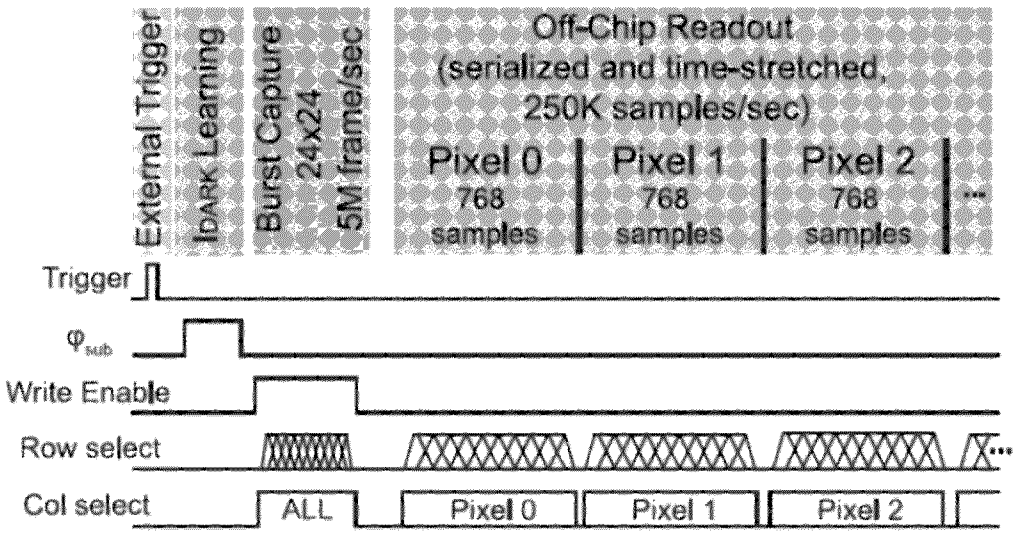
External Trigger
IDARK Learning
Burst Capture
24x24
5M frame/sec
Off-Chip Readout
(serialized and time-stretched,
250K samples/sec)
Pixel 0
768
samples
Pixel 1
768
samples
Pixel 2
768
samples
Trigger
φsub
Write Enable
Row select
Col select
ALL
Pixel 0
Pixel 1
Pixel 2

FIG. 3A

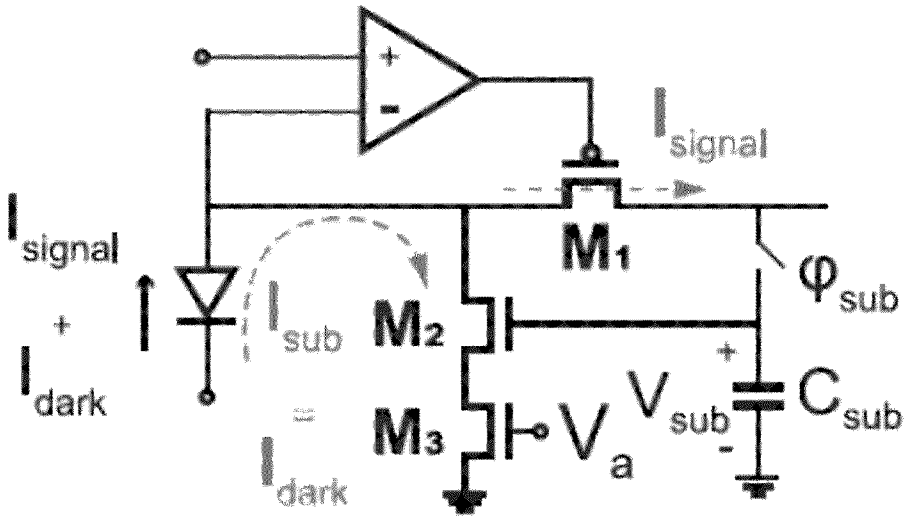
+
-
I signal
I signal
+
I dark
I sub
M1
M2
M3
φ sub
V a
V sub
C sub
+
-
=
I dark

FIG. 3B

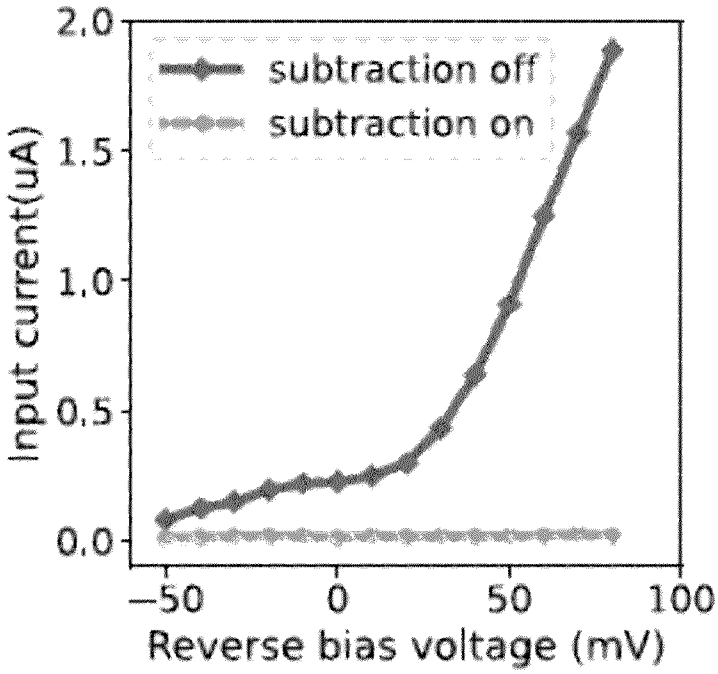
subtraction off
subtraction on
Input current(uA)
2.0
1.5
1.0
0.5
0.0
−50
0
50
100
Reverse bias voltage (mV)

FIG. 3C

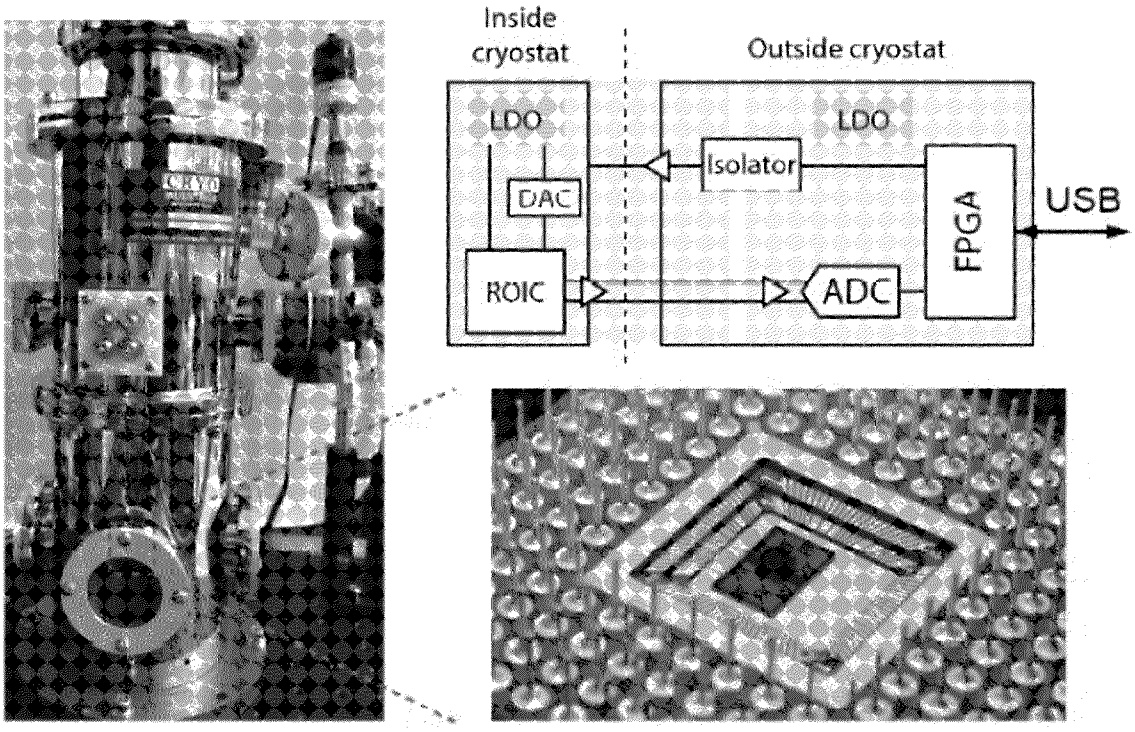
Inside cryostat
Outside cryostat
LDO
LDO
Isolator
DAC
FPGA
USB
ROIC
ADC

FIG. 4

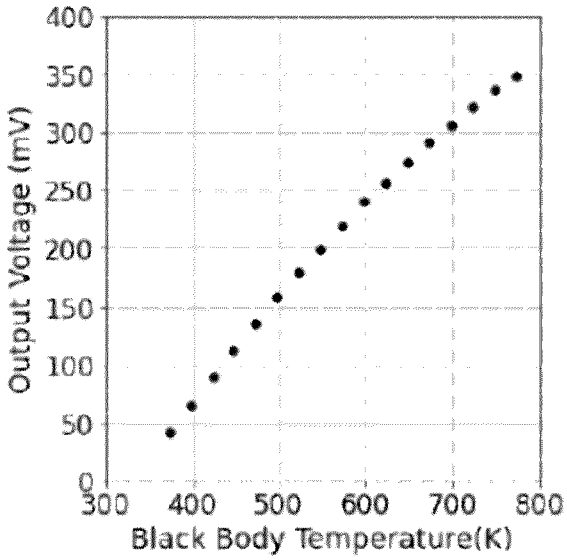
Output Voltage (mV)
400
350
300
250
200
150
100
50
0
300
400
500
600
700
800
Black Body Temperature(K)

FIG. 5A

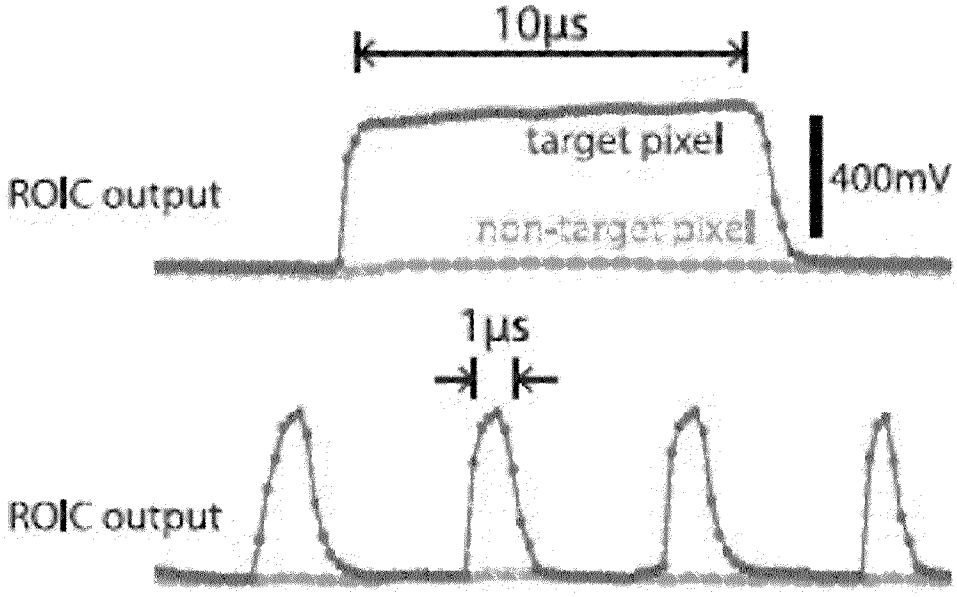
10µs
target pixel
400mV
ROIC output
non-target pixel
1µs
ROIC output

FIG. 5B

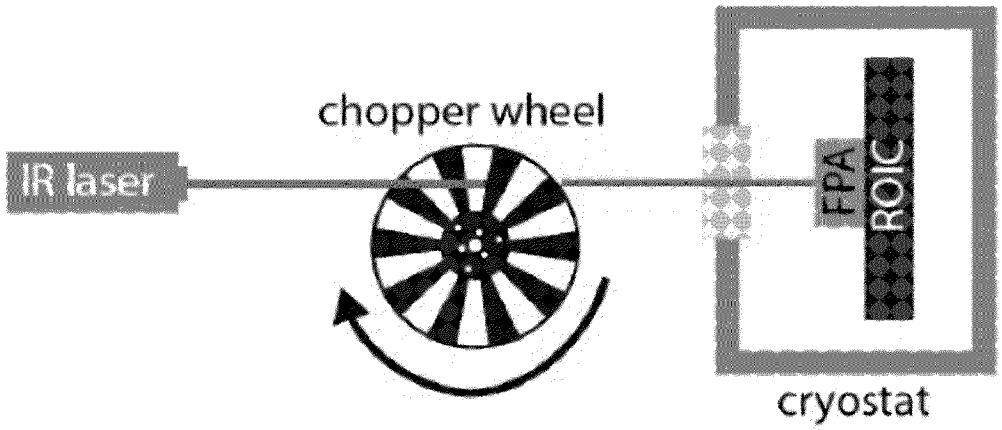
chopper wheel
IR laser
FPA
ROIC
cryostat

FIG. 6A

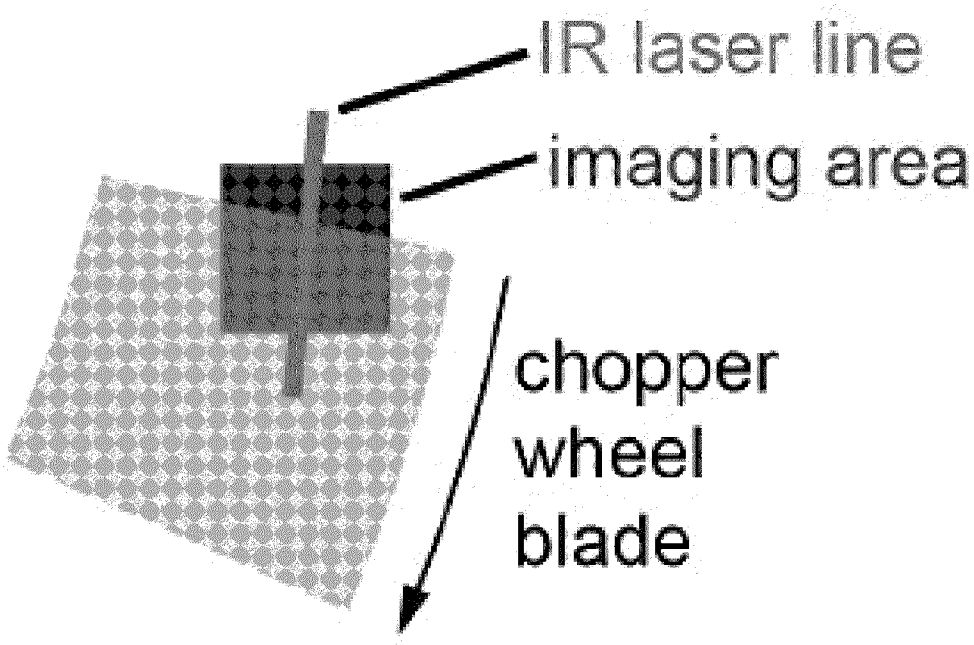
IR laser line
imaging area
chopper
wheel
blade

FIG. 6B

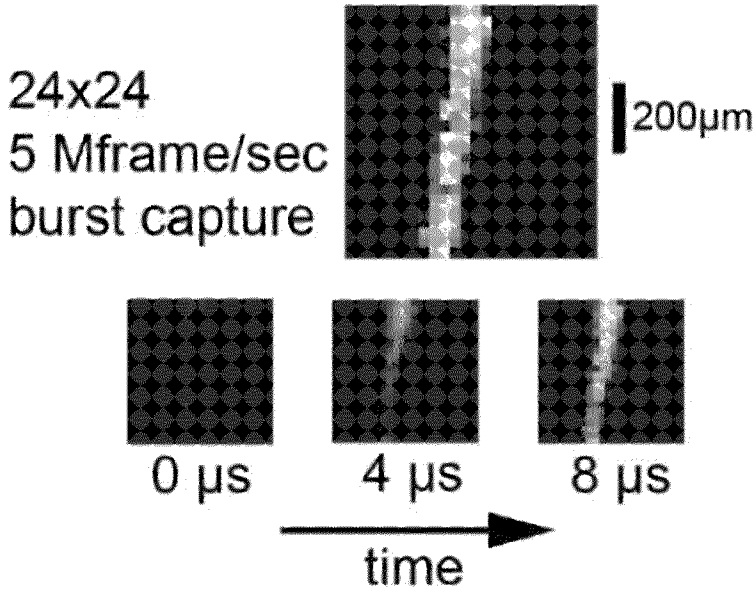
24x24
5 Mframe/sec
burst capture
200μm
0 μs
4 μs
8 μs
time

FIG. 6C

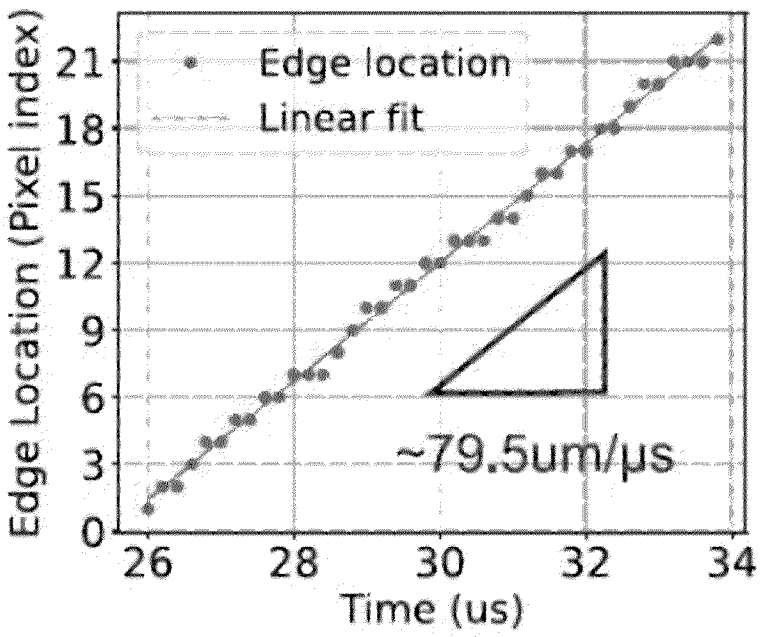
Edge location
Linear fit
~79.5um/μs
Edge Location (Pixel index)
Time (us)
0
3
6
9
12
15
18
21
26
28
30
32
34

FIG. 6D

TABLE I
COMPARISON TABLE WITH STATE-OF-THE-ART HIGH-SPEED GLOBAL SHUTTER IMAGERS

	This work	TELOPS FAST Mk3	JSSC 2015 [10]	ISSCC 2013 [11]	RSI 2000 [12]	JSSC 2012 [3]
Optical wavelengths	MWIR/LWIR ($3\,\mu m - 10\,\mu m$)	SWIR/MWIR ($1.5\,\mu m - 5\,\mu m$)	MWIR ($1.4\,\mu m - 7.3\,\mu m$)	LWIR ($8\,\mu m - 12\,\mu m$)	MWIR/LWIR ($3\,\mu m - 10\,\mu m$)	Visible/NIR (350 nm – 950 nm)
Capture rate (frames/sec)	5,000,000	100,000	2,000	60	1,000,000	10,000,000
Resolution	24×24	64×4 (at max speed)	80×80	640×480	8×8	400×250
Pixel rate (Mpixel/sec)	2,880	25.6	6.4	18.43	64	1,000,000
Burst frame depth	768 (on-chip)	–	–	–	25,000 (external)	124 (on-chip)
Detector pitch	$30\,\mu m \times 30\,\mu m$	$30\,\mu m \times 30\,\mu m$	$135\,\mu$m $\times$ $135\,\mu$m	$17\mu m \times 17\mu m$	$130\,\mu m \times 130\,\mu m$	$32\,\mu m \times 32\,\mu m$
Power per pixel	$434\,\mu W$	–	$< 1\,\mu W$ (static)	$0.55\,\mu W$	–	$195\,\mu W$
Operating temperature	Cryogenic ($77^\circ K$)	Cooled	Room temperature	Room temperature	Cryogenic ($77^\circ K$)	Room temperature
Technology	180nm + HgCdTe	InSb	350nm + PbSe	μbolometer + 180nm	HgCdTe + PCB	180nm

FIG. 7

TABLE II
ROIC PERFORMANCE SUMMARY

Technology node	180nm 1P6M CMOS
Die size	6.5mm × 4.1mm
Pixel pitch	$30\,\mu m$
Max capacity	$2,800\,ke$
Conversion Gain	$0.21\mu V/e$
RMS noise (ROIC only)	$1.37\,ke$ (1 cell/sample) $1\,ke$ (16 cells/sample)
RMS noise (ROIC + FPA)	$2.4\,ke$ (1 cell/sample) $2.28ke$ (16 cells/sample)
FPN	0.3% of full capacity
Dynamic range	$61.78\,dB$
SNR	$50.2\,dB$
Power consumption	$0.25W$ @ 5M fps $434\mu W$ per pixel

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2024/056402

A. CLASSIFICATION OF SUBJECT MATTER

IPC: ***H04N 23/23*** (2024.01); ***H04N 23/52*** (2024.01); *H04N 23/20* (2024.01); *G03B 17/55* (2024.01)

CPC: ***H04N 23/23; H04N 23/52;*** *H04N 23/20; G03B 17/55*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History Document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History Document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History Document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	US 2007/0081162 A1 (ROLLER ET AL.) 12 April 2007 (12.04.2007)	
Y	entire document, especially FIG. 2, FIG. 4, para [0002], [0034], [0044]	1-5, 10-11
A	entire document	6-9, 12-15
	US 2006/0097146 A1 (STROBEL) 11 May 2006 (11.05.2006)	
Y	entire document, especially FIG. 1, para [0024], [0032]	1-5, 10-11
A	entire document	6-9, 12-15
	US 5,382,797 A (KUNIMOTO ET AL.) 17 January 1995 (17.01.1995)	
Y	entire document, especially FIG. 1, col 1, ln 53-61, col 3, ln 47-col 4, ln 1	5, 11
	US 5,382,797 A (KUNIMOTO ET AL.) 17 January 1995 (17.01.1995)	
A	entire document	6-9, 12-15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 January 2025 (03.01.2025)	**21 January 2025 (21.01.2025)**

Name and mailing address of the ISA/US	Authorized officer
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