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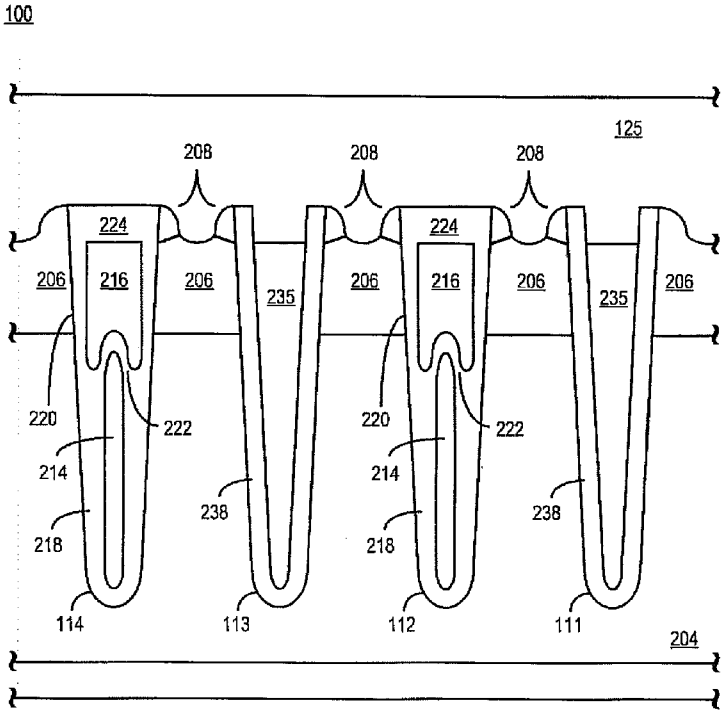

FIG. 2

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(57) Abstract: A semiconductor device includes a first group of trench-like structures and a second group of trench-like structures. Each trench-like structure in the first group includes a gate electrode contacted to gate metal and a source electrode contacted to source metal. Each of the trench-like structures in the second group is disabled. The second group of disabled trench-like structures is interleaved with the first group of trench-like structures.

SEMICONDUCTOR DEVICE

RELATED U.S. APPLICATION

This application claims priority to U.S. Provisional Application No. 61/487,627, titled "Semiconductor Device Having Reduced Gate Charges and Superior Figure of Merit," filed on May 18, 2011, which is hereby incorporated by reference in its entirety.

BACKGROUND

In order to realize an energy-efficient power conversion system, power MOSFETs (metal-oxide-semiconductor field-effect transistors) used as core switches rely on low gate charges as well as low on-state resistances. For example, in a DC-to-DC (direct current) converter such as a synchronous buck converter, two MOSFETs are used, one as the "high side" MOSFET and the other as the "low side" MOSFET. The high side MOSFET is controlled by an external enable signal and sources current to a load, while the low side MOSFET connects or disconnects the load to ground and thus sinks current from the load.

There are some specific features and requirements for each of the high side and low side MOSFETs. For example, while lower on-state resistances are

desired for the low side MOSFET, high speed switching characteristics having lower gate charges are desired for the high side MOSFET.

One of the widely used metrics for MOSFET performance is a FOM (figure of merit) defined as the gate charge multiplied by the drain-to-source resistance at the specified gate voltages. A lower value for this figure of merit translates to better performance for high side MOSFETs.

A MOSFET that can achieve lower gate charges and hence a lower value for the figure of merit would be both useful and beneficial as, for example, a high side MOSFET in a DC-to-DC converter.

SUMMARY

Embodiments according to the present invention provide efficient and novel metal/insulator/semiconductor (MIS) devices (e.g., MOSFETs) having lower gate charges and lower FOM values.

In one embodiment, a semiconductor device (e.g., a MOSFET) includes a first group of trench-like structures and a second group of trench-like structures (for simplicity, the trench-like structures may be referred to below as trenches). Each of the trenches in the first group includes a gate electrode that is contacted to gate metal, and also includes a source electrode that is contacted to source metal and is insulated from the gate electrode. Each of the trenches in the second group is disabled.

In one embodiment, a layer of the source metal traverses the first group of utilized trenches and the second group of disabled trenches. In such an embodiment, each of the disabled trenches includes a single polysilicon region. The polysilicon regions in each of the disabled trenches are substantially in the same plane as the source and gate electrodes in the utilized trenches. The polysilicon regions in each of the disabled trenches are contacted to the layer of source metal inside the active core region of the semiconductor device and are also contacted to the gate metal. In contrast, in the utilized trenches, the gate electrode is situated between the source electrode and the layer of source metal and is insulated from the layer of source metal but is contacted to the gate metal.

Also, in the utilized trenches, the source electrode is contacted to the source metal outside the active core region but is insulated from the layer of source metal inside the active core region.

The second group of disabled trenches is interleaved with the first group of utilized trenches. In one embodiment, the first group of utilized trenches and the second group of disabled trenches are interleaved in alternating fashion. That is, in one embodiment, every other trench is disabled. In other embodiments, every third trench is disabled, or every fourth trench is disabled, and so on.

As an unexpected benefit, if one-half of the trenches are disabled, for example, then the drain-to-source resistance increases by less than a factor of two instead of by a factor of two as expected, while the gate charge decreases by about a factor of two. As a result, the value of the FOM is advantageously reduced by disabling selected trenches as described above.

In one embodiment, the semiconductor device features described above are implemented in a MOSFET. In one such embodiment, those features are implemented in a high side MOSFET coupled to a low side MOSFET in a DC-to-DC converter.

These and other objects and advantages of the present invention will be recognized by one skilled in the art after having read the following detailed description, which are illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. Like numbers denote like elements throughout the drawings and specification.

Figure 1 shows a top-down view of a portion of a semiconductor device in an embodiment according to the present invention.

Figure 2 is a cross-sectional view showing elements of a semiconductor device in embodiments according to the present invention.

Figure 3 shows a top-down view of a portion of a semiconductor device in an embodiment according to the present invention.

Figure 4 is a flowchart listing masks used in a process for fabricating semiconductor devices in an embodiment according to the present invention.

DETAILED DESCRIPTION

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well-known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Some portions of the detailed descriptions that follow are presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations for fabricating or operating semiconductor devices. These descriptions and representations are the means used by those skilled in the art of semiconductor device fabrication to most effectively convey the substance of their work to others skilled in the art. In the present application, a procedure, logic block, process, or the like, is conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. It should be borne in mind, however, that all of these and similar terms are to be associated with the appropriate physical quantities and are merely convenient labels applied to these quantities. Unless specifically stated otherwise as apparent from the following discussions, it is appreciated that throughout the present application, discussions utilizing terms such as “forming,” “performing,” “producing,” “depositing,” “etching”

or the like, refer to actions and processes of semiconductor device fabrication or operation.

Figures are not drawn to scale, and only portions of the structures, as well as the various layers that form those structures, may be shown in the figures. Furthermore, fabrication processes and steps may be performed along with the processes and steps discussed herein; that is, there may be a number of process steps before, in between and/or after the steps shown and described herein. Importantly, embodiments in accordance with the present invention can be implemented in conjunction with these other (perhaps conventional) structures, processes and steps without significantly perturbing them. Generally speaking, embodiments in accordance with the present invention can replace portions of a conventional device or process without significantly affecting peripheral structures, processes and steps.

The term "trench," when discussed in the context of fabrication of a semiconductor device, generally refers to an empty volume formed within a material. Such a trench may be subsequently filled with another material or materials. The term "trench," when discussed in the context of a fabricated semiconductor device, generally refers to the structure formed within the formerly empty trench. A trench may also be referred to herein as a stripe. The meaning of the term "trench" in the discussion below will be clear within the context of the discussion.

Embodiments according to the present disclosure pertain to new structures to achieve lower gate charges and lower FOM values in semiconductor devices such as MOSFET devices that can be used as high side MOSFETs in, for example, DC-to-DC converters such as synchronous buck converters.

Figure 1 is a top-down view showing certain elements of a semiconductor device 100 in an embodiment according to the present invention. Not all elements that might be included in a semiconductor device are shown in Figure 1. Multiple levels are depicted in Figure 1; that is, for example, the source metal layer 125 is actually over (on top of) the stripes 111-116.

In the example of Figure 1, the device 100 includes a number of stripes (or cells) 111-116 that are essentially parallel to one another in the active core region 105. The active core region 105 is the region bounded by the dashed lines in Figure 1.

As will be described further in conjunction with Figure 2, each of the stripes 111-116 is a trench-like structure. Also, as will be described further in conjunction with Figure 2, some of the stripes are disabled while others are not. The disabled stripes are electrically and physically connected to the source metal layer 125 inside the active core region 105, and are also electrically and

physically connected to the gate metal layer 135 via the gate contact 137. The utilized stripes (those that are not disabled) are insulated from the source metal layer 125 inside the active core region 105, but include a source electrode (see Figure 2) that is electrically and physically connected to the source metal layer 125 via the source contact 127 outside the active core region, and also include a gate electrode (see Figure 2) that is electrically and physically connected to the gate metal layer 135 via the gate contact 137.

Figure 2 is a cross-sectional view (along the line A-A in Figure 1) of the device 100 in an embodiment according to the present invention. Not all elements that might be included in a semiconductor device are shown in Figure 2.

Four trench-like structures 111-114 are shown. For simplicity of discussion, the trench-like structures may be referred to simply as trenches in the discussion below. In the orientation of Figure 2, as in the orientation of Figure 1, the trenches 111-114 are parallel to one another.

In the example of Figure 2, the device 100 includes a first (or buffer) epitaxial layer 202 and a second epitaxial layer 204. There may also be a drain region (not shown) below the first epitaxial layer 202. The trenches 111-114 extend into the second epitaxial layer 204.

A body region 206 (e.g., a p-doped region) is formed between neighboring trenches as shown. Also, source regions 208 (e.g., n+ doped regions) are formed between neighboring trenches as shown. The source metal layer 125 extends across (traverses) the trenches 111-114. As described below, the source metal layer 125 is isolated from the electrodes in selected trenches (e.g., the trenches 112 and 114) in the active region 105 (Figure 1) of the device 100 but is in contact with the electrodes in other selected trenches (e.g., the trenches 111 and 113) in the active core region. Accordingly, in the example of Figure 2, the trenches 111 and 113 are disabled while the trenches 112 and 114 are utilized (not disabled).

The trenches 112 and 114 may be referred to as split gates. Each of the trenches 112 and 114 includes a first polysilicon (poly-1) region 214, also referred to as a source electrode or a shield electrode. Each of the trenches 112 and 114 also includes a second polysilicon (poly-2) region 216, also referred to as a gate electrode. The source electrodes 214 are separated from the adjacent epitaxial layer 204 by a shield oxide 218, and the gate electrodes 216 are separated from the adjacent epitaxial layer 204 by a gate oxide 220. The source electrodes 214 in the trenches 112 and 114 are insulated from the gate electrodes 216 in the trenches 112 and 114 by an intervening oxide layer 222. In the trenches 112 and 114, the gate electrodes 216 are situated between the source electrodes 214 and the source metal layer 125. The gate electrodes 216 are insulated from the source metal layer 125 by an intervening isolation oxide

layer 224. With reference also to Figure 1, the source electrodes 214 in the trenches 112 and 114 are electrically and physically contacted to the source metal layer 125 via the source contact 127, and the gate electrodes 216 inside the trenches 112 and 114 are electrically and physically contacted to the gate metal layer 135 via the gate contact 137 (Figure 1).

In the embodiment of Figure 2, each of the disabled trenches 111 and 113 includes a single polysilicon (poly-1) region 235 contacted to the source metal layer 125 and to the gate metal layer 135 (Figure 1). The poly-1 regions 235 of the disabled trenches 111 and 113 are substantially in the same plane as the source electrodes 214 and the gate electrodes 216 in the utilized trenches. That is, in the orientation of Figure 2, the tops of the poly-1 regions 235 roughly coincide with the tops of the gate electrodes 216, and the bottoms of the poly-1 regions 235 roughly coincide with the bottoms of the source electrodes 214. The poly-1 regions 235 are separated from the adjacent epitaxial layer 204 by an oxide layer 238.

Significantly, the poly-1 regions 235 are not insulated from the source metal layer 125; the source metal layer 125 is electrically and physically in contact with the poly-1 regions 235. Furthermore, with reference also to Figure 1, the poly-1 regions 235 in the trenches 111 and 113 are also electrically and physically contacted to the source metal layer 125 via the source contact 127 and to the gate metal layer 135 via the gate contact 137.

Thus, in the example of Figure 2, half of the cells/stripes/trenches are utilized (e.g., the trenches 112 and 114) and half of the cells/stripes/trenches are disabled (e.g., the trenches 111 and 113). In other words, the utilized cells/stripes/trenches are interleaved with the disabled cells/stripes/trenches in alternating fashion, such that every other cell/stripe/trench is disabled. This is shown in Figure 3, which represents a top-down view of the device 100. In other embodiments, the core cells/stripes can be disabled by one-third (every third cell/stripe/trench disabled), one-fourth, one-fifth, and so on.

As mentioned above, a widely used metric for MOSFET performance is a FOM defined as the gate charge multiplied by the drain-to-source resistance at the specified gate voltages. A lower value for this FOM translates to better performance for high side MOSFETs.

Utilizing a core area as large as before, it might be expected that, if half of the core cells/stripes/trenches are utilized and the other half of the core cells/stripes/trenches are disabled, then the gate charges would decrease by half and the resistances would increase by a factor of two. However, because there is current crowding in the drift region for high density cell devices such as those described herein, some series resistances from that region are experienced. By disabling some (e.g., half) of the core cells/stripes/trenches, the carriers flowing through one side channel of the core cell/stripe use the whole drift region, and so

less current crowding for the flow of carriers and less series resistance from that region are experienced. Consequently, in actuality, the overall drain-to-source resistances increase less than a factor of two if half of the core cells/stripes/trenches are disabled.

On the other hand, the gate charges decrease proportionally according to the active core cell area. As a result of the combined effects on the drain-to-source resistance and the gate charge, a better FOM can be achieved using the approach described in the present disclosure.

This is illustrated by the results included in Table 1. "Rsp4.5V(Core)" stands for the specific resistance between the drain and the source at a gate voltage of 4.5V of a single core cell/stripe. "Rds(on) @4.5V typical" demonstrates final product resistance between the drain and the source at a gate voltage of 4.5V in a Power PAK® 1212 package. "Qgsp4.5V" stands for the specific gate charges per unit active area at a gate voltage of 4.5V. "Qg4.5V" shows a value of the total gate charges at a gate voltage of 4.5V. The FOM is the product of Qg4.5V and Rds(on) @4.5V typical. Embodiments according to the present disclosure improve FOM values by about 32 percent if half of the core cells/stripes/trenches are disabled.

Table 1 – Example Results

	Units	Conventional Art	Embodiment of Present Disclosure	Percent Change
Rsp4.5V (core)	$m\Omega \cdot mm^2$	4.43	6.22	40%
Rds(on) @4.5V (typical)	$m\Omega$	2.2	2.8	28%
Qgsp4.5V	nC/mm^2	8.3	4.4	-47%
Qg4.5V	nC	24.1	12.8	-47%
FOM	Qg4.5*Rds4.5	53	36	-32%

Figure 4 is a flowchart 400 showing the sequence of masks that are used to form the disabled stripes/trenches and the utilized stripes/trenches in an embodiment according to the present invention. Other masks and fabrication process steps may be utilized with the masks included in the following discussion. The discussion below is intended to highlight changes in the fabrication process that are introduced to form the disabled trenches referred to above. Figure 4 is discussed with reference also to Figure 2.

In block 401, a trench mask is utilized to form empty trenches 111-114. In block 402, after poly-1 is deposited in the trenches, a shield (source) poly etch block mask is configured such that the poly-1 in the disabled trenches 111 and 113 is not exposed to an etch while the poly-1 in the utilized trenches 112 and 114 is exposed to the etch. Thus, the poly-1 in the disabled trenches 111 and

113 is not etched back, but the poly-1 in the utilized trenches 112 and 114 is etched back to form the source electrodes 214.

In block 403, an active mask is utilized to prevent the thick oxide layer 238 lining the disabled trenches 111 and 113 from being thinned and to prevent poly-2 from being deposited into the disabled trenches. The trenches 112 and 114 are not protected by the active mask, so that the gate oxide 220 is thinned prior to poly-2 deposition in the trenches 112 and 114 to form the gate electrodes 216.

In block 404, a gate poly etch block mask is used during etch back of the poly-2 regions. In block 405, a source implant mask is utilized for proper deposition of the source regions 208. In block 406, a body implant mask is utilized for proper deposition of the body regions 206. In blocks 407, 408, 409, and 410, poly contact, core contact, metal etch, and pad masks are respectively utilized to form the contacts 135 and 137 and to contact the electrodes 214, 216, and 235 with the source metal and gate metal.

Thus, in order to form the disabled trenches 111 and 113, a shield poly etch block mask (block 402) and an active mask (block 403) are introduced or modified. Accordingly, the disabled trenches can be formed without significantly perturbing the fabrication process.

In summary, embodiments of semiconductor devices, and embodiments of methods for fabricating such devices, are described. Embodiments according to the invention can be used in high density trench power MOS transistors and in the charge balance MOSFET family with a split gate structure. Embodiments according to the invention can be applied in high side DC-DC converter applications.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

Broadly, this writing discloses semiconductor devices. It further discloses a semiconductor device which includes a first group of trench-like structures and a second group of trench-like structures. Each trench-like structure in the first group includes a gate electrode contacted to gate metal and a source electrode contacted to source metal. Each of the trench-like structures in the second group

is disabled. The second group of disabled trench-like structures is interleaved with the first group of trench-like structures.

All elements, parts and steps described herein are preferably included. It is to be understood that any of these elements, parts and steps may be replaced by other elements, parts and steps or deleted altogether as will be obvious to those skilled in the art.

CONCEPTS:

This writing presents at least the following concepts.

Concept 1. A semiconductor device comprising:

a first plurality of trench-like structures, each trench-like structure in said first plurality comprising a gate electrode contacted to gate metal and a source electrode contacted to source metal; and

a second plurality of disabled trench-like structures interleaved with said first plurality of trench-like structures.

Concept 2. The semiconductor device of Concept 1 wherein each of said disabled trench-like structures comprises a single polysilicon region contacted to said source metal and contacted to gate metal.

Concept 3. The semiconductor device of Concept 2 wherein said single polysilicon region is substantially in the same plane as said source electrode and said gate electrode.

Concept 4. The semiconductor device of Concept 1 wherein said first plurality and said second plurality of trench-like structures are interleaved in alternating fashion.

Concept 5. The semiconductor device of Concept 1 wherein at least two

successive trench-like structures of said first plurality are separated from another trench-like structure of said first plurality by a disabled trench-like structure.

Concept 6. The semiconductor device of Concept 1 comprising a layer of said source metal that traverses said first plurality of trench-like structures and said second plurality of trench-like structures, wherein said source electrode is contacted to said source metal outside an active core region of said semiconductor device and wherein said source electrode is insulated from said layer of source metal inside said active core region, and wherein said disabled trench-like elements are contacted to said layer of source metal inside said active core region.

Concept 7. The semiconductor device of Concept 1 comprising a layer of said source metal that traverses said first plurality of trench-like structures and said second plurality of trench-like structures, wherein said gate electrode is situated between said source electrode and said layer of source metal, and wherein said gate electrode is insulated from said layer of source metal.

Concept 8. The semiconductor device of Concept 1 wherein said first and second pluralities of trench-like structures are arranged in a pattern selected from the group consisting of: one out of two trench-like structures are disabled; one out of three trench-like structures are disabled; one out of four trench-like structures are disabled.

Concept 9. The semiconductor device of Concept 1 comprising a metal-oxide-semiconductor field-effect transistor (MOSFET).

Concept 10. The semiconductor device of Concept 9 wherein said MOSFET comprises a high side MOSFET that is coupled to a low side MOSFET in a DC-to-DC converter.

Concept 11. A semiconductor device comprising:

a first split gate structure comprising a first electrode region and a second electrode region;

a second structure parallel to said first split gate structure and comprising a polysilicon region in contact with gate metal; and

a source metal layer that is insulated from said first split gate structure within an active region of said semiconductor device and is in contact with said polysilicon region within said active region.

Concept 12. The semiconductor device of Concept 11 wherein said first electrode region comprises a source electrode contacted to source metal outside said active region, and wherein said second electrode comprises a gate electrode contacted to gate metal outside said active region.

Concept 13. The semiconductor device of Concept 12 wherein said gate electrode is situated between said source electrode and said source metal layer, and wherein said gate electrode is insulated from said source metal layer and also from said source electrode.

Concept 14. The semiconductor device of Concept 11 wherein said polysilicon region is substantially in the same plane as said first electrode region and said second electrode region.

Concept 15. The semiconductor device of Concept 11 further comprising a second split gate structure comprising two electrode regions, wherein said second structure is situated between said first split gate structure and said second split gate structure.

Concept 16. The semiconductor device of Concept 11 further comprising at least two successive split gate structures, each comprising two electrode regions, wherein said second structure is situated between said first split gate structure and said two successive split gate structures.

Concept 17. A semiconductor device comprising:

a first trench-like structure comprising a first polysilicon region and a second polysilicon region that are insulated from each other by an oxide region;

a second trench-like structure parallel to said first trench-like structure and comprising a third polysilicon region; and

a source metal layer that traverses both said first trench-like structure and said second trench-like structure, wherein said second polysilicon region is situated between said first polysilicon region and said source metal layer, and wherein said source metal layer is insulated from said second polysilicon region and is in contact with said third polysilicon region.

Concept 18. The semiconductor device of Concept 17 wherein said first polysilicon region comprises a source electrode contacted to said source metal layer, wherein said second polysilicon region comprises a gate electrode contacted to gate metal, and wherein further said third polysilicon region is contacted to said source metal layer and to said gate metal.

Concept 19. The semiconductor device of Concept 17 wherein said third polysilicon region is in the same plane as said first polysilicon region and said second polysilicon region.

Concept 20. The semiconductor device of Concept 17 further comprising a third trench-like structure comprising two polysilicon regions, wherein said second trench-like structure is situated between said first trench-like structure and said third trench-like structure.

Concept 21. The semiconductor device of Concept 17 further comprising at least two successive trench-like structures parallel to said first trench-like structure and said second trench-like structure, each of said successive trench-like structures comprising two electrode regions, wherein said second trench-like structure is situated between said first trench-like structure and said two successive trench-like structures.

CLAIMS

What is claimed is:

1. A semiconductor device comprising:

a first plurality of trench-like structures, each trench-like structure in said first plurality comprising a gate electrode contacted to gate metal and a source electrode contacted to source metal; and

a second plurality of disabled trench-like structures interleaved with said first plurality of trench-like structures.

2. The semiconductor device of Claim 1 wherein each of said disabled trench-like structures comprises a single polysilicon region contacted to said source metal and contacted to gate metal.

3. The semiconductor device of Claim 2 wherein said single polysilicon region is substantially in the same plane as said source electrode and said gate electrode.

4. The semiconductor device of Claim 1 wherein said first plurality and said second plurality of trench-like structures are interleaved in alternating fashion.

5. The semiconductor device of Claim 1 wherein at least two successive trench-like structures of said first plurality are separated from another trench-like

structure of said first plurality by a disabled trench-like structure.

6. The semiconductor device of Claim 1 comprising a layer of said source metal that traverses said first plurality of trench-like structures and said second plurality of trench-like structures, wherein said source electrode is contacted to said source metal outside an active core region of said semiconductor device and wherein said source electrode is insulated from said layer of source metal inside said active core region, and wherein said disabled trench-like elements are contacted to said layer of source metal inside said active core region.

7. The semiconductor device of Claim 1 comprising a layer of said source metal that traverses said first plurality of trench-like structures and said second plurality of trench-like structures, wherein said gate electrode is situated between said source electrode and said layer of source metal, and wherein said gate electrode is insulated from said layer of source metal.

8. The semiconductor device of Claim 1 wherein said first and second pluralities of trench-like structures are arranged in a pattern selected from the group consisting of: one out of two trench-like structures are disabled; one out of three trench-like structures are disabled; one out of four trench-like structures are disabled.

9. The semiconductor device of Claim 1 comprising a metal-oxide-semiconductor field-effect transistor (MOSFET).

10. The semiconductor device of Claim 9 wherein said MOSFET comprises a high side MOSFET that is coupled to a low side MOSFET in a DC-to-DC converter.

11. A semiconductor device comprising:

a first split gate structure comprising a first electrode region and a second electrode region;

a second structure parallel to said first split gate structure and comprising a polysilicon region in contact with gate metal; and

a source metal layer that is insulated from said first split gate structure within an active region of said semiconductor device and is in contact with said polysilicon region within said active region.

12. The semiconductor device of Claim 11 wherein said first electrode region comprises a source electrode contacted to source metal outside said active region, and wherein said second electrode comprises a gate electrode contacted to gate metal outside said active region.

13. The semiconductor device of Claim 12 wherein said gate electrode is situated between said source electrode and said source metal layer, and wherein

said gate electrode is insulated from said source metal layer and also from said source electrode.

14. The semiconductor device of Claim 11 wherein said polysilicon region is substantially in the same plane as said first electrode region and said second electrode region.

15. The semiconductor device of Claim 11 further comprising a second split gate structure comprising two electrode regions, wherein said second structure is situated between said first split gate structure and said second split gate structure.

16. The semiconductor device of Claim 11 further comprising at least two successive split gate structures, each comprising two electrode regions, wherein said second structure is situated between said first split gate structure and said two successive split gate structures.

17. A semiconductor device comprising:

a first trench-like structure comprising a first polysilicon region and a second polysilicon region that are insulated from each other by an oxide region;

a second trench-like structure parallel to said first trench-like structure and comprising a third polysilicon region; and

a source metal layer that traverses both said first trench-like structure and

said second trench-like structure, wherein said second polysilicon region is situated between said first polysilicon region and said source metal layer, and wherein said source metal layer is insulated from said second polysilicon region and is in contact with said third polysilicon region.

18. The semiconductor device of Claim 17 wherein said first polysilicon region comprises a source electrode contacted to said source metal layer, wherein said second polysilicon region comprises a gate electrode contacted to gate metal, and wherein further said third polysilicon region is contacted to said source metal layer and to said gate metal.

19. The semiconductor device of Claim 17 wherein said third polysilicon region is in the same plane as said first polysilicon region and said second polysilicon region.

20. The semiconductor device of Claim 17 further comprising a third trench-like structure comprising two polysilicon regions, wherein said second trench-like structure is situated between said first trench-like structure and said third trench-like structure.

21. The semiconductor device of Claim 17 further comprising at least two successive trench-like structures parallel to said first trench-like structure and said second trench-like structure, each of said successive trench-like structures

comprising two electrode regions, wherein said second trench-like structure is situated between said first trench-like structure and said two successive trench-like structures.

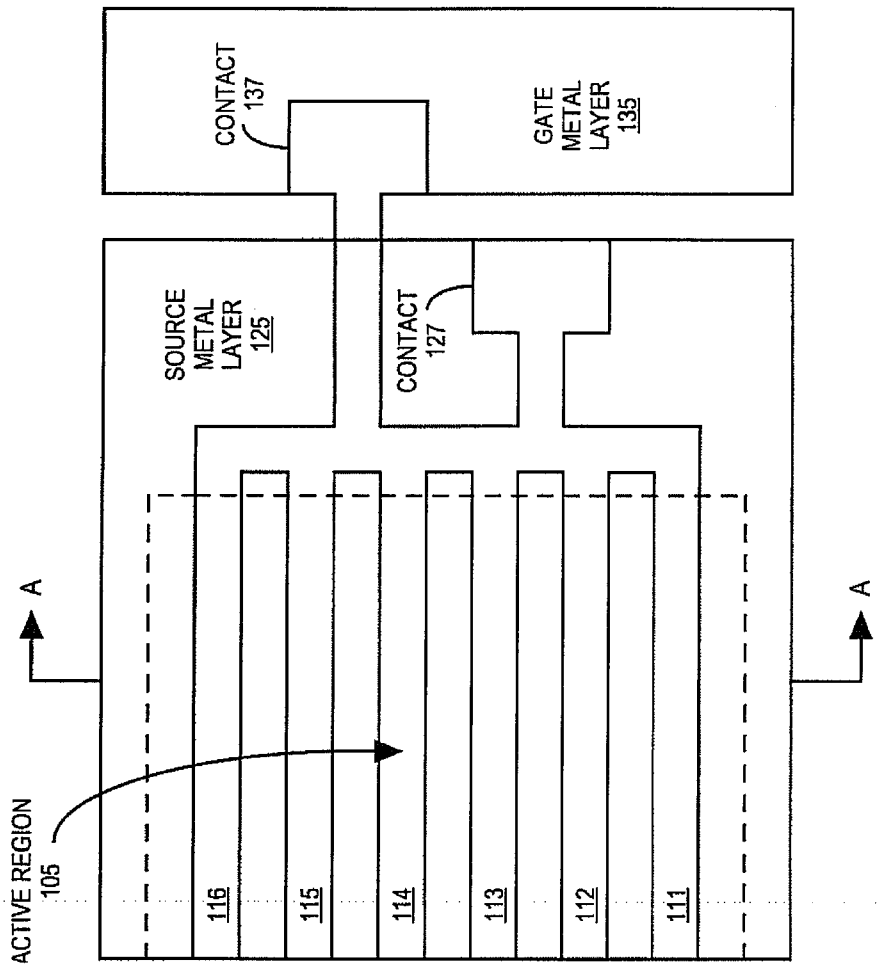
CONTACT
137
GATE
METAL
LAYER
135
SOURCE
METAL
LAYER
125
CONTACT
127
A
A
ACTIVE REGION
105
100
116
115
114
113
112
111

FIG. 1

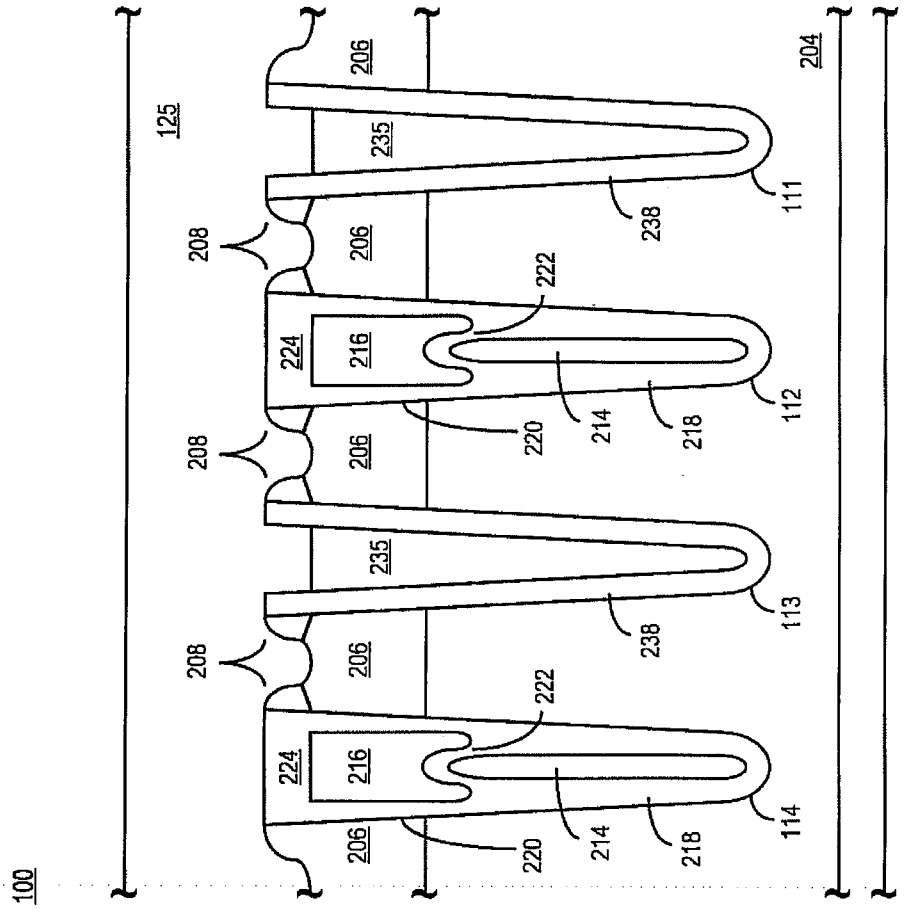
100
125
204
206
208
216
218
220
222
224
235
238
111
112
113
114
214

FIG. 2

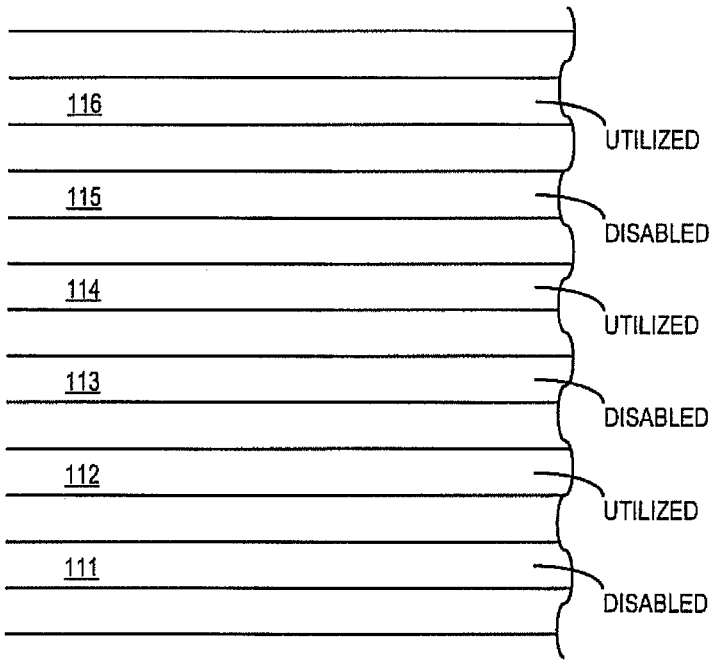
116
UTILIZED
115
DISABLED
114
UTILIZED
113
DISABLED
112
UTILIZED
111
DISABLED

FIG. 3

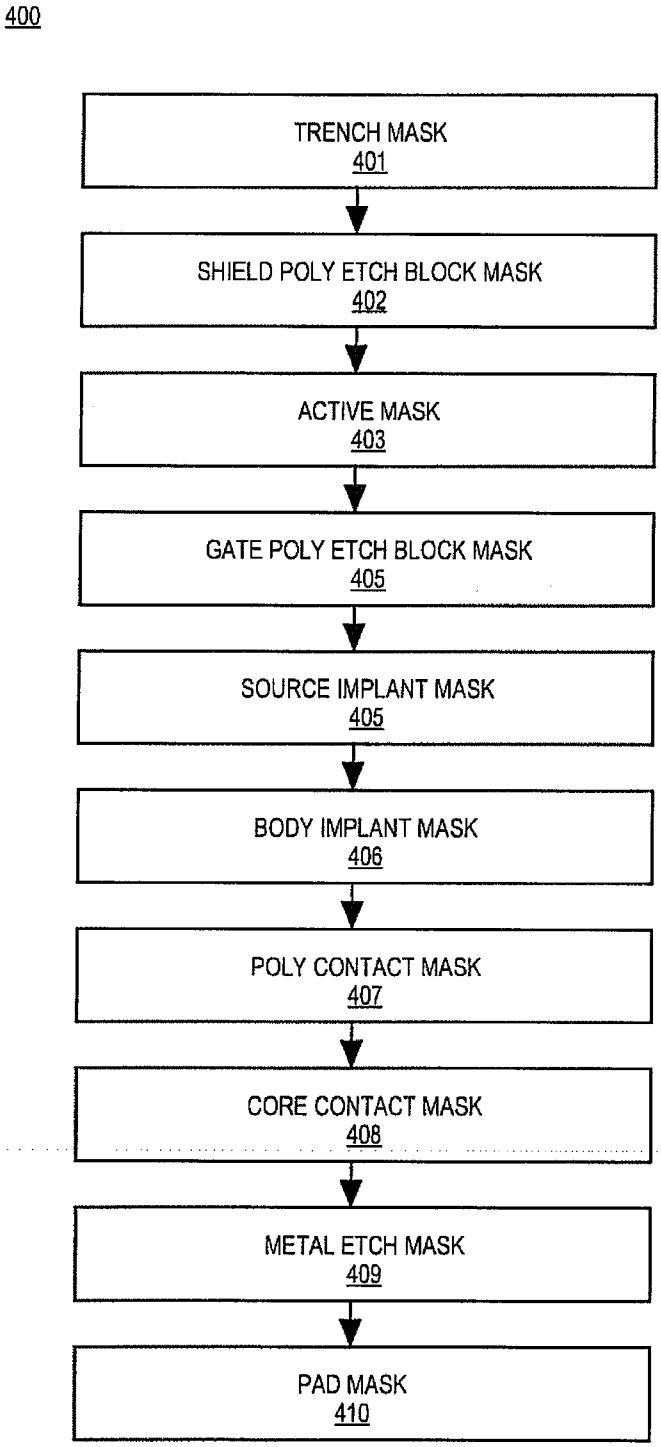
400
TRENCH MASK
401
SHIELD POLY ETCH BLOCK MASK
402
ACTIVE MASK
403
GATE POLY ETCH BLOCK MASK
405
SOURCE IMPLANT MASK
405
BODY IMPLANT MASK
406
POLY CONTACT MASK
407
CORE CONTACT MASK
408
METAL ETCH MASK
409
PAD MASK
410

FIG. 4