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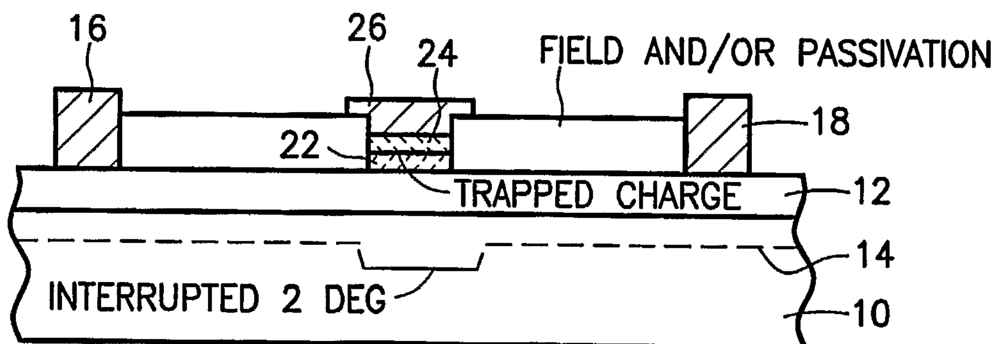
(54) Title: NORMALLY OFF III-NITRIDE SEMICONDUCTOR DEVICE HAVING A PROGRAMMABLE GATE



(57) Abstract: A III-nitride semiconductor device which includes a charged gate insulation body.

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NORMALLY OFF III-NITRIDE SEMICONDUCTOR DEVICE HAVING A PROGRAMMABLE GATE

RELATED APPLICATION

[0001] This application is based on and claims the benefit of United States Provisional Application Serial No. 60/703,931, filed on July 29, 2005, entitled NORMALLY OFF III-NITRIDE SEMICONDUCTOR DEVICE HAVING A PROGRAMMABLE GATE, to which a claim of priority is hereby made and the disclosure of which is incorporated by reference.

FIELD OF THE INVENTION

[0002] The present application relates to power semiconductor devices, and more particularly to III-nitride power semiconductor devices.

DEFINITION

[0003] As referred to herein a III-nitride semiconductor refers to a semiconductor alloy from the InAlGaN system, including, but not limited to, GaN, AlGaN, AlN, InGaN, InAlGaN, and the like.

BACKGROUND OF THE INVENTION

[0004] A conventional III-nitride heterojunction power semiconductor device includes one III-nitride semiconductor body of one band gap disposed over another III-nitride semiconductor body of another band gap to form a two dimensional electron gas that serves as a conduction channel between the power electrodes of the

device. III-nitride heterojunction power semiconductor devices are commercially desirable because of their high band gap and high current carrying capabilities. However, a typical III-nitride power semiconductor device is normally ON. Generally speaking, a normally ON power semiconductor device is less desirable in that it requires additional circuitry to keep its channel open in order to render the same OFF.

[0005] It is, therefore, desirable to have a normally off III-nitride power semiconductor device.

SUMMARY OF THE INVENTION

[0006] A semiconductor device according to the present invention includes a first III-nitride semiconductor body having a band gap, a second III-nitride semiconductor body having another band gap over the first III-nitride semiconductor body to form a III-nitride heterojunction having a two dimensional electron gas, a first power electrode coupled to the second III-nitride semiconductor body, a second power electrode coupled to the second III-nitride semiconductor body, a gate insulation body having charge (e.g. negative charge) trapped in the body thereof over the second III-nitride semiconductor body, and a gate electrode disposed over the gate insulation body.

[0007] According to one aspect of the present invention the charge in the gate insulation body is selected to interrupt the two dimensional electron gas.

[0008] According to another aspect of the present invention the charge in the gate insulation body can be varied to obtain a desired threshold voltage.

[0009] In a device according to the present invention, first III-nitride semiconductor body is comprised of one semiconductor alloy from the InAlGaN system, e.g., preferably, GaN, and the second III-nitride semiconductor body is comprised of another semiconductor alloy from the InAlGaN system, e.g., preferably, AlGaN.

[0010] According to an aspect of the present invention, gate insulation body includes at least one gate insulation body, e.g., preferably, Si_3N_4, disposed adjacent another, different insulation body, e.g., preferably, SiO_2. The present invention, however, is not limited to two insulation bodies, rather, the gate insulation body can include any number of alternately arranged first and second insulation bodies.

[0011] A semiconductor device according to the present invention may be formed as a discrete device over a substrate such as a silicon substrate, a silicon carbide substrate, or a sapphire substrate; or it may be formed as part of an integrated circuit alongside other elements in a common semiconductor body.

[0012] A device according to the present invention can be fabricated by disposing one III-nitride semiconductor body having one band gap over another III-nitride semiconductor body of another band gap to obtain a two dimensional electron gas, coupling a first and a second power electrode to the second III-nitride semiconductor body, forming a charged gate insulation body (e.g., preferably, negatively charged) over the second III-nitride semiconductor body, and forming a gate electrode over the charged gate insulation body.

[0013] A gate insulation body according to the present invention can be formed by forming one insulation body over another insulation body, and applying a bias to the gate electrode while heating the gate insulation body.

[0014] Alternatively, but not necessarily, the gate insulation body according to the present invention can be formed by forming a charged one insulation body adjacent another insulation body, and then heating the gate insulation body.

[0015] A gate insulation body can also be formed by forming one insulation body adjacent another insulation body, and implanting dopants into at least one of the insulation bodies. This may be followed by heating the gate insulation body if desired. The dopant species can be any one or a combination of Fluorine, Bromine, Iodine, and Chlorine atoms, for example. Note that any one of these techniques

allows for adjusting the threshold voltage of the gate, and thus allows the gate to be programmable.

[0016] Other features and advantages of the present invention will become apparent from the following description of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE FIGURES

[0017] Figure 1 schematically shows a cross-sectional view of the active region of a III-nitride power semiconductor device according to the prior art.

[0018] Figure 2 schematically shows a cross-sectional view of the active region of a III-nitride heterojunction power device according to the first embodiment of the present invention.

[0019] Figure 3 schematically shows a cross-sectional view of the active region of a III-nitride heterojunction power device according to the second embodiment of the present invention.

[0020] Figure 4 schematically shows a cross-sectional view of a portion of the gate structure of a III-nitride heterojunction power device according to the third embodiment of the present invention.

DETAILED DESCRIPTION OF THE FIGURES

[0021] Figure 1 illustrates an example of a typical III-nitride heterojunction high electron mobility transistor (HEMT). Specifically, a HEMT according to the prior art includes a first III-nitride semiconductor body 10 having one band gap, which may be composed of, for example, GaN, and a second III-nitride semiconductor body 12 having another band gap, which may be composed of, for example, AlGaN, disposed over first semiconductor body 10. First semiconductor body 10 may be formed over a transition body 8 composed, for example, of AlN, which is itself formed over substrate 6. As is known, transition body 8 could be a series of layers

including GaN, AlGaN, AlN, InGaAlN in various orders, to relieve stress due to the mismatch of a hetero-epitaxial layer with a substrate. Substrate 6 is preferably formed from Si, but may be formed from SiC, Sapphire, or the like. Alternatively, substrate 6 may be formed from a bulk III-nitride semiconductor (e.g. bulk GaN) which is compatible with first semiconductor body 10, in which case transition body 8 may be eliminated.

[0022] As is well known, the heterojunction of first III-nitride semiconductor body 10 and second III-nitride semiconductor body 12 results in the formation of a conductive region usually referred to as a two dimensional electron gas or 2DEG 14. Current may be conducted between a first power electrode 16 (which is preferably ohmically coupled to second semiconductor body 12), and second power electrode 18 (which is preferably also ohmically coupled to second semiconductor body 12) through 2DEG 14.

[0023] A conventional HEMT, such as the one seen in Figure 1, is a normally ON device. In many applications it is desirable to have a normally OFF device. Thus, a gate structure 20 may be disposed between first power electrode 16 and second power electrode 18. Gate structure 20 includes at least a gate electrode which may be electrically insulated by a gate insulation and thus capacitively couple to second III-nitride semiconductor body 12. The application of an appropriate voltage to the gate electrode of gate structure 20 causes the interruption of 2DEG 14 thereby turning the device OFF.

[0024] Referring to Figure 2, in which like numerals identify like features, a device according to the first embodiment of the present invention includes a gate structure having first insulation body 22 disposed over a portion second III-nitride semiconductor body 12, second insulation body 24 disposed on first insulation body 22, and gate electrode 26. A field or passivation layer 27 is provided as shown. According to the present invention first insulation body 22 and second insulation

body 24 are selected in order to create a charge trap. That is, charge can be trapped between first insulation body 22 and second insulation body 24.

[0025] For example, first insulation body 22 can be Si_3N_4 and second insulation body 24 can be SiO_2. Or, first insulation body 22 can be composed of SiO_2 and second insulation body 24 may be composed of Si_3N_4.

[0026] In a device according to the present invention, negative charge is trapped between first insulation body 22 and second insulation body 24. The amount of trapped charge can be selected so that 2DEG below gate electrode 26 is interrupted, thereby rendering the device normally OFF. An application of an appropriate voltage can then restore 2DEG 14 and render the device ON. Thus, a normally OFF switchable device can be obtained.

[0027] In order to trap the negative charge, after the fabrication of the device (according to any known method), a bias is applied to gate electrode 26 to generate the negative charge. This will cause a current to flow through the insulator (eg, through a tunneling mechanism), upon the application of a sufficiently high applied electric field. As a further feature of the invention, this effect may be enhanced if the bias is applied, while the device is heated. The application of heat generates the charge which is trapped between the first insulation body 22 and second insulation body 24. Temperature, the applied voltage and time affect how much charge is generated and trapped.

[0028] Alternatively, at least one insulation body can be grown with negative charge and then heated to allow the charge to migrate and become trapped between the two insulation bodies. Thus, for example, Si_3N_4 can be grown with negative charge for this purpose.

[0029] As another alternative, Fluorine, Bromine, Iodine, Chlorine, or the like atoms may be implanted in at least one of the insulation bodies, followed by the application of heat in order to allow charge to migrate to the interface of the insulation bodies.

[0030] In addition to being a normally OFF device, a device according to the present invention is capable of being programmed to have a variety of desirable threshold voltage. That is, the threshold voltage of a device according to the present invention can be varied by the selection of the appropriate amount of charge.

[0031] Furthermore, instead of only two insulation bodies multiple insulation bodies can be stacked in order to reach the desired threshold voltage. Thus, a device according to the present invention can include under gate electrode 26 thereof any one or a combination of the following:

[0032] SiO_2/Si_3N_4;

[0033] $SiO_2/Si_3N_4/SiO_2$;

[0034] $SiO_2/Si_3N_4/SiO_2/Si_3N_4$;

[0035] Si_3N_4/SiO_2;

[0036] $Si_3N_4/SiO_2/Si_3N_4$;

[0037] $Si_3N_4/SiO_2/Si_3N_4/SiO_2$;

and any combination of the above.

[0038] It should be understood that a device according to the present invention may be formed over a substrate in any known manner (e.g. over a transition body 8 formed on a substrate 10) as a discrete power device, or may be formed with other devices on a common substrate as a part of an integrated circuit.

[0039] Referring now to Figure 3, in a device according to the second embodiment of the present invention, first insulation body 22 includes a recess 28, second insulation body 24 is formed over at least the bottom and the sidewalls of recess 28, and gate electrode 26 may be formed at least inside recess 28 over second insulation body 24. According to the present invention, charge is trapped between first insulation body 22 and second insulation body 24, preferably along the bottom and the sidewalls of recess 28. As a result, the area devoted to charge entrapment is increased without increasing the lateral area covered by the gate structure.

[0040] Referring next to Figure 4, in a device according to the third embodiment of the present invention, a plurality of spaced recesses 30 are formed in first insulation body 22 instead of only one in order to further increase the interface area between first insulation body 22 and second insulation body 24, and thus allow for a larger charge trapping capacity between the two bodies.

[0041] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first III-nitride semiconductor body having a band gap;

a second III-nitride semiconductor body having another band gap over said first III-nitride semiconductor body to form a two dimensional electron gas;

a first power electrode coupled to said second III-nitride semiconductor body;

a second power electrode coupled to said second III-nitride semiconductor body;

a gate insulation body having charge trapped in the body thereof over said second III-nitride semiconductor body; and

a gate electrode disposed over said gate insulation body.

2. The semiconductor device of claim 1, wherein said first III-nitride semiconductor body is comprised of one semiconductor alloy from the InAlGaN system, and said second III-nitride semiconductor body is comprised of another semiconductor alloy from the InAlGaN system.

3. The semiconductor device of claim 1, wherein said first III-nitride semiconductor body is comprised of GaN, and said second III-nitride semiconductor body is comprised of AlGaN.

4. The semiconductor device of claim 1, wherein said gate insulation body is comprised of at least one gate insulation body disposed adjacent another, different insulation body.

5. The semiconductor device of claim 4, wherein said one insulation body is comprised of silicon nitride and said another insulation body is comprised of silicon dioxide.

6. The semiconductor device of claim 1, wherein said gate insulation body is comprised of alternately arranged first and second insulation bodies.

7. The semiconductor device of claim 6, wherein said first insulation body is comprised of silicon nitride and said second insulation body is comprised of silicon dioxide.

8. The semiconductor device of claim 1, wherein said charge interrupts said two dimensional gas.

9. The semiconductor device of claim 1, further comprising a substrate.

10. The semiconductor device of claim 9, wherein said substrate is comprised of silicon.

11. The semiconductor device of claim 9, wherein said substrate is comprised of silicon carbide.

12. The semiconductor device of claim 9, wherein said substrate is comprised of sapphire.

13. The semiconductor device of claim 1, wherein said semiconductor device is a discrete power device.

14. The semiconductor device of claim 1, wherein said semiconductor device is an integrated circuit.

15. The semiconductor device of claim 1, wherein said gate insulation body is negatively charged.

16. A method of fabricating a semiconductor device, comprising:

disposing one III-nitride semiconductor body having one band gap over another III-nitride semiconductor body of another band gap to obtain a two dimensional electron gas;

coupling a first and a second power electrode to said second III-nitride semiconductor body;

forming a charged gate insulation body over said second III-nitride semiconductor body; and

forming a gate electrode over said charged gate insulation body.

17. The method of claim 16, wherein said gate insulation body is negatively charged.

18. The method of claim 16, wherein said gate insulation body is formed by forming one insulation body over another insulation body, and applying a bias to said gate electrode.

19. The method of claim 16, wherein said gate insulation body is formed by forming a charged one insulation body, and another insulation body adjacent said one insulation body, and heating said gate insulation body.

20. The method of claim 16, wherein said gate insulation body is formed by forming a charged one insulation body, and another insulation body adjacent said one insulation body, and further comprising implanting dopants into at least one of said insulation bodies.

21. The method of claim 20, wherein said dopants may be selected from a group consisting of Fluorine, Bromine, Iodine, and Chlorine.

22. The method of claim 16, wherein the charge in said gate insulation body interrupts said two dimensional electron gas.

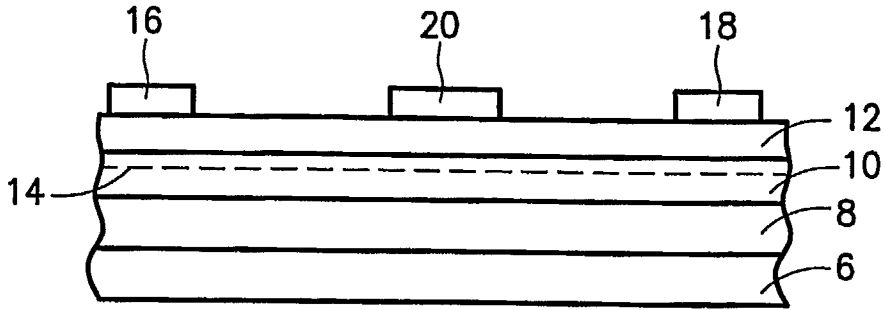

Figure 1
PRIOR ART

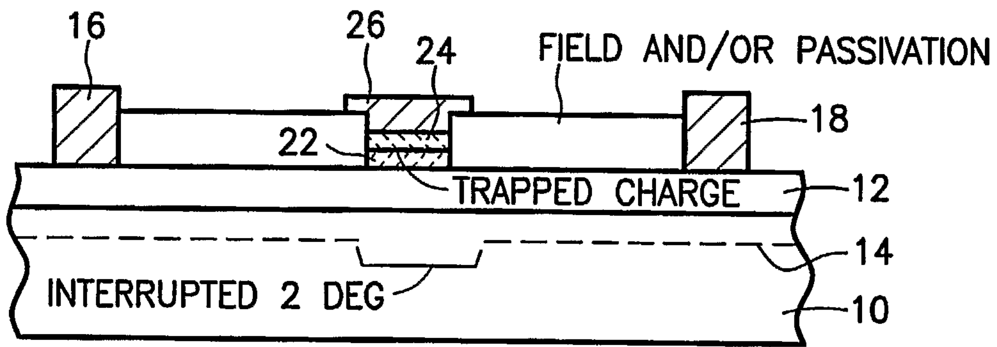

Figure 2

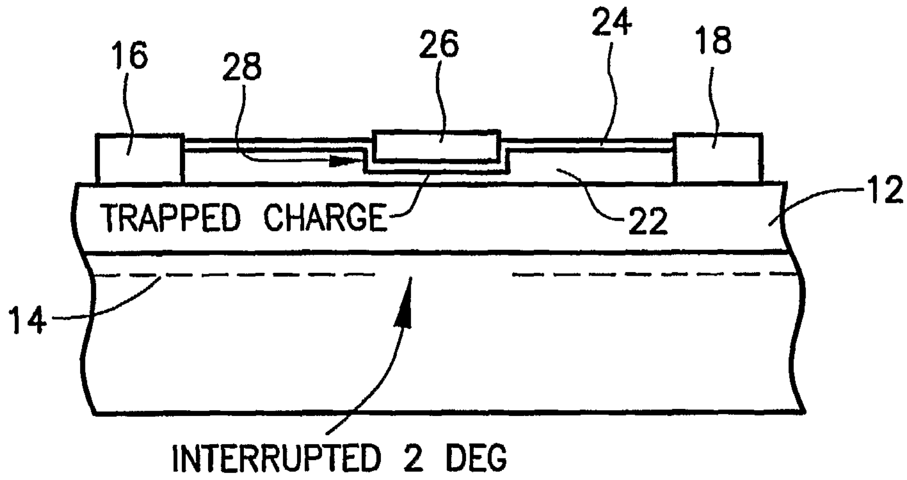

Figure 3

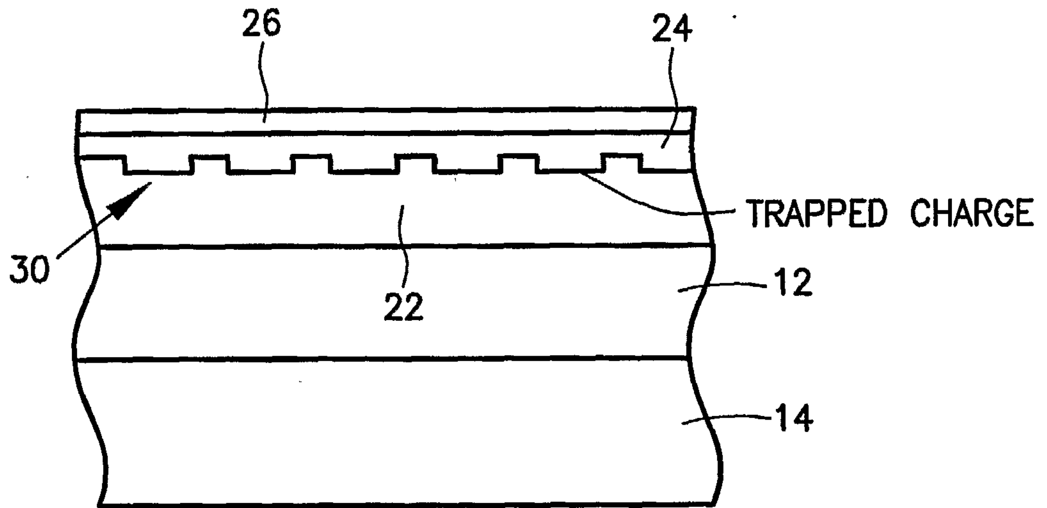

Figure 4