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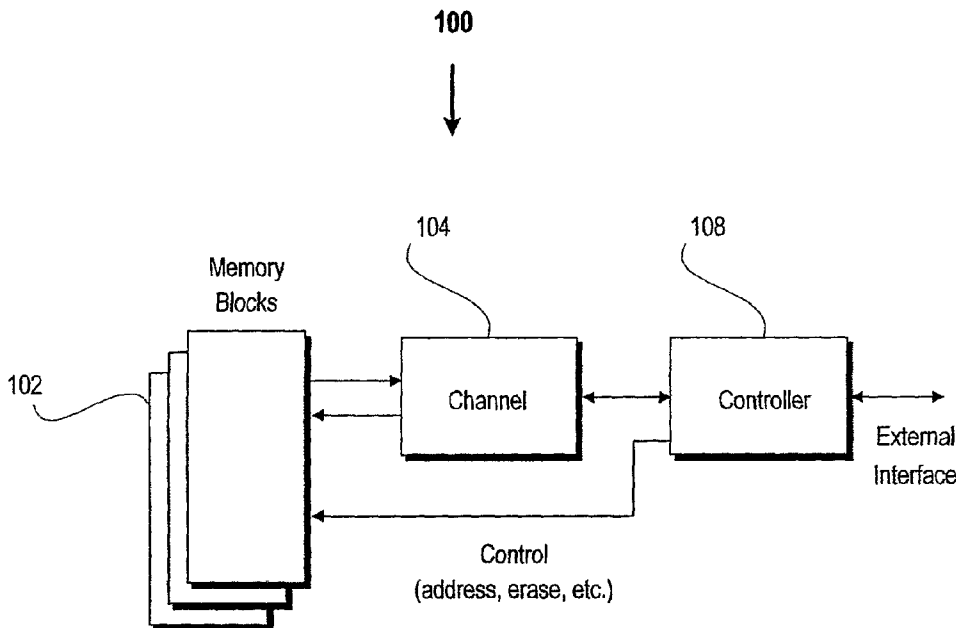
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(54) **Title:** MULTI-LEVEL MEMORY WITH LDPC BIT INTERLEAVED CODED MODULATION



(57) **Abstract:** Embodiments of the present invention provide a memory apparatus that includes a memory block comprising a plurality of memory cells, each memory cell adapted to operate with multi-level signals. Such a memory apparatus also includes a low density parity check (LDPC) coder (600) to LDPC code data values to be written into the memory cells and an interleaver (602) and a mapper (604) adapted to apply bit interleaved code modulation (BICM) to the LDPC coded data values to generate BICM coded data values.

WO 2007/116275 A1



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Cross Reference to Related Applications

The present application claims priority to U.S. Patent Application No. 60/788,291, filed March 31, 2006, entitled "LDPC Codes for Multi-Level Flash Memory," the entire disclosure of which is hereby incorporated by reference in its entirety.

Technical Field

Embodiments of the present invention relate to the field of integrated circuits, and more particularly, to providing multi-level signal memory with LDPC and interleaving.

Background

In order to increase memory capacity, manufacturers have continually moved memory chip or on-chip memory (such as flash memory) production to smaller process geometries over the last few years. Recently, multi-level signal memory cells have been used to increase flash memory capacity. In such an arrangement, a cell is configured to produce distinct signal threshold levels, which results in distinct read-back levels. With four level signals available per cell, two bits may be included into each flash memory cell. One problem with writing with four signal levels into each cell is that the distinction between adjacent levels may become difficult to discern. This is often referred to in the art as reduced signal distance (often shown as reduced D_{min}).

When writing a signal level to a given cell, there is generally an amount of uncertainty in the written-in signal level. When the probable distribution of each signal level overlaps the probable distribution of adjacent signal level, the signal level generally may not be determined by using a simple prior art slicer circuit. This results in a limit on the number of signal levels that may be employed to write into every cell. At present, the state of the art is four signal levels, or two bits per cell.

Summary of the Invention

In accordance with various embodiments of the present invention, a memory apparatus includes a memory block comprising a plurality of memory cells, each memory cell adapted to operate with multi-level signals. The memory apparatus also includes a low density parity check (LDPC) coder to LDPC code data values to be written into the memory cells and an interleaver adapted to apply bit interleaved code modulation (BICM) to the LDPC coded data values to generate BICM coded data values.

In accordance with various embodiments, the memory apparatus further includes a controller adapted to control the coding by the LDPC coder, the interleaving by the interleaver, and the receiving of the of the multi-level signals by the memory block.

In accordance with various embodiments, the memory apparatus further includes a mapper to map the BICM coded data values to modulation codes in accordance with a constellation map.

In accordance with various embodiments, the constellation map is based upon Gray code.

In accordance with various embodiments, the constellation map comprises 8 modulation codes.

In accordance with various embodiments, a set of least significant bits is mapped to a modulation code corresponding to a lowest transmission voltage level, and a set of most significant bits is mapped to a modulation code corresponding to a highest transmission voltage level.

In accordance with various embodiments, the memory apparatus further includes a pulse amplitude modulator (PAM) operatively coupled to the interleaver and the memory block to modulate the multi-level signals for the memory block.

In accordance with various embodiments, the memory apparatus further includes a channel block that comprises the interleaver and the PAM.

In accordance with various embodiments, the memory apparatus further includes a channel block that comprises the interleaver and at least one of the LDPC coder or the mapper.

In accordance with various embodiments, at least the memory block is configured as a flash memory device.

In accordance with various embodiments, the memory block comprises one of a floating gate device, oxide-nitride-oxide (ONO) charge trapping device or
5 a phase change memory device.

In accordance with various embodiments, the memory apparatus further includes a pulse amplitude modulator (PAM) and a digital bus interface operatively coupled to the PAM and the memory block, wherein the PAM is adapted to output multi-level signals to the memory block serially.

10 In accordance with various embodiments, the memory apparatus further includes a de-interleaver operatively coupled to the memory block to deinterleave BICM coded data values from multi-level signals received from the memory block.

In accordance with various embodiments, the memory apparatus further
15 includes a LDPC decoder operatively coupled to the de-interleaver to decode the data values from the de-interleaved LDPC coded data values.

In accordance with various embodiments, the memory apparatus further includes a channel block that comprises the de-interleaver and the LDPC decoder.

20 In accordance with various embodiments of the present invention, a method includes coding a plurality of multi-level signal data values with corresponding low density parity (LDPC) codes, interleaving the LDPC coded multi-level signal data values with bit interleaved code modulation (BICM), and outputting the interleaved LDPC coded data values for storage using multi-level
25 signals.

In accordance with various embodiments of the present invention, a method includes receiving a coded multi-level signal data value, wherein the coded multi-level signal data value has been coded with a low density parity check code (LDPC) and interleaved with bit interleaved code modulation (BICM),
30 and decoding the coded multi-level signal data value to recover a multi-level signal data value.

Brief Description of the Drawings

Embodiments of the present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments of the invention are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

Fig. 1 schematically illustrates a memory arrangement in accordance with various embodiments of the present invention;

Fig. 2 schematically illustrates an exemplary transistor for a flash memory cell suitable for use to practice various embodiments of the present invention;

Fig. 3 is a graph illustrating transistor characteristics corresponding to different charge levels;

Fig. 4 is a graph illustrating a probability density distribution for the threshold voltage of a system of four charge level flash memory cells;

Fig. 5 is a graph illustrating the shift profile for the probability distribution for the threshold voltage of a system of four charge level flash memory cells;

Fig. 6 schematically illustrates a high gain coding scheme in accordance with various embodiments of the present invention; and

Figs. 7 and 8 schematically illustrate exemplary channel block implementations in accordance with various embodiments of the present invention.

Detailed Description of Embodiments of the Invention

In the following detailed description, reference is made to the accompanying drawings which form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of illustration embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of embodiments in accordance with the present invention is defined by the appended claims and their equivalents.

Various operations may be described as multiple discrete operations in turn, in a manner that may be helpful in understanding embodiments of the present invention; however, the order of description should not be construed to imply that these operations are order dependent.

5 For the purposes of the present invention, the phrase "A/B" means A or B. For the purposes of the present invention, the phrase "A and/or B" means "(A), (B), or (A and B)". For the purposes of the present invention, the phrase "at least one of A, B, and C" means "(A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C)". For the purposes of the present invention, the phrase "(A)B" means "(B) or (AB)" that is, A is an optional element.

10 The description may use the phrases "in an embodiment," or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present invention, are
15 synonymous.

Embodiments of the present invention provide multi-level signal memory with LDPC and interleaving.

In general, a block diagram of a memory arrangement 100, in accordance with various embodiments of the present invention, is illustrated in Fig. 1.

20 Memory arrangement 100 includes one or more memory blocks 102 that each includes memory cell arrays, as well as read and write circuits. Memory arrangement 100 also includes a channel block 104 that performs signal processing used to decode signal levels received from memory blocks 102. In accordance with various embodiments, channel block 104 also performs signal
25 processing to code various data values to write into memory blocks 102. A controller 108 is provided to interface to external system(s) to receive and send data signals through its external data interface, to and from channel block 104. Controller 106 performs various tasks including tasks that direct where data values need to be written into or read from memory blocks 102 depending upon
30 command instructions received through its external interface. In various embodiments, memory blocks 102 may be flash memory blocks.

In accordance with various embodiments of the present invention, a high gain coding such as, for example, trellis coded modulation (TCM) is used by

channel block 104 to code and/or decode multi-level signal data values to and/or from a memory block. The addition of TCM imposes a certain constraint as to what sample sets may be adjacent to a previous and a future sample sequence. Various codes may be used to allow multi-level signals data values with a spread distribution that reduces overlaps with one another, enabling the multi-level signals data values to be more likely detected correctly, using e.g. maximum likelihood detection and decoding with trellis coding. Pulse Amplitude Modulation code (PAM), Quadrature Amplitude Modulation code (QAM) and Low Density Parity Check code (LDPC) are examples of codes that may be used. By encoding the multi-level signal data values with high gain coding and/or one or more of PAM, QAM and LDPC, a higher reliability of reading and writing the multi-level signals may be achieved within each memory cell, which in turn may lead to increase in data density of a memory array (reduce usage of memory cells for auxiliary information).

Generally, an exemplary flash memory cell, in accordance with various embodiments of the present invention and depicted in Fig. 2, includes an insulated gate transistor 200 that includes a floating gate 202 between the channel 204 and the control gate 206. Charge trapped in floating gate 202 modifies the turn-on threshold voltage. The transistor characteristics are illustrated in Fig. 3, corresponding to different charge levels stored on floating gate 202. With devices that include a plurality of memory cells arranged in arrays, many parameters that naturally vary from one device to another due to imperfect process control may affect the programmed threshold of the device. Consequently, if one were to write to many devices targeting a certain threshold value, the end result is a distribution of target threshold values instead of the desired distinct target threshold values. Fig. 4 illustrates a typical probability density function (PDF) for the target threshold voltages of a system of flash memory cells, each cell having four target charge levels.

Over time, the charge trapped in floating gate 202 generally leaks slowly and the threshold voltage may shift back towards a lower value. While the leakage is generally slow, the specification for any commercially acceptable storage device requires the data to be readable even after a ten-year period. The rate of leakage of the floating gate charge is dependent upon the voltage on

floating gate 202. Fig. 5 illustrates a typical shift profile for the threshold PDF over time. Furthermore, the physics of charge leakage in a memory cell is such that each signal level may leak at a different rate from the others. As such, over time, the signal levels generally will not drop at the same rate.

5 Thus, as an example, in accordance with various embodiments of the present invention, in a write mode, multi-level signals that are employed to write various data into memory cells within the memory block are encoded with the high gain coding. The high gain encoded data signals are output to the memory blocks to write data into the memory block cells.

10 During a read mode, in accordance with various embodiments of the present invention, memory blocks 102 responsive to the commands of controller 108 output data that is stored in at least one memory cell. In accordance with various embodiments, data stored in a whole row of memory cells may be outputted at different read-back signal levels. The multi-level read-back signals
15 for each cell are transferred to channel block 104. If a small interface is desired, the signals may be transferred in a serial fashion. In one embodiment, analog to digital conversion or a digitizing function (not shown), may be performed by an analog to digital converter (ADC) that is included on memory block 102 if inclusion of such ADC is practical. Thus, the signal levels may be transferred as
20 digitized data and sent back to channel block 104 serially. Otherwise, in accordance with various embodiments, analog signals may be transferred back to channel block 104 from memory block 102 as discrete time analog signals. Such transfers, in accordance with various embodiments, may be done serially if desired, or in parallel, in other embodiments. In a serial embodiment, the
25 channel block may either digitize the signal or not based upon whether an analog or digital channel implementation is used. In accordance with various embodiments of the present invention a digital channel implementation is used and thus, the channel block includes an ADC, and memory block 102 and channel block 104 are operatively coupled to one another via a digital bus
30 interface.

More particularly, with reference to Fig. 6, a coding scheme in accordance with various embodiments of the present invention includes multi-level signal data values being received at channel block 104 from controller 108. The received

data values are encoded with LDPC via LDPC encoder/de-coder 600. The LDPC coded values are then passed through an interleaver 602. The interleaved values are mapped to constellation points by the constellation mapper at 604. Thus, the system implements bit-interleaved coded modulation (BICM). In accordance with various embodiments, Gray code mapping is used. In accordance with various embodiments, the constellation map includes 8 constellation points. Those skilled in the art will understand that fewer constellation points may be used if desired, e.g., 4 or 2 constellation points, or if possible, more constellation points, e.g., 16, 32, etc. The mapped values are transferred from channel block 104 to memory block 102 and written into a memory cell of memory block 102.

In accordance with various embodiments of the present invention, PAM is used to transmit signals between channel block 104 and memory block 102. Thus, in accordance with various embodiments, there are 8 channels for the PAM. As an example, the channels may include $-7v$, $-5v$, $-3v$, $-1v$, $+1v$, $+3v$, $+5v$ and $+7v$ transmission voltage levels. In accordance with various embodiments of the present invention, a least significant bit (e.g. bit 0) represents the lowest or "worst" channel, while a most significant bit (e.g. bit 100) represents the highest or "best" channel.

When data needs to be retrieved from memory block 102, coded multi-level signal data values are transferred from the memory block to channel block 104, where they are decoded. Thus, in accordance with various embodiments, the LDPC encoder/de-coder, interleaver and mapper are included with channel block 104.

Thus, with a coding scheme in accordance with various embodiments of the present invention, more levels may be realized on a multi-level memory device since the coding allows for more reliable retrieval of data values from the memory, even with the reduced distance between levels.

In accordance with various embodiments, an exemplary channel block 104 may be configured similar to generally known communication or magnetic hard disk drive (HDD) channels, as illustrated in Fig. 7. As may be seen in Fig. 7, such an exemplary channel block 104 may include an interface 700, a run length limited (RLL) encoder 702 and channel modulation 704 along a write path. The

exemplary channel block 104 may further include a variable gain amplifier (VGA) 706, an offset setting 708, a continuous time filter (CTF) block 710, an ADC 712, a finite impulse response (FIR) block 714, a Viterbi detector 716, an RLL decoder 718, error generators 720, an offset control loop 722, a gain control loop 724, a
5 clock recovery 726 and clock generator 728 along a read path, coupled to each other substantially as illustrated.

Some simplification may be made from a conventional channel block. For example, since data sampling and transfer, in accordance with various embodiments, are clocked synchronously, there is no need to include a timing
10 recovery circuit (726, 728) in channel block 104. Such a timing recovery circuit may be included if desired such as, for example, for very high data-rate applications. However, generally the sampling clock frequency matches exactly to the incoming data signal frequency and thus, only the delay is potentially
15 unknown. For such a system only a Type I timing recovery loop may be desired.

Additionally, the signal returning from memory block 102 may match well to the target response, i.e., the original signal, such that linear equalizers in the channel block (CTF 710 and FIR 714) may not be necessary. Other functional blocks typical of a communication/HDD channel may be included, in accordance with various embodiments of the present invention, for memory arrangement 100.
20 In particular, as noted above, automatic gain control loop 724, Viterbi detector 716 (with trellis control) and channel encoder/decoder (702, 718) may also be included.

Often, standard deviation in the distribution of each target signal level is different from the others, and the mean distance between two adjacent ideal
25 signal levels may not be constant relative to the design target. Thus, in accordance with various embodiments, Viterbi detector 716 may implement adaptive and non-linear branch metrics calculators (e.g., the Viterbi detector may use a subset non-linear detector algorithm used in magnetic HDD).

In accordance with various embodiments of the present invention, channel
30 block 104 may also include a sample data buffer capable of storing a large section of data samples so iterative or over-a-block processing may be performed (e.g., block averaging for gain control so that signal levels may become normalized before other processing by the channel block). An example of such

an arrangement for channel block 104 is schematically illustrated in Fig. 8. As may be seen, such an exemplary channel block 104 may include an interface 800, RLL encoder 802 and channel modulation 804 along a write path. The exemplary channel block 104 may further include a VGA 806, offset setting 808,
5 ADC 810, sample buffer 812, offset setting 814, gain control 816, offset setting 818, feed forward offset control 820, offset setting 822, gain control 824, offset setting 826, offset control 828, error generator 830, Viterbi detector 832 and RLL decoder 834, coupled to each other substantially as illustrated.

In accordance with various embodiments of the present invention, at least
10 the memory block, and even the entire memory arrangement, is a flash-type memory device. For clarity, the present invention has been substantially described as such, although those skilled in the art will understand that other types of memory may benefit from the present invention. Additionally, in accordance with various embodiments of the present invention, the present
15 invention is useful for many types of memory devices such as, for example and not limited to, floating gate devices, oxide-nitride-oxide (ONO) charged trapping devices, and phase change memory devices.

While the present invention is useful for all types of devices that use memory, it is especially useful for portable electronic devices, such as, for
20 example, mobile phones, laptop computers, personal digital assistants, gaming devices, music players, and video players. In various embodiments, the portable electronic devices may include reduced instruction set (RISC) processors and wireless communication support, such as wireless communication in accordance with one or more of the Institute of Electrical and Electronic Engineer's (IEEE)
25 802.11 family of standards.

Although certain embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent
30 embodiments or implementations calculated to achieve the same purposes may be substituted for the embodiments shown and described without departing from the scope of the present invention. Those with skill in the art will readily appreciate that embodiments in accordance with the present invention may be implemented in a very wide variety of ways. This application is intended to cover

any adaptations or variations of the embodiments discussed herein. Therefore, it is manifestly intended that embodiments in accordance with the present invention be limited only by the claims and the equivalents thereof.

Claims

What is claimed is:

1. A memory apparatus comprising:
a memory block comprising a plurality of memory cells, each memory cell adapted to operate with multi-level signals;
5 a low density parity check (LDPC) coder to LDPC code data values to be written into the memory cells;
an interleaver adapted to apply bit interleaved code modulation (BICM) to the LDPC coded data values to generate BICM coded data values.
2. The memory apparatus of claim 1, further comprising a controller adapted
10 to control the coding by the LDPC coder, the interleaving by the interleaver, and the receiving of the of the multi-level signals by the memory block.
3. The memory apparatus of claim 1, further comprising a mapper to map the BICM coded data values to modulation codes in accordance with a constellation map.
- 15 4. The memory apparatus of claim 3, wherein the constellation map is based upon Gray code.
5. The memory apparatus of claim 4, wherein the constellation map comprises 8 modulation codes.
6. The memory apparatus of claim 5, wherein a set of least significant bits is
20 mapped to a modulation code corresponding to a lowest transmission voltage level, and a set of most significant bits is mapped to a modulation code corresponding to a highest transmission voltage level.
7. The memory apparatus of claim 1, further comprising a pulse amplitude modulator (PAM) operatively coupled to the interleaver and the memory block to
25 modulate the multi-level signals for the memory block.
8. The memory apparatus of claim 7, further comprising a channel block that comprises the interleaver and the PAM.
9. The memory apparatus of claim 3, further comprising a channel block that comprises the interleaver and at least one of the LDPC coder or the mapper.

10. The memory apparatus of claim 1, wherein at least the memory block is configured as a flash memory device.
11. The memory apparatus of claim 1, wherein the memory block comprises one of a floating gate device, oxide-nitride-oxide (ONO) charge trapping device or
5 a phase change memory device.
12. The memory apparatus of claim 1, further comprising a pulse amplitude modulator (PAM) and a digital bus interface operatively coupled to the PAM and the memory block, wherein the PAM is adapted to output multi-level signals to the memory block serially.
- 10 13. The memory apparatus of claim 1, further comprising a de-interleaver operatively coupled to the memory block to deinterleave BICM coded data values from multi-level signals received from the memory block.
14. The memory apparatus of claim 13, further comprising a LDPC decoder operatively coupled to the de-interleaver to decode the data values from the de-
15 interleaved LDPC coded data values.
15. The memory apparatus of claim 14, further comprising a channel block that comprises the de-interleaver and the LDPC decoder.
16. A method comprising:
coding a plurality of multi-level signal data values with corresponding low
20 density parity (LDPC) codes;
interleaving the LDPC coded multi-level signal data values with bit interleaved code modulation (BICM); and
outputting the interleaved LDPC coded data values for storage using multi-level signals.
- 25 17. The method of claim 16, further comprising mapping the interleaved LDPC coded data values to modulation codes in accordance with a constellation map.
18. The method of claim 17, wherein the constellation map is based upon Gray code.
19. The method of claim 17, wherein the constellation map comprising 8
30 constellation points.

20. The method of claim 17, wherein mapping the interleaved LDPC coded data values to a constellation map further comprises mapping a set of least significant bits to a modulation code corresponding to a lowest transmission voltage level and mapping a set of most significant bits to a modulation code
5 corresponding to a highest transmission voltage level.
21. The method of claim 16, further comprising modulating the interleaved LDPC coded data values for storage.
22. The method of claim 21, wherein the modulating is performed with a pulse amplitude modulator (PAM),
- 10 23. A method comprising:
receiving a coded multi-level signal data value, wherein the coded multi-level signal data value has been coded with a low density parity check code (LDPC) and interleaved with bit interleaved code modulation (BICM); and
decoding the coded multi-level signal data value to recover a multi-level
15 signal data value.
24. The method of claim 23, wherein the coded multi-level signal data value has also been mapped to a modulation code in accordance with a constellation map.
25. The method of claim 24, wherein the constellation map is based upon
20 Gray code mapping.
26. The method of claim 24, wherein the constellation map comprises 8 constellation points.
27. The method of claim 26, wherein a set of least significant bits have been mapped to a modulation code corresponding to a lowest transmission voltage level and a set of most significant bits have been mapped to a modulation code
25 corresponding to a highest transmission voltage level.
28. A memory apparatus comprising:
means for coding data values with low density parity check (LDPC) code to create coded data values;

means for generating bit interleaved code modulation (BICM) coded data values; and

means for storing BICM coded data values, the means for storing BICM coded data values being adapted to operate with multi-level signals.

5 29. The memory apparatus of claim 28, further comprising means for controlling the means for coding, the means for generating, and the means for storing.

10 30. The memory apparatus of claim 28, further comprising means for mapping the BICM coded data values to modulation codes in accordance with a constellation map.

31. The memory apparatus of claim 30, wherein a set of least significant bits is mapped to a modulation code corresponding to a lowest transmission voltage level, and a set of most significant bits is mapped to a modulation code corresponding to a highest transmission voltage level.

15 32. The memory apparatus of claim 28, further comprising means to modulate the multi-level signals.

33. The memory apparatus of claim 28, further comprising means for deinterleaving BICM coded data values from multi-level signals received from the means for storing the BICM coded data values.

20 34. The memory apparatus of claim 33, further comprising means for decoding the data values from the de-interleaved BICM coded data values.

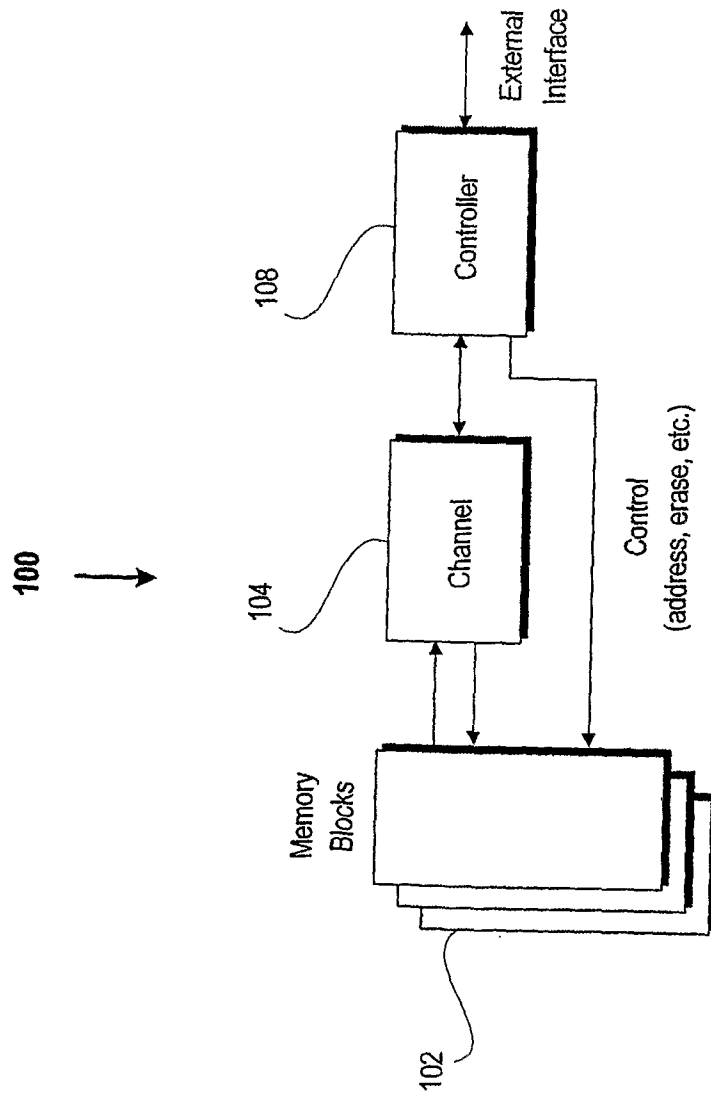


FIG. 1

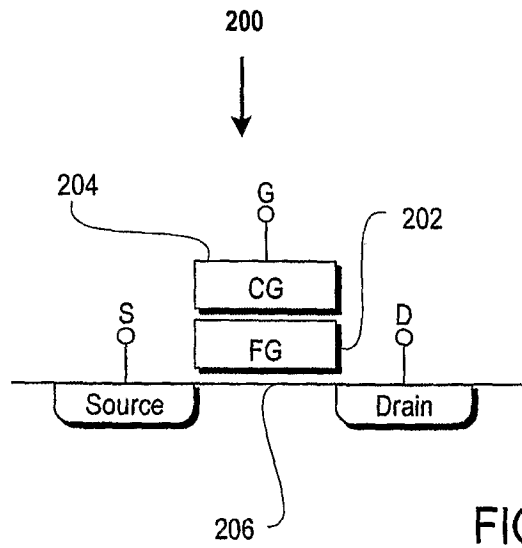


FIG. 2

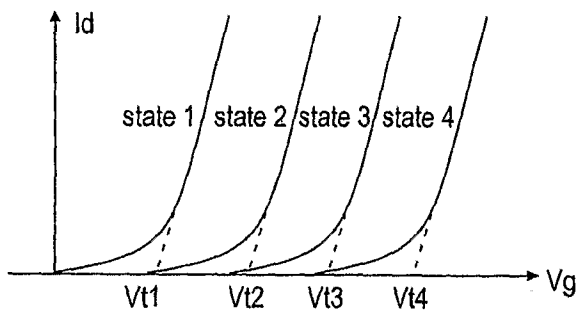


FIG. 3

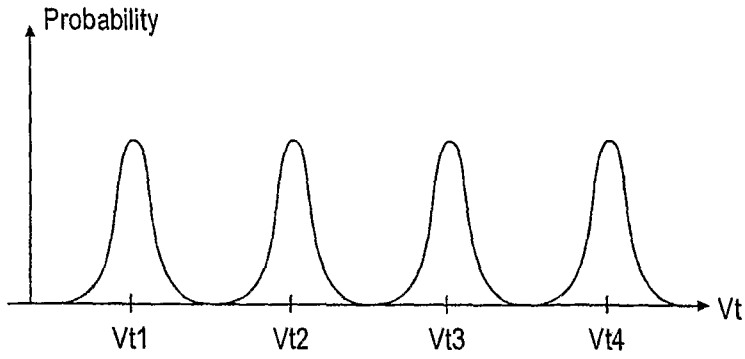


FIG. 4

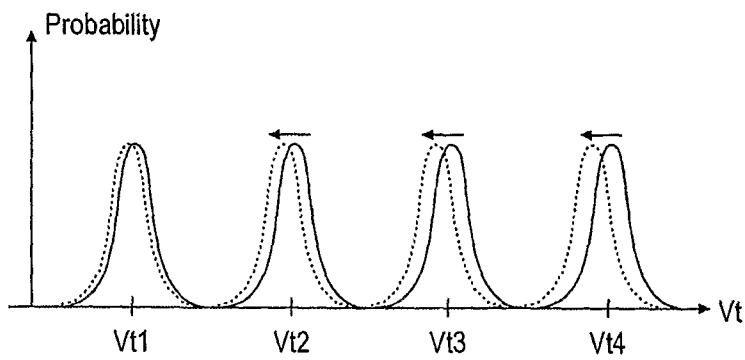


FIG. 5

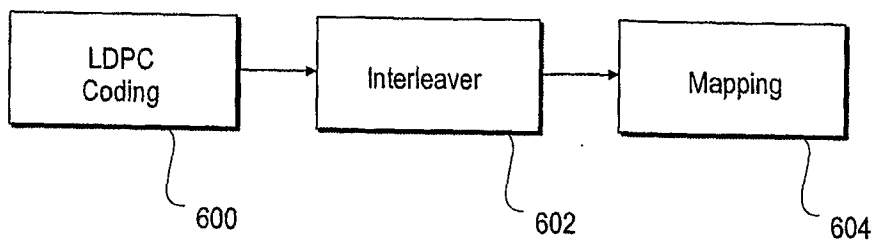


FIG. 6

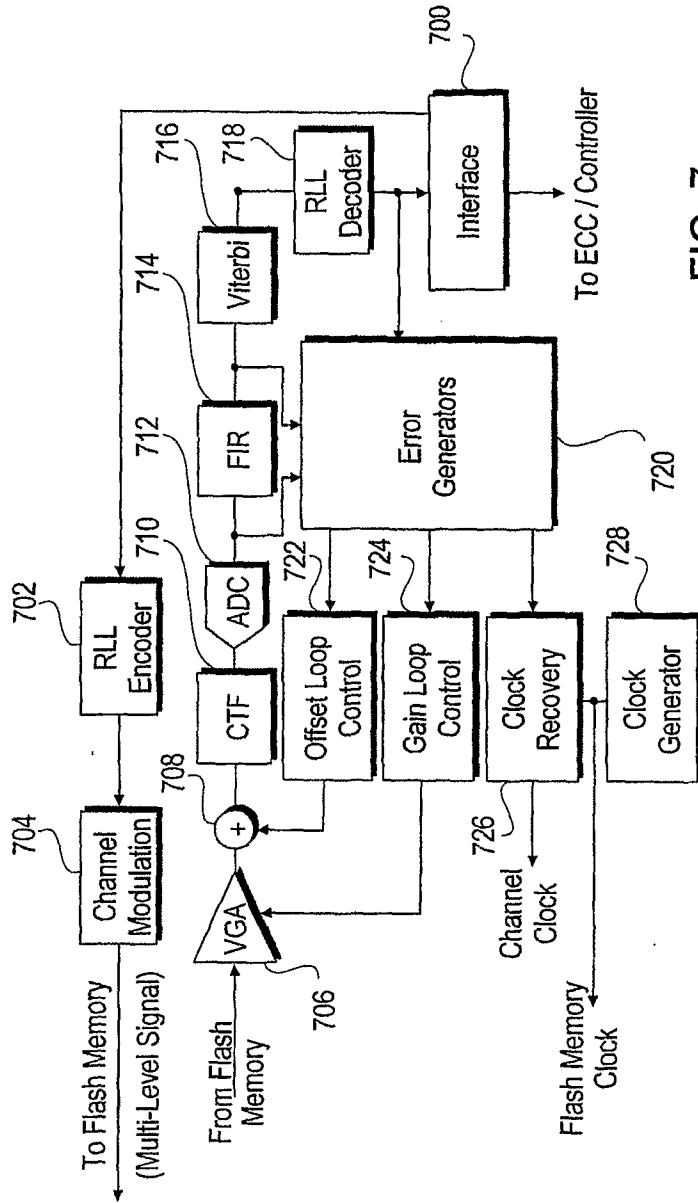


FIG. 7

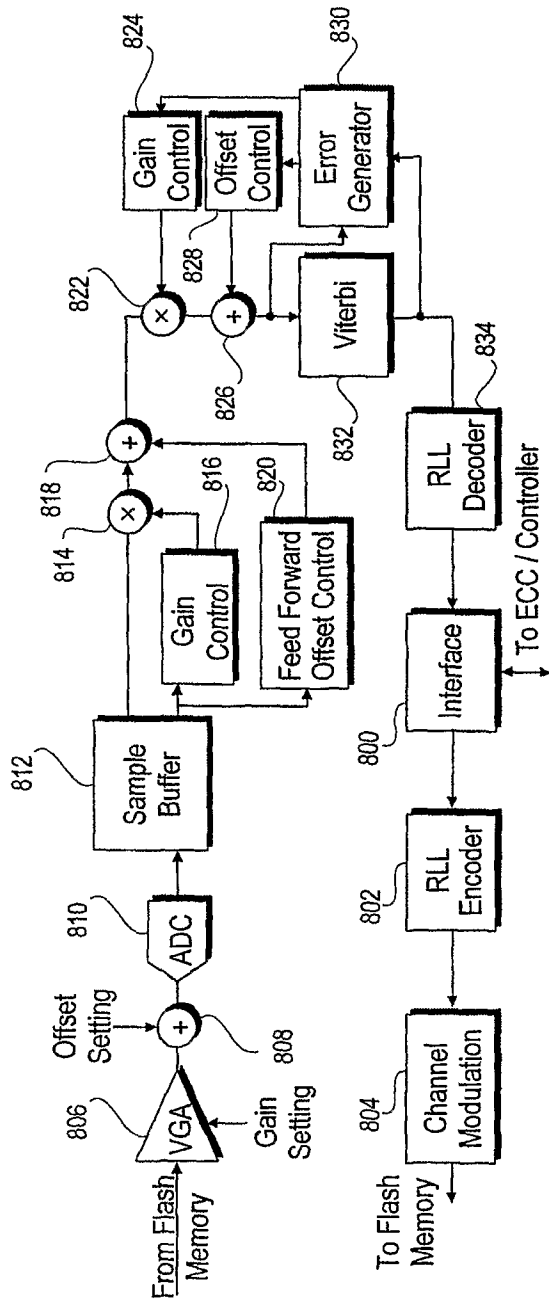


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2007/000822

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M13/25 H03M13/11

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M G06F G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ZHANG ZHI ET AL: "Low-density parity-check codes and high spectral efficiency modulation" PROC. PERSONAL, INDOOR AND MOBILE RADIO COMMUNICATIONS CONFERENCE, 7 September 2003 (2003-09-07), pages 444-448, XP010681635 PISCATAWAY, NJ, USA ISBN: 0-7803-7822-9	23-27
Y	abstract page 445 figure 2 ----- -/--	1-22, 28-34

Further documents are listed in the continuation of Box C.

See patent family annex.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2007/000822

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	<p>LOU H-L ET AL: "CODED MODULATION TO INCREASE STORAGE CAPACITY OF MULTILEVEL MEMORIES" PROC. IEEE GLOBECOM 1998, vol. VOL. 6, 1998, pages 3379-3384, XP000805261 Sydney, Australia ISBN: 0-7803-4985-7 abstract page 3379, left-hand column - page 3380, right-hand column figures 1-4</p>	1-22, 28-34
A	<p>----- WINSTEAD C: "Analog Soft Decoding for Multi-Level Memories" PROCEEDINGS 35TH INTERNATIONAL SYMPOSIUM ON MULTIPLE-VALUED LOGIC, 19 May 2005 (2005-05-19), pages 132-137, XP010798331 Calgary, Canada ISBN: 0-7695-2336-6 abstract page 3, right-hand column - page 4, left-hand column</p>	1-34
A	<p>----- HSIE-CHIA CHANG ET AL: "Multi-level memory systems using error control codes" PROCEEDINGS OF THE 2004 INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS, vol. 2, 23 May 2004 (2004-05-23), pages 393-396, XP010720188 Vancouver, Canada ISBN: 0-7803-8251-X the whole document</p>	1-34
A	<p>----- ROSSI D ET AL: "Fast and compact error correcting scheme for reliable multilevel flash memories" PROC. OF THE EIGHTH IEEE INTERNATIONAL ON-LINE TESTING WORKSHOP, 8 July 2002 (2002-07-08), pages 221-225, XP010601444 PISCATAWAY, NJ, USA ISBN: 0-7695-1641-6 the whole document</p>	1-34
A	<p>----- GREGORI S ET AL: "Construction of polyvalent error control codes for multilevel memories" PROC. INTERN. CONFERENCE ON ELECTRONICS, CIRCUITS AND SYSTEMS, vol. 2, 17 December 2000 (2000-12-17), pages 751-754, XP010535817 PISCATAWAY, NJ, USA ISBN: 0-7803-6542-9 the whole document</p> <p>-----</p>	1-34