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(54) DELAY NETWORK WITH WEIGHTING FACTOR ADJUSTING MEANS

(71) We, N.V. PHILIPS' GLOEILAMPENFABRIEKEN, a limited liability Company, organised and established under the laws of the Kingdom of the Netherlands, of Emmasingel 29, Eindhoven, the Netherlands, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a delay network comprising at least three storage/transfer elements each of which includes a storage capacitor, couplings between said elements so that said elements together form a shift register, first and second further couplings from a signal input to said shift register and from said shift register to a signal output respectively, and weighting-factor adjusting means included in a said coupling so that said weighting factor adjusting means is included in a signal path from said signal input to said signal output, said weighting-factor adjusting means comprising first and second field-effect transistor structures the channel of the first of which is included in series with the corresponding coupling in such manner that one main electrode of said first structure is connected to the storage capacitor of a said storage/transfer element said one main electrode of said first structure being effectively commoned with the corresponding main electrode of said second structure, both of said structures being integrated in the same semiconductor body.

The shift register may be a charge transfer device (CTD) in the form of a bucket brigade device (BBD) or a charge-coupled device (CCD) which shifts a signal, applied to its input in analog or digital form, stepwise from its input to its output under the influence of clock pulses.

Patent Specification 1,427,626 discloses a delay network comprising a shift register having a plurality of storage/transfer elements each of which includes a storage capacitor, signal transfer from each element to the next being controlled by clock voltages which are applied to the control electrodes of transistors also included in the various elements. Couplings are also provided between various elements and a signal output, these couplings each including weighting factor adjusting means which each comprise a pair of further field-effect transistors the gates of which are supplied with specific bias voltages and one main electrode of each of which is connected to the storage capacitor of the corresponding element. The weighting factor of the signal transmitted thereby to the output can be adjusted by adjusting the difference between the two gate voltages. It has been found that determination of the various weighting factors in this way can give rise to non-linear signal transfer, which can be a disadvantage.

It is an object of the invention to mitigate this drawback. The invention provides a delay network comprising at least three storage/transfer elements each of which includes a storage capacitor, couplings between said elements so that said elements together form a shift register, first and second further couplings from a signal input to said shift register and from said shift register to a signal output respectively, a said further coupling comprising individual couplings to or from a plurality of said storage/transfer elements, and weighting-factor adjusting means included in a said coupling between said elements and/or in a said individual coupling forming part of said second further coupling so that said weighting-factor adjusting means is included in a signal path from said signal input to said signal output, said weighting-factor adjusting means comprising first and second field-effect transistor structures the channel regions of which have mutually different length-to-width ratios and the channel of the first of which is included in series with the corresponding coupling in such manner that one main electrode of said

first structure is connected to the storage capacitor of the corresponding storage/transfer element if the corresponding weighting-factor adjusting means is included in a said individual coupling and is connected to the storage capacitor of the first of the two corresponding storage/transfer elements if the corresponding weighting-factor adjusting means is included in a said coupling between said elements, said one main electrode of said first structure being effectively commoned with the corresponding main electrode of said second structure, both of said structures being integrated in the same semiconductor body.

Embodiments of the invention will be described in detail, by way of example with reference to the accompanying diagrammatic drawings, in which:—

Figure 1 shows the basic functional configuration of a first embodiment,

Figure 2 shows one possible construction for part of the embodiment of Figure 1, and

Figure 3 shows an alternative possible construction for part of the embodiment of Figure 1.

The delay network shown in Figure 1 comprises a plurality of delay sections 1, 2, 3, 4, a signal V_i which is applied to the first section 1 consecutively passing through this and the sections 2, 3 and 4. Each section delays the signal applied to its input by a certain amount. The signals at the outputs of each of the sections 1, 2, 3, 4 are fed to a common summing device 9 via individual weighting factor adjusting means 5, 6, 7 and 8, so that suitably chosen "weighted" signal portions are applied to the summing device 9 to give a desired transfer characteristic from V_i to an output V_o.

The delay network operates on the input signal in a digital manner, the sections 1—4 being constructed so that a signal in the form of an electric charge is shifted from one section to the next under the control of clock pulses, specific portions thereof being taken off and transferred to the summing device 9 by means of the weighting factor adjusting means. Thus the sections 1—4 form a shift register in a similar manner to the storage/transfer elements which form part of the network known from the aforesaid Patent Specification 1,427,626 (which proposes, as previously mentioned, an integrated circuit which employs pairs of field effect transistors as the various weighting factor adjusting means, one main electrode of each of the two transistors of each pair being connected to a storage capacitor included in a said storage/transfer element, the average of the gate voltages of the two transistors of each pair being the same and the difference between the gate voltages of the transistors of each pair determining the corresponding weighting factor).

The network of Figure 1 also employs such pairs of field effect transistors as weighting factor adjusting means. However, in contrast to the known network, the weighting factors given by the adjusting means 5—8 of Figure 1 are primarily determined by suitably choosing the relative ratios between the channel lengths L and widths W of the two field-effect transistors included in each adjusting means, only fine adjustment of the weighting factors thus obtained being achieved by superimposing a difference voltage on the otherwise equal gate electrode voltages of the relevant transistors.

Figure 2 shows inter alia a first possible construction for a single weighting factor adjusting means of Figure 1. Similarly to the weighting factor adjusting means disclosed in the said Patent Specification 1,427,626, the adjusting means of Figure 2 comprises two field effect transistors 11 and 12, which are connected both to a storage capacitor included in a storage/transfer element 13 of a CTD (corresponding to the shaft register 1, 2, 3, 4 of Figure 1) and to a balanced summing device 14 (corresponding to the device 9 of Figure 1). Signals V_i which are applied to the input of the CTD are shifted therethrough under the control of clock pulses T and therefore arrive at the element 13 after a given delay. The signals V_i may be applied in the form of voltages. Field-effect transistors are used in the weighting factor adjusting means rather than bipolar transistors in order to avoid unnecessary current loading of the CTD. The transistors are both formed in an integrated circuit by one and the same process and have channel lengths L_1 and L_2 and channel widths W_1 and W_2 respectively. The transmission factor α between element 13 and the summing device 14 is given to a first approximation by $\alpha=a+bv$, where a and b are effectively constants and 2v is the difference between the gate voltages of the transistors 11 and 12. The constants a and b depend on the settings of the transistors and are, to a first approximation, inversely proportional to $V-V_d$ (where V is the average gate voltage of the two transistors and V_d is the input threshold voltage of each) and also directly proportional to

$$\frac{W_1L_2-W_2L_1}{W_1L_2+W_2L_1}$$

In the aforesaid Patent Specification 1,427,626 it is assumed that the two transistors have identical geometries. If this is so and the weighting factor adjustment is

obtained by suitably choosing the difference between their two gate voltages, weighting factor adjustment gives rise to signal distortion, because a larger or smaller portion of upper harmonics of the signal applied to the adjusting means 11, 12, relative to the fundamental thereof, is fed to the summing device 14 *via* the transistors 11, 12 depending on the difference $2v$ between the gate voltages of the two transistors and on their average value.

In contradistinction to the known network, in the network of Figures 1 and 2 the gate voltages of the pair of field-effect transistors of each weighting factor adjusting means are substantially equal to each other and their value is, of course, preferably selected so as to minimize the adverse effect on the upper harmonics of the signal. The required weighting factors are primarily obtained by constructing the transistors included in each adjusting means, e.g. transistors 11 and 12 in Figure 2, to have channels which have mutually different length/width ratios L/W. Only fine adjustment of the weighting factor given by each adjusting means is obtained (if required) by creating a difference $2v$ between the gate voltages on the pair of transistors included in the corresponding adjusting means. These differences may be stored in a read-only memory (ROM), which may be integrated on the same semiconductor body as the CTD storage/transfer elements and the weighting factor adjusting means, the memory being programmed so that the desired fine adjustment of the weighting factors can be obtained with the required accuracy. The provisions required for this are denoted schematically by reference numeral 15 in Figure 2.

The summing device 14 in Figure 2 may be connected to the inputs of a push-pull output amplifier, which amplifies the signals which have been tapped off the storage/transfer element 13 and which have been weighted by the weighting factor adjusting means 11, 12, these signals appearing as difference signals on the two conductors of the summing device 14.

As an alternative to the arrangement shown in Figure 2, the output of one transistor of each adjusting means may be connected to a point of fixed potential, the outputs of the other transistors of the various weighting factor adjusting means each being connected to one of the two conductors of the summing device 14. Such an arrangement is shown in Figure 3, this Figure also showing that, if desired, negative weighting factors may be obtained by connecting the outputs of the relevant adjusting means to an opposite-sign-input of the summing device 14 (see adjusting means 11′, 12′ in Figure 3).

As an alternative to or in addition to the weighting factor adjusting means of the embodiments described weighting factor adjusting means may be provided in the network between the storage/transfer elements, so that a specific weighted portion of the output of each element is transferred to the input of the next element. This may be done by connecting the common sources of the two transistors of each weighting factor adjusting means to the output of one storage/transfer element, the drain of one transistor of the pair to the input of the next element, and the drain of the other transistor of the pair to a point of constant potential, e.g. earth. If this is done the input signal may be applied to various elements in parallel, the output being taken from the final element of the network, or the input signal may be applied to the first element of the network, the output then being taken from various elements via an adder.

WHAT WE CLAIM IS:—

1. A delay network comprising at least three storage/transfer elements each of which includes a storage capacitor, couplings between said elements so that said elements together form a shift register, first and second further couplings from a signal input to said shift register and from said shift register to a signal output respectively, a said further coupling comprising individual couplings to or from a plurality of said storage/transfer elements, and weighting-factor adjusting means included in a said coupling between said elements and/or in a said individual coupling forming part of said second further coupling so that said weighting-factor adjusting means is included in a signal path from said signal input to said signal output, said weighting-factor adjusting means comprising first and second field-effect transistor structures the channel regions of which have mutually different length-to-width ratios and the channel of the first of which is included in series with the corresponding coupling in such manner that one main electrode of said first structure is connected to the storage capacitor of the corresponding storage/transfer element if the corresponding weighting-factor adjusting means is included in a said individual coupling and is connected to the storage capacitor of the first of the two corresponding storage/transfer elements if the corresponding weighting-factor adjusting means is included in a said coupling between said elements, said one main electrode of said first structure being effectively commoned with the

corresponding main electrode of said second structure, both of said structures being integrated in the same semiconductor body.

2. A network as claimed in Claim 1, including means for applying substantially equal potentials to the gate electrodes of said first and second field-effect transistor structures.

3. A delay network as claimed in Claim 1, substantially as described herein with reference to Figs. 1 and 2 of the drawings or to Figs. 1 and 3 of the drawings.

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2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

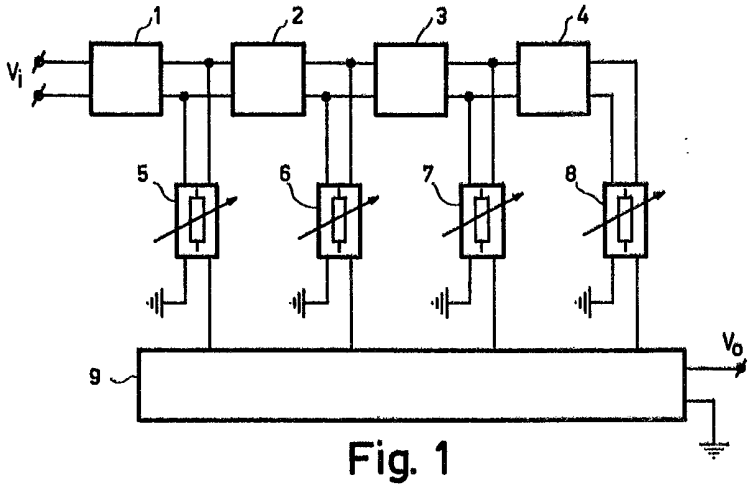

Fig. 1

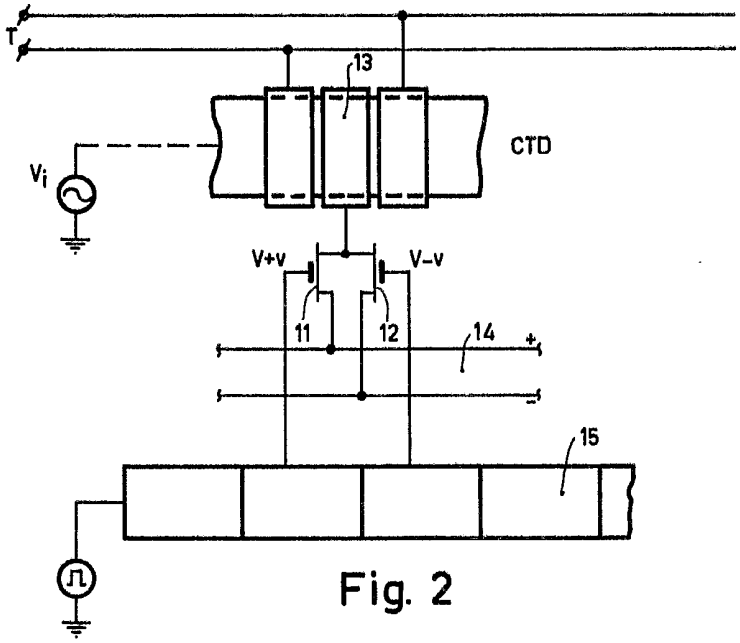

Fig. 2

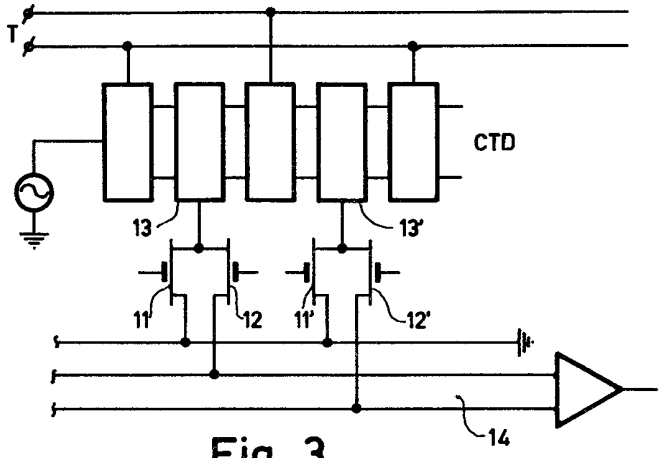

Fig. 3

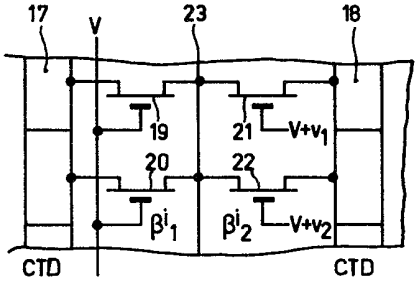

Fig. 4

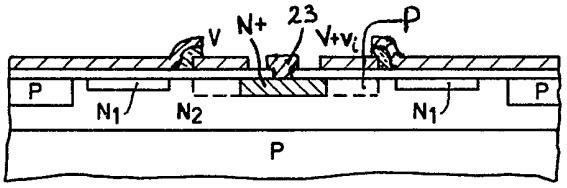

Fig. 5

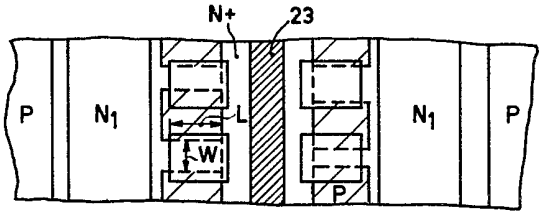

Fig. 6