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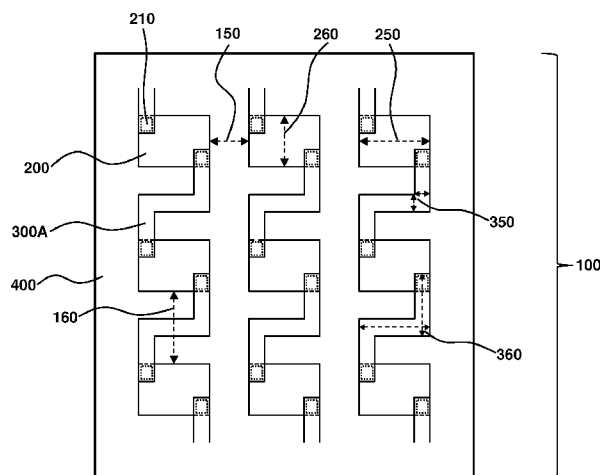


Figure 1A

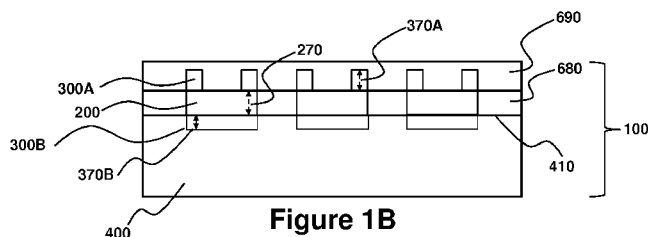


Figure 1B

(57) Abstract: Provided herein are electronic devices including arrays of printable light emitting diodes (LEDs) having device geometries and dimensions providing enhanced thermal management and control relative to conventional LED-based lighting systems. The systems and methods described provide large area, transparent, and/or flexible LED arrays useful for a range of applications in microelectronics, including display and lightning technology. Methods are also provided for assembling and using electronic devices including thermally managed arrays of printable light emitting diodes (LEDs).



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THERMALLY MANAGED LED ARRAYS ASSEMBLED BY PRINTING**CROSS-REFERENCE TO RELATED APPLICATIONS**

[001] This application claims the benefit of priority from U.S. Provisional Patent Application Nos. 61/486,487, filed May 16, 2011, and 61/608,839, filed March 9, 2012, each of which is hereby incorporated by reference in its entirety.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[002] This invention was made with United States governmental support under Award No. DEFG02-91ER45439 awarded by the U.S. Department of Energy. The U.S. government has certain rights in the invention.

BACKGROUND

[003] This invention is in the field of printable electronics and optical systems. This invention relates generally to methods for making and assembling electronic devices and printable electronic devices, including light devices such as arrays of light emitting diodes.

[004] A variety of platforms are available for fabricating and assembling printable structures and/or device components on substrates, including printing based assembly of nano- and micro-structures for applications in macroelectronics, flexible electronics, and optical systems (e.g., photovoltaics, displays, lighting, etc.). For example, a number of patents and patent applications describe different methods and systems for making and printing a wide range of structures, including U.S. Patent Nos. 7,195,733, 7,557,367, 7,622,367 and 7,521,292, U.S. Patent Application Publication Nos. 2009/0199960, 2007/0032089, 2008/0108171, 2008/0157235, 2010/0059863, 2010/0052112, 2010/0002402, 2010/0283069 and 2010/0317132, and U.S. Patent Application Nos. 13/046,191 (filed 03/11/2011); all of which are hereby incorporated by reference in their entireties to the extent not inconsistent herewith.

SUMMARY

[005] Provided herein are electronic devices including arrays of printable light emitting diodes (LEDs) having device geometries and dimensions providing enhanced thermal management and control relative to conventional LED-based lighting systems. LED arrays of some embodiments, for example, have physical dimensions and form factors that distribute high quality single crystalline semiconductor LEDs so as to achieve a combination of high performance attributes (e.g., useful luminous efficacy, radiant power, and power consumption) and beneficial thermal properties (e.g., useful heat dissipation rates and maximum LED temperatures for reasonable power consumptions). The systems and methods described provide large area, transparent, and/or flexible LED arrays useful for a range of applications in microelectronics, including display and lightning technology. Methods are also provided for assembling and using electronic devices including thermally managed arrays of printable light emitting diodes (LEDs).

[006] Devices of some aspects of the invention utilize printable semiconductor diode structures provided in a sparse array device geometry to achieve useful radiant output characteristics while efficiently managing heat generation and dissipation. Devices of some aspects of the invention utilize printable semiconductor LED structures characterized by a size scale small enough so as to access efficient passive heat dissipation by other structures and/or components of the device array. In some embodiments, printable LEDs having micro- and/or nano-sized physical dimensions are interconnected by electrical interconnects having physical dimensions and physical properties, such as thermal mass and thermal conductivity, such that they simultaneously function to electrically interconnect the LEDs in the array and efficiently dissipate heat generated by the LEDs in the array. In some embodiments, the physical dimensions of the LEDs and electrical interconnects are selected such that the electrical interconnects function as efficient heat sinks during operation of the device. In some embodiments, the LED arrays of embodiments have component dimensions and geometries such that electrical interconnects of the device provide an effective route for passively cooling the device during operation. Accordingly, device geometries and LED dimensions of the present systems are

useful for reducing peak operating temperatures so as to avoid temperatures wherein LED performance, longevity and functionality is degraded or destroyed.

[007] Aspects of the invention provide device geometries and process strategies for efficiently distributing semiconductor material in the form of thin printable LED structures on a substrate to achieve LED arrays exhibiting useful radiant and thermal management properties, for example. Benefits of the present include providing an economically viable and technically robust platform for assembling a wide variety of displays systems including large area display devices, flexible display devices and plastic electronics.

[008] In an embodiment, for example, provided is an electronic device comprising: a substrate; an array of light emitting diodes (LEDs) supported by the substrate, the array of LEDs comprising: a plurality of printable light emitting diode (LED) elements, wherein each LED element in the array of LEDs has one or more lateral dimensions, and optionally all lateral dimensions, less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm , and wherein a spacing between adjacent LED elements in the array of LEDs is greater than or equal to at least one lateral dimension of an LED element in the array; and a plurality of electrical interconnects, wherein each LED element in the array of LEDs is positioned in electrical communication and thermal communication with at least two of the plurality of electrical interconnects, wherein each of the electrical interconnects has lateral dimensions and a thickness large enough to provide dissipation of heat from the array of LEDs at a rate greater than or equal to $5 \mu\text{J s}^{-1}$. In an embodiment, for example, the lateral dimensions and a thickness of the interconnects is large enough to provide dissipation of heat from the array of LEDs at a rate equal to or greater than the heat power. In an embodiment, each of the electrical interconnects is in physical contact with one or more of the printable LED elements of the array.

[009] In an embodiment, for example, provided is an electronic device comprising: a substrate; and an array of light emitting diodes (LEDs) supported by the substrate, the array of LEDs comprising: a plurality of printable LED elements, wherein each LED element in the array of LEDs has one or more lateral dimensions, and optionally all lateral dimensions, less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm , and wherein a spacing between adjacent

LED elements in the array of LEDs is greater than or equal to 2 μm ; and a plurality of electrical interconnects, wherein each LED element in the array of LEDs is positioned in electrical communication with at least two of the plurality of electrical interconnects, wherein each of the electrical interconnects is characterized by lateral dimensions and an average thickness. In an embodiment, LED elements of the array are provided in a sparse geometry. In an embodiment, each of the electrical interconnects is in thermal communication and/or physical contact with one or more of the printable LED elements of the array.

[0010] In an embodiment, an electronic device further comprises one or more encapsulating layers provided to at least partially encapsulate one or more components of the array. In an embodiment, for example, the device further comprises an encapsulating layer provided on at least a portion of the array, wherein the encapsulating layer has a thickness selected over the range of 1 μm to 10 mm, and optionally a thickness selected over the range of 10 μm to 1 mm. In an embodiment, the device further comprises one or more adhesive layers on a receiving surface of the substrate for affixing at least a portion of the LED elements. In an embodiment, the device further comprises one or more planarizing layers on a receiving surface of the substrate for planarizing at least a portion of the LED elements. In an embodiment, an electronic device further comprises one or more planarizing layers on a receiving surface of the substrate for accommodating at least a portion of the LED elements. In an embodiment, the printable LED elements of the array and/or the electrical interconnects are positioned proximate to the neutral mechanical surface of the electronic device.

[0011] In an embodiment, one or more of the electrical interconnects are stretchable or flexible interconnects, for example, provided in a bent configuration and/or at least partially not in physical contact with the substrate. In an embodiment, the electronic device has an island - interconnect geometry wherein the printable LED elements comprise device island and the electrical interconnects provide bridge structures between the LED elements, for example, wherein the electrical interconnects provide bridge structures comprising stretchable interconnects.

[0012] Thermally managed devices are also provided herein, wherein the physical dimensions, properties and integration of individual LED structures and

electrical interconnect structures of the array are selected to achieve efficient dissipation of heat generated by the LEDs during operation, for example, so as to avoid peak operating temperatures capable of degrading LED performance and longevity. Electronic device embodiments are provided, for example, wherein the physical dimensions of the electrical interconnects of the array, such as lateral dimensions and thickness dimensions, are sufficiently large to provide heat dissipation from each of the LEDs in the array during operation at rate selected over the range of $5 \mu\text{J s}^{-1}$ to 100 J s^{-1} , and optionally for some applications selected over the range of $5 \mu\text{J s}^{-1}$ to 5 J s^{-1} . Certain embodiment are provided, for example, wherein the physical dimensions of electrical interconnects, such as lateral dimensions and thickness dimension, are sufficiently large to provide a maximum temperature of each of the LEDs in the array less than or equal to 373 K for a power consumption equal to or greater than $5 \mu\text{W}$.

[0013] In some devices of this aspect, the thermal properties of the electrical interconnects are selected so as to achieve efficient dissipation of heat generated by the LED structures of the array during operation. In an embodiment, for example, the heat capacity of the electrical interconnects is greater than or equal to $7.3 \times 10^{-11} \text{ J/K}$ per LED in the array and optionally selected from the range of $7.3 \times 10^{-11} \text{ J/K}$ to $7.3 \times 10^{-10} \text{ J/K}$ per LED in the array. In an embodiment, for example, the electrical interconnects of the array have an average heat capacity that is equal to or greater than $7.3 \times 10^{-11} \text{ J/K}$, and optionally selected from the range of $7.3 \times 10^{-11} \text{ J/K}$ to $7.3 \times 10^{-10} \text{ J/K}$. In an embodiment, for example, the specific heat capacity of the electrical interconnect is $2.422 \text{ J/cm}^3/\text{K}$ and the specific heat capacity of the LEDs, such as GaN LEDs, is $2.99 \text{ J/cm}^3/\text{K}$. In an embodiment, for example, the volumetric specific heat capacity of an interconnect is $2.422 \text{ J/cm}^3/\text{K}$ and, thus, a heat capacity of $7.3 \times 10^{-11} \text{ J/K}$ is obtained for an interconnect volume equal to approximately $30 \mu\text{m}^3$.

[0014] In an embodiment, the average thermal conductivity of the electrical interconnects is larger than the average thermal conductivity of that of the LED elements. In an embodiment, for example, the average thermal conductivity of each of the electrical interconnects is a factor of 0.4 to 50 of the average thermal conductivity of the LED elements, and optionally wherein the average thermal

conductivity of each of the electrical interconnects is a factor of 0.44 to 1.54 of the average thermal conductivity of the LED elements. Electronic devices of this aspect are provided, for example, wherein the thermal conductivity of each of the interconnects is 70, 160, or 247 W/m/k and the thermal conductivity of the LEDs, such as GaN LEDs, is 160W/m/k.

[0015] In some devices of this aspect, LEDs of the array are provided in a sparse device geometry. As used herein, a “sparse geometry” refers to arrays having sufficient spacing between adjacent LEDs in the array to allow effective thermal management, while also providing radiant properties useful for a given optical application. Sparse geometries useful in embodiments include a diffuse assembly of LEDs printed onto a device substrate and/or arrays characterized by low spatial densities of LEDs. In embodiments, for example, arrays of electronic devices feature a density of the LED elements less than or equal to 100 LEDs mm⁻², optionally for some applications less than or equal to 10 LEDs mm⁻², and optionally for some applications less than or equal to 1 LED mm⁻². In an embodiment, for example, embodiments provide a thermally managed device having an array with a density of the LED elements less than or equal to 81 LEDs mm⁻², and optionally for some applications a density of the LED elements selected over the range of 1 to 81 LEDs mm⁻². In an embodiment, for example, the spacing between adjacent LED elements in the array of LEDs is greater than or equal to 2 μm and optionally for some applications greater than or equal to 10 μm. As used herein, the term “spacing” with reference to LED structures in an LED array refers to the shortest distance separating adjacent LEDs in the array. In an embodiment, for example, the spacing between adjacent LED elements in the array of LEDs is selected over the range of 2 μm to 10 cm, and optionally for some applications selected over the range of 10 μm to 100 μm. In an embodiment, for example, the array has an average spacing between adjacent LED elements selected over the range of 10 μm to 1 μm, and optionally for some applications selected over the range of 2 μm to 100 μm. In an embodiment, thermally managed devices are provided having an array comprising LEDs with lateral dimensions equal to or less than 10 μm, wherein the spacing between adjacent LEDs in the array is greater than or equal to 2 μm.

[0016] In some devices of this aspect, the physical dimensions of the LEDs of the array are selected so as to achieve efficient heat removal via electrical interconnect components provided in thermal communication with the LEDs. In an embodiment, for example, each LED element in the array of LEDs has one or more, and optionally all, lateral dimensions less than or equal to 500 μm , and optionally for some applications less than or equal to 100 μm . In an embodiment, for example, provided is a device wherein the lateral dimensions of each of the LED elements are selected over the range of 10 μm to 500 μm , and optionally for some applications wherein each of the LED elements in the array has average lateral dimensions selected over the range of 10 μm to 500 μm . In an embodiment, for example, the thickness dimension of each of the LED elements is less than or equal to 50 μm , and optionally for some embodiments less than or equal to 10 μm . In an embodiment, for example, the thickness dimension of each of the LED elements is selected over the range of 500 nm to 50 μm , and optionally for some applications 1 μm to 50 μm . In an embodiment, for example, each of the LED elements in the array has an average thickness dimension selected over the range of 500 nm to 50 μm and optionally for some applications 1 μm to 50 μm . In an embodiment, for example, an electronic device of the invention features one or more lateral dimensions of each LED element, and optionally all lateral dimensions of each LED element, selected over the range of 10 μm to 500 μm , selected over the range of 50 μm to 300 μm , or selected over the range of 50 μm to 250 μm . In an embodiment, for example, the thickness of each LED element is selected over the range of 30 nm to 500 nm, selected over the range of 50 nm to 300 nm or selected over the range of 100 nm to 200 nm. In an embodiment, for example, each of the electrical interconnects has a thickness selected over the range of 300 nm to 5 μm , selected over the range of 500 nm to 2000 nm, selected over the range of 500 nm to 800 nm or selected over the range of 1000 nm to 1500 nm. In an embodiment, for example, each of the electrical interconnects has one or more lateral dimensions, and optionally all lateral dimensions, selected over the range of 10 μm to 100 mm, selected over the range of 100 μm to 100 mm or selected over the range of 200 μm to 100 mm.

[0017] In some devices of this aspect, the physical dimensions of the electrical interconnects of the array are selected so that they efficiently dissipate heat generated by the LEDs of the array during operation. In an embodiment, for

example, each of the electrical interconnects has an average thickness greater than or equal to 10 nm, and optionally for some applications greater than or equal to 100 nm, and optionally for some applications greater than or equal to 300 nm, and optionally for some applications, greater than or equal to 1 μm . In an embodiment, for example, each of the electrical interconnects has an average thickness selected over the range of 10 nm to 100 μm , and optionally for some applications selected over the range of 300 nm to 100 μm . In an embodiment, for example, each of the electrical interconnects has a thickness greater than or equal to 10 nm, and optionally for some applications greater than or equal to 300 nm, and optionally for some applications greater than or equal to 1 μm . In an embodiment, for example, each of the electrical interconnects has an average thickness selected over the range of 10 nm to 1.5 μm , and optionally for some applications selected over the range of 300 nm to 1 μm . In an embodiment, for example, each of the electrical interconnects has lateral dimensions selected over the range of 10 μm to 10 cm, and optionally for some applications selected over the range of 500 μm to 100 mm. As used herein, "lateral dimensions" refer to dimensions perpendicular to the thickness dimension, and optionally dimensions parallel to a receiving surface of the substrate. Lateral dimensions include, for example, length and width dimensions. In embodiments, the term "thickness" refers to a dimension of a component perpendicular to a supporting substrate.

[0018] Electronic devices of this aspect are compatible with a wide range of LED devices, device geometries and device configurations, including LED structures that are assembled on the receiving surface of the substrate via printing-based techniques such as dry transfer contact printing or solution printing. In an embodiment, for example, each LED element in the array comprises a vertical type LED. In an embodiment, for example, each LED element in the array is encapsulated by one or more polymer encapsulants, such as one or more elastomer encapsulating layers. In an embodiment, for example, a plurality of the LED elements is electrically connected in a series configuration. In an embodiment, for example, a plurality of the LED elements is electrically connected in a parallel configuration. In an embodiment, for example, each of the LED elements in the array is independently electrically addressable. In an embodiment, for example, the LED array consumes a power selected over the range of 5 μW to 100 W, and

optionally selected over the range of 5 μ W to 5 W. In an embodiment, for example, the LED array has a luminous efficacy greater than or equal to 0.1 lm/W, and/or optionally for some applications a luminous efficacy selected over the range of 0.1 lm/W to 250 lm/W.

[0019] Electronic devices of this aspect are compatible with LEDs comprising a wide range of semiconductor materials. In an embodiment, for example, the LEDs of the array comprise printable semiconductor structures, for example, semiconductor structures that are assembled via soft lithography printing techniques such as dry transfer contact printing. In an embodiment, for example, the LEDs of the array comprise one or more inorganic semiconductor materials including single crystalline inorganic semiconductors, polycrystalline semiconductors and doped semiconductors. In an embodiment, for example, each LED element independently comprises a material selected from the group consisting of: GaN, p-type GaN, n-type GaN, InGaN, AlGaIn and any combination of these. In an embodiment, for example, each LED element independently comprises a material selected from the group consisting of: a semiconductor, Si, Ga, Al, N, As, P, In and any combination of these. In an embodiment, for example, each LED element independently comprises a material selected from the group consisting of: GaN, GaP, AlN, GaAs, InAlP, AlGaAs, AlGaIn, InGaP, InGaIn, AlGaInP, and any combination of these.

[0020] A range of electrical interconnect geometries and materials are useful in the devices described herein. In embodiments, electrical interconnects are positioned in both electrical contact and thermal contact with LEDs in the array. In an embodiment, the plurality of electrical interconnects provides a current path to and from one or more LED elements. In an embodiment, the plurality of electrical interconnects provides a path for flow of heat generated by one or more LED elements. In an embodiment, the plurality of electrical interconnects functions as a heat sink for heat generated by one or more LED elements. In an embodiment, the plurality of electrical interconnects provides electrical interconnects between individual LED elements. In an embodiment, each of the electrical interconnects comprises a thin film structure. In an embodiment, each of the electrical interconnects comprises a unitary structure. In an embodiment, each of the electrical interconnects independently comprises a metal, for example, a metal

selected from the group consisting of aluminum, copper, gold, platinum, nickel, titanium or any combination of these. In certain embodiments, metals useful for electrical interconnects of devices of this aspect include metals capable of use in sputtering or e-beam evaporation systems.

[0021] A range of substrate geometries and materials are useful in the devices of this aspect. In an embodiment, the substrate has a receiving surface for supporting the LED elements and electrical interconnects. The LED elements and/or electrical interconnects may be in physical contact with the substrate or alternatively in physical contact with one or more intermediate structures (e.g., layers) provided between the LED elements and/or electrical interconnects and the substrate. In some embodiments, for example, the receiving surface has an adhesive layer to receive and secure the LED elements and/or the electrical interconnects on the substrate. In some embodiments, for example, the receiving surface has a planarizing layer to receive and accommodate the LED elements and/or the electrical interconnects, thereby planarizing the LED elements and/or the device. In some embodiments, for example, the receiving surface has an encapsulating layer to receive and at least partially encapsulate the LED elements and/or the electrical interconnects. Useful adhesive layers, planarizing layers and encapsulating layers for some applications include polymer layers and/or prepolymer layers. In an embodiment, the receiving surface is planar. Alternatively, useful substrates have a contoured receiving surface, such as a convex surface, a concave surface or a surface having a plurality of convex and/or concave regions. In an embodiment, the substrate is a flexible substrate, such as a polymer substrate. In an embodiment, the substrate is at least partially optically transparent, for example, at least partially optically transparent in the visible region of the electromagnetic spectrum or at least partially optically transparent in the ultraviolet region of the electromagnetic spectrum. In an embodiment, the substrate comprises a dielectric material. In an embodiment, the substrate comprises a material selected from the group consisting of: a flexible material, a stretchable material, an inorganic material, a ceramic, a polymer, an elastomer and any combination of these. In an embodiment, the substrate comprises a material selected from the group consisting of: a polymer, an inorganic polymer, an organic polymer, a plastic, an elastomer, a biopolymer, a thermoset, a rubber, fabric, paper, silk, a hydrogel and any combination of these.

[0022] Additional optical and device components are useful with the devices and methods described herein. In one embodiment, a device of this aspect further comprises an array of phosphors positioned in optical communication with the LED array. In a specific embodiment, an array of phosphor elements is provided, for example, as a polymer mold at least partially encapsulating an array of phosphor elements. In specific embodiments, phosphor elements useful with devices and methods described herein include those having one or more lateral dimensions, and optionally all lateral dimensions, less than or equal to 1000 μm , and optionally for some applications having lateral dimensions matching underlying LED elements. In some embodiments, phosphor elements useful with the devices and methods described herein include those having one or more thickness dimensions selected over the range of 50 μm to 250 μm , or optionally for some applications selected over the range of 60 μm to 105 μm . In embodiments, devices of this aspect optionally further comprise an optical diffuser positioned in optical communication with the LED array and/or a phosphor array, if present in the device. For certain embodiments, an optical diffuser has a thickness greater than 1 μm . Optionally, an optical diffuser has a thickness greater than 10 μm . In certain embodiments, a phosphor array and/or an optical diffuser are laminated over the top of an LED array. In some embodiments, spacing layers and/or adhesive layers are provided between an LED array and a phosphor array. In some embodiments, spacing layers and/or adhesive layers are provided between an LED array and an optical diffuser. In certain embodiments, both phosphor arrays and optical diffusers are incorporated into devices of this aspect, with optional spacing layers and/or adhesive layers positioned adjacent to each. Useful spacing layers and/or adhesive layers include polymer and prepolymer layers.

[0023] In an embodiment, for example, the electronic device further comprises a phosphor patterned polymer layer in optical contact with the array of printable LED elements, the phosphor patterned polymer layer having a plurality of phosphor-containing reservoirs aligned with one or more of the printable LED elements such that electromagnetic radiation from the printable LED elements is transmitted to the phosphor-containing reservoirs. In an embodiment, for example, the electronic device further comprises a thin film optical diffuser in optical contact with the array of printable LED elements such that electromagnetic radiation from the printable LED

elements or the phosphor-containing reservoirs in optical communication with the printable LED elements is transmitted through the thin film optical diffuser.

[0024] In another aspect, provided are methods of making electronic devices. Specific embodiments of this aspect provide methods for making electronic devices, for example devices described in the above aspects. One embodiment of this aspect comprises the steps of providing a substrate; assembling a plurality of printable LED elements onto the substrate by transfer printing the printable LED elements onto a receiving surface of the substrate, thereby making an array of LED elements, wherein each LED element has one or more lateral, and optionally all lateral dimensions, dimensions less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm and wherein a spacing between adjacent LED elements in the array of LED elements is greater than or equal to at least one lateral dimension of an LED element in the array of LED elements; providing a plurality of electrical interconnects to the array of LED elements, wherein each LED element in the array of LED elements is positioned in electrical communication and thermal communication with two or more of the plurality of electrical interconnects, wherein each of the electrical interconnects has lateral dimensions and an average thickness large enough to provide dissipation of heat from the array of LED elements at a rate greater than or equal to 5 $\mu\text{J s}^{-1}$. In an embodiment, the step of assembling a plurality of printable LED elements onto the substrate by transfer printing the printable LED elements onto a receiving surface of the substrate is achieved via dry contact transfer printing.

[0025] In an embodiment, for example, the invention provides a method of making an electronic device comprising the steps of: (1) providing a substrate; (2) assembling a plurality of printable LED elements onto the substrate by transfer printing the printable LED elements onto a receiving surface of the substrate, thereby making an array of LED elements, wherein each LED element has one or more lateral dimensions less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm and wherein a spacing between adjacent LED elements in the array of LED elements is greater than or equal to 2 μm ; (3) providing a plurality of electrical interconnects to the array of LED elements, wherein each LED element in the array of LED elements is positioned in electrical communication with two or more

of the plurality of electrical interconnects, wherein each of the electrical interconnects is characterized by lateral dimensions and an average thickness, thereby making the electronic device.

[0026] In an embodiment, for example, the invention provides a method of making an electronic device further comprising the steps of (1) providing a conformal patterning device, such as an elastomeric stamp, (2) contacting at least a portion of the printable LED elements with a conformable transfer device having a contact surface, wherein contact between the contact surface and the printable LED elements binds at least a portion of the printable LED elements to the contact surface, thereby forming the contact surface having the printable LED elements disposed thereon; (3) contacting the printable LED elements disposed on the contact surface with the receiving surface of the substrate; and (4) separating the contact surface of the conformable transfer device and the printable LED elements, wherein the LED elements are transferred onto the receiving surface, thereby assembling the printable LED elements on the receiving surface of the substrate. In an embodiment, for example, the printable LED elements are provided in a selected pattern, for example providing a preselected spacing between adjacent printable LED elements, and the selected pattern is maintain using the transfer printing process, for example, by maintaining the relative positions and orientations of the printable LED elements during transfer printing. In an embodiment, for example, conformal contact is established between the contact surface of the conformable transfer device and external surfaces of the printable LED elements. In an embodiment, for example, conformal contact is established between the contact surface having the printable LED elements disposed thereon and the receiving surface of the substrate. In an embodiment, for example, an adhesive layer is provided on the receiving surface, wherein the printable LED elements are contacted with the adhesive layer during transfer of the printable LED elements to the receiving surface of the substrate.

[0027] In an embodiment, a method of the invention further comprises the step of generating the printable LED elements via epitaxial growth of a semiconductor multilayer structure on a host substrate, for example, wherein the semiconductor multilayer structure is an InGaN multilayer. In an embodiment, the method further comprises selectively removing material from the InGaN multilayer so as to generate

a plurality of InGaN multilayer relief structures on the host substrate, for example, wherein the InGaN multilayer relief structures are defined lithographically. In an embodiment, the method further comprises at least partially releasing the InGaN multilayer relief structures so as to generate freestanding InGaN multilayer structures or InGaN multilayer structures at least partially physically separated from the host substrate, for example, wherein the InGaN multilayer structures are connected to the host substrate via a supporting anchor structure, such as an uncut GaN anchor structure. In an embodiment, the step of at least partially releasing the InGaN multilayer relief structures generates the printable LED elements. In an embodiment, the method further comprises depositing one or more metal contact pads on the InGaN multilayer and/or the InGaN multilayer relief structures.

[0028] In an embodiment, the host substrate is a Si host substrate having a (111) orientation, and the step of at least partially releasing the InGaN multilayer relief structures comprises: (i) selectively removing material from the InGaN multilayer by vertically etching through selected regions of the InGaN multilayer to a selected depth in the Si host substrate, thereby generating a plurality of recessed regions in the Si host substrate having the (111) orientation; and (ii) anisotropically etching the Si host substrate, wherein etching occurs along $\langle 110 \rangle$ directions of the Si host between the recessed features. In an embodiment, the step of anisotropically etching the Si host substrate is achieved by exposure to a solution of KOH, such as a solution of KOH at a temperature greater than 298 K. In an embodiment, the host substrate is a sapphire host substrate, wherein the step of at least partially releasing the InGaN multilayer relief structures comprises exposing one or more interfaces between the sapphire host substrate and the InGaN multilayer structures to electromagnetic radiation, such as electromagnetic radiation having a power, wavelength, fluence or any combination of these to provide for decomposition of GaN at the interface, thereby generating Ga metal and nitrogen gas.

[0029] In embodiments, methods of this aspect incorporate phosphors into electronic devices. A specific method of this aspect further comprises the steps of providing a phosphor-containing island mold comprising an array of phosphor-containing islands at least partially encapsulated in a polymer mold; and providing the phosphor-containing island mold on the electronic device, wherein at least a

portion of the phosphor-containing islands are positioned in optical communication with at least a portion of the LED elements. Optionally, the array of phosphor-containing islands is supported by and/or aligned over the array of LED elements. Optionally, the array of phosphor-containing islands are in physical contact with the array of LED elements. Useful phosphor arrays include those incorporated into a phosphor-containing island mold, as described above.

[0030] Methods of this aspect optionally utilize a strategy for forming self-aligned vias, for example vias useful for providing positions for thermal and electrical communication between an LED element and electrical interconnects. In a specific embodiment, a method for making an electronic device further comprises the steps of providing a photosensitive prepolymer layer over the array of LED elements, thereby encapsulating the array of LED elements; exposing portions of the photosensitive prepolymer layer to electromagnetic radiation, wherein the electromagnetic radiation is passed through the substrate and portions of the array of LED elements, thereby forming developed portions and undeveloped portions of the photosensitive prepolymer layer; and removing the undeveloped portions of the photosensitive prepolymer layer, thereby exposing portions of each LED element in the array of LED elements. In certain embodiments, the prepolymer layer is exposed to ultraviolet electromagnetic radiation.

[0031] In another aspect, provided are methods for generating electromagnetic radiation, for example methods for generating electromagnetic radiation using an electronic device comprising a substrate and an array of LEDs supported by the substrate. A specific method of this aspect comprises the steps of providing an electronic device comprising a substrate and an array of LEDs supported by the substrate, the array of LEDs comprising a plurality of printable LED elements, wherein each LED element in the array of LEDs has one or more lateral dimensions less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm , and wherein a spacing between adjacent LED elements in the array of LEDs is greater than or equal to at least one lateral dimension of an LED element in the array, and the array of LEDs further comprises a plurality of electrical interconnects, wherein each LED element in the array of LEDs is positioned in electrical communication and thermal communication with at least two of the plurality of

electrical interconnects, wherein each of the electrical interconnects has lateral dimensions and an average thickness large enough to provide dissipation of heat from the array of LEDs at a rate greater than or equal to $5 \mu\text{J s}^{-1}$; and providing a voltage and/or current across two or more of the plurality of electrical interconnects to generate electromagnetic radiation from at least a portion of the array of LEDs.

[0032] In an embodiment, for example, the invention provides a method of generating electromagnetic radiation comprising the steps of: (1) providing an electronic device comprising: a substrate; and an array of light emitting diodes (LEDs) supported by the substrate, the array of LEDs comprising: a plurality of printable LED elements, wherein each LED element in the array of LEDs has one or more lateral dimensions less than or equal to $1000 \mu\text{m}$ and a thickness dimension less than or equal to $50 \mu\text{m}$, and wherein a spacing between adjacent LED elements in the array of LEDs is greater than or equal to $2 \mu\text{m}$; and a plurality of electrical interconnects, wherein each LED element in the array of LEDs is positioned in electrical communication with at least two of the plurality of electrical interconnects, wherein each of the electrical interconnects is characterized by lateral dimensions and an average thickness; and (2) providing a voltage across two or more of the plurality of electrical interconnects, thereby generating electromagnetic radiation from at least a portion of the array of LEDs.

[0033] As described above, various parameters of the LED elements, electrical interconnects, and device configurations can be selected to achieve efficient heat removal from the LED elements while they are generating light. In an embodiment, the lateral dimensions and the average thickness of the interconnects are provided with large enough dimension to provide heat dissipation from each LED in the array sufficient to maintain a steady state temperature of each LED in the array less than or equal to 373 K , for example, for a power consumption equal to or greater than $5 \mu\text{W}$. In an embodiment, for example, each of the electrical interconnects has an average thickness greater than or equal to 300 nm . In an embodiment, for example, the LED array consumes power equal to or greater than $5 \mu\text{W}$. Optionally, the LED array is assembled on the substrate using a dry transfer contact printing method. In one embodiment, an electronic device further comprises a controller positioned in electrical communication with the plurality of electrical interconnects. A controller is

useful for aspects of the methods and devices described herein for selecting one or more individual LED elements for generation of light. Specific electrical configurations of LED elements in an array, for example multiple LED elements in a series configuration, multiple LED elements in a parallel configuration or independently addressable LED elements further enhance the utility of a controller.

[0034] In certain embodiments, the components of electronic devices described herein can be optimized for generation of electromagnetic radiation of a specific wavelength or wavelength region. For example, in one embodiment, electromagnetic radiation generated by an electronic device described herein has a wavelength or wavelength range selected over the range of 350 nm to 800 nm. Optionally, an array of phosphors is incorporated into an electronic device. Devices incorporating an array of phosphors optionally provide an additional level of configurability in the selection of output electromagnetic radiation. In one embodiment, an array of phosphor absorbs at least a portion of electromagnetic radiation generated by an LED array and emits electromagnetic radiation having a wavelength or wavelength range selected over the range of 400 nm to 800 nm. Specific configurations, for example phosphor thickness and identity, can be used to further tune the output electromagnetic energy. In an exemplary embodiment, the phosphor array and LED array together generate electromagnetic radiation having an x chromaticity coordinate in a CIE 1931 color space selected over the range of 0.25 to 0.4. In an exemplary embodiment, the phosphor array and LED array together generate electromagnetic radiation having an y chromaticity coordinate in a CIE 1931 color space selected over the range of 0.25 to 0.45.

[0035] Various features discussed here in relation to one or more of the exemplary embodiments can be incorporated into any of the described aspects of the present invention alone or in any combination. Certain exemplary aspects of the invention are set forth herein. It should be understood that these aspects are presented merely to provide the reader with a brief summary of certain forms the invention might take and that these aspects are not intended to limit the scope of the invention. Indeed, the invention may encompass a variety of aspects that may not be explicitly set forth herein as would be understood by one of ordinary skill in the relevant art without undue experimentation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0036] Figure 1. Figure 1A provides a top plan view of an electronic device and Figure 1B provides a side view of an electronic device.

[0037] Figure 2. Schematic illustration of arrays of InGaN μ -LED arrays (A) before and (B) after anisotropic etching of the near-interfacial region of a supporting Si (111) wafer. The colors correspond to the InGaN (light blue), the contact pads (gold) and a thin current spreading layer (red). SEM images of a dense array of μ -LEDs on a Si (111) wafer (C) before and (D) after this type of anisotropic etching process. The insets provide magnified views (colorized using a scheme similar to that in A). SEM images of the region of the μ -LED structure that connects to the underlying silicon wafer (E) before and (F) after etching. Break-away anchors serve as fracture points during retrieval of μ -LEDs from the Si (111) wafer. SEM images of a representative μ -LED, shown in sequence, (G) after undercut, (H) after removal from the Si wafer, and (I) after assembly onto a receiving substrate (colorized for ease of viewing).

[0038] Figure 3. SEM images of the interconnection process for a representative InGaN μ -LED, shown in sequence, (A) after assembly onto an optically transparent substrate (e.g. glass or plastic), (B) after spin-coating a photo-sensitive polymer, (C) after self-aligned via formation using a back-side exposure process, and (D) after deposition and patterning of a metallic interconnect layer. The colorized regions correspond to the contact pads (gold), a thin current spreading layer (red) and Al interconnects (green). Optical images of various lighting modules based on arrays of μ -LEDs (E) plastic and (F,G) glass substrates.

[0039] Figure 4. SEM images of arrays of released InGaN μ -LEDs with dimensions from (A) $25 \times 25 \mu\text{m}^2$, (B) $50 \times 50 \mu\text{m}^2$, (C) $75 \times 75 \mu\text{m}^2$ to (D) $150 \times 150 \mu\text{m}^2$. The colorized regions correspond to the contact pads (gold), and thin current spreading layers (red). (E) Corresponding current density-voltage (J-V) characteristics for μ -LEDs with the dimensions shown in (A). The inset provides a plot of current density as a function of μ -LED area, measured at 6V. (F) Current density-voltage (J-V) characteristics and emission spectrum (inset) of a

representative device before undercut etching on the Si wafer, and after assembly onto a glass substrate.

[0040] Figure 5. (A) Schematic illustration of the process for fabricating flexible, white lighting modules, achieved by integrating patterned, encapsulated tiles of YAG:Ce phosphor-containing islands with arrays of InGaN μ -LEDs. (B) Color chromaticity plotted on a CIE 1931 color space diagram for μ -LEDs integrated with phosphors with thicknesses of 60 μm , 80 μm , and 105 μm . Optical images of a fully interconnected array of μ -LEDs (C) without phosphor, (D) with a laminated film of encapsulated YAG:Ce phosphor-containing islands ($500 \times 500 \mu\text{m}^2$), and (E) with a laminated diffuser film.

[0041] Figure 6. (A) Schematic illustration of the device geometry and parameters used in the analytical model of heat flow. (B-G) Temperature distributions for isolated InGaN μ -LEDs with Al interconnects (300 nm and 1000 nm thick for (B-D) and (E-G), respectively) at input powers of (B) 7.8 mW, (C) 16.4 mW, (D) 25.2 mW, (E) 8.4 mW, (F) 18.0 mW, (G) 27.6 mW captured using a QFI Infra-Scope Micro-Thermal Imager (left) and calculated by analytical models (right). (H) Surface temperature for μ -LEDs with Al interconnect thicknesses of 300 nm (black) and 1000 nm (red) extracted from experiments (dots) and computed using the analytical model (lines) as a function of input power. (H) 3D plot of the surface temperature as function of device size and interconnect thickness, at a constant heat flux of 400 W/cm^2 .

[0042] Figure 7. Temperature distribution for (A) a macro-size LED (i.e. $1 \times 1 \text{ mm}^2$), and (B) an array of 100 μ -LEDs (i.e. $100 \times 100 \mu\text{m}^2$) at a spacing of 2 mm. (C) μ -LEDs surface temperature versus spacing for an array of 100 μ -LEDs.

[0043] Figure 8. Schematic illustration of epitaxial stack of InGaN MQW LED on Si (111) wafer.

[0044] Figure 9. Schematic overview of a fabrication process for making an electronic device embodiment.

[0045] Figure 10. Ohmic contact characteristics of Ni (10 nm) / Au (10 nm) to p-GaN. (a) Current-voltage characteristics of Ni/Au contact to p-GaN with TLM pad

spacing of 21 μm in three different annealing conditions (i.e. As deposited, 5 mins, 10 mins, and 15 mins annealing). (b) Plot of total resistance at four different pad spacing of 2.5 μm , 7.25 μm , 12 μm , and 17 μm .

[0046] Figure 11. Scanning electron microscopy (SEM) images of μ -ILEDs on (a) donor substrate after KOH undercut process, (b) donor substrate after transfer-printing process, and (c) receiving substrate (i.e. glass) after the transfer-printing process. μ -ILEDs are transfer-printed onto a glass substrate with varying pitches ranging from 25 μm to 500 μm .

[0047] Figure 12. (a) Schematic illustration of Back-Side Exposure (BSE) process for self-aligned passivation and via formation. Scanning electron microscopy (SEM) image of a 100 x 100 μm^2 printed μ -ILED (b) before, and (c) after BSE process. (d) SEM image of 25 x 25 μm^2 μ -ILED after BSE process (colorized for easy of viewing). (E) Cross-sectional profile of μ -ILEDs after BSE process.

[0048] Figure 13. (a) Forward voltage at 10 mA of current and corresponding current-voltage characteristics (inset) for representative μ -ILEDs printed on a PET substrate measured for varying bending radii. (b) Forward voltage at 10 mA of current and corresponding current-voltage characteristics (inset) for representative μ -ILEDs printed on a PET substrate measured for repetitive cycles.

[0049] Figure 14. (a) Current-voltage (I-V) characteristics of 100 μ -ILEDs from an array. (b) Optical image of an array consisting of 100 μ -ILEDs.

[0050] Figure 15. (a) Optical microscopy images of relief features filled with a PDMS/phosphor slurry (left column) and filled with the phosphor powder only (right column). (b) Emission spectra of white μ -ILEDs with phosphor layer thickness of 60 μm , 80 μm , and 105 μm .

[0051] Figure 16. Reported thermal conductivities of a thin-film Al from several references.

[0052] Figure 17. (a) A plot from analytical results on the surface temperature as a function of LED size up to 1 x 1 mm^2 . Inset provides comparison between

analytical solution and FEM simulations on the surface temperature as a function of LED size ranging from $10 \times 10 \mu\text{m}^2$ up to $100 \times 100 \mu\text{m}^2$.

[0053] Figure 18. Schematic illustrations and images corresponding to steps for forming, integrating and interconnecting ultrathin ($\sim 6 \mu\text{m}$), microscale inorganic light emitting diodes (μ -ILEDs) based on GaN materials grown epitaxially on sapphire substrates. (A) Arrays of μ -ILEDs ($100 \times 100 \mu\text{m}^2$ separated by $20 \mu\text{m}$; left: schematic; right: optical micrograph) are first defined, completely, on the sapphire substrate, including L-shaped current spreading p-contacts (Ni:15 nm/Au:15 nm) and square ($25 \times 25 \mu\text{m}^2$) n- and p- contact pads (Cr: 15 nm/Au:300 nm). (B) Bonding to a silicon wafer using an In-Pd alloy, followed by laser liftoff and removal of the sapphire substrate yields arrays of μ -ILEDs on Si (dark blue). The top sides of the devices (left: schematic; right: optical micrograph), coated with Ga (gray) from the LLO process, can be cleaned by etching with HCl. This etchant also removes unalloyed In, to leave only In-Pd alloy. (C) Schematic illustration (left), optical micrograph (right) and colorized, tilted view scanning electron microscope (SEM) image (right inset) after these etching processes. Only isolated agglomerates of In-Pd (black dots in the optical micrograph and schematic; pink structures in the SEM) remain. (D) Arrays of μ -ILEDs after transfer to the structured surface of a slab of PDMS (arrays of pillars diameters, heights and spacings of $3 \mu\text{m}$, $1.4 \mu\text{m}$ and $5 \mu\text{m}$, respectively) and complete removal of residual metal by etchants for Cr and Pd (left: schematic; right: optical micrograph). A layer of SiN_x protects the μ -LED metallization from these etchants. The inset on the right shows an individual device. (E) Arrays of μ -ILEDs (12 devices) on a $4 \times 15 \text{ mm}^2$ strip of PET, tied into a knot to illustrate its deformability (left) and on glass (100 devices; right).

[0054] Figure 19. Electrical (A and B) and optical properties (C-F) of representative μ -ILEDs ($100 \times 100 \mu\text{m}^2$) on a sapphire substrate, and on PET. (A) Current-voltage (I-V) characteristics. (B) Histogram of forward voltage at 10 mA current, measured on 25 μ -ILEDs on sapphire and on PET, respectively. (C) Images of single μ -ILED on PET (left; at 3mA) and sapphire (right; at 3mA). (D) Spectral properties of the emission from the devices shown in (C). (E) Light output-current and -voltage (LIV) measurements for a μ -ILED on PET. (F) Radiant flux and radiant

efficiency (energy conversion efficiency) as functions of applied current, for a μ -ILED on PET.

[0055] Figure 20. Size scaling effects in the operation of μ -ILEDs on 50 μm thick PET substrate. (A) Optical micrographs of μ -ILEDs with lateral dimensions from $1 \times 1 \text{ mm}^2$, $500 \times 500 \text{ }\mu\text{m}^2$, $300 \times 300 \text{ }\mu\text{m}^2$, $150 \times 150 \text{ }\mu\text{m}^2$, $100 \times 100 \text{ }\mu\text{m}^2$, $75 \times 75 \text{ }\mu\text{m}^2$, $50 \times 50 \text{ }\mu\text{m}^2$, to $25 \times 25 \text{ }\mu\text{m}^2$. (B) Micrographs of emission from a representative $1 \times 1 \text{ mm}^2$ device, showing uniform output at three current densities: 5, 10, to $30 \text{ }\mu\text{A/mm}^2$. (C) Measured (black symbols) and simulated (black line) maximum temperature as a function of μ -ILED size (lateral dimension), at 160 mW/mm^2 (For example, 40 mW at $500 \times 500 \text{ }\mu\text{m}^2$ μ -ILED and 160 mW at $1000 \times 1000 \text{ }\mu\text{m}^2$ μ -ILED) Red symbols show radiant efficiencies. (D) Output (optical) power density as a function of input (electrical) power density, for μ -ILEDs with different sizes.

[0056] Figure 21. Thermal management by control of size and spatial distributions of μ -ILEDs on PET. Optical images and emission profiles of a single device with size $500 \times 500 \text{ }\mu\text{m}^2$ and an equivalent active area consisting of a 5×5 array of devices with sizes of $100 \times 100 \text{ }\mu\text{m}^2$. (B) Measured (red symbols) and calculated (line – analytical model; black squares – FEM) temperature distribution along a dimension in the plane of a μ -ILED ($500 \times 500 \text{ }\mu\text{m}^2$) on PET, perpendicular to an edge and running through its center, for an applied power of 40 mW . (C) Measured (red symbols) and calculated (line – analytical model) maximum temperature of regular, square arrays (5×5) of μ -ILEDs ($100 \times 100 \text{ }\mu\text{m}^2$), with spacings of 0, 100, 200, 400 and $1000 \text{ }\mu\text{m}$. (D) Total light output power as a function of electrical input power, for a single μ -ILED with size $500 \times 500 \text{ }\mu\text{m}^2$ and for a regular, square array of $100 \times 100 \text{ }\mu\text{m}^2$ μ -ILEDs (5×5), corresponding to the case shown in (A).

[0057] Figure 22. Thermal behaviors of μ -ILEDs on unusual substrate materials. (A) Measured (left) and calculated (right) temperature distributions for isolated μ -ILEDs ($100 \times 100 \text{ }\mu\text{m}^2$). $700 \text{ }\mu\text{m}$ thick Al foil at an input power of 40 mW . (B) Results similar to those in (A), for the case of a hydrogel substrate and power of 5 mW . (C) Temperature for a similar μ -ILED on hydrogel with 100 (constant power), 70, 50, 30,

10 and 1 (D) % duty ratio cycle pulse (30 mW input power with 1 mS period). The peak temperature decreased from 232 °C (at constant power) to 30.3 °C (at 1 % pulsed duty cycle), as duty cycle decreases. (E) Calculated time dependence of the peak temperature, near the switching point (red arrow).

[0058] Figure 23. Illustration of full process.

[0059] Figure 24. LLO results with GaN material delineated at various lateral dimensions (left: 2X2mm², right: 5X5 mm²) (25 μm wide trench).

[0060] Figure 25. Image of a Si wafer removal of LEDs. Residual In-Pd particles remain.

[0061] Figure 26. Array of LEDs on a patterned PDMS slab (before transfer printing (left) and after (right)).

[0062] Figure 27. Via holes formed by backside exposure of a BCB coating.

[0063] Figure 28. LED arrays on 50 μm thick PET a) 28 LEDs (2 by 14), b) 46 LEDs (2 by 23) and c) 12 LEDs on 5X40 mm² strip shape PET.

[0064] Figure 29. Wavelength shift with various applied current.

[0065] Figure 30. Wavelength redshift by external heating (on hot plate) with low input current (power), 0.05 mA (0.14 mW).

[0066] Figure 31. Schematic illustration of the device geometry and parameters used in analytical model for heat.

[0067] Figure 32. Surface temperature of a 500X500 μm² LED. (20, 40 mW input power).

[0068] Figure 33. Surface temperature of an array of LEDs with 100 μm spacing, in a 5X5 square arrangement with individual device dimensions of 100X100 μm². 20, 40 mW applied power.

[0069] Figure 34. Surface temperature of an array of LEDs with 200 μm spacing, in a 5X5 square arrangement with individual device dimensions of 100X100 μm^2 . 20, 40 mW applied power.

[0070] Figure 35. Surface temperature of an array of LEDs with 400 μm spacing, in a 5X5 square arrangement with individual device dimensions of 100X100 μm^2 . 20, 40 mW applied power.

[0071] Figure 36. Surface temperature of an array of LEDs with 1000 μm spacing, in a 5X5 square arrangement with individual device dimensions of 100X100 μm^2 . 20, 40 mW applied power.

[0072] Figure 37. Thermal decay length at various PET thicknesses.

[0073] Figure 38. Schematic illustration of a μ -ILED on 700 μm thick Al foil and optical image.

[0074] Figure 39. Schematic illustration of a μ -ILED on 2 mm thick hydrogel and optical image.

[0075] Figure 40. LED on hydrogel at non-pulsed (100% duty cycle) 30 mW input power.

[0076] Figure 41. LED on hydrogel at pulsed (50% duty cycle) 30 mW input power (1 ms period).

[0077] Figure 42. Temperature change of LED on hydrogel at pulsed (1% duty cycle) 30 mW input power (1 ms period).

[0078] Figure 43. Temperature comparison between averaged pulsed input power and constant input power.

DETAILED DESCRIPTION

[0079] In general the terms and phrases used herein have their art-recognized meaning, which can be found by reference to standard texts, journal references and contexts known to those skilled in the art. The following definitions are provided to clarify their specific use in the context of the invention.

[0080] “Transferable” or “printable” are used interchangeably and relate to materials, structures, device components and/or integrated functional devices that are capable of transfer, assembly, patterning, organizing and/or integrating onto or into substrates. In an embodiment, transferring or printing refers to the direct transfer of a structure or element from one substrate to another substrate, such as from a host substrate (e.g. epitaxial growth substrate) to a device substrate or a device or component supported by a device substrate. Alternatively, printable refers to a structure or element that is printed via an intermediate substrate, such as an elastomeric stamp that lifts-off the structure or element and then subsequently transfers the structure or element to a device substrate or a component that is on a device substrate. In an embodiment, printable refers to a structure that is transferrable via transfer printing, such as dry contact transfer printing using an elastomeric stamp, such as a stamp comprising a high Young’s modulus polymer layer or a stamp comprising a low Young’s modulus polymer layer or a stamp comprising a combination of a high Young’s modulus polymer layer and a low Young’s modulus polymer layer. In an embodiment, the printing occurs without exposure of the substrate to high temperatures (i.e. at temperatures less than or equal to about 400 degrees Celsius). In one embodiment, printable or transferable materials, elements, device components and devices are capable of transfer, assembly, patterning, organizing and/or integrating onto or into substrates via solution printing or dry transfer contact printing. Similarly, “printing” is used broadly to refer to the transfer, assembly, patterning, organizing and/or integrating onto or into substrates, such as a substrate that functions as a stamp or a substrate that is itself a target (e.g., device) substrate.

[0081] “Substrate” refers to a material having a surface that is capable of supporting a component, including a device, or an interconnect. An interconnect that is “bonded” to the substrate refers to a portion of the interconnect in physical contact with the substrate and unable to substantially move relative to the substrate surface to which it is bonded. Unbonded portions, in contrast, are capable of substantial movement relative to the substrate. The unbonded portion of an interconnect generally corresponds to that portion having a “bent configuration,” such as by strain-induced interconnect bending.

[0082] “Host substrate” and “handle substrate” interchangeably refer to a substrate on which an electronic device is assembled, processed or otherwise manipulated. In certain embodiments, a handle substrate is a substrate useful as a transitory substrate, for example for holding structures for subsequent transfer to another substrate, such as by transfer printing. In some embodiments, a handle substrate is useful as a processing substrate, where structures present on the handle substrate undergo additional processing steps. In an embodiment, the host substrate is a “growth substrate”, which refers to a substrate useful for growing material, for example via epitaxial growth. In some embodiments, a growth substrate comprises the same material as is being grown. In some embodiments a growth substrate comprises material different from that being grown, optionally having one or more external layers to promote growth, such as epitaxial growth. Useful growth substrates include substrates which are lattice matched, or effectively lattice matched, to the material being grown. In some embodiments a growth substrate is a host substrate. “Device substrate” refers to a substrate useful for assembling device components. In some embodiments, a device substrate comprises functional device components. In some embodiments, a device substrate is a flexible substrate, a large area substrate, a pre-metalized substrate, a substrate pre-patterned with one or more device components, or any combination of these. In some embodiments a device substrate is a host substrate.

[0083] The term “surface” as used herein is intended to be consistent with its plain meaning which refers to an outer boundary of an object. In embodiments, surfaces may be given specific names, such as “receiving surface”, “contact surface”, “external surface”. In some embodiments, named surfaces can refer to their target use and/or identify subregions of a surface. In some embodiments, named surfaces can refer to their orientation, for example relative to other nearby or adjacent components.

[0084] “Functional layer” or “device layer” refers to a layer capable of incorporation into a device or device component and that provides at least partial functionality to that device or device component. Depending on the particular device or device component, a functional layer can include a broad range of compositions. For example, a device that is an LED can be made from a starting functional layer of

semiconductor material, including a functional layer that is itself made up of a plurality of distinct layers as provided herein. In certain embodiments, release and subsequent printing of such layers provides the basis for constructing an LED device or device component. In contrast, a functional layer for incorporation into electronics (MESFETs), solar cells, or optical systems may have a different layering configuration and/or compositions. Accordingly, the specific functional layer incorporated into the multilayer structure depends on the final device or device component in which the functional layer will be incorporated.

[0085] “Release layer” (sometimes referred to as “sacrificial layer”) refers to a layer that at least partially separates one or more layers. A release layer is capable of being removed or providing other means for facilitating separation of the functional layer from other layers of a multi-layer structure, such as by a release layer that physically separates in response to a physical, thermal, chemical and/or electromagnetic stimulation, for example. Accordingly, the actual release layer composition is selected to best match the means by which separation will be provided. Separation is by any one or more separating means known in the art, such as by interface failure or by release layer sacrifice. A release layer may itself remain connected to a functional layer, such as a functional layer that remains attached to the remaining portion of the multilayer structure, or a functional layer that is separated from the remaining portion of the multilayer structure. The release layer is optionally subsequently separated and/or removed from the functional layer.

[0086] “Structural layer” refers to a layer that imparts structural functionality, for example by supporting and/or encapsulating device components. Specific examples of structural layers include spacing layers and encapsulating layers.

[0087] “Buffer layer” refers to a layer of a device or device component which is useful for protecting other layers of the device component. In one embodiment, a buffer layer protects another device layer from etching. In an embodiment, a buffer layer does not impact or has a minimal impact on the function of the device. In one embodiment, an etch block layer is a buffer layer.

[0088] “Release” and “releasing” refer to at least partially separating two layers, devices or device components from one another, for example by mechanical or

physical separation, or by removal of at least a portion of one layer, device or device component. In some embodiments, removal of a sacrificial layer results in the release of a layer, device or device component. In some embodiments, layers, devices or device components are released by etching away a portion of the layer, device or device component and/or by etching away a portion of an underlying layer or substrate. In some embodiments, layers, devices or device components are released by exposure to electromagnetic radiation. In certain embodiments, released components remain attached to the object which they are released from by one or more anchors. In some embodiments, released components are subsequently attached to the object they are released from by one or more anchors.

[0089] “Etch” and “etching” refer to a process by which a portion of a layer, device or device component is reacted away, dissolved or otherwise removed. In embodiments, an anisotropic etch or a directional etch refers to an etching process which preferentially removes material along a specific direction. In embodiments, a wet etch refers to removal of material by exposure to a solution, such as a hot (e.g., $T > 298\text{ K}$) KOH solution. In embodiments, a selective etch refers to removal of a specific material or class of materials. In embodiments, a reactive ion etch or an inductively coupled plasma reactive ion etch refers to an etching method which utilizes a plasma to etch away material, for example by reaction with ions in the plasma. The term “etchant” is used in the present description to broadly refer to a substance which is useful for removal of material by etching. The term “electrochemical etching” refers to an etching process which utilizes an applied electric potential, electric field or electric current. The term “photoelectrochemical etching” refers to an etching process which utilizes an applied electric potential, electric field or electric current and exposure to electromagnetic radiation.

[0090] An “etch mask” refers to material useful for preventing underlying material from being etched. In some embodiments, a thick etch mask refers to an etch mask of a sufficient thickness that the majority of the mask remains after an etching process. In embodiments a thick etch mask has a thickness selected over the range of 100 nm to 5 μm . In some embodiments a metal etch mask refers to an etch block layer.

[0091] The term “mask” refers to a material which covers or otherwise blocks portions of an underlying material. Use of the term “mask” is intended to be consistent with use of the term in the art of microfabrication. In embodiments, the term “mask” refers to an etch mask, an optical mask, a deposition mask or any combination of these.

[0092] The terms “masked region” and “exposed region” respectively refer to portions of an underlying material which are blocked and unblocked by a mask. The term “exposed region” may also refer to a portion of a substrate, device or device component which is not encapsulated by an encapsulant.

[0093] “Epitaxial regrowth” and “epitaxial growth” refer to methods of growing a crystalline layer by deposition of material, for example gas or liquid phase deposition. The term “epilayer” refers to a layer grown via epitaxial growth.

[0094] The term “patterning” is used herein as in the art of microfabrication to broadly refer to a process by which portions of a layer, device or device component are selectively removed or deposited to create a specified structure.

[0095] “Supported by a substrate” refers to a structure that is present at least partially on a substrate surface or present at least partially on one or more intermediate structures positioned between the structure and the substrate surface. The term “supported by a substrate” may also refer to structures partially or fully embedded in a substrate.

[0096] “Printable electronic device” or “printable electronic device component” refer to devices and structures that are configured for assembly and/or integration onto substrate surfaces, for example by using dry transfer contact printing and/or solution printing methods. In embodiments, a printable electronic device component is a printable semiconductor element. In embodiments, printable semiconductor elements are unitary single crystalline, polycrystalline or microcrystalline inorganic semiconductor structures. In preferred embodiments, printable semiconductor elements are printable single crystalline LED structures, for example, generated via epitaxial growth and/or doping techniques. In various embodiments, printable semiconductor elements are connected to a substrate, such as a mother wafer, via one or more bridge or anchor elements. In this context of this description, a unitary

structure is a monolithic element having features that are mechanically connected. Semiconductor elements of various embodiments may be undoped or doped, may have a selected spatial distribution of dopants and may be doped with a plurality of different dopant materials, including p- and n-type dopants. Certain microstructured printable semiconductor elements include those having at least one cross sectional dimension greater than or equal to about 1 micron and certain nanostructured printable semiconductor elements include those having at least one cross sectional dimension less than or equal to about 1 micron.

[0097] Printable semiconductor elements useful for a variety of applications comprise elements derived from “top down” processing of high purity bulk materials, such as high purity crystalline semiconductor wafers generated using conventional high temperature processing techniques, including epitaxial growth. In an embodiment, a printable semiconductor element comprises a composite heterogeneous structure having a semiconductor operationally connected to or otherwise integrated with at least one additional device component or structure, such as a conducting layer, dielectric layer, electrode, additional semiconductor structure or any combination of these. In some methods and systems, the printable semiconductor element(s) comprises a semiconductor structure integrated with at least one additional structure selected from the group consisting of: another semiconductor structure; a dielectric structure; a conductive structure, and an optical structure (e.g., optical coatings, reflectors, windows, optical filters, collecting, diffusing or concentration optics, etc.). In some embodiments a printable semiconductor element comprises a semiconductor structure integrated with at least one electronic device component selected from the group consisting of: an electrode, a dielectric layer, an optical coating, a metal contact pad, and a semiconductor channel. In some embodiments, printable semiconductor elements comprise stretchable semiconductor elements, bendable semiconductor elements and/or heterogeneous semiconductor elements (e.g., semiconductor structures integrated with one or more additional materials such as dielectrics, other semiconductors, conductors, ceramics, etc.). Printable semiconductor elements include printable semiconductor devices and components thereof, including but not limited to printable LEDs, lasers, solar cells, p-n junctions, photovoltaics, photodiodes, diodes, transistors, integrated circuits, and sensors.

[0098] A “component” is used broadly to refer to a material or individual component used in a device. An “interconnect” is one example of a component and refers to an electrically conducting material capable of establishing an electrical connection with a component or between components. In particular, an interconnect may establish electrical contact between components that are separate and/or moveable with respect to each other. Depending on the desired device specifications, operation, and application, an interconnect is made from a suitable material. For applications where a high conductivity is required, typical interconnect metals may be used, including but not limited to copper, silver, gold, aluminum and the like, and alloys. Suitable conductive materials further include semiconductors, such as silicon and GaAs and other conducting materials such as indium tin oxide.

[0099] Other components include, but are not limited to, thin film transistors (TFTs), transistors, electrodes, integrated circuits, circuit elements, control elements, microprocessors, transducers, islands, bridges and combinations thereof. Components may be connected to one or more contact pads as known in the art, such as by metal evaporation, wire bonding, and application of solids or conductive pastes, for example.

[00100] An interconnect that is “stretchable” or “flexible” is used herein to broadly refer to an interconnect capable of undergoing a variety of forces and strains such as stretching, bending and/or compression in one or more directions without substantially adversely impacting electrical connection to, or electrical conduction from, a device component. Accordingly, a stretchable interconnect may be formed of a relatively brittle material, such as GaAs, yet remain capable of continued function even when exposed to a significant deformatory force (e.g., stretching, bending, compression) due to the interconnect’s geometrical configuration. In an exemplary embodiment, a stretchable interconnect may undergo strain larger than about 1%, 10% or 30% or up to about 100% without fracturing. In an example, the strain is generated by stretching an underlying elastomeric substrate to which at least a portion of the interconnect is bonded. For certain embodiments, flexible or stretchable interconnects include interconnects having wavy, meandering or serpentine shapes.

[00101] A “device component” is used to broadly refer to an individual component within an electrical, optical, mechanical or thermal device. Components include, but are not limited to, a photodiode, LED, TFT, electrode, semiconductor, other light-collecting/detecting component, transistor, integrated circuit, contact pad capable of receiving a device component, thin film device, circuit element, control element, microprocessor, transducer and combinations thereof. A device component can be connected to one or more contact pads as known in the art, such as by metal evaporation, wire bonding, application of solids or conductive pastes, for example.

[00102] “Electrical device” generally refers to a device incorporating a plurality of device components, and includes large area electronics, printed wire boards, integrated circuits, device components, arrays, biological and/or chemical sensors, physical sensors (e.g., temperature, light, radiation, etc.), solar cell or photovoltaic arrays, display arrays, optical collectors, systems and displays.

[00103] “Electronic device component” refers to a printable semiconductor or part of an electrical device. Exemplary electronic device component embodiments are configured for performing a function, for example emitting electromagnetic radiation or converting electromagnetic radiation into electrical energy. In specific embodiments, multiple electronic device components are electrically interconnected and perform a more complex task or function than the individual device components perform alone. Useful electronic device components include, but are not limited to P-N junctions, thin film transistors, single junction solar cells, multi-junction solar cells, photodiodes, light emitting diodes, lasers, CMOS devices, MOSFET devices, MESFET devices, photovoltaic cells, microelectromechanical devices, nanoelectromechanical devices and HEMT devices.

[00104] “Active circuit” and “active circuitry” refer to one or more device components configured for performing a specific function. Useful active circuits include, but are not limited to, amplifier circuits, multiplexing circuits, integrated circuits and current limiting circuits. Useful active circuit elements include, but are not limited to, transistor elements and diode elements.

[00105] “Sensing element” and “sensor” are used synonymously and refer to a device component useful as a sensor and/or useful for detecting the presence,

absence, amount, magnitude or intensity of a physical property, object, radiation and/or chemical.

[00106] “Sensing” refers to detecting the presence, absence, amount, magnitude or intensity of a physical and/or chemical property. Useful electronic device components for sensing include, but are not limited to electrode elements, chemical or biological sensor elements, pH sensors, optical sensors, temperature sensors, photodiodes, photovoltaic elements, strain sensors, acceleration sensors, movement sensors, displacement sensors, pressure sensors, acoustic sensors and capacitive sensors.

[00107] “Actuating element” and “actuator” are used synonymously and refer to a device component useful for interacting with, stimulating, controlling, or otherwise affecting another structure, material or fluid. In some embodiments, actuating elements are used for interacting with, modifying a property of or otherwise affecting a device component, for example a component adjacent to a heating or actuating element.

[00108] “Actuating” refers to stimulating, controlling, or otherwise affecting an external structure, material or fluid. Useful electronic device components for actuating include, but are not limited to, electrode elements, electromagnetic radiation emitting elements, light emitting diodes, lasers, and heating elements.

[00109] “Visualizing” refers to a method of observing or otherwise detecting electromagnetic radiation, for example with an eye or a photodetector.

[00110] “Device island” refers to a relatively rigid device element or component of an electronic device comprising one or more semiconductor elements or active semiconductor structures. “Bridge” or “bridge structure” refers to stretchable or flexible structures interconnecting two or more device islands or one device island to another device component. Specific bridge structures include flexible semiconductor interconnects.

[00111] “Vertical type LED” refers to a light emitting diode device in which the functional components or layers of the device are arranged in a stacked configuration and the electrical contacts are made at the top and bottom of the stack.

[00112] “ON/OFF state” refers to a configuration of a device component capable of and/or configured for generation of electromagnetic radiation, such as a light emitting diode or a laser. In one embodiment, an ON/OFF state distinguishes between moments when a device component is generating electromagnetic radiation and when a device component is not generating electromagnetic radiation. In an embodiment, an ON/OFF state distinguishes between moments when a device component is generating electromagnetic radiation having an intensity above a threshold value and when a device component is generating electromagnetic radiation having an intensity below a threshold value.

[00113] “Solution printing” is intended to refer to processes whereby one or more structures, such as transferable or printable elements, are dispersed into a carrier medium and delivered in a concerted manner to selected regions of a substrate surface. In an exemplary solution printing method, delivery of structures to selected regions of a substrate surface is achieved by methods that are independent of the morphology and/or physical characteristics of the substrate surface undergoing patterning. Solution printing methods include, but are not limited to, ink jet printing, thermal transfer printing, and capillary action printing.

[00114] “Contact printing” refers broadly to a dry transfer contact printing method such as with a stamp that facilitates transfer of structures, such as printable LEDs, from a stamp surface to a substrate surface. Alternatively, the transfer can be directly to a target (e.g., device) substrate or host substrate. In an embodiment, the stamp is an elastomeric stamp, such as a stamp comprising a high Young’s modulus polymer layer or a stamp comprising a low Young’s modulus polymer layer or a stamp comprising a combination of a high Young’s modulus polymer layer and a low Young’s modulus polymer layer. The following references relate to self-assembly techniques which may be used in methods described herein to transfer, assemble and interconnect transferable semiconductor elements via contact printing and/or solution printing techniques and are incorporated by reference in their entireties herein: (1) “Guided molecular self-assembly: a review of recent efforts”, Jiyun C Huie Smart Mater. Struct. (2003) 12, 264-271; (2) “Large-Scale Hierarchical Organization of Nanowire Arrays for Integrated Nanosystems”, Whang, D.; Jin, S.; Wu, Y.; Lieber, C. M. Nano Lett. (2003) 3(9), 1255-1259; (3) “Directed Assembly of One-

Dimensional Nanostructures into Functional Networks”, Yu Huang, Xiangfeng Duan, Qingqiao Wei, and Charles M. Lieber, Science (2001) 291, 630-633; and (4) “Electric-field assisted assembly and alignment of metallic nanowires”, Peter A. Smith et al., Appl. Phys. Lett. (2000) 77(9), 1399-1401.

[00115] Useful contact printing methods for assembling, organizing and/or integrating transferable elements include dry transfer contact printing, microcontact or nanocontact printing, microtransfer or nanotransfer printing and self assembly assisted printing. Use of contact printing is beneficial because it allows assembly and integration of a plurality of transferable semiconductors in selected orientations and positions relative to each other. Contact printing also enables effective transfer, assembly and integration of diverse classes of materials and structures, including semiconductors (e.g., inorganic semiconductors, single crystalline semiconductors, organic semiconductors, carbon nanomaterials etc.), dielectrics, and conductors. Contact printing methods optionally provide high precision registered transfer and assembly of transferable semiconductor elements in preselected positions and spatial orientations relative to one or more device components prepatterned on a device substrate. Contact printing is also compatible with a wide range of substrate types, including conventional rigid or semi-rigid substrates such as glasses, ceramics and metals, and substrates having physical and mechanical properties attractive for specific applications, such as flexible substrates, bendable substrates, shapeable substrates, conformable substrates and/or stretchable substrates. Contact printing assembly of transferable structures is compatible, for example, with low temperature processing (e.g., less than or equal to 298K). This attribute allows the present optical systems to be implemented using a range of substrate materials including those that decompose or degrade at high temperatures, such as polymer and plastic substrates. Contact printing transfer, assembly and integration of device elements is also beneficial because it can be implemented via low cost and high-throughput printing techniques and systems, such as roll-to-roll printing and flexographic printing methods and systems.

[00116] “Stretchable” refers to the ability of a material, structure, device or device component to be strained without undergoing fracture. In an exemplary embodiment, a stretchable material, structure, device or device component may

undergo strain larger than about 0.5% without fracturing, preferably for some applications strain larger than about 1% without fracturing and more preferably for some applications strain larger than about 3% without fracturing.

[00117] The terms “foldable,” “flexible” and “bendable” are used synonymously in the present description and refer to the ability of a material, structure, device or device component to be deformed into a curved shape without undergoing a transformation that introduces significant strain, such as strain characterizing the failure point of a material, structure, device or device component. In an exemplary embodiment, a flexible material, structure, device or device component may be deformed into a curved shape without introducing strain larger than or equal to about 5%, preferably for some applications without introducing strain larger than or equal to about 1%, and more preferably for some applications without introducing strain larger than or equal to about 0.5%. As used herein, some, but not necessarily all, flexible structures are also stretchable. A variety of properties provide flexible structures (e.g., device components), including materials properties such as a low modulus, bending stiffness and flexural rigidity; physical dimensions such as small average thickness (e.g., less than 100 μm , optionally less than 10 μm and optionally less than 1 μm) and device geometries such as thin film and mesh geometries.

[00118] “Semiconductor” refers to any material that is an insulator at very low temperatures, but which has an appreciable electrical conductivity at temperatures of about 300 Kelvin. In the present description, use of the term semiconductor is intended to be consistent with use of this term in the art of microelectronics and electrical devices. Useful semiconductors include element semiconductors, such as silicon, germanium and diamond, and compound semiconductors, such as group IV compound semiconductors such as SiC and SiGe, group III-V semiconductors such as AlSb, AlAs, AlIn, AlP, BN, GaSb, GaAs, GaN, GaP, InSb, InAs, InN, and InP, group III-V ternary semiconductor alloys such as $\text{Al}_x\text{Ga}_{1-x}\text{As}$, group II-VI semiconductors such as CsSe, CdS, CdTe, ZnO, ZnSe, ZnS, and ZnTe, group I-VII semiconductors such as CuCl, group IV – VI semiconductors such as PbS, PbTe and SnS, layer semiconductors such as PbI_2 , MoS_2 and GaSe, and oxide semiconductors such as CuO and Cu_2O .

[00119] The term semiconductor includes intrinsic semiconductors and extrinsic semiconductors that are doped with one or more selected materials, including semiconductors having p-type doping materials (also known as P-type or p-doped semiconductors) and n-type doping materials (also known as N-type or n-doped semiconductors), to provide beneficial electrical properties useful for a given application or device. The term semiconductor includes composite materials comprising a mixture of semiconductors and/or dopants. Specific semiconductor materials useful for some embodiments include, but are not limited to, Si, Ge, Se, diamond, fullerenes, SiC, SiGe, SiO, SiO₂, SiN, AlSb, AlAs, AlIn, AlN, AlP, AIS, BN, BP, BAs, As₂S₃, GaSb, GaAs, GaN, GaP, GaSe, InSb, InAs, InN, InP, CsSe, CdS, CdSe, CdTe, Cd₃P₂, Cd₃As₂, Cd₃Sb₂, ZnO, ZnSe, ZnS, ZnTe, Zn₃P₂, Zn₃As₂, Zn₃Sb₂, ZnSiP₂, CuCl, PbS, PbSe, PbTe, FeO, FeS₂, NiO, EuO, EuS, PtSi, TlBr, CrBr₃, SnS, SnTe, PbI₂, MoS₂, GaSe, CuO, Cu₂O, HgS, HgSe, HgTe, HgI₂, MgS, MgSe, MgTe, CaS, CaSe, SrS, SrTe, BaS, BaSe, BaTe, SnO₂, TiO, TiO₂, Bi₂S₃, Bi₂O₃, Bi₂Te₃, BiI₃, UO₂, UO₃, AgGaS₂, PbMnTe, BaTiO₃, SrTiO₃, LiNbO₃, La₂CuO₄, La_{0.7}Ca_{0.3}MnO₃, CdZnTe, CdMnTe, CuInSe₂, copper indium gallium selenide (CIGS), HgCdTe, HgZnTe, HgZnSe, PbSnTe, Tl₂SnTe₅, Tl₂GeTe₅, AlGaAs, AlGaIn, AlGaP, AlInAs, AlInSb, AlInP, AlInAsP, AlGaAsN, GaAsP, GaAsN, GaMnAs, GaAsSbN, GaInAs, GaInP, AlGaAsSb, AlGaAsP, AlGaInP, GaInAsP, InGaAs, InGaP, InGaN, InAsSb, InGaSb, InMnAs, InGaAsP, InGaAsN, InAlAsN, GaInNAsSb, GaInAsSbP, and any combination of these. Porous silicon semiconductor materials are useful in the field of sensors and light emitting materials, such as light emitting diodes (LEDs) and solid state lasers. Impurities of semiconductor materials are atoms, elements, ions and/or molecules other than the semiconductor material(s) themselves or any dopants provided to the semiconductor material. Impurities are undesirable materials present in semiconductor materials which may negatively impact the electrical properties of semiconductor materials, and include but are not limited to oxygen, carbon, and metals including heavy metals. Heavy metal impurities include, but are not limited to, the group of elements between copper and lead on the periodic table, calcium, sodium, and all ions, compounds and/or complexes thereof.

[00120] "Semiconductor element", "semiconductor structure" and "semiconductor circuit element" are used synonymously in the present description and broadly refer to any semiconductor material, composition, structure, device or device component,

and expressly include high quality, single crystalline and polycrystalline semiconductors, semiconductor materials fabricated via high temperature processing, doped semiconductor materials, inorganic semiconductors and composite semiconductor materials and structures having one or more additional semiconductor components and/or non-semiconductor components, such as dielectric layers or materials and/or conducting layers or materials. In some embodiments, for example, semiconductor element refers to semiconductor-containing devices or components thereof, such as LEDs, lasers, solar cells, semiconductor junctions, p-n junctions, photovoltaics, photodiodes, diodes, transistors, integrated circuits, logic circuits, sensors, heaters, temperature sensors, thermistors and resistive heating elements. Semiconductor elements expressly include structures having an average thickness selected over the range of 50 nm to 100 μm , one or more lateral dimensions selected over the range of 250 nm to 100000 μm , and any combinations of these. Optionally, semiconductor elements are provided in physical contact with other dielectric or insulating materials and structures. Optionally, semiconductor elements are provided in physical contact or electrical communication with other metallic, doped or conducting materials and structures. Optionally, semiconductor structures are provided in physical contact or electrical communication with other semiconductor devices, including, but not limited to LEDs, lasers, transistors, integrated circuits, logic circuits, photodiodes, multiplexer circuitry and amplifier circuitry. Optionally, a plurality of semiconductor structures is provided in array configurations, including arrays with a fixed element pitch or a variable element pitch. Semiconductor structures may optionally be provided in a plurality of individually encapsulated stacked layers, including stacked layers of array structures. Semiconductor elements utilized in the devices and methods described herein include high purity semiconductor elements having oxygen impurities less than about 5 to 25 parts per million atoms, carbon impurities less than about 1 to 5 parts per million atoms, and heavy metal impurities less than or equal to about 1 part per million atoms (ppma), preferably less than or equal to about 100 parts per billion atoms (ppba) for some applications, and more preferably less than or equal to about 1 part per billion atoms (ppba) for some applications. Semiconductor elements having low levels of heavy metal impurities (e.g. less than about 1 part per million atoms) are beneficial for applications and devices requiring

good electronic performance, as the presence of heavy metals in semiconductor materials can severely degrade their electrical properties.

[00121] In certain embodiments, the term “orientation” refers to a specific plane of a crystal structure, for example a semiconductor crystal. In certain embodiments, the term “direction” refers to a specific axis, or equivalent axes, of a crystal structure. In embodiments, use of the terms orientation and direction with a specific numeric indicator is intended to be consistent with use in the fields of crystallography and microfabrication.

[00122] “Quantum well” refers to an active layer of a light emitting diode device. In one embodiment, a quantum well is a layer of an LED device having a relatively narrow bandgap, surrounded on two sides by layers each having a relatively wider bandgap. “Barrier layer” refers to a layer of a light emitting diode device which is positioned adjacent to a quantum well layer and has a larger bandgap than the quantum well material. In one embodiment, a quantum well layer is sandwiched between two barrier layers. In another embodiment, multiple quantum well layers are sandwiched between multiple barrier layers.

[00123] “Contact layer” refers to a layer of a light emitting diode device, for example used to make electrical contact with external circuit components, such as electrical interconnects. “Spreader layer” refers to a layer of a light emitting diode device, for example useful for providing voltage or current from a contact layer across the area of a light emitting diode device. “Cladding layer” refers to a layer of a light emitting diode device, for example a layer surrounding the barrier layer and quantum well layer.

[00124] “Good electronic performance” and “high performance” are used synonymously in the present description and refer to devices and device components having electronic characteristics, such as field effect mobilities, threshold voltages and on – off ratios, providing a desired functionality, such as electronic signal switching and/or amplification. Exemplary printable elements exhibiting good electronic performance may have intrinsic field effect mobilities greater than or equal about $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and for some applications, greater than or equal to about $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Exemplary transistors exhibiting good electronic

performance may have device field effect mobilities great than or equal to about $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, for some applications, greater than or equal to about $300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, and for other applications, greater than or equal to about $800 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Exemplary transistors exhibiting good electronic performance may have threshold voltages less than about 5 volts and/or on – off ratios greater than about 1×10^4 .

[00125] “Plastic” refers to any synthetic or naturally occurring material or combination of materials that can be molded or shaped, generally when heated, and hardened into a desired shape. Useful plastics include, but are not limited to, polymers, resins and cellulose derivatives. In the present description, the term plastic is intended to include composite plastic materials comprising one or more plastics with one or more additives, such as structural enhancers, fillers, fibers, plasticizers, stabilizers or additives which may provide desired chemical or physical properties.

[00126] “Prepolymer” refers to a material which is a polymer precursor and/or a material which, when cured, is a polymer. A “liquid prepolymer” refers to a prepolymer which exhibits one or more properties of a liquid, for example flow properties. Specific prepolymers include, but are not limited to, photocurable polymers, thermally curable polymers and photocurable polyurethanes. Use of the term “developed” in reference to a prepolymer material refers to prepolymer materials that have been cured or partially cured. For example, in one embodiment, a developed prepolymer refers to a prepolymer that has been exposed to electromagnetic radiation, initiating the curing process. Use of the term “undeveloped” in reference to a prepolymer material refers to prepolymer materials that have not undergone curing. For example, in one embodiment, an undeveloped prepolymer refers to a prepolymer that has not been exposed to electromagnetic radiation and, thus, has not begun the curing process. In one embodiment, the term undeveloped is used to specifically distinguish an uncured portion of a single prepolymer region that is adjacent to other portions of the same prepolymer region that are cured or have begun the curing process.

[00127] “Curing” refers to a process by which a material is transformed such that the transformed material exhibits one or more properties different from the original, non-transformed material. In some embodiments, a curing process allows a liquid

material to become solid or rigid. In an embodiment, curing transforms a prepolymer material into a polymer material. Useful curing processes include, but are not limited to, exposure to electromagnetic radiation (photocuring processes), for example exposure to electromagnetic radiation of a specific wavelength or wavelength range (e.g., ultraviolet or infrared electromagnetic radiation); thermal curing processes, for example heating to a specific temperature or within a specific temperature range (e.g., 150 °C or between 125 and 175 °C); temporal curing processes, for example waiting for a specified time or time duration (e.g., 5 minutes or between 10 and 20 hours); drying processes, for example removal of all or a percentage of water or other solvent molecules; and any combination of these.

[00128] “Polymer” refers to a molecule comprising a plurality of repeating chemical groups, typically referred to as monomers. Polymers are often characterized by high molecular masses. Polymers are typically composed of repeating structural units connected by covalent chemical bonds or the polymerization product of one or more monomers. The term polymer includes homopolymers, or polymers consisting essentially of a single repeating monomer subunit. The term polymer also includes copolymers, or polymers consisting essentially of two or more monomer subunits, such as random, block, alternating, segmented, graft, tapered and other copolymers. Useful polymers include organic polymers and inorganic polymers, both of which may be in amorphous, semi-amorphous, crystalline or partially crystalline states. Polymers may comprise monomers having the same chemical composition or may comprise a plurality of monomers having different chemical compositions, such as a copolymer. Cross linked polymers having linked monomer chains are also useful for some embodiments. Useful polymers include, but are not limited to, plastics, elastomers, thermoplastic elastomers, elastoplastics, thermoplastics and acrylates. Exemplary polymers include, but are not limited to, acetal polymers, biodegradable polymers, cellulosic polymers, fluoropolymers, nylons, polyacrylonitrile polymers, polyamide-imide polymers, polyimides, polyarylates, polybenzimidazole, polybutylene, polycarbonate, polyesters, polyetherimide, polyethylene, polyethylene copolymers and modified polyethylenes, polyketones, poly(methyl methacrylate), polymethylpentene, polyphenylene oxides and polyphenylene sulfides, polyphthalamide, polypropylene, polyurethanes, styrenic resins, sulfone based resins, vinyl-based resins, rubber (including natural rubber, styrene-butadiene,

polybutadiene, neoprene, ethylene-propylene, butyl, nitrile, silicones), acrylic, polystyrene, polyvinyl chloride, polyolefin or any combinations of these.

[00129] “Elastomer” refers to a polymeric material which can be stretched or deformed and return to its original shape without substantial permanent deformation. Elastomers commonly undergo substantially elastic deformations. Useful elastomers may comprise polymers, copolymers, composite materials or mixtures of polymers and copolymers. An elastomeric layer refers to a layer comprising at least one elastomer. Elastomeric layers may also include dopants and other non-elastomeric materials. Useful elastomer embodiments include, but are not limited to, thermoplastic elastomers, styrenic materials, olefinic materials, polyolefin, polyurethane thermoplastic elastomers, polyamides, synthetic rubbers, PDMS, polybutadiene, polyisobutylene, poly(styrene-butadiene-styrene), polyurethanes, polychloroprene and silicones. In some embodiments, an elastomeric stamp comprises an elastomer. Exemplary elastomers include, but are not limited to silicon containing polymers such as polysiloxanes including poly(dimethyl siloxane) (i.e. PDMS and h-PDMS), poly(methyl siloxane), partially alkylated poly(methyl siloxane), poly(alkyl methyl siloxane) and poly(phenyl methyl siloxane), silicon modified elastomers, thermoplastic elastomers, styrenic materials, olefinic materials, polyolefin, polyurethane thermoplastic elastomers, polyamides, synthetic rubbers, polyisobutylene, poly(styrene-butadiene-styrene), polyurethanes, polychloroprene and silicones. In an embodiment, a flexible polymer is a flexible elastomer.

[00130] “Transfer device” or “transfer substrate” refers to a substrate, device or device component capable of and/or configured for receiving and/or relocating an element or array of elements, such as printable elements. Useful transfer devices include conformal transfer devices, such as devices having one or more contact surfaces capable of establishing conformal contact with elements undergoing transfer. An elastomeric stamp and/or transfer device is useful with a variety of the methods and devices described herein. Useful elastomeric transfer devices include, but are not limited to, elastomeric stamps, composite elastomeric stamps, an elastomeric layer, a plurality of elastomeric layers and an elastomeric layer coupled to a substrate such as a glass, ceramic, metal or polymer substrate.

[00131] “Elastomeric stamp” and “elastomeric transfer device” are used interchangeably and refer to an elastomeric material having a surface that can receive as well as transfer a feature. Exemplary elastomeric transfer devices include stamps, molds and masks. The transfer device affects and/or facilitates feature transfer from a donor material to a receiver material. Stamps and transfer devices may be used for assembling components via transfer printing, such as dry contact transfer printing.

[00132] “Target substrate” is used broadly to refer to the desired final substrate that will support the transferred structure(s). In an embodiment, the target substrate is a device substrate. In an embodiment, the target substrate is a device component or element that is itself supported by a substrate.

[00133] “Large area” refers to an area, such as the area of a receiving surface of a substrate used for device fabrication, greater than or equal to about 36 square inches.

[00134] “Pre-metalized” refers to a structure which includes metallic layers, components or features.

[00135] “Pre-patterned” refers to a structure which includes one or more devices, components or relief features.

[00136] “Optical communication” refers to a configuration of two or more elements wherein one or more beams of electromagnetic radiation are capable of propagating from one element to the other element. Elements in optical communication may be in direct optical communication or indirect optical communication. “Direct optical communication” refers to a configuration of two or more elements wherein one or more beams of electromagnetic radiation propagate directly from a first device element to another without use of optical components for steering and/or combining the beams. “Indirect optical communication” refers to a configuration of two or more elements wherein one or more beams of electromagnetic radiation propagate between two elements via one or more device components including, but not limited to, wave guides, fiber optic elements, reflectors, filters, prisms, lenses, gratings and any combination of these device components.

[00137] “Luminous efficacy” and “luminous efficiency” refer to a relative measure of an amount of luminous flux generated by a device or device element that consumes a specific power.

[00138] The term “phosphor” as used herein refers to a luminescent material, for example a material that emits electromagnetic radiation by a non-incandescent mechanism. In one embodiment, a phosphor emits electromagnetic radiation of one wavelength or wavelength distribution when exposed to electromagnetic radiation of a second wavelength or wavelength distribution. The term phosphor expressly includes phosphorescent materials and fluorescent materials.

[00139] An “optical diffuser” refers to a device component used for scattering, spreading or otherwise redirecting electromagnetic radiation. In one embodiment, an optical diffuser is used to enlarge the apparent size of a source of electromagnetic radiation. In one embodiment, a diffuser is used to make multiple discrete sources of light appear as a single, continuous, larger area source of light.

[00140] The term “chromaticity” as used herein refers to an apparent color of electromagnetic radiation or a distribution of electromagnetic radiation. In some embodiments, chromaticity is defined according to a defined color space. In a specific embodiment, chromaticity is referred to according to coordinates of the CIE 1931 color space, for example x and y coordinates.

[00141] “Electrical contact” and “electrical communication” refer to the arrangement of one or more objects such that an electric current efficiently flows from one object to another. For example, in some embodiments, two objects having an electrical resistance between them less than 100 Ω are considered in electrical communication with one another. An electrical contact can also refer to a component of a device or object used for establishing electrical communication with external devices or circuits, for example an electrical interconnection. “Electrical contact” also refers to the ability of two or more materials and/or structures to transfer charge between them, such as in the form of the transfer of electrons or ions. “Electrical communication” also refers to a configuration of two or more components such that an electronic signal or charge carrier can be directly or indirectly transferred from one component to another. As used herein, electrical

communication includes one-way and two-way electrical communication. In some embodiments, components in electrical communication are in direct electrical communication wherein an electronic signal or charge carrier is directly transferred from one component to another. In some embodiments, components in electrical communication are in indirect electrical communication wherein an electronic signal or charge carrier is indirectly transferred from one component to another via one or more intermediate structures, such as circuit elements, separating the components.

[00142] “Electrical resistivity” refers to a property of a material characteristic of the resistance to flow of electrons through the material. In certain embodiments, the resistivity of a material (ρ) is related to the resistance (R) of a length of material (L) having a specific cross sectional area (A), e.g., $\rho = R \times A / L$.

[00143] “Electrical interconnection” and “electrical interconnect” refer to a component of an electrical device used for providing electrical communication between two or more device components. In some embodiments, an electrical interconnect is used to provide electrical communication between two device components spatially separated from one another, for example spatially separated by a distance greater than 50 nm, for some applications greater than 100 nm, for other applications greater than 1 μm , and for yet other applications greater than 50 μm . “Electrode contact” refers to a component of an electronic device or device component to which an electrical interconnect attaches or provides electrical communication to or from.

[00144] “Independently electrically addressable” refers to an electrical circuit wiring scheme where currents or potentials are provided to individual device components irrespective of currents or potentials provided to other device components. “Series configuration” refers to an electrical circuit wiring scheme where multiple device components carry the same current due to a single conduction path through all the device components. “Parallel configuration” refers to an electrical circuit wiring scheme where a single potential difference is applied across multiple device components.

[00145] “Embed” refers to a process by which one object or device is buried, conformally surrounded or otherwise placed or positioned within or below the surface of another object, layer or material.

[00146] “Encapsulate” refers to the orientation of one structure such that it is entirely surrounded by one or more other structures. “Partially encapsulated” refers to the orientation of one structure such that it is partially surrounded by one or more other structures or has one or more exposed regions, such as regions exposed to the surrounding environment. “Completely encapsulated” refers to the orientation of one structure such that it is completely surrounded by one or more other structures. Some embodiments contemplate devices having partially or completely encapsulated electronic devices, device components and/or inorganic semiconductor components and/or electrodes.

[00147] “Laminate” refers to a process by which two or more layers are joined together to form a single multilayer structure. In one embodiment, two or more layers are laminated by positioning an adhesive layer between each layer. In one embodiment, two or more layers are laminated by positioning the layers adjacent to one another and then encapsulating all layers into a single encapsulated structure.

[00148] “Replicate” refers to a process by which one or more relief features are transferred and/or recreated during casting, molding, embedding, or embossing processes. Replicated features generally resemble the features they originate from except that the replicated features represent the negative of the original features; that is where the original features are raised features, the replicated features are recessed features and where the original features are recessed features, the replicated features are raised features. “Replica molding” and “nano imprint lithography” refer to specific replicating methods known in the art of microfabrication.

[00149] “Relief feature” refers to portions of an object or layer exhibiting differences in elevation and slope between the higher and lower parts of the surface of a given area or portion of the object or layer. “Raised features” refer to relief features which extend above the surface or average surface level of an object or layer or relief features which have elevations higher than other portions of the surface of an object or layer. “Recessed features” refer to relief features which

extend below the surface or average surface level of an object or layer or relief features which have elevations lower than other portions of the surface of an object or layer.

[00150] “Unitary structure” refers to a structure having one or more components within a single continuous or monolithic body, and includes structures having a uniform or non-uniform composition.

[00151] “Contiguous” refers to materials or layers that are touching or connected throughout in an unbroken sequence. In one embodiment, a contiguous layer of a device has not been etched to remove a substantial portion (e.g., 10% or more) of the originally provided material or layer.

[00152] “Accommodate” and “accommodation” refer to the configuration of one surface or device to match the contours or relief features of another surface or device such that the two surfaces/devices are in intimate contact. In one embodiment, a surface which accommodates a device or device component is a microstructured or nanostructured surface having relief features which match the shape, contours and or dimensions of the device or device component.

[00153] “Conformal contact” refers to contact established between surfaces, coated surfaces, and/or surfaces having materials deposited thereon which may be useful for transferring, assembling, organizing and integrating structures (such as printable elements) on a substrate surface. In one aspect, conformal contact involves a macroscopic adaptation of one or more contact surfaces of a conformal transfer device to the overall shape of a substrate surface or the surface of an object such as a printable element. In another aspect, conformal contact involves a microscopic adaptation of one or more contact surfaces of a conformal transfer device to a substrate surface leading to an intimate contact without voids. The term conformal contact is intended to be consistent with use of this term in the art of soft lithography. Conformal contact may be established between one or more bare contact surfaces of a conformal transfer device and a substrate surface. Alternatively, conformal contact may be established between one or more coated contact surfaces, for example contact surfaces having a transfer material, printable element, device component, and/or device deposited thereon, of a conformal

transfer device and a substrate surface. Alternatively, conformal contact may be established between one or more bare or coated contact surfaces of a conformal transfer device and a substrate surface coated with a material such as a transfer material, solid photoresist layer, prepolymer layer, liquid, thin film or fluid.

[00154] “Conformable” refers to a device, material or substrate which has a bending stiffness sufficiently low to allow the device, material or substrate to adopt any desired contour profile, for example a contour profile allowing for conformal contact with a surface having a pattern of relief features.

[00155] “Bind” and “bond” refer to the physical attachment of one object to another. Bind and bond can also refer the retention of one object on another. In one embodiment an object can bind to another by establishing a force between the objects. In some embodiments, objects are bound to one another through use of an adhesion layer. In one embodiment, an adhesion layer refers to a layer used for establishing a bonding force between two objects.

[00156] “Placement accuracy” refers to the ability of a transfer method or device to transfer a printable element, to a selected position, either relative to the position of other device components, such as electrodes, or relative to a selected region of a receiving surface. “Good placement accuracy” refers to methods and devices capable of transferring a printable element to a selected position relative to another device or device component or relative to a selected region of a receiving surface with spatial deviations from the absolutely correct position less than or equal to 50 microns, more preferably less than or equal to 20 microns for some applications and even more preferably less than or equal to 5 microns for some applications. Methods and devices described herein include those comprising at least one printable element transferred with good placement accuracy.

[00157] “Fidelity” refers to a measure of how well a selected pattern of elements, such as a pattern of printable elements, is transferred to a receiving surface of a substrate. Good fidelity refers to transfer of a selected pattern of elements wherein the relative positions and orientations of individual elements are preserved during transfer, for example wherein spatial deviations of individual elements from their

positions in the selected pattern are less than or equal to 500 nanometers, more preferably less than or equal to 100 nanometers.

[00158] “Undercut” refers to a structural configuration wherein the bottom surfaces of an element, such as a printable element, bridge element and/or anchor element, are at least partially detached from or not fixed to another structure, such as a mother wafer or bulk material. Entirely undercut refers to a structural configuration wherein the bottom surface of an element, such as printable element, bridge element and/or anchor element, is completely detached from another structure, such as a host substrate or bulk material. Undercut structures may be partially or entirely free standing structures. Undercut structures may be partially or fully supported by another structure, such as a host substrate, mother wafer or bulk material, that they are detached from. Undercut structures may be attached, affixed and/or connected to another structure, such as a wafer or other bulk material, at surfaces other than the bottom surfaces.

[00159] “Anchor” refers to a structure useful for connecting or tethering one device or device component to another. “Anchoring” refers to a process resulting in the connection or tethering of one device or device component to another. Printable LED elements of the invention, such as printable InGaN structures, may be connected or otherwise attached to a host substrate via homogeneous anchoring or heterogeneous anchoring. Anchor structures useful in some embodiments include partially or fully undercut structures.

[00160] “Homogeneous anchoring” refers to an anchor that is an integral part of the functional layer. In general, methods of making transferable elements by homogenous anchoring systems is optionally by providing a wafer, depositing a sacrificial layer on at least a portion of a wafer surface, defining semiconductor elements by any means known in the art, and defining anchor regions. The anchor regions correspond to specific regions of the semiconductor element. The anchor regions can correspond to a geometrical configuration of a semiconductor layer, e.g., anchors defined by relatively large surface areas and connected to transferable elements by bridge or tether elements. Such geometry provides a means for facilitating lift-off of specific non-anchored regions for either single-layer or multi-layer embodiments. Alternatively, anchors correspond to semiconductor regions that are

attached or connected to the underlying wafer. Removing the sacrificial layer provides a means for removing or transferring semiconductor elements while the portion of semiconductor physically connected to the underlying wafer remains.

[00161] “Heterogeneous anchoring” refers to an anchor that is not an integral part of the functional layer, such as an anchor that is made of a different material than the semiconductor layer or is made of the same material, but that is defined after the transferable semiconductor elements are placed in the system. One advantage of heterogeneous anchoring compared to homogeneous anchoring relates to better transfer defining strategies and further improvement to the effective useable wafer footprint. In the heterogeneous strategy embodiment, a wafer is provided, the wafer is coated with a sacrificial layer, semiconductor elements are defined, and heterogeneous anchor elements are deposited that anchor semiconductor regions. In an aspect, the anchor is a resist material, such as a photoresist or SiN (silicon nitride), or other material that has a degree of rigidity capable of anchoring and resisting a lift-off force that is not similarly resisted by non-anchored regions. The anchor may span from the top-most semiconductor layer through underlying layers to the underlying wafer substrate. Removal of the sacrificial layer provides a means for removing unanchored regions while the anchored regions remain connected to the wafer, such as by contact transfer, for example. In another embodiment, for a multi-layer system, the anchor provides anchoring of a top layer to an underlying semiconductor layer. Alternatively, the anchoring system is for single-layer semiconductor layer systems.

[00162] “Carrier film” refers to a material that facilitates separation of layers. The carrier film may be a layer of material, such as a metal or metal-containing material positioned adjacent to a layer that is desired to be removed. The carrier film may be a composite of materials, including incorporated or attached to a polymeric material or photoresist material, wherein a lift-off force applied to the material provides release of the composite of materials from the underlying layer (such as a functional layer, for example).

[00163] In the context of this description, a “bent configuration” refers to a structure having a curved conformation resulting from the application of a force. Bent structures may have one or more folded regions, convex regions, concave regions,

and any combinations thereof. Useful bent structures, for example, may be provided in a coiled conformation, a wrinkled conformation, a buckled conformation and/or a wavy (i.e., wave-shaped) conformation.

[00164] Bent structures, such as stretchable bent interconnects, may be bonded to a flexible substrate, such as a polymer and/or elastic substrate, in a conformation wherein the bent structure is under strain. In some embodiments, the bent structure, such as a bent ribbon structure, is under a strain equal to or less than about 30%, a strain equal to or less than about 10%, a strain equal to or less than about 5% or a strain equal to or less than about 1% in embodiments preferred for some applications. In some embodiments, the bent structure, such as a bent ribbon structure, is under a strain selected from the range of about 0.5% to about 30%, a strain selected from the range of about 0.5% to about 10%, or a strain selected from the range of about 0.5% to about 5%. Alternatively, the stretchable bent interconnects may be bonded to a substrate that is a substrate of a device component, including a substrate that is itself not flexible. The substrate itself may be planar, substantially planar, curved, have sharp edges, or any combination thereof. Stretchable bent interconnects are available for transferring to any one or more of these complex substrate surface shapes.

[00165] “Thermal contact” or “thermal communication” refers to the arrangement of two materials or structures such that they are capable of substantial heat transfer from the higher temperature material to the lower temperature material, such as by conduction. In embodiments, electrical interconnects positioned in electrical contact with printable LED elements are also provided in thermal communication with the printable LED elements and/or are also provided in physical contact with the printable LED elements. In embodiments, electrical interconnects positioned in thermal communication with printable LED elements are also provided in physical contact with the printable LED elements.

[00166] “Heat dissipation” refers to a process of transferring heat from one object to another object or fluid. In embodiments, dissipation of heat is achieved by providing two objects in thermal communication, for example an electrical interconnect and a device element. In embodiments, heat dissipation is referred to in units of a rate of energy transferred, for example J/s or W.

[00167] “Heat capacity” refers to a property of a material corresponding to the amount of heat required to increase the temperature of the material by a specific amount, for example the amount of heat required to increase the temperature by 1 K. “Specific heat capacity” refers to a property of a material corresponding to the amount of heat required to increase the temperature of a specified mass of material by a specific amount, for example the amount of heat required to increase the temperature of 1 g of a material by 1 K.

[00168] “Thermal conductivity” refers to a property of a material describing the relative ability of the material to transfer heat. For example, a material with a higher thermal conductivity transfers heat more quickly than a material with a lower thermal conductivity. In specific embodiments, materials having relatively high thermal conductivities are useful for managing the temperature of objects that generate heat by transferring heat away from the objects more efficiently than would materials having relatively lower thermal conductivity.

[00169] “Ultrathin” refers to devices of thin geometries that exhibit extreme levels of bendability. In an embodiment, ultrathin refers to circuits having a thickness less than 1 μm , less than 600 nm or less than 500 nm. In an embodiment, a multilayer device that is ultrathin has a thickness less than 200 μm , less than 50 μm , or less than 10 μm .

[00170] “Thin layer” refers to a material that at least partially covers an underlying substrate, wherein the thickness is less than or equal to 300 μm , less than or equal to 200 μm , or less than or equal to 50 μm . Alternatively, a thin layer may be described in terms of a functional parameter, such as a thickness that is sufficient to isolate or substantially reduce the strain on the electronic device. A thin layer may be a functional layer (e.g. a layer that is sensitive to strain) in the electronic device.

[00171] “Isolate” refers to the presence of an elastomer layer that substantially reduces the strain or stress exerted on a functional layer when the device undergoes a stretching or folding deformation. In an embodiment, strain is said to be “substantially” reduced if the strain is at least a factor of 20, at least a factor of 50, or at least a factor of 100 times reduced compared to the strain of the same system without the elastomer layer.

[00172] “Dielectric” and “dielectric material” are used synonymously in the present description and refer to a substance that is highly resistant to flow of electric current. Useful dielectric materials include, but are not limited to, SiO_2 , Ta_2O_5 , TiO_2 , ZrO_2 , Y_2O_3 , Si_3N_4 , STO, BST, PLZT, PMN, and PZT. In an embodiment, an inorganic dielectric comprises a dielectric material substantially free of carbon. Specific examples of inorganic dielectric materials include, but are not limited to, silicon nitride and silicon dioxide.

[00173] “Device field effect mobility” refers to the field effect mobility of an electronic device, such as a transistor, as computed using output current data corresponding to the electronic device.

[00174] “Fill factor” refers to the percentage of the two-dimensional or three-dimensional area between two elements, such as between two electrodes, that is occupied by a material, element and/or device component. In one embodiment, two electrodes are provided in electrical contact with one or more printable semiconductor elements that provide a fill factor between first and second electrodes greater than or equal to 20%, preferably greater than or equal to 50% for some applications, and more preferably greater than or equal to 80% for some applications. In some embodiments, the term “density” refers to a specific number of elements found in a specified area.

[00175] “Multilayer stacked geometry” refers to a device comprising a plurality of functional layers in a stacked configuration. In some embodiments, stacked multilayers are provided in an offset configuration such that one or more device components in a first functional layer are not provided directly adjacent to one or more device components in a second functional layer, such as a first functional layer positioned adjacent to, above or below a second functional layer.

[00176] “Collecting” and “concentrating”, as applied to optics and optical components, refers to the characteristic of optical components and device components that collect light from a first area, in some cases a large area, and optionally direct that light to another area, in some cases a relatively smaller area. In the context of some embodiments, collecting and concentrating optical components

are useful for light detection or power harvesting by printed solar cells or photodiodes.

[00177] “Conductive material” refers to a substance or compound possessing an electrical resistivity which is typical of or equivalent to that of a metal, for example copper, silver or aluminum. In embodiments, the electrical resistivity of a conductive material is selected over the range of $1 \times 10^{-10} \Omega \cdot \text{cm}$ to $1 \times 10^{-2} \Omega \cdot \text{cm}$. In the present description, use of the term conductive material is intended to be consistent with use of this term in the art of electronic devices and electric circuits. In embodiments, conductive materials are useful as electrical interconnections and/or for providing electrical communication between two devices. A “conductive paste” refers to a conductive material comprising a mixture which is generally soft and malleable. In some embodiments, cured conductive pastes lose their soft and malleable nature and generally exhibit properties of a solid or a monolithic body. Exemplary conductive pastes comprise metal micro- and/or nano-particles. Silver epoxy refers to a conductive paste comprising micro- and/or nano particles including metallic silver (Ag) and which, when cured, exhibits a low electrical resistivity, for example an electrical resistivity lower than $1 \times 10^{-5} \Omega \cdot \text{cm}$ or selected over the range of $1 \times 10^{-10} \Omega \cdot \text{cm}$ to $1 \times 10^{-5} \Omega \cdot \text{cm}$.

[00178] “Fill” and “filling” refer to a process of depositing a material into a recessed feature. In one embodiment, a recessed region is filled by scraping material across and into the recessed feature. A filling tool generally refers to a device for moving material into a recessed feature. In an embodiment, a filling tool refers to a device for scraping material across and/or into a recessed region. In a specific embodiment, a filling tool comprises a layer or solid body of PDMS. For certain embodiments, a filling process is conceptually similar to a screen printing process where a material is scraped across a recessed feature by a tool or device having dimensions larger than the recessed feature, thereby at least partially filling the recessed feature with the material.

[00179] “Align” refers to a process by which two objects are arranged with respect to one another. “Aligned off center” refers to a process by which the centers of two objects or two areas are arranged such that the two centers are not coincident with respect to one or more spatial dimensions. For certain embodiments, the term

aligned off center refers to alignment of the center of two objects such that the centers of the objects are spatially separated by a distance greater than 50 nm, for some applications greater than 100 nm, for other applications greater than 1 μm , and for yet other applications greater than 50 μm .

[00180] “Neutral mechanical surface,” “NMS,” “neutral mechanical plane,” and “NMP” interchangeably refer to a position within a device or component under strain that experiences an absence of strain. In some embodiments a NMS or NMP is a plane positioned between two regions or layers of a device or component under strain, such as a plane between regions under compressive strain and regions under expansive strain. The NMP is less susceptible to bending stress than other planes of the device that lie at more extreme positions along a vertical axis of the device and/or within more bendable layers of the device. Thus, the position of the NMP is determined by both the thickness of the device and the materials forming the layer(s) of the device.

[00181] A “NMS adjusting layer” refers to a layer whose primary function is adjusting the position of the NMS in the device. For example, the NMS adjusting layer may be an encapsulating layer or an add layer such as an elastomeric material.

[00182] “Coincident” refers to the relative position of two or more objects, planes or surfaces, for example a surface such as a NMS or NMP that is positioned within or is adjacent to a layer, such as a functional layer, substrate layer, or other layer. In an embodiment, a NMS or NMP is positioned to correspond to the most strain-sensitive layer or material within the layer.

[00183] “Proximate” refers to the relative position of two or more objects, planes or surfaces. For example, a NMS or NMP is proximate to or closely follows the position of a layer, such as a functional layer, substrate layer, or other layer while still providing desired foldability or bendability without an adverse impact on the strain-sensitive material physical properties. “Strain-sensitive” refers to a material that fractures or is otherwise impaired in response to a relatively low level of strain. In general, a layer having a high strain sensitivity, and consequently being prone to being the first layer to fracture, is located in the functional layer, such as a functional layer containing a relatively brittle semiconductor or other strain-sensitive device

element. A NMS or NMP that is proximate to a layer need not be constrained within that layer, but may be positioned proximate or sufficiently near to provide a functional benefit of reducing the strain on the strain-sensitive device element when the device is folded.

[00184] “Adjacent” refers to the position of two or more structures, such as device components, that are located next to each other. In an embodiment, for example, proximate LED elements are positioned such that they are located next to each other in an LED array geometry. Adjacent structures, such as adjacent LED elements, are not necessarily provided in physical contact, and in some embodiments, for example, adjacent structures, such as adjacent LED elements, are separated by a distance greater than or equal to 2 μm , optionally for some applications are separated by a distance greater than or equal to 10 μm , optionally for some applications are separated by a distance greater than or equal to 100 μm , optionally for some applications are separated by a distance greater than or equal to 1000 μm , and optionally for some applications are separated by a distance greater than or equal to 10000 μm .

[00185] “Young’s modulus” refers to a mechanical property of a material, device or layer which refers to the ratio of stress to strain for a given substance. Young’s modulus may be provided by the expression;

$$E = \frac{(\text{stress})}{(\text{strain})} = \left(\frac{L_0}{\Delta L} \times \frac{F}{A} \right)$$

where E is Young’s modulus, L_0 is the equilibrium length, ΔL is the length change under the applied stress, F is the force applied and A is the area over which the force is applied. Young’s modulus may also be expressed in terms of Lamé constants via the equation:

$$E = \frac{\mu(3\lambda + 2\mu)}{\lambda + \mu}$$

where μ and λ are Lamé constants. High Young's modulus (or "high modulus") and low Young's modulus (or "low modulus") are relative descriptors of the magnitude of Young's modulus in a given material, layer or device. In the present description, a high Young's modulus is larger than a low Young's modulus, about 10 times larger for some applications, more preferably about 100 times larger for other applications and even more preferably about 1000 times larger for yet other applications. In an embodiment of the present invention, a polymer layer having a high Young's modulus comprises a polymer having a Young's modulus selected over the range of about 1 GPa to about 10 GPa. Exemplary high Young's modulus polymer layers may comprise polyimide, polyester, polyetheretherketone, polyethersulphone, polyetherimide, polyethyleneapthalate, polyketones, poly(phenylene sulfide), any combinations of these materials or other polymeric materials having similar mechanical properties. In an embodiment of the present invention, a polymer layer having a low Young's modulus comprises a polymer having a Young's modulus selected over the range of about 1 MPa to about 10 MPa. Exemplary low Young's modulus polymer layers may comprise elastomers such as, PDMS, h-PDMS, polybutadiene, polyisobutylene, poly(styrene-butadiene-styrene), polyurethanes, polychloroprene and silicones.

[00186] Figure 1A provides a top plan view of an electronic device **100** and Figure 1B provides a side view of electronic device **100**. As show in Figures 1A and 1B, electronic device **100** comprises a LED array comprising LED elements **200** and electrical interconnects **300A** (top side) and **300B** (bottom side) supported by a receiving surface **410** of a substrate **400**. LED elements **200** are provided in a sparse array geometry wherein adjacent LED elements are spaced apart from each other by distances **150** and **160**. LED elements **200** are characterized by lateral dimensions, such as width **250** and length **260**, and a thickness dimension **270**. Each LED element **200** includes two electrical contacts **210**. Electrical interconnects are also characterized by lateral dimensions, such as widths **350** and lengths **360**, and a thickness dimension **370A** and **370B**. In some embodiments, lateral and thickness dimensions of LED elements **200** are small enough so as to provide useful thermal properties, such as the ability to efficiently passively cool LED elements **200** via heat transfer and dissipation by electrical interconnects **300A** and **300B**. In some embodiments, lateral and thickness dimensions of electrical interconnects **300A** and

300B are large enough such that electrical interconnects **300A** and **300B** function as efficient heat sinks for dissipating heat generated by LED elements **200** during operation. Optionally, device **100** further comprises planarizing layer **680** and/or encapsulating layer **690**.

Example 1: Unusual Strategies for Using InGaN Grown on Silicon (111) for Solid State Lighting

[00187] Properties that can now be achieved with advanced, blue InGaN light emitting diodes (LEDs) lead to their potential as replacements for existing infrastructure in general illumination, with enormous positive implications on power efficiency. Further advances in this technology will benefit from re-examination of the modes for incorporating this materials technology into lighting modules that manage light conversion, extraction and distribution in ways that most critically minimize adverse thermal effects associated with operation, with packages that fully exploit the unique aspects of these light sources. This example describes techniques including anisotropic etching, microscale device assembly/integration, and module configuration that address these challenges in unconventional ways. Various device demonstrations provide examples of the capabilities, including thin, flexible lighting 'tapes' based on patterned phosphors and large collections of small, light emitters on plastic substrates. Quantitative modeling and experimental evaluation of heat flow in such structures illustrates one particular, important aspect of their operation: small, distributed LEDs can be passively cooled simply by direct thermal transport through thin film metallization used for electrical interconnect, providing an enhanced and scalable means to integrate these devices in modules for white light generation.

[00188] InGaN-based blue LEDs hold a dominant position in the rapidly growing solid-state lighting industry. The materials and designs for the active components of these devices are increasingly well developed, due to widespread research focus on these aspects over the last one and a half decades. Internal and external quantum efficiencies of greater than 70% and 60%, respectively, with luminous efficacies larger than 200 lm/W and lifetimes of >50,000 hours are now possible. High luminous efficacy of these LEDs (i.e. 249 lm/W) compared to that of a tri-phosphor fluorescent lamp (i.e. 90 lm/W) represents an appealing solution to more energy-

efficient lighting systems. In particular, electricity consumption for lighting could potentially be cut in half using solid-state lighting. Although there remain opportunities for further improvements in these parameters, the emergence of LEDs into a ubiquitous technology for general illumination will rely critically on cost effective techniques for integrating the active materials into device packages, interconnecting them into modules, managing the accumulation of heat during their operation, and spatially homogenizing their light output at desired levels of chromaticity. Existing commercial methods use sophisticated, high-speed tools, but which are based on conceptually old procedures that exploit robotic systems to assemble material mechanically diced from a source wafer, with collections of bulk wires, lenses and heat sinks in millimeter-scale packages, on a device-by-device basis, followed by separate steps to form integrated lighting modules. The intrinsic features of such processes prohibit cost competitive realization of some of the most appealing configurations of LEDs for lighting, such as those that involve large collections of ultra-small, thin devices distributed uniformly, but sparsely, over emissive areas of large modules that could serve as direct replacements for troffers currently used in fluorescent building lights. Alternative techniques, such as those that use directed assembly of solution suspensions of LEDs, first reported nearly twenty years ago, appear interesting but efforts to design commercially relevant manufacturing schemes have been unsuccessful. This example describes a set of procedures that address the limitations of existing approaches in a different way, using ideas that extend beyond previous flexible electronics, information displays and photo-voltaics systems, to the area of solid-state lighting by introducing new materials, etching strategies, interconnection methods, thermal management techniques and schemes for wavelength conversion and light distribution. The process begins with removal of InGaN epitaxial material grown on silicon wafers with (111) orientation, using lithographically defined structures and anisotropic wet chemical etching, in ways that bypass conventional laser liftoff techniques and wafer dicing. When implemented with fully formed LEDs, these ideas can be combined with precision assembly via transfer printing, to allow high-throughput manipulation of devices with geometries that are orders of magnitude smaller than those compatible with robotic pick-and-place procedures. Self-aligned techniques for thin film metallization that exploit the large band-gap of GaN provide remarkably simple

routes to interconnect large collections of devices. The outcome consists of finely distributed sources of illumination that naturally manage the thermal aspects of operation through dramatically accelerated rates for passive heat spreading, consistent with analytical models for heat flow. Laminating such systems with patterned layers of phosphors and film type optical diffusers yields thin, flexible lighting modules whose formats make them attractive for wide ranging applications in general illumination, both conventional and unconventional.

[00189] The work described in this example focuses on model multilayer InGaN epitaxial stacks grown on Si wafers with (111) orientation, due to the cost and throughput advantages that are expected to result from this materials technology when optimized to offer levels of quality (e.g. threading dislocation densities $< 10^9 \text{ cm}^{-2}$) currently available from material grown on conventional substrates such as sapphire or SiC. The layer configurations appear in Figure 8. As illustrated in Figure 9, lithographically patterned n-type ohmic contacts (Ti:15 nm/Al:60 nm/Mo:20 nm/Au:100 nm) result from electron beam (e-beam) evaporation and rapid thermal annealing (RTA, in N_2 ambient) of metal deposited on regions of n-GaN exposed by inductively coupled plasma reactive ion etching (ICP-RIE). Similar procedures yield partially transparent p-type ohmic contacts (Ni:10 nm/Au:10 nm) to the top p-GaN layer, as shown in Figure 10. Opaque pads (Ti:10 nm/Au:120 nm) e-beam evaporated on top of the p- and n- contacts enable single-step planarization and self-aligned passivation, using procedures outlined subsequently. Etching by ICP-RIE (i.e. mesa etch) defines the lateral dimensions of individual devices, in densely packed, arrayed layouts. Etching proceeds through the entire thickness of the InGaN material, and to a controlled depth ($\sim 1 \mu\text{m}$) into the silicon, for purposes of release described next. A representative array of such devices appears in graphic illustration in Figure 2A, and in a corresponding scanning electron microscope (SEM) image in shown in Figure 2C.

[00190] The procedure for releasing these devices from the underlying substrate exploits the large differences in rates ($>100\times$) for removing planes of Si(110) compared to Si(111) with wet chemical etching baths of potassium hydroxide (KOH) or tetramethylammonium hydroxide (TMAH). To take advantage of this effect, the arrays are configured such that two sides of each device lie perpendicular to $\langle 110 \rangle$.

The devices are tightly packed in this direction (i.e. spacing of 10 μm for this example, but with values that can be as small as 2 μm), and somewhat less so in the orthogonal direction (i.e. 40 μm shown here). Immersion in a hot, aqueous solution of KOH rapidly removes silicon along the Si(110) planes exposed by the mesa etch, thereby undercutting the devices without etching into the depth of the silicon wafer. Because the etching proceeds only along $\langle 110 \rangle$, relief structures of silicon remain in the orthogonal ($\langle 111 \rangle$) direction between devices. A pair of small supporting structures (i.e. anchors) of GaN, also defined during the mesa etch, connects each of the devices to the silicon in these regions (i.e. anchor bars), to yield freely suspended configurations after the KOH etching self-terminates on the (111) planes. A graphical illustration and corresponding SEM image appear in Figure 2B and Figure 2D, respectively. Figures 2E and 2F show magnified views of the anchor regions before and after anisotropic silicon etching. At this stage, the devices can be removed, in a non-destructive, high-speed and parallel operation, using soft stamps and the techniques of transfer printing. In this way, assembly into arrayed layouts on glass, plastic or other classes of substrate can be achieved at room temperature, with throughputs of millions of devices per hour and micron-scale positioning accuracy, in deterministic and adjustable ranges of pitch (Figure 11) over areas that can be much larger than those defined by the devices on the source wafer. The SEM images of Figures 2G-2I show a progression of a representative device from delineation on a donor substrate, to removal and delivery onto a receiving substrate, respectively. The LEDs formed in this manner have emission areas and thicknesses that can be up to 1600x and 100x smaller, respectively than conventional devices (i.e. $1 \times 1 \text{ mm}^2$). For these reasons, the devices are referred to herein as microscale inorganic light emitting diodes (μ -ILEDs).

[00191] The small thicknesses of μ -ILEDs make them amenable to interconnect based on thin film metallization, to provide a high-speed, parallel alternative to traditional wire bonds. Practical challenges exist for applications in lighting, however, due to requirements on overlay and registration, especially for large area modules (i.e. troffer-scale). Fortunately, the properties of GaN devices allow a remarkably simple method for accomplishing precise registration, without the need for lithographic alignment or photo-resist processing. In this “back-side exposure” (BSE) technique, both planarization and via formation occur simultaneously in a

single-step, self-aligned process. Here, the device structures themselves serve as a mask for photo-induced cross-linking of a polymer overcoat (Figure 12). Figure 3A shows an SEM image of a single $100 \times 100 \mu\text{m}^2$ μ -ILED printed on a glass substrate. Spin-coating a photosensitive polymer (Dow Chemical, Benzocyclobutene (BCB), Cyclotene 4024-40 Resin) fully encapsulates the device (Figure 3B). H-line radiation incident on the backside of the structure passes through the transparent substrate (e.g. glass or plastic) and the GaN (band gap $\approx 3.4 \text{ eV}$), to flood expose the polymer in all regions except those shadowed by the opaque contact pads, shown in colorized gold in Figure 3C. Washing away the unexposed regions leaves a pattern of polymer with openings at the contacts, and with positively sloped sidewalls for conformal deposition of interconnect metal (Figure 3D). Due to the encapsulating nature of the polymer coating, requirements on registration for the interconnects are greatly relaxed compared to those for the contact pads themselves. In particular, the relevant length scale for registration decreases from roughly the size of a contact pad to the size of an entire device. This improvement corresponds to a factor of four for the case considered here with $25 \times 25 \mu\text{m}^2$ contact pads, but could be as large as a factor of 20 with $5 \times 5 \mu\text{m}^2$ contact pads. As shown in Figure 3D, arrays were interconnected with overly wide leads (which easily accommodates small misalignments in the printed location of devices) by edge-over metallization, photolithographic patterning, and subsequent metal etching. This method is amenable to interconnecting large numbers of μ -ILEDs over large area arrays (e.g. 396 μ -ILEDs over $\sim 12 \text{ cm}^2$ in Figure 3G), shown here for arrays integrated on PET (Figure 3E) and on glass (Figures 3F and 3G) substrates, and for exceptionally small devices. As an example of the latter capability, vias of $\sim 4 \times 4 \mu\text{m}^2$ were easily formed on devices with lateral dimensions as small as $25 \times 25 \mu\text{m}^2$ (Figure 12D).

[00192] To illustrate the versatility, Figures 4A-4D show SEM images of exemplary μ -ILEDs with various sizes from (Figure 4A) $25 \times 25 \mu\text{m}^2$, (Figure 4B) $50 \times 50 \mu\text{m}^2$, (Figure 4C) $75 \times 75 \mu\text{m}^2$, and (Figure 4D) $150 \times 150 \mu\text{m}^2$. The sizes of the smallest and largest devices are limited by the resolution in device processing (i.e. lithography and mesa etching) and by degradation of etch-resist layers during silicon etching, respectively. The current density–voltage (J - V) characteristics of these μ -ILEDs show a noticeable increase in J as the size of μ -ILEDs decreases (Figure 4E). This behavior might be attributed to superior current spreading in small devices. The

properties are unaltered by the processing, as shown in Figure 4F. The small, thin geometries also provide enhanced mechanical bendability (Figure 13) and dramatically improved rates for passive thermal spreading. Both of these qualities facilitate integration with flexible sheets of plastic, as shown in Figure 3E. Details related to the bending mechanics appear below; the thermal properties represent a focus discussed shortly below.

[00193] To demonstrate integrated sources of white light that exploit these unique capabilities, schemes were developed for integrating phosphors, patterned into small tiles, with arrays of μ -ILEDs and thin film optical diffusers. As an example, a flexible lighting device that incorporates an amount of active material equal to that of a single, conventional $1 \times 1 \text{ mm}^2$ LED, but spread sparsely across an area of $\sim 300 \text{ mm}^2$ at an areal coverage corresponding to $\sim 0.3\%$, was built to optimize the thermal and optical properties (Figure 5 and Figure 14). The process for constructing these systems follows two parallel routes: (i), μ -ILED fabrication, array assembly and interconnection as shown in Figure 8 using a thin, PET substrate similar to the one in Figure 3, but with interconnects patterned such that 90% of each device is covered by reflective metal (Ti:3 nm/Al:500 nm), and the remaining 10% comprises the separation of leads to the p- and n- contacts; and, (ii), generation of a separate, patterned array of phosphor tiles matching the spatial geometry of the printed devices, on a soft, flexible sheet of the elastomer poly(dimethylsiloxane) (PDMS). The design of this second sub-module allows the use of phosphor only where required, i.e. directly above each of the μ -ILEDs in the array. A schematic representation of the processing steps appears in Figure 5A. The substrate consists of a thin sheet of PDMS embossed with an array of square wells of relief. A slurry incorporating a cerium-doped yttrium aluminum garnet phosphor (Intematix, NYAG-1) in an uncured PDMS matrix uniformly disperses the phosphor particles (Figure 15), in a manner that allows their delivery to the wells using a doctor blade. Thermally curing the slurry completes this part of the fabrication process. Soft contact lamination against a patterned, interconnected array of μ -ILEDs yields white light output, with chromaticity that can be tuned by controlling the well depth using slurries at a constant phosphor-in-PDMS weight loading (37.35 wt%). Chromaticity data at different phosphor thicknesses appear in a CIE 1931 color space diagram in Figure 5B. As expected, the chromaticity follows an approximately linear path

between the limits of the blue emission of the μ -ILED and yellow emission of the phosphor, with increasing thickness. For this PDMS-phosphor composition CIE coordinates of $x = 0.321$ and $y = 0.376$ with a phosphor thickness of $80\ \mu\text{m}$ were obtained.

[00194] The LED component of the system consists of 100 μ -ILEDs, each $100 \times 100\ \mu\text{m}^2$, in a hexagonal array, printed with an inter-device spacing of 2 mm, set to exceed the characteristic thermal diffusion length in this system. Figures 5C and 5D show images of the array before and after lamination against a sheet of patterned phosphor, respectively. (In this layout, the PET substrate provides a spacer between the μ -ILEDs and the phosphor tiles.) To complete the fabrication, a thin plastic diffuser film laminates onto the array to achieve diffuse, larger area emission, as in Figure 5E. This sparse array of printed μ -ILEDs provides an effective illuminated area >100 times larger than the area of a traditional LED die, in a way that uses the same amount of InGaN in a configuration that has strong optical and thermal benefits.

[00195] The thermal benefits of the type of layout in Figure 5 are critically important, due to the adverse effects of excessive heating that can occur in devices with conventional sizes (e.g. $1 \times 1\ \text{mm}^2$), in the absence of bulk, or miniature, heat sinking structures. Quantitative study shows that for the sparse, μ -ILED designs, the electrical interconnects serve simultaneously as effective heat sinks. This example examines the system using both analytical treatments and rigorous finite element methods (FEM) simulations. For the former, the approximately axi-symmetric nature of the system allows a precise analytical study of the thermal transport properties. Figure 6A shows the thicknesses H , thermal conductivity k , (the subscripts denote metal interconnect, BCB, μ -ILED, and glass, respectively), and surrounding temperature T_∞ . The heat source is modeled as a disk with a radius r_0 , and total heat generation Q , which is approximately equal to the input power to μ -ILED that does not result in light emission. The temperature distribution is obtained from the steady-state heat transfer governing equation $\frac{\partial^2 T}{\partial r^2} + \frac{1}{r} \frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial z^2} = 0$ in cylindrical coordinates (r, z) (Figure 6A). The boundary conditions include the free convection $-k_m \frac{dT}{dz} = h(T - T_\infty)$ at the top (air-interconnect) surface, and constant temperature T

$= T_{\infty}$ at the bottom (glass) surface, where h is the coefficient of natural convection. The continuity of temperature and heat flux across interconnect-BCB interface requires $[T] = 0$ and $\left[k \frac{\partial T}{\partial z}\right] = 0$, where $[]$ stands for the discontinuity between two adjacent layers. The above continuity conditions also hold at other interfaces. Heat generation requires $\left[k \frac{\partial T}{\partial z}\right] = \frac{Q}{\pi r_0^2}$ ($r \leq r_0$) across the top and bottom surfaces of a μ -ILED. The interconnect surface temperature is obtained as

$$T_{surface}(r) = T_{\infty} + \frac{Q}{2\pi r_0 k_b} \int_0^{\infty} \left[C_1(\xi) + C_2(\xi) e^{2\xi H_b} \right] e^{-\xi(H_b + H_m)} \frac{k_m}{k_m \xi + h} J_1(\xi r_0) J_0(\xi r) d\xi, \quad (1)$$

where

$$C_1(\xi) = (1 + k_b/k_m) \left\{ \left[(1 + k_g/k_b) - (1 - k_g/k_b) e^{2\xi(H_L + H_g)} \right] \beta(\xi) + 1 \right\},$$

$$C_2(\xi) = (1 - k_b/k_m) \left\{ \left[(1 - k_g/k_b) - (1 + k_g/k_b) e^{2\xi(H_L + H_g)} \right] \beta(\xi) - 1 \right\},$$

$$\beta(\xi) = \frac{\kappa + 1}{\left[(1 - k_g/k_b) - (1 + k_g/k_b) \kappa \right] - \left[(1 + k_g/k_b) - (1 - k_g/k_b) \kappa \right] e^{2\xi(H_L + H_g)}},$$

$$\kappa = \left[\left(1 - \frac{k_b}{k_m} \right) - \frac{k_m \xi - h}{k_m \xi + h} \left(1 + \frac{k_b}{k_m} \right) e^{-2\xi H_m} \right] e^{-2\xi H_b} / \left[\frac{k_m \xi - h}{k_m \xi + h} \left(1 - \frac{k_b}{k_m} \right) e^{-2\xi H_m} - \left(1 + \frac{k_b}{k_m} \right) \right], \text{ with } J_0$$

and J_1 being the Bessel functions of order 0 and 1, respectively. The operating μ -ILED temperature is given by

$$T_{LED} = T_{\infty} + \frac{2Q}{k_b \pi r_0^2} \int_0^{\infty} \left(1 - e^{2\xi(H_L + H_g)} \right) \frac{\beta(\xi)}{\xi^2} J_1^2(\xi r_0) d\xi. \quad (2)$$

[00196] This analytical treatment agrees well with full three-dimensional FEM simulations as shown in Figure 17. The differences between temperatures in Equations (1) and (2) and FEM simulations are less than 3% for μ -ILED sizes from 10 μm to 100 μm with 1000 nm-thick interconnects at a power density 400 W/cm^2 . The coefficient of natural convection is $h = 25 \text{ W}/\text{m}^2/\text{°C}$. Other conditions in experiments include the surrounding temperature $T_{\infty} = 50 \text{ °C}$, thickness and thermal conductivity $H_b = 1 \mu\text{m}$, $k_b = 0.3 \text{ W}/\text{m}/\text{°C}$ for BCB; $H_g = 800 \mu\text{m}$, $k_g = 1.1 \text{ W}/\text{m}/\text{°C}$ for

glass; $H_L = 5 \mu\text{m}$ for μ -ILED. The thermal conductivity for Al interconnects is thickness dependent, and is taken as $70 \text{ W/m/}^\circ\text{C}$ and $160 \text{ W/m/}^\circ\text{C}$ for 300 nm -thick and 1000 nm -thick interconnects, respectively. The radius of disk heat source is $r_0 = 56 \mu\text{m}$ to yield the same area as the square μ -ILED with dimensions of $100 \times 100 \mu\text{m}^2$.

[00197] The left and right frames of Figures 6B-6G show a set of experiments involving infrared thermal imaging of temperature distributions (QFI Infra-Scope Micro-Thermal Imager) and analytical predictions, respectively. These experiments compare surface temperatures for cases of Al interconnect with thicknesses of 300 nm and 1000 nm (Figures 6B-6D for 300 nm and Figures 6E-6G for 1000 nm), for input power ranging from 7.8 mW to 43.2 mW (i.e. power density ranging from 78 W/cm^2 to 432 W/cm^2). Figure 6H presents surface temperatures as a function of power, where analytical model results (lines) agree very well the experimental measurements (symbols) for devices with these two interconnect thicknesses.

[00198] The results of Figures 6B-6H clearly show pronounced decreases in the temperatures with thicker Al interconnects, thereby demonstrating that the interconnects themselves serve a dual role as efficient heat sinks by accelerating the rates of lateral thermal diffusion. These effects can be attributed predominantly to the significant thermal mass of the interconnects compared to the μ -ILEDs, and to their higher thermal conductivities. By consequence, both the thickness of the interconnects and the size of the devices are important. A theoretical parametric study, summarized in Figure 6I, shows the surface temperatures at a constant heat flux density of 400 W/cm^2 , as a function of these two variables. Clearly, the temperature can be greatly reduced by decreasing the sizes of the LEDs and by increasing the thicknesses of the interconnects. As a particular example, consider a conventional, macro-size LED (i.e. $1 \times 1 \text{ mm}^2$) and an array of 100μ -ILEDs (i.e. $100 \times 100 \mu\text{m}^2$) at a spacing of 2 mm on otherwise identical platforms, both at total input power densities of 400 W/cm^2 . The method of superposition is used to determine the temperature of μ -ILED arrays based on the solution for a single LED, i.e.,

$$T_{\text{array}}(r, z) = T_{\infty} + \sum_i [T_i(r, z) - T_{\infty}], \text{ where } T_i(r, z) \text{ is the temperature distribution due to}$$

*i*th μ -ILED. The surface temperature distributions for a macro-size LED and μ -ILED array with spacing 2 mm are shown in Figures 7A-7B, respectively. The maximum

temperature occurs at the center of the array and it decreases as the spacing increases (Figure 7C). The conventional LED would reach a temperature of over 1000 °C, whereas the array of μ -ILEDs would operate at $\sim 100^\circ\text{C}$ (Figure 17). In real devices, the conventional LED would be completely destroyed under these conditions, thereby motivating the requirement for advanced heat sinking structures of the type that are presently in use commercially. By contrast, the μ -ILEDs experience temperatures that enable stable operation, without any additional components.

[00199] The strategies described in this example incorporate advanced ideas in etching to release thin devices, self-aligned photo-exposures to form metal features that serve simultaneously as electrical interconnect and thermal heat spreaders, and module designs that include thin, patterned phosphors with film diffusers. This collection of procedures, combined with analytical models of heat flow, create new design opportunities in solid state lighting. Although all of these processes were combined to yield integrated systems, each can be implemented separately and matched to existing techniques for certain steps, to add new capabilities to otherwise conventional module designs. For example, the same concepts can be applied to active materials derived from epitaxial growth on sapphire substrates.

[00200] Materials and Methods. Fabrication of GaN μ -ILEDs. A GaN/Si(111) wafer (Azzurro Semiconductor) with layers of GaN:Mg (110 nm), five repeats of InGaN/GaN:Si (3 nm:10 nm), GaN:Si (1700 nm), AlN:Si/GaN:Si (1900 nm), GaN (750 nm), and AlN/AlGaIn (300 nm) served as the starting material. Spin casting, exposing, and developing a layer of photoresist (AZ5214-E, Clariant; developer, AZ327, Clariant) formed a square array of holes that provided an etch mask for ICP-RIE etching to expose the GaN:Si layer. After removing the resist with acetone, image-reversal photolithography defined another square array of holes, aligned to the first. Immersing the sample in a buffered oxide etchant (BOE) for 2 min, rinsing in deionized (DI) water and immediately loading into an e-beam evaporator enabled deposition of n-type ohmic contact metal (Ti:15 nm/Al:60 nm/Mo:20 nm/Au:100 nm). Rinsing the resist away with acetone and then annealing at 860 °C for 30 sec in N₂ ambient completed the formation of the n contacts. Image-reversal photolithography defined another array of holes. Immersing the sample in a solution of hydrochloric

acid ($\text{HCl}:\text{H}_2\text{O} = 3:1$) for 5 min and immediately loading into an e-beam evaporator enabled deposition of p-type ohmic contact metal (Ni:10 nm/Au:10 nm). Rinsing the resist away with acetone and subsequently annealing at 500 °C for 10 min $\text{N}_2:\text{O}_2$ (80:20) ambient completed the formation of p contacts. Next, image-reversal photolithography defined another array of holes for deposition of opaque contact pads by e-beam evaporation (Ti:10 nm/Au:120 nm), patterned by lift-off, as with the contact metal. As a resist for KOH attack on ohmic contacts, a 300 nm layer of silicon nitride was deposited by plasma enhanced chemical vapor deposition (PECVD). The geometry of the device array was photo-lithographically defined by patterning a metal etch mask of metal (Ti:50 nm/Ni:450 nm) by lift-off, and then removing the exposed silicon nitride by RIE with SF_6 . An ICP-RIE step provided the mesa etch, to generate an isolated array of devices. A commercial etchant (Ni Etchant Type TFB, Transene) removed the Ni mask. Anisotropic undercut etching of the silicon was performed by complete immersion in a solution of KOH (PSE-200, Transene) at 100 °C (hot plate temperature). Removing the silicon nitride by RIE completed the fabrication.

[00201] Fabrication of arrays of InGaN μ -ILEDs. Devices were transfer printed from the source wafer to a target substrate. BSE was performed by spin-casting and baking an adhesion layer (AP3000, Dow Chemical, 2000 rpm for 30 sec, 80 °C for 30 sec) and then spin-casting and pre-baking a layer of benzocyclobutene (Cyclotene 4024-40 Resin, 2000 rpm for 60 sec, 80 °C for 2 min). Samples were inverted, placed on a Cr-coated glass slide, exposed under a MJB3 Mask Aligner (Karl Suss), and then developed (DS2100). After curing (210 °C for 60 min O_2 -free glove box), the sample was exposed to RIE ($\text{O}_2:\text{CF}_4$ 4:1 mixture) to remove any residual cyclotene. Interconnect metal (Ti/Al in desired thickness) was sputter deposited and patterned by photolithography and metal etching (Ti-6:1 BOE, Al-Al Etchant Type A (Transene)).

[00202] Fabrication of thin, flexible white light modules. Fabricating supports for the phosphor involved casting and curing PDMS (10:1 mixture of base to curing agent) against a functionalized silicon wafer (trichlorosilane, United Chemical Technologies) with a photodefined set of structures of epoxy (SU-8 50, MicroChem Corp.) with desired thicknesses. Peeling away the cured PDMS yielded an array of

relief features ($500 \times 500 \mu\text{m}^2$) matching the spatial geometry of interconnected μ -ILEDs. Phosphor-containing islands were created by scraping a PDMS-based slurry of phosphor (NYAG-1, Intematix, created by mixing with uncured PDMS) across the PDMS substrate using a doctor-blade type implement consisting of a PDMS-coated razor blade. Thermal curing (70°C for >3 hr) completed the process. The phosphor mold was manually aligned and laminated to a matching array of μ -ILEDs. The module was completed by bonding an optical diffuser film (AX27425, Anchor Optics) to the phosphor mold.

[00203] Characterization of electrical, optical, mechanical, and thermal properties.

Electrical measurements were performed with a semiconductor parameter analyzer (4155C, Agilent or 2400 Sourcemeter, Keithley). Optical measurements of the emission spectra were performed with a high resolution spectrometer (HR4000, Ocean Optics). Color chromaticity was determined using SpectraSuite (Ocean Optics) with a radiometric calibration source (HL-2000, Mikropack) and an Ocean Optics spectrometer optical fiber in a fixed location ~ 1 mm above the sample. Bending measurements involved determining the forward voltage needed to produce 10 mA current with the sample mounted on cylindrical tubes with various radii, ranging from 5.9 mm to 65.3 mm. Fatigue measurements were performed by repeatedly bending the specimen from a flat state to the bent state with a bending radius of 5.9 mm. Thermal measurements of the surface temperature of μ -ILEDs were performed using MWIR-based InSb thermal imager (InfraScope, QFI) with the base temperature of 50°C .

[00204] Stack Design of InGaN/GaN Multiple Quantum Well (MQW) LED on Si(111) Substrate.

Figure 8 shows a schematic illustration of the epitaxial semiconductor multilayer stack of InGaN MQW LED on a Si(111) wafer. Active layers consist of a Si-doped n-GaN layer with a thickness of 1700 nm, 5 layers of multi-quantum well (MQW) of 3 nm InGaN and 10 nm of Si-doped GaN capped with Mg-doped p-GaN layer with a thickness of 110 nm. This wafer was purchased from Azzurro Semiconductor in Germany.

[00205] Fabrication Process of InGaN/GaN MQW μ -ILEDs on Flexible Substrates.

Figure 9 shows a schematic overview of the fabrication process. The process starts with InGaN epitaxial layers grown on a Si (111) wafer, as illustrated in Figure 8. For

photolithography, photo-resist AZ5214 was used as both a positive tone and negative tone resist. The steps for photolithography with this material appear below.

[00206] Photolithography using AZ5214 as a positive tone resist. a. Spin-coat at 4000 rpm for 30 seconds. b. Pre-bake at 110 °C for 60 seconds. c. Exposure dose of 78.5 mJ/cm² at 365nm. d. Develop in MIF 327 for 35 seconds. e. Hard bake at 130 °C for 180 seconds. f. O₂ descuum for 45 seconds in 250 mTorr, 20 sccm of O₂ under 50 W.

[00207] Photolithography using AZ5214 as a negative tone resist (Image Reversal). a. Spin-coat at 5000 rpm for 30 seconds. b. Pre-bake at 110°C for 60 seconds. c. Exposure dose of 110 mJ/cm² at 320 nm. d. Post-exposure bake (PEB) at 110 °C for 65 seconds. e. Flood UV exposure of 400 mJ/cm². f. Develop in MIF 327 for 35 seconds. More negatively sloped sidewalls can be achieved for easy lift-off if developed in MIF327 for longer time (i.e. additional 10~15 seconds). g. O₂ descuum for 45 seconds in 250 mTorr, 20 sccm of O₂ under 50 W.

[00208] N-ohmic contact recession. P-GaN and MQW layers must be etched in the region where n-ohmic contacts are to be formed. First, n-ohmic contact regions are photo-lithographically defined using AZ positive-tone process (see above). Etching the GaN can be achieved using ICP-RIE with BCl₃ and Cl₂ gases, with pressures of 3 mTorr and temperatures of 25 °C. A two-step etching process was employed. The first step consisted of 15 sccm of BCl₃ with RF power of 300 W and parallel plate DC voltage of 100 V for 90 seconds. The second step consisted of 15 sccm of Cl₂ gas with RF power of 300 W and parallel plate DC voltage of 100 V for an additional 120 seconds. An etch depth of 350 nm to 400 nm can be achieved with this recipe. After the ICP-RIE etching of GaN, the photo-resist (PR) was removed using acetone in an ultrasonic bath for about 120 seconds. The total etching depth was about 350 nm to 400 nm, as measured using profilometry.

[00209] N-ohmic contact Deposition and Annealing. Image Reversal of AZ5214-E (see above) and lift-off process were used to define n-ohmic contact metal. The native oxide on the surface n-GaN was removed using Buffered Oxide Etchant (BOE) at a 10:1 mixing ratio for 120 seconds prior to metal deposition. (Ti:15 nm) / (Al:60 nm) / (Mo:20 nm) / (Au:100 nm) were evaporated at base pressures of 8×10^{-7}

Torr as ohmic contacts to the n-GaN. An AG Assoc. Heatpulse 610 RTP was used for rapid thermal annealing at 860 °C for 30 seconds under N₂ environment.

[00210] P-ohmic contact Deposition and Annealing. Image reversal with AZ5214-E (see above) was used to define the p-ohmic contact regions. Immersion of p-GaN in HCl:DI=3:1 for 5 mins removed the native oxide. Ni (10nm)/Au (10nm) layers were deposited in an e-beam evaporator at a base pressure of $<5 \times 10^{-7}$ Torr at a relatively slow rate (approx. 0.5Å/s). After deposition, PR was removed using acetone in an ultrasonic bath for 120 seconds, and then Ni/Au layers were annealed in a furnace at 500 °C for 10 minutes in air (80% N₂ + 20% O₂) to improve the ohmic properties. Ohmic contact characteristics are depicted in Figure 10.

[00211] Opaque Contact Pad. Image reversal with AZ5214-E (see above) was used to define the opaque contact pad regions on both p-ohmic contact region and n-ohmic contact region. Opaque contact pads served not only as contact electrodes, but also as mask patterns for the self-aligned passivation process, as illustrated in Figure 12. As an opaque contact pad, Ti(10 nm) / Au(120 nm) was deposited using an e-beam evaporator. After deposition, PR was removed using acetone in an ultrasonic bath for 120 seconds.

[00212] SiN passivation layer deposition condition. SiN, which served as an etch barrier during the KOH undercut process, was deposited using an STS Multiplex PECVD system. 300 nm of SiN film was deposited at a pressure of 650 mTorr, temperature of 300 °C, and gas flow rates of 1960 sccm (N₂) + 40 sccm (SiH₄) + 35 sccm (NH₃). Mixed frequency RF power of 20 W, with frequencies of 13.56 MHz for 6 seconds and 380 KHz for 2 seconds was used.

[00213] Ni etch mask deposition. On top of SiN film, AZ5214-E was used in an image reversal mode (see above) to define the lateral dimensions of the μ-ILEDs and the geometries of the anchors. Ti (50 nm) / Ni (450 nm) was deposited using an e-beam evaporator at relatively high deposition rate of approx. 6Å/sec to minimize the thermal stress caused by the heating inside the chamber. After the deposition, PR was removed using acetone in an ultrasonic bath for 60 seconds.

[00214] SiN + GaN Dry etching. SiN was dry-etched using a parallel plate RIE (Unaxis/Plasma Therm) with 40 sccm of SF₆, 35 mTorr pressure, and 100 W RF

power, for an etch rate of SiN of ~100 nm/min. Upon the removal of SiN, GaN / InGaN / AlN / AlGaN epi-layers were all etched with a gas combination of BCl₃ / Cl₂ / Ar in inductively coupled plasma reactive ion etching (ICP-RIE, Plasma Therm SLR770). Two etching steps were incorporated in etching GaN / AlN based epitaxial layers, as in the following.

[00215] GaN etching step 1 in ICP-RIE. A. Pressure: 5 mTorr. B. Temperature: 25 °C. C. Gas: 10 sccm of BCl₃ + 16 sccm of Cl₂ + 4 sccm of Ar. D. ICP coil power of 500 W and parallel plate voltage of 300 V. E. Etching time: 1 minute.

[00216] GaN etching step 2 in ICP-RIE. A. Pressure: 5 mTorr. B. Temperature of 25 °C. C. Gas: 20 sccm of Cl₂ + 4 sccm of Ar. D. ICP coil RF power of 500 W and parallel plate voltage of 260 V. E. Etching time: 8 additional minutes.

[00217] Anisotropic etching of silicon using KOH (Transene PSE-200). A. Hot plate temperature: 100 °C. B. Etching time: 45 minutes for a 100 x 100 μm² device.

[00218] Ti / Ni, SiN removal. A. Ni etchant: (Transene TFB). B. Etch rate: 3 nm/sec at 25 °C. C. SiN is dry etched using conditions described above.

[00219] Transfer-printing. Transfer-printing of μ-ILEDs was carried out onto either glass or PET substrates. Glass substrates were prepared by cleaving a slide into appropriate dimensions. PET substrates were prepared by spinning uncured PDMS (10:1 mixture of base to curing agent) on a glass slide cleaved to appropriate dimensions at 2000 rpm for 30 seconds. The PET film (Dura-Lar, Grafix) was laminated to the uncured PDMS and the entire substrate was cured at 70 °C for 3 hours. A thin-film adhesive was spin-coated onto the secondary substrate after O₂ plasma (see above) at 3000 rpm for 30 seconds and soft-baked at 110 °C for 10 min. Transfer printing of μ-ILEDs was carried out in an automated printer system using PDMS as a stamp. Step and repeat printing allowed formation of arrays with arbitrary configurations. The thin-film adhesive was cured under UV light for 10 minutes.

[00220] Self-aligned passivation by Back-Side Exposure (BSE). A. Adhesion promoter (AP3000) is spin-coated at 2000 rpm for 30 seconds. B. Soft-baking at 80°C for 30 seconds. C. BCB (Cyclotene 4024-40, Dow) is spin-coated at 2000 rpm

for 60 seconds. D. Pre-baking at 80 °C for 120 seconds. E. Flood exposure dose from the back side of 123 mJ/cm² at 405 nm. F. Post-exposure baking (PEB) at 70 °C for 30 seconds. G. Develop in DS2100 for 70 seconds. H. Curing of BCB is carried out in oxygen-free environment at 210 °C for 60 minutes. I. Descum process using RIE at the pressure of 200 mTorr with 18 sccm of O₂ with 2 sccm of CF₄ with 150 W RF power for 30 seconds.

[00221] Metallization. Sputtered or e-beam evaporated Al was used for reflective interconnection. Aluminum was deposited and patterned photo-lithographically using AZ5214 and an etch-back process (Type A, Transene). Fully interconnected arrays of μ -ILED resulted from this metallization process.

[00222] Ohmic contact characterization of Ni / Au layers to p-GaN. Figure 10 illustrates the ohmic contact characteristics of Ni (10 nm) / Au (10 nm) to p-GaN. Figure 10A shows the current-voltage characteristics of Ni/Au contact to p-GaN with TLM pad spacings of 21 μ m in three different annealing conditions (i.e. as deposited, 5 minutes annealing, 10 minutes annealing, and 15 minutes annealing). Figure 10B shows a plot of total resistance at four different pad spacings ranging from 2.5 μ m to 17 μ m. The specific contact resistance could not be extracted due to the large sheet resistance associated with the highly resistive p-GaN. It is, however, qualitatively shown that 10 minutes annealing at 500 °C exhibits better ohmic characteristics than 15 minutes or 5 minutes annealing at the same temperature.

[00223] Versatility of transfer-printing process. The versatility of the transfer printing process is shown in Figure 11 via corresponding SEM images of (a) after KOH undercut and (b) after transfer printing. In Figure 11C, μ -ILEDs are transfer printed onto a glass substrate with varying pitches ranging from 25 μ m to 500 μ m.

[00224] Schematic for Passivation and Via formation using Back-side Exposure (BSE) Process. In Figure 12A, a schematic illustration of an unusual passivation scheme using a Back-Side Exposure (BSE) process is shown. The self-aligned passivation starts with a transparent substrate such as a glass or a plastic. A transfer-printed μ -ILED exhibits transparency in wavelengths above its band-gap. First, a photosensitive polymer with a significant sensitivity (absorption) in the wavelength regime higher than the corresponding wavelength of the band-gap of

GaN (~365 nm) is applied (e.g. by spin-coating) on the surface of printed μ -ILEDs. The polymer can effectively be cross-linked by the irradiation through the GaN and the substrate. The opaque contact pads serve as a masking layer. Corresponding SEM images of μ -ILEDs are shown in Figures 12B and 12C with a $100 \times 100 \mu\text{m}^2$ device and in Figure 12D with a $25 \times 25 \mu\text{m}^2$ device after the BSE process. Cross-sectional profiles of a passivated μ -ILED (acquired using profilometry) are shown in Figure 12E. This process naturally generates vias with positive sidewalls.

[00225] Uniformity in electrical properties of μ -ILED on mechanical deformation.

Figures 13A and 13B show electrical properties (I-V characteristics and forward voltage at 10 mA of current) for representative μ -ILEDs printed on a PET substrate measured for varying bending radii and repetitive cycles. These I-V data demonstrate that the μ -ILEDs do not change in an appreciable way to bending radii down to ~5.9 mm and up to 1000 bending cycles. For this specific substrate configuration, these results indicate robust operation of the devices to strains up to 0.18%.

[00226] Uniformity in electrical properties of μ -ILED in an array. Current-voltage characteristics of 100 μ -ILEDs from an array, shown in Figure 14A, exhibit excellent uniformity. For example, less than 100 mV difference in the forward voltage is shown at 3 mA current. An array consists of 100 μ -ILEDs in a hexagonal arrangement (e.g. equal spacing between all μ -ILEDs) are shown in Figure 14B.

[00227] Integration YAG:Ce Phosphors with μ -ILED in an array. Phosphors must be dispersed uniformly to generate uniform white light. Figure 15A shows optical microscope images of relief features filled with a PDMS/phosphor slurry (left column) and filled with the phosphor powder only (right column). Compared to the “dry filling” method, the PDMS/phosphor slurry provides excellent dispersion and uniformity of phosphor in the PDMS matrix. Emission spectra of white μ -ILEDs are shown in Figure 15B with phosphor layer thicknesses of 60 μm , 80 μm , and 105 μm .

[00228] Fabricating SU-8 mold for phosphor-containing island mold. A. Spin coat SU-8 5 on Si(100) wafer 1800 rpm for 30 sec. B. Bake at 95 °C for 5 min. C. Flood exposure dose of 216 mJ/cm^2 at 365 nm. D. Spin SU-8 50 and expose: a. For 60 μm film: Spin 1800 rpm for 30 sec, Exposure dose of 432 mJ/cm^2 at 365 nm; b. For

80 μm film: 1600 rpm for 30 sec, Exposure dose of 513 mJ/cm^2 at 365 nm; c. For 105 μm film: 1250 rpm for 30 sec, Exposure dose of 583 mJ/cm^2 at 365 nm. E. Bake at 65 $^{\circ}\text{C}$ for 1 min then ramp to 95 $^{\circ}\text{C}$, total bake time 11 min. F. Develop in SU-8 Developer 12 min. G. Bake 180 $^{\circ}\text{C}$ for 10 min. H. UVO treatment for 2 min. I. Treat with tridecafluoro-1,1,2,2-tetrahydrooctyl trichlorosilane for 2 hr in air-tight container.

[00229] Creating white light, μ -ILED. A. Cast 10:1 mixture (base to curing agent) of uncured PDMS over SU-8 master. B. Cure at 70 $^{\circ}\text{C}$ for 3 hrs. C. Create phosphor/PDMS slurry: Mix 37.35 wt% phosphor in 10:1 PDMS with glass stir rod. D. Drip small amount of slurry on PDMS mold. E. With PDMS-coated razor blade, squeegee slurry into relief features of PDMS mold. F. Repeat in orthogonal direction. G. Cure at 70 $^{\circ}\text{C}$ for 3 hrs. H. Phosphor-containing island mold is manually aligned to the back side of a functioning μ -ILED array.

[00230] Analytical Model of printed μ -ILED on a glass substrate. Basic equations. A half space with built-in disk heat source is used to model the present problem. The cylindrical coordinate system is set such that the origin is coincident with the center of the heat source. The steady-state axisymmetric heat conduction in cylindrical coordinates is

$$\frac{\partial^2 T}{\partial r^2} + \frac{1}{r} \frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial z^2} = 0, \quad (3)$$

Setting $\theta = T - T_{\infty}$, where T_{∞} is the remote temperature, the above equation is equivalent to

$$\frac{\partial^2 \theta}{\partial r^2} + \frac{1}{r} \frac{\partial \theta}{\partial r} + \frac{\partial^2 \theta}{\partial z^2} = 0, \quad (4)$$

Boundary and continuity conditions are as follows:

(Boundary Condition 1) $z = -H_g - H_L = h_1$ (Glass bottom surface):

$$\theta_g \Big|_{z=h_1} = 0 \quad (\text{BC1})$$

(Boundary Condition 2) $z = 0$ (BCB-glass interface):

Downward heat flux

$$-k_b \frac{\partial \theta_b}{\partial z} \Big|_{z=0} = G_1(r) = \begin{cases} -q_1, & 0 \leq r \leq r_0 \\ q_{0,\text{int}}, & r > r_0 \end{cases} \quad (\text{a})$$

Upward heat flux

$$-k_g \frac{\partial \theta_g}{\partial z} \Big|_{z=0} = G_2(r) = \begin{cases} q_2, & 0 \leq r \leq r_0 \\ q_{b,\text{int}}, & r > r_0 \end{cases} \quad (\text{b})$$

Here the heat flux satisfy the following conditions:

$$q_1 \pi r_0^2 + q_2 \pi r_0^2 = Q, \quad (\text{c})$$

$$\theta_g \Big|_{z=0} = \theta_b \Big|_{z=0}, \quad \left[-k_b \frac{\partial \theta_b}{\partial z} \right]_{z=0, r \geq r_0} = \left[-k_g \frac{\partial \theta_g}{\partial z} \right]_{z=0, r \geq r_0} \quad (\text{BC2})$$

where k_g and k_b are the thermal conductivities of glass and BCB, r_0 is the equivalent radius of LED and Q is the total heat generated in the LED.

(Boundary Condition 3) $z = H_b = h_2$ (BCB-interconnect interface):

$$\theta_b \Big|_{z=h_2} = \theta_m \Big|_{z=h_2}, \quad -k_b \frac{\partial \theta_b}{\partial z} \Big|_{z=h_2} = -k_m \frac{\partial \theta_m}{\partial z} \Big|_{z=h_2} \quad (\text{BC3})$$

where k_m is the thermal conductivity of metal interconnect.

(Boundary Condition 4) $z = H_b + H_m = h_3$ (Interconnect-air interface):

$$-k_m \frac{d\theta_m}{dz} \Big|_{z=h_3} = h \theta_m \Big|_{z=h_3} \quad (\text{BC4})$$

where h is the coefficient of convection at the lower surface of a plate.

[00231] Solution. Equation (3) is solved via the Hankel transform, for which the following transform pair of the first kind is used,

$$\begin{aligned} \varphi(r, z) &= \int_0^\infty \bar{\varphi}(\xi, z) J_0(\xi r) \xi d\xi \\ \bar{\varphi}(\xi, z) &= \int_0^\infty \varphi(r, z) J_0(\xi r) r dr \end{aligned} \quad (\text{5a,b})$$

where $\varphi(r, z)$ is the original function and $\bar{\varphi}(\xi, z)$ is the transform.

[00232] The Hankel transform of (4) is

$$\frac{d^2 \bar{\theta}}{d\zeta^2} - \zeta^2 \bar{\theta} = 0 \quad (6)$$

for which the solution is obtained as

$$\bar{\theta} = A e^{-\zeta z} + B e^{\zeta z}, \quad (7)$$

and the heat flux is

$$-k \frac{\partial \bar{\theta}}{\partial z} = k \zeta (A e^{-\zeta z} - B e^{\zeta z}) \quad (8)$$

where A and B are two unknown functions to be determined according to boundary and continuity conditions. The temperature and heat flux are obtained as

$$\theta = \int_0^\infty (A e^{-\zeta z} + B e^{\zeta z}) J_0(\zeta r) \zeta d\zeta \quad (9)$$

$$q_z = -k \frac{\partial \theta}{\partial z} = \int_0^\infty k \zeta (A e^{-\zeta z} - B e^{\zeta z}) J_0(\zeta r) \zeta d\zeta \quad (10)$$

[00233] The boundary and continuity conditions can also be expressed in Hankel transform. Using (5-8), the two unknowns A and B for each layer can be solved.

For glass,

$$\begin{aligned} A_g &= \frac{1}{\beta_1 - \beta_2 e^{-2\zeta h_1}} \frac{(\kappa_c + 1)}{k_b \zeta} \frac{Q}{\pi r_0} \frac{J_1(\zeta r_0)}{\zeta} \\ B_g &= -A_g e^{-2\zeta h_1} \end{aligned} \quad (11)$$

For BCB,

$$\begin{aligned} A_b &= \frac{1}{2} \left(1 + \frac{k_g}{k_b} \right) A_g + \frac{1}{2} \left(1 - \frac{k_g}{k_b} \right) B_g + \frac{1}{2k_b \zeta} \frac{Q}{\pi r_0} \frac{J_1(\zeta r_0)}{\zeta} \\ B_b &= \frac{1}{2} \left(1 - \frac{k_g}{k_b} \right) A_g + \frac{1}{2} \left(1 + \frac{k_g}{k_b} \right) B_g - \frac{1}{2k_b \zeta} \frac{Q}{\pi r_0} \frac{J_1(\zeta r_0)}{\zeta} \end{aligned} \quad (12)$$

For interconnect,

$$\begin{aligned} A_m &= \frac{1}{2} \left[\left(1 + \frac{k_b}{k_m} \right) A_b e^{-2\zeta h_2} + \left(1 - \frac{k_b}{k_m} \right) B_b \right] e^{2\zeta h_2} \\ B_m &= \frac{1}{2} \left[\left(1 - \frac{k_b}{k_m} \right) A_b e^{-2\zeta h_2} + \left(1 + \frac{k_b}{k_m} \right) B_b \right] \end{aligned} \quad (13)$$

where $\beta_1 = \left(1 - \frac{k_g}{k_b}\right) - \left(1 + \frac{k_g}{k_b}\right) \kappa_c$, $\beta_2 = \left(1 + \frac{k_g}{k_b}\right) - \left(1 - \frac{k_g}{k_b}\right) \kappa_c$

$$\kappa_c = \frac{\left(1 - \frac{k_b}{k_m}\right) e^{-2\xi h_3} - \frac{k_m \xi - h}{k_m \xi + h} e^{-2\xi h_3} \left(1 + \frac{k_b}{k_m}\right)}{\frac{k_m \xi - h}{k_m \xi + h} e^{-2\xi h_3} \left(1 - \frac{k_b}{k_m}\right) e^{2\xi h_3} - \left(1 + \frac{k_b}{k_m}\right)}.$$

The temperature in each layer can be obtained by Eq. (9). For example, the temperature in interconnect is given by

$$T_m(r, z) = T_\infty + \int_0^\infty (A_m e^{-\xi z} + B_m e^{\xi z}) J_0(\xi r) \xi d\xi. \quad (14)$$

The interconnect surface temperature is then obtained by setting $z = h_3$. The LED temperature can be approximated by its average value over the entire active region as

$$T_{LED} = T_\infty + \frac{2}{r_0} \int_0^\infty (1 - e^{-2\xi h_1}) A_g J_1(\xi r_0) d\xi. \quad (15)$$

[00234] The thermal conductivity of Al decreases as the film thickness decreases as shown in Figure 16. For the model described here, the thermal conductivity of Al is used as a fitting parameter, but with constraints to approximate literature values. In the case of 300 nm and 1000 nm Al interconnects, the thermal conductivities of 70 W/m/k and 160 W/m/k, respectively, are used in the model. These values were compared with reported values to make sure they are within the reasonable range as depicted in Figure 16.

[00235] Finite element model to determine the temperature distribution. A 3D finite element model is established to study the temperature distribution in the LED system and validate the analytical model. Eight-node, hexahedral brick elements in the finite element software ABAQUS are used to discretize the geometry. A volume heat source is applied on the LED. The thermal convection boundary is applied at the air-interconnect interface and a constant temperature is applied at the bottom of the glass substrate. For LED arrays, a $\frac{1}{4}$ unit cell is used to take advantage of symmetry and periodic boundaries are applied. The finite element simulations agree well with analytical modeling as shown in Figure 17.

[00236] Experimental setup for measuring the LED temperature. The printed μ -ILED is placed on a heated chuck with a base temperature of 50 °C, and pixel-by-pixel calibration is performed to yield a reference irradiance image of an unpowered sample in order to account for the emissivity differences on the sample surface. In some cases, however, when the material has emissivity <0.1 , such as Al, temperature measurement could be inaccurate due to very low thermal emission. A surface ink or polymer that emits as a blackbody can be placed on top of the sample and to eliminate variation in emissivity. This procedure was not used because of the destructive nature of this material to electrical devices. As a result, quantitative values were extracted for the temperature only at the open areas between Al interconnects.

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Example 2: High Efficiency, Microscale GaN Light Emitting Diodes and Their Thermal Properties on Unusual Substrates

[00237] This Example presents materials and assembly methods that enable efficient, ultrathin (slightly larger than 6 μm) LEDs based on GaN, with lateral dimensions ranging from $\sim 1 \times 1 \text{ mm}^2$ to $\sim 25 \times 25 \text{ }\mu\text{m}^2$, and their integration onto substrates of unconventional materials, including hydrogels. Quantitative experimental and theoretical studies shows the benefits of thermal management that results from these geometries, for both continuous and pulsed mode operation, the latter of which demonstrates potential for use of these technologies in bio-integrated contexts.

[00238] Materials and processing schemes for inorganic light emitting diodes (LEDs) are increasingly important for applications in areas ranging from consumer electronics to energy efficient lighting. Conventional routes to devices involve epitaxial growth of active materials followed by wafer dicing and pick-and-place robotic manipulation into individually packaged components, for interconnection by bulk wire bonding. Recently reported schemes based on advanced methods in epitaxial liftoff and deterministic assembly allow devices with extremely thin geometries, in layouts that can be interconnected by planar metallization and photolithography.^[1-6] Alternative, related strategies involve LEDs comprised of vertically aligned arrays of micro or nanowires to offer similar advantages, including the ability to form devices on thin, plastic substrates^[7-8], but also with relaxed constraints on growth conditions. These and other recent advances have the potential to create new engineering opportunities and application possibilities for LED technologies. Even if flexible LEDs are in high demand and have a lot of applications, high efficiency and robust, flexible LEDs and their thermal analysis have not been addressed or only theoretical analysis^[1] is reported. Importantly, these LEDs should be utilized in commercial/biomedical applications in the near future.

[00239] This Example presents materials and fabrication strategies that enable efficient, ultrathin (slightly larger than 6 μm) LEDs based on GaN, with lateral

dimensions ranging from $\sim 1 \times 1 \text{ mm}^2$ to $\sim 25 \times 25 \text{ }\mu\text{m}^2$, and their integration onto unconventional substrates. The process begins with high quality epitaxial material grown using state-of-the-art techniques on sapphire substrates, but with unusual methods for releasing this material in the form of completed devices suitable for assembly using the techniques of transfer printing. This strategy represents a significant improvement over recently reported ^[1] routes to similar classes of devices, which rely critically on comparatively low performance active materials grown on silicon. Particular additional points of emphasis in the following are theoretical and experimental aspects of heat dissipation with devices mounted on hydrogels and other 'soft' substrate materials, as models for their integration with organs of the body.

[00240] Figure 18 outlines the growth and processing steps, in a sequence of schematic illustrations, micrographs and images. Fig. 18A shows commercially obtained epitaxial material on sapphire, etched into square islands ($100 \times 100 \text{ }\mu\text{m}^2$) with L-shaped current spreading layers (Ni: 15 nm/Au 15 nm) and pads in the corners for top p-contacts (upper right; $25 \times 25 \text{ }\mu\text{m}^2$; Cr: 15 nm / Au: 300 nm), and recessed n-contacts (lower left; $25 \times 25 \text{ }\mu\text{m}^2$; Cr: 15 nm / Au: 300 nm). Details appear in the Methods section and in Fig. 23. Uniform deposition of a thin layer (200 nm) of SiN_x passivates and protects the top surfaces and sidewalls of these structures, as preparation for coating with a bilayer of Cr (adhesion layer: 15 nm) / Pd (150 nm) that facilitates bonding to another substrate (silicon or glass) which supports metallization of Cr (adhesion layer: 15 nm) / Pd (150 nm) / In (900 nm). Bonding at pressures and temperatures of 400 bar and 220 °C, respectively, causes the In (melting point $\sim 156 \text{ }^\circ\text{C}$; Brinell hardness 8.83 MPa (cf. lead (Pb): 38.3 MPa))^[9] to flow and partially fill the recessed n-contacts and the trenches between the devices. A fraction of the In forms an alloy with the Pd, ^[10-11] to form a solid layer (InPd_x) that prevents cracking in the LEDs during subsequent processing, including laser lift off (LLO) as described next.

[00241] Passing light from a krypton fluoride (KrF) (0.9 J/cm^2 , 248 nm wavelength) or yttrium aluminum garnet (YAG): Nd laser (0.3 J/cm^2 , 266 nm, single pulse with 5 ns exposure time) through the sapphire leads to strong absorption at the interface with the GaN, where thermal decomposition forms Ga metal and nitrogen gas.

Pressure associated with this process releases the GaN from the sapphire, in the form of individual microscale inorganic LEDs (μ -ILEDs). Heating to 70 °C (melting point of Ga is 29.7 °C^[9]) and applying mild mechanical force enables complete removal of the sapphire, as in Fig. 18B and Fig. 24. Immersing the exposed μ -ILEDs in dilute HCl (5 wt%) etches away the residual Ga, to yield clean surfaces on top. This same etchant removes unalloyed In, leaving only agglomerates of InPd_x . This remaining metal is important because it tethers the μ -ILEDs to the underlying substrate, in their transferred locations. The micrograph in Fig. 18C shows a sample after these process steps. The tilted scanning electron microscope (SEM) image in the inset reveals voids and InPd_x agglomerates between a representative μ -ILED and the substrate.

[00242] Contacting a bulk slab of poly(dimethylsiloxane) (PDMS) that has an array of vertical pillars (3 μm in diameter, 1.2 μm in height, and 5 μm spacings) embossed on its surface, and then peeling it away retrieves, in a single step, all of the μ -ILEDs from their substrate via separation at the contact points defined by the InPd_x , leaving the devices bound by van der Waals forces to the structured surface of the PDMS. Etching the exposed Pd and Cr layers removes all residual metal particles (Fig. 25 shows a Si wafer after removal of all μ -ILEDs) including, by liftoff, any remaining particulates of InPd_x . Fig. 18D presents optical micrographs of the results; the inset shows an individual μ -ILED on a structured PDMS slab. (As shown in this image, a fraction of the devices, typically $\sim 10\%$, undergo some translational and rotational misalignment during the transfer. This aspect of the process can be further minimized through optimized processing, or it can be accommodated in the steps described next.) Techniques of transfer printing are used to remove individual μ -ILEDs, or selected collections of them, from this PDMS slab and then to deliver them to nearly any substrate of interest, where they can be electrically interconnected to yield functional lighting systems using procedures described elsewhere ^[1]. (see Fig. 26-28) The printed μ -ILEDs on PET or any other transparent substrates were electrically interconnected after passivation by a “back side exposure” method^[1] using light sensitive tone resist. In case of a non-transparent, high heat dissipation substrate, like Al foil, the whole device layer including the printed μ -ILED and interconnects is transferred onto a non-transparent substrate (i.e. Al foil) by

additional transfer printing. The main focus of work presented here corresponds to systems in which the densely arrayed μ -ILEDs on the structured PDMS are distributed over large areas, in sparse coverages on soft substrates. Fig. 18E (left) shows an interconnected string of 12 μ -ILEDs on a strip ($5 \times 40 \text{ mm}^2$) of poly(ethylene terephthalate) (PET, 50 μm thick; Grafix® Dura-Lar™ film roll) and a square array of 100 μ -ILEDs on glass (right). Comparisons of performance in μ -ILEDs on sapphire and on PET (50 μm thick) (**Fig. 19 A-D**) reveal nearly identical behaviors at low power. At high power, the μ -ILEDs on sapphire show a slight blue-shift in emission wavelength (from 447 nm at 1 mA to 445.2 nm at 10 mA), consistent with charge accumulation that results from band filling effects described previously^[12-13]. By contrast, μ -ILEDs on PET exhibit red-shift (from 447.3 nm at 1 mA to 451.7 nm at 10 mA) due to heating associated with the low thermal conductivity of the PET (compared to the sapphire).^[13] (See Fig. 29 and 30.) Figure 19 shows a comparison of the μ -ILED properties to a commercialized LED. These properties can be enhanced through optimized processing and use of a high quality wafer stack.

[00243] As suggested by previous thermal modeling results, an advantage of μ -ILEDs on plastic substrates is their accelerated rates of passive heat spreading due to favorable size scaling effects in thermal transport.^[1] The strategy of Fig. 18 is compatible with a wide range of μ -ILED sizes (much wider than previously possible^[11]), in a manner that allows the first quantitative experimental investigations of these effects. **Fig. 20A** shows examples, from $1 \times 1 \text{ mm}^2$, $500 \times 500 \mu\text{m}^2$, $300 \times 300 \mu\text{m}^2$, $150 \times 150 \mu\text{m}^2$, $100 \times 100 \mu\text{m}^2$, $75 \times 75 \mu\text{m}^2$, $50 \times 50 \mu\text{m}^2$ to $25 \times 25 \mu\text{m}^2$. This size range spans the commercial regime to dimensions limited only by resolution and alignment accuracy set by tools for photolithography used in this work. Even the largest devices show spatially uniform emission across the active regions (Fig. 20B). Studies of size dependent operational characteristics over this available range illustrate clearly the relevant behaviors. Fig. 20C, for example, shows a sharp decrease in operating temperatures of μ -ILEDs on a 50 μm thick PET substrate, at the same power per unit area, with decreasing μ -ILED size. The results are significant reductions in the operating temperatures, and corresponding enhancements in efficiency (Fig. 20C). These improvements can be illustrated in

plots of the input and output power densities, shown in Fig. 20D. The overlap of these data at low power densities demonstrates that the beneficial aspects of small device geometries (in the regime studied) are due mostly to thermal effects and not, for example, to increases in optical output coupling efficiency which might also occur. These output power and junction temperature results from LEDs on PET show quite similar trends compared to LEDs on sapphire. ^[12-13]

[00244] This improvement in thermal behavior with decreasing size can be exploited by structuring an LED with conventional dimensions into an array of interconnected μ -ILEDs with sufficient spacing, as suggested theoretically in our recent report.^[1] **Figure 21** provides detailed experimental evidence of the effects. Here, two device designs are compared (Fig. 21A). The first involves a single, $500 \times 500 \mu\text{m}^2$ μ -ILED; the second is a 5 by 5 array of $100 \times 100 \mu\text{m}^2$ μ -ILEDs, separated by $200 \mu\text{m}$. Fig. 21B and Fig. 32 show heat dissipation results for the first case (red symbols $\circ$ experimental; black lines – analytical models; black symbols $\blacksquare$ finite element models) at 40 mW of applied power at room temperature. The peak device temperature is $\sim 86^\circ\text{C}$, with a characteristic lateral decay length of $\sim 200 \mu\text{m}$ along the PET substrate ($\sim 50 \mu\text{m}$ thick). Separating adjacent μ -ILEDs in the 5×5 array by slightly more than $200 \mu\text{m}$ can yield significant reductions in peak temperatures. Measurements on arrays with various separations were performed; the results for the peak temperatures appear in Fig. 21C and Fig. 33-36, at applied powers of 20 mW and 40 mW. (The characteristic lateral decay length will be sensitive to many parameters, including the PET thickness, i.e. increasing the thickness increases this length. Some modeling results appear in Fig. 30-37.)

[00245] As with the thickness, the intrinsic thermal properties of the substrate materials have a large effect on heat dissipation, consistent with expectation. **Figure 22** shows results from two dramatically different cases: $700 \mu\text{m}$ thick Al foil and 2 mm thick hydrogel. The μ -ILED on Al foil reaches only 48°C at 40 mW of applied power (Fig. 22A and Fig. 38) and it cannot be degraded even after 5 min operation while an identical one on hydrogel reaches 65°C even at only 5 mW (Fig. 22B and Fig. 39). At 40 mW, this latter case leads to strong degradation of both the device and the substrate even at 5 sec operation, due to the high temperatures that are reached (cf. 232°C at 30 mW). Nevertheless, as discussed above, small device

geometries create opportunities for reliable operation even on such substrates, thereby demonstrating their potential use on or under the skin or integrated with internal tissues of the body. Here, pulsed mode can provide additional benefits, especially in applications of optogenetics, where the biological response can be suppressed with continuous mode operation.^[14] The thermal behaviors under pulsed operation are shown in Fig. 22C for an μ -ILED on hydrogel, to simulate biological tissue, for various duty cycles (1, 10, 30, 50, 70, 90 and 100 %) at 30 mW peak power. The various duty cycles of 1, 10, 30, 50, 70, 90 and 100% correspond to on and (off) times of 10 μ s (990 μ s), 100 μ s (900 μ s), 300 μ s (700 μ s), 500 μ s (500 μ s), 700 μ s (300 μ s), 900 μ s (100 μ s). As can be seen in simulation results in Fig. 22C (black symbols, $\circ$ (minimum) and $\bullet$ (maximum temperature)) and right images of Figs. 22D, 40 and 41, the time dependent behavior of the temperature reflects the pulsed operational mode, with decreases in temperature between pulses, due to thermal diffusion. As the duty cycle decreases, so does the temperature, from 232 °C at 100 % (Fig. 40) to 30.3 °C at 1 % (Fig. 22D and Fig. 42). For the regimes of operation explored here, reducing the duty cycle of the pulsed mode at short period (less than 1 ms) has similar effects to reducing the average power in a continuous (i.e. non-pulsed) mode (Fig. 43). For example, the temperature of a μ -ILED with 50 % duty cycle and 1ms period at 30 mW is about 128 °C (maximum and minimum of 154 °C and 102 °C, respectively), similar to the temperature (125 °C) at 15 mW continuous power. The characteristic times for passive cooling in this case are $\sim$ 20 ms. (Fig. 22E) The pulsed mode shows promise for achieving challenging requirements in optogenetics, where peak powers must be $\sim$ 10 mW/mm² with sustained changes in temperature of less than 1-2 °C.^[14]

[00246] The results reported here demonstrate that state-of-the-art GaN epitaxial materials grown on sapphire substrates can be manipulated in the form of μ -ILEDs, for use in applications that would be difficult or impossible to address with conventional LED technologies.

Experimental Section

[00247] *Delineating μ -ILEDs and forming Ohmic contacts on them.* The fabrication began with GaN epitaxially grown on a double-sided polished sapphire wafer (2 inch

diameter; Cermet Inc.). The epitaxial layers consisted of undoped GaN (3.8 μm), n-type doped GaN (2 μm), multiple quantum wells (0.14 μm), and p-type doped GaN (0.2 μm). Rinsing with diluted HCl (HCl:DI=1:3) for 5 min removed residual metal ions and oxidized GaN. Sputter deposition (AJA, ATC 2000) formed a bilayer of Ni (15 nm) and Au (15 nm) as a thin p-contact. Wet etching the Au (for 3 s) and Ni (for 2 min) with commercial etchants (Transene) patterned this bilayer into a *L*-shape for effective current spreading. The sample was annealed in an oxygen and nitrogen atmosphere at 500 °C for 5 min to enhance the contact properties. Next, patterning photoresist near the inner edges of the *L*-shaped pad and then removing the exposed epitaxial material by chlorine based inductively coupled reactive ion etching (ICP-RIE; PlasmaTherm, SLR-770) formed square (40×40 μm^2) recessed regions to open access to the n-type layers at the base. In a single step, contact pads to the n- and p- regions, each 25×25 μm^2 , were formed by electron beam evaporation (Temescal, FC-1800) of 15 nm of Cr and then 300 nm of Au. A low-stress silicon nitride (200 nm; SiN_x) was then formed uniformly over the entire substrate, using plasma enhanced chemical vapor deposition (PECVD; STS, Mesc Multiple). Next, a negative tone photoresist (PR, 7 μm thick; MicroChemicals Inc., AZ nLOF 2070) was patterned by photolithography, to serve as a mask for etching the SiN_x as well as the GaN to define the lateral dimensions of arrays of μ -ILEDs. As a final step, residual PR was removed by immersion in piranha solution (3:1 mixture of sulfuric acid with hydrogen peroxide at 90 °C) for 5 min.

[00248] *Bonding and Laser Lift Off (LLO).* After delineating and forming contacts for the μ -ILEDs, another layer of SiN_x (200 nm) was deposited for passivation, as preparation for wafer bonding and transfer. The process used Cr (15 nm) / Pd (150 nm) on the SiN_x -coated μ -ILED substrate and Cr (15 nm) / Pd (150 nm) / In (900 nm) on a target silicon wafer. The bonding occurred upon contact with a pressure of 400 bar and heating to 220 °C. The LLO used 0.9 J/cm² from a krypton fluoride (KrF) laser (JSPA, excimer laser with 248 nm wavelength) or 0.3 J/cm² from yttrium aluminum garnet (YAG) laser (Sandia Nat. Lab, third harmonic of a Q-switched YAG:Nd laser, 266 nm wavelength, single pulse with 5 ns exposure time), directed through the polished bottom surface of the sapphire. Absorption occurred at the GaN-sapphire interface, to cause decomposition of the undoped GaN into nitrogen (N_2) and gallium (Ga) metal according to: $2\text{GaN} \rightarrow 2\text{Ga (m)} + \text{N}_2 \text{ (g)}$. The sample

was then heated to 70 °C, to melt the Ga. Afterward, the sapphire substrate could be removed easily, to complete the transfer of GaN.

[00249] *Transfer printing individual μ -ILEDs.* Immersion in dilute HCl (5 % volume ratio) removed the unalloyed In in the vicinity of the bonding layer. The In-Pd alloy was not removed in this etchant, thereby leaving it to serve as distributed tethers (i.e. anchors) to hold the μ -ILEDs to the underlying silicon. Next, the residual Pd and Cr material on the passivated μ -ILEDs was eliminated by Pd and Cr etchant (Transene Inc.), respectively. Contacting a bulk slab of PDMS with an array of vertical pillars (3 μ m in diameter, 1.2 μ m in height, and 5 μ m in space) against the processed substrate and then quickly peeling it back transferred all of the μ -ILEDs to the structured surface of the PDMS. Etching the exposed Pd and Cr layers removed substantially all residual metal. A PDMS stamp with posts (100 $\times$ 100 μ m and heights of 100 μ m) was positioned above the μ -ILEDs to allow their retrieval and printing to a substrate of interest. The printing was performed using a slightly modified mask aligner (Karl Suss, MJB) or an automated printing machine. The structured PDMS slab is important because it allows the μ -ILEDs to be flipped over for further processing, in a way that provides sufficiently weak adhesion (defined by van der Waals interactions, and contact area) for efficient retrieval by transfer printing.

[00250] *Interconnect.* To form interconnected arrays of μ -ILEDs, or for electrically probing individual devices, the SiN_x layer was first etched away by reactive ion etching (RIE; a mixture of CF₄ (40 sccm) and O₂ (1.2 sccm); Plasmatherm 790). Coating with an adhesion promoter (Dow, AP3000) and then a layer of photosensitive benzocyclobutene (6 μ m thick; BCB) prepared the devices for backside exposure to ultraviolet light, through a transparent substrate. This light exposes the BCB in all regions except those above the opaque n-, and p- contact pads. Developing away the unexposed BCB (Advanced Developer, DS2100) and blowing with a stream of N₂ removed the residual developer, to complete the patterning process. After fully curing the BCB in an Ar atmosphere glove box, remaining BCB residue was removed by oxygen RIE. To form metallization lines to the contacts, 15 nm of Cr and 300 nm of Au were sputtered, and then etched using a mask of patterned PR.

[00251] *Characterization of electrical, optical and thermal properties.* A semiconductor parameter analyzer (4155C, Agilent) was used to measure the electrical properties. Optical measurements of the emission spectra and light output were performed with a spectrometer (HR4000 and FOIS-1 fiber optics integrating sphere, Ocean Optics). Radiant efficiency was simply calculated by $P_{\text{out}}/P_{\text{in}}$. Thermal measurements were performed using a MWIR-based InDb thermal imager (InfraScope, GFI) with a base temperature of 30°C.

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Analytical Model of printed μ -LED on a PET substrate

[00252] The approximately axisymmetric nature of the problem allows an analytical study of the thermal transport properties. The LED is modeled as a disk heat source with the total heat generation Q and a radius $r_0 = L/\sqrt{\pi}$ such that it yields the same area as a square ($L \times L$) LED. Schematic illustration of the device geometric and thermal parameters used in the model is shown in Fig. 31. The BCB layer encapsulating the entire LED on a PET substrate (thickness H_p and thermal conductivity k_p) can be divided into two layers. The top layer (thickness H_B and thermal conductivity k_B) is BCB only while the bottom layer (thickness H_L and thermal conductivity k_L) includes both BCB and LED.

[00253] The temperature distribution $T(r, z)$ at each layer can be obtained from

the steady-state heat transfer governing equation $\frac{\partial^2 T}{\partial r^2} + \frac{1}{r} \frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial z^2} = 0$ in cylindrical

coordinates (r, z) with the origin coincident with the center of the heat source. The boundary conditions include constant temperature $T = T_\infty$ at the bottom surface ($z = -H_p - H_L$) of PET and natural convection $-k_B \partial T / \partial z = h(T - T_\infty)$ at the top surface ($z = H_B$) of BCB, where h is the coefficient of natural convection. At the interface $z = -H_L$, the temperature and heat flux are continuous, i.e., $[T] = 0$ and $\left[k \frac{\partial T}{\partial z} \right] = 0$, where $[]$ stands for the discontinuity between two adjacent layers. At the interface $z = 0$, $[T] = 0$ holds for all r , $\left[k \frac{\partial T}{\partial z} \right] = 0$ for $r \geq r_0$, and $\left[k \frac{\partial T}{\partial z} \right] = \frac{Q}{\pi r_0^2}$ for $r \leq r_0$. The steady-state heat transfer governing equation can be solved via Hankel transformation. The surface temperature is obtained as

$$T_{surface}(r) = T_\infty + \int_0^\infty \frac{2k_B \xi}{k_B \xi + h} A_B e^{-\xi H_B} J_0(\xi r) \xi d\xi, \quad (1)$$

$$\text{where } A_B = \frac{\kappa_L + 1}{\left(1 - \frac{k_L}{k_B}\right)(\kappa_L - \kappa_B) + \left(1 + \frac{k_L}{k_B}\right)(1 - \kappa_L \kappa_B)} \frac{Q}{k_B \pi r_0^2 \xi^2} J_1(\xi r_0), \quad \kappa_B = \frac{k_B \xi - h}{k_B \xi + h} e^{-2\xi H_B},$$

$$\text{and } \kappa_L = \frac{\left(1 + \frac{k_p}{k_L}\right) e^{-2\xi H_p} - \left(1 - \frac{k_p}{k_L}\right)}{\left(1 - \frac{k_p}{k_L}\right) e^{-2\xi H_p} - \left(1 + \frac{k_p}{k_L}\right)} e^{-2\xi H_L}. \quad \text{The above temperature holds for } r \geq r_0. \quad \text{For}$$

the temperature within the active region ($r \leq r_0$), it is approximately a constant (See Fig. 21B), which can be approximated by the average value as

$$T_{Surface}(r; r \leq r_0) = T_\infty + \frac{2}{r_0} \int_0^\infty \frac{2k_B \xi}{k_B \xi + h} e^{-\xi H_B} J_1(\xi r_0) A_B d\xi, \quad (2)$$

The LED temperature is given by

$$T_{LED} = T_\infty + \frac{2}{r_0} \int_0^\infty (1 + \kappa_B) J_1(\xi r_0) A_B d\xi. \quad (3)$$

[00254] Figure 20C shows surface temperature in Eq. (2) versus the LED size for a power density 16 W/cm^2 , ambient temperature $T_\infty = 30^\circ \text{C}$, coefficient of natural convection $h = 25 \text{ W/m}^2/\text{K}$ [1], thicknesses $H_p = 75 \mu\text{m}$, $H_L = 6.54 \mu\text{m}$ and $H_B = 0.5 \mu\text{m}$, and thermal conductivity $k_p = 0.15 \text{ W/m/K}$ [2], $k_L = 1.6 \text{ W/m/K}$, and

$k_B = 0.3 \text{ W/m/K}$ [3], where k_L is an effective thermal conductivity that accounts for the 3D effect of LED. The analytical results agree well with experiments (Fig. 21C). The temperature profile shown in Fig. 21B also agrees well with experiments and 3D finite element analysis.

[00255] The method of superposition is used to determine the temperature of μ -ILED arrays based on the solution for a single LED, i.e.,

$$T_{array}(r, z) = T_{\infty} + \sum_i [T_i(r, z) - T_{\infty}], \text{ where } T_i(r, z) \text{ is the temperature distribution due to}$$

the i^{th} μ -ILED. The surface temperature distributions for a single $500 \times 500 \mu\text{m}^2$ μ -ILED and 5 by 5 arrays of $100 \times 100 \mu\text{m}^2$ μ -ILEDs with different separations are shown in Fig. 33-36 at applied powers of 20 mW and 40 mW. The maximum temperature occurs at the center of the array and it decreases with increasing the spacing (Fig. 21C). Once the spacing is larger than the characteristic lateral decay length $\sim 200 \mu\text{m}$, the temperature remains unchanged and is equal to that of a single $100 \times 100 \mu\text{m}^2$ μ -ILED.

Finite element model to determine the temperature distribution

[00256] A 3D finite element model is established using ABAQUS finite element software to obtain the temperature distribution in the LED systems (LED on a PET substrate in Fig. 31, LED on an aluminum substrate in Fig. 38 and LED on a hydrogel substrate in Fig. 39). The geometry is discretized by eight-node, hexahedral brick elements. A volume heat source is applied on the LED. The thermal convection boundary condition is imposed at the air-BCB or air-SU8 interface and a constant temperature is applied at the bottom of the substrate.

[00257] The thermal properties for the LED/PET system are given in the previous section. The properties for LED/aluminum and LED/hydrogel include the thermal conductivity, thermal capacity and mass density of 0.2 W/m/K , 1200 J/kg/K and 1190 kg/m^3 for SU8 [4,5], 0.52 W/m/K , 1150 J/kg/K and 1430 kg/m^3 for PI [6,7], 0.6 W/m/K , 2375 J/kg/K and 1112 kg/m^3 for hydrogel [8], and 148 W/m/K , 700 J/kg/K and 2330 kg/m^3 for an LED that is approximated by the properties of Si [9]. The thermal conductivity of aluminum and PDMS are 237 W/m/K [10] and 0.15 W/m/K [11],

respectively. The comparisons of FEM simulations with experiments for constant power and pulsed power are shown in Fig. 22 and Fig. 40-42.

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STATEMENTS REGARDING INCORPORATION BY REFERENCE AND VARIATIONS

[00258] All references throughout this application, for example patent documents including issued or granted patents or equivalents; patent application publications; and non-patent literature documents or other source material; are hereby incorporated by reference here in their entireties, as though individually incorporated by reference, to the extent each reference is at least partially not inconsistent with the disclosure in this application (for example, a reference that is partially inconsistent is incorporated by reference except for the partially inconsistent portion of the reference).

[00259] The terms and expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention in the use of such terms and expressions of excluding any equivalents of the features shown and described or portions thereof, but it is recognized that various modifications are possible within the scope of the invention claimed. Thus, it should be understood that although the present invention has been specifically disclosed by preferred embodiments, exemplary embodiments and optional features, modification and variation of the concepts herein disclosed may be resorted to by those skilled in the art, and that such modifications and variations are considered to be within the scope of this invention as defined by the appended claims. The specific embodiments provided herein are examples of useful embodiments of the present invention and it will be apparent to one skilled in the art that the present invention may be carried out using a large number of variations of the devices, device components, method steps set forth in the present description. As will be obvious to one of skill in the art, methods and devices useful for the present methods can include a large number of optional composition and processing elements and steps.

[00260] When a group of substituents is disclosed herein, it is understood that all individual members of that group and all subgroups, including any isomers, enantiomers, and diastereomers of the group members, are disclosed separately. When a Markush group or other grouping is used herein, all individual members of the group and all combinations and subcombinations possible of the group are intended to be individually included in the disclosure. When a compound is described herein such that a particular isomer, enantiomer or diastereomer of the compound is not specified, for example, in a formula or in a chemical name, that description is intended to include each isomers and enantiomer of the compound described individually or in any combination. Additionally, unless otherwise specified, all isotopic variants of compounds disclosed herein are intended to be encompassed by the disclosure. For example, it will be understood that any one or more hydrogens in a molecule disclosed can be replaced with deuterium or tritium. Isotopic variants of a molecule are generally useful as standards in assays for the molecule and in chemical and biological research related to the molecule or its use. Methods for making such isotopic variants are known in the art. Specific names of compounds are intended to be exemplary, as it is known that one of ordinary skill in the art can name the same compounds differently.

[00261] Many of the molecules disclosed herein contain one or more ionizable groups [groups from which a proton can be removed (e.g., -COOH) or added (e.g., amines) or which can be quaternized (e.g., amines)]. All possible ionic forms of such molecules and salts thereof are intended to be included individually in the disclosure herein. With regard to salts of the compounds herein, one of ordinary skill in the art can select from among a wide variety of available counterions those that are appropriate for preparation of salts of this invention for a given application. In specific applications, the selection of a given anion or cation for preparation of a salt may result in increased or decreased solubility of that salt.

[00262] Every formulation or combination of components described or exemplified herein can be used to practice the invention, unless otherwise stated.

[00263] Whenever a range is given in the specification, for example, a temperature range, a time range, a range of one or more physical dimensions (e.g., length, width, thickness, etc.) or a composition or concentration range, all intermediate ranges and

subranges, as well as all individual values included in the ranges given are intended to be included in the disclosure. It will be understood that any subranges or individual values in a range or subrange that are included in the description herein can be excluded from the claims herein.

[00264] All patents and publications mentioned in the specification are indicative of the levels of skill of those skilled in the art to which the invention pertains.

References cited herein are incorporated by reference here in their entirety to indicate the state of the art as of their publication or filing date and it is intended that this information can be employed herein, if needed, to exclude specific embodiments that are in the prior art. For example, when compositions of matter are claimed, it should be understood that compounds known and available in the art prior to Applicant's invention, including compounds for which an enabling disclosure is provided in the references cited herein, are not intended to be included in the composition of matter claims herein.

[00265] Unless defined otherwise, all technical and scientific terms used herein have the same meanings as commonly understood by one of ordinary skill in the art to which this invention belongs. Although any methods and materials similar or equivalent to those described herein can be used in the practice or testing of the present invention, the preferred methods and materials are now described. Nothing herein is to be construed as an admission that the invention is not entitled to antedate such disclosure by virtue of prior invention.

[00266] As used herein, "comprising" is synonymous with "including," "containing," or "characterized by," and is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. As used herein, "consisting of" excludes any element, step, or ingredient not specified in the claim element. As used herein, "consisting essentially of" does not exclude materials or steps that do not materially affect the basic and novel characteristics of the claim. In each instance herein any of the terms "comprising", "consisting essentially of" and "consisting of" may be replaced with either of the other two terms. The invention illustratively described herein suitably may be practiced in the absence of any element or elements, limitation or limitations which is not specifically disclosed herein.

[00267] It must be noted that as used herein and in the appended claims, the singular forms "a", "an", and "the" include plural reference unless the context clearly dictates otherwise. Thus, for example, reference to "a cell" includes a plurality of such cells and equivalents thereof known to those skilled in the art, and so forth. As well, the terms "a" (or "an"), "one or more" and "at least one" can be used interchangeably herein. It is also to be noted that the terms "comprising", "including", and "having" can be used interchangeably. The expression "of any of claims XX-YY" (wherein XX and YY refer to claim numbers) is intended to provide a multiple dependent claim in the alternative form, and in some embodiments is interchangeable with the expression "as in any one of claims XX-YY."

[00268] One of ordinary skill in the art will appreciate that starting materials, biological materials, reagents, synthetic methods, purification methods, analytical methods, assay methods, and biological methods other than those specifically exemplified can be employed in the practice of the invention without resort to undue experimentation. All art-known functional equivalents, of any such materials and methods are intended to be included in this invention. The terms and expressions which have been employed are used as terms of description and not of limitation, and there is no intention in the use of such terms and expressions of excluding any equivalents of the features shown and described or portions thereof, but it is recognized that various modifications are possible within the scope of the invention claimed. Thus, it should be understood that although the present invention has been specifically disclosed by preferred embodiments and optional features, modification and variation of the concepts herein disclosed may be resorted to by those skilled in the art, and that such modifications and variations are considered to be within the scope of this invention as defined by the appended claims.

We claim:

1. An electronic device comprising:

a substrate; and

an array of light emitting diodes (LEDs) supported by said substrate, said array of LEDs comprising:

a plurality of printable LED elements, wherein each LED element in said array of LEDs has one or more lateral dimensions less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm , and wherein a spacing between adjacent LED elements in said array of LEDs is greater than or equal to at least one lateral dimension of an LED element in said array; and

a plurality of electrical interconnects, wherein each LED element in said array of LEDs is positioned in electrical communication and thermal communication with at least two of said plurality of electrical interconnects, wherein each of said electrical interconnects has lateral dimensions and an average thickness large enough to provide dissipation of heat from said array of LEDs at a rate greater than or equal to 5 $\mu\text{J s}^{-1}$.

2. An electronic device comprising:

a substrate; and

an array of light emitting diodes (LEDs) supported by said substrate, said array of LEDs comprising:

a plurality of printable LED elements, wherein each LED element in said array of LEDs has one or more lateral dimensions less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm , and wherein a spacing between adjacent LED elements in said array of LEDs is greater than or equal to 2 μm ; and

a plurality of electrical interconnects, wherein each LED element in said array of LEDs is positioned in electrical communication with at least two of said plurality of electrical interconnects, wherein each of said electrical interconnects is characterized by lateral dimensions and an average thickness.

3. The electronic device of any of claims 1-2, wherein said lateral dimensions and said average thickness of said electrical interconnects are large enough to provide heat dissipation from each of said LEDs in said array during operation at a rate selected over the range of $5 \mu\text{J s}^{-1}$ to 100 J s^{-1} .
4. The electronic device of any of claims 1-3, wherein said lateral dimensions and said thickness of said electrical interconnects are large enough to provide a maximum temperature of each of said LEDs in said array less than or equal to 373 K for a power consumption equal to or greater than $5 \mu\text{W}$.
5. The electronic device of any of claims 1-4, wherein a net heat capacity of said electrical interconnects is greater than or equal to $7.3 \times 10^{-11} \text{ J/K}$ per LED in said array.
6. The electronic device of any of claims 1-5, wherein each of said electrical interconnects of said array has an average heat capacity equal to or greater than $7.3 \times 10^{-11} \text{ J/K}$.
7. The electronic device of any of claims 1-6, wherein an average thermal conductivity of each of said electrical interconnects is a factor of 0.4 to 50 of an average thermal conductivity of said LED elements.
8. The electronic device of any of claims 1-7, wherein an average thermal conductivity of each of said electrical interconnects is a factor of 0.44 to 1.54 of an average thermal conductivity of said LED elements.
9. The electronic device of any of claims 1-8, wherein said array has a density of said LED elements less than or equal to 100 LEDs mm^{-2} .
10. The electronic device of any of claims 1-9, wherein said array has a density of said LED elements selected over the range of 1 LEDs mm^{-2} to 81 LEDs mm^{-2} .

11. The electronic device of any of claims 1-10, wherein a spacing between adjacent LED elements in said array of LEDs is greater than or equal to 10 μm .
12. The electronic device of any of claims 1-11, wherein said spacing between adjacent LED elements in said array of LEDs is selected over the range of 2 μm to 10 μm .
13. The electronic device of any of claims 1-12, wherein said array has an average spacing between adjacent LED elements selected over the range of 10 μm to 100 μm .
14. The electronic device of any of claims 1-13, wherein each LED element in said array of LEDs has lateral dimensions less than or equal to 500 μm .
15. The electronic device of any of claims 1-14, wherein each of said LED elements in said array has average lateral dimensions selected over the range of 10 μm to 1 mm.
16. The electronic device of any of claims 1-15, wherein said lateral dimensions of each of said LED elements are selected over the range of 10 μm to 500 μm .
17. The electronic device of any of claims 1-16, wherein each of said LED elements in said array has average lateral dimensions selected over the range of 10 μm to 500 μm .
18. The electronic device of any of claims 1-17, wherein said thickness dimension of each of said LED elements is less than or equal to 10 μm .
19. The electronic device of any of claims 1-18, wherein said thickness dimension of each of said LED elements is selected over the range of 500 nm to 50 μm .
20. The electronic device of any of claims 1-19, wherein each of said LED elements in said array has an average thickness dimension selected over the range of 500 nm to 50 μm .
21. The electronic device of any of claims 1-20, wherein said thickness dimension of each of said LED elements is selected over the range of 1 μm to 50 μm .

22. The electronic device of any of claims 1-21, wherein each of said LED elements in said array has an average thickness dimension selected over the range of 1 μm to 50 μm .
23. The electronic device of any of claims 1-22, wherein each of said electrical interconnects has an average thickness greater than or equal to 10 nm.
24. The electronic device of any of claims 1-23, wherein each of said electrical interconnects has an average thickness selected over the range of 10 nm to 100 μm .
25. The electronic device of any of claims 1-24, wherein each of said electrical interconnects has a thickness greater than or equal to 10 nm.
26. The electronic device of any of claims 1-25, wherein each of said electrical interconnects has an average thickness selected over the range of 10 nm to 1.5 μm .
27. The electronic device of any of claims 1-26, wherein each of said electrical interconnects has lateral dimensions selected over the range of 10 μm to 10 cm.
28. The electronic device of any of claims 1-27, wherein each of said electrical interconnects has lateral dimensions selected over the range of 10 μm to 100 mm.
29. The electronic device of any of claims 1-28, wherein each LED element comprises a vertical type LED.
30. The electronic device of any of claims 1-29, wherein said LED array is assembled on said substrate by dry transfer contact printing.
31. The electronic device of any of claims 1-30, wherein each LED element is encapsulated by a polymer encapsulating layer having a thickness selected over the range of 10 μm to 10 mm.
32. The electronic device of any of claims 1-31, wherein a plurality of said LED elements is electrically connected in a series configuration.

33. The electronic device of any of claims 1-32, wherein a plurality of said LED elements is electrically connected in a parallel configuration.
34. The electronic device of any of claims 1-33, wherein a plurality of said LED elements are each independently electrically addressable.
35. The electronic device of any of claims 1-34, wherein each LED element independently comprises an inorganic semiconductor.
36. The electronic device of any of claims 1-35, wherein each LED element independently comprises a single crystalline inorganic semiconductor.
37. The electronic device of any of claims 1-36, wherein each LED element independently comprises a material selected from the group consisting of: GaN, p-type GaN, n-type GaN, InGaN, AlGaN and any combination of these.
38. The electronic device of any of claims 1-37, wherein each LED element independently comprises a material selected from the group consisting of: a semiconductor, Si, Ga, Al, N, As, P, In and any combination of these.
39. The electronic device of any of claims 1-38, wherein each LED element independently comprises a material selected from the group consisting of: GaN, GaP, AlN, GaAs, InAlP, AlGaAs, AlGaN, InGaP, InGaN, AlGaInP, and any combination of these.
40. The electronic device of any of claims 1-39, wherein said LED array consumes a power selected over the range of 5 μ W to 100 W.
41. The electronic device of any of claims 1-40, wherein said LED array has a luminous efficacy greater than or equal to 0.1 lm/W.
42. The electronic device of any of claims 1-41, wherein said LED array has a luminous efficacy selected over the range of 0.1 lm/W to 250 lm/W.
43. The electronic device of any of claims 1-42, wherein said lateral dimensions of each LED element are selected over the range of 10 μ m to 500 μ m.

44. The electronic device of any of claims 1-43, wherein said thickness of each LED element is selected over the range of 30 nm to 500 nm.
45. The electronic device of any of claims 1-44, wherein each of said electrical interconnects has a thickness selected over the range of 300 nm to 5 μ m.
46. The electronic device of any of claims 1-45, wherein said plurality of electrical interconnects provides a current path to and from one or more LED elements.
47. The electronic device of any of claims 1-46, wherein said plurality of electrical interconnects provides a path for flow of heat generated by one or more of said LED elements of said array.
48. The electronic device of any of claims 1-47, wherein said plurality of electrical interconnects functions as a heat sink for heat generated by one or more LED elements.
49. The electronic device of any of claims 1-48, wherein said plurality of electrical interconnects provides electrical interconnects between individual LED elements of said array.
50. The electronic device of any of claims 1-49, wherein each of said electrical interconnects comprises a thin film structure.
51. The electronic device of any of claims 1-50, wherein each of said electrical interconnects comprises a unitary structure.
52. The electronic device of any of claims 1-51, wherein each of said electrical interconnects comprises a metal.
53. The electronic device of any of claims 1-52, wherein each of said electrical interconnects independently comprises a metal selected from the group consisting of aluminum, copper, gold, platinum, nickel, titanium or any combination of these.
54. The electronic device of any of claims 1-53, wherein said substrate is a flexible substrate.

55. The electronic device of any of claims 1-54, wherein said substrate is an optically transparent substrate.
56. The electronic device of any of claims 1-55, wherein said substrate is transparent to ultraviolet electromagnetic radiation, visible electromagnetic radiation or both ultraviolet electromagnetic radiation and visible electromagnetic radiation.
57. The electronic device of any of claims 1-56, wherein said substrate comprises a material selected from the group consisting of: a flexible material, a stretchable material, an inorganic material, a ceramic, a polymer, an elastomer, an inorganic polymer, an organic polymer, a plastic, a biopolymer, a thermoset polymer, a rubber, fabric, paper, silk, a hydrogel and any combination of these.
58. The electronic device of any of claims 1-57, further comprising an encapsulating layer provided on at least a portion of said array, wherein said encapsulating layer has a thickness selected over the range of 1 μm to 10 mm.
59. The electronic device of any of claims 1-58, further comprising a phosphor patterned polymer layer in optical contact with said array of printable LED elements, said phosphor patterned polymer layer having a plurality of phosphor-containing reservoirs aligned with one or more of said printable LED elements such that electromagnetic radiation from said printable LED elements is transmitted to said phosphor-containing reservoirs.
60. The electronic device of any of claims 1-59, further comprising a thin film optical diffuser in optical contact with said array of printable LED elements such that electromagnetic radiation from said printable LED elements or said phosphor-containing reservoirs is transmitted through said thin film optical diffuser.
61. A method of making an electronic device, the method comprising the steps of:
- providing a substrate;

assembling a plurality of printable LED elements onto said substrate by transfer printing said printable LED elements onto a receiving surface of said substrate, thereby making an array of LED elements, wherein each LED element has one or more lateral dimensions less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm and wherein a spacing between adjacent LED elements in said array of LED elements is greater than or equal to at least one lateral dimension of an LED element in said array of LED elements; and

providing a plurality of electrical interconnects to said array of LED elements, wherein each LED element in said array of LED elements is positioned in electrical communication and thermal communication with two or more of said plurality of electrical interconnects, wherein each of said electrical interconnects has lateral dimensions and an average thickness large enough to provide dissipation of heat from said array of LED elements at a rate greater than or equal to 5 $\mu\text{J s}^{-1}$, thereby making said electronic device.

62. A method of making an electronic device, the method comprising the steps of:

providing a substrate;

assembling a plurality of printable LED elements onto said substrate by transfer printing said printable LED elements onto a receiving surface of said substrate, thereby making an array of LED elements, wherein each LED element has one or more lateral dimensions less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm and wherein a spacing between adjacent LED elements in said array of LED elements is greater than or equal to 2 μm ; and

providing a plurality of electrical interconnects to said array of LED elements, wherein each LED element in said array of LED elements is positioned in electrical communication with two or more of said plurality of electrical interconnects, wherein each of said electrical interconnects is characterized by lateral dimensions and an average thickness, thereby making said electronic device.

63. The method of any of claims 61 - 62, wherein the step of assembling a plurality of printable LED elements onto said substrate is achieved using dry contact transfer printing.
64. The method of any of claims 61 – 63 further comprising providing a polymer encapsulating layer that completely or partially encapsulates said printable LED elements, said electrical interconnects or both.
65. The method of any of claims 61 - 64, further comprising the steps of:
- providing a phosphor array layer comprising an array of phosphor elements at least partially encapsulated in a polymer mold; and
 - providing said phosphor array layer on said electronic device, wherein at least a portion of said phosphor elements are positioned in optical communication with at least a portion of said LED elements such that electromagnetic radiation from said printable LED elements is transmitted to said phosphor elements.
66. The method of claim 65, wherein said phosphor elements have lateral dimensions less than or equal to 1000 μm and a thickness dimension selected over the range of 50 μm to 250 μm .
67. The method of claim 65, wherein said method further comprises:
- a. providing a spacer layer positioned between said phosphor array layer and said plurality of electrical interconnects and said array of LED elements; or
 - b. providing a thin film optical diffuser in optical contact with said array of printable LED elements such that electromagnetic radiation from said printable LED elements or said phosphor elements is transmitted through said thin film optical diffuser
68. The method of claim 65, wherein said phosphor array layer is laminated on top of said electronic device.
69. The method of any of claims 61 - 68, further comprising the steps of:

providing a photosensitive prepolymer layer over said array of LED elements, thereby encapsulating said array of LED elements;

exposing portions of said photosensitive prepolymer layer to electromagnetic radiation, wherein said electromagnetic radiation passes through said substrate and portions of said array of LED elements, thereby forming developed portions and undeveloped portions of said photosensitive prepolymer layer; and

removing said undeveloped portions of said photosensitive prepolymer layer, thereby exposing portions of each LED element in said array of LED elements.

70. The method of claim 69, wherein exposed portions of each LED element are electrical contacts of said LED elements.

71. A method of generating electromagnetic radiation, the method comprising the steps of:

providing an electronic device comprising:

a substrate; and

an array of light emitting diodes (LEDs) supported by said substrate, said array of LEDs comprising:

a plurality of printable LED elements, wherein each LED element in said array of LEDs has one or more lateral dimensions less than or equal to 1000 μm and a thickness dimension less than or equal to 50 μm , and wherein a spacing between adjacent LED elements in said array of LEDs is greater than or equal to at least one lateral dimension of an LED element in said array; and

a plurality of electrical interconnects, wherein each LED element in said array of LEDs is positioned in electrical communication and thermal communication with at least two

of said plurality of electrical interconnects, wherein each of said electrical interconnects has lateral dimensions and an average thickness large enough to provide dissipation of heat from said array of LEDs at a rate greater than or equal to $5 \mu\text{J s}^{-1}$; and

providing a voltage across two or more of said plurality of electrical interconnects, thereby generating electromagnetic radiation from at least a portion of said array of LEDs.

72. A method of generating electromagnetic radiation, the method comprising the steps of:

providing an electronic device comprising:

a substrate; and

an array of light emitting diodes (LEDs) supported by said substrate, said array of LEDs comprising:

a plurality of printable LED elements, wherein each LED element in said array of LEDs has one or more lateral dimensions less than or equal to $1000 \mu\text{m}$ and a thickness dimension less than or equal to $50 \mu\text{m}$, and wherein a spacing between adjacent LED elements in said array of LEDs is greater than or equal to $2 \mu\text{m}$; and

a plurality of electrical interconnects, wherein each LED element in said array of LEDs is positioned in electrical communication with at least two of said plurality of electrical interconnects, wherein each of said electrical interconnects is characterized by lateral dimensions and an average thickness; and

providing a voltage across two or more of said plurality of electrical interconnects, thereby generating electromagnetic radiation from at least a portion of said array of LEDs.

73. The method of any of claims 71 - 72, wherein said lateral dimensions and said average thickness of said electrical interconnects are large enough to provide heat dissipation from each LED in said array sufficient to maintain a maximum steady state temperature of each LED in said array less than or equal to 373 K for a power consumption equal to or greater than 5 μ W.
74. The method of any of claims 71 - 73, wherein said LED array consumes a power equal to or greater than 5 μ W.
75. The method of any of claims 71 - 74, wherein each of said electrical interconnects has an average thickness greater than or equal to 300 nm.
76. The method of any of claims 71 - 75, wherein said step of providing an electronic device comprises assembling said LED array on said substrate using a dry transfer contact printing method.
77. The method of any of claims 71 - 76, wherein said electronic device further comprises a controller positioned in electrical communication with said plurality of electrical interconnects.
78. The method of any of claims 71 - 77, wherein said electromagnetic radiation has a wavelength or wavelength range selected over the range of 350 nm to 800 nm.
79. The method of any of claims 71 - 78, wherein said electronic device further comprises a phosphor-containing island mold having an array of phosphor-containing islands, wherein said array of phosphor-containing islands is positioned in optical communication with said printable LED elements, such that electromagnetic radiation from said printable LED elements is transmitted to said phosphor-containing islands.
80. The method of claim 79, wherein said phosphor-containing island mold is laminated over said array of LEDs and said plurality of electrical interconnects.
81. The method of claim 79, wherein said array of phosphor-containing islands is aligned over said array of LEDs.

82. The method of claim 79, wherein said phosphor-containing islands absorb at least a portion of said electromagnetic radiation generated from said array of LEDs and emit electromagnetic radiation having a wavelength or wavelength range selected over the range of 400 nm to 800 nm.
83. The method of claim 79, wherein said phosphor-containing islands and said LEDs together generate electromagnetic radiation having an x chromaticity coordinate in a CIE 1931 color space selected over the range of 0.25 to 0.4.
84. The method of claim 79, wherein said phosphor-containing islands and said LEDs together generate electromagnetic radiation having a y chromaticity coordinate in a CIE 1931 color space selected over the range of 0.25 to 0.45.
85. The method of any of claims 71 - 84, wherein a plurality of said LED elements is electrically connected in a series configuration.
86. The method of any of claims 71 - 85, wherein a plurality of said LED elements is electrically connected in a parallel configuration.
87. The method of any of claims 71 - 86, wherein a plurality of said LED elements is independently electrically addressable.
88. The method of any of claims 71 - 87, wherein said electronic device further comprises a diffuser positioned in optical communication with said array of LEDs such that electromagnetic radiation from said printable LED elements is transmitted through said diffuser.
89. The method of claim 88, wherein said diffuser is a thin film optical diffuser laminated over at least a portion of said printable LED elements.

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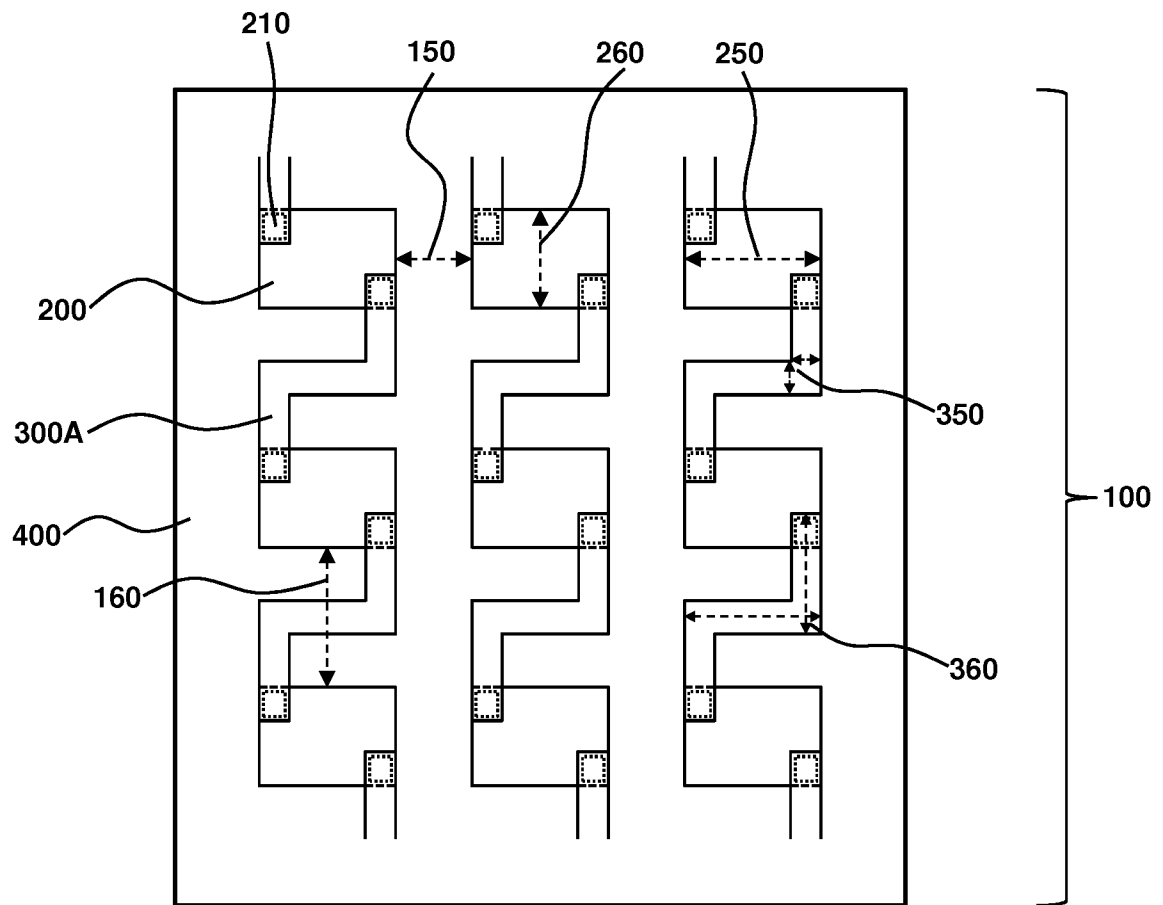


Figure 1A

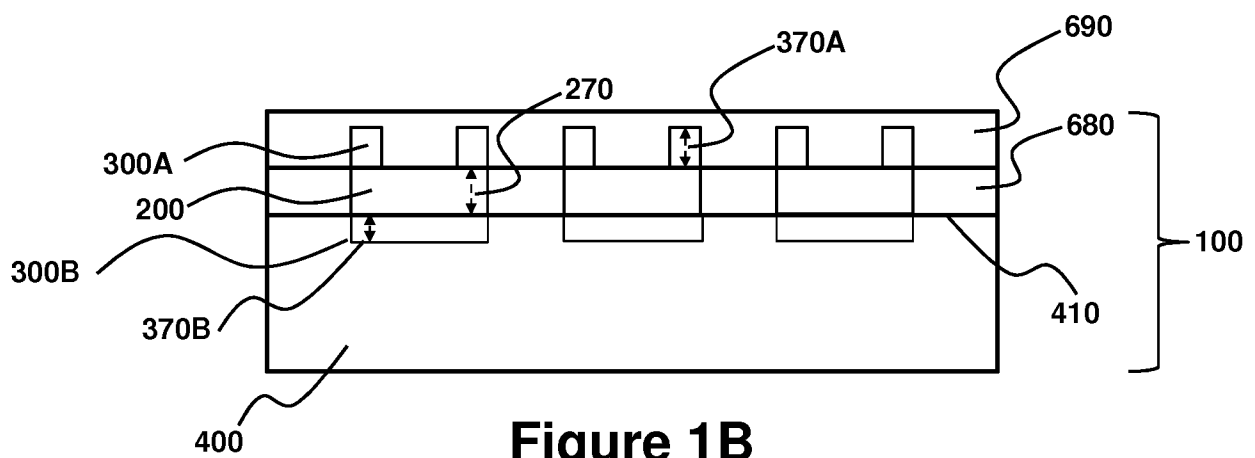


Figure 1B

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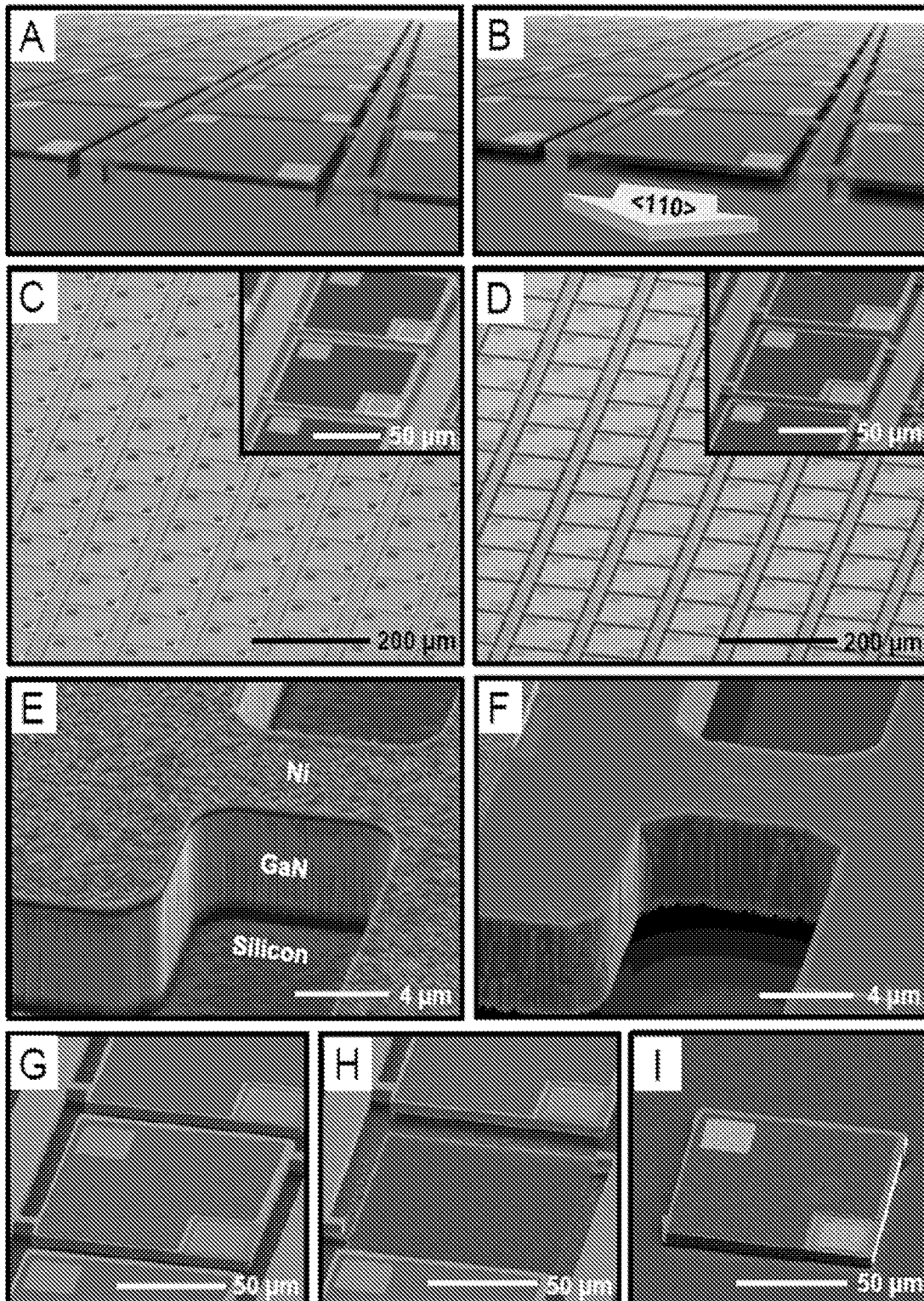


Figure 2

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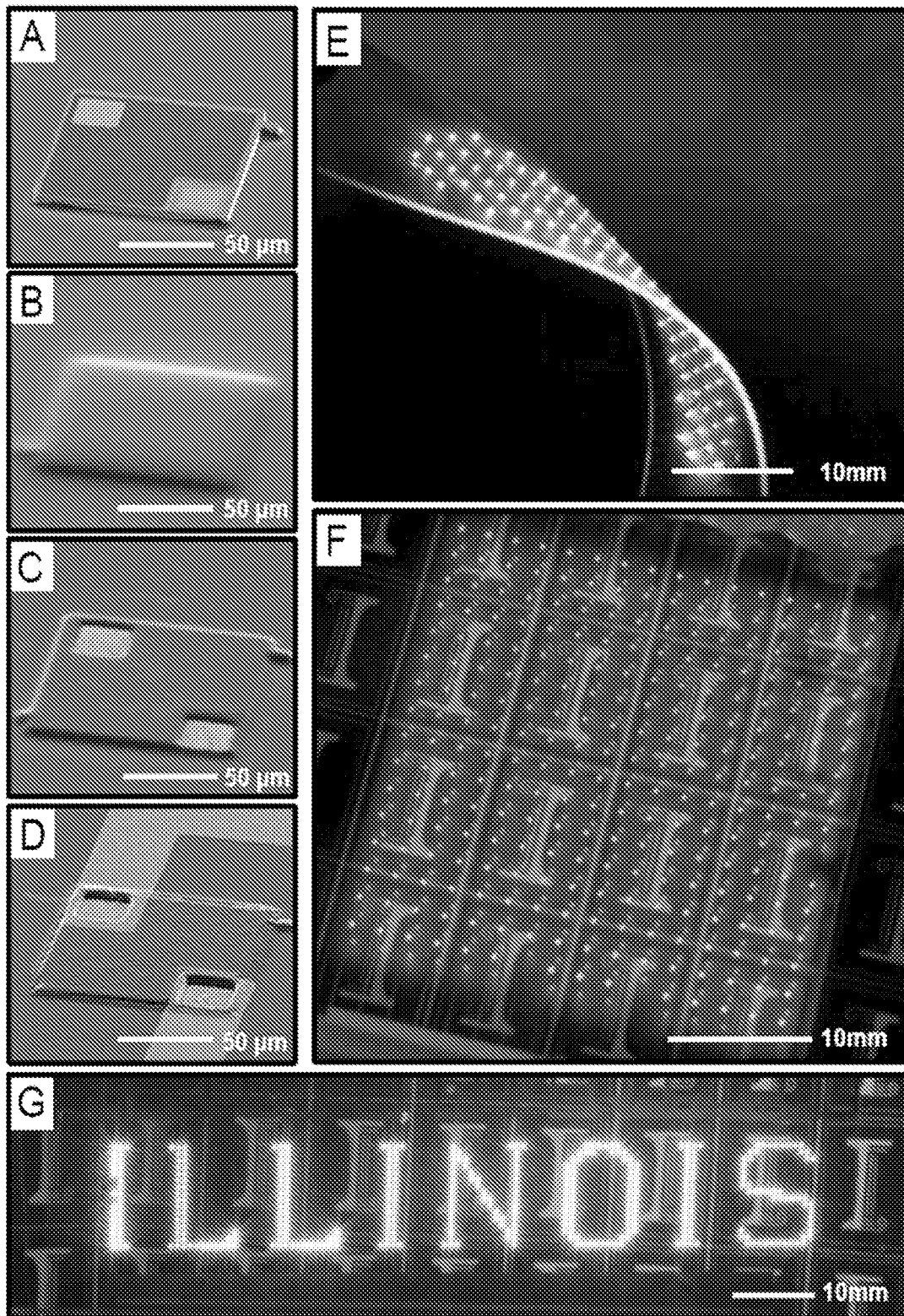
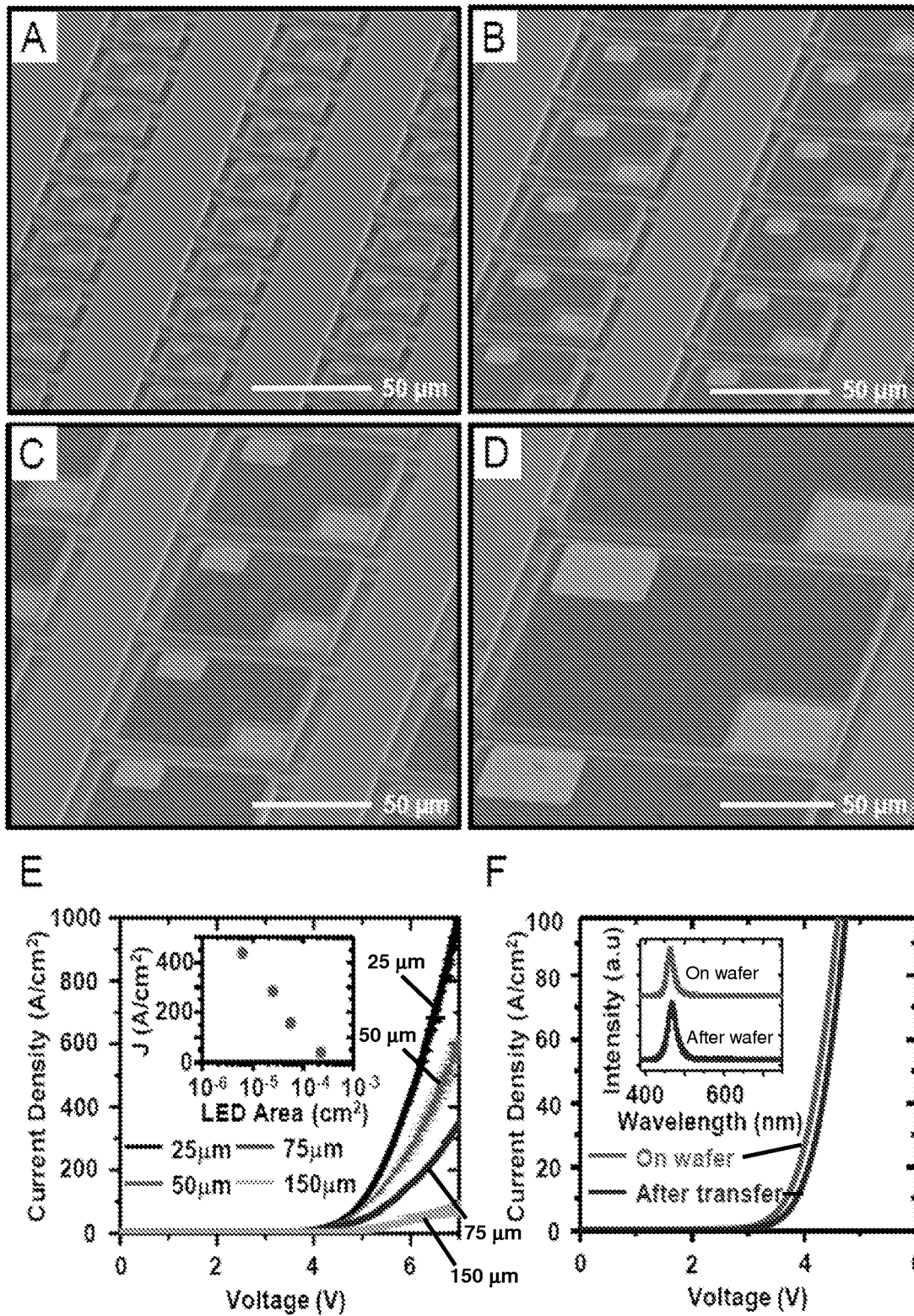


Figure 3

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**Figure 4**

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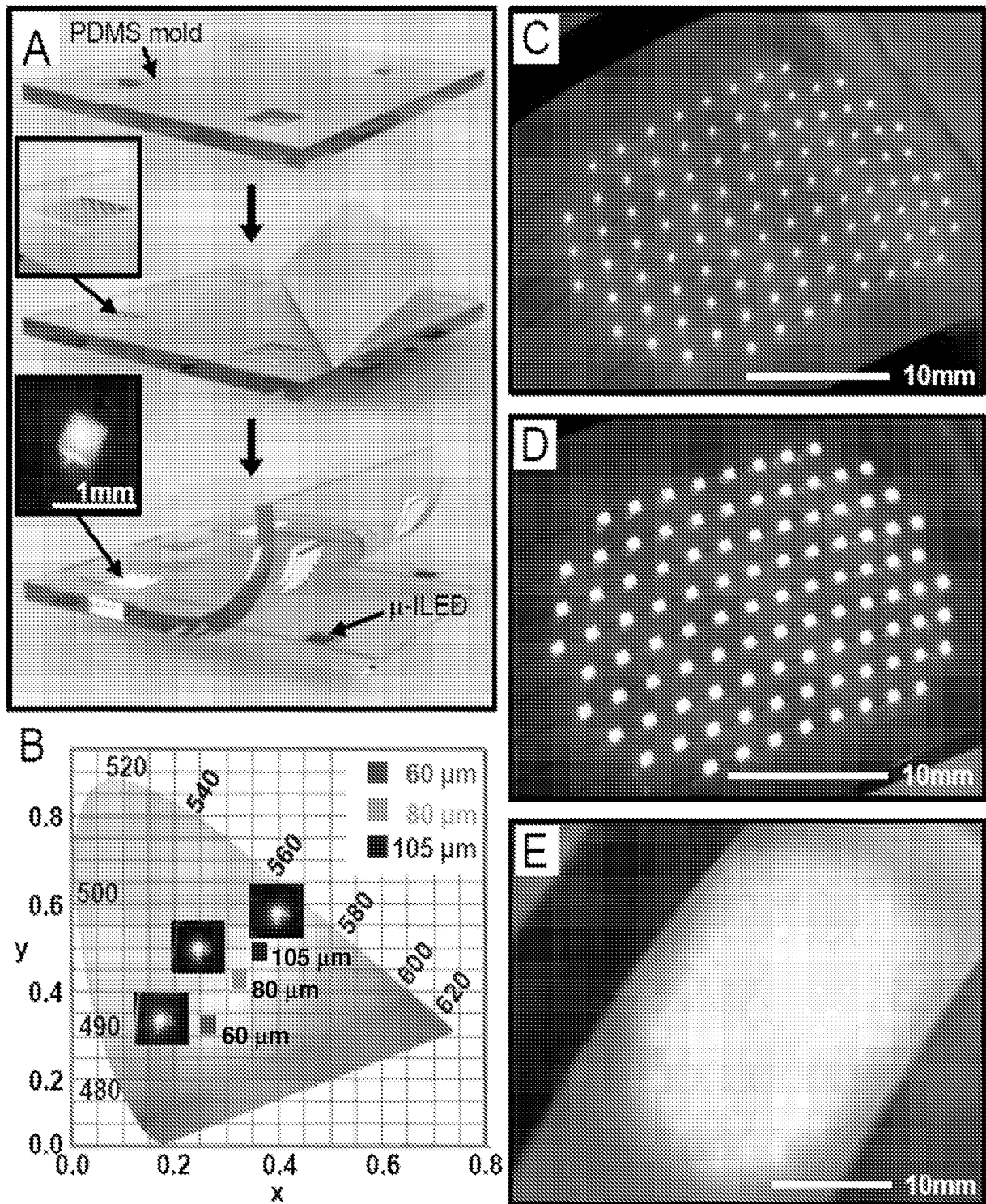


Figure 5

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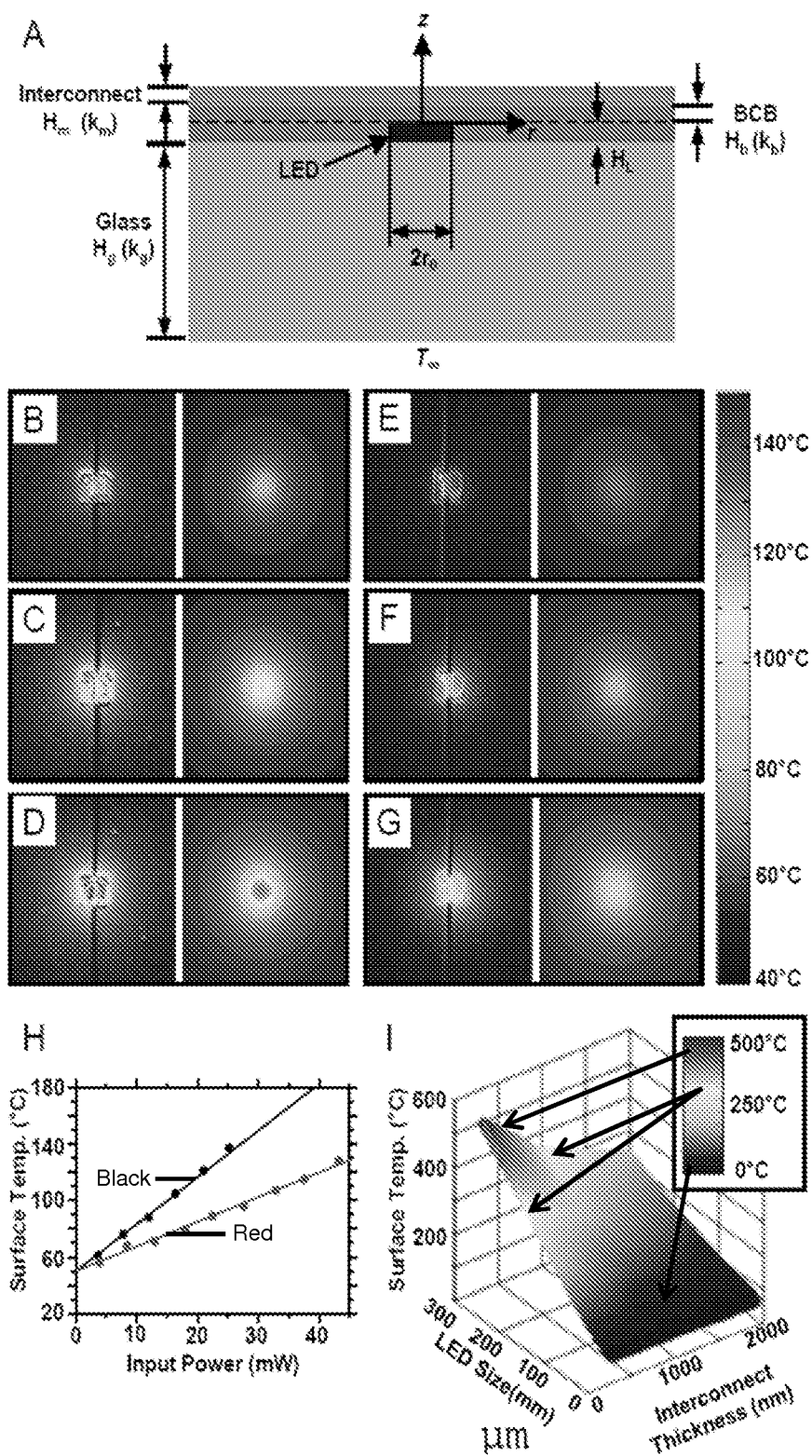


Figure 6

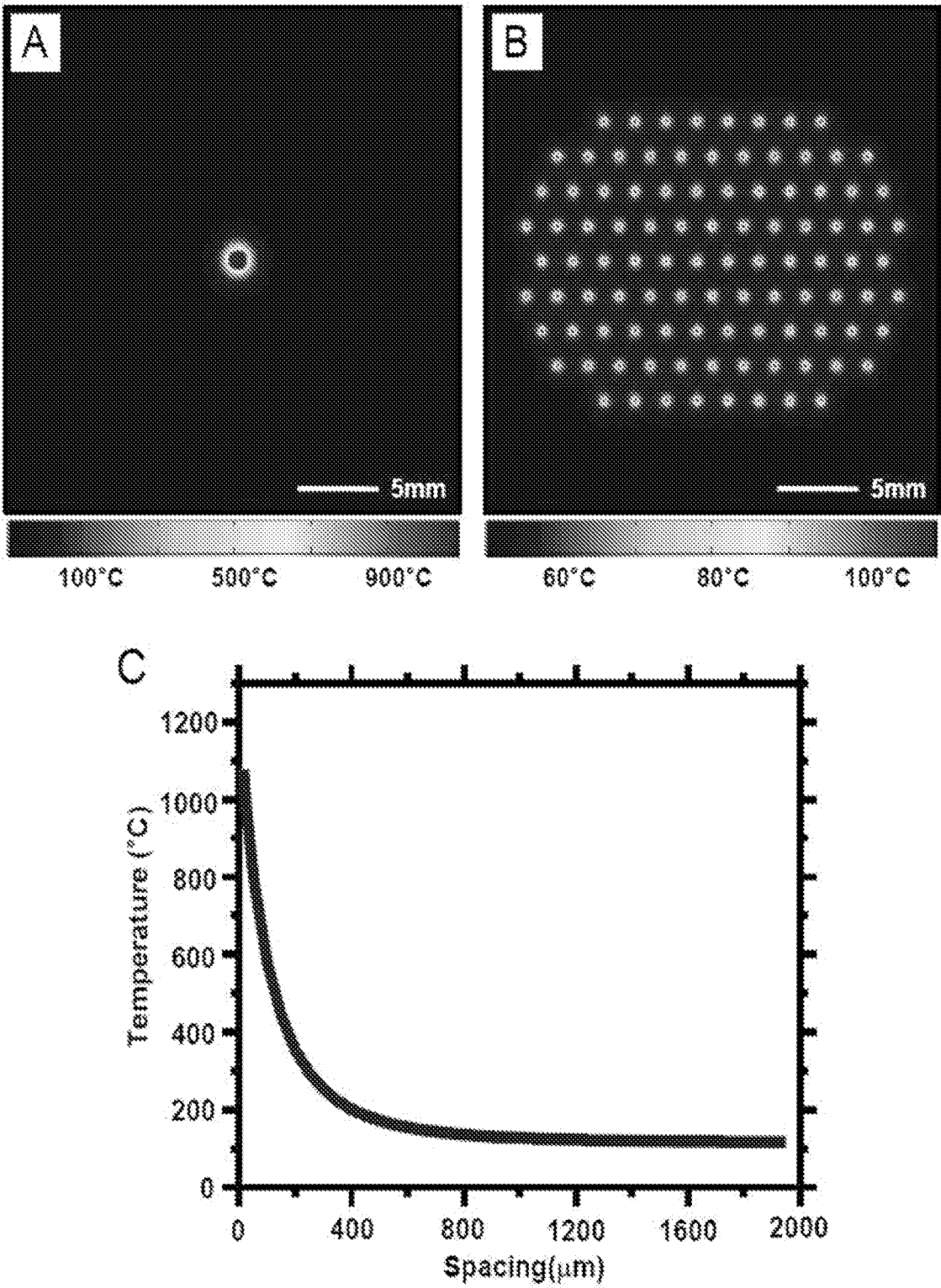
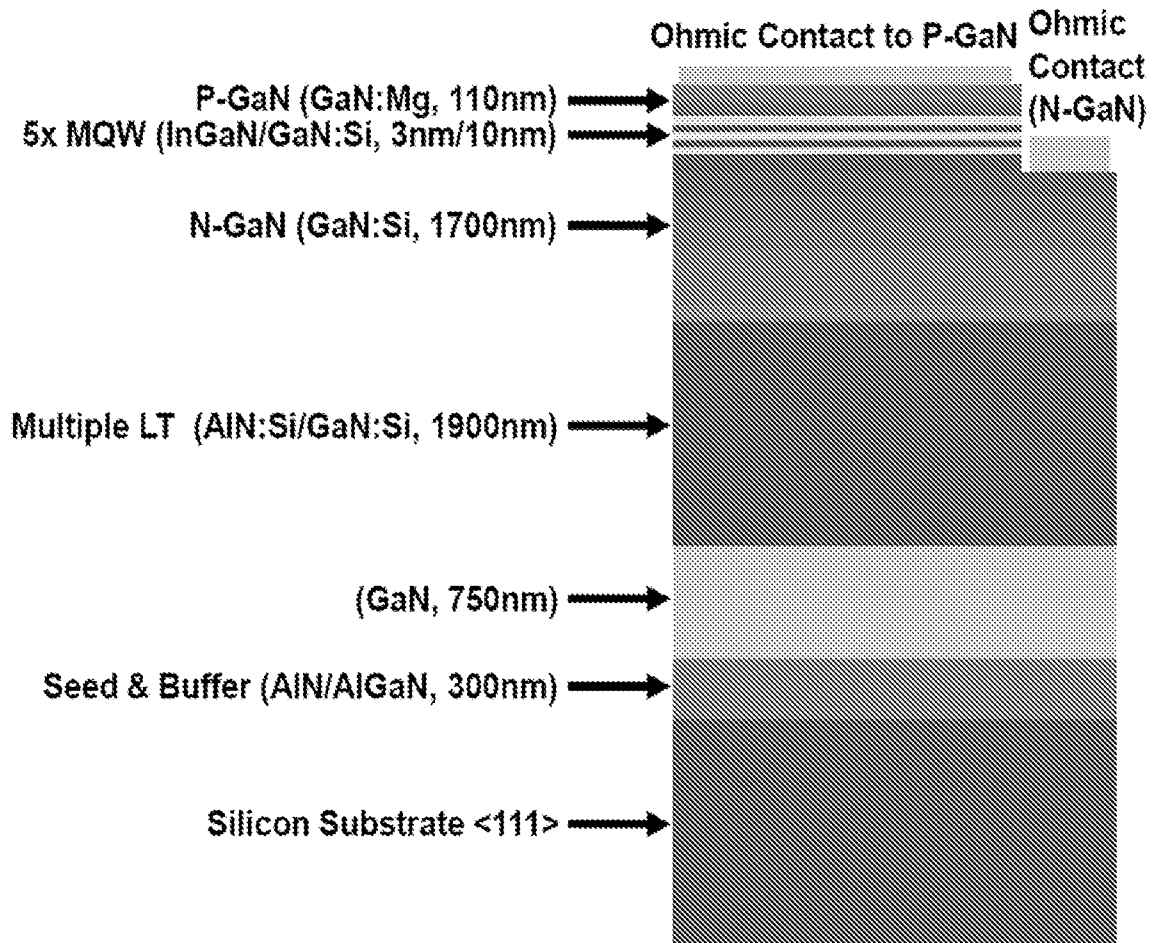


Figure 7

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**Figure 8**

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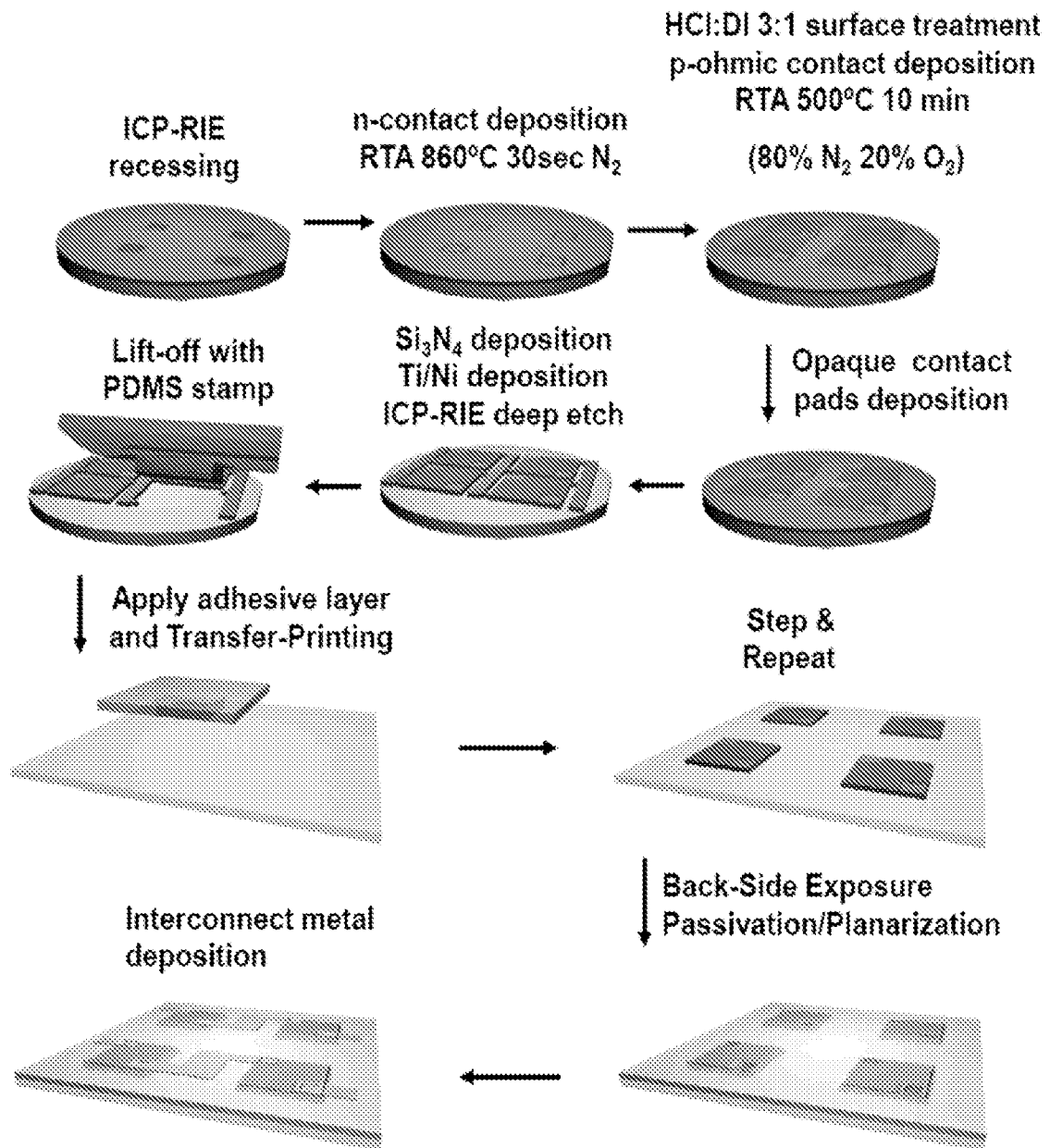


Figure 9

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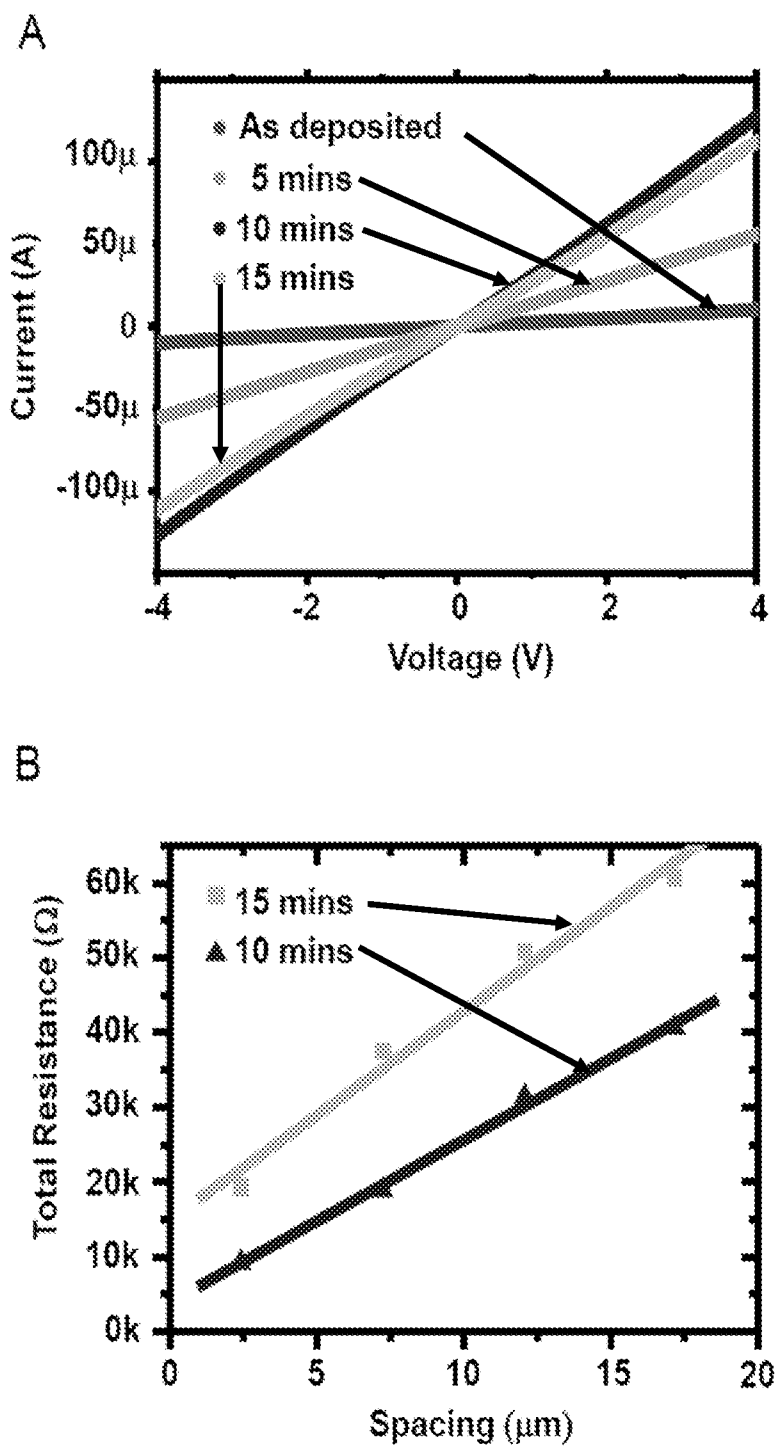


Figure 10

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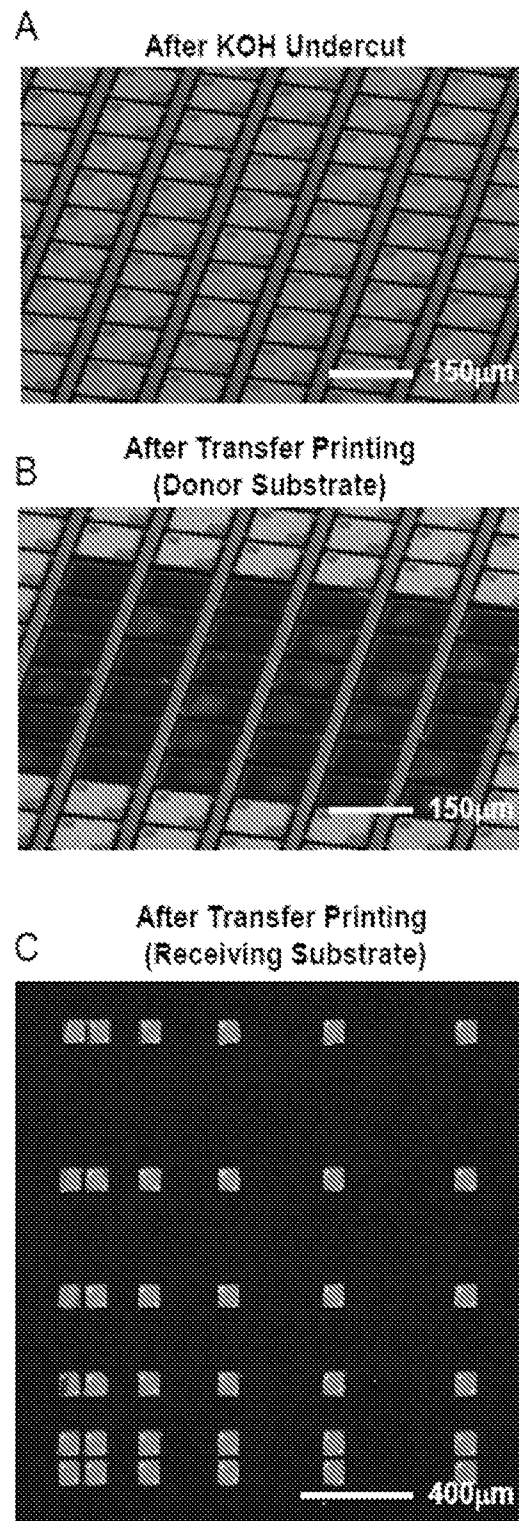


Figure 11

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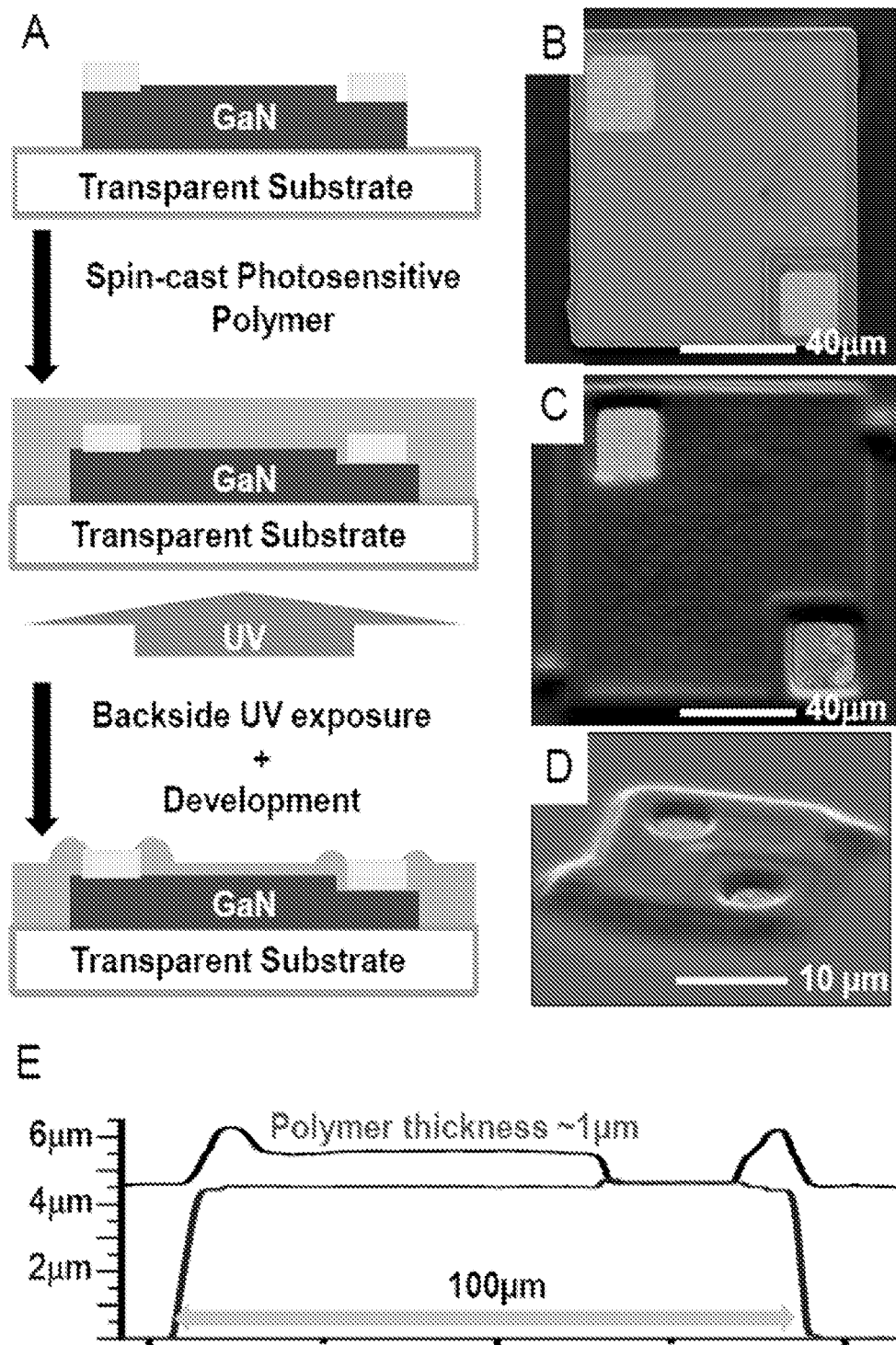


Figure 12

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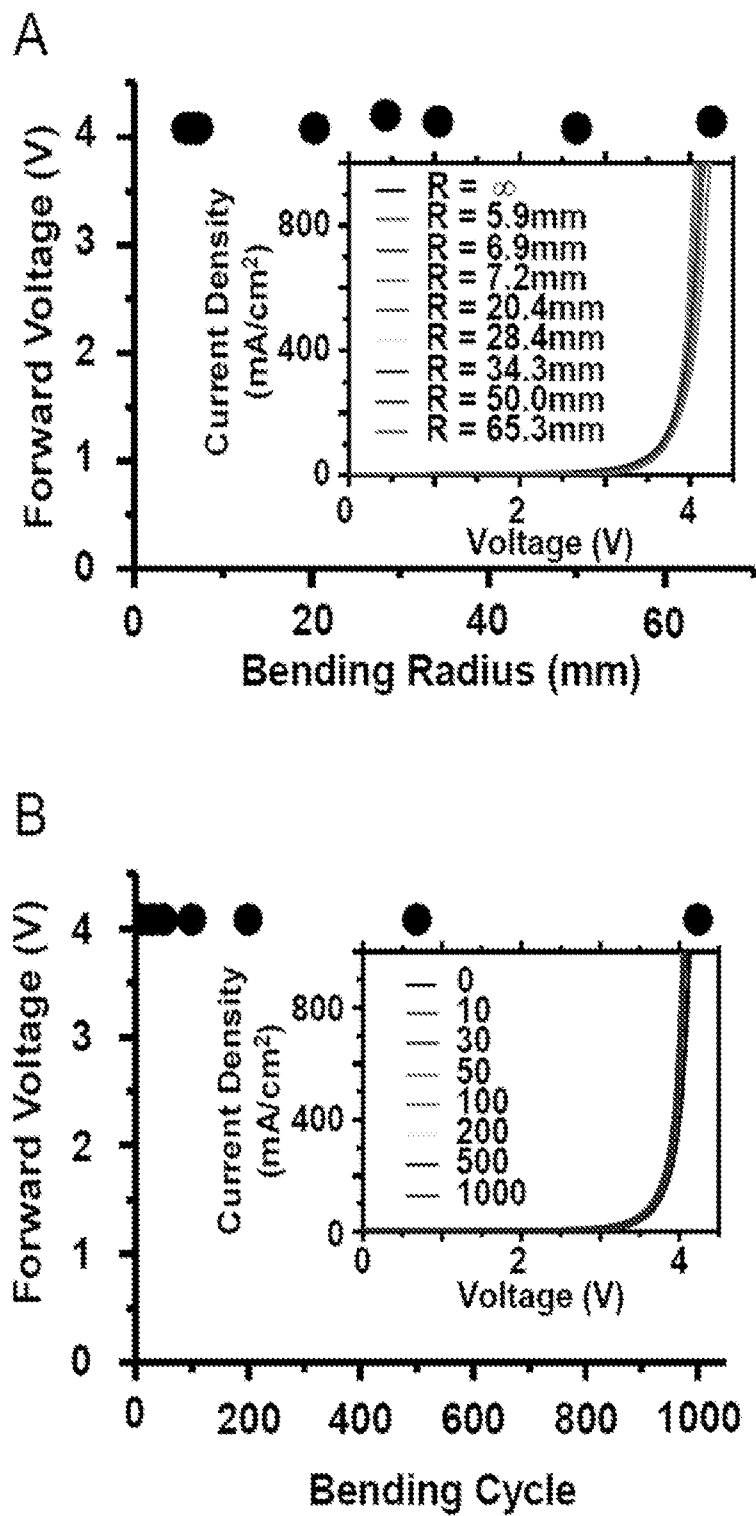
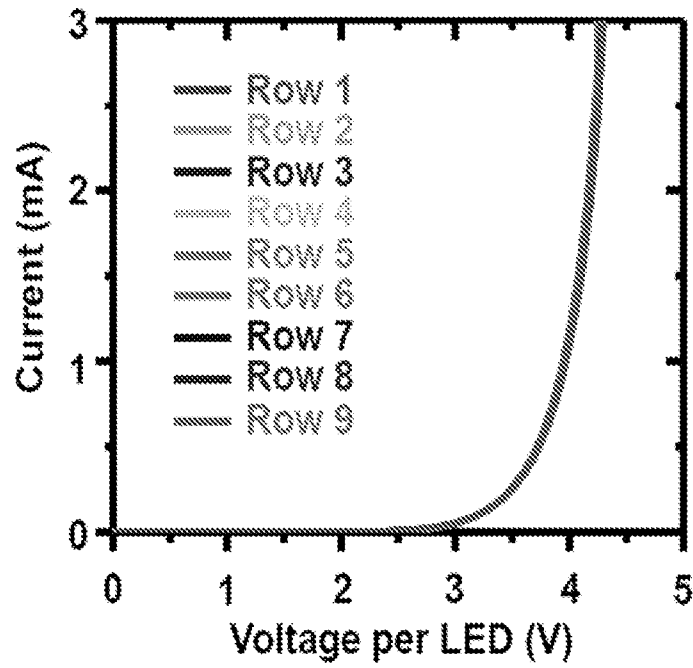


Figure 13

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A



B

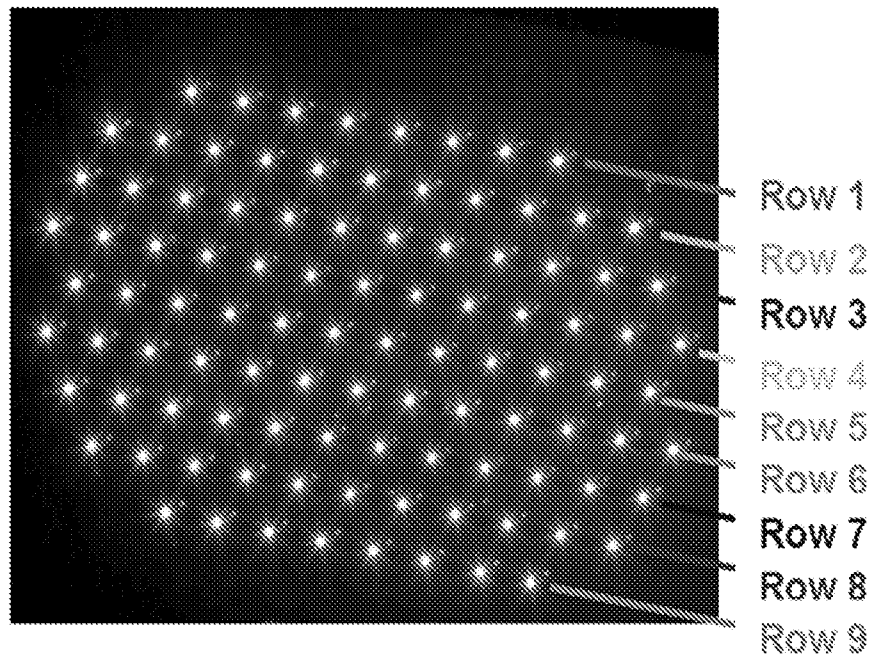


Figure 14

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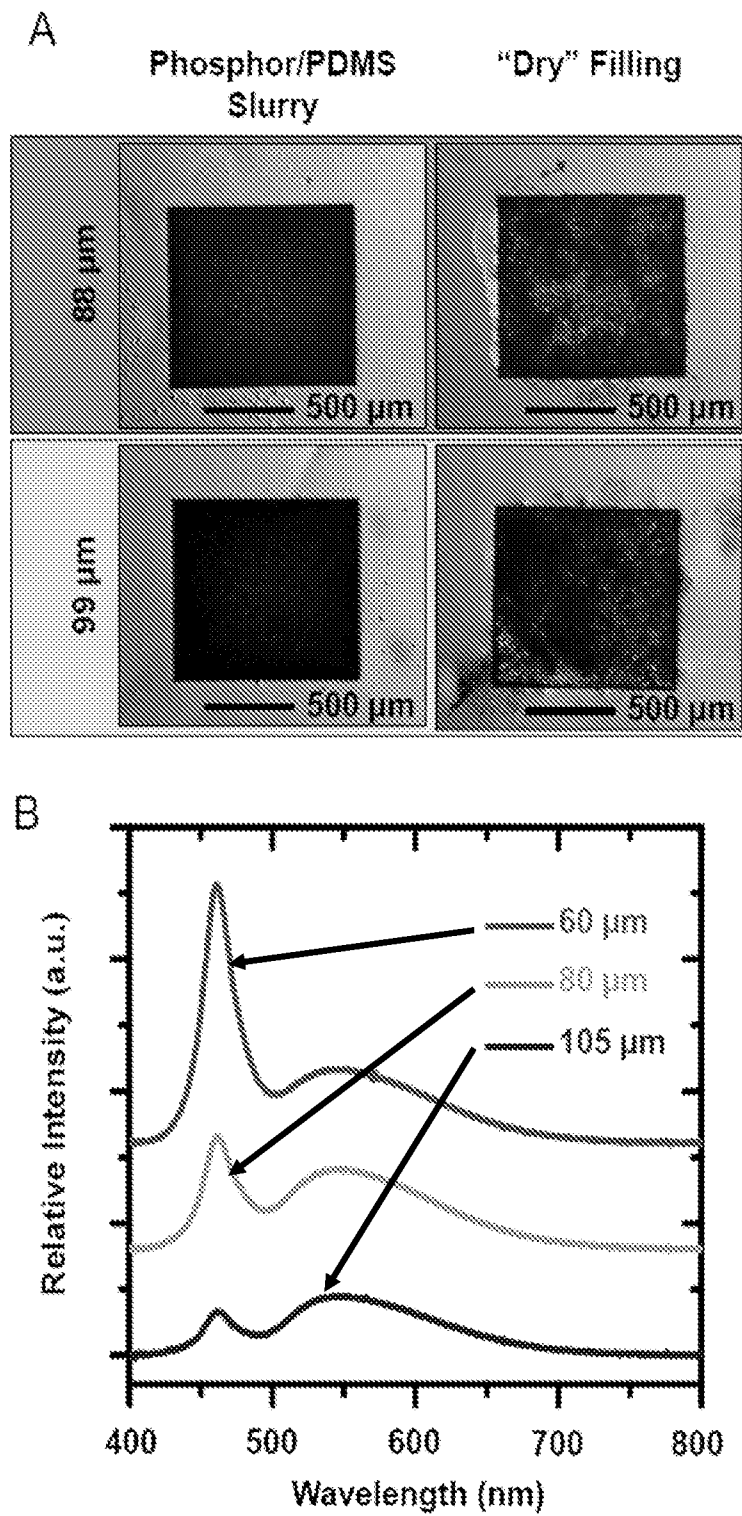


Figure 15

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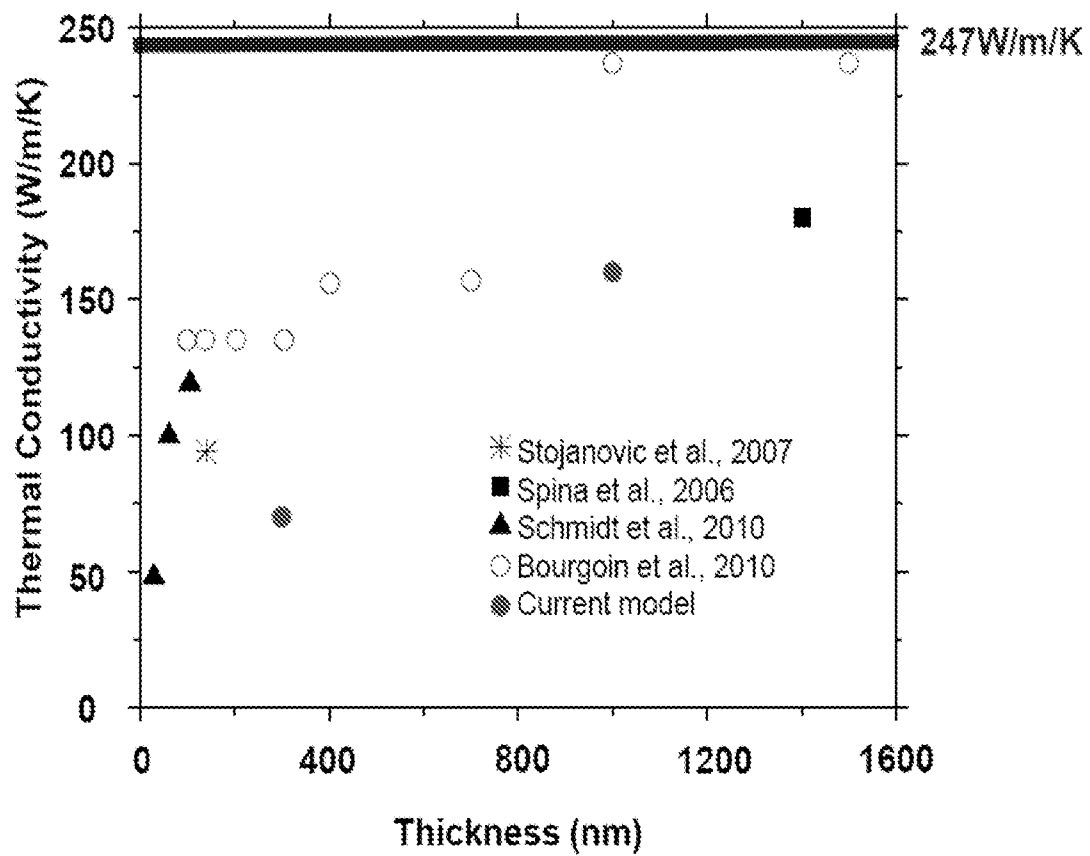


Figure 16

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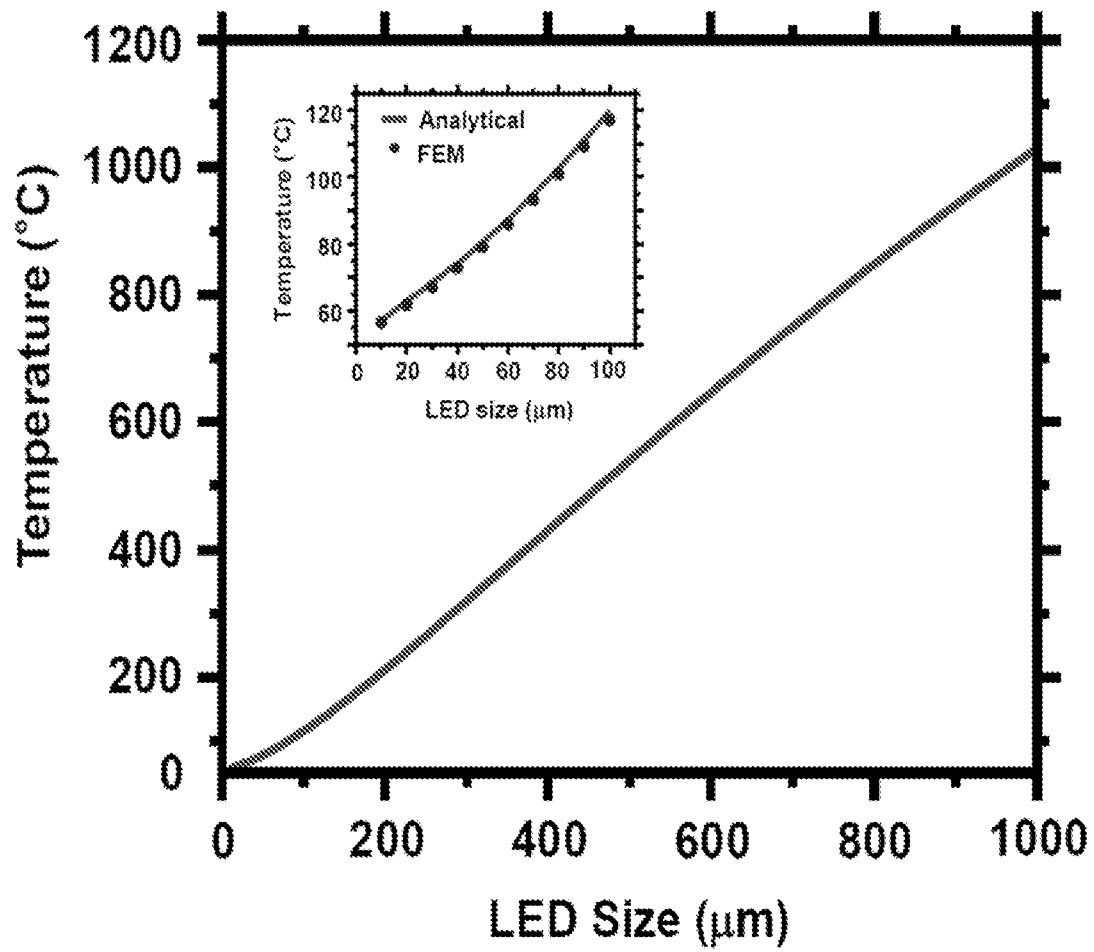


Figure 17

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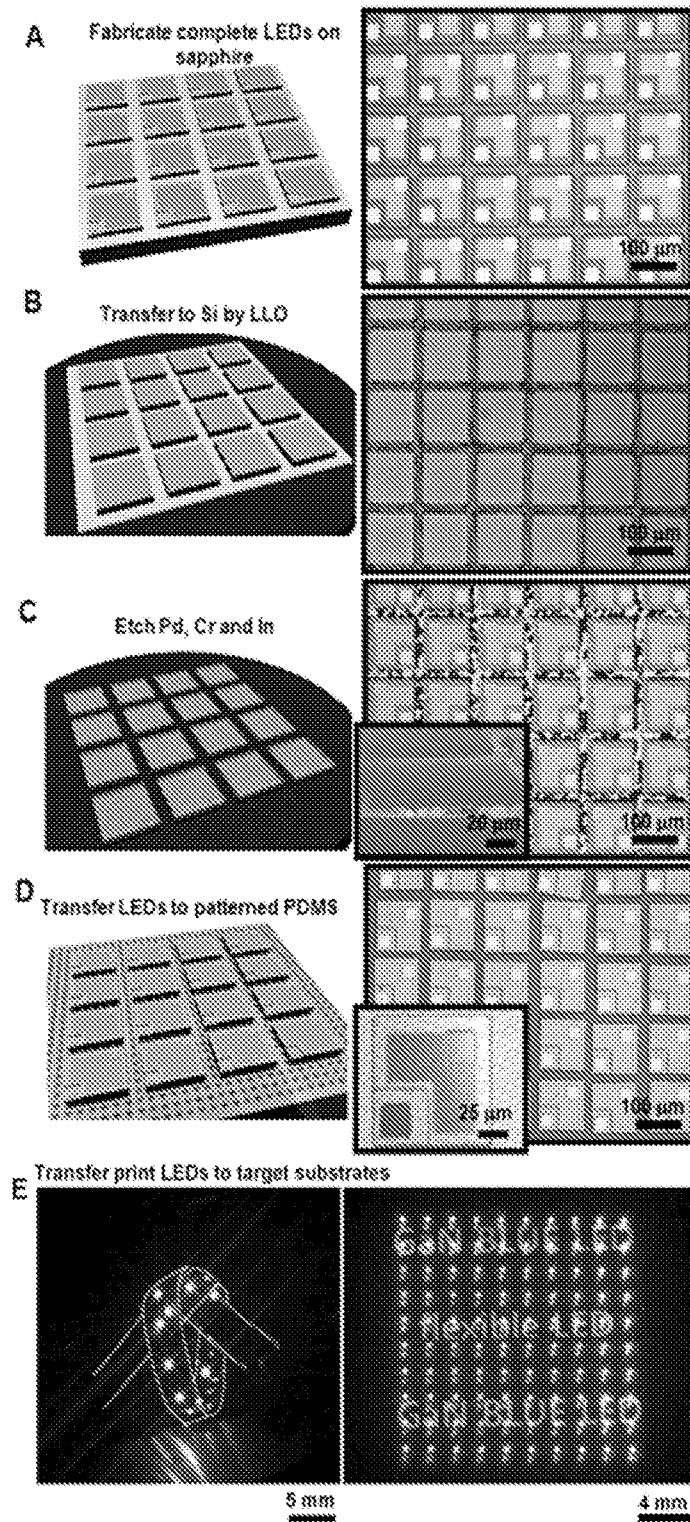


Figure 18

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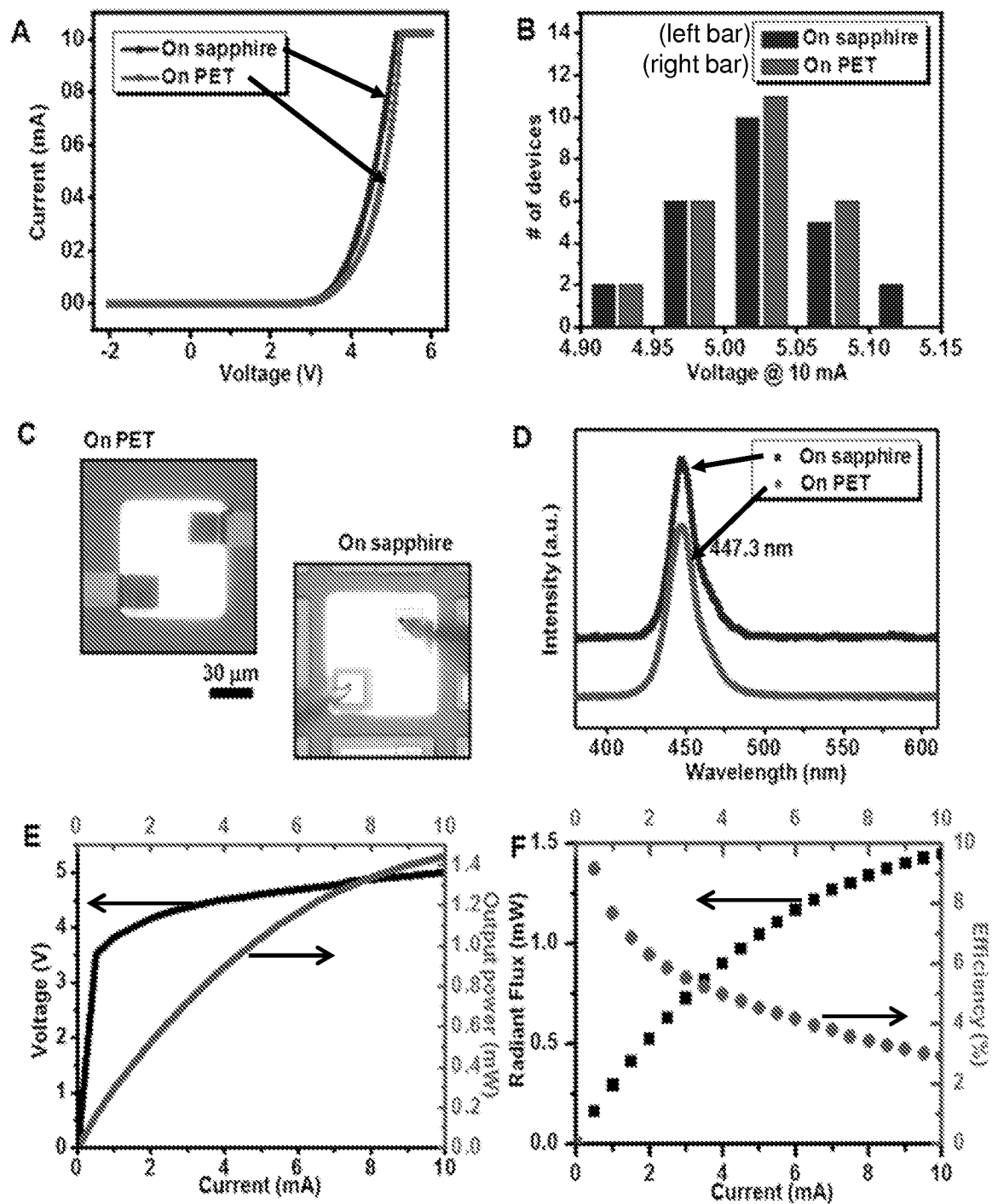


Figure 19

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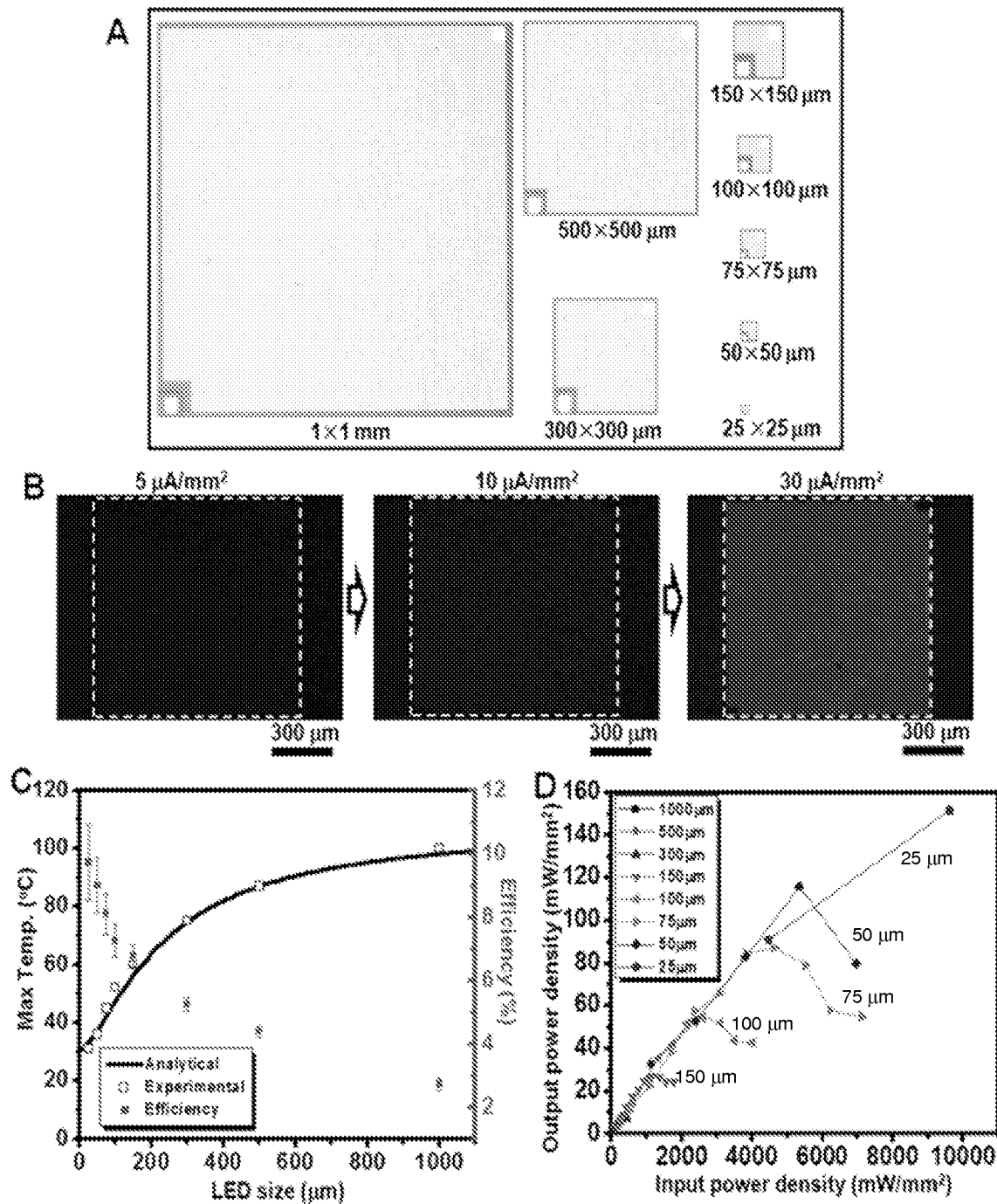


Figure 20

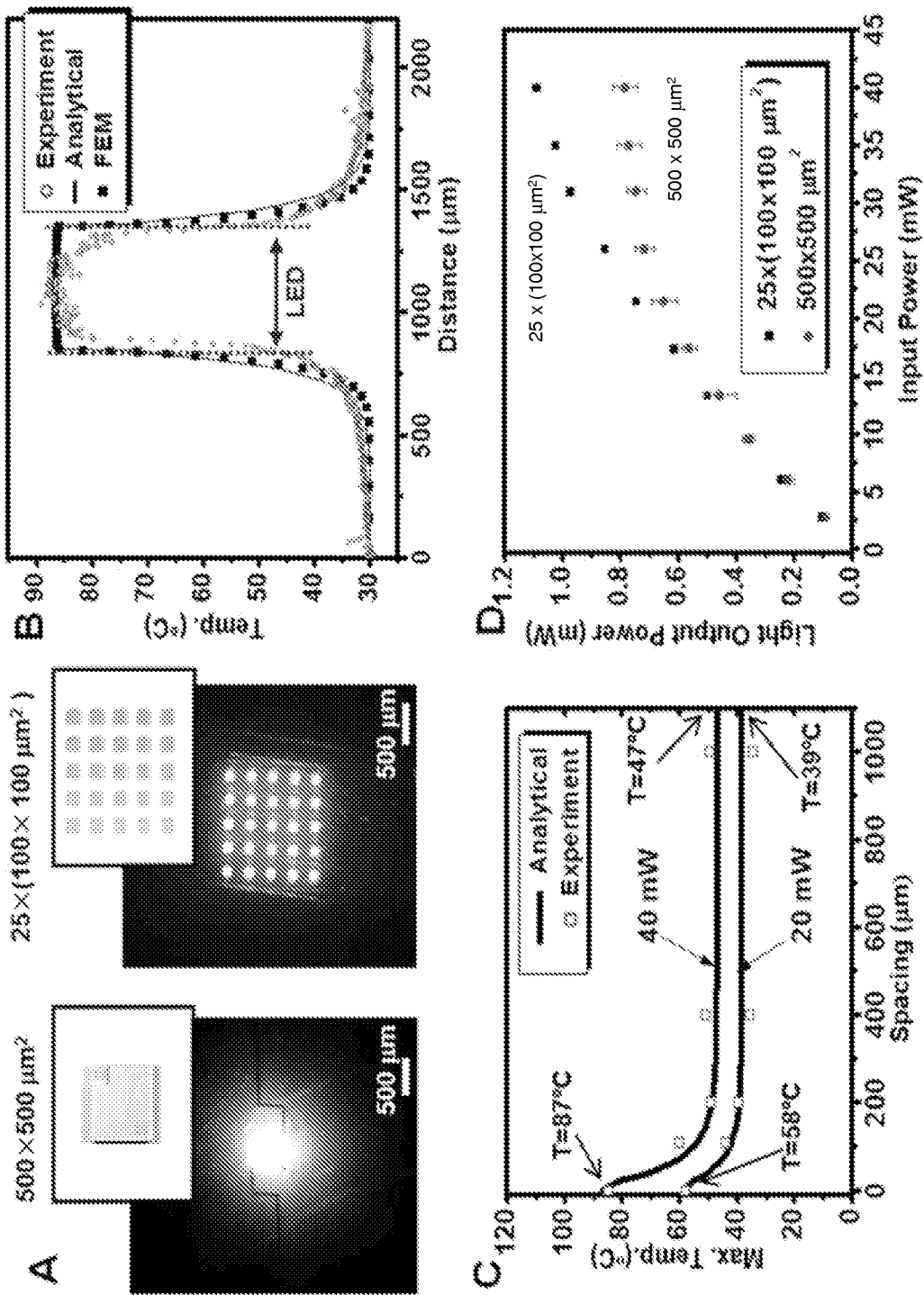


Figure 21

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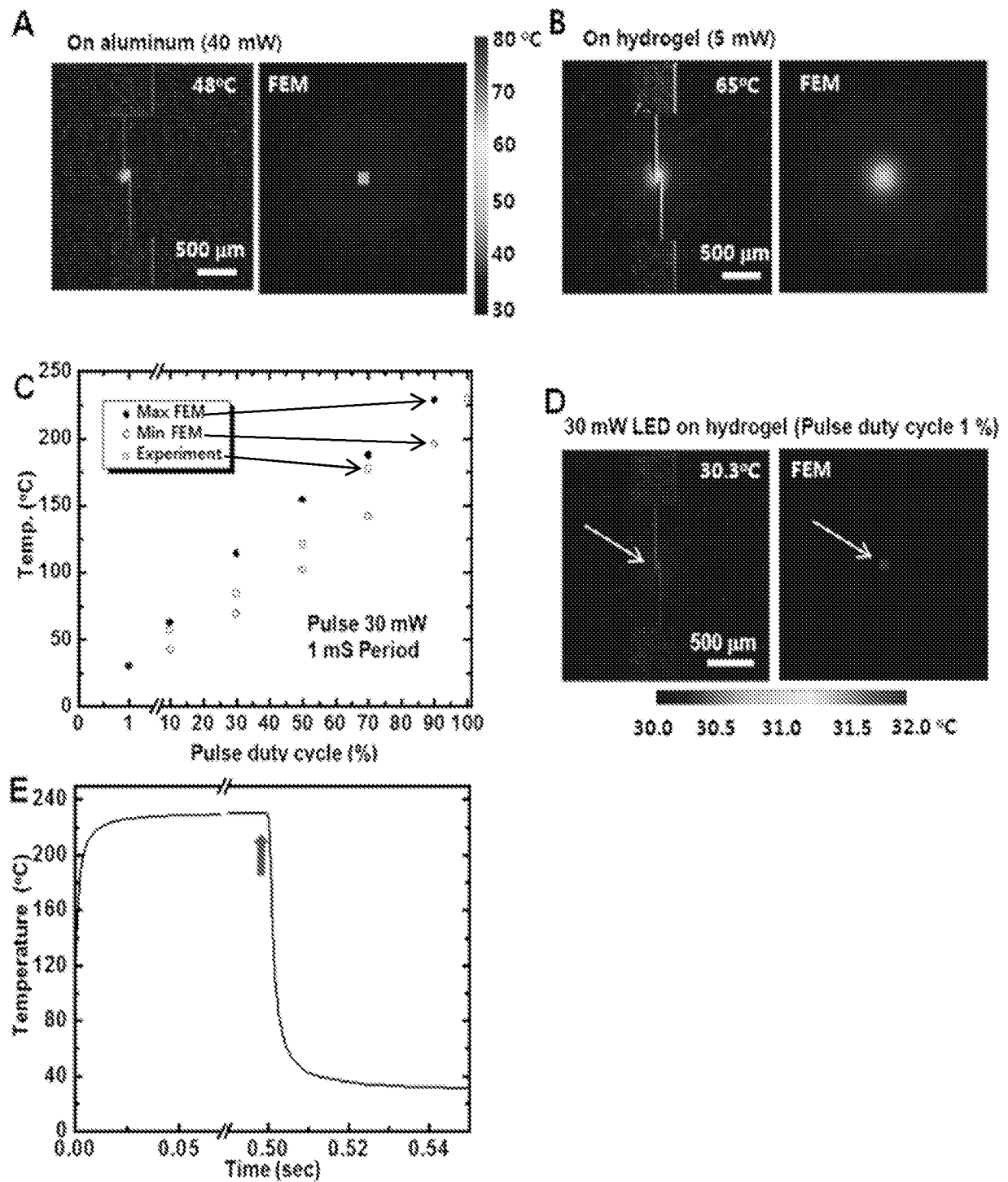


Figure 22

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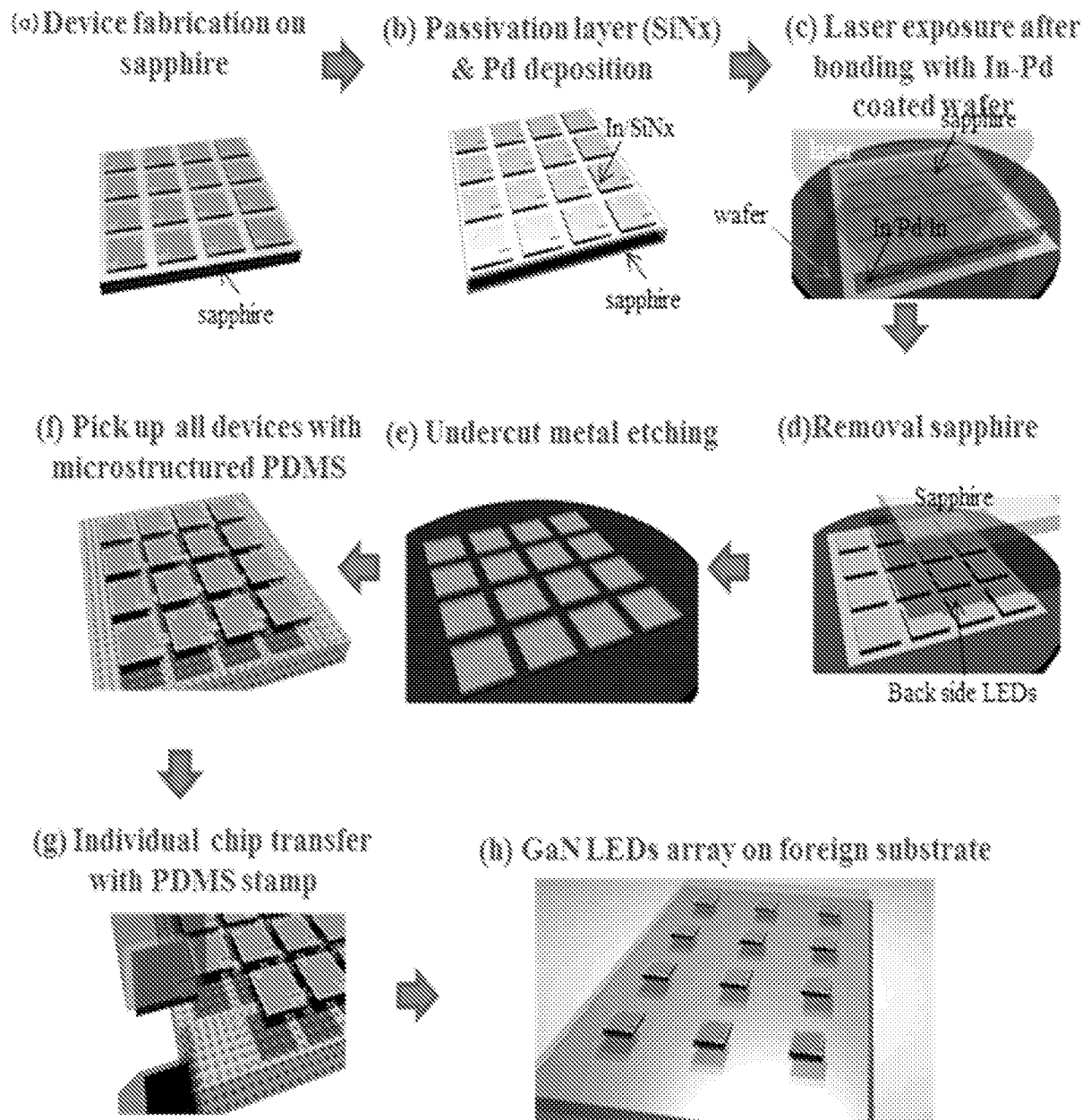


Figure 23

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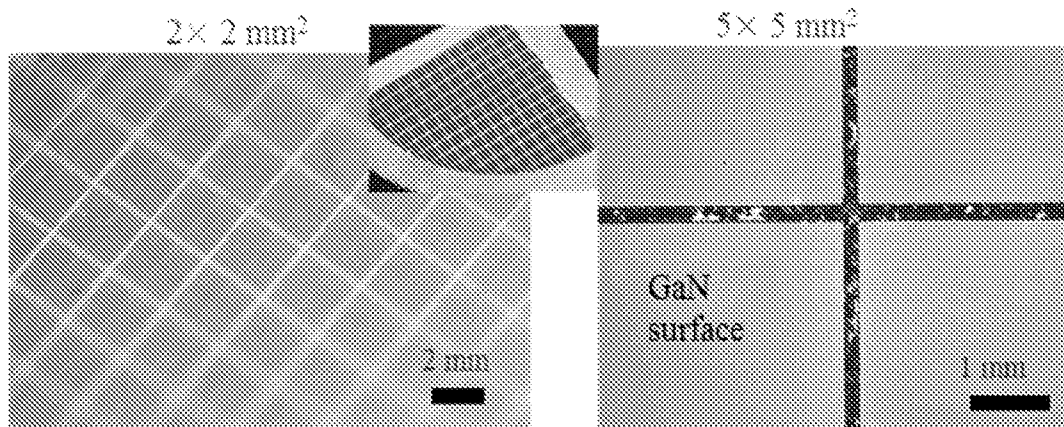


Figure 24

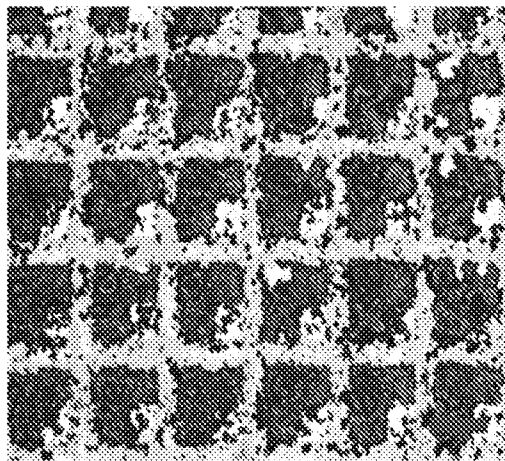


Figure 25

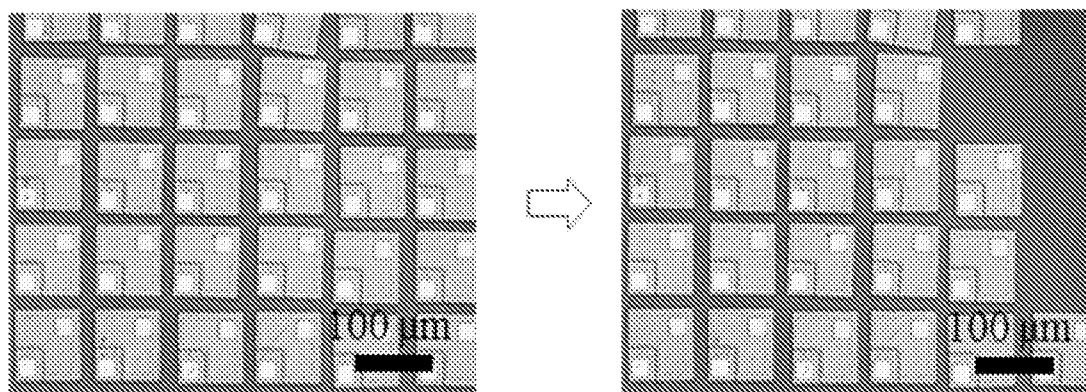


Figure 26

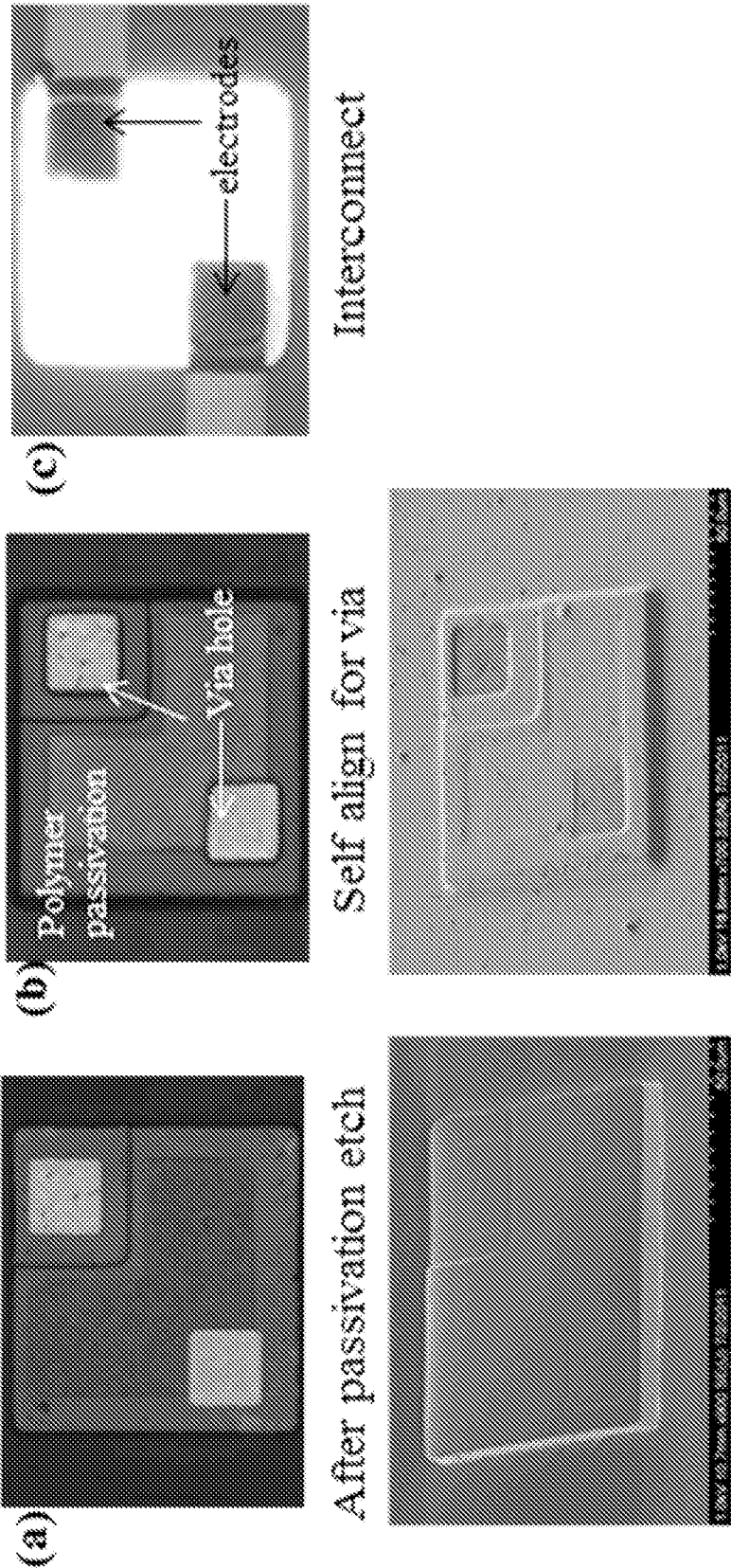


Figure 27

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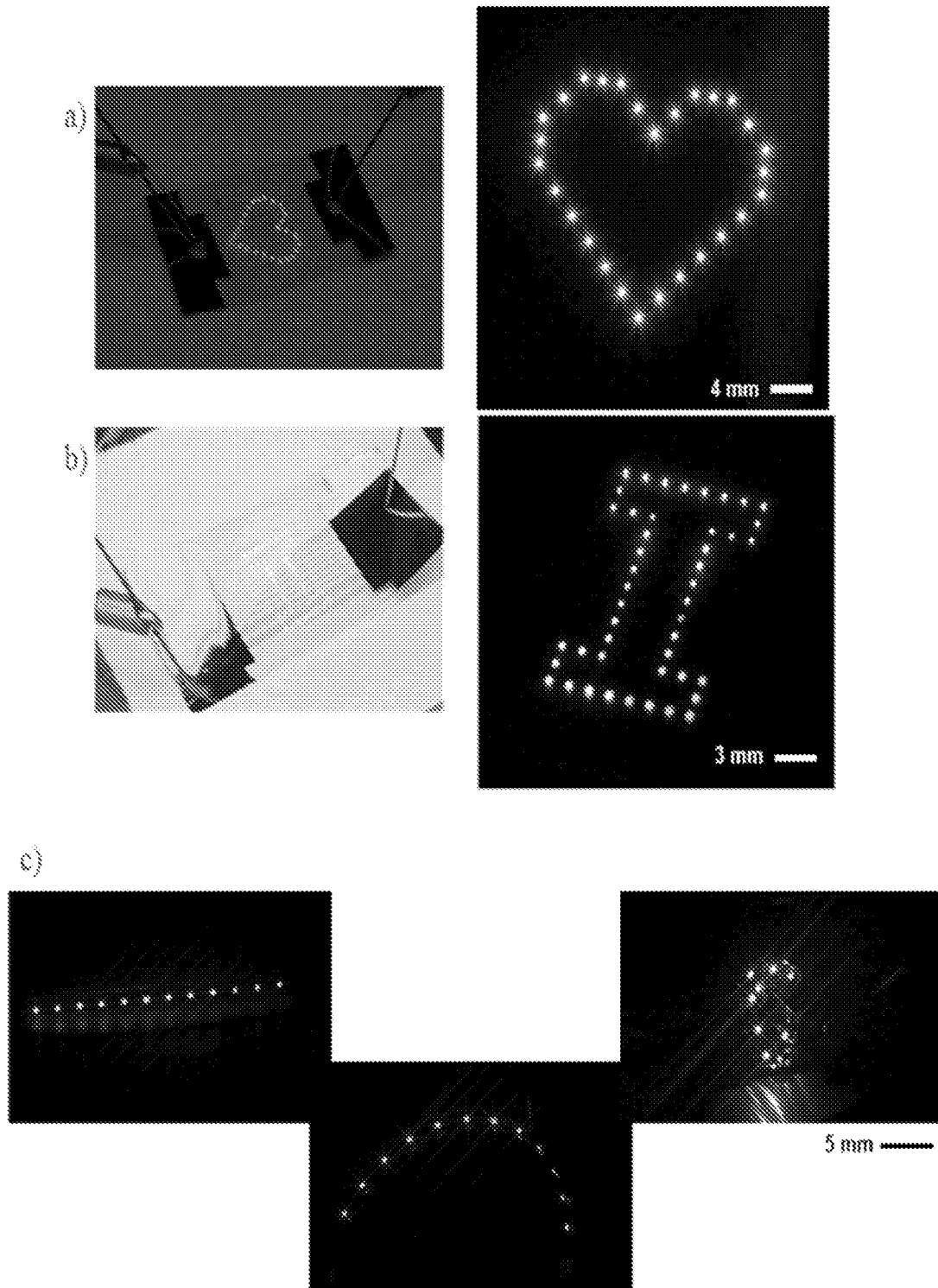
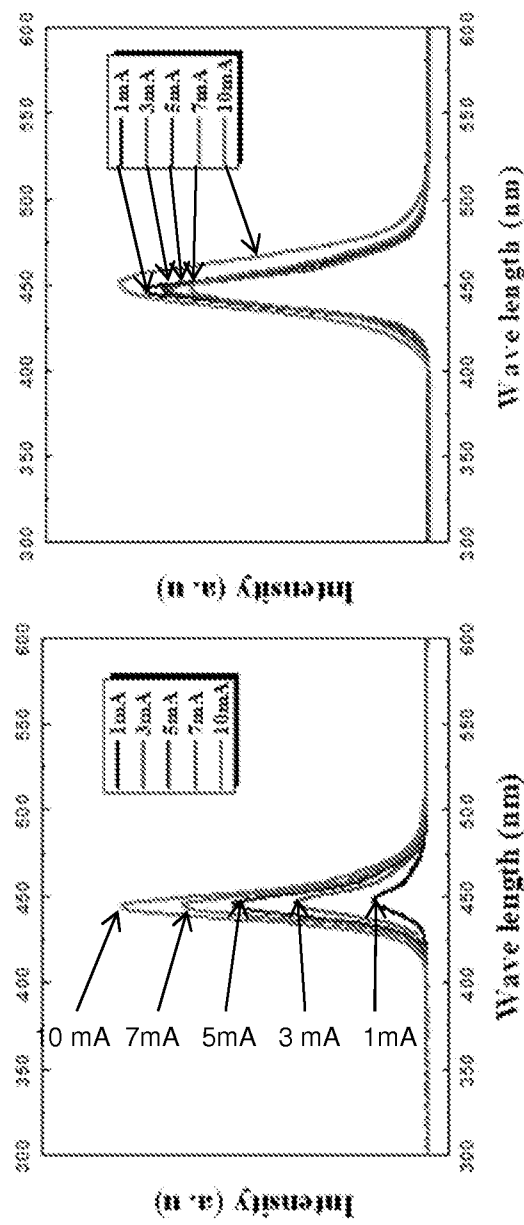


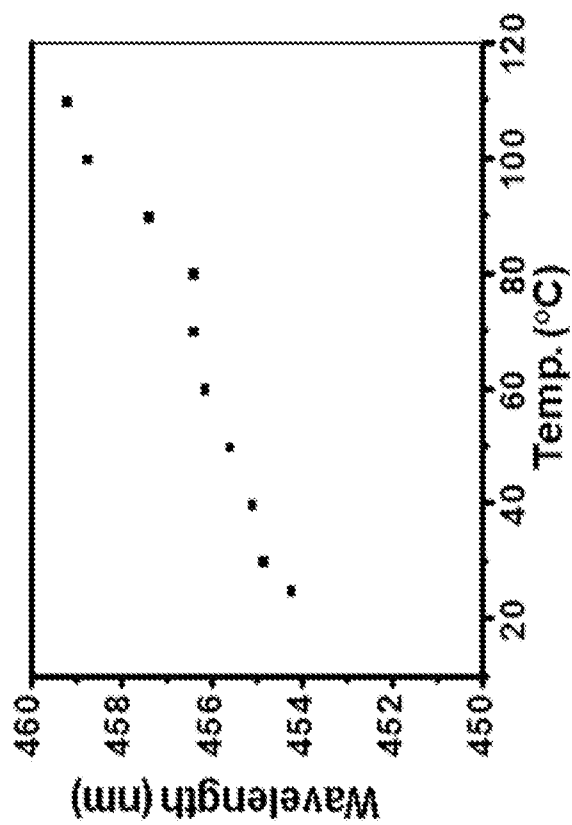
Figure 28



Before LLO (LED on sapphire) After LLO (LED on PET)

Current (mA)	1 mA	3 mA	5 mA	10 mA
Before LLO (on sapphire)	447.3	446.5	446.0	445.2
After LLO (on PET)	447.3	447.3	447.3	451.7

Figure 29



Temp (°C)	25	30	40	50	60	70	80	90	100	110
Wavelength (nm)	454.2	454.8	455.1	455.6	456.13	456.39	456.39	457.39	458.73	459.2

Figure 30

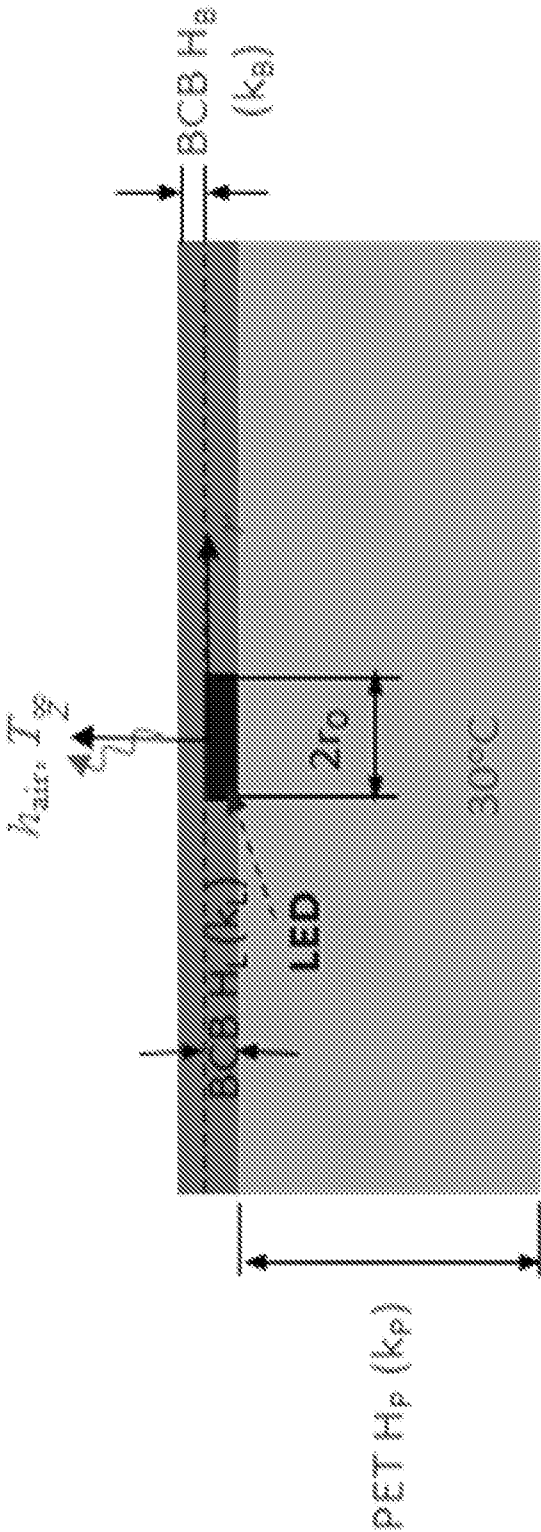


Figure 31

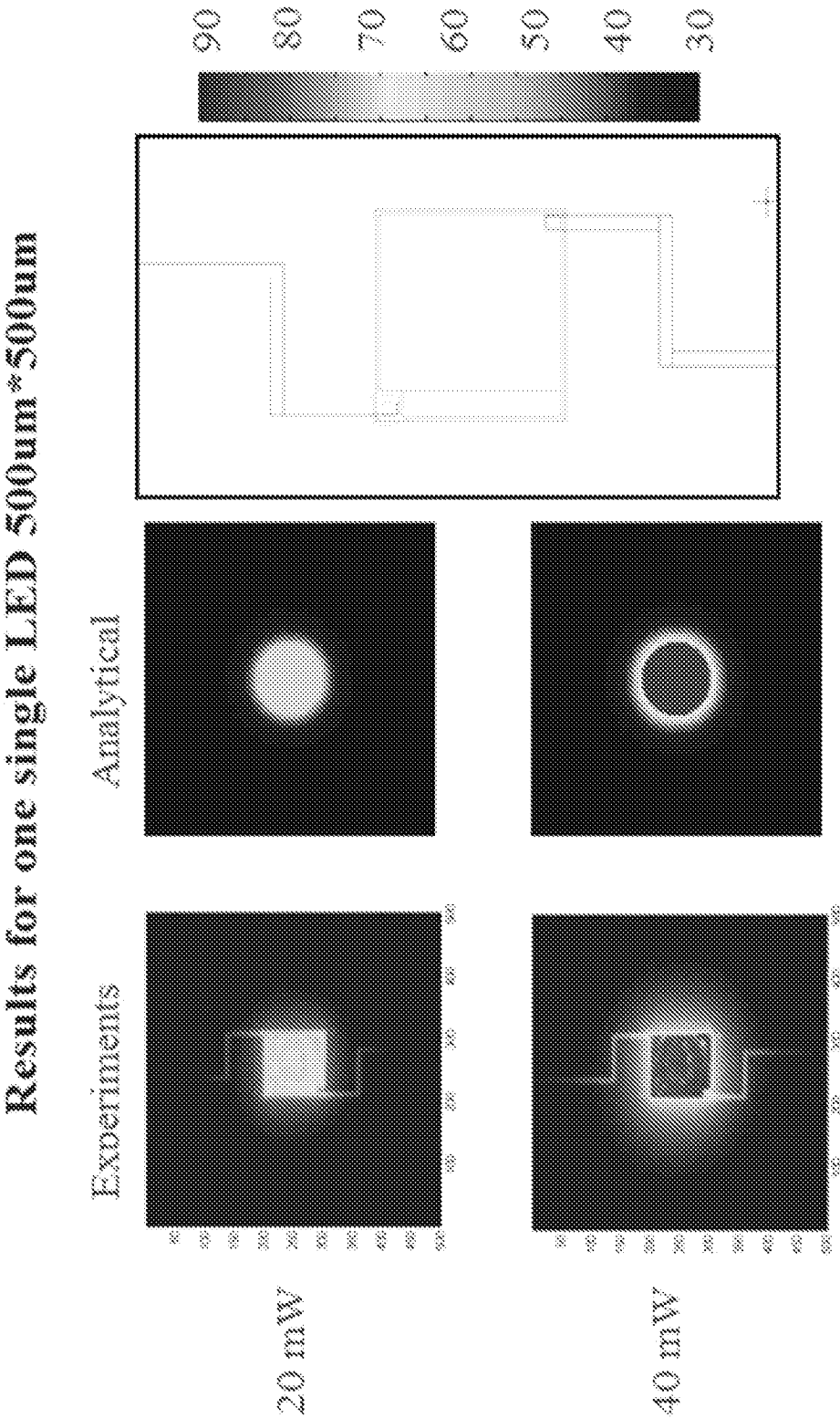
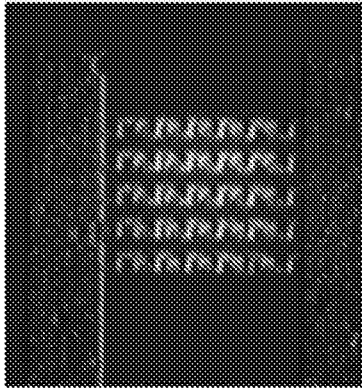


Figure 32

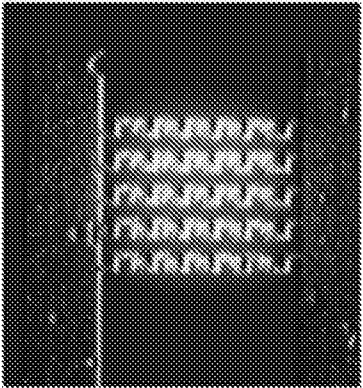
Results for LED array with spacing 100um

Experiments

Analytical



20 mW



40 mW

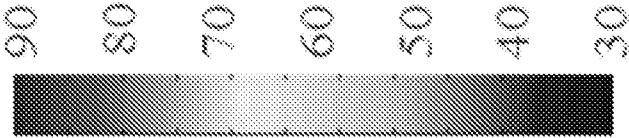
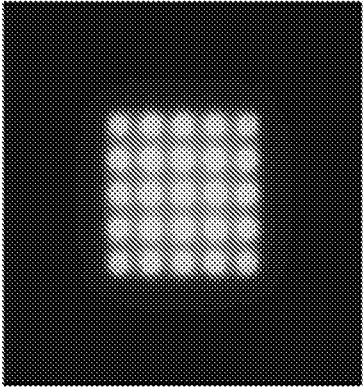
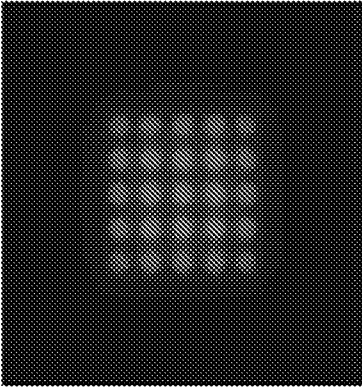


Figure 33

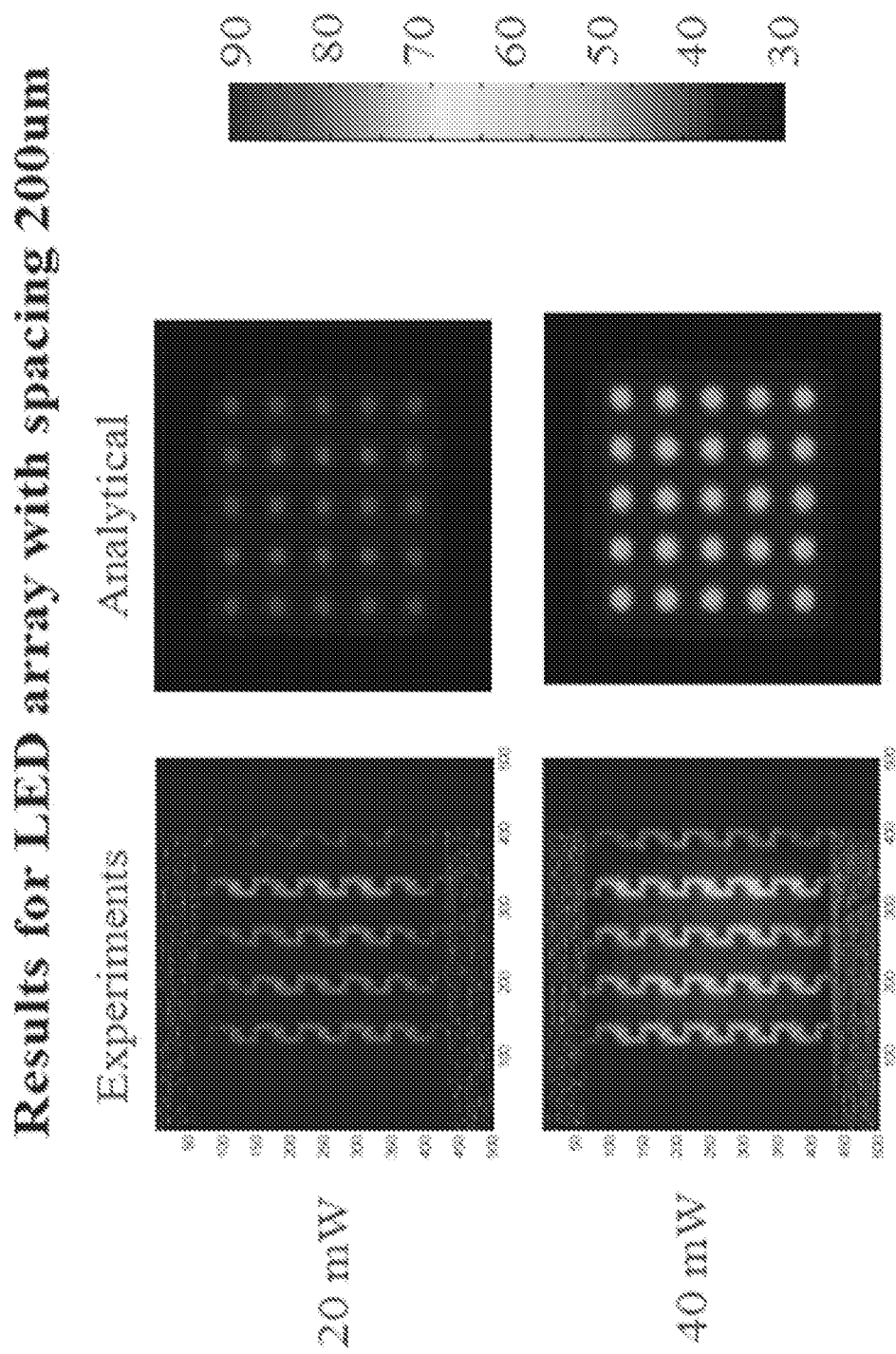


Figure 34

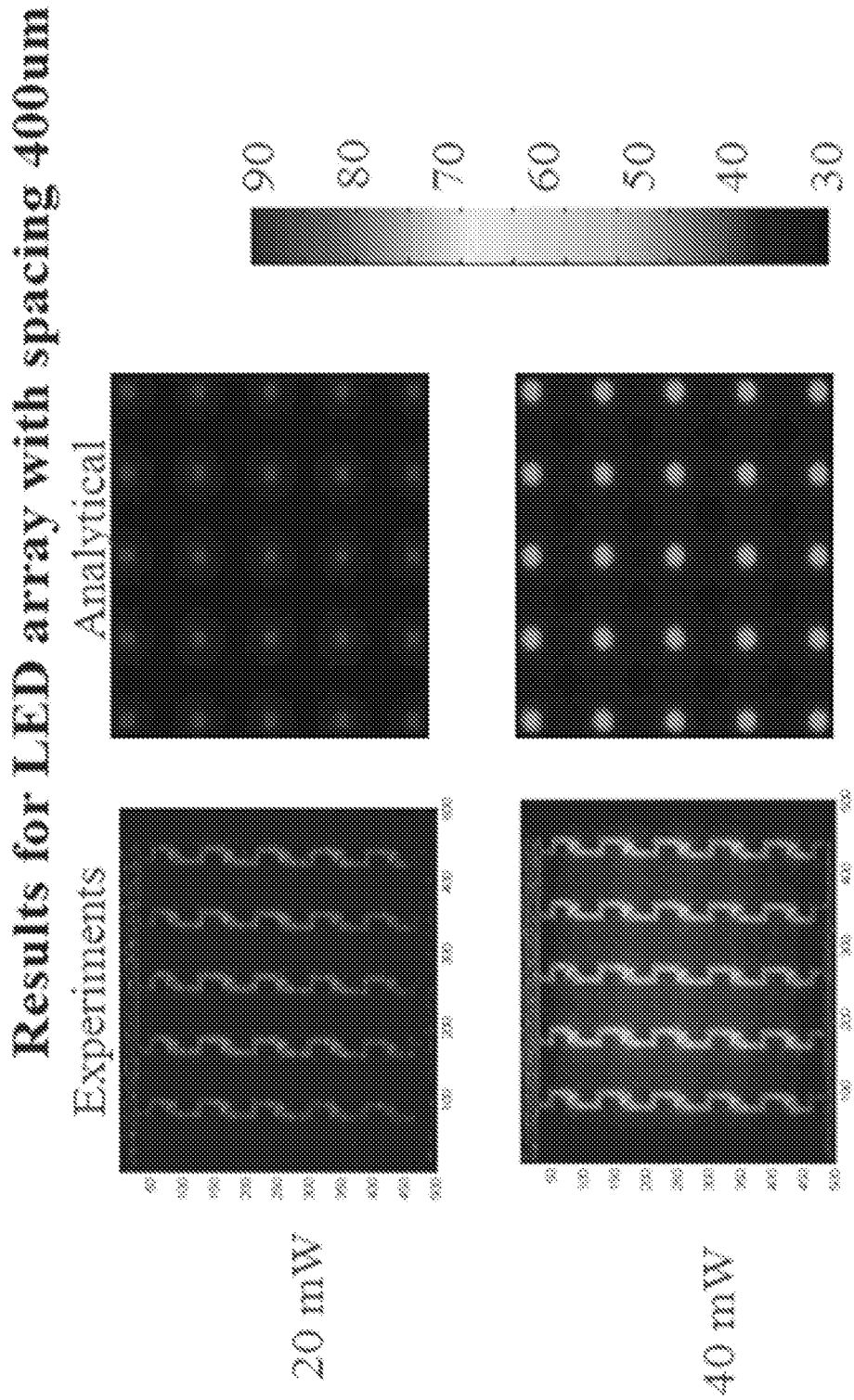


Figure 35

Results for LED array with spacing 1000um

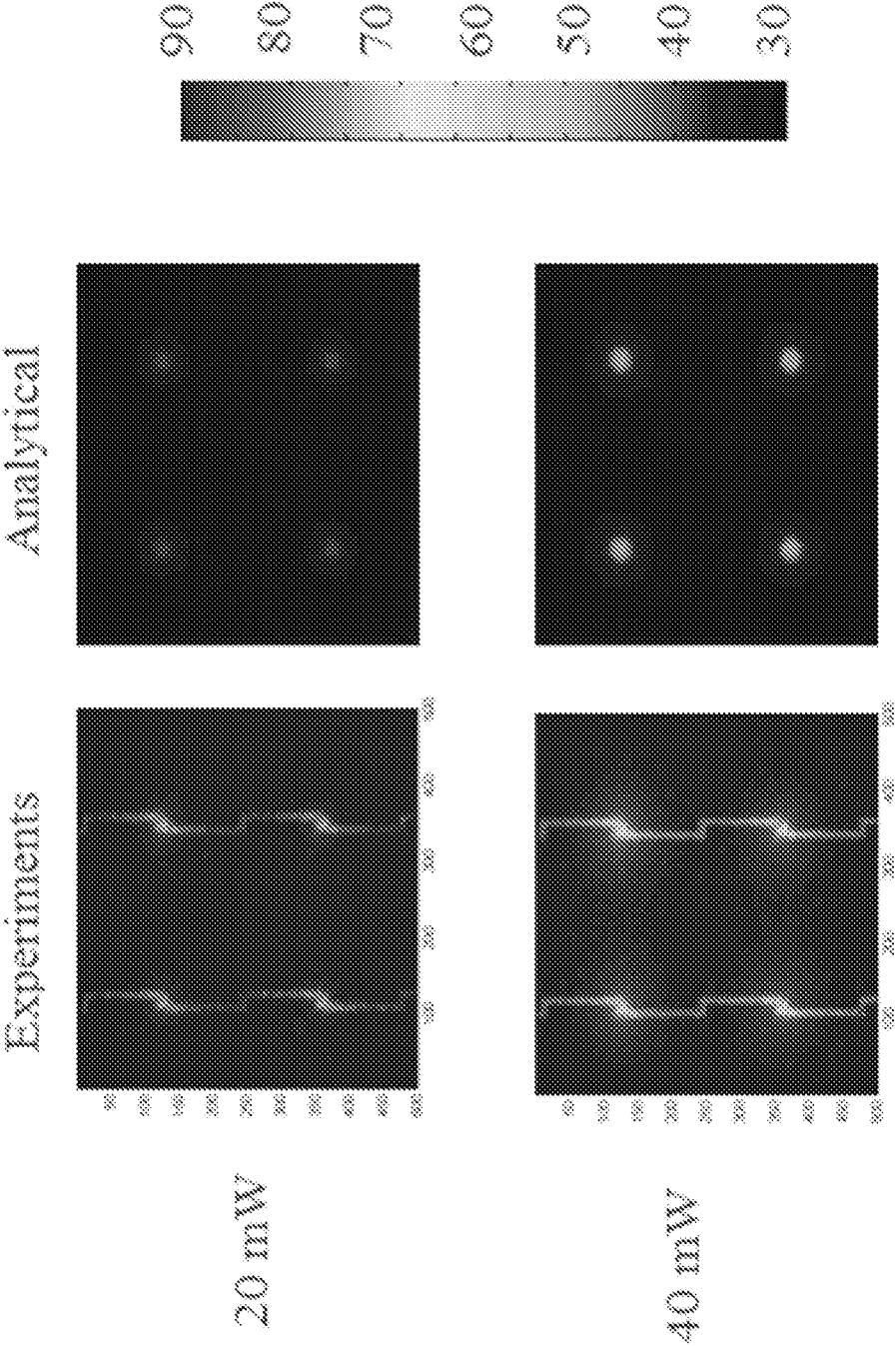
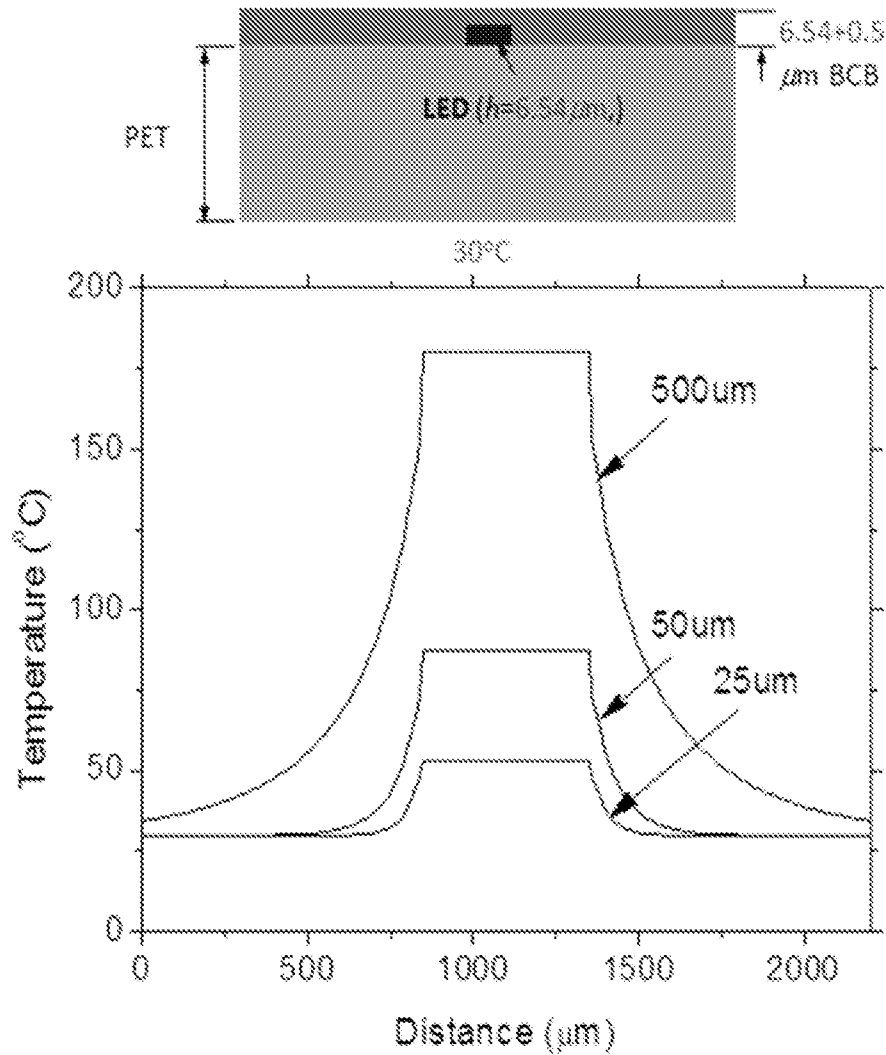


Figure 36

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Effect of PET thickness



Thermal decay length

25 μm thick PET: 100 μm (LED Temp: 53 °C)

50 μm thick PET: 210 μm (LED Temp: 87 °C)

500 μm thick PET: 850 μm (LED Temp: 179.8 °C)

Figure 37

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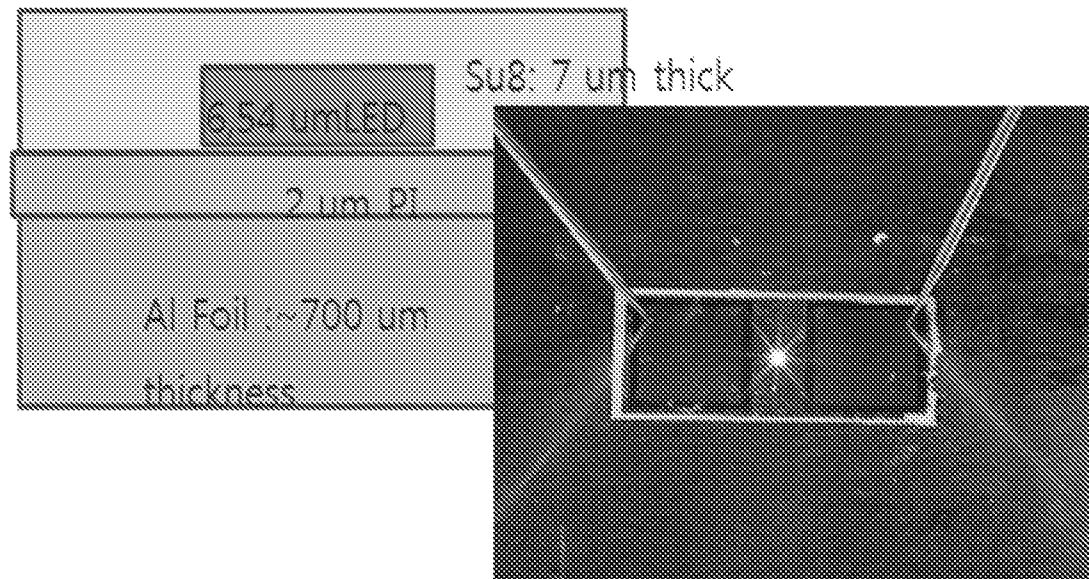


Figure 38

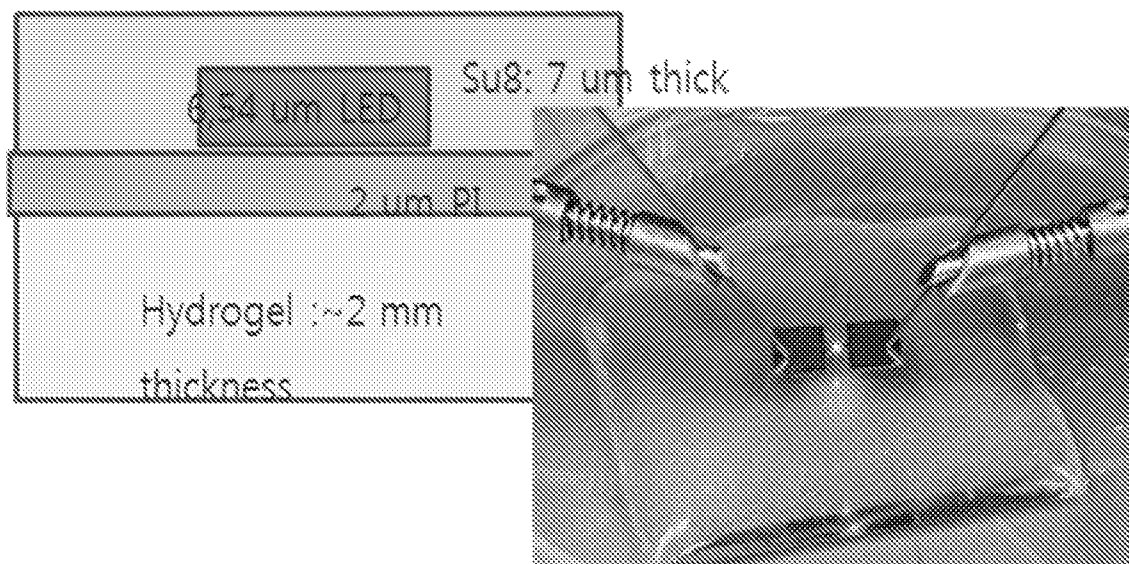


Figure 39

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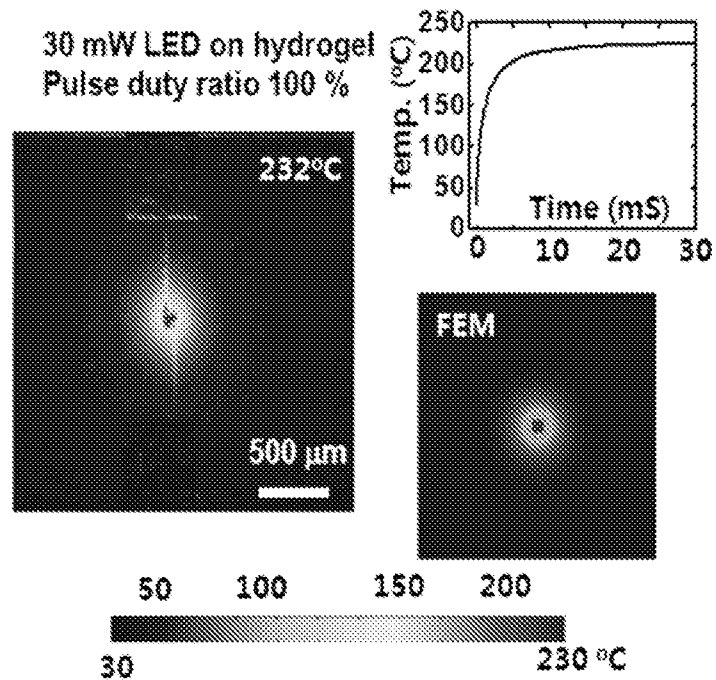


Figure 40

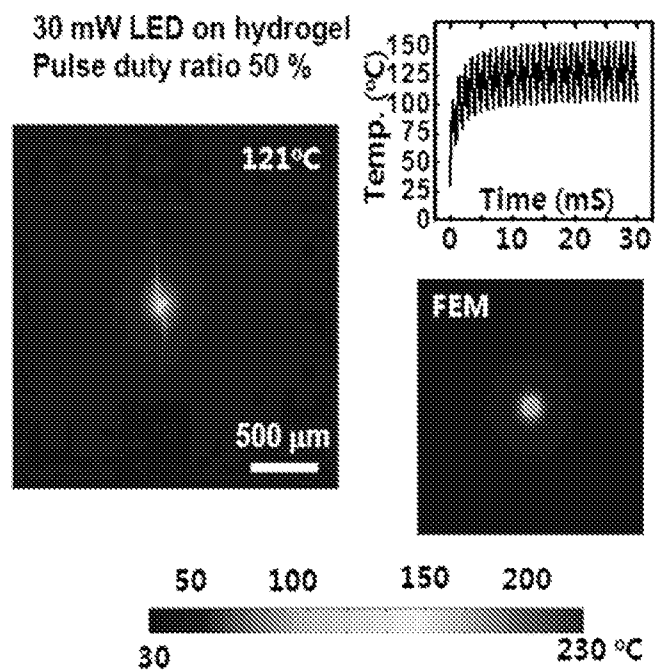


Figure 41

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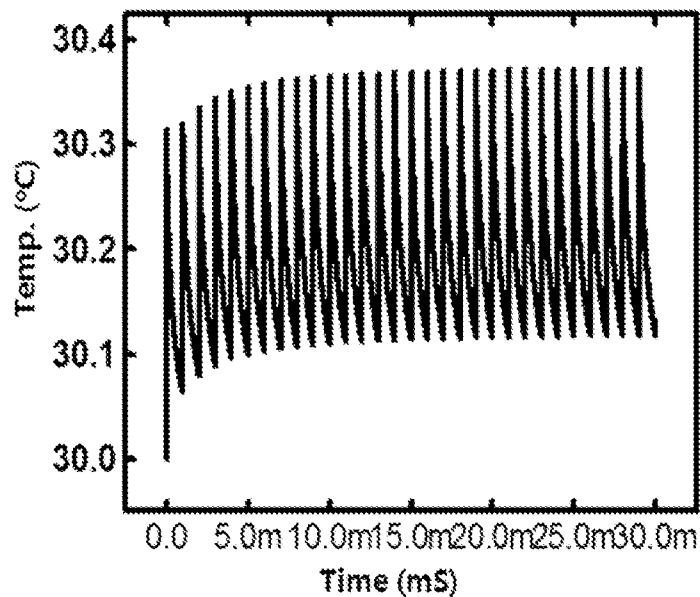


Figure 42

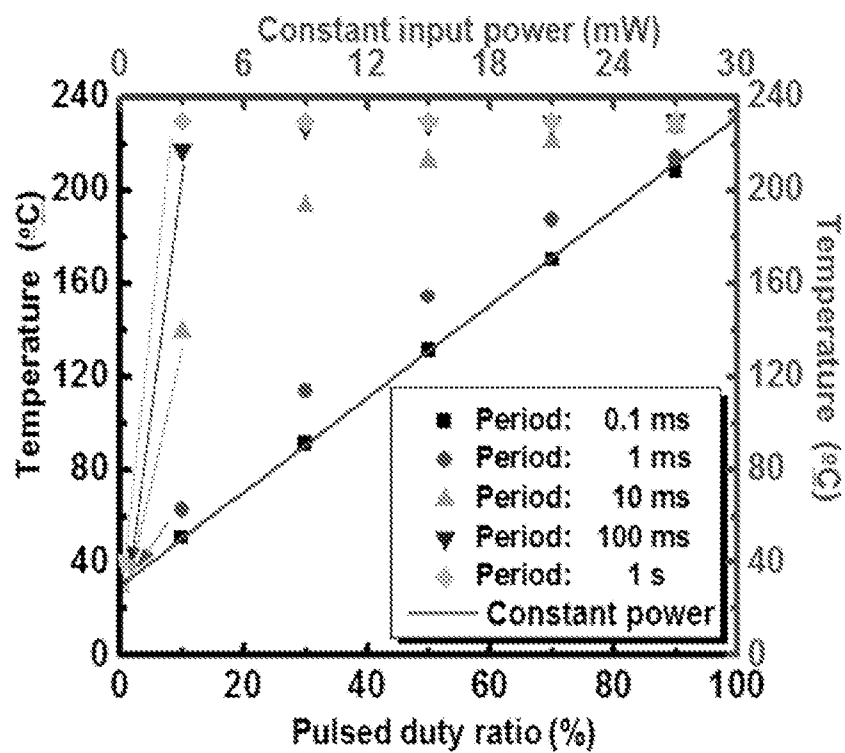


Figure 43

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 12/37973

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 29/18 (2012.01)

USPC - 257/88

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

USPC: 257/88

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

IPC: H01L29/18; USPC: 438/22, 438/29, 438/69; 257/79, 257/88, 257/98, 257/414, 257/443, 257/ E23.00, 257/E23.08 (keyword limited; terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PubWEST (USPT, PGPB, EPAB, JPAB); Google Scholar; Google Patents

Keywords: LED array; LED elements; printable; interconnects; spacing; dimensions; thickness; heat dissipation; substrate; dry contact

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2010/0252840 A1 (IBBETSON et al.) 07 October 2010 (07.10.2010), entire document, especially; para [0036], [0037], [0039], [0041], [0042], [0047], [0050]-[0052], [0057], [0064], [0066], [0067], [0069], [0070], [0098]	1-3, 61-63, 71-73
Y	US 2010/0317132 A1 (ROGERS et al.) 16 December 2010 (16.12.2010), entire document, especially; para [0016], [0057], [0066], [0075], [0195], [0226], FIG. 10	1-3, 61-63, 71-73
A	US 2011/0068672 A1 (HASNAIN) 24 March 2011 (24.03.2011), entire document	1-3, 61-63, 71-73
A	US 2010/0052112 A1 (ROGERS et al.) 04 March 2010 (04.03.2010), entire document	1-3, 61-63, 71-73
A	US 2010/0176705 A1 (VAN HERPEN et al.) 15 July 2010 (15.07.2010), entire document	1-3, 61-63, 71-73

☐ Further documents are listed in the continuation of Box C.


* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 July 2012 (26.07.2012)

Date of mailing of the international search report

14 AUG 2012

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-3201

Authorized officer:

Lee W. Young

PCT Helpdesk: 571-272-4300

PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 12/37973

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 4-60, 64-70, 74-89
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.