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(81) Designated States: AU, BR, CH (European patent), DE (European patent), FI, FR (European patent), GB (European patent), KR, US.

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: CLIPPER CIRCUIT FOR POWER TRANSISTOR CIRCUIT AND INVERTER CIRCUIT UTILIZING THE SAME

A clipper circuit includes an auxiliary diode connected between a capacitor and diode forming a clipper circuit. The auxiliary diode thus forms an auxiliary clipper circuit taking the capacitor as common capacitor. The auxiliary clipper circuit shunts current through the capacitor into first and second current flow through the diodes. This obviates the necessity for a snubber circuit and power source clipper circuit as employed in the power transistor circuit of an inverter circuit in the prior art.
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SPECIFICATION

CLIPPER CIRCUIT FOR POWER TRANSISTOR CIRCUIT AND INVERTER CIRCUIT UTILIZING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to a clipper circuit for a power transistor for absorbing surge voltage. More specifically, the invention relates to a clipper circuit which is suitable for simplification of a power transistor circuit and whereby allowing the power transistor circuit to be made satisfactorily compact.

Description of the Background Art

Power transistor circuits have been used in various electric source units as large current control elements. For example, a power transistor may be employed as a switching element in an inverter circuit. In such cases, it is a known technique to provide a clipper circuit in the power transistor circuit for absorbing surge voltages which are generated upon shutting off of the current, and whereby protecting the power transistor.

The conventional power transistor circuit, which is employed in a single phase inverter circuit, is associated with a power source clipper circuit interposed between the power transistor circuit and a power source. The power source clipper circuit is designed to absorb surge voltage generated in the power source. The power transistor circuit also incorporates a clipper circuit. The clipper circuit in the power transistor circuit is cooperative with the power source clipper circuit upon shutting off the current so that surges having high dv/dt are absorbed by the clipper circuit in the power transistor circuit and large energy
surges are absorbed by the power source clipper circuit.

In general, the clipper circuit is incorporated in the power transistor circuit, a series circuit comprised of a capacitor and a diode, and a discharge resistor. The capacitor-diode circuit is connected in parallel to a collector-emitter circuit of a power transistor. When the power transistor is turned OFF, collector current flows through the capacitor-diode series circuit. In the transition, the current is divided by the capacitor and the diode. By the dividing the current, voltage surges caused due to inductance of the wiring and so forth can be absorbed to lower the $dv/dt$ of voltage variations in collector-emitter circuit of the power transistor. However, in the vicinity of zero-crossing of the divided current, high frequency vibration tends to be caused. This high frequency vibration causes turning ON of the power transistor which, in turn causes shorting breakage upon ON-set of the other power transistor of the other power transistor circuit. In order to suppress the voltage vibration, a snubber circuit is provided in the power transistor circuit.

**SUMMARY OF THE INVENTION**

The present invention is intended to reduce the number of circuit components used in constructing a power transistor circuit and thus allow the power transistor circuit to be made satisfactorily compact.

Therefore, it is an object of the present invention to provide a power transistor circuit including an improved clipper circuit which eliminates the necessity of a snubber circuit.

Another object of the invention is to provide a power transistor circuit which is applicable for an inverter circuit and allows the omission a power source clipper circuit.

In order to accomplish the aforementioned and
other objects, a clipper circuit, according to the present invention, includes an auxiliary diode connected between a capacitor and diode forming a clipper circuit. The auxiliary diode thus forms an auxiliary clipper circuit taking the capacitor as a common capacitor. The auxiliary clipper circuit shunt current through the capacitor into a first and second current flowing through the diodes. This avoids necessity of a snubber circuit and of power source clipper circuit as employed in the power transistor circuit of an inverter circuit.

According to one aspect of the invention, a clipper circuit for a power transistor circuit including a power transistor comprises a first clipper circuit connected in parallel to a collector-emitter circuit of the power transistor and including a capacitor and a first diode, and a second clipper circuit including a second diode connected to the capacitor in parallel to a discharge resistor.

According to another aspect of the invention, a power transistor circuit comprises a power transistor connected to a power source and switching between a first state for establishing a collector-emitter circuit and a second state for blocking the collector emitter circuit for supplying a drive power for a load connected thereto, and a clipper circuit for absorbing surge energy to be generated upon switching of the power transistor from the first state to the second state, the clipper circuit includes a first clipper circuit connected in parallel to a collector-emitter circuit of the power transistor and including a capacitor and a first diode, and a second clipper circuit includes a second diode connected to the capacitor in parallel to a discharge resistor.

According to a further aspect of the invention, an inverter circuit connected to a direct current source via a smoothing circuit including a
smoothing capacitor, comprises a plurality of power transistor circuits connected to a load for supplying a driving alternating current to the latter, each of the power transistor circuit includes a power transistor switching between a first state for establishing a collector-emitter circuit and a second state for blocking the collector emitter circuit, and a clipper circuit for absorbing surge energy to be generated upon switching of the power transistor from the first state to the second state, the clipper circuit includes a first clipper circuit connected in parallel to a collector-emitter circuit of the power transistor and including a capacitor and a first diode, and a second clipper circuit including a second diode connected to the capacitor in parallel to a discharge resistor.

In practice, the second diode of the second clipper circuit is connected to a junction between the capacitor and the first capacitor so that current flowing through the capacitor is shunted into a first shunted current flowing through the first diode and a second shunted current flowing through the second diode. Preferably, the second clipper circuit is provided greater L than the first clipper circuit.

With the constructions set forth above, the, first clipper circuit is adapted to absorb high dv/dt surge voltage and second clipper circuit is adapted to absorb surge energy generated by wiring inductance, upon switch of the power transistor from the first state to the second state. The first and second clipper circuits are active for absorbing surge generated upon switching of the power transistor from the first state to the second state and reduces first and second shunted current flowing through the first and second diodes according to rising of charge voltage in the capacitor, and the first and second clipper circuits are so designed as to decrease current levels of the first and
second shunted current to zero at mutually different timing.

In order to effectively suppress voltage fluctuation which can be caused by recovery of diodes upon termination of the shunted current, the second clipper circuit preferably maintains the second shunted current after termination of said first shunted current flowing through the first diode.

It is also preferable that the power transistor circuit further comprises an auxiliary capacitor connected in parallel to the first diode. The auxiliary transistor has smaller capacity than the capacitor in the clipper circuits.

In the mechanical construction, the first and second clipper circuits are mounted on a printed circuit board connected to collector and emitter electrode terminal of the power transistor formed on a substrate via connecting screw, the printed circuit board is placed in spaced apart relationship with opposing surface of the substrate. Such construction of circuit assembly effective reduces wiring inductance and provides better surge absorption characteristics.

**BRIEF DESCRIPTION OF THE DRAWINGS**

The present invention will be understood more fully from the detailed description given herebelow and from the accompanying drawings of the preferred embodiment of the invention, which, however, should not be taken to limit the invention to the specific embodiment but are for explanation and understanding only.

In the drawings:

Fig. 1 is a circuit diagram of the a single phase inverter circuit which employs power transistor circuits, each incorporating the preferred embodiment of a clipper circuit according to the present invention;

Fig. 2 shows waveforms at various section in
the inverter circuit of Fig. 1;

Fig. 3 is a plan view of the preferred construction of an assembly of the power transistor circuit;

Fig. 4 is a front elevation of the power transistor circuit assembly of Fig. 3; and

Fig. 5 is a front elevation of another embodiment of the construction of the power transistor circuit assembly according to the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the drawings, particularly to Fig. 1, there is depicted a known main or power circuit of a single phase inverter circuit, which is connected to a load 10, such as an induction motor. The inverter main circuit is connected to a known converter circuit (not shown) to receive direct current power supply therefrom. The inverter main circuit generally comprises a smoothing stage 20 including a smoothing capacitor 22 for smoothing, and an inverter stage which is generally represented by the reference numeral 30. As is well known, the smoothing stage 20 is interposed between the converter and the inverter stage 30 is the inverter main circuit for absorbing ripples in the direct power supplied from the converter.

The inverter stage 30 includes pairs of the power transistor circuits 32, 34 and 36, 38, of the preferred embodiments. These pairs of power transistor circuits 32, 34 and 36, 38 are connected to the load 10 for driving the latter. On the other hand, the power transistors 32, 34 and 36, 38 are connected to a known switching signal generator circuit in an inverter control circuit. Thus, the switching timing is controlled so as to generate a single-phase alternating current to supply to the load 10, in a per se well known manner.

It should be noted that the power transistor
circuits 36 and 38 are identical in construction to the power transistors 32 and 34. Therefore, detailed construction of these power transistor circuits 36 and 38 are not shown in Fig. 1.

The power transistor circuit 32 includes a power transistor 321 connected to the switching signal generator of the control circuit at the base electrode. The collector electrode of the power transistor 321 receives the power source current Ic from the converter. A flywheel diode 322 is connected in parallel to the collector-emitter circuit of the power transistor 321. A first clipper circuit 323 comprising a capacitor 324 and a first diode 325, is also provided in parallel to the collector-emitter circuit of the power transistor 321. A junction between the capacitor 324 and the first diode 325, is connected to the negative terminal of the converter via a discharge resistor 326. A second diode 327 is also connected to the junction between the capacitor 324 and the first diode 325 in parallel to the discharge register 326. The second diode 325 is thus forms a second clipper circuit 328 with the capacitor 324.

In the preferred construction, the second diode 327 of the second clipper circuit 328 is so designed and arranged as to provide the second clipper circuit 328 a much greater inductance (L) than that of the first clipper circuit 323.

Similarly to the power transistor circuit 32, the power transistor 34 includes a power transistor 341 connected to the switching signal generator of the control circuit at the base electrode. The collector electrode of the power transistor 341 is connected to the emitter electrode of the power transistor 321 to form a series circuit comprised of the power transistors 321 and 341. The emitter electrode of the power transistor 341 is connected to negative terminal of the
converter. A junction between the power transistors 321 and 341 is connected to the load 10.

In parallel to the collector-emitter circuit of the power transistor 341, a flywheel diode 342 is connected. A first clipper circuit 343 comprising a capacitor 344 and a first diode 345, is also provided in parallel to the collector-emitter circuit of the power transistor 341. The junction between the capacitor 344 and the first diode 345, is connected to the negative terminal of the converter via a discharge resistor 346. A second diode 347 is also connected to the junction between the capacitor 344 and the first diode 345 in parallel to the discharge register 346. The second diode 345 thus forms a second clipper circuit 348 with the capacitor 344.

The second diode 347 of the second clipper circuit 348 is so designed and connected as to provide much greater inductance (L) for the second clipper circuit 348 than that of the first clipper circuit 343.

The second clipper circuits 328 and 348 perform an equivalent function to the power source clipper circuit in the conventional inverter main circuit for absorbing surge voltage generated in the converter used as the DC power source, upon shutting OFF of the power supply. These second clipper circuits 328 and 348 are also cooperative with the first clipper circuits 323 and 343 to suppress voltage fluctuations caused in the OFF-set transition of respectively associated power transistors 321 and 341.

Absorption of the voltage fluctuation in the first and second clipper circuits 323 and 328 of the power transistor circuit 32 will be discussed herebelow.

When the power transistor 321 is turned OFF, load current Ic at the collector electrode of the power transistor 321 commutates to flow through the capacitor 324 as shunted current Icc. The current through the
capacitor 324 is further shunted to flow through the
diodes 325 and 327 as shunted currents $I_1$ and $I_2$. By
this, the capacitor 324 is charged. The collector-emitter
voltage $V_{CE}$ of the power transistor 321 is raised
according to the increase of the capacitor voltage.

The smoothing capacitor 22 then serves as to
absorb surge energy for suppressing fluctuation of the
power source voltage $V_{DC}$.

According to increase of the capacitor voltage
by charging the capacitor 324, the shunted currents $I_1$
and $I_2$ flowing through the diodes 325 and 327 drop to
zero. In the shown embodiment, the first and second
clipper circuits 323 and 328 are so constructed as to
maintain the shunted current $I_2$ flowing through the
diode 327 even after the shunted current $I_1$ of the diode
325 becoming zero, as shown in Fig. 2. By this, voltage
fluctuation caused on the collector-emitter circuit of
the power transistor 321 by recovery of the diode 325
upon drop to zero of the shunted current $I_1$ flowing
therethrough to zero, can be held to a substantially
small magnitude. The magnitude of voltage fluctuation
at termination of the shunted current $I_1$ is sufficiently
reduced to make snubber circuit which is required in the
conventional circuit, unnecessary.

Upon termination of the shunted current $I_2$,
recovery of the diode 327 causes voltage fluctuation due
to $L$ and $C$ in the whole circuit of the inverter main
circuit. However, since the second clipper circuit 328
is so designed as to have much greater $L$ than that of
the first clipper circuit, frequency of voltage
fluctuation can be kept at low. Furthermore, backward
resistance of the diode 327 aids suppression of the
voltage fluctuation. Therefore, even upon recovery of
the diode 327, high frequency voltage fluctuation which
tends to cause breakage of the power transistor 321 can
be successfully suppressed.
It should be noted that the voltage fluctuation suppressive operation to be performed by the power transistor circuit 34 is substantially the same as that of the power transistor circuit 32 as set forth above. Therefore, detailed discussion about the circuit operation of the power transistor circuit 34 is neglected in order to simplify the disclosure and to avoid redundance.

In the circuit construction shown in Fig. 1 and disclosed hereabove, it is further preferable to provide a capacitor $C_0$ which has substantially smaller capacity that that of the diode 324 and 344. The capacity of the capacitor $C_0$ can be one tenth of the capacity of the capacitor 324, 344, for example. The capacitor $C_0$ may be effective for suppressing large magnitude surge voltages which can be caused upon termination of the shunt current flowing through the diodes 324 and 327.

Figs. 3 and 4 show the preferred construction of the power transistor circuit 32. The power transistor 321 has a collector electrode terminal C and an emitter electrode terminal E. To these collector electrode terminal C and the emitter electrode terminal E, a printed circuit board 40 is secured by conductive screws. The printed circuit board 40 is oriented in a spaced apart relationship to the opposing surface of the power transistor 321 by means of spacers 42 and 44. The capacitor 324, the diodes 325 and 327, the discharge resistor 326 and so forth are rigidly secured on the surface of the printed circuit board 40 with electric communication maintained by the printed wiring on the circuit board.

The shown construction of the power transistor circuit 32 is effective for reducing wiring inductance between the collector and emitter electrode terminals C and E and the clipper circuits 323 and 328 so as to
effectively absorb surge voltage.

Fig. 5 shows another example of preferred construction of the transistor circuit 32. In this embodiment, pair of printed circuit boards 50 and 52 are secured to the collector and the emitter electrode terminals C and E by means of conductive screws. The printed circuit boards 50 and 52 are arranged essentially perpendicular to the upper surface of the power transistor 321 and in parallel to each other. The pair of printed circuit boards 50 and 52 support therebetween the capacitor 324. Other circuit elements, such as the diodes 325 and 327, the discharge resistor 326 and so forth are mounted on one of the printed circuit boards 50 and 52.

The circuit construction illustrated in Fig. 5 is also effective for reducing the amount of wiring inductance and effectively absorbing the surge voltage.

Therefore, the invention fulfills all of the objects and advantages sought therefor.

While the present invention has been disclosed in terms of the preferred embodiment in order to facilitate better understanding of the invention, it should be appreciated that the invention can be embodied in various ways without departing from the principle of the invention. Therefore, the invention should be understood to include all possible embodiments and modifications to the shown embodiments which can be embodied without departing from the principle of the invention set out in the appended claims.
WHAT IS CLAIMED IS:

1. A clipper circuit for a power transistor circuit including a power transistor comprising:
a first clipper circuit connected in parallel to a collector-emitter circuit of said power transistor and including a capacitor and a first diode; and
a second clipper circuit including a second diode connected to said capacitor in parallel to a discharge resistor.

2. A clipper circuit as set forth in claim 1, wherein said second diode of said second clipper circuit is connected to a junction between said capacitor and said first capacitor so that current flowing through said capacitor is shunted into a first shunted current flowing through said first diode and a second shunted current flowing through said second diode.

3. A clipper circuit as set forth in claim 1, wherein said second clipper circuit is provided greater L than said first clipper circuit.

4. A clipper circuit as set forth in claim 1, wherein said first clipper circuit is adapted to absorb high dv/dt surge voltage and second clipper circuit is adapted to absorb large surge energy generated by wiring inductance, upon turning OFF of said power transistor.

5. A clipper circuit as set forth in claim 1, wherein said first and second clipper circuits are active for absorbing surges generated upon turning OFF of said power transistor and reduces said first and second shunted currents flowing through said first and second diodes according to rising of charge voltage in said capacitor, and said first and second clipper circuits are so designed as to decrease said first and
second shunted current to zero at mutually different timings.

6. A clipper circuit as set forth in claim 5, wherein second clipper circuit maintains said second shunted current after termination of said first shunted current flowing through said first diode.

7. A power transistor circuit comprising:

- a power transistor connected to a power source and switching between a first state for establishing a collector-emitter circuit and a second state for blocking said collector emitter circuit for supplying drive power to a load connected thereto; and
- a clipper circuit for absorbing surge energy to be generated upon switching of said power transistor from said first state to said second state, said clipper circuit including
  - a first clipper circuit connected in parallel to a collector-emitter circuit of said power transistor and including a capacitor and a first diode; and
  - a second clipper circuit including a second diode connected to said capacitor in parallel to a discharge resistor.

8. A power transistor circuit as set forth in claim 7, wherein said second diode of said second clipper circuit is connected to a junction between said capacitor and said first capacitor so that current flowing through said capacitor is shunted into a first shunted current flowing through said first diode and a second shunted current flowing through said second diode.

9. A power transistor circuit as set forth in
claim 7, wherein said second clipper circuit is provided greater I than said first clipper circuit.

10. A power transistor circuit as set forth in claim 7, wherein said first clipper circuit is adapted to absorb high dv/dt surge voltage and said second clipper circuit is adapted to absorb surge energy generated by wiring inductance, upon switching of said power transistor from said first state to said second state.

11. A power transistor circuit as set forth in claim 7, wherein said first and second clipper circuits are active for absorbing surges generated upon switching of said power transistor from said first state to said second state and reduce first and second shunted current flows through said first and second diodes according to the increase of charge voltage in said capacitor, and said first and second clipper circuits are so designed as to decrease said first and second shunted current to zero at mutually different timings.

12. A power transistor circuit as set forth in claim 11, wherein second clipper circuit maintains said second shunted current after termination of said first shunted current flowing through said first diode.

13. A power transistor circuit as set forth in claim 7, which further comprises an auxiliary capacitor connected in parallel to said first diode.

14. A power transistor circuit as set forth in claim 13, wherein said auxiliary transistor has smaller capacity than said capacitor in said clipper circuits.

15. A power transistor circuit as set forth in
claim 7, wherein said first and second clipper circuits are mounted on a printed circuit board connected to collector and emitter electrode terminal of said power transistor formed on a substrate via connecting screws, and said printed circuit board is placed in spaced apart relationship with opposing surface of said substrate.

16. An inverter circuit connected to a direct current source via a smoothing circuit including a smoothing capacitor, comprising:

   a plurality of power transistor circuits connected to a load for supplying a driving alternating current to the latter, each of said power transistor circuits including a power transistor switching between a first state for establishing a collector-emitter circuit and a second state for blocking said collector-emitter circuit; and

   a clipper circuit for absorbing surge energy generated upon switching of said power transistor from said first state to said second state, said clipper circuit including a first clipper circuit connected in parallel to a collector-emitter circuit of said power transistor and including a capacitor and a first diode, and a second clipper circuit including a second diode connected to said capacitor in parallel to a discharge resistor.

17. An inverter circuit as set forth in claim 16, wherein said second diode of said second clipper circuit is connected to a junction between said capacitor and said first capacitor so that current flowing through said capacitor is shunted into a first shunted current flowing through said first diode and a second shunted current flowing through said second diode.

18. An inverter circuit as set forth in claim 16,
wherein said second clipper circuit is provided greater L than said first clipper circuit.

19. An inverter circuit as set forth in claim 16, wherein said first clipper circuit is adapted to absorb high dv/dt surge voltage and second clipper circuit is adapted to absorb surge energy generated by wiring inductance, upon switching of said power transistor from said first state to said second state.

20. An inverter circuit as set forth in claim 16, wherein said first and second clipper circuits are active for absorbing surges generated upon switching of said power transistor from said first state to said second state and reduces first and second shunted current flowing through said first and second diodes according to rising of charge voltage in said capacitor, and said first and second clipper circuits are so designed as to decrease said first and second shunted current to zero at mutually different timings.

21. An inverter circuit as set forth in claim 20, wherein second clipper circuit maintains said second shunted current after termination of said first shunted current flowing through said first diode.
**INTERNATIONAL SEARCH REPORT**

**I. CLASSIFICATION OF SUBJECT MATTER**

According to International Patent Classification (IPC) or to both National Classification and IPC

| IPC | H 02 M 7/5387; H 03 K 17/16 |

**II. FIELDS SEARCHED**

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**IV. CERTIFICATION**

Date of the Actual Completion of the International Search: 19th August 1988

Date of Mailing of this International Search Report: 16 Sep 1988

International Searching Authority: EUROPEAN PATENT OFFICE

Signature of Authorized Officer: P.C.G. VANDER PUTTEN
ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO. JP 8800458
SA 22155

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 08/09/88. The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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