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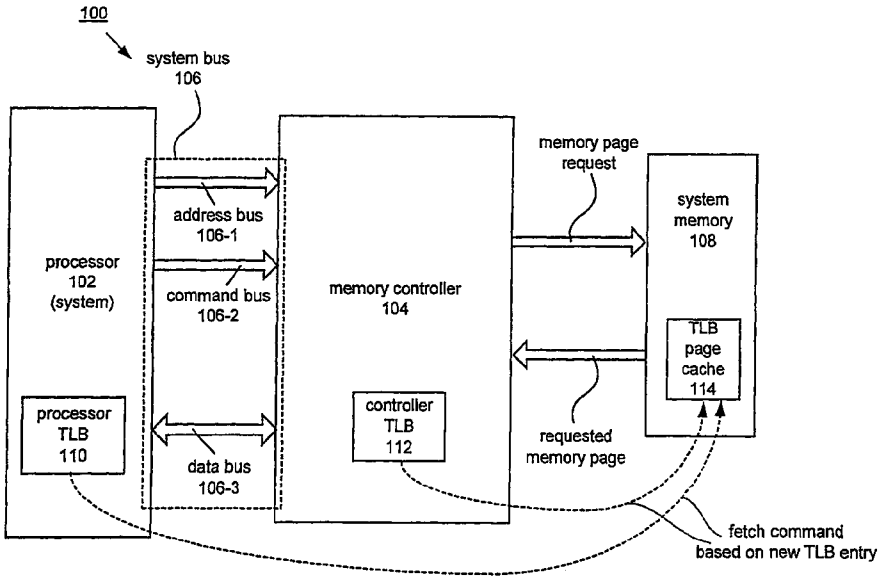

(57) Abstract: According to the present invention, methods and apparatus for reducing memory access latency are disclosed. When a new entry is made to translation look aside buffer (110), the new TLB entry points to a corresponding TLB page of memory (108). Concurrently with the updating of the TLB (110), the TLB page is moved temporally closer to a processor (102) by storing the TLB page in a TLB page cache (114). The TLB page cache (114) is temporally closer to the processor (102) than is a main memory (108).

WO 00/45270 A1

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