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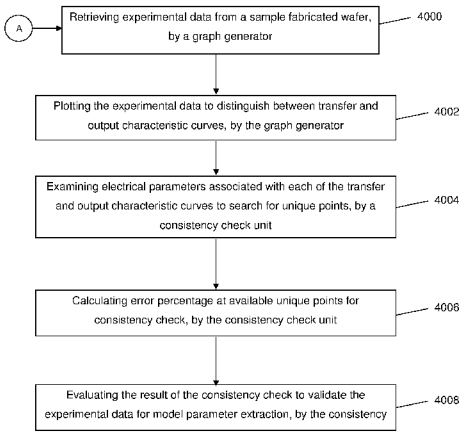
FIG.4



(57) Abstract: Model parameter extraction for transistor modeling relies on experimental data provided and any discrepancy therein, if undetected at the outset, results in inaccurate models and delay in device/technology development. The method and apparatus of the present disclosure addresses this problem by introducing a consistency check prior to the model extraction stage. The method requires a set of experimental data, such as measured drain currents from the actual fabricated wafer for consistency check. The experimental data is formatted into readable ASCII or text file data for identification of unique points. A set of computer instructions which form the apparatus that evaluates the data consistency then provides the result of the consistency check to permit or restrain the model parameter extraction stage. The most illustrative drawing.

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METHOD AND APPARATUS FOR VALIDATING EXPERIMENTAL DATA PROVIDED FOR TRANSISTOR MODELING

FIELD OF THE INVENTION

The present invention relates to the field of simulation of semiconductor integrated circuits (ICs), particularly to a method and apparatus for evaluating transistor characteristics based on experimental data provided for model parameter extraction in transistor modeling.

DEFINITIONS

The terms used throughout this specification are defined as follows, unless otherwise limited in specific instances.

The expression 'machine readable media' used hereinafter in the specification refers to RAM, ROM, EPROM, EEPROM, CD-ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other medium which can be used to carry or store desired program code in the form of machine-executable instructions or data structures and which can be accessed by a general purpose or special purpose computer or other machine with a processor.

The expression 'computer program product' is defined as a manufactured product embodied in a machine readable medium as defined herein above.

The expression 'plotting' used hereinafter in the specification includes at least one of computationally generating a graphical display of data, computationally establishing a mathematical expression corresponding to data and computationally generating data based on predetermined relationships.

The expressions 'graph generator' and 'consistency check unit' used hereinafter in the specification refer to modules embodied in machine readable media.

The expression 'unique points' used hereinafter in the specification refers to plotted data wherein identical values are retrieved for the electrical parameter such as 'bias voltages'.

These definitions are in addition to those expressed in the art.

BACKGROUND

The three main steps involved in generating a transistor model for circuit simulation include electrical measurements followed by model parameter extraction and finally model verification. It is critical to ensure that functional integrated circuits at design level also function as per specifications after being fabricated at wafer level. Accordingly, accurate device models are essential to fulfill requirements where extracted model parameters are actually the medium that transfers electrical and process parameters from wafer fab into a design environment. Inaccurate device models reduce the possibility of having a working design on silicon wafers.

Device models provided by wafer fab are typically in SPICE format, since SPICE simulator is generally the industry standard for accurate circuit simulations. Transistor models are further divided into several types such as threshold-based, inversion charge-based and surface potential-based models, depending on how the mathematical equations are derived to represent different modeling approaches. Industry standard Berkeley Short Channel IGFET Model (BSIM) such as BSIM3 and BSIM4 are examples of threshold-based models. ACM and EKV models fall under inversion charge-based models while PSP and HISIM models are examples of surface potential-based models. Although these models are identified differently with respect to their modeling approaches, they are actually identical with regards to the usage of measurement data. The common feature between these models is that the list of model parameters are actually extracted from the same experimental data namely transfer and output characteristic curves.

Transfer characteristic curve refers to drain current (I_d) versus gate voltage (V_g) plot while output characteristic curve refers to drain current (I_d) versus drain voltage (V_d) plot. Since the accuracy of the models rely mainly on mainstream research and development, most available literature focus on sophisticated and adventurous model parameter extraction methods and are not directed to issues pertaining to inconsistencies in experimental data.

Reliable measurement data is vital for accurate model extraction as well as for ease of parameter extraction. For a device or technology under development, such as in research and development (R & D) laboratories, the collected data is mostly measured from different samples at different times and under varying conditions. When the experimental data is still under engineering and prone to modification, researchers tend to inadvertently provide such inconsistent data to the device modeling engineer for model parameter extraction purposes. The unreliable measurement data provided lengthens the model extraction cycle and invariably results in inaccurate models that fail at the final model verification stage further contributing to a delay in the device or technology development. There is a high probability that even after several changes of the fabricated samples, the final stage of model verification is still unsuccessful, thus wasting a lot of time and effort.

There are several methods disclosed in the art with respect to quality assurance of the extracted device models, in terms of measurement and extraction accuracy as well as for different applications from digital and analog to mixed signal and radio frequency (RF). Unfortunately, the reports usually rely on the assumption that the measurement data provided is reliable and consistent. Although, such an assumption may be true, situations when measured data suffering from discrepancy and inconsistency issues jeopardize the further step of model parameter extraction stage cannot be ruled out.

Therefore, there is a need to bridge the gap between wafer fab and the integrated circuit design in a manner wherein human intervention is minimal, handling of large volume of varying data is facilitated precisely and most importantly any inconsistency in the experimental data is detected at the outset to eliminate unnecessary process loops and waste of time, effort and money.

SUMMARY

Model parameter extraction for transistor modeling relies on experimental data provided and any discrepancy therein, if undetected at the outset, results in inaccurate models and delay in device/technology development. The method and

apparatus of the present disclosure addresses this problem by introducing a consistency check prior to the model extraction stage.

In accordance with an aspect of the present invention, there is provided a method for validating experimental data for model parameter extraction in transistor modeling, the method includes the steps of: retrieving the experimental data from a sample fabricated wafer, by a graph generator; plotting the experimental data to distinguish between transfer and output characteristic curves of the transistor, by the graph generator; examining electrical parameters associated with each of the transfer and output characteristic curves to search for unique points, by a consistency check unit; calculating error percentage at available unique points for consistency check, by the consistency check unit; and evaluating the result of the consistency check to validate the experimental data for model parameter extraction, by the consistency check unit.

In accordance with a second aspect of the present disclosure, there is provided an apparatus for validating experimental data for model parameter extraction in transistor modeling, the apparatus comprises: (i) a graph generator to retrieve and plot the experimental data for evaluating transfer and output characteristic curves of the transistor; and (ii) a consistency check unit to examine the transfer and output characteristic curves for unique points, calculate the error percentage at the available unique points for consistency check and evaluate the result of the consistent check to validate the experimental data for model parameter extraction.

In accordance with yet another aspect of the present disclosure, there is provided a computer program product for validating experimental data for model parameter extraction in transistor modeling, the computer program product having instructions operable to cause one or more modules to: retrieve the experimental data from a sample fabricated wafer; plot the experimental data to distinguish between transfer and output characteristic curves of the transistor; examine electrical parameters associated with each of the transfer and output characteristic curves to search for unique points; calculate error percentage at available unique

points for consistency check; and evaluate the result of the consistency check to validate the experimental data for model parameter extraction.

In accordance with still another aspect of the present disclosure, there is provided a computer program product for model parameter extraction in transistor modeling, the computer program product being tangibly implemented on a machine readable media and comprises: a graph generator to retrieve and plot the experimental data for evaluating transfer and output characteristic curves of the transistor; and a consistency check unit to examine the transfer and output characteristic curves for unique points, calculate the error percentage at the available unique points for consistency check and evaluate the result of the consistent check to validate the experimental data for model parameter extraction.

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BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

A method and apparatus for validating experimental data provided for transistor modeling, in accordance with the present disclosure will now be described with the help of the accompanying drawings, in which:

Figure 1 is a flow diagram illustrating the key steps involved in a conventional transistor modeling method;

Figures 2A through 2C are a graphical representation of the three key steps involved in transistor modeling;

Figure 3 is a flow diagram illustrating the key steps involved in the method of the present disclosure for transistor modeling;

Figure 4 is a flow diagram illustrating the key steps involved in the method for validating experimental data provided for transistor modeling, in accordance with the present disclosure;

Figure 5 is a flow diagram illustrating the key steps involved in the method of plotting the experimental data to distinguish between transfer and output characteristic curves, in accordance with the present disclosure;

Figure 6 is a flow diagram illustrating the key steps involved in the method of examining electrical parameters associated with the characteristic curves to search for unique points, in accordance with the present disclosure;

Figure 7 is a graphical representation of unique points identified in I_d versus V_d and I_d versus V_g curves, in accordance with the present disclosure; and

Figure 8 is a block diagram illustrating an apparatus for validating experimental data provided for transistor modeling, in accordance with the present disclosure.

DETAILED DESCRIPTION

Figure 1 is a flow diagram illustrating the key steps involved in a conventional transistor modeling method. A typical transistor modeling method includes three important stages namely electrical measurements, model parameter extraction and model verification as illustrated. The extraction flow starts with acquiring measurement data (1002) from a sample fabricated wafer (1000) which represents the experimental data. Transfer (1006) and output (1004) characteristic curves are derived from the experimental data. These characteristic curves are required for model parameter extraction (1008). Various transfer and output characteristic curves are derived based on experimental data obtained from varying transistor geometries which further results in a significant increase in the electrical measurement data. The output characteristics based on measured data are generally represented as illustrated in Fig. 2A. Model parameters are extracted from the exhaustive list of characteristic curves. Also, simulated characteristic curves are generated using circuit simulators. The output characteristics based on measured and simulated data are generally represented as illustrated in Fig. 2B. Then the process progresses to the model verification stage (1010) where simulated curves (continuous lines) are compared with the actual measured curves and it is recommended to have a close fit between the two types of characteristic curves. The model is ready (1012) to be released to the users once the error between the measured and simulated curves (continuous lines) are within pre-determined acceptable limits, as illustrated generally in Fig. 2C. If the two curves do not exhibit a close fit, the process continues to be executed in loops with optimization of certain model parameters in the model parameter extraction stage. The optimization continues until the simulated curves satisfactorily fit the measured curves. But if the curve fit is still not satisfactory, then

the modeling flow needs to return back to the measurement of electrical parameters to acquire new measurement data from other reliable samples. The electrical parameters typically include drain current (I_d) and the applied bias voltages including gate voltage (V_g), drain voltage (V_d) and bulk voltage (V_b).

In the prior art, any discrepancy between transfer and output characteristic curves could only be detected at a later stage of model verification since smooth transition is always expected from electrical measurement to model parameter extraction stage. However, the method and apparatus of the present disclosure addresses this problem by identifying discrepancy, if any, as early as the first step of electrical measurement.

The method and apparatus for validating experimental data provided for transistor modeling, of the present disclosure will now be described with reference to the embodiment shown in the accompanying drawings. The embodiment does not limit the scope and ambit of the disclosure. The description relates purely to the exemplary embodiment and its suggested applications.

The embodiment herein and the various features and advantageous details thereof are explained with reference to the non-limiting embodiment in the following description. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the embodiments herein. The examples used herein are intended merely to facilitate an understanding of ways in which the embodiment herein may be practiced and to further enable those of skill in the art to practice the embodiment herein. Accordingly, the description should not be construed as limiting the scope of the embodiment herein.

The description herein after, of the specific embodiment will so fully reveal the general nature of the embodiments herein that others can, by applying current knowledge, readily modify and/or adapt for various applications such specific embodiment without departing from the generic concept, and, therefore, such adaptations and modifications should and are intended to be comprehended within the meaning and range of equivalents of the disclosed embodiments. It is to be understood that the phraseology or terminology employed herein is for the purpose of description and not of limitation.

Figure 3 is a flow diagram illustrating the key steps involved in the transistor modeling method of the present disclosure. The method, in accordance with the present disclosure introduces an additional consistency check of electrical measurement data for a transistor, namely between transfer and output characteristic curves so that any discrepancy is identified earlier, before the model parameter extraction stage.

Figure 4 is a flow diagram illustrating the key steps involved in the method for validating experimental data provided for transistor modeling, viz.,

(i) retrieving the experimental data from a sample fabricated wafer, by a graph generator (4000);

(ii) plotting the experimental data to distinguish between transfer and output characteristic curves of the transistor, by the graph generator (4002);

(iii) analyzing electrical parameters associated with each of the transfer and output characteristic curves to search for unique points, by a consistency check unit (4004);

(iv) calculating error percentage at available unique points for consistency check, by the consistency check unit (4006); and

(v) evaluating the result of the consistency check to validate the experimental data for model parameter extraction, by the consistency check unit (4008).

It is essential to firstly confirm that the transfer and output characteristic curves are derivable from the available experimental data. The step of retrieving the experimental data may be performed by any known computational method in the art.

Figure 5 is a flow diagram illustrating the key steps involved in the method of plotting the experimental data to distinguish between transfer and output characteristic curves, viz.,

(i) loading at least two sets of experimental data, obtained from a single transistor geometry using discrete measurement setups, into the graph generator, wherein the experimental data comprises drain current (I_d) associated with applied bias voltages including gate voltage (V_g), drain voltage (V_d) and bulk voltage (V_b) (5000);

(ii) checking the graphs generated by the graph generator to identify transfer and output characteristic curves, wherein the transfer and output characteristics relate drain current (I_d) responses to gate voltage (V_g) and drain voltage (V_d) respectively (5002);

(iii) iteratively performing the step of retrieving the experimental data, if the two sets of experimental data do not produce the transfer and output characteristic curves (5004); and

(iv) proceeding to the step of examining electrical parameters associated with each of the transfer and output characteristic curves to search for unique points, if the two sets of experimental data produce the transfer and output characteristic curves (5006).

Transfer characteristic curve shows the drain current (I_d) variations as a function of gate voltage (V_g) while output characteristic curve illustrates the drain current (I_d) variations as a function of drain voltage (V_d). Transfer characteristic or I_d - V_g curve is required for the extraction of basic model parameters such as mobility, threshold voltage and drain current. For a BSIM3 model, the SPICE parameters for mobility characteristic are represented by the parameters U0, UA, UB and UC. For the same BSIM3 model, the SPICE parameters for threshold voltage characteristics are represented by the parameters VTH0, K1 and K2 while VOFF and NFACTOR are the SPICE parameters for drain current characteristics. Output characteristic or I_d - V_d curve is required for the extraction of output resistance behaviors such as the SPICE parameters of VSAT, PCLM, ALPHA0, BETA0 and PDIBLC1 in BSIM3 model.

Figure 6 is a flow diagram illustrating the key steps involved in the method of examining electrical parameters associated with the characteristic curves to search for unique points, viz.,

(i) reading the experimental data associated with each of the transfer and output characteristic curves for discrete analysis (6000);

(ii) sorting the experimental data associated with each of the transfer and output characteristic curves, by electrical parameters, to differentiate between drain current (I_d) and the applied bias voltages including gate voltage (V_g), drain

voltage (V_d) and bulk voltage (V_b) to form a list associated with each experimental data (6002);

(iii) searching the list associated with each experimental data for unique points, wherein unique points share identical values for all applied bias voltages (6004);

(iv) iteratively performing the step of retrieving the experimental data, if the two sets of experimental data do not contain any unique point; and

(v) storing respective drain current (I_d) at each unique point to proceed with the step of calculating error percentage, if the two sets of experimental data contain unique points (6006).

The discrete analysis may be performed by any known algorithm / logic known in the art.

The experimental data is provided using any readable format such as ASCII or text file and are then sorted out by electrical parameters of voltage and current.

The table below shows an example of sorted readable measurement data where it contains several terminal biases, particularly for gate voltage (V_g), drain voltage (V_d) and bulk voltage (V_b) as well as related measured drain current (I_d).

I_d -V_g			
Bulk Voltage (V_{b1})	Drain Voltage (V_{d1})	Gate Voltage (V_{g1})	Drain Current (I_{d1})
V_{b1a}	V_{d1a}	V_{g1a}	I_{d1a}
V_{b1b}	V_{d1b}	V_{g1b}	I_{d1b}
V_{b1c}	V_{d1c}	V_{g1c}	I_{d1c}
V_{b1d}	V_{d1d}	V_{g1d}	I_{d1d}
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I_d-V_d			
Bulk Voltage (V_{b2})	Drain Voltage (V_{d2})	Gate Voltage (V_{g2})	Drain Current (I_{d2})
V_{b2a}	V_{d2a}	V_{g2a}	I_{d2a}

V_{b2b}	V_{d2b}	V_{g2b}	I_{d2b}
V_{b2c}	V_{d2c}	V_{g2c}	I_{d2c}
V_{b2d}	V_{d2d}	V_{g2d}	I_{d2d}
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Figure 7 is a graphical representation of unique points identified in the Transfer (I_d versus V_d) and Output (I_d versus V_g) characteristic curves. In accordance with the present disclosure, as a consistency check tool for the provided experimental data, the transfer and output characteristic curves of the transistor are analyzed discretely. The characteristic curves are actually the typical measurement data obtained during DC operation of any transistor, such as metal oxide semiconductor transistor (MOSFET), ion sensitive field effect transistor (ISFET) or carbon nanotube field effect transistor (CNTFET). In the search for unique points, only the values of applied bias voltages in both the transfer and output characteristic curves are studied. A unique point refers to the point where all the applied bias voltages share the same values. Particularly for the purpose of transistor model extraction, the combination of I_d - V_g and I_d - V_d curves is analyzed for some common test setups. The 7 nos. I_d –V_g curves illustrated in Figure 7, as an exemplary embodiment, are generated as a function of bulk voltage (V_b), starting from 0V through 3.3V in steps of 0.55V. The unique points are identified such that all biased voltages (V_g, V_d and V_b) must share the same values. Therefore if a unique point is not detected, then the analysis needs to be stopped and checked for data mismatch issues. Once unique points are identified for the experimental data provided, the process continues with reading and saving of the related drain current (I_d) values for the next stage of consistency check.

In accordance with the present disclosure, the consistency check between two drain currents (I_d) at any unique point is executed by calculating error percentage at available unique points as a drain current (I_d) difference between a transfer characteristic data and an output characteristic data divided by the drain current of respective transfer characteristic data and multiplied by 100. The

computed error percentage is further evaluated based on a pre-determined acceptable level of drain current (I_d) error percentage permissible at the final stage of model verification during curve-fit of the measured and simulated curves. An exemplary value for the acceptable level of error percentage is 2%, particularly in relation to stringent accuracy requirements for analog mixed signal applications. Alternatively, an acceptable level may vary within a pre-determined range of values, for instance, 2% to 5% depending on the tool used for model parameter extraction, permitted accuracy by users and instrument resolution during data collection.

Figure 8 is a block diagram illustrating an apparatus (100) for validating experimental data provided for transistor modeling, in accordance with the present disclosure. A set of computer instructions forms the apparatus (100) of the present disclosure, for plotting experimental data, analyzing the generated characteristic curves and conclusively indicating whether the experimental data is appropriate for proceeding to the step of model extraction.

The apparatus (100), of the present disclosure, for validating experimental data provided for model extraction in transistor modeling includes a graph generator (10) and a consistency check unit (12) as illustrated. The graph generator (10) retrieves at least two sets of experimental data (ExD1 and ExD2) from a sample fabricated wafer and plots transfer (T/F) and output (O/P) characteristic curves of the transistor. For a scalable transistor model, experimental data corresponding to different transistor length (L) and width (W) accurately simulate the characteristic curves at different transistor (T1, T2, T3, T4) geometries. The graph generator (10) is adapted to handle large volume of varying experimental data. For instance, data corresponding to several temperature nodes at room temperature, hot and cold temperatures is accurately handled for executing model parameter extraction with respect to temperature variations.

The consistency check unit (12) evaluates the suitability of experimental data based on calculation of acceptable level of error percentage for further model parameter extraction.

For two sets of experimental data that contain bias voltages, if the acceptable level of error percentage in drain current (I_d) is pre-determined as 2%, a calculated error percentage of more than 2% is considered as a failed output and accordingly, the apparatus and the method of the present disclosure restrains the process from proceeding to the next step of model parameter extraction. Experimental data with calculated error percentage equal to or less than 2% is considered as a passed output and the apparatus and the method of the present disclosure deems the experimental data to be suitable and permits the process to proceed to the next step of model parameter extraction.

Factors that may contribute to data inconsistency include instrument errors and measurement of data from different samples. In order to eliminate discrepancy due to different samples, the device modeling engineer needs to ensure that both I_d - V_g and I_d - V_d curves are measured from the same sample and within a short span of time. To eliminate instrument errors, where researchers are unable to provide consistent data even by using the same sample, the device modeling engineer may consider changing the instrument measurement integration time such as from short to medium or medium to large for further refinement of time required at each measurement steps.

Early detection of data disagreement by the method and apparatus of the present invention helps to remove any unnecessary looping procedures which consequently accelerate the time for further extraction of semiconductor device models.

The technical / economical advancements offered by one or more aspects of the method and apparatus for validating experimental data provided for transistor modeling, of the present disclosure, include the realization of:

- scalable transistor models obtained by processing a plurality of varying transistor geometries;
- reduction of device or technology development cycle with no time being wasted on processing unreliable data;
- automated process with no human intervention; and

- minimized data overlook and ensured accuracy irrespective of the volume of experimental data.

The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting. As used herein, the singular forms "a", "an" and "the" may be intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms "comprises," "comprising," “including,” and “having,” are inclusive and therefore specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. The method steps, processes, and operations described herein are not to be construed as necessarily requiring their performance in the particular order discussed or illustrated, unless specifically identified as an order of performance. It is also to be understood that additional or alternative steps may be employed.

The use of the expression “at least” or “at least one” suggests the use of one or more elements, as the use may be in one of the embodiments to achieve one or more of the desired objects or results.

Wherever a range of values is specified, a value up to 10% below and above the lowest and highest numerical value respectively, of the specified range, is included in the scope of the disclosure.

The numerical values mentioned for the various physical parameters, dimensions or quantities are only approximations and it is envisaged that the values higher/lower than the numerical values assigned to the parameters, dimensions or quantities fall within the scope of the disclosure, unless there is a statement in the specification specific to the contrary.

CLAIMS

1. A method for validating experimental data provided for model parameter extraction in transistor modeling, characterized in the following steps:
   (i) retrieving the experimental data from a sample fabricated wafer, by a graph generator (10);
   (ii) plotting the experimental data to distinguish between transfer and output characteristic curves of the transistor, by the graph generator (10);
   (iii) examining electrical parameters associated with each of the transfer and output characteristic curves to search for unique points, by a consistency check unit (12);
   (iv) calculating error percentage at available unique points for consistency check, by the consistency check unit (12); and
   (v) evaluating result of the consistency check to validate the experimental data for model parameter extraction, by the consistency check unit (12).

2. A method according to claim 1, wherein the step of plotting the experimental data comprises the following steps:
   (i) loading at least two sets of experimental data, obtained from a single transistor geometry using discrete measurement setups, into the graph generator, wherein the experimental data comprises drain current (I_d) associated with applied bias voltages including gate voltage (V_g), drain voltage (V_d) and bulk voltage (V_b);
   (ii) checking the graphs generated by the graph generator to identify transfer and output characteristic curves, wherein the transfer and output characteristics relate drain current (I_d) responses to gate voltage (V_g) and drain voltage (V_d) respectively;
   (iii) iteratively performing the step of retrieving the experimental data, if the two sets of experimental data do not produce the transfer and output characteristic curves; and

(iv) proceeding to the step of examining electrical parameters associated with each of the transfer and output characteristic curves to search for unique points, if the two sets of experimental data produce the transfer and output characteristic curves.

3. A method according to claim 1, wherein the step of examining electrical parameters comprises the following steps:
   (i) reading the experimental data associated with each of the transfer and output characteristic curves for discrete analysis;
   (ii) sorting the experimental data associated with each of the transfer and output characteristic curves, by electrical parameters, to differentiate between drain current (I_d) and the applied bias voltages including gate voltage (Vg), drain voltage (V_d) and bulk voltage (V_b) to form a list associated with each experimental data;
   (iii) searching the list associated with each experimental data for unique points, wherein unique points share identical values for all applied bias voltages;
   (iv) iteratively performing the step of retrieving the experimental data, if the two sets of experimental data do not contain any unique point; and
   (v) storing respective drain current (I_d) at each unique point to proceed with the step of calculating error percentage, if the two sets of experimental data contain unique points.

4. A method according to claim 1, wherein the step of calculating error percentage at available unique points is computed as a drain current (I_d) difference between a transfer characteristic data and an output characteristic data divided by the drain current of respective transfer characteristic data and multiplied by 100.

5. A method according to claim 1, wherein the step of evaluating the result of the consistency check comprises the step of determining an acceptable level of drain current (I_d) error percentage at unique points.

6. A method according to claim 5, wherein the step of determining an acceptable level during consistency check further comprises:
   (i) defining the consistency check as failed if drain current error percentage is higher than 2%; and
   (ii) defining the consistency check as passed if drain current error percentage is lower than 2%.

7. An apparatus (100) for validating experimental data provided for model parameter extraction in transistor modeling comprises:
   (i) a graph generator (10) adapted to retrieve and plot the experimental data for evaluating transfer and output characteristic curves of the transistor; and
   (ii) a consistency check unit (12) adapted to examine the transfer and output characteristic curves for unique points, calculate the error percentage at the available unique points for consistency check and evaluate the result of the consistent check to validate the experimental data for model parameter extraction.

8. An apparatus according to claim 7, wherein the graph generator (10) is adapted to process experimental data associated with a plurality of varying transistor geometries for generating a scalable transistor model.

9. A computer program product for validating experimental data provided for model parameter extraction in transistor modeling, characterized by instructions operable to cause one or more modules to,
   (i) retrieve the experimental data from a sample fabricated wafer;
   (ii) plot the experimental data to distinguish between transfer and output characteristic curves of the transistor;
   (iii) examine electrical parameters associated with each of the transfer and output characteristic curves to search for unique points;
   (iv) calculate error percentage at available unique points for consistency check; and

(v) evaluate the result of the consistency check to validate the experimental data for model parameter extraction.

10. A computer program product for validating experimental data provided for model parameter extraction in transistor modeling, said computer program product being tangibly implemented on a machine readable media, characterized in that it comprises:

(i) a graph generator (10) adapted to retrieve and plot the experimental data for evaluating transfer and output characteristic curves of the transistor; and

(ii) a consistency check unit (12) adapted to examine the transfer and output characteristic curves for unique points, calculate the error percentage at the available unique points for consistency check and evaluate the result of the consistent check to validate the experimental data for model parameter extraction.

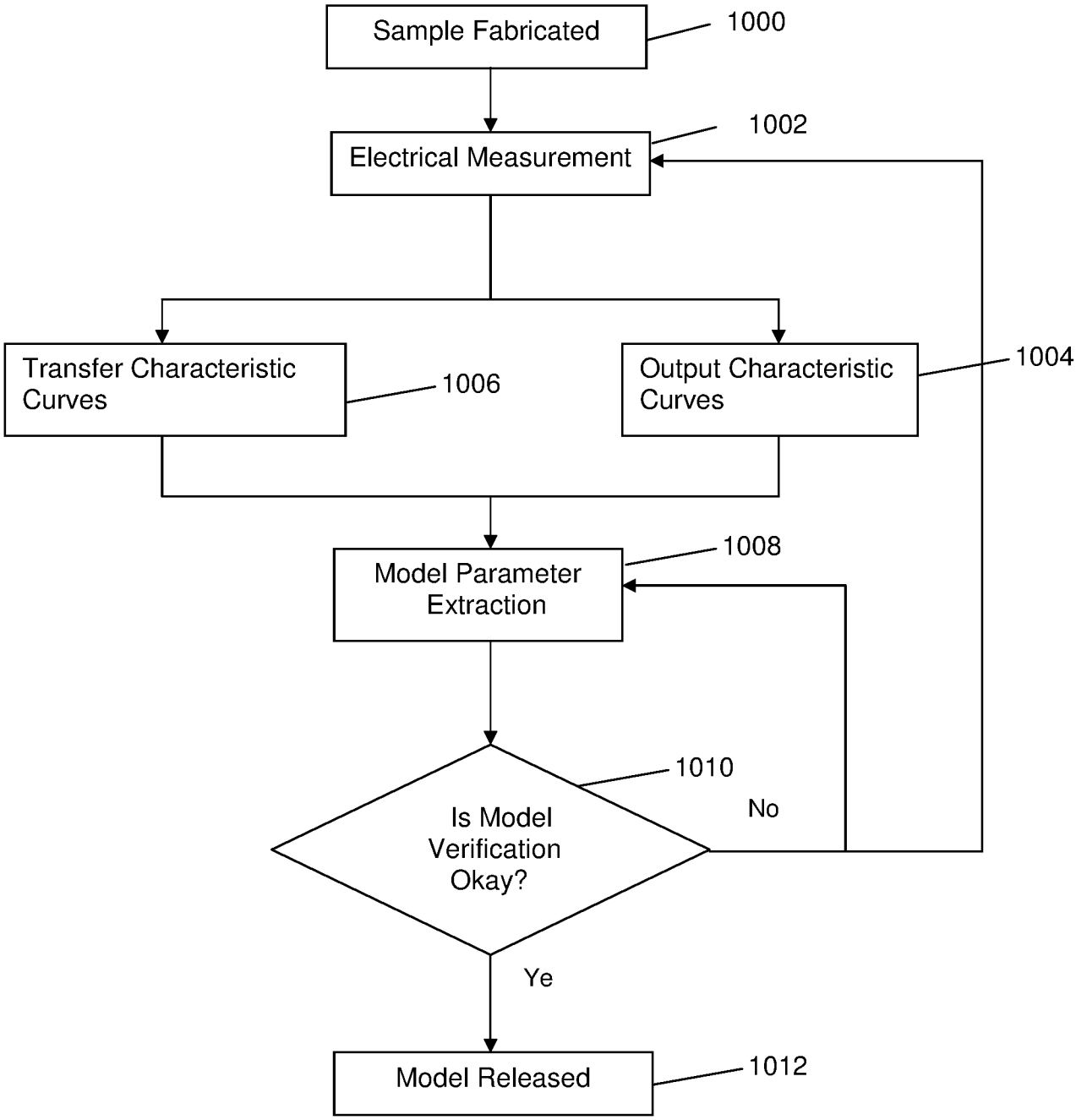

FIG. 1 (PRIOR ART)

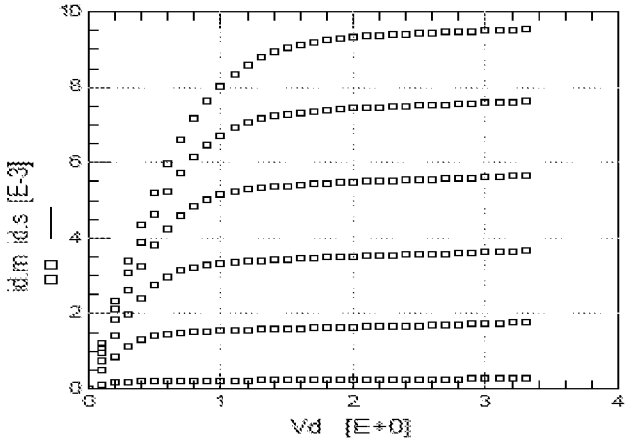

FIG.2A

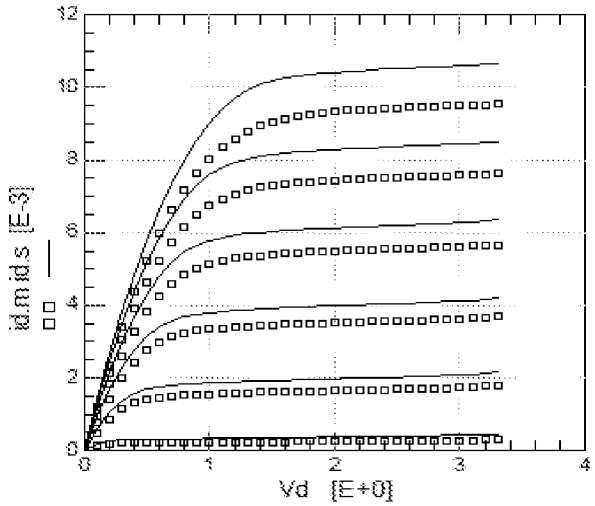

FIG.2B

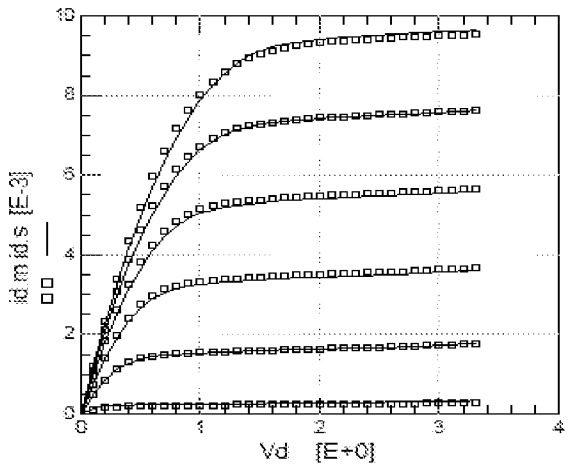

FIG.2C

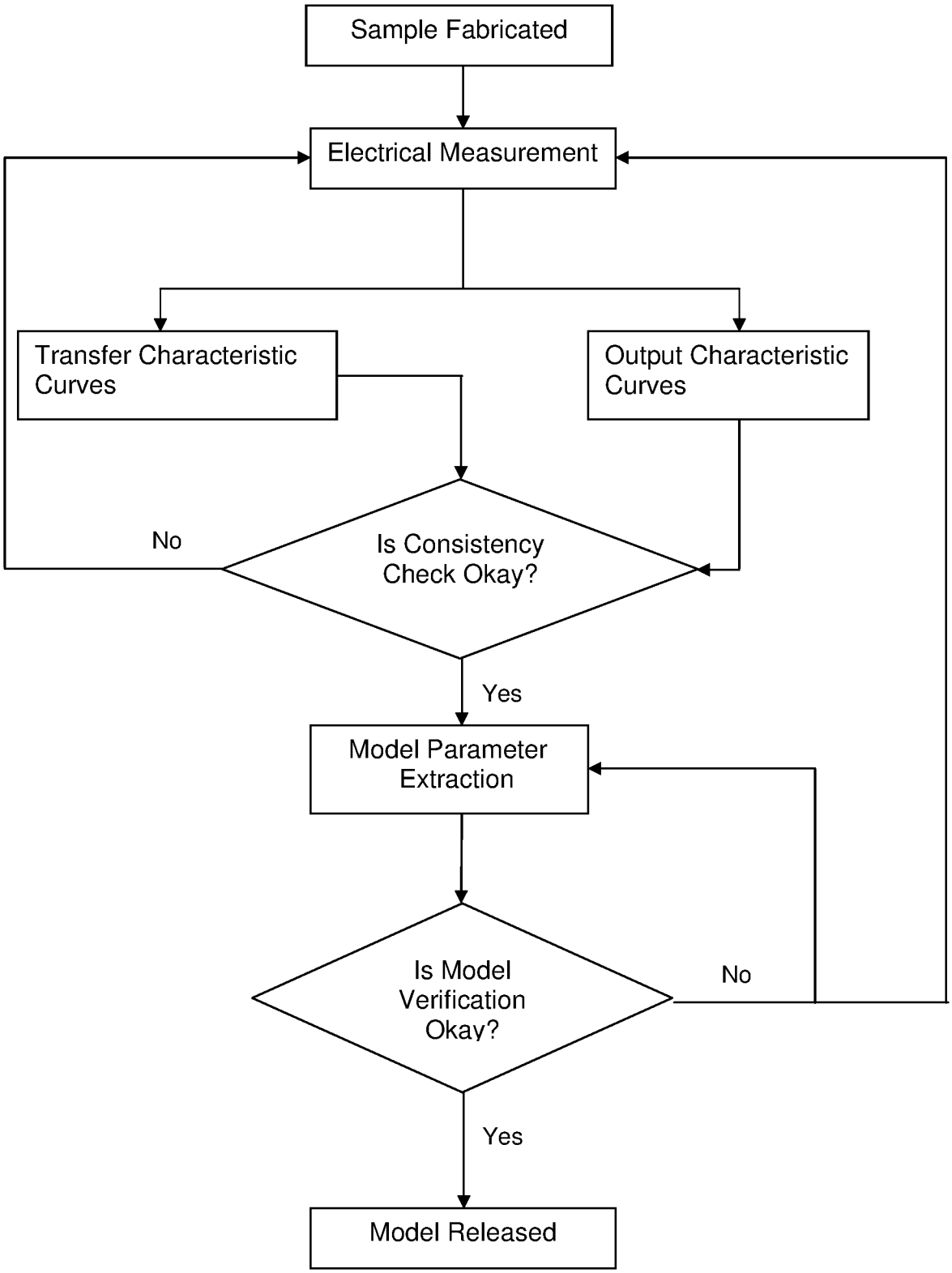
Sample Fabricated
Electrical Measurement
Transfer Characteristic Curves
Output Characteristic Curves
Is Consistency Check Okay?
No
Yes
Model Parameter Extraction
Is Model Verification Okay?
No
Yes
Model Released

FIG.3

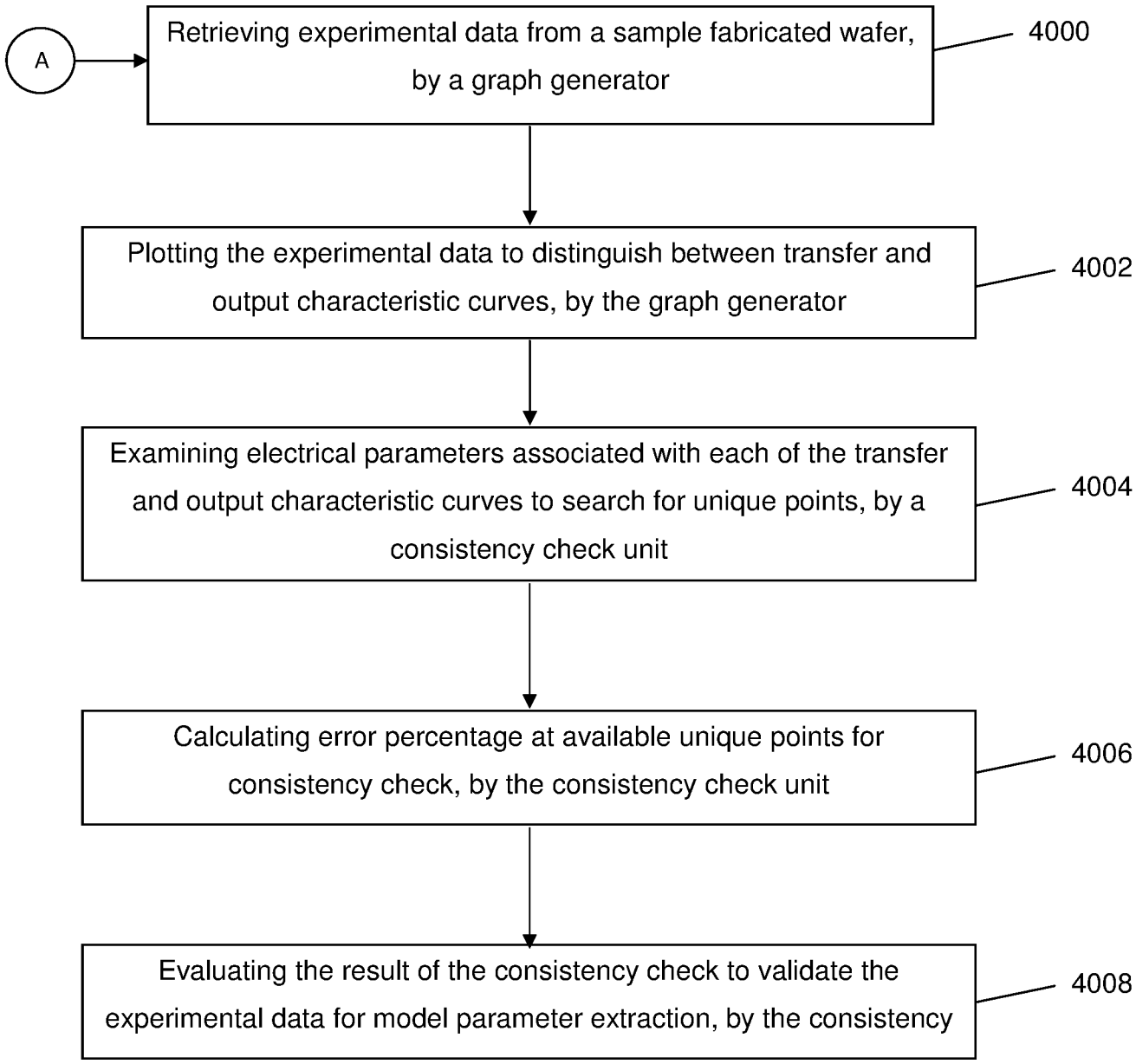
A
Retrieving experimental data from a sample fabricated wafer, by a graph generator
4000
Plotting the experimental data to distinguish between transfer and output characteristic curves, by the graph generator
4002
Examining electrical parameters associated with each of the transfer and output characteristic curves to search for unique points, by a consistency check unit
4004
Calculating error percentage at available unique points for consistency check, by the consistency check unit
4006
Evaluating the result of the consistency check to validate the experimental data for model parameter extraction, by the consistency
4008

FIG.4

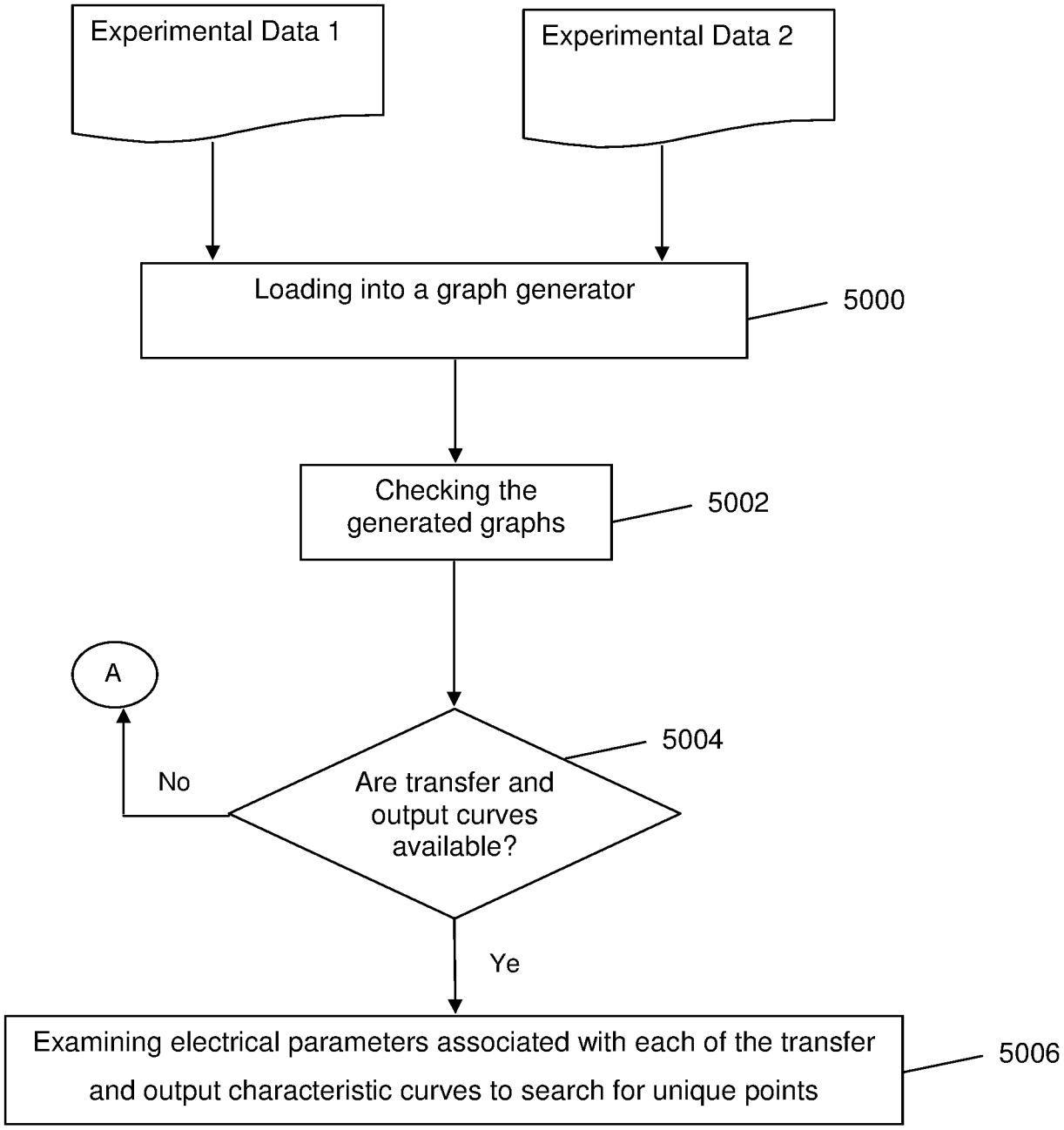
Experimental Data 1
Experimental Data 2
Loading into a graph generator
5000
Checking the generated graphs
5002
A
5004
No
Are transfer and output curves available?
Ye
Examining electrical parameters associated with each of the transfer and output characteristic curves to search for unique points
5006

FIG.5

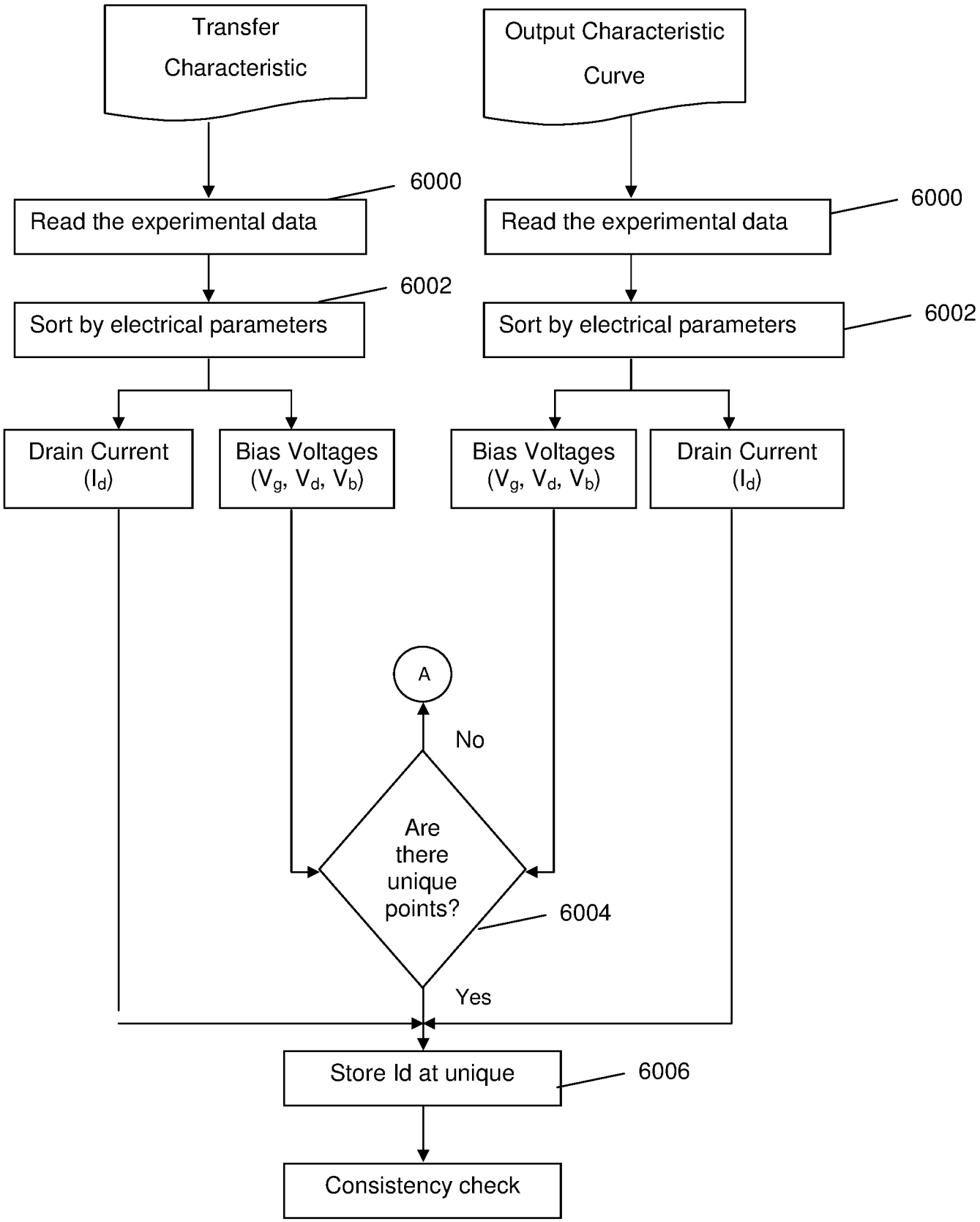
Transfer Characteristic
Output Characteristic Curve
6000
Read the experimental data
6000
Read the experimental data
6002
Sort by electrical parameters
6002
Sort by electrical parameters
Drain Current (I_d)
Bias Voltages (V_g, V_d, V_b)
Bias Voltages (V_g, V_d, V_b)
Drain Current (I_d)
A
No
Are there unique points?
6004
Yes
Store Id at unique
6006
Consistency check

FIG.6

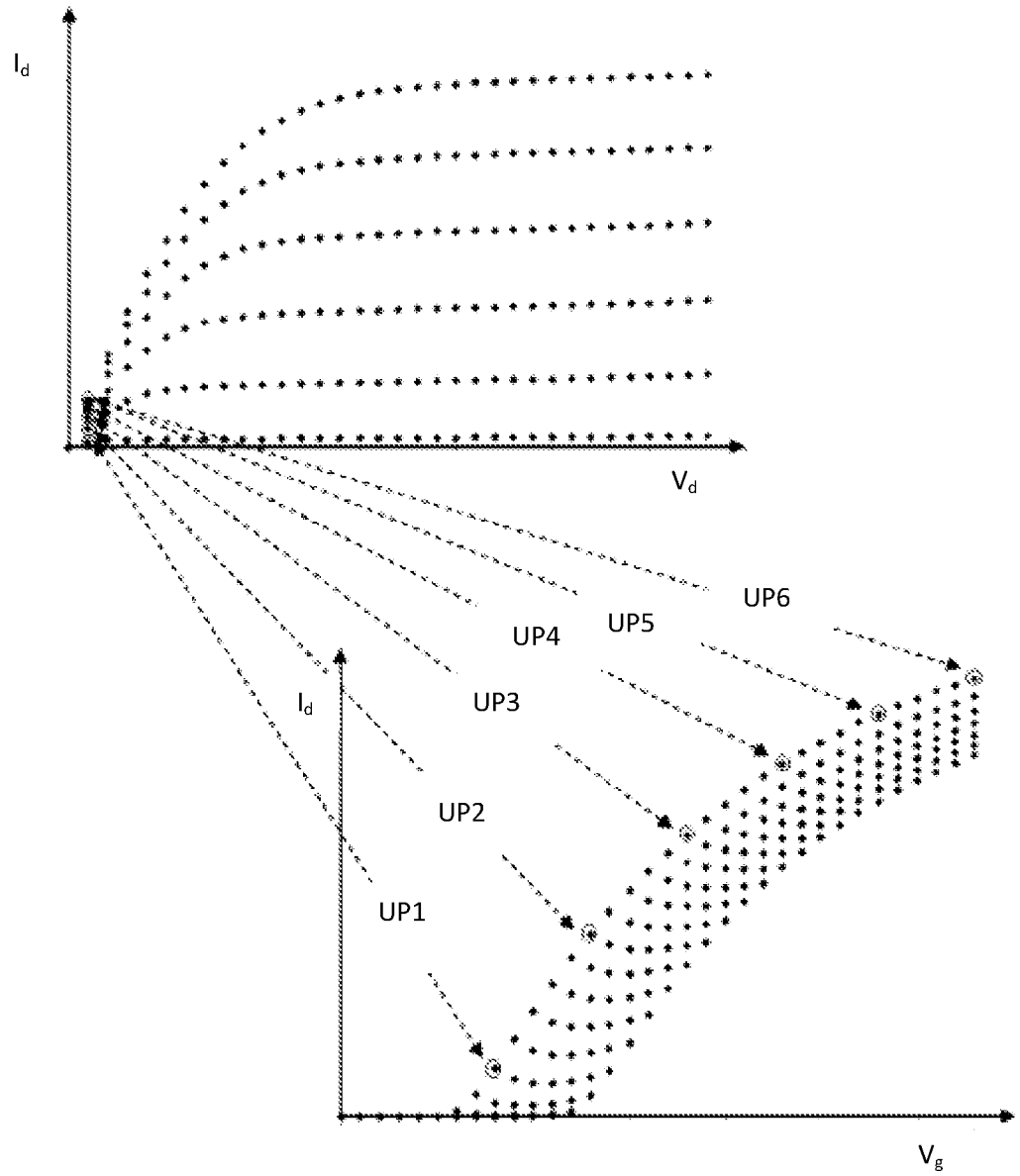

FIG.7

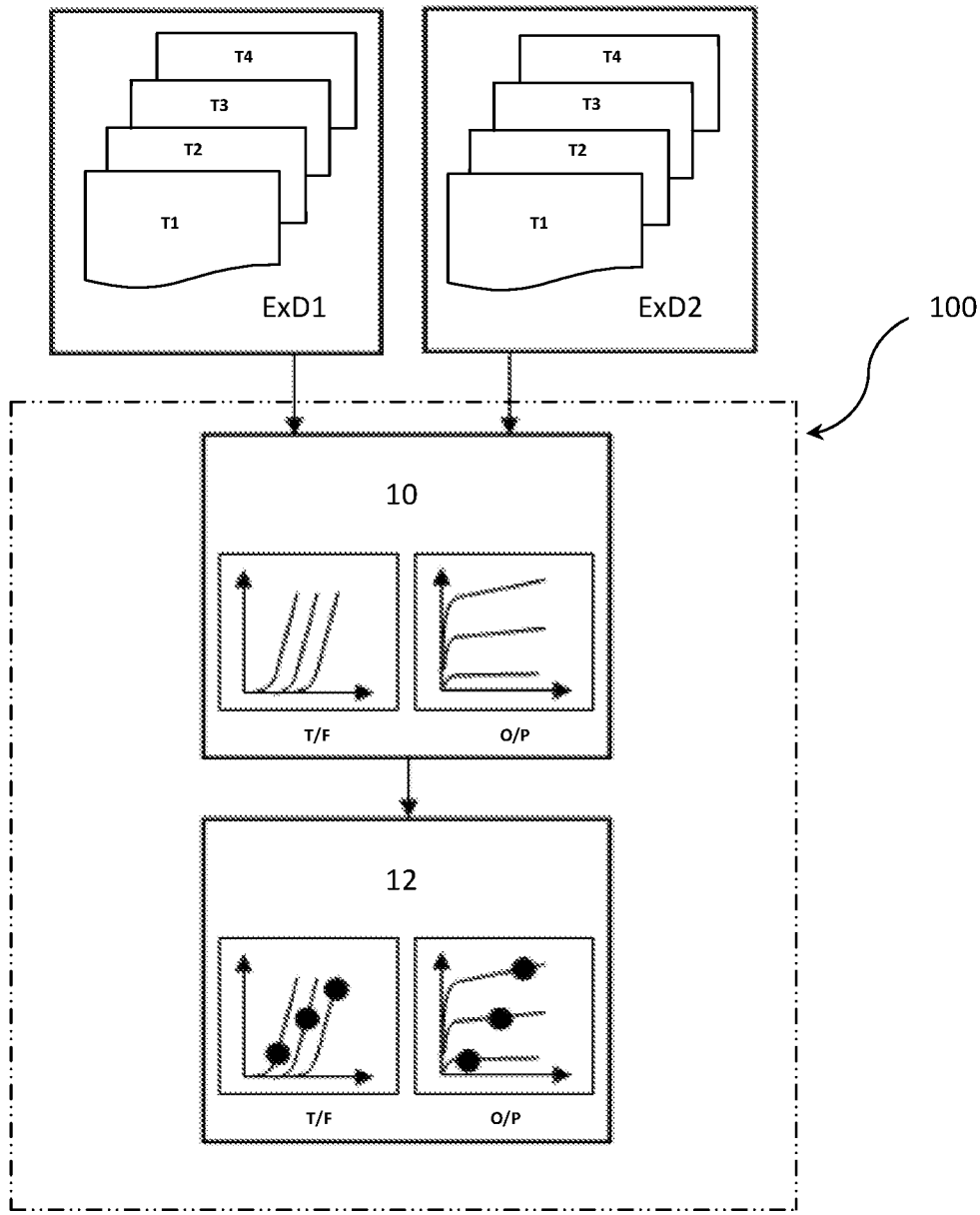

FIG.8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2015/055345

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L29/00(2006.01)i, H01L21/00(2006.01)i, H01L21/336(2006.01)i, H01L21/82(2006.01)i, H01L29/78(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/00, H01L21/00, H01L21/336, H01L21/82, H01L29/78, G06F17/50

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2015
Registered utility model specifications of Japan 1996-2015
Published registered utility model applications of Japan 1994-2015

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2002-124666 A (MATSUSHITA DENKI SANGYO KK) 2002.04.26, paragraphs [0001], [0023], Figure 4 (No Family)	1-10
A	JP 10-65159 A (SHARP KK) 1998.03.06, paragraphs [0001], [0023]-[0026], Figure 4 (No Family)	1-10

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29.09.2015	13.10.2015

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