

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
20 October 2005 (20.10.2005)

PCT

(10) International Publication Number
WO 2005/099088 A1

(51) International Patent Classification⁷: **H03H 9/05**,
9/10, 9/64

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(21) International Application Number:
PCT/US2005/009887

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(22) International Filing Date: 24 March 2005 (24.03.2005)

(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,
GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,
KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD,
MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG,
PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ,
TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA,
ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/556,812 26 March 2004 (26.03.2004) US

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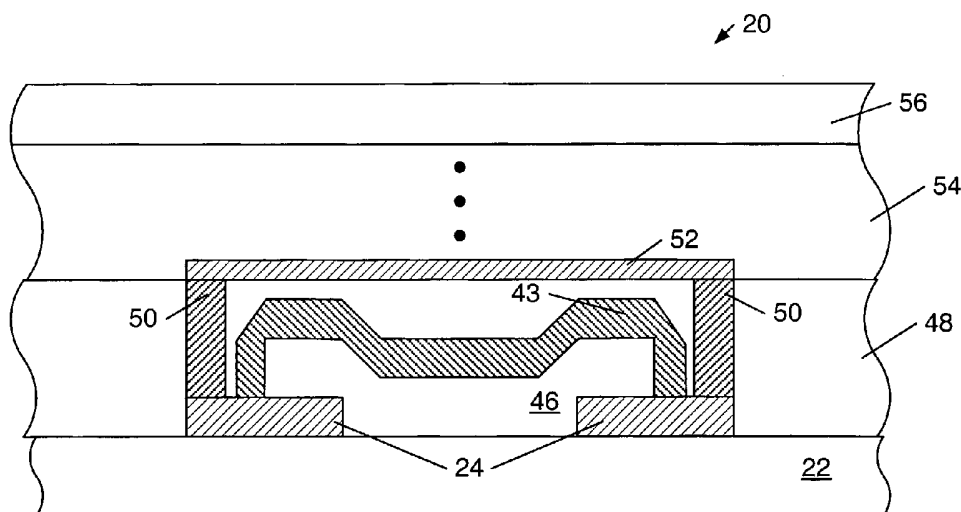
(84) Designated States (*unless otherwise indicated, for every
kind of regional protection available*): ARIPO (BW, GH,
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,
FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO,

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[Continued on next page]

(54) Title: INTEGRATED CIRCUIT HAVING ONE OR MORE CONDUCTIVE DEVICES FORMED OVER A SAW AND/OR MEMS DEVICE



(57) Abstract: An integrated circuit is provided which includes one or more device elements (24) formed above a base substrate (22), a structure (43) forming a sealed cavity (44) above at least a portion of the one or more device elements (24), and one or more conductive devices (52) formed above the sealed cavity (44). A method for fabrication of such an integrated circuit is also provided. An exemplary embodiment of the integrated circuit includes a surface acoustic wave device having a plurality of tracks each with a first interdigitated transducer configured to convert a receiving electric field energy into mechanical wave energy and a second interdigitated transducer configured to convert the mechanical wave energy into an output electric field energy. The SAW device also includes a conductor arranged above and spanning across at least two tracks of the plurality of tracks and coupled to the first interdigitated transducers of at least the two tracks.



SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, — *with amended claims and statement*
GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

TITLE: INTEGRATED CIRCUIT HAVING ONE OR MORE CONDUCTIVE DEVICES FORMED OVER A SAW AND/OR MEMS DEVICE**BACKGROUND OF THE INVENTION****1. Field of the Invention**

5 The present invention relates generally to microelectronic device fabrication and, more particularly, the fabrication of a SAW device and/or a MEMS device having one or more conductive devices formed thereover.

2. Description of the Related Art

The following descriptions and examples are given as background information only.

10 Microelectronic devices have been developed for a diversity of applications using a variety of technologies. Some exemplary microelectronic devices include surface acoustic wave (SAW) devices and micro electro-mechanical system (MEMS) devices. SAW devices exploit the propagation properties of waves along the surface or the near surface of a substrate. Changes in velocity and/or amplitude of the waves correlate to physical parameters and, therefore, may be monitored to serve as a sensor. SAW devices are often used as bandpass filters in
15 communication devices, such as mobile phone handsets and communication networks, for example. Other applications of SAW devices include but are not limited to torque sensors, pressure sensors, humidity sensors and temperature sensors. MEMS devices integrate electro-mechanical functions using mechanical moving structures formed upon wafers. MEMS devices are of interest in part because of their potential for providing miniaturized sensors and actuators and performing functions not done or poorly done by technologies including fixed structures
20 formed upon semiconductor wafers. Examples of MEMS devices include but are not limited to switching devices used in optical telecommunications cables and sensing devices used to control the deployment of airbags in automobiles.

One challenge associated with both SAW and MEMS devices is that free areas are needed for the mechanical properties of the devices. Because of this restriction, other conductors and devices cannot be easily
25 formed above SAW or MEMS devices. Consequently, SAW or MEMS devices are generally not integrated on the same chip with other conductive structures. Rather, additional conductors or circuits are generally formed external to the substrate upon which a SAW or MEMS device is fabricated and are often formed external to the device package. In cases in which additional conductors or circuits are fabricated on the same chip as SAW or MEMS devices, the additional devices must be laterally disposed across the chip, leading to undesirably large die sizes.
30 Another predicament with SAW and MEMS devices is that the active regions of the devices can be very sensitive to the presence of surface contaminants. Surface contaminants may, for example, alter the wave velocities of a SAW device or modify the voltage level at which a moving part with a MEMS device is brought into contact or released from a contact pad. As a consequence, device performance may be degraded for the SAW device or MEMS device. Even a monolayer of contaminant on the surface of a SAW or MEMS device can noticeably alter device
35 performance.

Accordingly, it would be beneficial to develop an architecture which includes a SAW and/or MEMS device integrally fabricated with one or more other conductive devices on a single substrate and which does not require an undesirably large die size. In addition, it would be advantageous to inhibit the formation of contaminants within the active region of the SAW or MEMS device during the formation of the architecture.

SUMMARY OF THE INVENTION

The problems outlined above may be in large part addressed by an integrated circuit including a surface acoustic wave device and/or a micro electro-mechanical system device having one or more conductive devices formed thereover. The following are mere exemplary embodiments of the integrated circuit and an exemplary method of fabricating the integrated circuit and are not to be construed in any way to limit the subject matter of the claims.

One embodiment of the integrated circuit includes one or more device elements formed above a base substrate, a structure forming a sealed cavity above at least a portion of the one or more device elements, and one or more conductive devices formed above the sealed cavity.

Another embodiment of the integrated circuit includes a surface acoustic wave device having a plurality of tracks each with a first interdigitated transducer configured to convert a receiving electric field energy into mechanical wave energy and a second interdigitated transducer configured to convert the mechanical wave energy into an output electric field energy. The SAW device also includes a conductor arranged above and spanning across at least two tracks of the plurality of tracks and coupled to the first interdigitated transducers of at least the two tracks.

An embodiment of the method for fabricating the integrated circuit includes forming one or more device elements above a substrate and enclosing at least a portion of the one or more device elements within a sealed cavity. The method further includes depositing a conductive layer above the sealed cavity and patterning the conductive layer to form a conductive device above the sealed cavity.

BRIEF DESCRIPTION OF THE DRAWINGS

These and various other features and advantages of the present invention will be apparent upon reading of the following detailed description in conjunction with the accompanying drawings and the appended claims provided below, where:

Fig. 1 is a partial cross-sectional view of a topography configured for fabrication of an integrated circuit including device elements formed above a base substrate;

Fig. 2a is a partial top view of one of the device elements depicted in Fig. 1 including an interdigitated transducer of an ensuing surface acoustic wave device;

Fig. 2b is a partial cross-sectional view of one of the device elements depicted in Fig. 1 including a structure suspended above a contact pad of an ensuing micro electro-mechanical device;

Fig. 3 is a partial cross-sectional view of the topography depicted in Fig. 1 subsequent to the deposition of a sacrificial layer upon the device elements;

Fig. 4 is a partial cross-sectional view of the topography subsequent to the deposition of a sealing layer upon a patterned portion of the sacrificial layer deposited in Fig. 3;

Fig. 5 is a partial cross-sectional view of the topography subsequent to the patterning of the sealing layer deposited in Fig. 4;

Fig. 6 is a partial cross-sectional view of the topography having the patterned portion of the sacrificial layer removed subsequent to the patterning of the sealing layer in Fig. 5;

Fig. 7 is a partial cross-sectional view of the topography in which the holes in the sealing layer have been filled to form a sealed cavity and a dielectric layer has been deposited subsequent to the removal of the patterned portion of the sacrificial layer in Fig. 6;

Fig. 8 is a partial cross-sectional view of the topography subsequent to the formation of contacts within the dielectric layer deposited in Fig. 7;

Fig. 9 is a partial cross-sectional view of the topography in which a patterned conductive device has been formed above the sealed cavity subsequent to the formation of the contacts in Fig. 8;

Fig. 10 is a partial cross-sectional view of the topography in which multiple layers of conductive features and interlevel dielectric layers as well as an overlying passivation layer have been formed above the patterned conductive feature formed in Fig. 9; and

Fig. 11 is a partial top view of an exemplary surface acoustic wave device having conductive features formed over tracks of the device.

While the invention may include various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Turning to the drawings, an exemplary method for fabricating an integrated circuit including a surface acoustic wave (SAW) device and/or a micro electro-mechanical system (MEMS) device having one or more conductive devices formed thereover is provided. In particular, Figs. 1-10 depict a process in which one or more device elements of a SAW device and/or a MEMS device are formed within a sealed cavity and one or more conductive features are formed thereover. As shown in Fig. 1, topography 20 includes device elements 24 arranged upon base substrate 22. As described in more detail below, device elements 24 are general reference blocks representing one of more conductive features of a SAW device or a MEMS device. In reference thereto, it is noted that the components of topography 20 are not drawn to scale in Fig. 1 nor in Figs. 2-11. For instance, the aggregate thickness of components among each of device elements 24 may be on the order of thousands of angstroms to a few microns, while the thickness of base substrate 22 may be on the order of hundreds of microns.

For the fabrication of a SAW device, base substrate 22 may generally include a material which enables acoustic waves to travel elastically across its surface, such as lithium tantalate, lithium niobate, or single crystal quartz, for example. On the other hand, for the fabrication of MEMS devices, base substrate 22 may include a semiconductor material, such as a silicon, ceramic, or gallium arsenide. Alternatively, base substrate 22 may be glass, polyimide, metal, or any other substrate material commonly used in the fabrication of MEMS devices. In some cases, base substrate 22 may include a silicon on insulator (SOI) layer or an epitaxial silicon layer grown on a monocrystalline silicon substrate for the fabrication of MEMS devices.

In general, the composition and configuration of device elements 24 depends on the device being formed, namely a SAW device or a MEMS device. Some exemplary component configurations of device elements 24 for a SAW device and a MEMS device are shown in Figs. 2a and 2b, respectively, and described in more detail below. It is noted, however, that the integrated circuits and method of fabrication described herein are not necessarily so

restricted. In particular, device elements 24 may include any configuration of components for SAW and MEMS devices known to those skilled in such industries. Furthermore, device elements 24 may include components in addition to the components specifically configured for a SAW or MEMS device, such as for example, line traces for connection to input/output pads or ground contacts. Moreover, although two device elements are shown upon base substrate 22, topography 20 may include any number of device elements, including a single device element or more than two device elements. As will be discussed in more detail below, device elements 24 may collectively serve as a SAW device or MEMS device, or may serve as separate devices, depending on the operating attributes of the components comprising device elements 24 and the design specifications of the ensuing device. As such, although portions of device elements 24 are sealed with a single cavity as described below in reference to Figs. 3-7, portions of device elements 24 may alternatively be formed in multiple cavities or portion of only one of device elements 24 may be formed within a sealed cavity.

As noted above, Fig. 2a illustrates an exemplary configuration of components which may be used for a SAW device. In particular, Fig. 2a shows a partial top view of topography 20 having interdigitated transducer (IDT) 27 arranged upon base substrate 22. In general, IDT 27 may be patterned from a metal such as aluminum for example. The general function of IDTs within SAW devices is to convert electrical field energies to mechanical wave energies and vice versa. In particular, IDTs may be used to convert electrical signals received on bus bars to mechanical waves which propagate along the surface or near the surface of an underlying substrate. In addition, IDTs may be used to receive mechanical waves propagating along the surface of the substrate and convert them into output electrical field energies. In either case, wave propagation may occur in areas between electrodes of a single IDT as well as in areas between different IDTs. Such areas are referred to herein as the active areas of the SAW device.

As shown in Fig. 2a, IDT 27 includes bus bars 26a and 26b having a plurality of electrodes 28a and 28b respectively extending therefrom. Although the plurality of electrodes 28a and 28b as well as bus bars 26a and 26b are spaced apart and, therefore, are not electrically connected, IDT 27 as a whole may collectively represent one of device elements 24. The distinction between the components of IDT 27 is not shown in Fig. 1 such that the drawing may be applicable for MEMS device fabrication as well as SAW device fabrication. In some embodiments, device elements 24 may include similar component configurations. In other cases, however, device elements 24 may have different configurations of components. In any case, the spacing, length, width and quantity of electrodes within an IDT may generally affect the conversion of electrical field energies to mechanical wave energies and vice versa and, therefore, may affect the performance of the ensuing SAW device. As such, it is noted that IDT 27 is exemplary and, therefore, other IDT configurations known in the SAW device industry may be employed for the integrated circuits described herein, including those that utilize piezoelectrically-coupled Rayleigh waves as well as those that utilize non-Rayleigh waves. In particular, IDTs having different quantities, lengths, widths and/or spacings of electrodes than electrodes 28a and 28b shown in Fig. 2a may be employed.

It is further noted that Fig. 2a illustrates an exemplary configuration of components for device elements 24 and, therefore, one or both of device elements 24 may include alternative component configurations. For example, one or both of device elements 24 may include a plurality of IDTs in some embodiments. Furthermore, one or both of device elements 24 may include reflectors. In some embodiments, the configuration of components within a SAW device may depend on its application and, as such, the integrated circuit described herein may include any application of SAW devices, including bandpass filters and any other applications known in the industry. In turn,

the dimensions and compositions of SAW device components included in the integrated circuit described herein may be in accordance with design specifications for the ensuing device. In addition, the SAW device components may generally be formed by techniques known in the microelectronic fabrication industry including, for example, deposition, photolithographic, and etching processes.

5 As noted above, IDTs are used in SAW devices to convert electrical field energies to mechanical wave energies and vice versa. In particular, the conversion of electrical field energies to mechanical waves and vice versa within a SAW device may be directed along a track of IDTs. The term "track," as used herein, may generally refer to a compilation of SAW device IDTs, some of which are used to primarily convert a receiving electric field energy into a mechanical wave energy and others which are used to primarily convert the mechanical wave energy into an
10 output electric field energy. In some embodiments, one of device elements 24 illustrated in Fig. 1 may be configured to primarily convert a receiving electric field energy into a mechanical wave energy and the other of device elements 24 may be configured to primarily convert the mechanical wave energy into an output electric field energy. In such cases, device elements 24 may collectively serve as a track. In other embodiments, however, one or both of device elements 24 may be individually configured as one or more tracks. For instance, one or both of
15 device elements 24 may include a plurality of IDTs with which to convert electrical field energies to mechanical wave energies and vice versa. An exemplary SAW device including multiple tracks arranged upon a substrate is illustrated in Fig. 11 and described in more detail below.

Turning to Fig. 2b, an exemplary configuration of components which may be used for a MEMS device is shown. In particular, Fig. 2b illustrates an expanded view of one of device elements 24 showing beam 30 supported
20 by structure 32 and suspended above gate 34 and contact pad 36. The distinction of such components is not shown in Fig. 1 such that the drawing may be applicable for SAW device fabrication as well as MEMS device fabrication. As noted above, the term "MEMS devices" as used herein may generally refer to microelectronic devices which integrate electro-mechanical functions using moving structures. In regard to the configuration of components illustrated in Fig. 2b, the application and release of voltages to gate 34 may move beam 30 relative to contact pad 36
25 and, therefore, may serve as a MEMS device. It is noted that the MEMS device may include additional components which are not depicted in the cross-sectional view of Fig. 2b. Moreover, alternative component configurations of MEMS devices known to those skilled in the MEMS device industry may be incorporated into one or both of device elements 24 and, therefore, the integrated circuits described herein are not restricted to the MEMS structure depicted in Fig. 2b. For instance, one or both of device elements 24 may include a plurality of beams, support structures,
30 gates and/or contact structures.

In some embodiments, device elements 24 may include similar configurations of MEMS components. In other cases, however, device elements 24 may have different configurations of MEMS components. In either case, device elements 24 may, in some embodiments, be configured to function together. In other words, device elements 24 may collectively serve as a single MEMS device. In other embodiments, device elements 24 may be configured
35 to function as separate MEMS devices. In either case, the dimensions and compositions of the components may be in accordance with design specifications generally known in the MEMS fabrication industry. Exemplary materials for the components may include but are not limited to gold, copper, titanium, tungsten, or alloys of such metals. In some embodiments, one or more of the MEMS components may additionally include dielectric materials. In any case, the MEMS device components may generally be formed by techniques known in the microelectronic
40 fabrication industry including, for example, deposition, photolithographic, and etching processes.

Regardless of whether device elements 24 make up a SAW device or a MEMS device, the method of fabrication described herein may continue to Fig. 3 in which sacrificial layer 40 is deposited onto topography 20. As shown in Fig. 3, sacrificial layer 40 may, in some embodiments, be deposited conformably, such that its upper surface mimics the underlying contour of topography 20. In other embodiments, sacrificial layer 40 may be deposited such that a substantially planar surface is formed. In either case, sacrificial layer 40 may, in some embodiments, be polished subsequent to deposition. In general, the thickness of sacrificial layer 40, as deposited or subsequent to polishing, may be between approximately 4000 angstroms and approximately 2 microns and more generally, between approximately 8000 angstroms and approximately 1 micron. Larger or smaller thicknesses for sacrificial layer 40 may be employed, however, depending on the design specifications of the ensuing device.

In general, sacrificial layer 40 may include a material having substantially different etch characteristics to that of the materials of base substrate 22 and device elements 24, particularly in reference to the etch chemistry used to pattern the sacrificial layer described below in reference to Fig. 4. In addition, sacrificial layer 40 may include a material having substantially different etch characteristics to that of a subsequently deposited sealing layer, particularly in reference to the process used to remove remaining portions of sacrificial layer 40 relative to the sealing layer as described below in reference to Fig. 6. Some exemplary materials for sacrificial layer 40 are discussed below, but the method described herein is not necessarily so restricted. Consequently, other materials may, in some embodiments, be considered for sacrificial layer 40.

In some embodiments, sacrificial layer 40 may include polysilicon. The use of polysilicon as a sacrificial material has an advantage that its deposition may increase either the bulk or surface conductivity of substrate materials used for SAW devices, such as lithium niobate or lithium tantalate, for example. This is due to a chemical reduction process that is known to occur when these substrate materials are heated in vacuum. In particular, the chemical reduction process may produce a thin skin of chemically reduced material of readily oxidized silicon having increased conductivity on the surface of the base substrate. This increased conductivity can be valuable in suppressing the build up of charge on these substantially insulating substrates which occurs due to a pyroelectric effect. For example, lithium tantalate can build up thousands of volts of pyroelectrically-induced charge during temperature changes and this built-up charge can potentially degrade the performance of a SAW device. In particular, built-up charge on a lithium tantalate substrate may damage the IDT structures or may form microscopic domains of reversed crystal orientation in the SAW active area. In some embodiments, built-up charge on a lithium tantalate substrate may damage the wafer even to the point of fracture since pyroelectrically-induced voltages may exceed the breakdown voltage of the substrate material. Consequently, using polysilicon sacrificial layers in fabricating SAW devices may result in devices with superior resistance to these deleterious pyroelectric effects.

In order to avoid adversely affecting the material of base substrate 22 during the deposition of polysilicon, sacrificial layer 40 may, in some embodiments, be deposited at temperatures above the Curie temperature of the base substrate material. For example, in embodiments in which base substrate 22 includes lithium tantalate, sacrificial layer 40 may be deposited around 550°C, since the Curie temperature of congruent lithium tantalate is about 600°C and the Curie temperature for stoichiometric lithium tantalate is about 695°C. Smaller or larger temperatures, however, may be used for the deposition of polysilicon for sacrificial layer 40, depending on the specifications of the fabrication process and the composition of the base material. For example, sacrificial layer 40 may, in some cases, include polysilicon when device elements 24 include MEMS device components. In such cases, the substrate materials used for MEMS devices may not, in some embodiments, include magnetic materials and,

therefore, may not include a Curie temperature reference at which to avoid adverse affects as compared to those materials used for SAW devices. Consequently, polysilicon may, in some embodiments, be deposited at higher temperatures than those mentioned above. In other cases, polysilicon may be deposited at lower temperatures than those mentioned above to lower the thermal budget of the fabrication process.

5 Although polysilicon offers advantages for SAW devices in some cases, other materials for sacrificial layer 40 may be used, including embodiments in which topography 20 includes SAW devices or MEMS devices. For example, sacrificial layer 40 may, in some embodiments, include amorphous silicon. Amorphous silicon may generally be deposited at a lower temperature than polysilicon and, therefore, may advantageously offer a manner in which to lower the thermal budget of the fabrication process. For example, amorphous silicon may be deposited at
10 temperatures as low as 50° C using sputter deposition techniques. A further benefit of using amorphous silicon for sacrificial layer 40 is it may be dry etched in a highly selective manner using xenon difluoride gas, which is described below in reference to Fig. 6 as an etch chemistry which may be used to remove portions of sacrificial layer 40 from under a subsequently deposited sealing layer.

 In yet other embodiments, sacrificial layer 40 may be a polymer material, such as polyimide, photoresist, or
15 polymethyl methacrylate (PMMA), for example. These polymer sacrificial materials may be beneficial when low temperature processing is needed through the sealing process described below. The use of polymer materials for sacrificial layer 40 may, in some embodiments, have disadvantages and, therefore, the pros and cons of using such materials may need to be weighed for design specifications of the device. A disadvantage of using polymer materials for sacrificial layer 40 may include difficulty of removing the material from an area with significant lateral
20 dimensions due to the directional nature of plasma etching needed to etch the material. In addition, some polymer materials may include impurities that fail to react with plasma etch chemistries, thereby leaving a residue. The formation of such residue may not be an issue with PMMA, however. Furthermore, polymer materials may facilitate the formation of water molecules that adsorb to the surfaces inside an enclosed area and may prevent hermeticity due to the moisture.

25 Subsequent to its deposition, sacrificial layer 40 may be patterned as illustrated in Fig. 4. The patterning process may generally include lithography techniques known to those skilled in microelectronic fabrication. As shown in Fig. 4, sacrificial layer 40 may be patterned such that portions of device elements 24 are exposed. In this manner, electrical contact may be made to device elements 24, such as for coupling to input/output pads or ground contacts. In some embodiments, the exposed portions of device elements 24 may include all or portions of bus bars of an IDT within a SAW device. Alternatively, the exposed portions of device elements 24 may include portions of
30 a contact pad or extensions from a support structure within a MEMS device. In yet other embodiments, the exposed portions of device elements 24 may include line traces which are configured for coupling to input/output pads or ground traces of either a MEMS device or a SAW device.

 In addition to exposing portions of device elements 24, sacrificial layer 40 may be patterned such that
35 portions of the sacrificial material remain over a portion of the microelectronic device. In particular, sacrificial layer 40 may be patterned such that portions of the material remain over regions of the device in which mechanical motion will be detected, referred to herein as active areas. For example, in embodiments in which device elements 24 include SAW devices, sacrificial layer 40 may be patterned such that portions of the material remain over areas between IDTs and areas between electrodes of the IDTs, since it is these regions over which waves will be

propagated. In embodiments in which device elements 24 include MEMS devices, sacrificial layer 40 may be patterned such that portions of the material remain over areas having structures configured to move.

As shown in Fig. 4, patterned portions of sacrificial layer 40 remain over the area between device elements 24. As such, in some embodiments, the area between device elements 24 may be active. In other embodiments, the area may not be active. In such cases, sacrificial layer 40 may alternatively be patterned to expose a portion of the area between device elements 24. Thus, the pattern in which sacrificial layer 40 is formed may depend on the design specifications of the device/s comprising device elements 24. Consequently, sacrificial layer 40 may, in some embodiments, be patterned in different patterns than the one shown in Fig. 4. For instance, sacrificial layer 40 may, in some embodiments, be patterned with vias formed in the area between device elements 24, but exterior to the active areas of the device. The formation of vias may, for example, be advantageous for forming support posts for the subsequently formed sealing structure. In particular, since sacrificial layer 40 will be removed subsequent to the deposition of a sealing layer as described below in reference to Fig. 7, vias extending through portions of sacrificial layer 40 may allow a sealing material to be deposited therein to form posts with which to support the sealing structure over the open-space cavity. Such support structures may be particularly advantageous in embodiments in which a relatively large area of base substrate 22 will be sealed.

As illustrated in Fig. 4, sealing layer 42 may be deposited over the patterned portion of sacrificial layer 40 as well as over the exposed portions of device elements 24 and base substrate 22. As with sacrificial layer 40, sealing layer 42 may, in some embodiments, be deposited conformably as shown in Fig. 4, such that its upper surface mimics the underlying contour of topography 20. In other embodiments, sealing layer 42 may be deposited such that a substantially planar surface is formed. In either case, sealing layer 42 may, in some embodiments, be polished subsequent to deposition. In general, the thickness of sealing layer 42 may be sufficient to be impermeable to contaminants and moisture and, therefore, may depend on the material composition. An exemplary thickness range for sealing layer 42, as deposited or subsequent to polishing, may, however, generally be between approximately 0.8 microns and approximately 2 microns, and in some cases, approximately 1.6 microns. Larger or smaller thicknesses for sealing layer 42 may be employed, however, depending on the design specifications of the ensuing device.

In general, sealing layer 42 may include a material having substantially different etch characteristics to that of the materials of base substrate 22 and device elements 24, particularly in reference to the etch chemistry used to pattern the sealing layer described below in reference to Fig. 5. In addition, sealing layer 40 may include a material having substantially different etch characteristics to that of sacrificial layer 40, particularly in reference to the process used to remove remaining portions of sacrificial layer 40 relative to the sealing layer as described below in reference to Fig. 6. Furthermore, the material of sealing layer is preferably impermeable to contaminants and moisture. In some cases, the proximity and electrical characteristics of sealing layer 42 for applications of SAW devices may need to be considered for material selection of the sealing layer as well. Exemplary materials for sealing layer 42 may include spin-on-glass, a sputtered glass, metal or silicon dielectric materials. The method described herein, however, is not necessarily so restricted. Consequently, other materials may, in some embodiments, be considered for sealing layer 42. The term, "silicon dielectric materials" is used herein to refer to dielectric materials including silicon, such as silicon oxide, silicon nitride and silicon oxynitride, for example. Such materials, as well as glass materials, may be advantageous for insulating device elements 24 from conductive

features subsequently formed overlying sealing layer 42. Alternatively, a metal material for sealing layer 42 may advantageously provide electrical connection between such features.

Fig. 5 illustrates the patterning of sealing layer 42, exposing portions of base substrate 22 and portions of device elements 24. In this manner, electrical contact may be subsequently made to device elements 24, such as for coupling to input/output pads or ground contacts. The patterning process may generally include lithography techniques known to those skilled in microelectronic fabrication. As shown in Fig. 5, the patterning process may form openings 44 within sealing layer 42, exposing portions of sacrificial layer 40. In general, the dimensions of openings 44 may be sufficient to allow an etch chemistry to slip therethrough to remove remaining portions of sacrificial layer 40, which is described in more detail below in reference to Fig. 6. In some cases, the dimensions may be optimized such that openings 44 may be efficiently closed subsequent to the removal of sacrificial layer 40, which is described in more detail below in reference to Fig. 7. In general, openings 44 may include a width smaller than a length, the width dimension having a higher correlation for efficiently removing sacrificial layer 40 as well as subsequently plugging openings 44. Although the dimensions of openings 44 may depend on the area of topography 20 covered by sealing layer 42 and the placement of the openings across the sealing layer, exemplary dimensions may include a width between approximately 0.4 microns and approximately 1.0 micron, or more specifically about 0.8 micron. In addition, exemplary dimensions of a length for openings 44 may be between approximately 5 microns and approximately 20 microns, or more specifically about 10 microns.

In some embodiments, openings 44 may be formed in areas which do not overly the active areas of the device. Such placement of openings 44 may be advantageous for preventing contamination of the active areas, particularly during the subsequent process of filling the openings as described in more detail below in reference to Fig. 7. In some embodiments, openings 44 may be formed at a lateral distance of up to approximately 5 microns from the active areas. Fig. 5 shows openings 44 over device elements 24, but such placement is exemplary. In particular, openings 44 may be formed over other areas of the topography, including the area between device elements 24 when such an area is not active. It is noted that, in some embodiments, the areas between device elements 24, particularly at the cross-sectional line along which Fig. 5 is shown, may be an active area. In particular, the area between device elements 24 may be configured for the transmission of acoustical waves between the device elements. In such cases, topography 20 may be configured with areas which are not active on either side of the cross-sectional line depicted in Fig. 5 and openings 44 may alternatively be placed over such areas. It is further noted that the areas between individual components of one or both of device elements 24 may additionally or alternatively be active areas and, therefore, it may not be advantageous to place openings 44 over device elements 24 in some embodiments. In such cases, openings 44 may be placed over regions of topography 20 which do not include device elements 24.

Turning to Fig. 6, remaining portions of sacrificial layer 40 are removed through openings 44 to create cavity 46. Such a removal process is preferably etch selective to the material of sacrificial layer 40 over the material of sealing layer 42 such that a sufficient portion of sealing layer 42 may remain to surround cavity 46. As described above, openings 44 may be bound and, therefore, the central portion of sealing layer 42 shown in Fig. 6 may be suspended over cavity 46. In some embodiments, the removal of remaining portions of sacrificial layer 40 may be conducted by a dry etching process that does not leave undesirable residue. Leaving the acoustically active portion of a SAW device free of the surface residue prevents adverse alterations to wave propagation characteristics. In addition, a MEMS device free of surface residue inhibits the modification of the voltage level at which a moving

part with a MEMS device is brought into contact or released from a contact pad. As a consequence, device performance may not be degraded for the SAW device or MEMS device comprising device elements 24.

An exemplary dry etch process which may be particularly effective for embodiments in which sacrificial layer 40 includes polysilicon involves exposing topography 20 to an ambient of xenon difluoride (XeF_2) and is referred to herein as a " XeF_2 release process." In particular, a XeF_2 release process may be substantially selective to etching polysilicon without substantially etching other materials, such as silicon dielectric materials for example. Consequently, in embodiments in which sealing layer 42 includes a silicon dielectric material, the XeF_2 release process may not remove substantial portions of the layer. In addition, the XeF_2 release process may generally be less reactive with metallic materials than polysilicon and, therefore, such a removal process may be advantageous in embodiments in which sealing layer 42 includes a metal material. In both cases, the XeF_2 release process removes the sacrificial material without leaving a substantial residue on the surface of the wafer, which as noted above, may cause degradation of the device.

In general, the XeF_2 release process may include purging a chamber comprising topography 20 with a gas such as nitrogen, for example, prior to exposing topography 20 with XeF_2 . The chamber may include the vessel in which sealing layer 42 was patterned or may include a different vessel. In either case, the chamber may be subsequently evacuated down to a moderate vacuum. The XeF_2 may be sublimated in a separate container to a pressure of about 4 mTorr (i.e., the vapor pressure of XeF_2) and then introduced into the chamber comprising topography 20 to remove remaining portions of sacrificial layer 40. In some embodiments, the XeF_2 release process may be performed in vapor phase at a pressure of approximately 60 mTorr, at room temperature and with no external energy sources. Larger or smaller pressures and temperatures, however, may be used for the XeF_2 release process as well as with the use of external energy sources in some cases.

It is noted that although the removal of the remaining portions of sacrificial layer 40 is described specifically with reference to the XeF_2 release process and the sacrificial layer including polysilicon, the method is not necessarily restricted to such materials or the use of the XeF_2 release process. In particular, the method described herein may be used with any of the materials noted above for the respective structures and layers of topography 20, including amorphous silicon or polymers for sacrificial layer 40. In addition, the method may include other release processes which are configured to be highly selective to the material of sacrificial layer 40 and substantially non-selective to the material of sealing layer 42.

In some embodiments, cavity 46 may be filled with one or more gases prior to plugging openings 44, a process which is described in more detail below in reference to Fig. 7. In particular, cavity 46 may be pressurized by placing topography 20 in a sputtering, evaporating or other vacuum chamber pumped down to a target pressure. More specifically, one or more gases, such as argon or any other noble gases, may be introduced in a chamber comprising topography 20 and brought to equilibrium such that the gas pressure with cavity 46 is the same as the gas pressure external to the cavity. Such a pressurized atmosphere may aid in supporting sealing layer 42 over cavity 46. In other embodiments, the method may not include filling cavity 46 with gases and, therefore, the method may continue to Fig. 7 subsequent to removing sacrificial layer 40.

Fig. 7 illustrates openings 44 within sealing layer 42 filled such that cavity 46 is sealed by sealing structure 43. In general, openings 44 may be filled with a material sufficient to prevent the permeation of contaminants or moisture therethrough. For example, openings 44 may be filled with a silicon dielectric material or a metal material. In some embodiments, the material used to fill openings 44 may be same material as sealing layer 42. In other

embodiments, however, the material used to fill openings 44 may be a different material than sealing layer 42. In either case, the deposition of the material used to fill openings 44 may include any deposition technique known to those skilled in microelectronic fabrication.

For example, sputtering techniques may be used to fill openings 44, particularly when configured to be isotropic in nature. In particular, an isotropic sputter deposition process may coat the rims of openings 44, building up material until the holes are sealed. The isotropic nature of such a process, however, will inevitably introduce some of the fill material into cavity 46. If the sputtered material lands on active regions of the underlying device, its performance may be degraded. To avoid this detrimental effect, openings 44 may be purposely positioned over inactive areas of the device as described above in reference to Fig. 5. Alternatively, evaporation deposition techniques may be used to fill openings 44. Since evaporation tends to be highly directional in nature, it may be advantageous to position the beam at an angle to topography 20 such that openings 44 may be filled without introducing a significant amount of material into cavity 46. An additional advantage of evaporation is that a higher vacuum may be achieved in an evaporation chamber in comparison to a sputtering chamber.

In general, plugging openings 44 may form sealing structure 43, which, as noted above, may include materials specifically configured to serve as a hermetic seal, preventing the permeation of contaminants and moisture therethrough. In some embodiments, the hermeticity of sealing structure 43 can be enhanced by coating it with a film of silicon nitride (not shown) deposited using plasma-enhanced chemical vapor deposition (PECVD), although such an additional film is not necessarily needed.

Subsequent to the filling of openings 44, dielectric layer 48 may be deposited upon topography 20 as shown in Fig. 7. Such a dielectric layer may include dielectric materials such as but not limited to silicon dioxide, silicon nitride and silicon oxynitride. As shown in Fig. 7, dielectric layer 48 may be formed to a thickness such that its upper surface is spaced above the uppermost surface of sealing structure 43. In this manner, sealing structure 43 may be isolated from conductive features subsequently formed thereover. In other embodiments, however, dielectric layer 48 may be formed coplanar with a portion of sealing structure 43 such that conductive features may be formed thereon. In yet other cases, dielectric layer 48 may not be formed and a conductive layer may be deposited in place thereof. Such sequence of process steps may also be used to form conductive features upon sealing structure 43. In some cases, sealing layer 42 may include a conductive material and, therefore, the formation of conductive features thereon may be particularly beneficial for using sealing structure 43 for electrically connecting such features with device elements 24. In other embodiments, however, sealing layer 42 may not include a conductive material and, therefore, sealing structure 43 may not be used to electrically connect overlying features with device elements 24.

As shown in Fig. 8, vias 50 may be formed within dielectric layer 48 when such a layer is deposited. Vias 50 may generally be formed by patterning openings within dielectric layer 48 and subsequently filling the openings with a conductive material, such as but not limited to aluminum, copper, gold, titanium, tungsten and metal alloys thereof. As shown in Fig. 8, vias 50 may be formed upon upper portions of contact elements 24 arranged exterior to cavity 46. In this manner, vias 50 may be used to electrically connect subsequently formed overlying conductive features to device elements 24. In other embodiments, vias 50 may be formed upon other conductive features of topography 20, such as contact pads coupled to input/output pads or ground pads of the topography, or may be formed upon the upper surface of base substrate 22. In such cases, vias 50 may or may not be used to electrically connect subsequently formed overlying conductive features to device elements 24. In particular, vias 50 may, in

some embodiments, be used to connect to devices formed upon topography 20 which function independent of the device disposed within cavity 46. As noted above, dielectric layer 48 may not, in some embodiments, be formed and, therefore, vias 50 may not be formed in some cases.

Regardless of whether dielectric layer 48 and vias 50 are formed, the method described herein may include the formation of a conductive feature above sealed cavity 46. In general, the formation of the conductive feature may include depositing a conductive material, such as but not limited to aluminum, copper, gold, titanium, tungsten and metal alloys thereof, upon topography 20. Thereafter, the deposited material may be patterned according to design specifications of the device. The patterning process may generally include lithography techniques known to those skilled in microelectronic fabrication. In some embodiments, the formation of such a conductive feature may be upon dielectric layer 48 and vias 50 as shown by conductive feature 52 in Fig. 9. In addition or alternatively, conductive feature 52 may be formed upon sealing structure 43. In any case, conductive feature 52 may be formed directly above and sometimes spanning sealing structure 43 as shown in Fig. 9.

In general, conductive feature 52 may be a conductive device or a partial portion of a conductive device used to enhance the integrated circuit formed from topography 20. In some embodiments, conductive feature 52 may be used in conjunction with the device formed within cavity 46 and, therefore, may be electrically connected to device elements 24. In other embodiments, conductive feature 52 may be used independent of the device formed within cavity 46 and, therefore, may not be electrically connected to device elements 24. In either case, conductive feature 52 may serve as an interconnect line. In other embodiments, conductive feature 52 may be used to form other conductive devices, such as but not limited to capacitors, inductors, interconnects, resistors, shields and electro static discharge protection structures. The thickness and lateral dimensions of conductive feature 52 may generally depend on the design specifications of the ensuing integrated circuit and, therefore, may vary for different applications.

Fig. 10 illustrates the formation of additional layers 54 above conductive feature 52. In general, additional layers 54 may include any number of layers and/or structures which may be used to fabricate the ensuing integrated circuit from topography 20. In some cases, additional layers 54 may include conductive features formed by deposition, photolithographic, and etching processes known in the microelectronic fabrication industry. In this manner, an integrated circuit may be fabricated including multiple levels of conductive features formed above a sealed cavity. The conductive features are depicted in Fig. 10 by the continuation dots extending above conductive features, indicating that any number of conductive features may be formed thereover. As noted above, the multiple levels of conductive features within topography 20 may form conductive devices, such as but not limited to capacitors, inductors, interconnects, resistors, shields and electro static discharge protection structures. In some cases, additional layers 54 may further include interlevel dielectric materials to insulate the conductive devices disposed therein as well as conductive feature 52. Other layers and materials may also be included within additional layer 54 for the formation of the conductive devices, depending on the design specifications of the device. In some embodiments, additional layers 54 may not be formed upon conductive feature 52 and, consequently, an integrated circuit formed from topography 20 may only include a single level of metallization formed above cavity 46.

Regardless of whether additional layers 54 are formed within topography 20, passivation layer 56 may be deposited on the upper surface of the topography to prevent permeation of contaminants and moisture to the conductive features disposed above cavity 46. In some embodiments, passivation layer 56 may also prevent permeation of contaminants and moisture into cavity 46. Examples of suitable dielectric materials for passivation

layer 56 include silicon nitride, polyimide, spun on glass, silicon dioxide and silicon carbide, but other passivation materials known in the microelectronics industry for sealing integrated circuitry on a chip may be used. Subsequent to the deposition of passivation layer 56, bond pads may be patterned therein such that the topography may be wire-bonded or surface mounted to a substrate carrier.

5 In accordance with the present disclosure, sealing structure 43 enables the addition of multiple levels of metal over a SAW device or a MEMS device and the substrate upon which such devices are formed. The addition of one or more levels of metallization in turn enables the creation of interconnects and other conductive structures that were previously unrealizable at the chip level. This integration further enables the die size to be reduced. Furthermore, the multiple levels of conductors over mechanical active area enables the construction of various
10 integrable components on the same substrate as SAW or MEMS devices. For example, in some embodiments, SAW device and MEMS devices may be fabricated on the same substrate. In addition or alternatively, thin film transistors may be formed on a substrate with SAW and/or MEMS devices.

In addition to the aforementioned benefits, the formation of conductive devices over a SAW device may add functionality to an integrated circuit by enabling tracks of the SAW device to be split and, consequently,
15 increase performance. As noted above, the spacing, length, width and quantity of electrodes within an IDT may generally affect the conversion of electrical field energies to mechanical wave energies and vice versa and, therefore, may affect the performance of the ensuing SAW device. The size of the electrodes and, more particularly, the length of the electrodes are generally limited by the parasitic resistance of the electrodes. The formation of conductive devices over SAW devices may allow tracks to be arranged side by side and in close enough proximity
20 such that IDTs within one or more of the different tracks may be coupled to a single input and/or output trace and the mechanical waves converted or received from the IDTs may be partially aggregated. Such a "split track" configuration effectively allows IDTs within the tracks to operate as a single IDT with longer electrodes than each IDT may individually comprise. As a result, the performance of the device may be improved.

Fig. 11 illustrates an exemplary circuit employing a configuration of "split tracks" for a SAW device. It is
25 noted, however, the concept of "split tracks" is not limited to the configuration depicted in Fig. 11. In particular, the concept of "split tracks" may be integrated within any SAW device design, including those with more or less tracks than the circuit illustrated in Fig. 11. Moreover, the quantity, placement and connection of conductors integrated over SAW devices are not restricted to the configuration of conductors illustrated in Fig. 11. In particular, the circuit illustrated in Fig. 11 is presented as an example of how conductors may be used to enhance the functionality
30 of a SAW device, particularly with regard to connecting IDTs of neighboring tracks such that the parasitic resistance limitations on the lengths of electrodes may be superseded.

As shown in Fig. 11, circuit 60 may include sets of tracks 70 and 80. For the description of circuit 60, each set of tracks reference by numbers 70 and 80 may represent a set of split tracks. It is noted that circuit 60 is not restricted to two sets of split tracks, nor are each set of split tracks restricted two tracks. In particular, circuit 60 may
35 include any number of split track sets, including one or more than one, and the split track sets may include any plurality of tracks. It is further noted that circuit 60 may, in some embodiments, include tracks which are not split. As shown in Fig. 11, the split-tracks within tracks 70 and 80 may each include a similar configuration of components. Circuit 60, however, is not necessarily so restricted. In particular, one or both of track sets 70 and 80 may include individual split-tracks with a different set of components. As such, circuit 60 is not necessarily limited
40 to the illustration of Fig. 11.

The components within each of track sets 70 and 80 are outlined by a dotted line indicating they are arranged below sealing structures 78 and 88, respectively. Sealing structures 78 and 88 may be formed similar to sealing structure 43 described above in reference to topography 20 and, therefore, may serve to seal the components with a cavity and prevent the permeation of contaminants or moisture therein. It is noted that other components of circuit 60, such as the conductors 90, 92 and 94, ground contacts 64 and input/output pads 66 and 68 as well as other components are not shown underlying dielectric layers or a passivation layer. Dielectric and passivation layers have been omitted from Fig. 11 to illustrate the integration of split-tracks within a SAW device, but should not be presumed to be omitted from circuit 60. As will be described in more detail below, each track within track sets 70 may include an IDT configured to primarily convert an incoming electric field energy to a mechanical wave energy and another IDT configured to primarily receive the mechanical wave energy and convert it to an output electric field energy. Fig. 11 illustrates each track including reflector components, respectively referenced for track sets 70 and 80 by numbers 76 and 86. It is noted that the inclusion, number and placement of such reflectors is exemplary. In addition, other components known for use in SAW devices may be additionally or alternatively included within the individual tracks of track sets 70 and 80.

As shown in Fig. 11, each of the split-tracks within track set 70 may include an IDT 72 interposed between two of IDTs 74. In the configuration of circuit 60, IDTs 72 are coupled to input pad 66 and, therefore, are configured to primarily convert an incoming electric field energy to mechanical wave energies. In general, the phrase "configured to primarily", as used herein, may refer to adaptations which are mainly or predominately used to perform a given function. It is noted, however, that IDTs 72 may convert mechanical wave energies to output electric field energies in some embodiments. As shown in Fig. 11, IDT 72 arranged in the left track of track set 70 is coupled to input pad 66 via trace 67. In such embodiments, IDTs 72 as well as IDTs 74 may be rotated 90° relative to the orientation depicted in Fig. 2a. Conductor 90 is also coupled to trace 67 by a via and spans over track set 70 to another via coupled to a contact pad disposed on the far side of the right track of track set 70. In this manner, the right track of track set 70 is coupled to input pad 66 as well. As shown in Fig. 11, ground trace 62 extends between the individual tracks of track sets 70 and 80, indicating bus bars arranged along the respective sides of the tracks are grounded. Consequently, IDTs 72 are configured to receive an electric field energy from input pad 66. As noted above, IDTs 72 are configured to primarily convert an incoming electric field energy to a mechanical wave energy. In turn, IDTs 74 are configured to primarily receive the mechanical wave energies generated from IDTs 72 in each respective track and convert the mechanical wave energies to output electric field energies.

As shown in Fig. 11, circuit 60 may include conductors 94 arranged over track set 70 and, more specifically, spanning over opposing IDTs 74 arranged within the individual tracks of track set 70. Conductors 94 may be coupled to underlying contact pads along the sides of the individual tracks of track set 70 by vias. Such a connection allows output electric field energies generated from IDTs 74 to aggregate along conductors 94 and be transmitted as input to track set 80. Each track of track set 80 includes IDTs 82 coupled to each of conductors 94. In particular, conductors 94 are coupled to contact pads arranged along the exteriors of sealing structures 88 by vias. The contact pads are coupled to IDTs 82 such that an incoming electric field energy may be received. As shown in Fig. 11, ground track 62 is interposed between the tracks of track set 80 and, therefore, IDTs 82 may be configured to primarily convert an incoming electric field energy to mechanical wave energies. It is noted, however, that IDTs 82 may convert mechanical wave energies to output electric field energies in some embodiments. Such mechanical wave energies may be collected by IDTs 84 and converted to electric field energies. Each of the tracks within track

set 80 may include two of IDTs 84 to support a dual-output signal transmitted to output pads 68. As shown in Fig. 11, circuit 60 includes conductors 92 arranged over IDTs 84 and coupled to contact pads arranged along the sides of sealing structures 88. Consequently, the electric field energies generated from IDTs 84 may be aggregated and transmitted over traces 69 to output pads 68.

5 As noted above, the configuration of circuit 60 is exemplary. In particular, the concept of “split-tracks” may be configured with any SAW device configuration. In addition, circuit 60 is not limited to the number or placement of conductors 90, 92 and 94 to produce the split tracks. In particular, circuit 60 is not necessarily limited to coupling IDTs which are in substantial alignment with each other, nor is it limited to splitting all tracks within a device. Consequently, all or portions of conductors 90, 92 and 94 may be repositioned or may be omitted from
10 circuit 60. In any case, additional conductive features may be formed above sealing structures 78 and 88 to enhance the operation of the integrated circuit as described above in reference to Figs. 9 and 10 for topography 20.

 The foregoing description of specific embodiments and examples of the invention have been presented for the purpose of illustration and description, and although the invention has been described and illustrated by certain of the preceding examples, it is not to be construed as being limited thereby. They are not intended to be exhaustive
15 or to limit the invention to the precise forms disclosed, and many modifications, improvements and variations within the scope of the invention are possible in light of the above teaching. It is intended that the scope of the invention encompass the generic area as herein disclosed, and by the claims appended hereto and their equivalents.

WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:
one or more device elements formed above a base substrate of the integrated circuit;
5 a structure forming a sealed cavity above at least a portion of the one or more device elements; and
one or more conductive devices formed above the sealed cavity.
2. The integrated circuit of claim 1, wherein the one or more device elements comprise a surface acoustic device.
- 10 3. The integrated circuit of claim 2, wherein the one or more device elements comprise a plurality of tracks each including:
a first interdigitated transducer configured to convert a receiving electric field energy into mechanical wave energy; and
15 a second interdigitated transducer configured to convert the mechanical wave energy into an output electric field energy; and
4. The integrated circuit of claim 3, wherein the one or more conductive devices comprise a first conductor arranged above and spanning across at least two tracks of the plurality of tracks, and wherein the first conductor is
20 coupled to the first interdigitated transducers of at least the two tracks.
5. The integrated circuit of claim 1, wherein the one or more device elements comprise a micro electro-mechanical systems device.
- 25 6. The integrated circuit of claim 1, wherein the one or more conductive devices are selected from the group consisting of capacitors, inductors, interconnects, resistors, shields and electro static discharge protection structures.
7. The integrated circuit of claim 1, wherein the structure is configured to electrically connect at least one of the one or more device elements to at least one of the one or more conductive devices.
- 30 8. A method for fabricating an integrated circuit, comprising:
forming one or more device elements above a substrate of the ensuing integrated circuit;
enclosing at least a portion of the one or more device elements within a sealed cavity;
depositing a conductive layer above the sealed cavity; and
35 patterning the conductive layer to form a conductive device above the sealed cavity.
9. The method of claim 8, wherein the step of enclosing at least a portion of the one or more device elements comprises:
forming a structure of sacrificial material upon over the area of the microelectronic topography;
40 forming a coating layer upon and about the structure of sacrificial material;

etching openings within the coating layer;
removing the sacrificial material through the openings; and
sealing the openings to form the cavity.

5 10. The method of claim 9, wherein the step of sealing the openings comprises depositing metal within the openings.

11. The method of claim 8, further comprising depositing additional conductive layers above the conductive device to form additional conductive devices above the sealed cavity.

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12. The method of claim 8, wherein the step of forming the one or more device elements comprises patterning interdigitated components of a surface acoustic device.

13. The method of claim 8, wherein the step of forming the one or more device elements comprises forming a
15 suspended structure above a contact pad for a micro electro-mechanical device.

14. The method of claim 8, further comprising:
depositing a passivation layer above the conductive device; and
etching bond pads within the passivation layer.

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15. A surface acoustic wave (SAW) device, comprising:
a plurality of tracks each comprising:
a first interdigitated transducer configured to convert a receiving electric field energy into
mechanical wave energy; and
25 a second interdigitated transducer configured to convert the mechanical wave energy into an
output electric field energy; and
a first conductor arranged above and spanning across at least two tracks of the plurality of tracks, wherein
the first conductor is coupled to the first interdigitated transducers of at least the two tracks.

30 16. The SAW device of claim 15, further comprising a second conductor arranged above and spanning across the two tracks, wherein the second conductor is coupled to the second interdigitated transducers of the two tracks.

17. The SAW device of claim 16, wherein the second conductor is further arranged above and spanning across additional tracks, and wherein the second conductor is coupled to the first interdigitated transducers of the additional
35 tracks.

18. The SAW device of claim 17, further comprising a third conductor arranged above and spanning across the additional tracks, wherein the third conductor is coupled to the second interdigitated transducers of the additional tracks.

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19. The SAW device of claim 15, wherein the first conductor is coupled to an input/output pad of the SAW device.

20. The SAW device of claim 15, wherein at least portions of the first and second interdigitated transducers are
5 disposed within a sealed cavity.

AMENDED CLAIMS

[Received by the International Bureau on 12 September 2005 (12.09.2005):
original claims 1-14 and 20 canceled and 21-31 added]

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STATEMENT

WHAT IS CLAIMED IS:

15. A surface acoustic wave (SAW) device, comprising:
a plurality of tracks arranged side by side each comprising:
 - 5 a first interdigitated transducer configured to convert a receiving electric field energy into mechanical wave energy; and
 - a second interdigitated transducer configured to convert the mechanical wave energy into an output electric field energy, wherein at least portions of the first and second interdigitated transducers are disposed within a sealed cavity;
 - 10 a first set of contact pads arranged exterior to the sealed cavity and each coupled to a different first interdigitated transducer of the plurality of tracks; and
 - a first conductor arranged above and spanning across at least two tracks of the plurality of tracks, wherein the first conductor is coupled to two of the first set of contact pads which are respectively coupled to two first interdigitated transducers corresponding to the at least two tracks such that electrical
 - 15 interconnection between the two first interdigitated transducers is made.
16. The SAW device of claim 15, further comprising:
 - a second set of contact pads arranged exterior to the sealed cavity and each coupled to a different second interdigitated transducer of the plurality of tracks; and
 - 20 a second conductor arranged above and spanning across the at least two tracks, wherein the second conductor is coupled to two of the second set of contact pads which are respectively coupled to two second interdigitated transducers corresponding to the at least two tracks such that electrical interconnection between the two second interdigitated transducers is made.
- 25 17. The SAW device of claim 16, wherein the second conductor is arranged above and further spans across additional tracks of the plurality of tracks, and wherein the second conductor is further coupled to two more of the second set of contact pads which are respectively coupled to two other second interdigitated transducers corresponding to the additional tracks such that electrical interconnection between the two other second interdigitated transducers is made.
- 30 18. The SAW device of claim 17, further comprising a third conductor arranged above and spanning across the additional tracks, wherein the third conductor is coupled to two first interdigitated transducers corresponding to the additional tracks.
- 35 19. The SAW device of claim 15, wherein the first conductor is coupled to an input/output pad of the SAW device.
21. The SAW device of claim 18, further comprising a fourth conductor arranged above and spanning across the additional tracks, wherein the fourth conductor is coupled to another two first interdigitated transducers corresponding to the additional tracks.
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22. The SAW device of claim 21, further comprising a fifth conductor arranged above and spanning across the at least two tracks, wherein the fifth conductor is coupled to two more of the second set of contact pads which are respectively coupled to two further second interdigitated transducers corresponding to the at least two tracks such that electrical interconnection between the two further second interdigitated transducers is made.

23. The SAW device of claim 22, wherein the fifth conductor is further arranged above and spanning across the additional tracks, and wherein the fifth conductor is further coupled to another two of the second set of contact pads which are respectively coupled to two more second interdigitated transducers corresponding to the additional tracks such that electrical interconnection between the two more second interdigitated transducers is made.

24. A surface acoustic wave (SAW) device, comprising:

a plurality of tracks arranged side by side each comprising:

a first interdigitated transducer configured to convert a receiving electric field energy into mechanical wave energy; and

a second interdigitated transducer configured to convert the mechanical wave energy into an output electric field energy, wherein at least portions of the first and second interdigitated transducers are disposed within a sealed cavity;

a first set of contact pads arranged exterior to the sealed cavity and each coupled to a different second interdigitated transducer of the plurality of tracks; and

a first conductor arranged above and spanning across at least two tracks of the plurality of tracks, wherein the first conductor is coupled to two of the first set of contact pads which are respectively coupled to two second interdigitated transducers corresponding to the at least two tracks such that electrical interconnection between the two second interdigitated transducers is made.

25. The SAW device of claim 24, further comprising:

a second set of contact pads arranged exterior to the sealed cavity and each coupled to a different first interdigitated transducer of the plurality of tracks; and

a second conductor arranged above and spanning across the at least two tracks, wherein the second conductor is coupled to two of the second set of contact pads which are respectively coupled to two first interdigitated transducers corresponding to the at least two tracks such that electrical interconnection between the two first interdigitated transducers is made.

26. The SAW device of claim 25, wherein the first conductor is further arranged above and spanning across additional tracks of the plurality of tracks, and wherein the first conductor is further coupled to two more of the second set of contact pads which are respectively coupled to two other second interdigitated transducers corresponding to the additional tracks such that electrical interconnection between the two other second interdigitated transducers is made.

27. The SAW device of claim 26, further comprising a third conductor arranged above and spanning across the additional tracks, wherein the third conductor is coupled to two first interdigitated transducers corresponding to the additional tracks.

28. The SAW device of claim 27, wherein the third conductor is coupled to an output pad of the SAW device.

29. The SAW device of claim 27, further comprising a fourth conductor arranged above and spanning across the additional tracks, wherein the fourth conductor is coupled to another two first interdigitated transducers corresponding to the additional tracks.

30. The SAW device of claim 29, further comprising a fifth conductor arranged above and spanning across the at least two tracks, wherein the fifth conductor is coupled to two more of the first set of contact pads which are respectively coupled to two further second interdigitated transducers corresponding to the at least two tracks such that electrical interconnection between the two further second interdigitated transducers is made.

31. The SAW device of claim 30, wherein the fifth conductor is further arranged above and spanning across the additional tracks, and wherein the fifth conductor is further coupled to another two of the first set of contact pads which are respectively coupled to two more second interdigitated transducers corresponding to the additional tracks such that electrical interconnection between the two more second interdigitated transducers is made.

PATENT COOPERATION TREATY
THE INTERNATIONAL BUREAU OF THE
WORLD INTELLECTUAL PROPERTY ORGANIZATION

In re Application of:	)	
Cypress Semiconductor	)	
	)	
Serial No. PCT/US2005/009887	)	
	)	
Filed: 24 March 2005	)	Atty. Dkt. No. 5298-19002
	)	
For: INTEGRATED CIRCUIT HAVING ONE	)	
OR MORE CONDUCTIVE DEVICES	)	
FORMED OVER A SAW AND/OR MEMS	)	
DEVICE	)	

I hereby certify that this paper or fee is being deposited with the U.S. Postal Service with sufficient postage as first-class mail 12 September 2005, and is address to: International Bureau of WIPO, 34, chemin des Colombettes, 1211 Geneva 20, Switzerland, or is being transmitted via facsimile.

Pamela Gerik
 Pamela Gerik

STATEMENT FOR AMENDMENTS UNDER ARTICLE 19

Via Facsimile: 011 41 22 338 8270

International Bureau of WIPO
 34, chemin des Colombettes
 1211 Geneva 20, Switzerland

Dear Sir/ Madam:

This paper is submitted in response to the International Search Report mailed 17 June 2005 to explain the relevance of at least some of the claim amendments.

As noted in the accompanying Section 205(b) Letter for Amendments Under Article 19, claims 15-18 have been replaced by amended claims bearing the same numbers, claims 1-14 and 20 have been canceled, and new claims 21-31 have been added. Claim 15 has been amended to include the subject matter of canceled claim 20 as well as the specification that the plurality of tracks are arranged side by side. In addition, the amendments to claim 15 include the addition of contact pads and their connections to the conductor arranged above and spanning across at least two of the tracks of the SAW device such that electrical interconnection between interdigitated transducers of the two tracks is made. Claims 16-18 have been amended in light of the amendment to claim 15. Moreover, claims 21-23 have been added to further specify the method recited in claims 15-18, namely to specify the inclusion of additional conductors arranged and spanning over tracks of the SAW device. Independent claim 24 has been added to specify a SAW device in which a conductor is arranged above and spans across a sealing structure which overlies tracks of the SAW device. The conductor is coupled to contact pads connected to interdigitated transducers of the tracks which are configured to convert mechanical wave energy into an

output electric field energy. Such a connection allows electrical interconnection between the interdigitated transducers.

Respectfully submitted,



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Date: 12 September 2005

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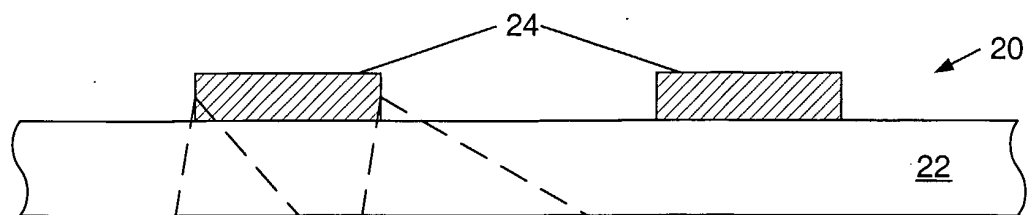


Fig. 1

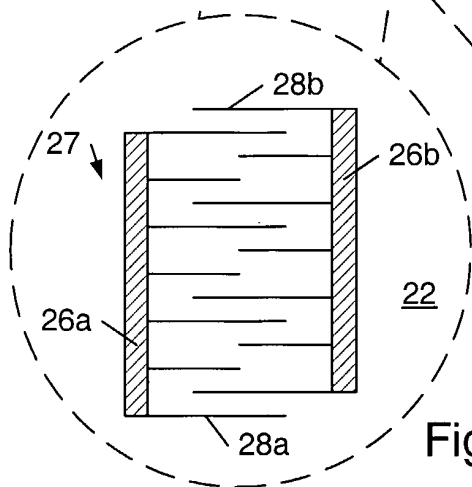


Fig. 2a

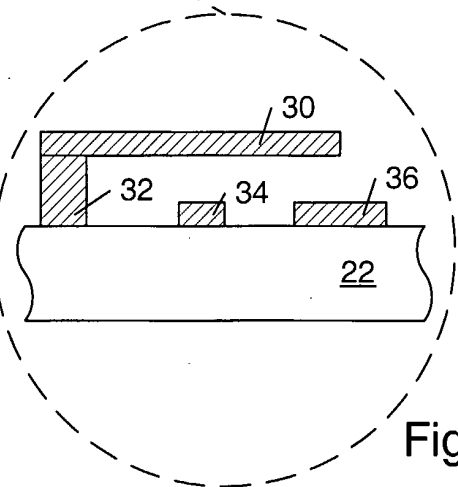


Fig. 2b

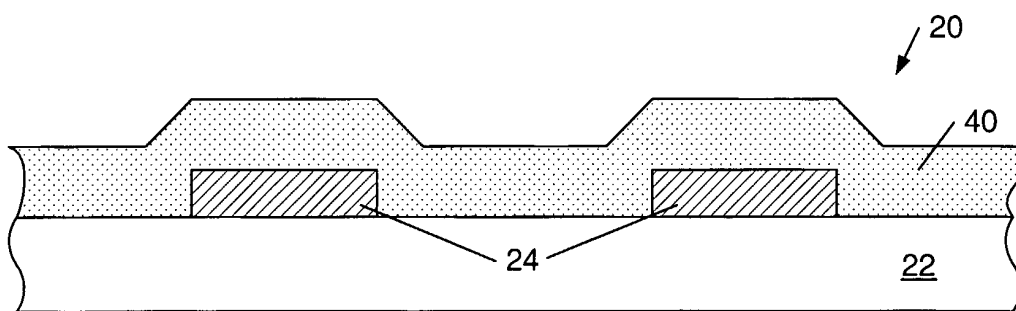


Fig. 3

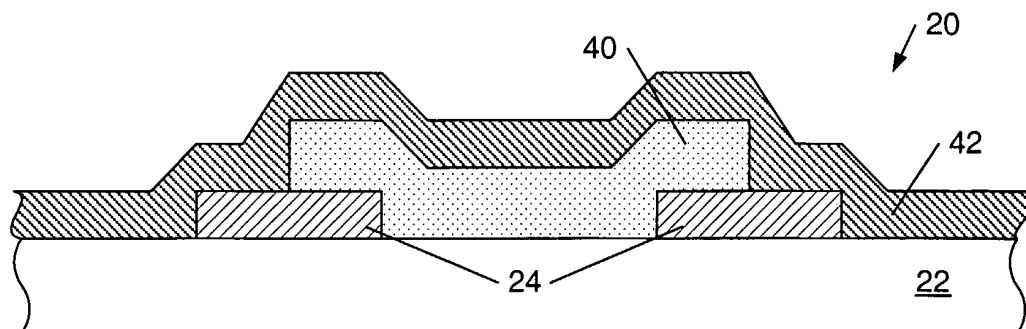


Fig. 4

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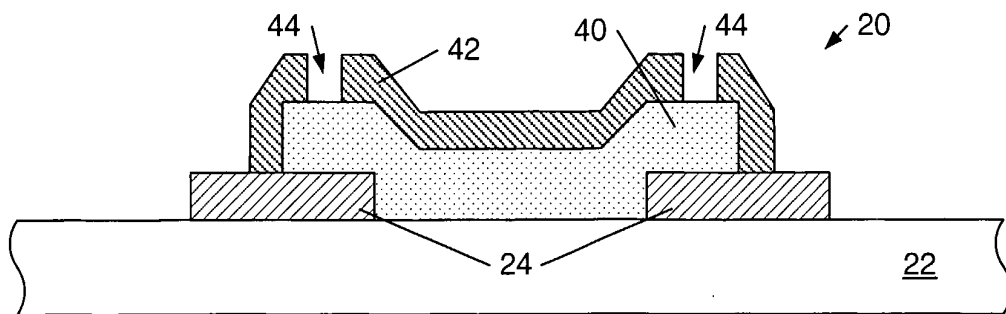


Fig. 5

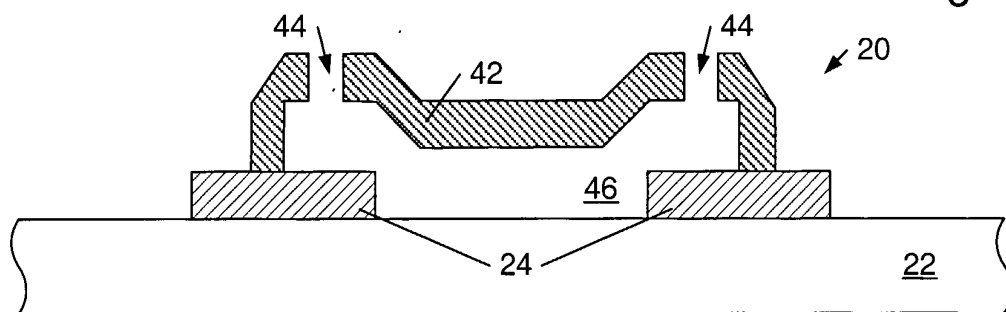


Fig. 6

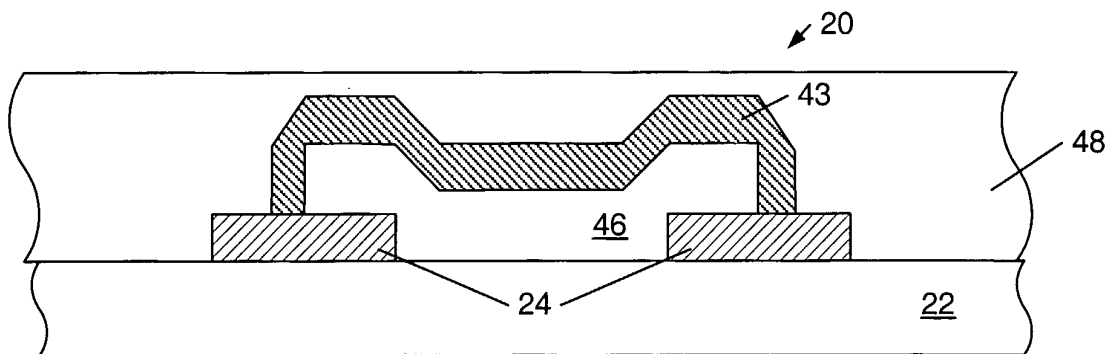


Fig. 7

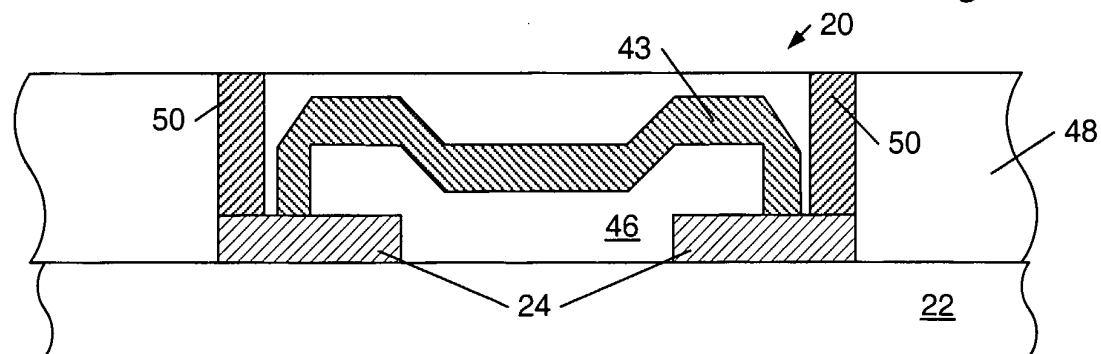


Fig. 8

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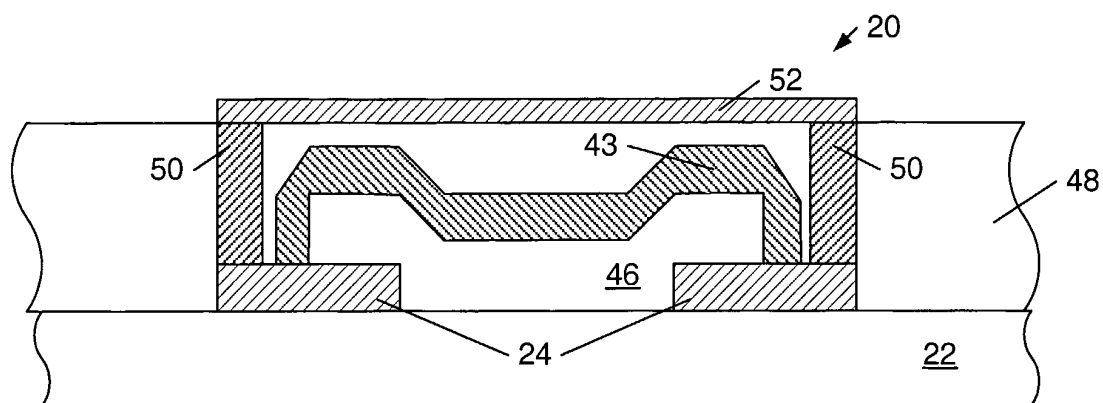


Fig. 9

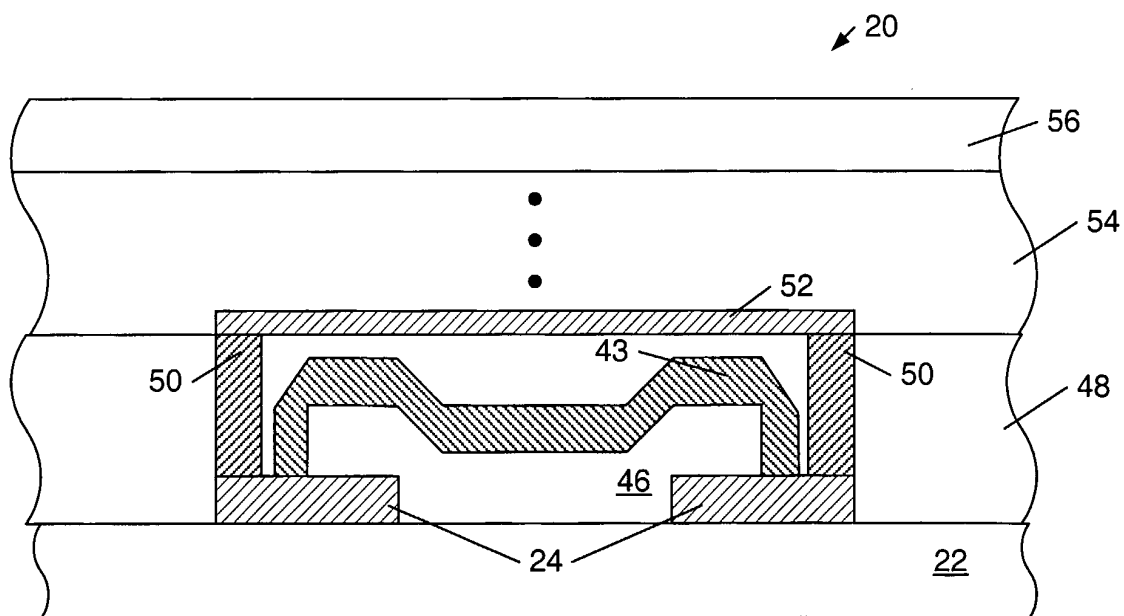


Fig. 10

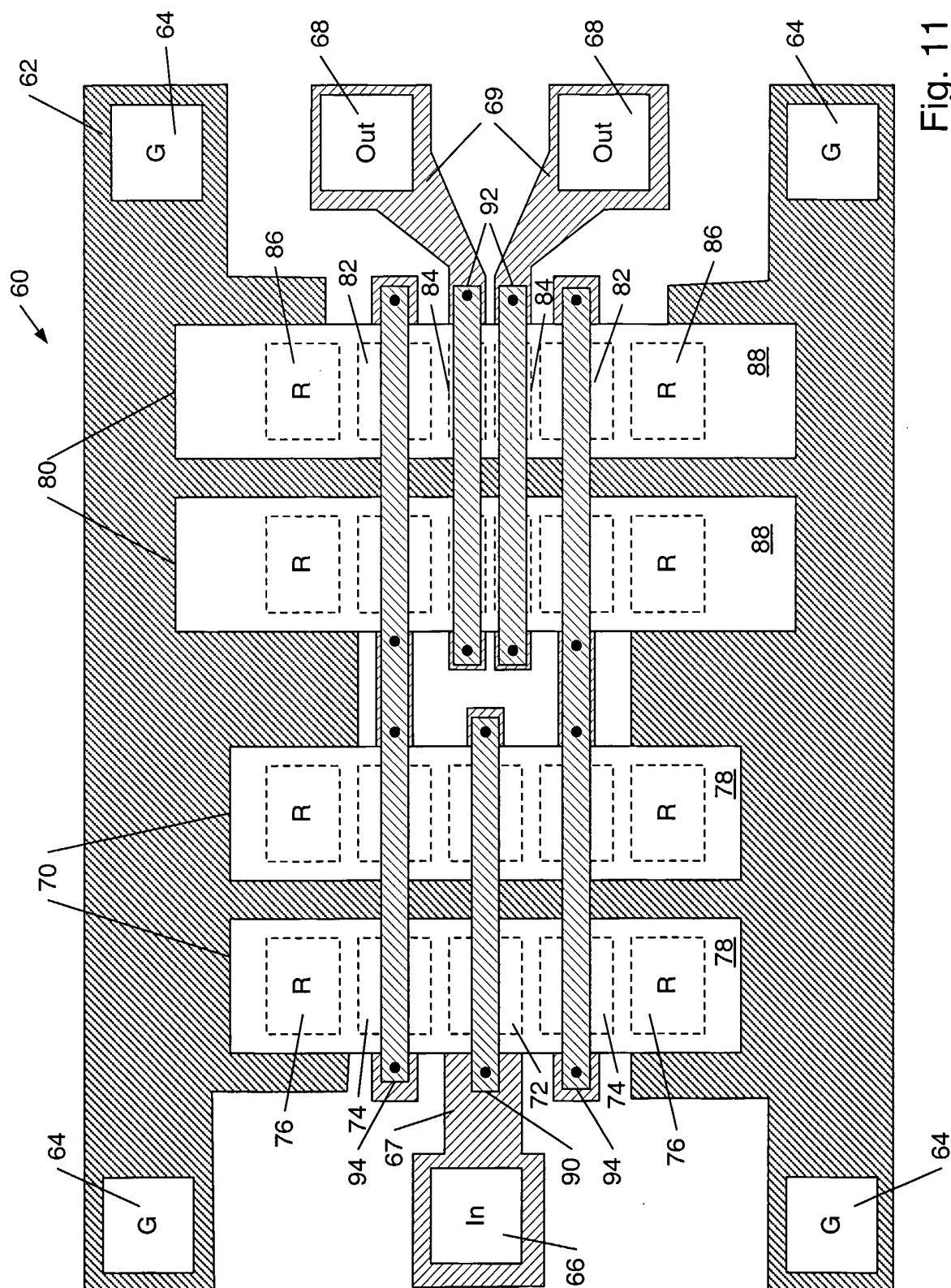


Fig. 11

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/009887

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03H9/05 H03H9/10 H03H9/64

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	abstract; figures 1-15 paragraphs '0016! - '0020!, '0023! - '0025!, '0027! - '0036!, '0039!, '0042!, '0043!, '0047! - '0062!, '0082!, '0083!, '0086!	9,10
Y	US 2003/155643 A1 (FREIDHOFF CARL B) 21 August 2003 (2003-08-21)	9,10
A	the whole document ----- -/--	1-8, 11-20

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

23 June 2005

Date of mailing of the international search report

12/07/2005

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US2005/009887

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	abstract; figures 1,2,11-14 paragraphs '0012!, '0017!, '0018!, '0040! - '0049!, '0064!, '0065! -----	4,15-20
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INTERNATIONAL SEARCH REPORT

International Application No

PCT/US2005/009887

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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