United States Patent

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[54] **PROGRAM SEQUENCE INFORMATION DISPLAY DEVICE**
12 Claims, 3 Drawing Figs.

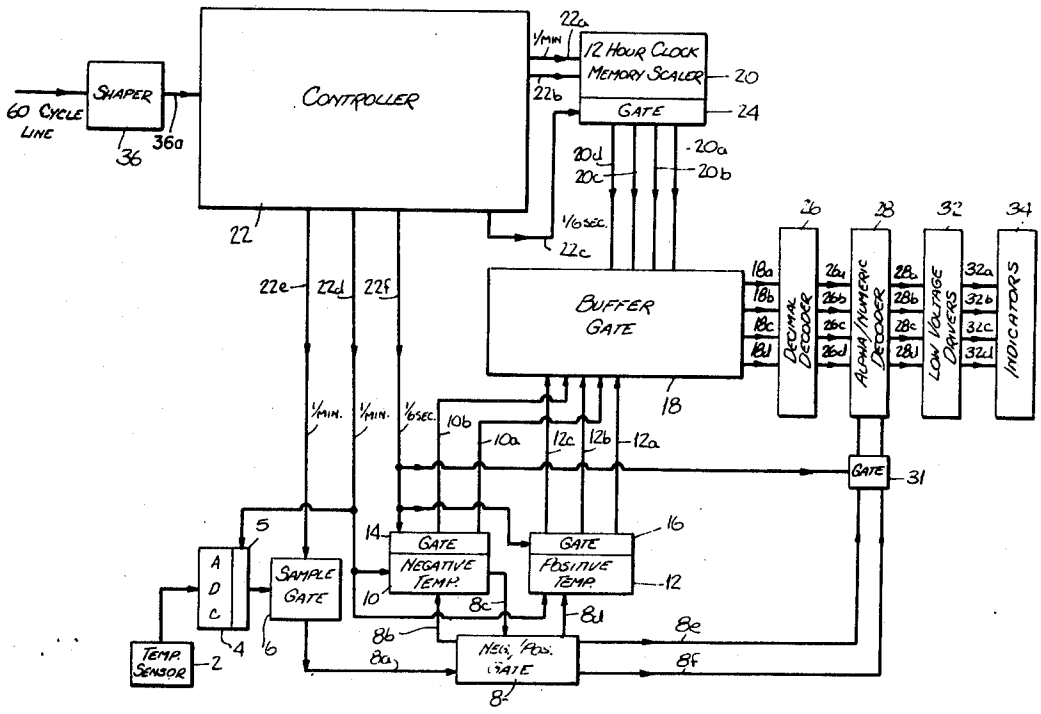
[52] **U.S. Cl.** **340/324,** 340/334
[51] **Int. Cl.** **H05b 39/00**
[50] **Field of Search** 340/324, 334

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ABSTRACT: An all electronic display device for sequentially displaying information. The information to be displayed is converted into the form of binary coded decimal pulses which are in turn converted into decimals in electronic form. By appropriate gating circuitry, the information is sequentially displayed during predetermined intervals of time and the information is updated at longer predetermined intervals of time.



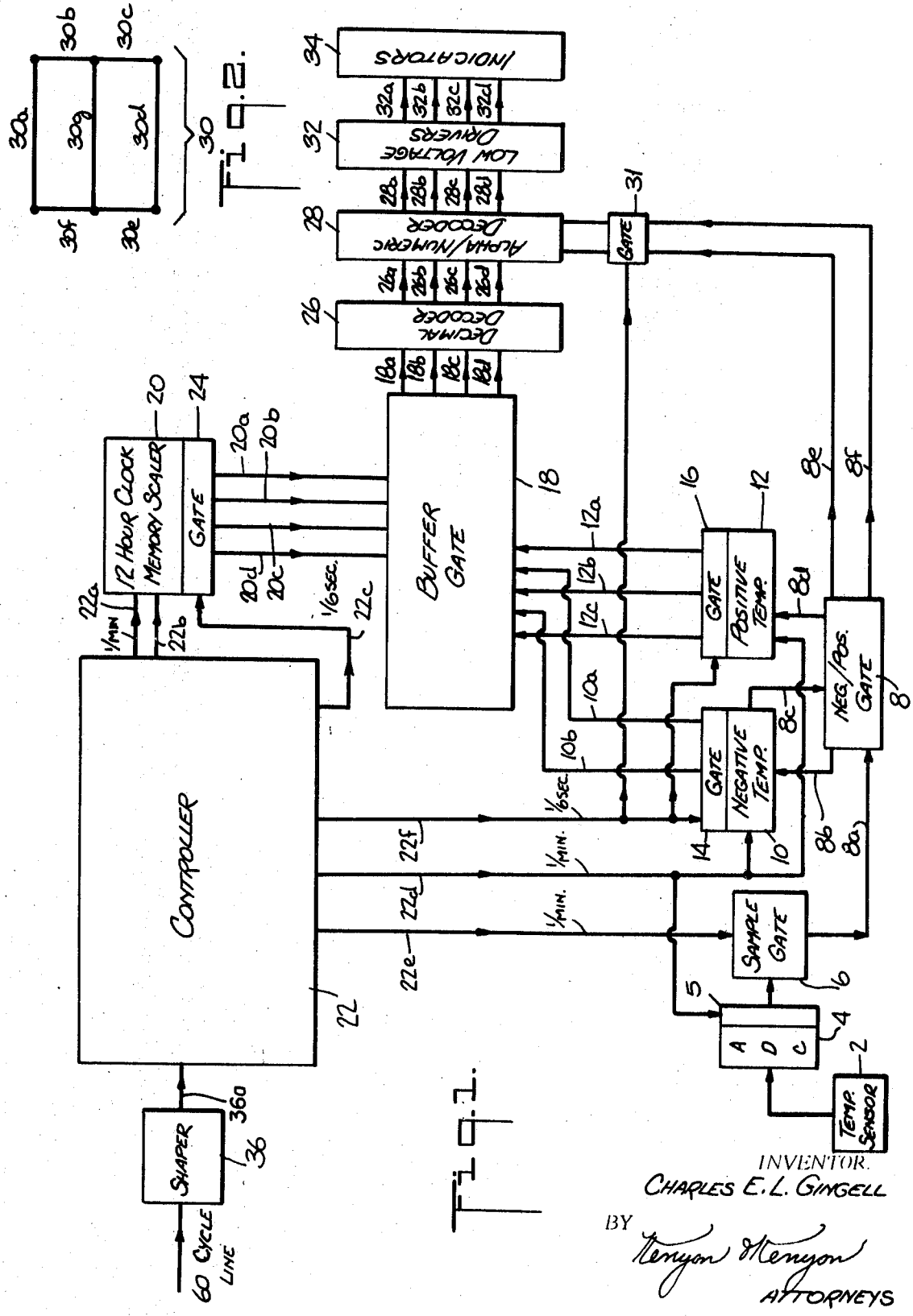


Fig. 2.

Fig. 1.

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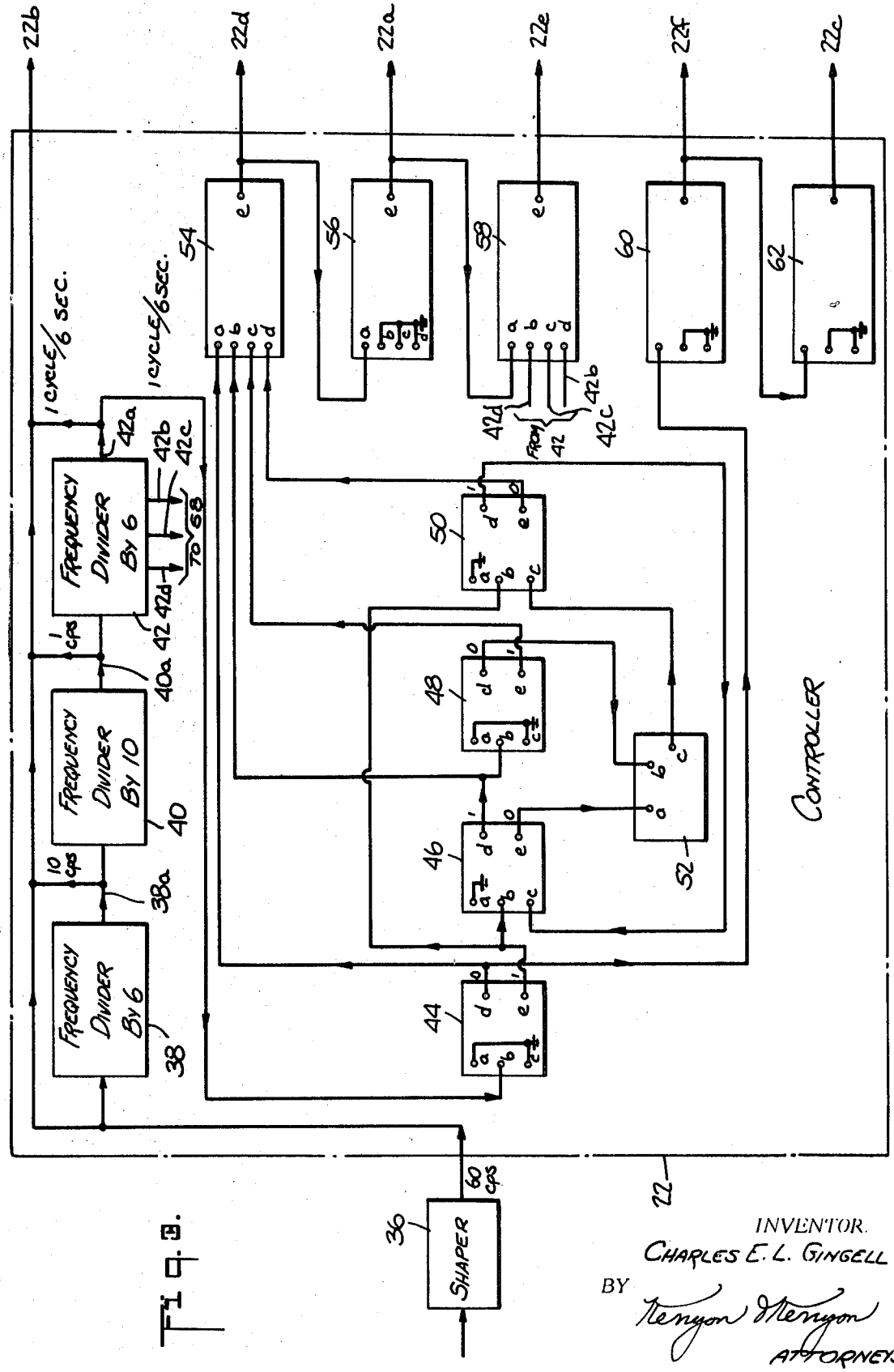


FIG. 3.

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PROGRAM SEQUENCE INFORMATION DISPLAY DEVICE

BACKGROUND OF THE INVENTION

This invention relates to information display systems and particularly to information display systems wherein it is desired to sequentially display information at an arbitrary interval of time as well as update the information to be displayed at a greater interval of time.

The use of display devices in the advertising as well as other media is well known. These, however, have comprised either mechanical or electromechanical display apparatus and have generally utilized cam mechanisms and bulky switching devices. Typically, the display device of the prior art contained a plurality of bulky contact-swtiching devices connected to a display panel. These contacts were opened and closed to light appropriate lamps on the display panel. A set of such contacts was provided for each type of information sought to be displayed and cam means were provided to shift control of the lamps on the display panel between the sets of contacts corresponding to the various types of information to be displayed, thereby providing the desired sequence of display. The disadvantage of the prior art display devices reside in their unwieldy size due partially to the bulky switching equipment and cam mechanism employed therein. In addition to their unwieldy size in volume as well as in weight the prior art display devices are extremely cumbersome to repair. If a prior art display device was in need of repair only a skilled mechanic in the art with great difficulty and much expense could accomplish the repair. In addition, once a prior art display device had been built to display time and temperature it would be very cumbersome if not virtually impossible to alter the device to display time and a worded message or to control a traffic system. It would also be very difficult to alter the device to change the display cycle frequency. Other disadvantages of prior art display devices reside in the fact that the input power requirements are generally high; that they do not lend themselves readily to remote control operations; that they have at least some moving parts which, of course, increases the maintenance of the device and finally, the prior art display devices contain many switches which can cause troublesome arcing and burning out of contacts.

SUMMARY OF INVENTION

With these problems with prior art display devices in mind, it is an object of my invention to provide a display device which has no cam mechanisms or bulky switching devices.

It is a further object of my invention to provide a display device which is all electronic.

It is a still further object of my invention to provide a display device which is very compact and very light in weight.

It is a still further object of my invention to provide a display device which is comprised of no moving parts.

It is a still further object of my invention to provide a display device which can be repaired easily, inexpensively and by one unskilled in the art.

It is a still further object of my invention to provide a display device in which either the type of information to be displayed can be changed or the timing cycle can be changed very easily, very inexpensively by simply replacing a card of electronics.

It is a still further object of my invention to provide a display device which can be adapted to sequentially display information and/or used to control a traffic light system and/or used to control any program sequence information display system.

These objects and others are achieved by my invention in which the information which is to be sequentially displayed is first converted electronically to binary coded decimal pulses. These binary coded decimal pulses are electronically converted to decimal form, one set for each set of information to be sequentially displayed. Each set of binary coded decimal pulses is applied in sequence to a buffer unit in accordance with strobe pulses applied to gates associated with each set of information to be displayed. The output of the buffer unit is converted electronically to pure decimal or alpha/numeric form which can be applied to high or low level indicator units.

For a fuller understanding of the nature and objects of the invention, reference should be had to the following detailed description taken in connection with the accompanying drawings in which:

FIG. 1 is a diagrammatic view of the complete mechanism which provides for displaying the sequence of time and temperature displays on a display panel;

FIG. 2 is a view of the configuration of bulbs which can represent the numerals from 0 to 9;

FIG. 3 is a view of the portion of the present invention which provides for the control signals for regulating the timing of sequential display.

Referring now to the drawings, and to FIG. 1 in particular, my invention is shown as embodied in a display mechanism adapted to measure and sequentially display time and temperature. The temperature is measured by a temperature sensor indicated at 2. The temperature sensor 2 may be any conventional device which senses the temperature and converts this information into an electric signal for use in display. For example, and by way of illustration, the temperature sensor 2 might be a single transistor connected to an emitter follower through appropriate circuitry. In that case the single transistor would be constrained to operate in a range of linear change of base/emitter voltage with a change of temperature. This voltage would then be measured from the single transistor buffered by an emitter follower. This method of temperature sensing is well known in the art and the values of the elements in the circuitry involved may be determined by methods well known in the art and will depend generally on the characteristics of the transistors used as well as the temperature range to be measured, which for the purpose of the present illustration we may take to be from −20 ° F. to +199° F. Of course, this range is purely arbitrary and is used to illustrate the inventive concepts of my invention and should not be interpreted as a limitation on its range of operation. For this illustration of the temperature sensor 2, the voltage measured, is fed via an emitter follower from the temperature sensor 2 to an analog to digital converter 4, a device well known in the art. The analog to digital converter 4 receives the signal from the temperature sensor 2 and converts this analog signal to a sequential series of pulses the frequency of which changes with the amplitude of the input signal. In other words the output of the analog to digital converter is a linear frequency approximation to the input signal. By way of illustration a typical analog to digital converter comprises an integrator, a discriminator and a switch. The signal from the temperature sensor 2 is fed into the integrator which charges up a capacitive circuit. When the capacitive circuit reaches a predetermined level, let us say 4 volts by way of illustration, this triggers the discriminator circuit which feeds back, through an electronic switch, a predetermined opposite charge into the capacitive circuit. This opposite charge tends to discharge the capacitive circuit, turning the discriminator off and allowing the capacitive circuit to charge up again to the triggering level. This cycle continues linearly and follows the input signal i.e. the frequency of the output pulses will increase and decrease with the input voltage. The output pulses from the analog to digital converter 4 are next led to a prescaler 5. The prescaler 5 scales down the frequency of the pulses from the analog to digital converter 4 so that the output of the prescaler 5 is a pulse train of frequency in cycles per second equal to the temperature in degrees plus 20. The output pulses from the prescaler 5 are next led to a sample gate 6. The sample gate 6 serves two functions. First it acts as a gate wherein it will allow a first signal to pass through it only when it is activated by a second signal applied to it. Gating circuitry of this nature is generally known in the art. Secondly, the sample gate 6 shapes the pulses that it receives from the analog to digital converter 4. The output of this shaping circuitry comprises well defined pulses of steeply rising and falling edges. The output of the sample gate 6 is led into a negative/positive gate 8 along input

wires designated as 8*a*. The pulses which are fed into the negative/positive gate **8** along the input wires 8*a* are immediately fed to a negative temperature memory scaler **10** through wires 8*b*. The negative temperature memory scaler **10** starts with a count of −20 and then counts in a negative direction to zero. When the negative temperature memory scaler **10** has reached a count of zero there is an electronic change over to a positive temperature memory scaler **12**. The pulses which were applied to the negative/positive gate **8** through the wires 8*a* are transferred from the negative temperature memory scaler **10** to the positive temperature memory scaler **12**. The positive temperature memory scaler **12** then continues to counting in a positive direction from zero to +199 for the purposes of illustration. The electronic change over from the negative temperature memory scaler **10** to the positive temperature memory scaler **12** may be accomplished in several equivalent ways. By way of illustration, this change over may be accomplished by causing the negative temperature memory scaler **10** to act as a short circuit with respect to the incoming pulses which enter negative temperature memory scaler **10** through lines 8*b*. These pulses would then go directly from line 8*b* to line 8*c* without further counting being registered in the negative temperature sensor. According to the preferred embodiment of my invention, the pulses on wires 8*c* are routed through the negative/positive gate **8** and out again over wires 8*d* to the positive temperature memory scaler **12** where the counting is registered from zero to +199 in the illustration. Of course it would be equivalent if the pulses on wires 8*c* were led directly into the positive temperature memory scaler **12**, thus bypassing the negative/positive gate **8** en route from the negative temperature memory scaler **10** to the positive temperature memory scaler **12**. Another possible method of effectuating the electronic change over when the negative temperature memory scaler **10** reaches a count of zero, which is not shown would be to have the negative temperature memory scaler **10**, on the count of zero, re-route the pulses coming in on the wires 8*a* into the negative/positive gate **8**, which at the same time causes the pulses coming in on line 8*a* to go directly to the positive temperature memory scaler **12** through wires 8*d*. To summarize the operation of the temperature memory scaler portion of my invention, it can be seen that the shaped pulses from the analog to digital converter **4** is a linear sequential train of pulses which is a direct representation of the output of the temperature sensor **2**. These pulses are sampled by the sample gate **6** and gated by the sample gate **6** to the negative temperature memory scaler **10**. The negative temperature memory scaler **10** consists of two reverse memory scalers, reverse in the sense that these scalers count backwards from a predetermined level as pulses are sent through it. The first reverse memory scaler has a scale of 10 and the other reverse memory scaler has a scale of two. For the range of −20° F to +199° F given in the present illustration, the negative temperature memory scaler **10** is so arranged that when the first pulse of the sequential signals enters the negative temperature memory scaler **10** on wires 8*b* the first reverse memory scaler counts the pulse and goes from zero to nine and at the same time the second negative memory scaler goes from zero to one, thus a reading of −19° is seen on the output of the negative temperature memory scaler **10** after it has counted the first pulse through it. The first and second reverse memory scalers are so connected that the second will not receive pulses to count unless the first has a reading of zero. When the second pulse enters the negative temperature memory scaler **10** on wires 8*b* the first reverse memory scaler will receive it and its count will go from nine to eight but the second reverse memory scaler will not receive the second pulse since the count on the first reverse memory scaler was not zero when the pulse entered the negative temperature memory scaler **10**. Thus, the output of negative temperature memory scaler **10** will be −18 after the second pulse. On succeeding pulses the first reverse memory scaler will run down through eight, seven, etc. to one and zero while the second reverse memory scaler will remain at one. On the very next pulse after the first reverse memory scaler registers zero the first reverse memory scaler will go from zero to nine and the second reverse memory scaler, because the first reverse memory scaler had registered a zero, will receive the pulse and go from one to zero. On succeeding pulses the first reverse memory scaler will again run down through nine, eight, seven, etc. to zero. When the first reverse memory scaler has a count of zero there will be a coincidence of a count of zero in both the first and second reverse memory scalers. When this occurs the negative temperature memory scaler **10** is adapted to ensure that the next pulse that it receives is not counted by the negative temperature memory scaler **10** but is sent to the positive temperature memory scaler **12** through the negative/positive gate **8**. At the same time the negative temperature indicator signal which had been on wires 8*e* is switched to wires 8*f* and become a positive temperature indicator signal. The positive temperature memory scaler **12** is a conventional scaler of the type well known in the art. This scaler operates in the reverse of the negative temperature memory scaler **10** and operates in the upward counting direction. The positive temperature memory scaler of this illustration with an upper temperature range of +199° F. has three conventional positive memory scalers with scales of 10, 10 and two respectively. The first two scalers reset to zero at the count of 10 and the third scaler resets to zero at the count of two. The output of the negative temperature memory scaler **10** and the positive temperature memory scaler **12** are in the form of binary coded decimals and are gated respectively through gate **14** and gate **16**. The output of gate **14** is carried on wires **10***a* and **10***b*. Wires **10***a* carry the binary coded decimal representation of the units of negative temperature and wires **10***b* carry the binary coded decimal representation of the 10's of negative temperature. The output of gate **16** is carried on wires **12***a*, **12***b* and **12***c*. Wires **12***a* carry the binary coded decimal representation of the units of positive temperature, wires **12***b* carry the binary coded decimal representation of the tens of positive temperature and wires **12***c* carry the binary coded decimal representation of the hundreds of positive temperature. The wires **12***a*, **12***b* and **12***c* feed the binary coded decimal representation of the temperature into a buffer gate **18**. The function of the buffer gate **18** will become apparent shortly. Time is measured and prepared for display by a 12-hour-clock memory scaler **20**. The 12-hour-clock memory scaler **20** received pulses at the rate of 1 pulse per minute from a controller unit **22** on wires **22***a*. The controller unit **22** is the heart of the present invention and will be described in more detail below. The 12-hour-clock memory scaler comprises four memory scalers. The first memory scaler has a scale of 10 and resets to zero on a count of 10. The second memory scaler has a scale of six and resets to zero on a count of six. These two memory scalers register the minutes. The third memory scaler has a scale of 10 and resets to zero on a count of 10. The fourth memory scaler has a scale of two and it is so adapted to act with the third memory scaler such that the third and fourth memory scalers reset to one on a count of 13, hence giving a time change of from 12:59 on the four memory scalers to 1:00 instead of 13:00. The output of the 12-hour-clock memory scaler is gated through gate **24** on wires **20***a*, **20***b*, **20***c*, and **20***d* to the buffer gate **18**. Wires **20***a* conducts the binary coded decimal representation of the units of minutes and comprises four wires, Wires **20***b* conducts the binary coded decimal representation of the 10's of minutes and comprises three wires. Wires **20***c* conducts the binary coded decimal representation of the units of hours and comprises four wires. Wires **20***d* conduct the binary coded decimal representation of the 10's of hours and comprises one wire. The binary coded decimal outputs from the clock memory scaler **20** and from the negative and positive temperature scalers **10** and **12** respectively must pass through the buffer gate **18**. The buffer gate **18** performs two functions. First, it is capable of accepting, sequentially, information from the 12-hour-clock memory scalers **20** on the one-hand and the negative and positive temperature memory scalers **10** and **12** respectively. Secondly, it converts each bi-

nary coded decimal pulse from each decimal position into a nonambiguous condition for decoding. For example, the output of the 12-hour-clock memory scaler appearing on wires **20***a* represent in binary code the units of minutes. The wires **20***a* comprise four wires which represent 1, 2, 4 or 8 when energized. Thus the decimal numbers from zero to nine can be represented on wires **20***a* by energizing the appropriate wires representing 1, 2, 4 and 8. The output of the buffer gate **18** corresponding to the input on wires **20***a* let us say appears on wires **18***a*. Whereas wires **20***a* comprise four wires representing 1, 2, 4 and 8 the wires **18***a* comprise eight wires representing 1, $\overline{1}$, 2, $\overline{2}$, 4, $\overline{4}$, 8 and $\overline{8}$. In other words on wires **18***a* the lack of a **4** component, for example, is represented by a signal on wire $\overline{4}$ whereas the lack of a **4** component on wires **20***a* is represented by the lack of a signal on the wire **4**. This eight wire method of decimal decoding is completely unambiguous because no combination of signals is ever repeated, whereas with a four wire method of decimal decoding of the digits 1 to 9 the combination of signals representing the digit 1 is included in the representation of the digits 1, 3, 5, 7, 9. The outputs of the buffer gate **18** are fed to a decimal decoder **26** along lines **18***a*, **18***b*, **18***c* and **18***d* as hereinabove described. The decimal decoder converts the binary coded decimal representation of each decimal position into its decimal form by methods and devices well known in the art. For example, for each set of wires **18***a*, **18***b*, **18***c* and **18***d* coming into the decimal decoder **26** from the buffer gate **18** there is a corresponding group of wires **26***a*, **26***b*, **26***c*, **26***d* each with 10 wires corresponding to the decimal numbers zero through nine. So if on wires **18***a*, for example, the decimal to be represented is five, then the wires of **18***a* will have signals on the following wires: 1, $\overline{2}$, 4, $\overline{8}$. This particular input on wires **18***a* would cause the decimal decoder **26** to produce a signal on that wire of wires **26***a* which corresponds to the decimal number five. The outputs of the decimal decoder **26** are fed into an alpha/numeric decoder **28**. The alpha/numeric decoder **28** is well known in the art. One can better understand the operation of the alpha/numeric decoder **28** by reference to FIG. **2** where in a configuration of lamps **30** are shown which comprises seven lamps designated by **30***a*, **30***b*, **30***c*, **30***d*, **30***e*, **30***f* and **30***g*. It can be seen from configuration **30** of FIG. **2** that the numeral three can be displayed if lamps **30***a*, **30***b*, **30***c*, **30***d* and **30***g* are actuated. Thus, referring back to FIG. **1**, for each set of wires **26***a*, **26***b*, **26***c*, and **26***d* coming into the alpha/numeric decoder **28** from the decimal decoder **26** there is a corresponding set of wires **28***a*, **28***b*, **28***c*, and **28***d* each with seven wires corresponding to the seven elements **30***a* through **30***g* of configuration **30** of FIG. **2** which are needed to represent any of the decimal numbers zero through nine. Then, as above-described, if the output of the buffer gate **18** on wires **18***a* is the binary coded decimal five then the wires 1, $\overline{2}$, 4, $\overline{8}$ will carry signals of the wires **18***a*. These signals will enter the decimal decoder **26** and produce a signal on the wire representing the decimal five on the wires **26***a*. This signal will enter the alpha/numeric decoder **28** and will produce a signal on those wires of wires **28***a* which would correspond to the elements **30***a*, **30***f*, **30***g*, **30***c* and **30***d* of the configuration **30** of FIG. **2**. The negative and positive temperature indicator signals on wires **8***e* and **8***f* are gated into the alpha/numeric decoder **28** through a gate **31**. Of course, the above description is by way of illustration only and it should be fully realized that alpha/numeric decoders are readily available in the art which could produce alphabetic and punctuation as well as numerals. The present illustration of my invention is for a sequential display of time and temperature but of course my invention is equally well adapted to sequentially display time and a message, for example. In that case, an alpha/numeric decoder would be used which was capable of coding into an alphabet, punctuation as well as numerals. For the purpose of the present illustration I have shown in FIG. **1** that the output of the alpha/numeric decoder **28** is fed to a low voltage driver **32**. The low voltage driver **32** has four discrete sections each adapted to receive one of the four decimal representations. Each section is a transistor amplifier driven for indicators **34** such as "Data Lite" or like indicators. For example, a positive voltage appearing on one of the wires of wires **28***a*, let us say the wire corresponding to the lamp **30***a* of FIG. **2**, will turn NPN transistors to saturation causing a current through lamp **30***a*. The lamp drive is through the NPN transistors, the collectors of which are connected through the lamps to a positive potential, for example 24 volts. Of course, the outputs from the alpha/numeric decoder **28** could be fed into a high-voltage driver, not shown. Such a high-voltage driver is the Triac. A Triac is a newly developed device that is energized by an alternating current and triggered by a direct current. The Triac operates quite similarly to the low-voltage driver **32** except that, although usually unnoticed, the lamps do in actual fact extinguish as in a normal electric lamp. The Triac, as well as switching high potentials, can pass heavy current and unlike relays, are entirely noiseless in operation.

The above has been a detailed description of how temperature and time are measured, coded, decoded and prepared for display in the present illustration of my invention. The most important aspect of my invention, however, resides in the method and means of controlling the cycle of sequential display. This control is provided by the controller **22**. A raw 60 cycles from the line is fed into a shaper **36**. The shaper **36** receives the line at about the 6 volt level. The sine waves of the line are changed to sharp spikes which are required to activate the micrologic. Thus, the output of the shaper **36** comprises well defined pulses of steeply rising and falling edges. Shapers of this nature are readily available in the art. The output of the shaper **36**, the 60 cycle pulses of steeply rising and falling edges, are fed into the controller **22**. The controller **22** comprises a plurality of micrologic scalers which are so arranged that when the controller **22** receives the 60 cycle pulses from the shaper **36** the controller **22** emits the following pulses for the purpose of controlling the cycle of sequential display of time and temperature as above-described, the controller **22** emits 1 clock pulse per minute of adequate duration on wires **22***a* to the 12-hour-clock memory scaler **20**. In addition, the controller emits calibration pulses on line **22***b* at frequencies of 10 pulses per second and 1 pulse per second and pulses of other frequencies as needed to the 12-hour-clock memory scaler **20**. Further, the controller **22** emits pulses every 12 seconds which are of 6 seconds duration on wires **22***c* to the gate **24** which allows the 12-hour-clock memory scaler **20** display its count for 6 seconds every 12 seconds. The controller **22** emits "reset" pulses of short duration once a minute to the temperature scalers **10** and **12** and the negative/positive gate **8** on wires **22***d*. The controller **22** so coordinates the "reset" pulses generated on wires **22***d* with the pulses generated on wires **22***a* so that the "reset" pulses are generated 6 seconds before the pulses on wires **22***a*. Further, the controller **22** so coordinates the "reset" pulses generated on wires **22***d* with the pulses generated on wires **22***c* so that whenever a pulse is generated on wires **22***d* a pulse is also generated on wires **22***c*. The controller **22** emits a "sample" pulse of 1 second duration every minute to the sample gate **6** on wires **22***e*. The controller **22** so coordinates the "sample" pulses generated on wires **22***e* with the pulses generated on wires **22***d* so that the sample pulses are generated 1 second after the pulses generated on wires **22***d*. Further the controller **22** coordinates the "sample" pulses generated on wires **22***e* with the pulses generated during a period when a pulse is generated on wires **22***c*. This coordination of the pulses generated on wires **22***e* with those generated on wires **22***c* will ensure that whenever the temperature is being "sampled" and updated once a minute by the generation of a pulse on wires **22***e*, time will be displayed by the gating pulses every 12 seconds which are of 6 seconds duration on wires **22***f* to the gate **14**, the gate **16** and the gate **31** which allows the output of the negative temperature scaler **10**, the output of the positive temperature scaler **12** and the outputs on wires **8***e* and **8***f* to be displayed for 6 seconds every 12 seconds. The controller **22** so coordinates the pulses on wires **22***f* with the pulses on wires

22c so that when there is a pulse on wires 22c there will not be a pulse on wires 22f and when there is a pulse on wires 22f there will be no pulse on wires 22c. This coordination by the controller 22 of the pulses generated on wires 22c with the pulses generated on wires 22f will ensure that the time and temperature will be alternately displayed for a duration of 6 seconds each. It is to be noticed that because of the coordination provided by the controller 22 that when the temperature is being "sampled" time is being displayed and that when the 12-hour-clock memory scaler 20 is receiving a pulse on line 22a to advance its output by 1 minute the temperature will be displayed.

Referring now to FIG. 3 I will describe the controller 22 in more detail. Line voltage of 60 cycles per second is applied to the shaper 36. As described the shaper 36 changes the 60 cycle sinusoidal line into 60 cycle pulses with rapidly rising and rapidly falling edges especially adapted to activate the micrologic portion of my invention. The shaper 36 feeds these 60 cycle pulses into the controller 22 on wire 36a. Inside the controller, these 60 cycle per second pulses are fed to a frequency divider 38. The frequency divider 38 is constructed from micrologic chips and has a construction well known in the art. The frequency divider 38 is so constructed that the output on the frequency divider 38 appearing on wires 38a are pulses having one-sixth of the frequency of the pulses fed into it on wires 36a. Therefore, the signal on wires 38a are pulses of frequency 10 per second. In addition to being fed into the frequency divider 38, the pulses on wires 36a are switched into a wire of wires 22b. These pulses are switched on the wires 22b to the 12-hour-memory clock scaler 20 for calibration purposes as hereinabove described. The pulses on wires 38a are fed into a frequency divider 40. The frequency divider 40, like the frequency divider 38, is constructed from micrologic chips but unlike the frequency divider 38 is so constructed that the output of the frequency divider 40 appearing on wires 40a is pulses of a frequency one-tenth of the pulses on wires 38a. Therefore, the pulses on wires 40a have a frequency of 1 cycle per second. In addition to being fed into the frequency divider 40, the pulses on wires 38a are switched into a wire of wires 22b. These 1 cycle per second pulses are switched on the wires 22b to the 12-hour-memory clock scaler 20 for calibration purposes as hereinabove described. The output of the frequency divider 40 is fed on wires 40a to a frequency divider 42. The frequency divider 42 is essentially the same as the frequency divider 38. The output of the frequency divider 42 is pulses of frequency one-sixth of the frequency of the pulses on wires 40a. Therefore, the output of the frequency divider 40 are pulses of frequency 1 cycle per 6 seconds. In addition to being fed into the frequency divider 42, the pulses on wires 40a are switched into a wire of wires 22b. These 1 cycle per 6 second pulses are switched on wires 22b to the 12-hour-memory clock scaler 20 for calibration purposes as hereinabove described.

The output of the frequency divider 42 is fed on wire 42a to a micrologic flip-flop 44. The flip-flop 44 is connected through a noninverting high voltage "OR" gate 52 to micrologic flip-flops 46, 48 and 50. The function of the "OR" gate 52 is to produce an output of high potential when either of its inputs are at a high potential and to produce an output of a low potential when both of its inputs are at low potential. The micrologic flip-flops 44, 46, 48 and 50 are so connected that they count the pulses on wires 42a and reset to zero on a count of 10. The flip-flop 44 registers the binary 1 and when it is in the "on" state its pin "e" is at a high potential and its pin "d" is at a low potential. When flip-flop 44 is in the "off" state its pin "d" is at a high potential and its pin "e" is at a low potential. The flip-flop 46 registers the binary 2 and when it is in the "on" state its pin "d" is at a high potential and its pin "e" is at a low potential. When flip-flop 46 is in the "off" state its pin "d" is at a low potential and its pin "e" is at a high potential. The flip-flop 48 registers the binary 4 and when it is in the "on" state its pin "e" is at a high potential and its pin "d" is at a low potential. When flip-flop 48 is in the "off" state its pin "d" is at a high potential and its pin "e" is at a low potential. The flip-flop 50 registers the binary 8 and when it is in the "on" state its pin "d" is at a high potential and its pin "e" is at a low potential. When flip-flop 50 is in the "off" state its pin "e" is at a high potential and its pin "d" is at a low potential. Assume that the flip-flops 44 and 50 are all in the "off" state. This would represent a count of zero. It can be seen that when the flip-flops 44 to 50 are in the "off" state that both of the inputs to the "OR" gate 52 will be at high potential. In other words pins "a" and "b" of "OR" gate 52 will be at high potential. Therefore, as hereinabove described, the output of the "OR" gate 52 at pin "c" will be at high potential. This high potential at pin "c" of "OR" gate 52 is applied to pin "c" of flip-flop 50 and thus keeps flip-flop 50 in a disabled state, i.e., unable to receive pulses at pin "b" of flip-flop 50 and so pin "d" of flip-flop 50 will be at a low potential. Thus flip-flop 46 will be held in an enabled state because a low potential on pin "d" of flip-flop 50 will cause a low potential on pin "c" of flip-flop 46. Tracing through the successive pulses on wires 42a into the flip-flops 44 to 50, it can be seen that on a count of six, flip-flops 46 and 48 are in the "on" state. When flip-flops 46 and 48 are in the "on" state the two inputs to the "OR" gate 52 are both at a low potential. Therefore, as hereinabove explained, the output of the "OR" gate 52 at pin "c" must be at a low potential. This then switches flip-flop 50 to an enabled state because pin "c" of flip-flop 50 will be at a low potential. The next count into flip-flop 44 on wires 42a will put flip-flop 44 in an "on" state. Now flip-flops 44, 46 and 48 are all in an "on" state thus making a count of seven. The next pulse on wires 42a will put flip-flops 44, 46 and 48 all in "off" states. However, before this occurs, the same pulse will put flip-flop 50 in an "on" state (flip-flop 50 having been enabled by the preceding pulse). When flip-flop 50 is thus switched to an "on" state pin "d" of flip-flop 50 is at a high potential thus pin "c" of flip-flop 46 is also at a high potential and is thereby disabled from receiving the next pulse. The next pulse on wires 42a into flip-flop 44 puts flip-flop 44 into an "on" state thus giving a total count of nine in the scalers (i.e. flip-flop 44 is in an "on" state; flip-flop 46 is in an "off" state; flip-flop 48 is in an "off" state and flip-flop 50 is in an "on" state). The next pulse on wires 42a into flip-flop 44 puts flip-flop 44 into an "off" state. The pulse from flip-flop 44 by passes flip-flop 46 (because it was disabled by the previous pulse on wires 42a) and resets flip-flop 50 to an "off" state. The flip-flops 44 to 50 are now all in the "off" state and the cycle is then repeated.

It is to be noticed that pin "d" of flip-flop 44, pin "d" of flip-flop 46, pin "e" of flip-flop 48 and pin "e" of flip-flop 50 are all connected to a low voltage "AND" gate 54. The function of the "AND" gate 54 is to produce an output only when all of its inputs are at a low potential. Only at a count of nine will pin "d" of flip-flop 44, pin "d" of flip-flop 46, pin "e" of flip-flop 48 and pin "e" of flip-flop 50 all be at a low potential. Therefore, the "AND" gate 54 will be switched on and produce an output pulse at a count of nine. At a count of 10 all of the flip-flops 44 to 50 are switched to the "off" state and therefore pin "d" of flip-flop 44 will be at a high potential and thus the "AND" gate 54 will switch off again. So at a count of nine the "AND" gate 54 will produce a positive going pulse on wires 22d which will remain at a predetermined positive level for 6 seconds until a count of 10 at which time the pulse will be negative going to ground. Thus the reset pulses on wires 22d are produced as hereinabove described. It is the positive going edge of these pulses, occurring at a count of nine, which actuates the reset circuitry. The output from the "AND" gate 54, in addition to being produced on wires 22d are led to a gate 56. The output of gate 56 is a pulse similar to the output of gate 54 except that it is the negative going edge of the pulse which actuates the 1 pulse per minute on the minute on the wires 22a. The output from the gate 56, in addition to being produced on wires 22a, is fed to a gate 58. In addition to this input to gate 58 there are three outputs from the frequency divider 42 counts pulses at the rate of one per second and the

three outputs from this unit are such that it will allow the output of gate **56** to pass through the gate **58** for only one second and beginning one second after the count of nine occurs. Thus the output of the gate **58** on the wires **22***e* is the "sample" pulse, hereinabove described, which is of one second duration and which occurs one second after the reset pulse is actuated on wires **22***d*. The pin "*d*" of flip-flop **44**, in addition to being connected to the "AND" gate **54**, is also connected to a gate **60**. The output of gate **60** is a pulse train with a period of 12 seconds; the first 6 seconds at a positive potential and the second 6 seconds at a ground potential. The output of the gate **60** is fed on wires **22***f*. In addition to being fed on wires **22***f*, the output of gate **60** is led to a gate **62**. The output of gate **62** is also a pulse train with a period of 12 seconds; the first 6 seconds at ground potential and the second 6 seconds at a positive potential. The output of gate **62** is fed on wires **22***c*. This electronic coordination of the pulses on wires **22***f* and wires **22***c* produces the desired sequential display as hereinabove described. It is thus that the controller **22** controls the frequency and timing of the sampling of the information to be displayed as well as controls the timing of the sequential display.

The foregoing is considered as illustrative only of the principles of my invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation shown and described, and accordingly all suitable modifications and equivalents may be resorted to, falling within the scope of the invention as claimed.

What is claimed is:

1. A program sequence information display device comprising:

a plurality of electronic information sensing means to sense and convert the information from each information source to be displayed into a sequential series of pulses;

a plurality of electronic counting means to sample the sequential series of pulses from the information sensing means and to convert these pulses into a simultaneous binary coded decimal output;

a plurality of first gating means to allow the sequential series of pulses from the information sensing means to be sampled by the electronic counting means for a predetermined period of time;

a plurality of second gating means to allow the simultaneous binary coded decimal output of the electronic counting means to be displayed for a predetermined period of time;

a control means to actuate the first gating means and control the frequency and timing of the sampling of the information sensing means and to actuate the second gating means and control the frequency and timing of the display of the output of the electronic counting means.

2. A program sequence information display device according to claim **1** wherein the control means comprises a plurality of solid-state devices to convert a line voltage which enters the control means into a plurality of pulse trains of varying frequency to actuate said first and second gating means.

3. A program sequence information display device according to claim **2** wherein the plurality of solid-state devices comprises:

a shaping means to shape said line voltage and to generate therein pulses of sharply rising and falling edges;

a plurality of frequency scaling means operatively connected to said shaping means to receive said pulses of sharply rising and falling edges and to produce said pulse train of varying frequencies.

4. A program sequence information display device according to claim **3** wherein the frequency scaling means comprises:

a plurality of solid-state flip-flops to count said sharply rising and falling pulses and to generate a pulse after a preset number of counted pulses;

solid state logic circuitry operatively connecting said solid-state flip-flops to establish the number of said sharply rising and falling input pulses between successive output pulses from the plurality of flip-flops.

5. A program sequence information display device according to claim **1** wherein the electronic information sensing means comprises:

measuring means for receiving the information to be displayed and for generating an analog electronic signal which varies in a predetermined manner with the information to be displayed;

converting means for receiving said analog electronic signal from said measuring means and for generating a discrete electronic signal which varies in a predetermined manner with the information to be displayed.

6. A program sequence information display device according to claim **5** wherein the said measuring means is adapted to generate a continuous variable voltage signal which varies with the information to be displayed in a predetermined manner and wherein the converting means is an analog to digital converter which received the said variable voltage signal and generates a pulse train whose frequency varies proportionally to the voltage of said continuous variable voltage signal.

7. A program sequence information display device according to claim **1** wherein the said counting means comprises:

a plurality of scalers of various counting capacity adapted to receive pulses from the information sensing means; and

logic circuitry operatively connecting said scalers and adapted to have each scaler represent in count a decimal position of the information to be displayed.

8. A program sequence information display device according to claim **7** wherein the said scalers comprises a plurality of solid-state flip-flops so arranged with solid-state logic circuitry that the scalers sequentially count pulses from the information sensing means and displays this count in binary coded decimal form.

9. A program sequence information display device according to claim **1** wherein the first gating means comprises a solid-state "AND" gate to receive pulses from the control means and from the information sensing means and to pass the pulser from the information sensing means through to its output only when there is a coincidence of pulses into said "AND" gate from said control means and said information sensing means.

10. A program sequence information display device according to claim **1** wherein the second gating means comprises a solid-state "AND" gate to receive pulses from the control means and from the counting means and to pass the output from the counting means through to its output only when there is a coincidence of signals into said "AND" gate from said control means and said counting means.

11. A program sequence information display device according to claim **1** wherein the first gating means comprises a solid-state device to receive pulses from the control means and to lead said pulses to the information sensing means to actuate the output of said information sensing means whenever there is a pulse from said control means into said first gating means.

12. A program sequence information display device according to claim **1** wherein the second gating means comprises a solid-state device to receive pulses from the control means and to lead said pulses to the counting means to actuate the output of said counting means whenever there is a pulse from said control means into said second gating means.

UNITED STATES PATENT OFFICE

CERTIFICATE OF CORRECTION

Patent No. 3,611,347 Dated October 5, 1971

Inventor(s) Charles E. L. Gingell

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 6, line 64, after "generated" and before "during" insert --on wires 22c so that the pulses on wires 22e will be generated--.

Column 6, line 69, after "pulses" and before "every" insert --generated on wires 22c. The controller 22 generates pulses--.

Column 8, line 6, change "and" to --to--.

Column 8, line 75, after "42" and before "counts" insert --which are fed to gate 58. The frequency divider 42--.

Signed and sealed this 18th day of April 1972.

(SEAL)
Attest:

EDWARD M.FLETCHER,JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

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