A bandgap voltage generator includes a plurality of calibration transistors. A test circuit measures the bandgap reference voltage generated by the bandgap voltage generator and enables a subset of the calibration transistors to correct to the bandgap reference voltage.
FIG. 2A

FIG. 2B
FIG. 2C
FIG. 3

Bandgap Voltage Generator

Control Circuit

Output

Programmable Transistors

Memory
FIG. 5

Graph showing voltage (V) vs. temperature (°C) for different conditions:
- **Prior**
  - 1.24502 VG_BIMAX
  - 1.21447 VG_BTYP
  - 1.17954 VG_BIMIN

- **Proposed (after calibration)**
  - 1.21837 VG_BIMAX
  - 1.21447 VG_BTYP
  - 1.20407 VG_BIMIN

Temperature range: -40°C to 120°C.
Start

Check bandgap voltage at room temperature

Is 1.20 < V_G < 1.22?

Yes: Pass the sample → Stop

No: Is V_G < 1.20?

Yes: Decrement calibration code

No: Is V_G > 1.20?

Yes: Increment calibration code

FIG. 6
ULTRA LOW TEMPERATURE DRIFT BANDGAP REFERENCE WITH SINGLE POINT CALIBRATION TECHNIQUE

BACKGROUND

[0001] 1. Technical Field

The present disclosure relates to the field of bandgap circuits. The present disclosure relates more particularly to a low temperature drift bandgap circuit in integrated circuit dies.

[0002] 2. Description of the Related Art

Integrated circuits often include reference voltage generators that generate various reference voltages. The reference voltages can be used in a large number of applications including accurate reading of memory cells, phase locked loops, voltage controlled oscillators, analog circuits, digital signal processing circuits, etc. It is beneficial for a reference voltage to have a particular don't value without variation data processing or environmental factors.

[0005] Bandgap voltage generators are often used to generate a reference voltage that can be used in any circuit applications. Bandgap voltage generators rely on the bandgap between the conduction band and the valence band of a semiconductor. Bandgap energy is the energy required for an electron to make the transition from the valence band of a semiconductor material to the conduction band of the semiconductor material. Each semiconductor material has a bandgap particular to that material. Because the bandgap energy is a physical characteristic of the semiconductor material it can be relied on as a reference voltage to which other voltages can be compared. Thus, bandgap voltage generators that generate a voltage based on the bandgap of a semiconductor material are commonly used in integrated circuits in which a reliable reference voltage is desired.

[0006] In spite of the constancy of the bandgap energy, bandgap voltage generators are imperfect. Bandgap voltage generators include circuitry such as transistors, resistors, and amplifiers that imperfectly reproduce the bandgap voltage. In particular, bandgap voltage generators may generate a voltage that varies unacceptably with changes in temperature. This is due to problems that can occur and processing of the integrated circuit die.

[0007] FIG. 1 is a schematic diagram of a known bandgap voltage generator 20 implemented in integrated circuit die with a monocrystalline silicon substrate. The bandgap voltage generator 20 generates a bandgap reference voltage VG based on the bandgap energy of monocrystalline silicon.

[0008] The bandgap voltage generator 20 includes a first group of p type bipolar transistors Q1. In the example FIG. 1, there are n transistors Q1 connected in parallel with each other. The emitters of the transistors Q1 are coupled to the non-inverting input of an operational amplifier 22. The collector and base terminals of the transistors Q1 are coupled to ground.

[0009] Bandgap voltage generator 20 further includes a second group of p type bipolar transistors Q2. An example of FIG. 1, there are n*m transistors Q2 each connected in parallel with each other. Thus, the number of transistors Q2 is the number of transistors Q1 multiplied by a number m. The emitters of the transistors Q2 are coupled to a resistor R1. The base and collector terminals of the transistors Q2 are connected to ground.

[0010] The resistor R1 is coupled between the inverting input of the amplifier 22 and a resistor R2. The resistor R2 is coupled between the inverting input of the amplifier 22 and the train terminal of a PMOS transistor M1. The gate of the transistor M1 is coupled to the output of the amplifier 22. The source of the transistor M1 is coupled to the supply voltage VDD.

[0011] A resistor R3 is coupled between the non-inverting input of the amplifier 22 and the train terminal of a PMOS transistor M2. The gate of the PMOS transistor is coupled to the output of the amplifier 22. The source of the PMOS transistor M2 is coupled to VDD.

[0012] The output of the bandgap voltage generator 20 is the node between the resistor R3 and the drain of the transistor M2. The output of the bandgap voltage generator generates the bandgap voltage VG based on the bandgap of the semiconductor substrate.

[0013] The reference voltage VG is based on the base emitter voltage Vbe1 of the transistors Q1 and the factor m. In particular, the voltage VG is given by the following relation:

\[
VG = V_{be1} + \Delta V_{be} \times R2/R1
\]

The term Vbe1 is complementary to absolute temperature (decreases with increases in absolute temperature). The term VP is proportional to absolute temperature (increases with increases in absolute temperature). K is the ratio of R2 and R1.

\[\text{where }\]

\[V_C = V_{be1},\]

\[V_P = \ln(m) \times \frac{Kb \times T}{q}\]

and

\[K = \frac{R2}{R1}\]

The term VCG is complementary to absolute temperature (decreases with increases in absolute temperature). The term VP is proportional to absolute temperature (increases with increases in absolute temperature). K is the ratio of R2 and R1.

[0014] Designers of a bandgap voltage generator 20 according to FIG. 1 typically try to design the circuit so that the temperature complementary term VCG and the temperature proportional term VP balance each other over a wide range of temperatures so that the generated bandgap voltage VG varies little with temperature.

[0015] FIGS. 2A and 2B illustrate two graphs showing the dependence of Vbe1 and \(\Delta V_{be}\) on temperature. In the example of FIG. 2A, Vbe, which corresponds to VC in equation 3, varies by \(-2 \text{ mV per degree rise in Celsius}\), whereas \(\Delta V_{be}\), which corresponds to VP in equation 3, varies by 0.08 \text{ mV per degree Celsius}. It can be seen that these two values of VC and VP do not cancel each other out well. However, in the graph of FIG. 2B the term VP is multiplied by the constant K which is the ratio of R2 to R1. When multiplied by the factor K, VP more closely cancels VC as can be seen in the curve labeled VG, which is the sum of the two and is thus the final bandgap voltage VG from equation 3. The generated bandgap voltage VG curve on the graph on FIG. 2B has only a mild
curve with changing temperature. The constant K is selected to minimize the change in the generated bandgap voltage VG with temperature.

However, this solution suffers from some drawbacks. In particular, the absolute value of the base emitter voltage varies with the processing carried out on the semiconductor substrate during manufacture. Room temperature Vbe may vary slightly from one die to another based on processing. Furthermore, the slope of Vbe will vary with processing so that the VP and VC do not cancel the same way on each die. Thus, the bandgap voltage may drift with temperature from die to die.

These drawbacks can be seen with respect to the graphs in FIG. 2C. The upper graph on FIG. 2C discloses several curves of Vbe for different processes carried out to make a die. The middle line, labeled VBE_BTYP, starts at about 730 mV at the low temperature of -40° and drops to about 420 mV at a high temperature of 120° C. The upper line, labeled VBE_BIMIN, starts at about 850 mV and decreases to about 480 mV. The lower line, labeled VBE_BIMAX starts at about 700 mV and decreases to about 400 mV with increasing temperature. This graph also shows that for different processes Vbe starts at different values at room temperature.

The lower graph of FIG. 2C shows three curves representing the slope of Vbe for different processes. As can be seen, the slopes of Vbe with respect to temperature (dV/ dT) are different for the three different processes. Thus, a single design for a bandgap voltage generator will produce different bandgap voltages based on the process steps carried out in the manufacture of the semiconductor die.

BRIEF SUMMARY

One embodiment is an integrated circuit die having a tunable bandgap voltage generator including a plurality of calibration transistors. The tunable bandgap voltage generator can be calibrated before first use by testing the slope of Vbe and the starting point of Vbe and then enabling a certain number of the calibration transistors based on the test results. Thus, the bandgap voltage generator can be calibrated prior to use by the end customer.

In one embodiment, the bandgap voltage generator includes a calibration current path. The calibration transistors are placed in parallel in the calibration current path between the output of the bandgap voltage generator and ground. The bandgap voltage generator also includes a test circuit that tests Vbe and the slope of Vbe and then turns on select ones of the calibration transistors.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. 1 is a block diagram of a known band voltage generator.

FIGS. 2A and 2B are graphs of base emitter voltage characteristics vs. temperature for a single die.

FIG. 2C is two graphs of base emitter voltage characteristics vs. temperature for different processes.

FIG. 3 is a block diagram of a bandgap voltage generator according to one embodiment.

FIG. 4 is a schematic diagram of a bandgap voltage generator according to one embodiment.

FIG. 5 is a series of graphs of bandgap voltages for different processes according to one embodiment.

FIG. 6 is a flowchart of process for calibrating a bandgap voltage generator according to one embodiment.

DETAILED DESCRIPTION

FIG. 3 is a block diagram of an integrated circuit die including a bandgap voltage generator. The integrated circuit die includes a bandgap voltage generator which includes an output and a plurality of programable transistors. The bandgap voltage generator is coupled to a control circuit. A memory is coupled to the control circuit.

FIG. 6 is a flowchart of process for calibrating a bandgap voltage generator according to one embodiment. In order to ensure that the bandgap voltage generator generates bandgap voltage that does not vary greatly with each different process, the bandgap voltage generator includes a plurality of programable transistors. The control circuit measures the band voltage reference voltage generated by the bandgap voltage generator and compares the measured voltage to the data stored in the memory. The control circuit retrieves a calibration code from the memory corresponding to the measured bandgap voltage value. The control circuit that enables one or more of the programable transistors based on the calibration code. In particular, the calibration code indicates the subset of the programable transistors which should be enabled in order to calibrate the bandgap voltage generator so that the voltage it outputs varies less with temperature.

In one embodiment, the control circuit applies a particular calibration code and then measures the bandgap voltage again. The control circuit then compares the newly measured bandgap voltage to the data stored in the memory and performs further calibration if further correction to the bandgap voltages needed. The control circuit can continue this process until the bandgap voltage generated by the bandgap voltage generator is a satisfactory stable value over the expected range of operating temperatures.

FIG. 4 is a schematic diagram of a bandgap voltage generator according to one embodiment. The bandgap voltage generator includes a first group of n the type of bipolar transistors Q1 and a group of n*m transistors Q2. The bandgap voltage generator also includes a group n-k the type of bipolar transistors Q3 and a group of programable transistors all labeled Q3. The transistors Q1-Q3 all have gate and collector terminals connected to ground. The emitters of the group of Q1 transistors are connected to the non-inverting input of an amplifier. Each of the groups n, n*m, and n-k will usually have many transistors, but only one is shown in the figure.

The emitters of the group of n*m Q2 transistors are connected to a resistor R1. The emitters of the group of n-k Q3 transistors are connected to a resistor R2 and a resistor R3. The emitters of the programable transistors Q3 are coupled to respective switches 27 that receive a calibration code. The switches can couple or decouple the emitters of the Q3 transistors to the emitters of the group of n-k Q3 transistors. As shown in FIG. 4, some emitters start coupled to the resistors, with the switch 27 closed, as shown in the transistor labelled 25-1, while other transistors start with the switch 27
open, as shown with the transistors labelled 25-2. The resistor R1 is coupled between the emitters of the Q2 transistors and the inverting input of the amplifier 22. PMOS transistors M1-M3 each have their gate terminals coupled to the output of the amplifier 22 and there source terminals coupled to the high supply voltage VDD. A plurality of resistors R2 are each coupled to the respective drain terminals of the transistors M1-M3. The resistor R3 is coupled between the emitters of the group of n-Q3 transistors and the emitters of the group of p-k Q3 transistors.

Because the base terminals of the Q1 and Q2 transistors are grounded, the voltage on the emitter terminals of the transistors Q1 and Q2 corresponds to the respective base emitter voltages Vbe1, Vbe2 of the bipolar transistors Q1, Q2.

The amplifier 22 outputs a signal corresponding to the difference between Vbe1 and Vbe2 as described previously. The output of the amplifier 22 goes to the gate terminals of the transistors M1-M3. Because the gate terminals of the transistors M1-M3 receive the same voltage from the amplifier 22, and because the sources of the transistors M1-M3 receive the same voltage VDD, the same current flows through each of the transistors M1-M3.

The voltage at the drain of the transistor M3 corresponds to the bandgap voltage but might not be the same as the semiconductor substrate. However, as described previously, due to process variations the bandgap reference voltage generated by the bandgap voltage generator 20 can both be offset with respect to the bandgap of the semiconductor substrate and can vary with temperature in a manner that takes it outside the design tolerances.

In order to ensure that the bandgap voltage generator 20 generates a bandgap voltage that is within tolerance, the control circuit 32 as described previously measures the bandgap voltage at room temperature. The control circuit 32 then refers to the data stored in the memory 34 to find a calibration code that corresponds to the measured voltage. The control circuit 32 then outputs the calibration code to the switches 27 coupled between the calibration transistors Q3 and the resistor R3. Based on a calibration code, some number of the calibration transistors Q3 will be coupled to the resistors R2 and R3. In some cases, it will be required to close more switches 27, while in other cases, it will be required to open more switches 27. This allows a portion of the current flowing through the transistor M3 to pass through those of the transistors Q3 that were enabled by the calibration code. This causes the voltage drop across the resistor R2 to change, thereby adjusting the bandgap voltage reference output by the bandgap voltage generator 20.

In this manner, the bandgap voltage generator 20 can be quickly and easily calibrated, either up or down, to output a bandgap reference voltage that is more accurate at room temperature and that varies less with changes in temperature.

In one embodiment, there are two thousand calibration transistors Q3. About half of these will start with the switch 27 closed and half with switch 27 open. The switch 27 can an MOS transistor whose state is easily changed by application of a voltage to the gate, or it can be a fuse or anti-fuse that will be blown or connected as needed to achieve the desired voltage. Of course, those of skill the art will understand that more or fewer calibration transistors Q3 can be used in light of the present disclosure. Also, different types of circuits can be used for the calibration transistors 25 or the switches 27.

FIG. 5 shows graphs of a plurality of bandgap voltages from three different circuits that included the calibration transistors and structure of FIG. 4. The upper graph includes three curves for the respective three bandgap reference voltages prior to calibration. VG_BIMIN is the lowest voltages output of the three circuits, at 1.17954 volts; VG_BTYP is in the middle value at 1.21447 volts and VG_BIMAX is at 1.24502 Volts. Only one of these is within the acceptable range of about 1.21 Volts, so calibration is carried out on the other two.

The lower graph shows the outputs of these same circuits with their bandgap reference voltages after calibration. In this particular example, the target is to have a bandgap voltage above 1.2 V but less than 1.22 V. Namely, it is desired that at room temperature the bandgap voltage be in the range of 1.21 V with a tolerance of 0.009 V. After calibration, the output of the circuit with the middle voltage is unchanged since no calibration was carried out. The circuit that output the highest bandgap voltage has now been calibrated to be lower, at 1.21837 Volts, while the lower of the voltages of the three has been raised, to be about 1.20407 Volts. This is accomplished by connecting or disconnecting a selected number of the calibration 25 transistors to raise or lower the output of the bandgap voltage of that circuit. This is done by closing or opening the proper number of switches.

In the upper graph, the middle curve has a bandgap voltage of about 1.21 V at room temperature, the upper curve has a bandgap voltage of about 1.24 V at room temperature, and the lower curve has a bandgap voltage of about 1.18 V at room temperature. There is a range of about 0.06 V at room temperature between the three curves. The difference in the bandgap voltages is due to process variations. As can be seen, while the target bandgap voltage when the dies was made is 1.21 V, the actual voltage that was produced due to the process variations ranges from a high of 1.24 V to a low of 1.17 V. Accordingly, with the use of calibration, the bandgap voltage can be adjusted to closer to 1.21 V.

In the lower graph, after calibration, the middle curve has a bandgap voltage of about 1.214 volts, and was not calibrated since it was within the tolerance range. The upper curve has a bandgap voltage of about 1.218 V at room temperature, and the lower curve has a bandgap voltage of about 1.204 V at room temperature. Each of them is about 1.21 V., namely within the accepted tolerance of 0.009 V of 1.21 V. Not only has the variance due to process of the bandgap voltage at room temperature decreased greatly after calibration, the changes in the bandgap voltages with temperature after calibration are also greatly reduced. Thus, a bandgap voltage generator 20 including the calibration transistors provides for much more accurate and stable bandgap reference voltage.

FIG. 6 is a flowchart of a process for calibrating the bandgap reference voltage generated by a bandgap voltage generator 20 according to one embodiment. At 100 a control circuit 32 measures the bandgap reference voltage generated by a bandgap voltage generator 20 at temperature. At 102, the control circuit checks to see if the bandgap reference voltage is between 1.20 and 1.22 V. If so, then calibration is complete and calibration is exited. If the bandgap reference voltage is not within the desired range, at 104 the control circuit 32 determines if the bandgap voltage is lower than 1.20 V. If the bandgap voltage is lower than 1.20 V the calibration code is that you are of the transistors. At 106 the control circuit checks whether the bandgap reference voltage is greater than 1.20 V.
If yes, then the calibration code is incremented and calibration returns to step 100. The calibration process continues incrementing or decrementing until the bandgap reference voltage falls within the desired range. Since the band gap voltage has been adjusted at room temperature, the entire curve has moved, as shown in FIG. 5 and will likely stay at about 1.21 V for all operating temperatures.

[0045] Of course, with this invention, the bandgap voltage can be tuned to as many decimal points as desired, such as to within four or five decimal points.

[0046] In one alternative embodiment, it is also possible to calibrate the bandgap voltage for operation at a different temperature besides room temperature. According to this alternative embodiment, when the device is under test, the die is heated to an expected long-term operating temperature. This heating can take place by leaving the die on for a period of time so the die naturally reaches its operating temperature. Alternatively, the die can be heated with a heater near the test socket as part of the burn-in calibration test. Once the die has reached the expected operating temperature, which normally would be in the range of about 105°C to 110°C, the calibration sequence of FIG. 6 is repeated. Specifically, the bandgap voltage calibration steps, as set forth herein, and explained in FIG. 6, are carried out once again with the die at the full operating temperature. A new calibration factor is determined by the repeated tests as set forth in the flowchart of FIG. 6, this time at a full operating temperature. The correct number of calibration transistors needed to be switched into or out of the circuit is determined, and this is stored as calibration data in the memory 34 as shown in FIG. 3. Further, the indication is also stored that this is the correct calibration data when the circuit is at a full operating temperature.

[0047] The die is thereafter put into the commercial market and sold. Over the lifetime of the die, which may be several years, when the die is first placed in operation, the calibration data for room temperature operation is downloaded and used when the die is first turned on. The die has been properly calibrated to the desired bandgap voltage. After some period of time, the calibration data will be changed and the new data will be retrieved from the memory 34 representing the calibration data to be used when the die is at full operating temperature, for example 105°C. The time for changing the calibration data from room temperature operation to high temperature operation can be determined by any number of acceptable techniques. A first acceptable technique is merely on a timing basis. Namely, the expected time for the die to reach full operating temperature, which will often be in the range of half an hour, is determined. In some circuits it may be shorter or longer. Assume, in this example, that the time to reach the full operating temperature is expected to be about 30 minutes. Accordingly, in this example, after the die has been in operation for 30 minutes, as determined by clocks located in the control circuit 32, the calibration data for the high temperature operation will automatically be downloaded according to the software instructions stored in the memory 34 as guided by the control circuit 32. Thereafter, the high temperature calibration data will be loaded into the programmable transistors 25 and the die will then operate at the preferred bandgap voltage at the high temperature and will remain with this calibration data loaded until the die is turned off, after which time the process will repeat. Alternatively, a temperature sensor may be positioned adjacent to the die 30 which can sense the temperature and can download the proper calibration data based on the actual temperature as sensed.

However, in most situations a temperature sensor will not be needed; it will be sufficient to download the new calibration data based on the time the die has been in operation, since this is generally a reliable indication of the expected temperature of the die.

[0048] While this alternative embodiment is not always used, if extremely fine tuning to an exact bandgap voltage over all operating temperatures is desired, it can be provided.

[0049] While various ranges, circuit designs, and configurations that the described those of skill the art will understand in light of the present disclosure that many other ranges, configurations, and circuit designs can be implemented in accordance with principles of the present disclosure. All such other ranges configurations and circuit designs fall within the scope of the present disclosure.

[0050] The various embodiments described above can be combined to provide further embodiments. All of the U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet are incorporated herein by reference, in their entirety. Aspects of the embodiments can be modified, if necessary to employ concepts of the various patents, applications and publications to provide yet further embodiments.

[0051] These and other changes can be made to the embodiments in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific embodiments disclosed in the specification and the claims, but should be construed to include all possible embodiments along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

1. A bandgap voltage generator, comprising:
   a. an output configured to output a bandgap reference voltage;
   b. a plurality of calibration transistors;
   c. a calibration input configured to receive a calibration signal enabling one or more of the calibration transistors; and
   d. a resistor electrically coupled between the output and the plurality of calibration transistors.

2. The bandgap voltage generator of claim 1, comprising a first transistor having a drain terminal coupled to the output.

3. The bandgap voltage generator of claim 2 wherein a current passes from the first transistor through the one or more calibration transistors that have been enabled by the calibration signal.

4. The bandgap voltage generator of claim 3 wherein the current does not pass through the calibration transistors that have not been enabled by the calibration signal.

5. The bandgap voltage generator of claim 4, comprising an amplifier having:
   a. a first input;
   b. a second input; and
   c. an amplifier output coupled to a gate terminal of the first transistor.

6. The bandgap voltage generator of claim 5, comprising a second transistor having a collector terminal coupled to the first input of the amplifier.

7. The bandgap voltage generator of claim 6, comprising:
   a. a third transistor; and
   b. a second resistor electrically coupled between a collector terminal of the third transistor and the second input of the amplifier.
8. The bandgap voltage generator of claim 7, comprising:
a fourth transistor having a collector terminal coupled to the first resistor; and
a third resistor coupled between the collector terminal of the second transistor and the collector terminal of the fourth transistor.
9. The bandgap voltage generator of claim 8, comprising:
a fifth transistor having a gate terminal coupled to the amplifier output;
a fourth resistor electrically coupled between a drain terminal of the fifth transistor and the first input of the amplifier;
a sixth transistor coupled having a gate terminal coupled to the amplifier output; and
a fifth resistor coupled between a drain terminal of the sixth transistor and the second input of the amplifier.
10. The bandgap voltage generator of claim 9 wherein first, fifth, and sixth transistors include respective drain terminals coupled to a first supply voltage.
11. The bandgap voltage generator of claim 10 wherein the second, third, and fourth transistors have respective gate and emitter terminals each connected to a second supply voltage.
12. A method, comprising:
generating a bandgap reference voltage at an output of a bandgap voltage generator;
making a first measurement of the bandgap reference voltage;
generating a first calibration signal based on the first measurement; and
enabling a first set of calibration transistors of the bandgap voltage generator by supplying the first calibration signal to the bandgap voltage generator.
13. The method of claim 12, comprising:
after supplying the first calibration signal to the bandgap voltage generator, making a second measurement of the bandgap reference voltage;
generating a second calibration signal based on the second measurement; and
enabling a second set of calibration transistors by supplying the second calibration signal to the bandgap voltage generator.
14. The method of claim 12, comprising:
after supplying the first calibration signal to the bandgap voltage generator, making a second measurement of the bandgap reference voltage; and
ending a calibration operation if the bandgap reference voltage is within a selected range.
15. The method of claim 12, comprising passing a current from a first transistor to the first set of calibration transistors upon enabling the first set of calibration transistors, a drain terminal of the first transistor being coupled to the output of the bandgap voltage generator.
16. The method of claim 13, comprising:
passing a second current from a second transistor to a third transistor;
amplifying a signal from the second transistor; and
passing the amplified signal to a gate terminal of the first transistor.
17. A device, comprising:
a bandgap voltage generator including:
an output;
a first transistor coupled to the output;
a resistor coupled to the output;
a plurality of calibration transistors coupled to the first resistor.