

[54] **NUMBER COMPARING SYSTEM**
 [72] Inventors: **Robert W. Steiger, Munster; Ralph E. Skoog, Highland, both of Ind.**
 [73] Assignee: **Delcon Corporation, Hammond, Ind.**
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Primary Examiner—Eugene G. Botz
Assistant Examiner—James F. Gottman
Attorney—Olson, Trexler, Wolters & Bushnell

[52] **U.S. Cl.**.....**340/146.2, 235/177, 340/149 R, 340/149 A, 235/61.7 B**
 [51] **Int. Cl.**.....**G06f 7/02, G06f 15/30**
 [58] **Field of Search****340/146.2, 149 R, 149 A; 235/177, 61.7 B; 179/2 CA**

[57] **ABSTRACT**

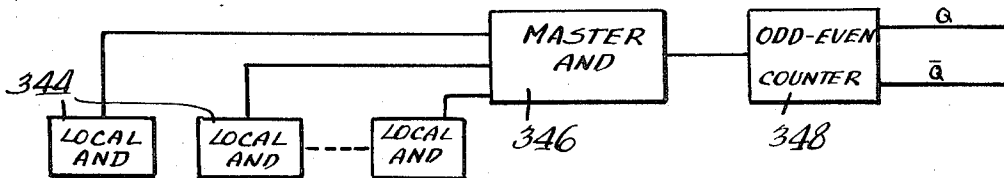
A number comparing system usable in checking credit cards, inventory control, and many other areas. An input device is provided for setting a number to be verified, this number may be read electronically from a credit card or ticket, or it may be set manually by means of knobs and dials, etc. A high speed tape unit, which may use punched paper tape or magnetic tape, acts as a memory and readout unit. A logic system compares the number to be verified with numbers read from the memory. The logic system actuates an indicator or alarm to confirm verification, or to attract attention, as to a stolen credit card.

6 Claims, 18 Drawing Figures

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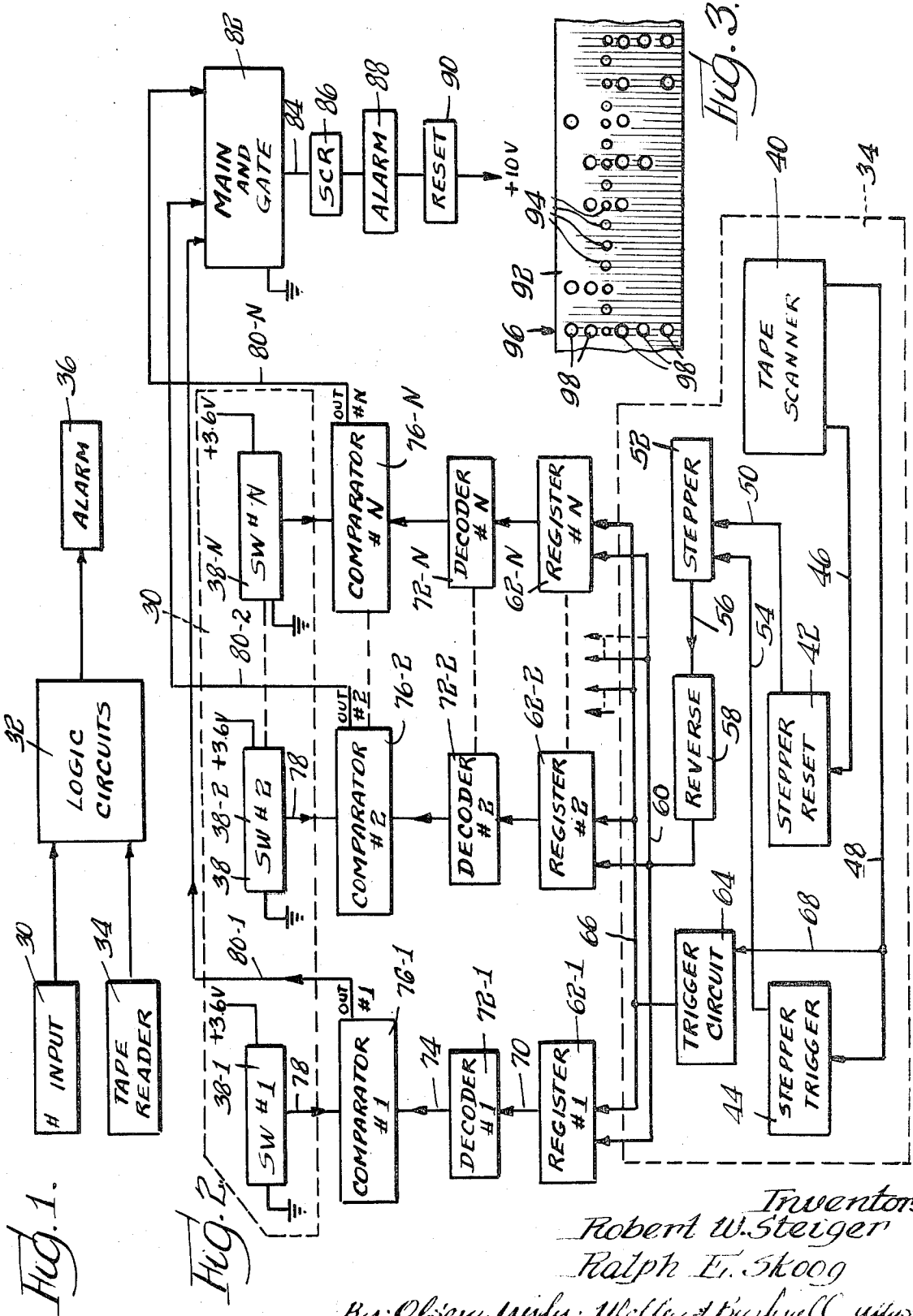


FIG. 1.

FIG. 2.

FIG. 3.

Inventors
Robert W. Steiger
Ralph E. Skoog

By Olson, Miller, Weller & Bushnell attys.

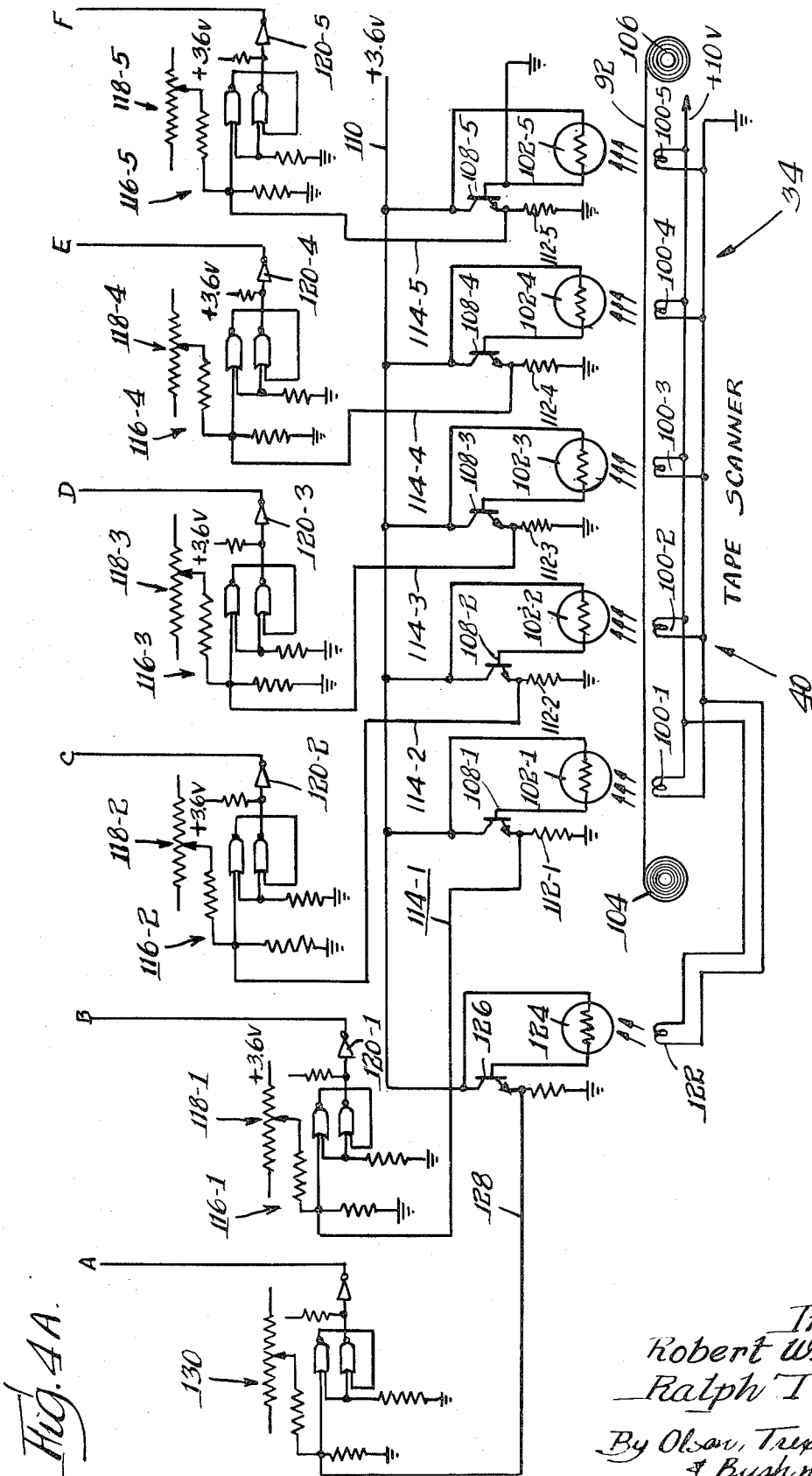
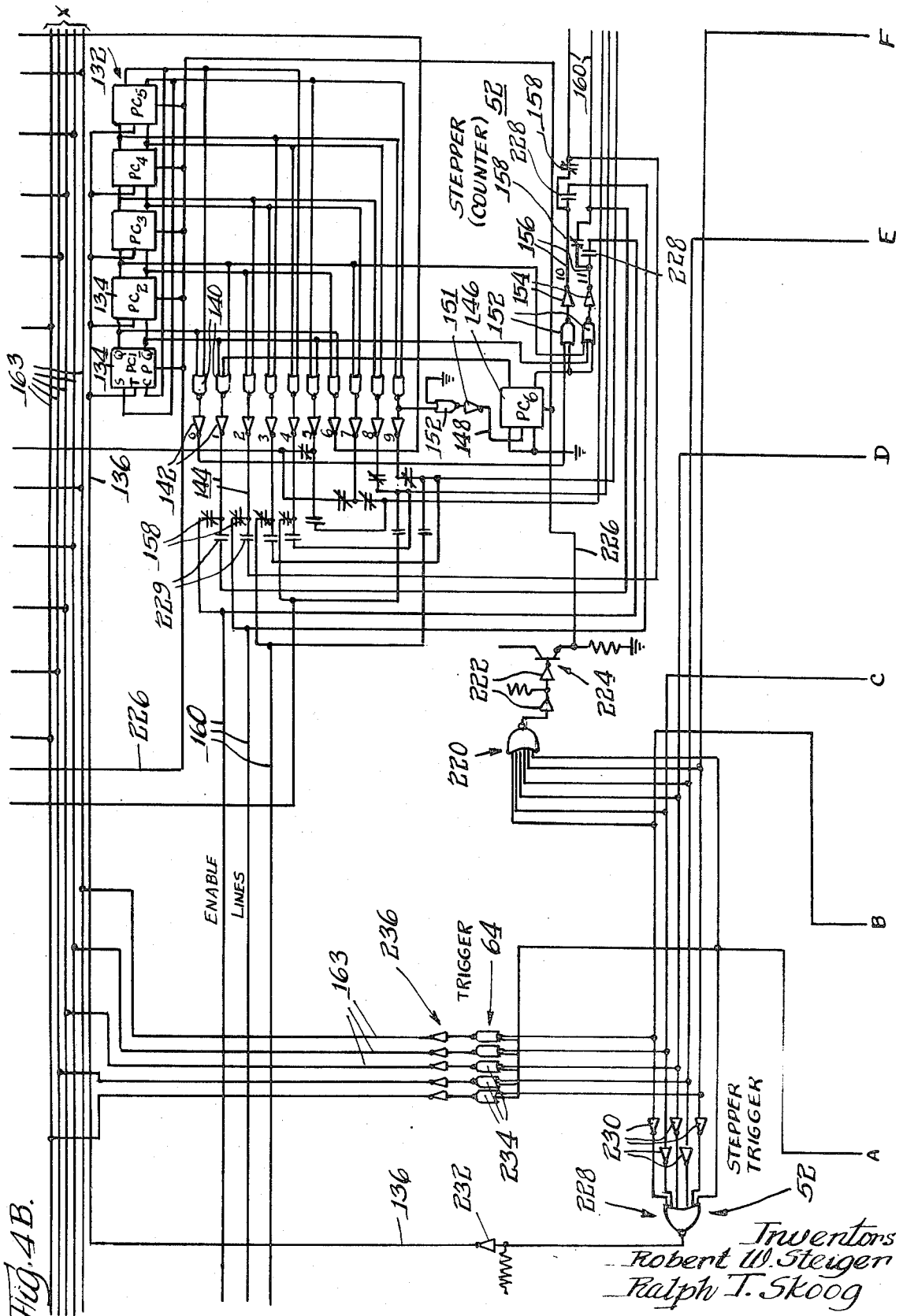


Fig. 4A.

Inventors
Robert W. Steigen
Ralph T. Skoog
By Olson, Trepier, Wolter
& Bushnell attys



By Olson, Tremler, Walters & Bushnell attys

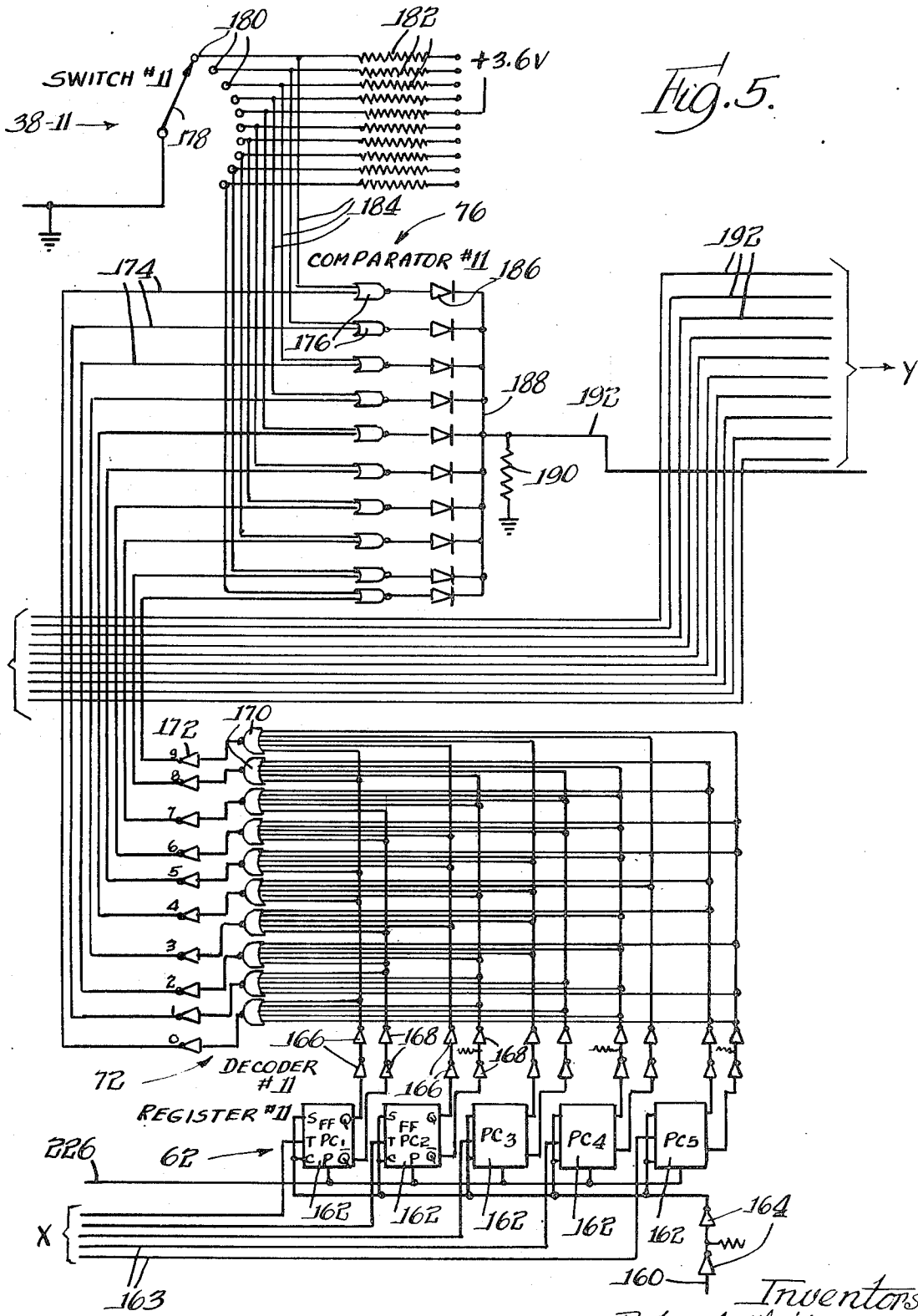
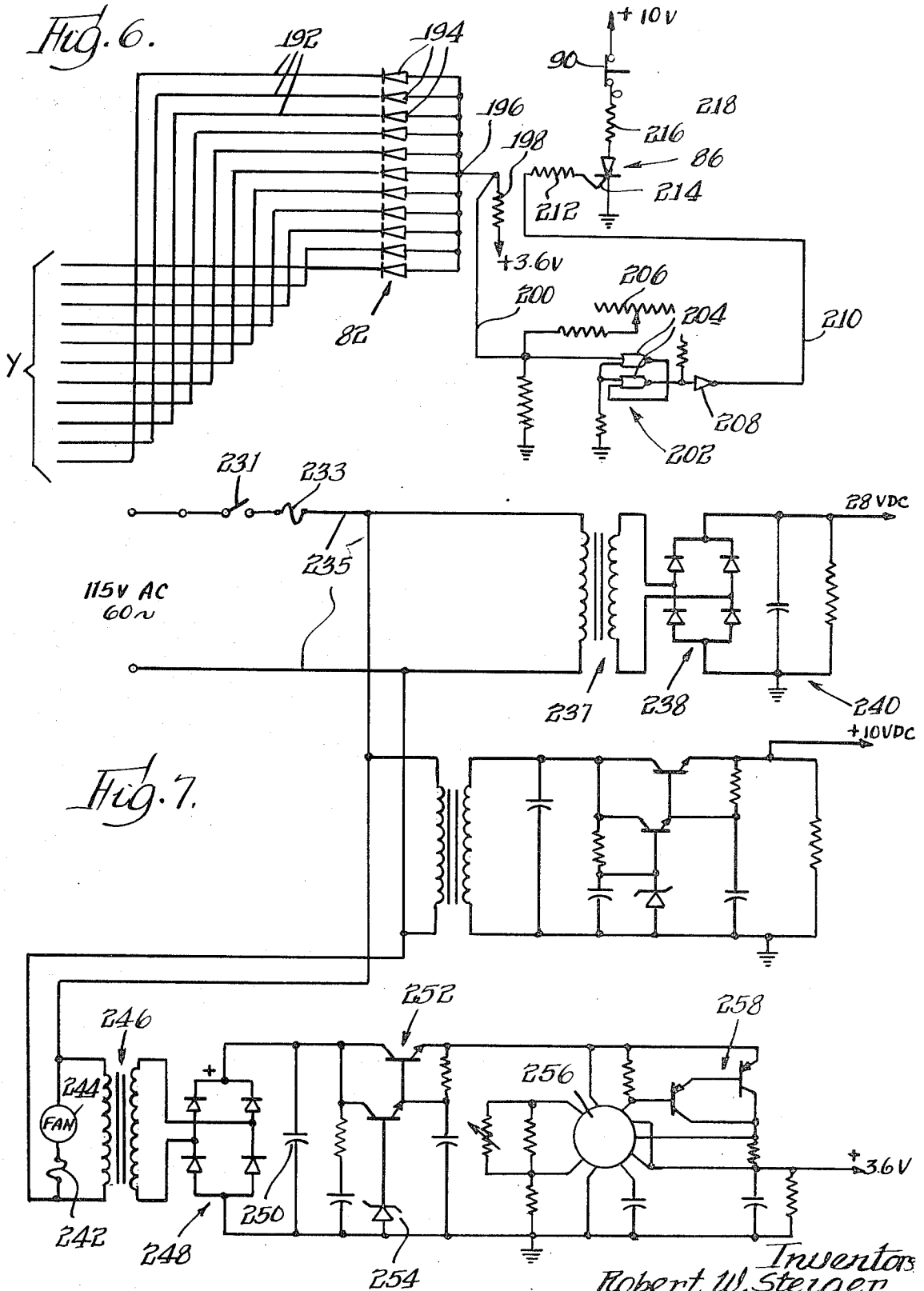
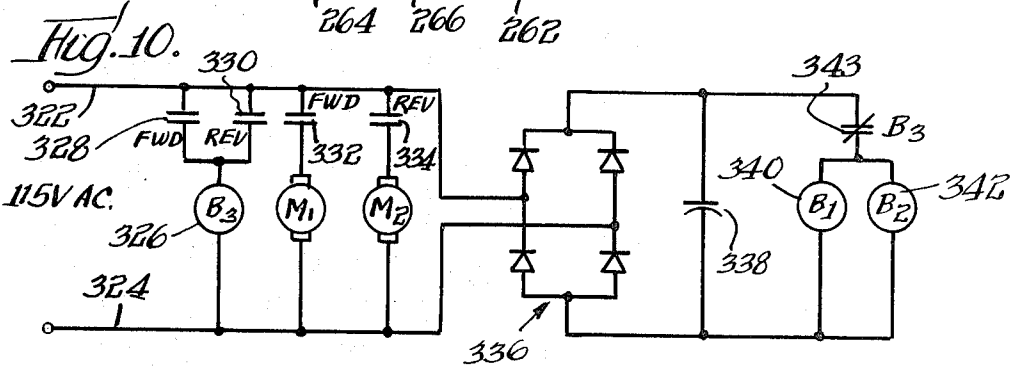
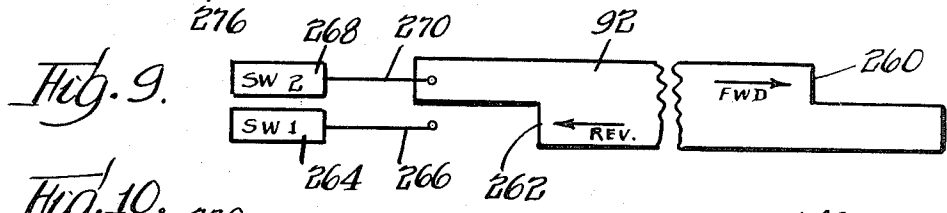
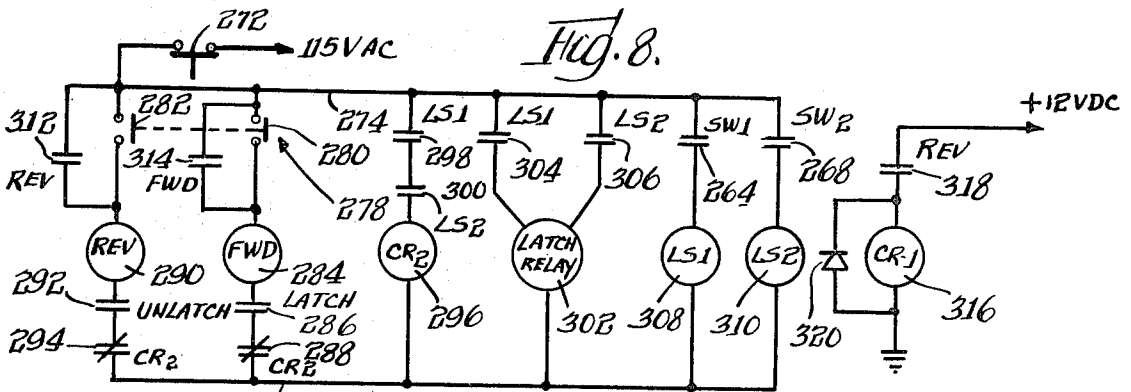


Fig. 5.

Inventors
Robert W. Steiger
Ralph E. Skoog
By: Olson, Trexler, Woltus & Bushnell attys.



Inventors
Robert W. Steiger
Ralph I. Skoog
By: Olson, Tremler, Wolter & Bushnell attys.





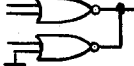



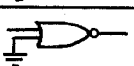

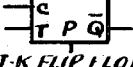
DEVICE	EQUIVALENT	DEVICE TYPE & No. USED
 2 INPUT NOR. GATE	NONE	1/2 UL 914
 3 INPUT NOR GATE		1 UL 914
 5 INPUT NOR GATE		2 UL 914
 INVERTER		1/2 UL 914
 INVER. BUFFER	NONE	1 UL 900
 J-K FLIP FLOP	NONE	1 UL 923

Fig. 11

Inventors
 Robert W. Steiger
 Ralph T. Skoog
 By: Olson, Taylor, Walton
 & Bushnell

FIG. 12.

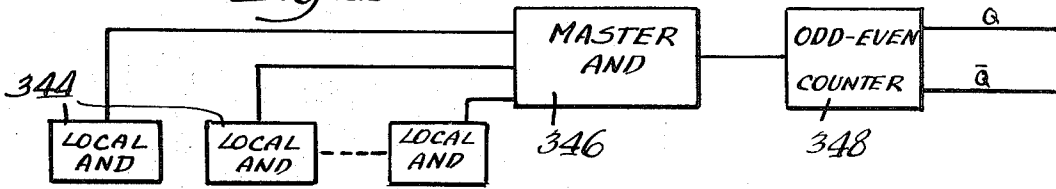
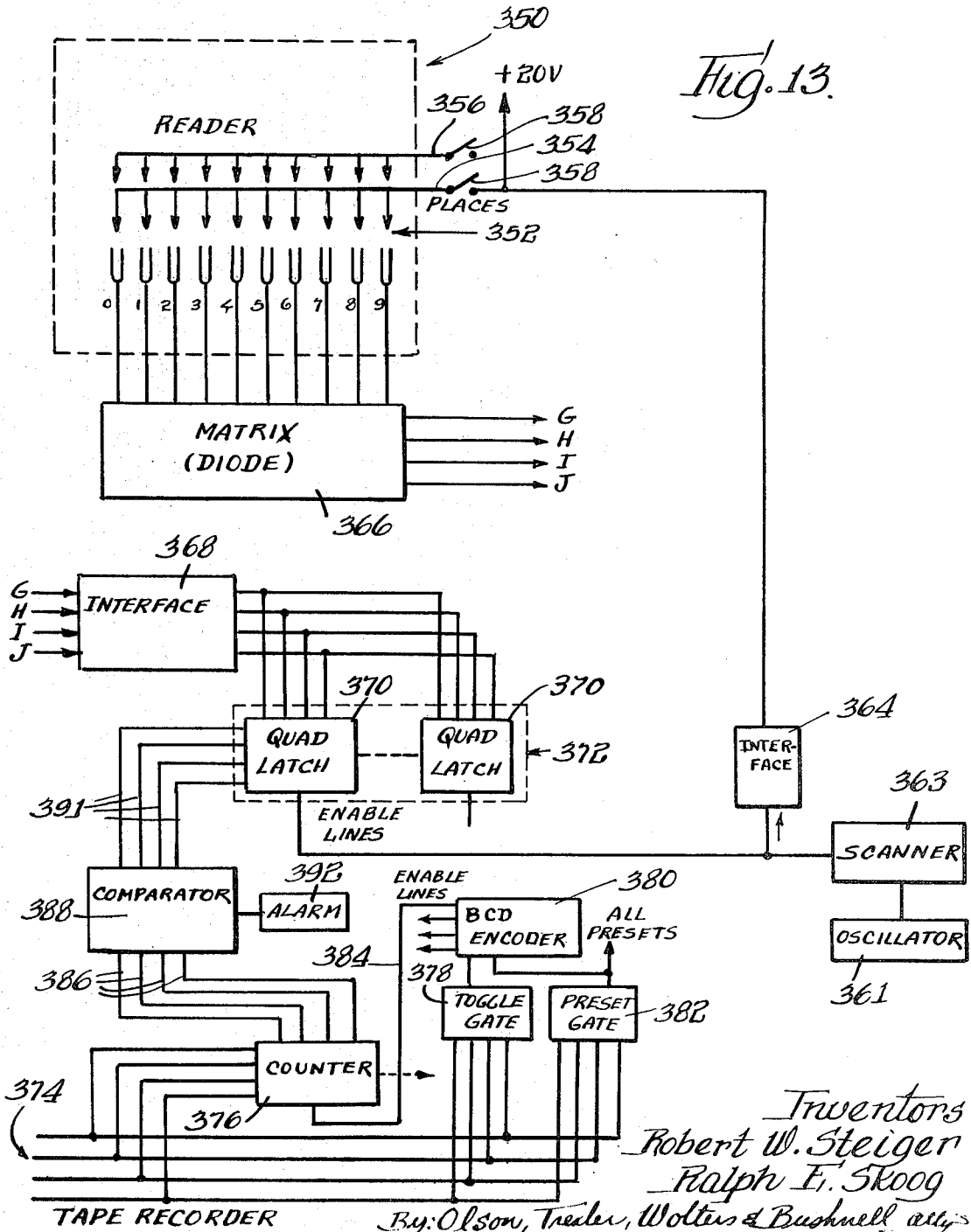
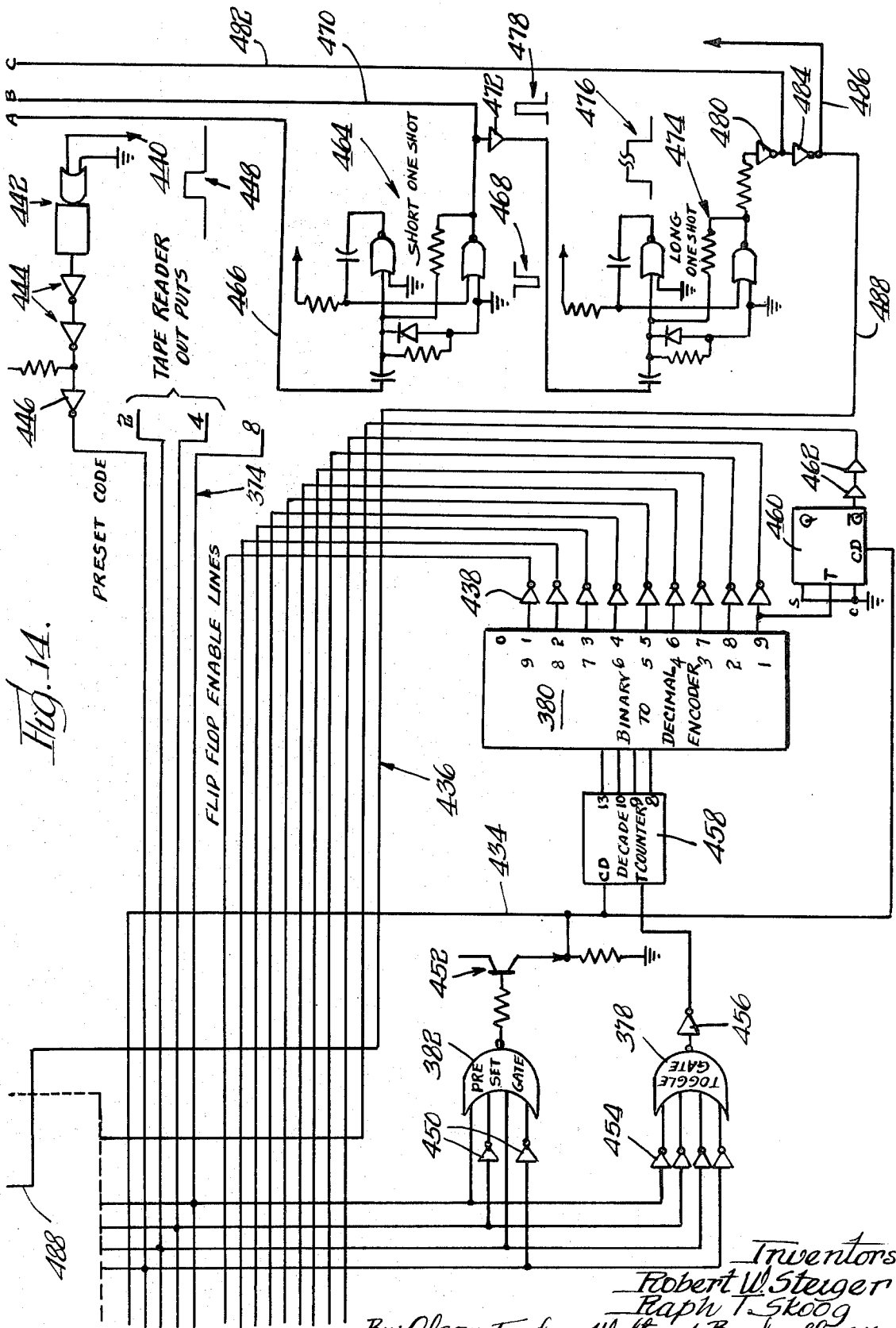


FIG. 13.



Inventors
Robert W. Steiger
Ralph E. Skoog

By: Olson, Treiber, Wolters & Bushnell attys.



Inventors
 Robert W. Steiger
 Ralph T. Skoog
 By: Olson, Treplin, Wolter & Bushnell attys.

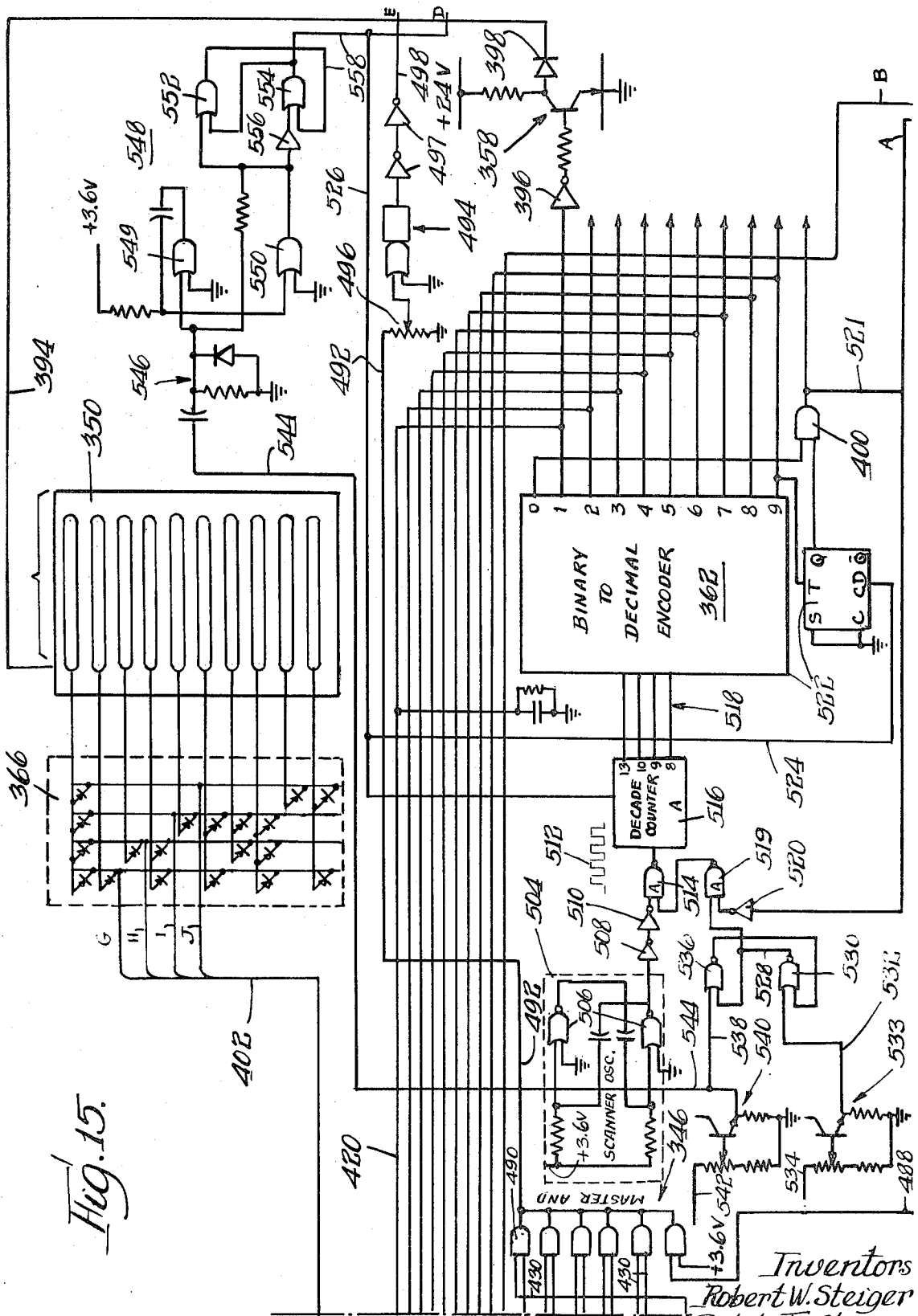
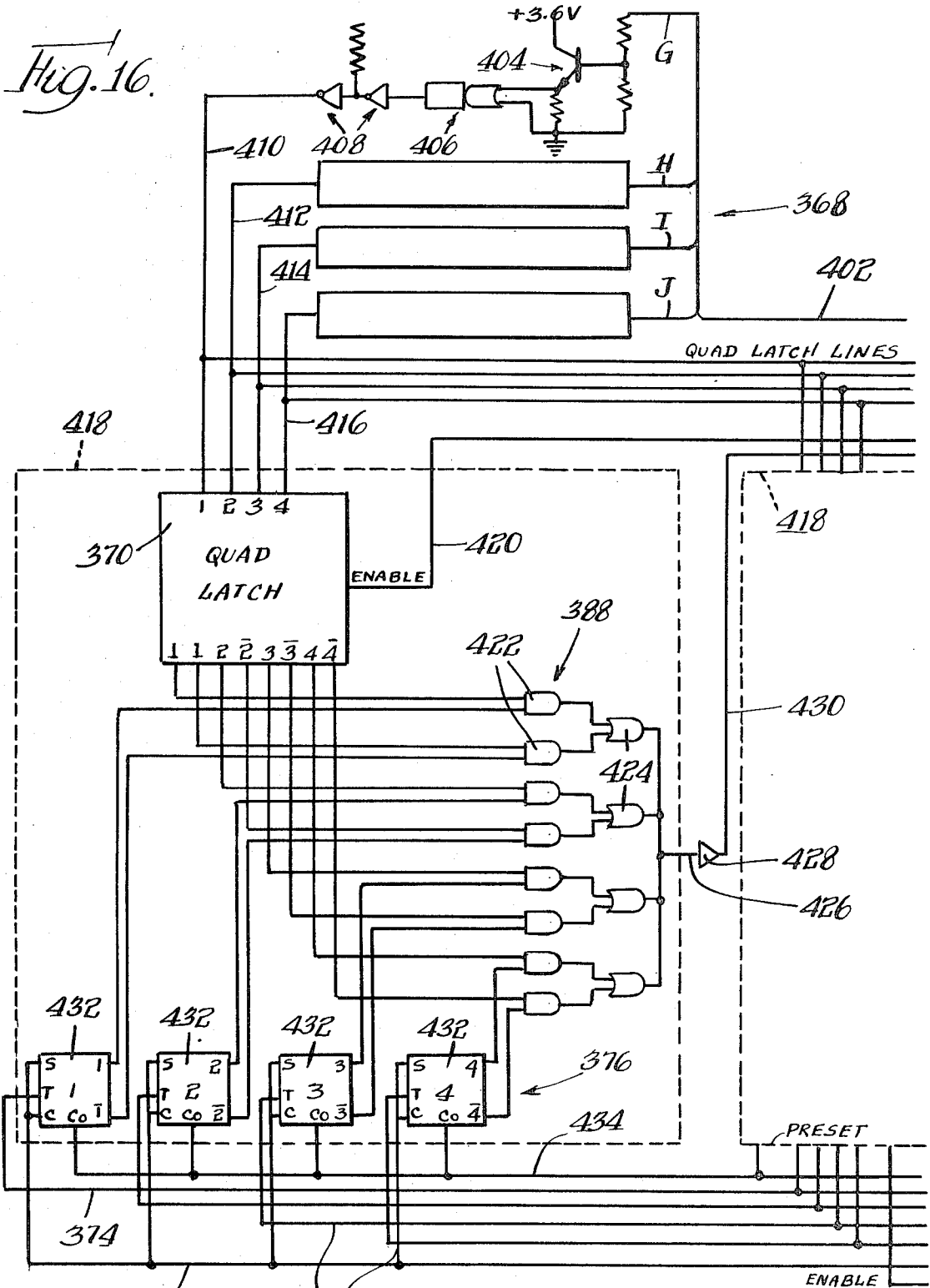
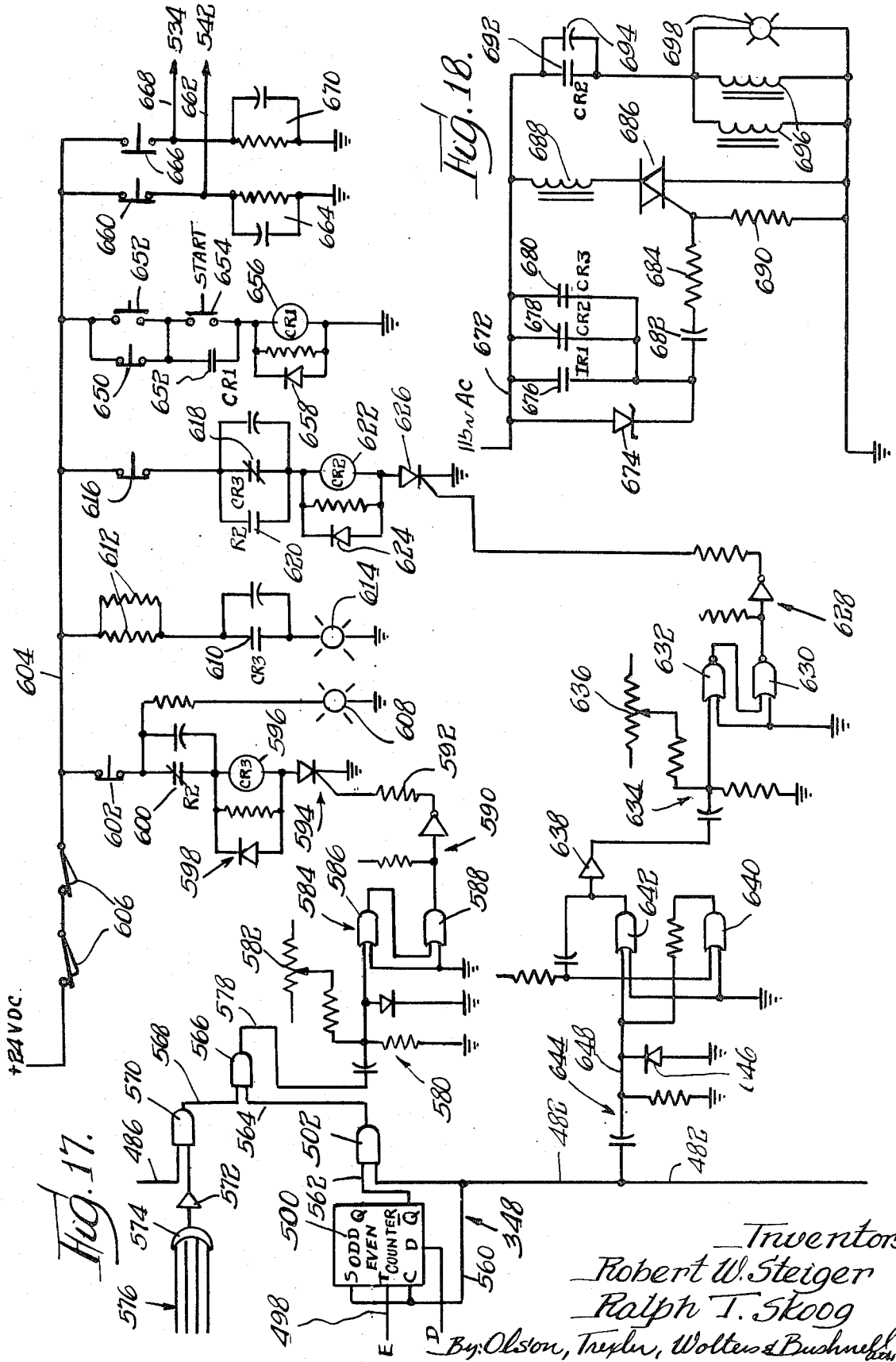


Fig. 15.

Inventors
Robert W. Steiger
Ralph T. Skoog
By: Olson, Trexler, Wolters & Bushnell attys.



Inventors
 Robert W. Steiger
 Ralph T. Skoog
 By: Olson, Tredin, Wolters & Bushnell attys.



Inventors
Robert W. Steiger
Ralph T. Skoog
By Olson, Trexler, Wolters & Bushnell Attorneys

NUMBER COMPARING SYSTEM

BACKGROUND AND OBJECTS OF THE INVENTION

Credit cards are today widely used. The general situation is that below a certain value, it is not necessary for a clerk to check with a home office before issuing credit on the card. However, above a certain value, it is necessary for a clerk to call a home office. During busy periods it may take an extensive time, perhaps as much as an hour or so, before a verification can be effected. Obviously this is an annoyance and a great waste of time both to the consumer and to the clerk, resulting in ill will and lost sales. Furthermore, it is an expensive mode of operation, requiring a large number of salaried clerks to check the numbers as they are verified into the home office or checking station.

Somewhat similar considerations pertain with regard to inventory control wherein merchandise must be moved from the stockroom to the shelves when the supplies of merchandise on the shelves become low and wherein merchandise must be moved from a warehouse to the storeroom or stockroom when supplies in the latter become low. Any system requiring human personnel to compare stocks with a catalog or list of available items in a stockroom or in a warehouse is inefficient and wasteful by present day standards. Other systems in which number comparing is necessary would occur to those skilled in the art, and it is not the purpose of the present application to detail all of them.

Accordingly, it is an object of the present invention to provide a relatively fast and efficient, yet low cost system for comparing numbers, for use in checking credit cards, inventory control, etc.

More specifically, it is an object of the present invention to provide a tape memory for reading at high speed to check or match a pre-selected set of digits with continuous reading of the tape.

In accordance with the last preceding object, it is a further object of the present invention to provide a tape memory in which the tape is in an endless loop and runs continuously, and in which the tape is automatically reversing.

In one form of the present invention, it is an object thereof to use a modified five level code somewhat similar to Teletype with the holes in the tape read by means of a semi-conductor photocell array, in combination with means for converting the five level code to decimal.

Yet another object of one form of the invention is the provision of a punched tape memory on the Teletype system, with the tape driven by rollers, and the sprocket holes used for triggering reading.

Yet another object of the present invention is the provision of a tape memory in combination with an odd-even counter, whereby it is unnecessary to locate and remove the number of a "hot" card, but wherein it is only necessary to add the number of the card a second time to cancel an indication of a "hot" card by means of an odd-even counter.

Specifically, it is an object of the present invention to provide a number comparing system reading only one number or digit at a time in sequence.

SUMMARY OF THE DISCLOSURE

An input device is provided for setting or reading a number to be verified. The number may be set manually in accordance with one form of the invention, or in another form of the invention the number may be read directly, as from a credit card. A high speed tape unit is provided, which may be a punched paper tape, a magnetic tape, an optical reading tape, etc. which acts as a memory and readout unit. A logic system compares a number to be verified with the numbers read from the memory, and operates a readout to indicate a match or a mismatch of numbers.

DESCRIPTION OF THE DRAWINGS AND DETAILED SPECIFICATION

Objects and advantages of the present invention in addition to those enumerated heretofore, as well as specific exemplifications thereof, will be understood from the following description when taken in connection with the accompanying drawings, wherein:

FIG. 1 is a block diagram illustrating the entire system in simplest form;

FIG. 2 is a more detailed block diagram illustrating the overall system;

FIG. 3 is a fragmentary view of a section of punched paper tape as used in the first embodiment of the present invention;

FIG. 4a is a detailed wiring diagram of a portion of the system;

FIG. 4b is a similar detailed wiring diagram of an adjacent portion of the system wiring and lying immediately above FIG. 4a;

FIG. 5 is another detailed wiring diagram of the portion of the system wiring lying immediately to the right and slightly above the wiring of FIG. 4b;

FIG. 6 is a further detailed wiring diagram comprising the main AND gate and lying immediately to the right of FIG. 5;

FIG. 7 is a detailed wiring diagram of the power supply forming a part of the present system;

FIG. 8 is a detailed wiring diagram of the motor control circuit forming a part of the present invention;

FIG. 9 is a somewhat schematic view illustrating the means by which the paper tape is reversed at either end of the travel;

FIG. 10 is a further wiring diagram of the motor control circuit;

FIG. 11 comprises a legend as to the symbols used in the preceding wiring diagrams;

FIGS. 12 and 13 comprise block diagrams corresponding to portions of an improved form of the invention;

FIG. 14 is a fragmentary schematic wiring diagram corresponding to FIGS. 12 and 13;

FIG. 15 is a further fragmentary schematic wiring diagram lying immediately above FIG. 14;

FIG. 16 is yet another fragmentary schematic wiring diagram lying to the left of FIGS. 14 and 15;

FIG. 17 is a further fragmentary schematic wiring diagram lying to the right of FIG. 15; and,

FIG. 18 is yet another fragmentary schematic wiring diagram.

Turning now in greater particularity to the drawings, and first to FIG. 1, a rather basic representation of the

invention will be seen. Thus, there is an input indicated at 30 related to the credit card, inventory ticket, etc. to be checked. This may be read directly from the card, etc., or it may be set manually. The input is connected to logic circuits indicated at 32. A tape reader 34 also is connected to the logic circuits to compare numbers stored in the tape reader with the number from the input 30. The output from the logic circuits is connected at 36 to an alarm or some other suitable audio or visual indication of a so-called "hot card", namely a stolen or cancelled credit card. Alternatively, it will be understood that an indication could be provided indicating favorable matching, as in a credit card system or as in an inventory control system.

Turning now to FIG. 2, the input 30 will be seen to comprise a series of switches 38, respectively identified as 38-1, 38-2, etc. In a specific example of the invention as reduced to practice there are eleven switches, but the precise number is not critical, and accordingly the last switch has been designated as switch number N. In the first example of the invention as herein shown and described, and as will be brought out in detail hereinafter, the switches are manually set. Each has a voltage input of +3.6 volts, and the output is either +3.6 volts or zero.

The tape reader 34 comprises a tape scanner 40 past which the tape is moved for scanning of the code thereon. The scanner 40 is connected to a stepper reset 42, and also to a stepper trigger 44, by separate lines 46 and 48 respectively. The stepper reset is connected by a line 50 to a stepper 52, or the stepper trigger 44 is connected by a line 54 to the stepper 52.

The stepper is connected at 56 to a reverse 58, whereby information from the tape scanner can be read with the tape moving either in a forward or in a reverse direction.

The output from the reverse 58, indicated schematically at the bus line 60, is connected to a series of registers 62, respectively indicated at 62-1, 62-2 through 62-N, the registers corresponding in position and number to the switches 38.

A trigger circuit 64 is provided which is connected by means such as a bus line 66 to each of the registers 62. The trigger circuit 64 is controlled from the tape scanner, as by a connection indicated at 68 from the line 48.

Each of the registers 62 is respectively connected at 70 to a decoder 72, the respective decoders being numbered 72-1, 72-2, 72-N. As will be discussed later, the decoders change the five level code on the tape to a decimal code. The decoders 72 in turn are respectively connected at 74 to comparators 76, respectively numbered 76-1, 76-2, 76-N. Likewise, each of the switches 38 is respectively connected at 78 to a corresponding comparator 76. Each of the comparators has an output at 80, respectively identified as 80-1, 80-2, - - - 80-N, all leading to a main AND gate 82. The main AND gate is connected at its output 84 to a silicon controlled rectifier 86 acting as a relay to connect an alarm 88, which may be audio, or visual, or both, to identify a bad credit card. As will be understood, the alarm is exemplary only, and some other control function should be effected, as in an inventory control system. Potential, indicated at +10 volts, is connected to the alarm through a manual reset 90 which allows the alarm to be shut off for another operation to begin.

The paper tape used in the present form of the invention is shown at 92 in FIG. 3, only a fraction of the tape being shown, since such tape is commonly supplied in rolls of several hundred or several thousand feet. The tape is provided with small sprocket holes 94 along a longitudinal line displaced from the center line of the tape. In normal use, the sprocket holes are used for feeding the tape by means of a toothed sprocket. However, in the present invention the sprocket holes are used for position detecting, and feeding is by means of rubber friction rollers.

Each transverse number position 96 of the tape has a possible five punched holes 98, two on one side of the sprocket hole 94, and three on the other side. Any number and combination of holes from 0 to 5 can be punched, corresponding in teletype code to a digit from 0 to 9. In accordance with the first form of the invention, the system is set up for 11 digit numbers, whereby the number N on each of the switches, etc. comprises 11. Correspondingly, 11 number spaces are necessary on the paper tape for each number, which in the credit card checking system corresponds to a "hot card".

For purposes of comparing most of the wiring at the same time, FIGS. 4a, 4b, 5 and 6, may be aligned if desired, FIG. 4b lying directly above FIG. 4a, with letter designation A through F indicating connecting lines. FIG. 5 lies to the right of FIG. 4b, but at a higher level, one bundle of wires being indicated at X on each for purposes of alignment. FIG. 6 lies immediately to the right of FIG. 5, and a corresponding bundle of wires on each figure is identified at Y.

Considering first FIG. 4a, the tape scanner 40 comprising a part of the tape reader 34 includes an array of five electric lights 100, distinguished among one another as 100-1 through 100-5. The lights are arranged transversely of, and on one side of the path of transport, of the tape 92, which winds from one reel 104, to another 106. As will be understood, whichever reel 104, 106 is serving as the take-up reel is positively driven. The tape, herein a paper tape 92, is driven by rubber drive rollers, not shown. As will be understood, the positive drive of the reel tends to take up the tape somewhat faster when it is driven by the rubber drive rollers, in order to maintain tension on the tape.

Also transversely of the path of the tape 92, and aligned with the electric lights 100 is a set of five light dependent resistors 102, respectively distinguished as 102-1 through 102-5. Each of the light dependent resistors, hereinafter referred to as an LDR, is connected to one of five similar transistor circuits including a transistor 108, the same suffixes of numerals 1 through 5 again being applied for distinction. Specifically, each LDR is connected across the base-collector of an NPN transistor, positive voltage of 3.6 volts being applied from a bus 110. The emitter of each transistor 108 is grounded through a resistor 112, and the output thereof is taken in an emitter-follower configuration from the top of the resistor-1-112-5 through a line 114 to a corresponding sequential NOR gate 116, again provided with the suffixes numerals 1 through 5 for individual distinction. Each of these NOR gate circuits is provided with a potentiometer device 118 for setting the response threshold level, and each of the NOR gate circuits has an output through a buffer inverter 120 (see FIG. 11 for a coding of symbols, although the symbols used herein are conventional) to a line, respective-

ly indicated as B, C, D, E and F. These five lines lead up to FIG. 4b, and more will be said about that shortly hereinafter upon completing description of FIG. 4a.

A sixth electric light 122 is incorporated in the transverse array with the lights 100, this one being positioned for alignment with the sprocket holes 94 of the tape 92. An LDR 124 is positioned on the opposite side of the tape for exposure to light emanating from the lamp or light 122 when the sprocket hole is in exposing position between the two. The connection of the LDR 124 is similar to that previously described, being across the base-collector of an NPN transistor 126 receiving bias from the line 110, and having an emitter-follower output at 128 leading to a NOR gate circuit 130 similar to the NOR gate circuits 116 and having an output line indicated at A.

As will be apparent from what ensues, no reading is made of the condition of the LDR's 102, until such time as the LDR 124 is conductive, i.e. exposed to the light 122. The reason for this is that it is possible that the tape might be very slightly cocked in passing the lights and LDR's, whereby not all LDR's opposite punched holes will start conducting at the same time. To prevent this contingency, a reading is made only when the LDR 124 opposite the sprocket hole is exposed to light. Since the sprocket hole is much smaller than the other holes, it is manifest that all other holes will be opposite the respective LDR's when the sprocket hole is opposite the LDR 124 whereby accurate readings are taken.

The stepper 52, of FIG. 4B, includes a ring counter 132 comprising a series of five J-K flip-flops interconnected in conventional fashion. The flip-flops, hereinafter identified by numeral 134 are toggled from a toggle line 136, about which more will be said hereinafter.

The outputs of the J-K flip-flops 134 are interconnected as will be seen in detail in FIG. 4B through a series of 10 NOR gates 140, the outputs of which are respectively connected through inverters 142 to output lines 144. This amounts to a count by 10 counter, and in the present illustrative example it is intended to count 11 digits.

Accordingly, a sixth J-K flip-flop 146 is provided which is toggled by the output line 148 of an inverter 150 from a NOR gate 152 connected between the ninth of the NOR gates 140 and its corresponding inverter. Connection is made from the J-K flip-flop 146 and the preceding flip-flops 134 to NOR gate 152 and inverters 154 to output lines 156, providing a count up to 12. The first position is considered to be a zero or rest position, whereby provision is made for counting 11 digits.

Each of the output lines 144 and 156 is connected through corresponding normally closed relay contacts 158 to a series of 11 enable lines 160 corresponding to the bus line schematically shown at 60 in FIG. 2, and leading individually to the respective registers 1 through 11.

The registers 62 are not all shown in detail, since they are identical. However, in FIG. 5 register number 11 is shown in detail, and includes a series of J-K flip-flops having the 11 enable line 160 connected through a pair of inverters 164 to the S and C-inputs of all five flip-flops 162. Respective toggle input lines 163 are connected to the T-inputs of the five flip-flops 162, the

five lines together being indicated at X for correlation of FIGS. 4b and 5.

As is known, each of the flip-flops 162 initially has a Q-output. When there is a coincidence of signals on the enable line 160, and a respective input line 163, then that particular flip-flop is operated to produce a Q-output. The outputs are connected as shown in FIG. 5 through pairs of Q-inverters 166 and Q-bar-inverters 168 of 10 NOR gates 170 constituting decoder number 11 of the decoders 72 shown in FIG. 2. The outputs of the respective NOR gates 170 are taken through 10 inverters 172, the respective output lines 174 leading to a series of 10 NOR gates 176 constituting comparator number 11 of the comparators 76.

Switch number 11 of the switches 38 is shown in FIG. 5, and comprises a grounded movable switch arm 178 engageable with any one of 11 fixed contacts 180. The fixed contacts are connected through respective resistors 182 to a positive voltage supply line, specifically +3.6 volts. Additionally, each of the contacts 180 is connected through a respective wire or lead 184, each of which leads to one of the NOR gates 176. Only one of the NOR gates 176 will have a 0 applied to it due to the position of the switch arm 178, and if a 0 is supplied to that same NOR gate through one of the lines 174, then there would be a coincidence of input, and there will be an output from the respective nor gate to a diode 186 of a series of 10 thereof, having a common cathode connection 188 leading to a shunting resistor 190 and to an output line 192. Thus, there will be an output only if the 11th digit of the credit card or the like as set on the switch 38-11 coincides with the 11th digit of a number read from the tape.

There are 11 output lines 192, one from each comparator, and these are indicated all at Y to indicate correlation of FIG. 5 to FIG. 6.

The lines 192 are connected as input lines to the main AND gate 82, which comprises a plurality of diodes 194, the input lines 192 being connected to the cathodes thereof, and there being a common anode connection at 196. If all 11 digits of the credit card, or the like, as set up on the respective switches 38 and as read from the tape coincide, then there will be outputs on all of the lines 192, and there thus will be an output at 196.

The common anode connection 196 is connected through a resistor 198 to a source of positive potential of +3.6. The common connection 196 is also connected by a line 200 to a Schmitt trigger circuit 202 having a pair of NOR gates 204 and a potentiometer adjustment 206 to adjust the threshold voltage. The output of the Schmitt trigger circuit is connected through an inverter 208 to a line 210 leading to a resistor 212 to the control element 214 of the SCR 86. The output of the SCR leads through a resistor 216 to a lamp filament 218 comprising the alarm 88, and leading to a manual reset 90, in turn leading to the positive 10 volts as previously indicated in connection with FIG. 2. Thus, the coincidence of the input 192 is indicated at the output 196, the SCR 86 is rendered conductive, and the lamp filament 218 lights. The lamp filament comprises all or part of the alarm, and remains on until such time as the manually operated reset 90 is manually operated to break the connection.

Returning now to FIG. 4b, the various lines A to S are connected to a pre-set NOR gate 220 having an output connected through a pair of inverters 222 to a transistor 224 connected as an emitter-follower, and having a pre-set line 226 leading to the P-input of all of the J-K flip-flops 134 and 146. The pre-set line 226 also is connected to the P-inputs of the J-K flip-flops 162 of all of the registers 62. The tape 92 is coded so that there will be five punched holes 98 across each time it is desired to re-set, i.e. following each 11 digits. At this time, all of the LDR's 102 will be exposed to light, as will be the LDR 124 of the strobe. The output of the pre-set NOR gate 220 normally is at 0, but goes to 1 when all of the lights are on.

All of the lines A through F are connected to a toggle NOR gate 228 comprising a part of the stepper 52. The line A is connected direct to one of the inputs of the NOR gate 228, while the lines B through F are connected through respective inverters 230. When there are no holes punched in the tape, then the LDR's 102 are dark, and cause the respective Schmitt trigger circuits 116 and corresponding inverters 120 to supply 1's to the inverters 230, and to supply 0's from the inverters to the inputs to the NOR gate 228. When the condition of no punched holes pertains, and a sprocket hole is encountered, then the LDR 124 is exposed to light and causes its Schmitt trigger circuit 130 to supply a 0 which is applied direct to the input of the NOR gate 228 through the line A. At this time, there is a coincidence of input to the NOR gates 228, and the output thereof goes from 0 to 1, being applied to an inverter 232 which supplies a signal falling from 1 to 0 to the toggle line 136, thereby causing all of the previously mentioned J-K flip-flops to toggle.

The trigger circuits comprise five NOR gates 234. The line A is connected to the input of each of these NOR gates, and the lines B through F are respectively connected to the other input of every five NOR gates. This circuit is provided to ensure proper reading as heretofore noted. Should the tape be cocked slightly in the reading gate, it is certain that each of the larger punched holes will be between the respective lights and LDR's when the sprocket hole passes between its light and LDR. Thus each NOR gate 234 provides an output to a respective inverter 236 only when the LDR 124 is exposed to light through the sprocket hole. The inverters 236 are respectively connected to the input lines 163. It will be appreciated that there are five input lines 163 respectively corresponding to the five possible positions of punched holes on the Teletype coded paper tape. Thus, it is possible for one of the J-K flip-flops 162 to register a number only when the corresponding enable line is enabled, regardless of the input of a signal on the respective line 160. As will be understood, there are five J-K flip-flops 162, each of the lines 163 leading to a corresponding J-K flip-flop in all 11 registers. Since there are five digit inputs to the J-K flip-flops 162 from the Teletype code on the tape, and there are 10 outputs from the decoder 72, it will be recognized that there is herein provided a Teletype-to-decimal converter.

Due to the action of the stepper or counter 52, the digits read from the tape are successively applied to the registers 62-1 through 62-11, and lead through the decoders 72 to the comparators 76. Hence, the 11

digits for each number coded on the tape, are respectively compared with the 11 digits set on the switches 38 corresponding to a credit card or the like. As will be understood, it would be possible to read direct from the credit card or the like and to apply a signal therefrom without the necessity of the switches 38. However, the system using the manually set switches 38 is cheaper, even though somewhat slower.

When the paper tape comes to an end, it is reversed by means hereinafter to be set forth. At the same time, all of the normally closed relay contacts 158 are open. Concurrently therewith, normally open relay contacts 229 connecting the inverters 142 and 154 to the output or enable lines 160 in inverse order are closed. The tape then is run backwards, and the enable lines 160 are enabled in reverse order, whereby the digits on the tape are read reversely for comparison with the digits set on the switches 38.

A power supply for this system is shown in FIG. 7. AC input at 60-cycles is provided through a switch 231 and a fuse 233 to lines 235 leading to the input winding of a transformer 237. The output winding of the transformer 237 is connected to a bridge-rectifier 238 and a filter 240 to provide 28 volts DC output for read-out lamps.

The lines 235 also are connected through a fuse 242 to a fan 244 for cooling the rectifier and the entire system. The lines 235 are also connected to the input winding of a transformer 246, the output winding of which is connected to a bridge-rectifier 248. A smoothing capacitor 250 is connected across the output, and two transistors are connected in a regulating circuit 252 in combination with a zener diode 254. From this point circuit connections are made to a Fairchild or other satisfactory packaged regulator 256, and this in turn controls a Darlington circuit 258 to provide a highly regulated +3.6 volts DC output. The highly regulated output is necessary to preclude spurious responses.

As will be seen in FIG. 9, the tape 92 is provided with notches 260 and 262 at its opposite ends. A first switch 264 has a follower 266 which rides on the tape to keep it closed, but which falls off the tape when it reaches the end of the tape with the tape travelling in the forward direction. A second switch 268 has a follower 270 which rides on the tape, but which falls off into the notch 260 when the tape reaches the end of its reverse motion. The same results have been attained with a special code at each end of the tape.

Turning now to FIG. 8, 115 volts AC is connected through a stop switch 272 to a line 274. An opposite line 276 is returned to the other side of the 115 volt power supply.

A start switch 278 has two ganged contacts 280 and 282. The contact 282 provides a circuit connection to a forward relay 284 leading through normally open latch relay contact 286 and normally closed relay contacts 288 comprising control relay contacts to the line 276.

Similarly, the contact 282 provides for completing a circuit to a reverse relay 290 which leads through unlatched relay contacts 292 which are normally open, and normally closed contacts 294 of a second control relay.

Connections made to the second control relay 296 between the lines 274 and 276 through normally open

limit switch-1 contacts 298, and normally open limit switch-2 contacts 300.

A mechanical latch relay 302 also is connected across the lines through LS-1 contacts 304 and LS-2 contacts 306.

LS-1 relay 308 is connected across the lines 274 and 276 by switch-1 contacts 264, while limit switch-2 relay 310 is connected across the lines through switch-2 contacts 268.

Normally open reverse relay contacts 312 shunt start-switch connection 282, while forward relay contacts 314 shunt switch-connection 280.

Control relay-1, identified by a numeral 316 controls the reversal of the logic relay contacts 158 and 229, and is connected to +12 volts DC through reverse relay contacts 318. A diode 320 shunts control relay 316.

Turning now to FIG. 10, the 115 volts AC again is connected across lines 322 and 324. Brake relay-3, identified by numeral 326 is connected across these two lines alternatively through forward-relay contacts 328 and reverse-relay contacts 330. Motor No. 1 for driving the tape in a forward connection is connected across the line through forward-relay contacts 332, while motor No. 2 for driving the tape in a reverse direction is connected across the lines through reverse-relay contacts 334.

The lines 322 and 324 are connected to a bridge-rectifier 336, the DC output of which is connected across a filter capacitor 338 to supply power to the brake relays, B1 identified by numeral 340, and B2 identified by numeral 342, through contacts 343 of brake-relay 3, namely 326.

The showing in FIG. 9, is somewhat schematic. The switches 264 and 268 can be controlled mechanically in the manner shown, or preferably are controlled by a code on the tape to close the respective switches 264 or 268. If we assume that the tape is initially in the position shown in FIG. 9, with switch-2 closed, and with start-switch 278 manually depressed, both contacts 280 and 282 will close, tending to energize both relays 284 and 290. However, the circuit is not complete through both relay switches 286 and 292. Under the conditions assumed, switch-2 is closed, due to its follower 270 being held up by the tape. This causes contact 229 to be closed, whereby relay 310 is energized, closing the latch relay 302 in latching position through latch switch-2 contacts 306. Thus, the latch relay contacts 286 are closed, completing the circuits through the forward-relay 284. This closes contacts 314 so that when the switch 278 is manually released, the forward-relay 284 remains energized. With the forward-relay energized, the contacts 328 in FIG. 10 are closed, thus energizing relay 326, and opening contacts 344 to release brakes from both motors. Simultaneously, forward-relay contacts 332 are closed, to run forward motor-1, thus transporting the tape. When the tape reaches the end, switch-2 opens, and the circuit drops out. When the start switch is again pushed, operation is similar, but this time it is switch-1 contacts 264 that are closed, and relay LS-1, namely 308, is operated, to close contacts 304, and thus to place the latch relay 302 in unlatched position, energizing contacts 292. Again, the brake relay-3 is operated to release the brakes, and the reverse contacts 334 are closed thereby reverse motor-2 is energized to drive the tape in a reverse direction.

Simultaneously, when the reverse relay 290 is operated, reverse relay contacts 318 at the right end of FIG. 8 are closed whereby to energize relay CR-1, and thereby to reverse the logic relay-contacts. When the tape reaches its limit in the reverse direction, switch SW-1 opens and the circuit drops out. The brakes are applied at either end of the run.

The second form of the invention as shown in FIGS. 12-18, utilizes numbers stored on a magnetic tape in a modified binary code, rather than punched paper tape in teletype code. Furthermore, the credit card is read direct without the necessity of having switches set by a clerk or other operator. Since the numbers are read direct from a credit card, it is necessary to store these numbers for comparison. Each digit is stored in a quad-latch, the plurality of quad-latches comprising a storage register. In the present embodiment of the invention, and in accordance with the particular credit card and reader used, the numbers are ten digit numbers, and hence, there are ten quad-latches in the quad-latch storage register.

With reference to FIG. 12, the digit in each quad-latch is compared with a digit read from the tape recorder in local AND circuit 344, there being 10 such local AND circuits. All of the local AND circuits are connected to a master AND circuit 346, so that if all of the digits properly compare, then the master AND circuit has an output to an odd-even counter 348, having a Q-output and a \bar{Q} -output. With this set-up, if a number has been placed the tape as a hot card, it is not necessary to find and remove this number if the card subsequently has become a good card, as through return to the original owner, the number is simply placed on the tape a second time. If the same number is read twice, then the odd-even counter is back to the same condition as when it started, and the alarm is not actuated. On the other hand, if the number has been read only once, then the odd-even counter is at an odd state and the \bar{Q} -output causes the alarm to be operated.

Turning now to FIG. 13, the reader mechanism is shown generally at 350. The reader mechanism is manufactured by A.M.P. Inc. of Harrisburg, Penna., as a commercial device, and a complete description therefore is not required. The credit card has 10 places across the narrow dimension of the card, and 10 number positions along the longer dimension of the card opposite the various places. The 10 possible number connections are shown at 352 across the card reading mechanism 350, while two of the places are shown at 354 and 356. Transistor switches 358 are represented schematically for sequentially reading the successive places.

An oscillator 361 controls a 10 digit scanner 363 having 10 output lines (only one of which is shown) connected to respective interfaces 364, sequentially to close the 10 switches 358 to read the various places in succession.

The 10 place or decimal output of the card reader 350 is connected to a diode matrix 366, having four output lines indicated at: G, H, I and J. These lines are connected through an interface 368 to a series of 10 quad-latches 370 forming a quad-latch storage register 372 for storing in binary form the 10 digits of the number read from the credit card. The enable lines from the scanner 363 are respectively connected to the

quad-latches 370 for sequential setting of the digits as they are read from the credit card.

There are four tracks on the tape recorder, and the pick-up heads therefrom are connected to four lines 374 to provide ten digits in binary form. The lines 374 are connected to a counter 376. The four lines 374 also are connected to a toggle gate 378, the latter in turn being connected to a binary to decimal decoder 380. The four lines 374 also are connected to a pre-set gate 382 having an output to all pre-sets in the circuit including the BCD encoder 380.

The BCD encoder has an output therefrom on 10 enable lines 384 respectively going to the 10 counters 376.

Each of the counters 376 has four outputs or sets thereof, as indicated at 386 leading to a comparator 388. The quad-latches 370 also have four outputs at 391 leading to the comparator 388. The comparator 388 includes both the local AND circuits 344 and the master AND circuits 346 of FIG. 12. The comparator is connected to an alarm 392. Provision is also made for indicating a good card, as will be brought out hereinafter.

It will now be desired to consider FIGS. 14-17 together. FIG. 15 lies directly above FIG. 14, in vertical alignment therewith, and FIG. 17, lies immediately to the right of FIG. 15, in horizontal alignment therewith. FIG. 16 lies to the left of FIGS. 15 and 14, with the top of FIG. 16 being about on the level with the top of FIG. 15.

The card reader 350 will be seen at the top center of FIG. 15. Only one of the 10 place connections is indicated as a line 394, the total of 10 places being indicated by a label. The line 394 is connected from a transistor switch 358 which is controlled through an inverter 396. The transistor switch also is incorporated in the interface 364, FIG. 13, and is connected through a diode 398 to the line 394. As will be understood, there are 10 such transistors 358 and associated circuitry, each transistor being controlled through a respective inverter 396 from a respective output line 1 through 9 of the binary-to-decimal encoder 380. The tenth output line is taken through an AND gate 400, and more will be said about this later.

The ten digit output connections of the reader 350 are connected into the diode matrix 366 which has the four output lines G, H, I and J, as indicated previously, connected together as a cable 402.

Moving to the left to FIG. 16, the cable 402 again branches out to the four lines G, H, I and J. The interface 368 actually comprises four similar interface circuits, each of which includes an input transistor 404, a Schmitt trigger circuit 406, and a pair of inverters 408. The interface circuits sharpen the circuitry providing excellent pulses, and also convert the voltage from 24 volts from the diode matrix to 3.6 volts output from the interface.

The four outputs from the interface are indicated as lines 410, 412, 414 and 416. The lines go to a first quad-latch 370 indicated in solid lines in FIG. 16, and located within a broken line square 418. The broken line square as indicated symbolically are duplicated at the right, and it will be understood that there is a total of 10 such broken line squares, each having similar circuitry therein. A quad-latch enable line 420 is shown in

FIG. 16, and continuing on over to the right to FIG. 15, considering that there are 10 replicas of the circuit within the square 418, the enable line 420 will be seen to be but one of 10 enable lines connected to the output of the BCD encoder 380. As will be understood, the 10 quad-latches together constitute a quad-latch storage register.

The eight outputs of the quad-latch 370, indicated as 1, $\bar{1}$, etc. are connected as shown in FIG. 16, to the inputs of eight AND gates 422, comprising the comparator 388 of FIG. 13. In turn, the outputs of the AND gates 422 are connected as shown to four NOR gates 424, also comprising a part of the comparator, and otherwise referred to as the local AND gate circuit, having an output at 426, through an inverter 428 to an output line 430.

The counter 376, also enclosed within the broken line square 418, comprises four J-K flip-flops 432, the outputs of which are connected as shown to the AND gates 422. As will be apparent, it is necessary to have ones out of both the quad-latch outputs and the J-K flip-flop outputs to any one AND gate to have a one output from the AND gate. The flip-flops 432 are all connected to a master pre-set line 434, and the S and C inputs of a flip-flop 432 are all connected in parallel to an enable line 436. There is a separate enable line connected to each of the ten circuits at 418. The ten enable lines are all indicated jointly at 436 in FIG. 14, and are connected through inverters 438 from the 1 through 9 outputs of the binary-to-decimal encoder 380.

Turning now to the upper right hand corner of FIG. 14, the input from one track 440 of the tape is connected to a Schmitt trigger circuit 442 to give a square wave of good quality, through a pair of inverters 444 to a buffer or inverter 446, and thus to a tape recorder output line 374 corresponding to decimal digit 1. The other three lines 374 are similarly supplied from the other three tracks of the tape, comprising the lines corresponding to decimal digits 2, 4 and 8, whereby decimal digits 1 through 10 can be supplied by binary information. As is indicated at 448, the usable input must be ground going positive to plus 2.0 volts DC, i.e. a positive going square wave pulse.

The tape recorder output lines 374 continue on to the left to FIG. 16, and are connected to the toggle input connections of the J-K flip-flops 432.

The lines 374 at the upper left corner of FIG. 14, also lead down to the inputs of a pre-set gate 382, two of the inputs being through inverters 450. The reason for this is that a specific code is placed on the tape when it is desired to pre-set to check another number, and this code as leading down to the left of the inverters 450 is 0101. Thus, with the inverters four zeros are applied to the pre-set gate 382, which is a NOR gate, and which therefore supplies an output to an interface or buffer 452 supplying the pre-set line 434 in an emitter-follower configuration.

Immediately below the pre-set gate in FIG. 14 will be seen the toggle gate 378. The inputs are all through inverters 454, since it is desired to toggle when there is a pulse on each line 374, and this must be inverted to provide four zeros into the NOR gate comprising a toggle gate 378. The one output thereof is applied to an inverter 456, leading to the toggle input of a decade counter 458, the four binary outputs of which are con-

ected to the binary-to-decimal encoder 380. It will be observed that the pre-set line 434 also is connected to the decade counter 458, specifically to the CB input thereof.

It will be understood that the input from the toggle gate, through the inverter 456, goes from 1 to 0 each time the gate toggles, and this acts through the decade counter 458 to shift the binary-to-decimal encoder 380 from one enable line to the next.

Commercially available decade counters actually provide only nine active positions, and one rest position. In the present invention, in order to provide a true decimal output, the inverters 438 are connected to outputs 1-9 of the binary-to-decimal encoder 380, the zero position not being connected to anything. Since the outputs are 1's, they are inverted by the inverters 438 to provide 0's for the flip-flop enable lines 436. In addition, a connection is made from output 9 to the toggle input of a J-K flip-flop 460, the CD input of which is connected to the master pre-set lines 434. The \bar{Q} -output is connected through two inverters 462, since the Q-output when toggled is zero and it is zero that is desired. This goes to the first of the flip-flop enable lines 436.

Before leaving FIG. 14, and perhaps slightly out of order, reference will be made to a short one shot trigger circuit 464 having an input line 466. A 0 input is applied on this line when reading is first started, as will be brought out hereinafter. A 0 appears on this line at the start of reading, giving a negative output pulse of rather short duration as indicated at 468. This negative output pulse is applied to a line 470 about which more will be said later, and is connected through an inverter 472 to a long one shot circuit 474 of approximately 10 seconds, the long output being indicated at 476. The positive input 478 to the long one shot circuit 474 is of the same short duration as the negative pulse 468, both being on the order of microseconds, due to the circuit constants employed in the circuits.

The output of the long one shot circuit 474 is taken through an inverter 480 to a line 482. The 0 on this line follows the end of tape reading, since tape reading is timed rather precisely to approximately 9.5 seconds, and the 0 at this point produces various results to be set forth hereinafter. The inverter 480 is connected in cascade to a second inverter 484, having an output line 486 of which more will be said later, and also an output line 488 leading to the master AND circuits 346. The upper end of the line 488 in the upper left corner of FIG. 14 aligns with the lower end of the line 488 in FIG. 15, facilitating alignment of the two figures.

Moving up now to the left side of FIG. 15, the master AND circuit 346 comprises six AND gates 490. The two inputs to the uppermost of the AND gates 490 are from the most adjacent of the circuits 418, and from the next most adjacent of these circuits. As previously noted, there are 10 such circuits, the tenth one being the one shown in FIG. 16, and the inputs to the master ANDs being from the lines 430 in pairs to the five uppermost of the master AND gates. The sixth or lowest master AND gate has one input of +3.6 volts DC, while the other input is from the line 488, as previously mentioned. The outputs of all of the master AND gates 490 are connected in common at 492. RTL logic (resistor-transistor logic) is used throughout. Thus, if the output of any of the AND gates 490 is 0, all of the outputs will

be dragged down to 0, and the output line 492 will be 0. Stated otherwise, all of the inputs at 430 and 488 must be at 1 in order for there to be an output from the master AND gate.

The output line 492 is connected near the right side of FIG. 15 to a Schmitt trigger circuit 494 through an input potentiometer 496 for level setting. The output of the Schmitt trigger circuit is taken through two inverters 497 for shaping, and is connected to an output line 498 leading to the odd-even counter 348. The odd-even counter 348 includes a J-K flip-flop 500 and an AND gate 502 connected to the \bar{Q} -output thereof.

Returning now to FIG. 15, at the left central portion thereof will be seen a scanner oscillator 504 having a pair of NOR gates 506 interconnected as shown in the multivibrator or flip-flop circuit supplied with 3.6 volts DC. The oscillator operates at 1 kilocycle, and the output thereof is applied through successive inverters 508 and 510 for wave shaping, the output thereof being shown as a pulse train 512. The output is connected to an AND gate 514, the output of which leads to a decade counter 516. The decade counter has four outputs as indicated at 518 connected to the binary-to-decimal encoder 362. The decade counter counts each time there is a square wave or positive pulse in.

The second input to the AND gate 514 comprises the output of an AND gate 519. One of the inputs to the AND gate 519 is through an inverter 520 connected to the line A, which in turn is connected through a wire 521 to the output of the AND gate 400. As has been noted, the first input to the AND gate 400 is taken from the 0 output of the binary-to-decimal encoder 362. The second input to the AND gate 400 is taken from the Q-output of a flip-flop 522. The T-input to the flip-flop 522 is taken from the nine output of the BCD encoder 362. The S and C inputs are grounded, while the CD input is connected by a line 524 to a pre-set line 526. The J-K flip-flop 522 is pre-set to zero at the start of an operation so that the Q-output is zero when pre-set. When the BCD encoder reaches output position 9, the J-K flip-flop 522 is toggled to provide a 1 output, whereby to provide the 10th count from the BCD encoder.

The second input to the AND gate 519 comprises the output line 528 of a bounceless switch device to prevent unwanted operation upon possible bouncing of the contacts of a low travel switch upon movement of the reading head. The bounceless switch comprises a NOR gate 530, one input of which is taken at 532 as an emitter-follower output of an interface having an input at 534 from a reader head switch to be discussed hereinafter.

The other input to the NOR gate 530 comprises the output of a NOR gate 536, one input of which is the output 528 of the NOR gate 530, and the other of which is from a line 538 which is connected to the output of an interface 540 in emitter-follower configuration. The input to the interface 540 at 542 likewise is taken from a switch controlled by the reader head, as will be brought out hereinafter. The output of the interface 540 also is connected to a line 544 leading to the upper right corner of FIG. 15 past a shaping network 546 to a one shot circuit 548 including a pair of interconnected NOR gates 549 and 550 in a pulse generator or mono-stable flip-flop circuit feeding a second pair of

NOR gates 552 and 554, the latter through an inverter 556, as shown. The output is connected at 558 to the pre-set line 526 and also to the line D. The line D should now be followed to FIG. 17.

Referring now to FIG. 17, the D line is connected to the CD input of a J-K flip-flop serving as an odd-even counter. The line 498 (also identified as E) previously mentioned is connected to the T-input of the flip-flop 500. The SC inputs to the flip-flop 500 are connected at 560 to the C line, also identified for convenience at 482 in FIG. 14.

The output from the odd-even counter or flip-flop 500 is taken at \bar{Q} leading at 562 to the NAND gate 502, as previously mentioned. If the number of a card comes up an odd number of times, then there is an output from the odd-even counter 500 to the NAND gate 502, whereas if the number comes up an even number of times, then there is no output, and there is no indication of a hot card. The second input to the NAND gate 502 is from the line 482.

The output from the NAND gate 502 is applied at 564 to an AND gate 566 requiring two 1's in to provide a 1 out.

The second input to the AND gate 566 at 568 comprises the output of a NAND gate 570. One input to this NAND gate 570 is indicated at 486, which leads back to the output of the long one shot 474. The second input to the NAND gate 570 is taken through an inverter 572 forming the output of a multi-input NOR gate 574. There are four input lines 576 to the NOR gate 574, and these are connected to the first three quad-latches 370 and to a fourth source of zero potential, such as ground, whereby to provide a check for proper identity of the card inserted in the reader. The check in the present system is a negative check. If a number is not found, the card is assumed to be good. Thus, an irrelevant card could appear to be a good card. To prevent this, the first three digits are used as check digits to indicate that the card is one that is supposed to be read. Zero outputs from the first three quad-latches, and hence 0's into the NOR gate 574 on all four inputs will provide a 1 output, whereby to render the circuit operative.

With two inputs into the AND gate 566, there is an output at 578 to a shaping circuit 580 having a level set at 582 to a flip-flop 584 responsive only to a negative pulse in, the flip-flop comprising two NOR gates 586 and 588. The output of the flip-flop 584 is connected through a buffer inverter 590 and hence through a resistor 592 to the control element of a silicon controlled rectifier (SCR) 594 to complete a circuit to the operating coil 596 of a relay CR 3 having a resistor and diode shunt combination 598 thereacross. A circuit is completed through normally closed contacts 600 of relay R2 and normally closed microswitch contacts 602 to a bus line 604, receiving 24 volts DC potential through door interlock switches 606 which are closed as long as cabinet doors of the card reader are closed. A yellow light 608 is connected to the top of the relay contacts 600 to indicate that power is on to that point.

Contacts 610 of relay CR 3 are connected to the bus line 604 through a resistance means 612, the lower end thereof being connected to a red light 614, the lower end of which is grounded. The relay contacts CR 3 are shunted by a capacitor, as are the relay contacts 600.

Thus, when the CR 3 relay is energized upon conduction of the SCR 594, the contacts 610 will close, thereby to cause the red light to light, and thus to signal a bad card.

A normally closed microswitch 616 is connected to the bus 604 and also to normally closed contacts 618 of relay CR 3. Normally open contacts 620 of relay R2 are connected in parallel with the normally closed contacts 618, as is a capacitor.

The lower end of the parallel combination including the relay contacts is connected to a further parallel combination comprising relay CR 2 identified by numeral 622, a resistor, and a diode 624 with the cathode of the diode connected to the bottom of the relay contacts 618. The bottom of this parallel combination is connected to the anode of a silicon controlled rectifier (SCR) 626, the cathode of which is grounded. The control element is connected to and under the control of a buffer inverter 628 through a resistor, the buffer inverter being controlled by a pair of interconnected NOR gates 630 and 632, in turn controlled from a differentiating circuit 634 having a level set at 636. The input to the differentiating circuit is from an inverter 638 actuated by a pair of NOR gates 640 and 642 connected to produce a positive pulse upon receipt of an input, and comprising a one shot delay mechanism to allow the odd-even counter 500 time to indicate a bad card, if the card is bad, before there is an indication of a good card.

The one shot circuit including the NOR gates 640 and 642 is under the control of the line 482, being connected thereto by a differentiating circuit 644 and a shunting diode 646 with the anode grounded and the cathode thereof connected to the input line 648 of the one shot circuit. A 0 appears on the line 482 at the end of the tape.

Toward the upper right corner of FIG. 17, there will be seen normally closed and normally open relay contacts 650 and 652 connected in parallel to the line 604. The bottom ends of these contacts are connected in parallel, and are connected to the parallel combination of normally open relay contacts 652 of relay IR1 and a normally open push button start switch 654. The bottom of this parallel bottom combination is connected to yet another parallel combination comprising relay CR 1 numbered 656, a resistor, and a diode 658, the bottom of this parallel combination being grounded.

Further to the right will be seen a connection from the line 604 to normally closed switch contacts 660, leading to a voltage output line 662 providing positive potential at S4 when the reader head is down. The bottom of the contact 660 and the line 662 is connected to ground through a shunt resistance capacitance circuit 664.

Adjacent thereto a connection will be seen from the line 604 to normally open switch contact 666, leading to a voltage output line 668 providing positive output potential at S3 when the reader head is down. The line 668 is connected to ground through a shunt resistance-capacitance network 670.

The circuit shown in FIG. 18 is associated with the reader head, and is that of the commercial AMP reader previously referred to. This circuit includes 115 volt AC input line 672, having connected thereto in parallel a zener diode 674, and three normally open relay con-

contacts 676, 678 and 680, respectively comprising contacts 1 through 3 of relay IR. The bottom of this parallel combination is connected through a capacitor 682 and resistor 684 to the control element of a triac 686, which is connected at the top of motor windings 688, the upper end of which is connected to the line 672, for lowering the reader head. The triac is also connected to ground, and the control element is grounded through a resistor 690.

Also connected to the 115 voltage line 672 are normally open 3R2 relay contacts 692 paralleled by a capacitor 694. The bottom of this parallel combination is connected to solenoid windings 696, the opposite ends of which are connected to the ground line. The solenoid's effect printing of the credit card in the card printer. A green light 698 parallels the solenoid windings 696.

OPERATION, SECOND EMBODIMENT

The start button is pushed on the reader which activates the motor in the reader. The reader head comes down, first making contact with the punched holes in the credit card to back up fingers in the reader itself. This is the reader control circuitry, and more specifically this is initiated with start button 654, FIG. 710, which will then energize relay CR1 to drive the reader head down. The reader head moves into position with the fingers properly lined up through the holes in the credit card. Microswitch 650 opens, thus stopping the reader head in down position. At the same time there is an initiation of the decade counter 516 (FIG. 15). This counter is normally held inactive through gate 514, FIG. 15. Opening of microswitch unlocks this gate and will allow this decade counter 516 to start counting, the later being decoded by binary-to-decimal encoder 362. The decade counter stops after counting ten places. During the counting procedure the various lines (digit lines) to the reader head are energized. These output lines of binary-to-decimal encoder 362, then go through transistor interface system 396, 358 and through an isolation diode 398, up to the reader via line 394. This is typical of 10 lines and these lines then are scanned sequentially, so that the net result is that it takes somewhere in the order of 1 millisecond to look at the total of 10 digits in the reader. In the reader the digits are converted to a modified binary code through matrix 366, and this particular matrix then will read out a four bit code and this is read out sequentially for each of the 10 digits. The four bit code then is transmitted via line 402 over to another transistor interface primarily consisting of items 404, 406, 408, (FIG. 16) and again this is typical. There are four such interfaces. These then will go to some quad-latch buses 416 (FIG. 16). These buses are common to the 10 quad-latches, and the quad-latches are enabled in order by line 420, which also comes off of the binary-to-decimal encoder 362 as shown on FIG. 15. This then loads the information into the quad-latches. In the meantime further action is held off by the one-shots, further action being the starting of the tape recorder which is held off until the quad-latches have been loaded with the proper set of digits which will be used for comparison. In FIG. 14 the short one-shot 464 holds off any further action until the numbers have been loaded into the quad-latches for further processing. Once they are loaded in this one-

shot will then fire which in turn will activate long one-shot 474, and this then will enable further action of the system. At this time when the system has been enabled with the long one-shot which primarily judges the time that the reader head will remain down, the tape recorder is running. Certain information will enter the system through the tape reader. From the tape recorder the system is entered at point 440 (FIG. 14), to go through the Schmitt trigger and shaping circuits typically shown at 442, 444, 446. This then will enter the system immediately after 446 at inputs 1, 2, 4 and 8. The inputs then transverse to a set of four bus lines 374. These bus lines are common to 10 flip-flops 432 (FIG. 16). These also are common (FIG. 14) to the inputs of the preset gate 382, and the toggle gate 378, upon the proper code which precedes every set of 10 digits. This is a preset code. The preset gate 382 will be activated. This acts through a transistor driver 452 to preset all counters 432 (FIG. 16). It will also preset decade counter 458 (FIG. 14), and this assures that everything has been preset to the proper position to start accepting the digits.

On a 0000 code (four zeros) toggle gate 378 (FIG. 14) is activated and this then will give a toggle pulse which activates decade counter 458 which in conjunction with the binary-to-decimal encoder 380 will activate various flip-flops 432 (FIG. 16) in order, one at a time sequentially so that at the proper time the particular codes which are on bus lines 374 (FIG. 14) will be entered into the proper counter 432 (FIG. 16). This then will give an output to various sub-ANDS 422-424 (FIG. 16) which comprise the whole sub-assembly of anding and oring at 388. Assuming that there is a proper match, that is assuming that the outputs of flip-flops 432 (FIG. 16) will match the outputs of the quad-latch in FIG. 16 370. Then there is a sub-AND output which is available at 426. Typically, this will precede sequentially for 10 times in a row and if there is a match 10 times in a row, there is an output at 426 to the master AND connected by line 430.

Assuming a master AND occurs there will be an output which will feed an interface at 496, which is a potentiometer to adjust proper threshold level to the Schmitt trigger circuit. The Schmitt trigger circuit 494 and shaping inverters 497 go via line 498 to an odd-even counter, of FIG. 17, which has previously been preset to a 0. This will then toggle the odd-even counter and depending on how many times this counter has been toggled will set it in a position as to whether the counter calls for a good card or a bad card.

If the counter is toggled once or any odd number of times, it will then treat the card as a bad card. If the counter is toggled twice, or any even number of times, it is then effectively reset and the system will then look at this counter as if a good card has occurred and the reason for this is that numbers can be added to the ends of the magnetic tape without having to indicate whether the numbers are good or bad or having to go to an indexing type of system. This counter keeps track of how many times a particular number on the magnetic tape will match a number which has been set into the quad-latches from a credit card. If the match is an odd number of times, it is treated as a bad card, if it is an even number of times it is treated as a good card. This then will set up the logic which follows the system, and

if attention is directed to gate 502 in FIG. 17 it will be seen that nothing particularly can happen at this gate until line 482 has been activated. Line 482 is activated by the long one-shot 474 in FIG. 14. Thus, any action is held off until this long one-shot 474 has reached the time of a complete cycle. Subsequently, action continues as set forth hereinafter. If the odd-even counter 500 (FIG. 17) is in an unactivated or even position (either one), then gate 502 cannot be activated. Rather, the system starting at 644, 648, etc. continuing on through 628 will be activated. This system is a one-shot system composed of gates 642, 640 and this in effect is an additional timing circuit so that when line 482 is activated it gives gate 502 a chance to run up a bad card. If gate 502 has not been activated by the odd-even counter 500, then a short period later after line 482 is activated, which period is determined by the system including gates 640, 642, SCR 626 will be activated. As soon as 626 is activated relay CR 2 will operate, and this controls several operations. First of all, referring to FIG. 18, as soon as CR 2 is operated two sets of CR 2 relay contacts 678 and 692 will close. One set 692 energizes the green lamp 698 as well as print solenoid 696. This will allow the print roller to go over the invoice and print the embossing of the card onto the invoice as the second set 678 fires the triac 686 to drive the motor 688. The motor will continue to drive through the cycle until it returns to home position. The home position limit switch 616 (FIG. 17) opens the circuit to relay CR 2 which will then open contacts 678 (FIG. 18) stops the motor in the home position. Contacts 692 also open to release print solenoids 696 and to turn off the green (good card) lamp 698.

The second or alternative mode of operation, which at the end of the long one-shot 474 cycle if the odd-even counter 500, is in the one or odd position. This would indicate a stolen, or nonvalid card. The network through gates 502, 566, line 578 and gates 586 and 588, will activate SCR 594. This energizes relay CR 3 596. Such energization does several things. First of all, it will close CR 3 contacts 610, thereby energizing red lamp 614, indicating a bad card has been read. It will also close CR 3 contacts 680 (FIG. 18), this again causing the card reader holder to activate; starting driving the reader head off. Print solenoids 696, FIG. 18 are not energized, so the invoice will not be imprinted. This action will continue until the home position is reached where microswitch 602 will open. This drops relay CR 3, which will in turn deenergize the red lamp 614 and stop the motor and the printer in home position.

The specific examples of the invention are for illustrative purposes only. Various changes will doubtlessly occur to those skilled in the art and will be understood as comprising a part of the present invention insofar as they fall within the spirit and scope of the appended claims.

We claim:

1. Apparatus for comparing numbers such as on a credit card or the like comprising, tape means for storing a group of numbers for sequential readout, each of the numbers of the group having a plurality of digits, and each number appearing on said tape means one or more times, tape readout means, operable on demand, sequentially to read out each number of the group on said tape means and produce output signals corresponding to each digit of each number, number input means for setting in a particular number to be compared against one of the numbers of the group of numbers stored on said tape means, said number input means producing signals corresponding to the digits of the number set therein, comparator means for receiving the output signals from said tape means and the signals from said number input means to produce a compare signal for each digit of the number which are the same, gate means connected to said comparator means only to produce an output therefrom when all of the digits from said number input means correspond to all of the digits of a number of the group of numbers on said tape means, and counter means connected to the output of said gate means to count the number of times the same number appears on said tape means.

2. The apparatus as set forth in claim 1 wherein said counter means is a bistable circuit to register only odd and even counts of the number of times the same number appears on said tape means.

3. The apparatus as set forth in claim 2 wherein each odd count will produce a reject signal and each even count will produce an accept signal.

4. The apparatus as set forth in claim 1 further including means to detect the end of travel of said tape means, signal means to indicate a quality state of the number set in said number input means, said signal means having a first input connected to said means to detect the end of travel of said tape means and a second input connected to said counter means, whereby the quality state of the number set in said number input means is determined by the number of times the number appears on said tape means.

5. The apparatus as set forth in claim 1 wherein the number set into said number input mean corresponds to the identification number of a credit card, said counter means is a bistable circuit to register only odd and even counts of the number of times the same number appears on said tape means, said odd counts indicating a first quality of the credit card number being checked and said even counts, including zero, indicating a second quality of the credit card number being checked.

6. The apparatus as set forth in claim 5 wherein said first quality of the credit card number being checked is that of an invalid credit card, and said second quality of the credit card number being checked is that of a valid credit card.

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