May 29, 1962 J. L. BROWN 3,036,773

INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

Filed Dec. 26, 1957 244 Sheets-Sheet 1

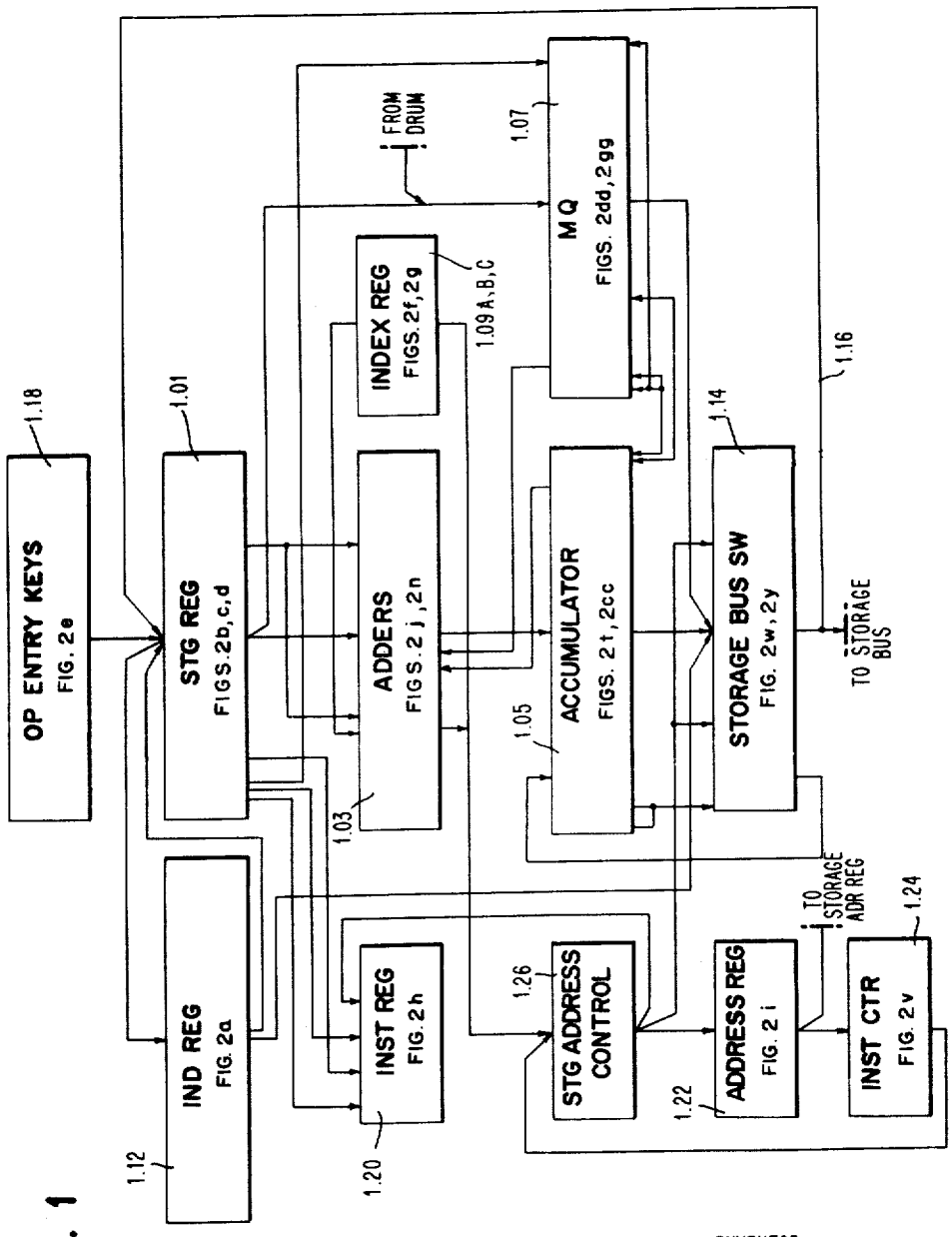


FIG. 1

INVENTOR
JOSEPH L. BROWN
BY Marshall M. Truex
ATTORNEY

FIG. 2a

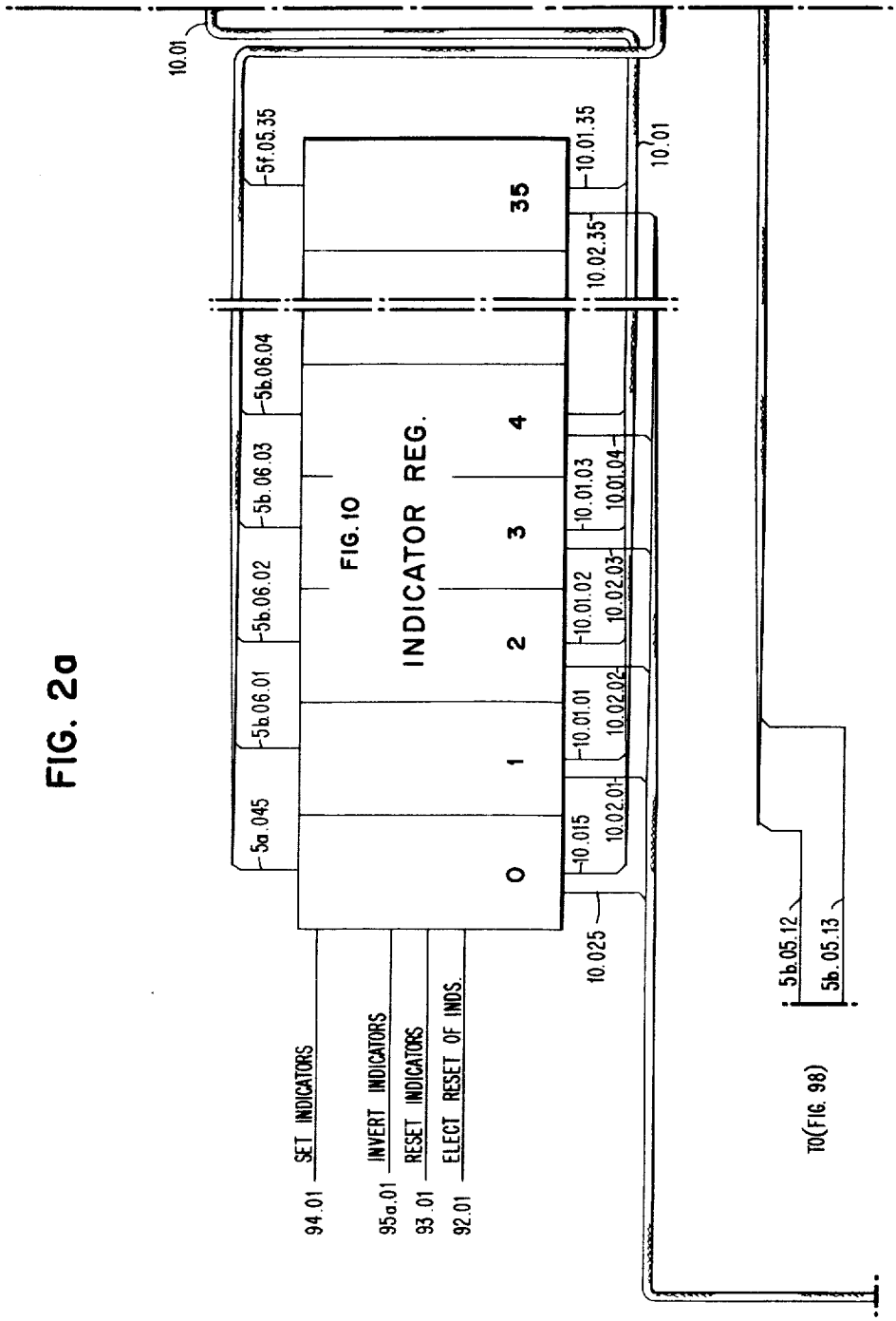
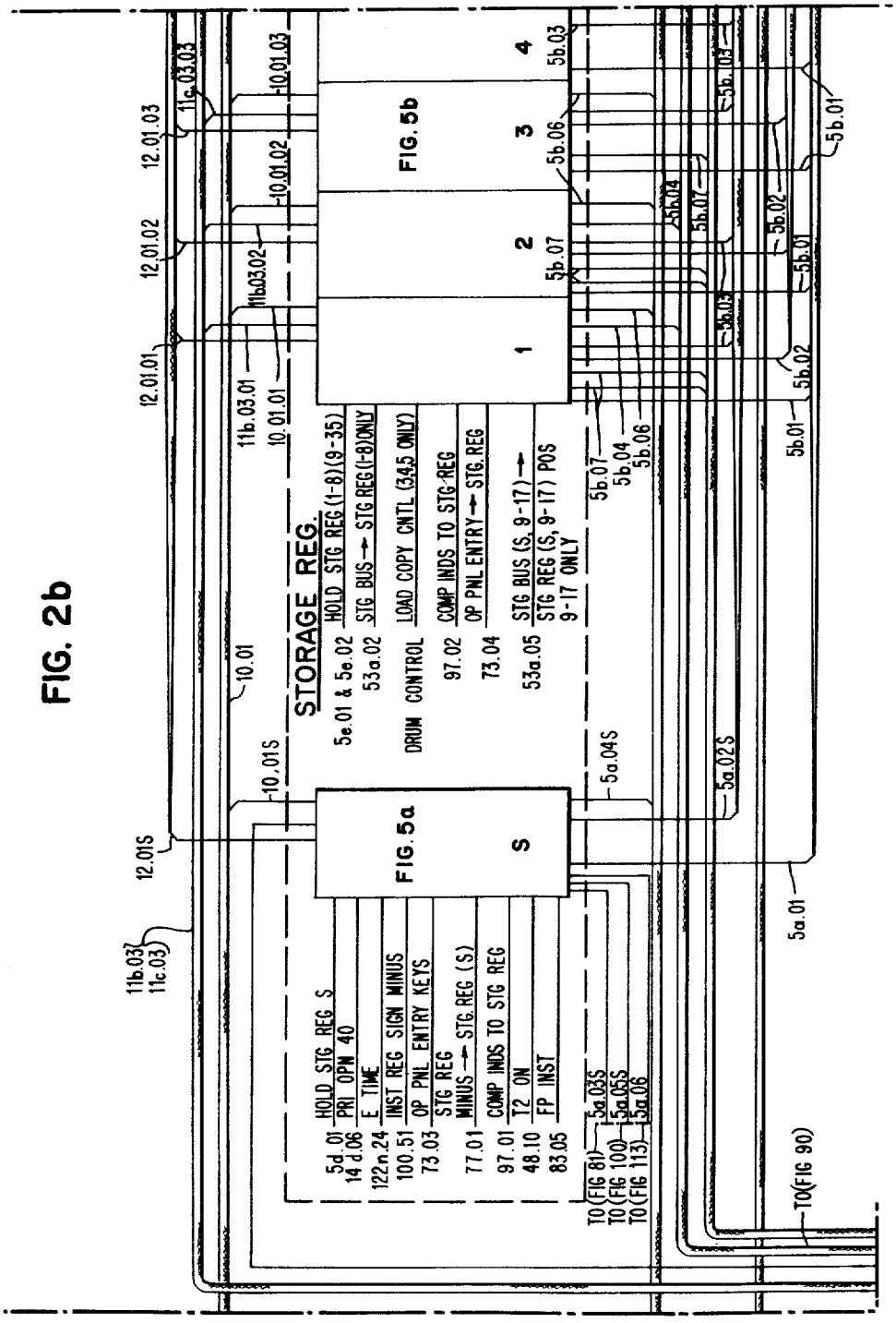

10.01
5f.05.35
10.01.35
10.01
35
10.02.35
5b.06.04
5b.06.03
5b.06.02
5b.06.01
5a.045
INDICATOR REG.
4
3
2
1
0
10.01.03
10.01.04
10.01.02
10.02.03
10.01.01
10.02.02
10.015
10.02.01
10.025
5b.05.12
5b.05.13
TO(FIG. 98)
94.01 SET INDICATORS
95a.01 INVERT INDICATORS
93.01 RESET INDICATORS
92.01 ELECT RESET OF INDS.

FIG. 10

FIG. 2b


STORAGE REG.
HOLD STG REG (1-8)(9-35)
STG BUS → STG REG (1-8) ONLY
LOAD COPY CNTL (34,5 ONLY)
COMP INDS TO STG REG
OP PNL ENTRY → STG REG
STG BUS (S, 9-17) →
STG REG (S, 9-17) POS 9-17 ONLY
DRUM CONTROL
5a.01 & 5a.02
53a.02
97.02
73.04
53a.05
FIG. 5a
FIG. 5b
S
1
2
3
4
HOLD STG REG S
PRI OPN 40
E TIME
INST REG SIGN MINUS
OP PNL ENTRY KEYS
STG REG MINUS → STG REG (S)
COMP INDS TO STG REG
T2 ON
FP INST
5d.01
14 d.06
122n.24
100.51
73.03
77.01
97.01
48.10
83.05
TO (FIG 81)
TO (FIG 100)
TO (FIG 113)
TO (FIG 90)
10.01
10.01S
12.01S
11b.03
11c.03
12.01.01
12.01.02
12.01.03
11b.03.01
11b03.02
10.01.01
10.01.02
10.01.03
11c.03.03
5a.01
5a.02S
5a.04S
5b.01
5b.02
5b.03
5b.04
5b.06
5b.07

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INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

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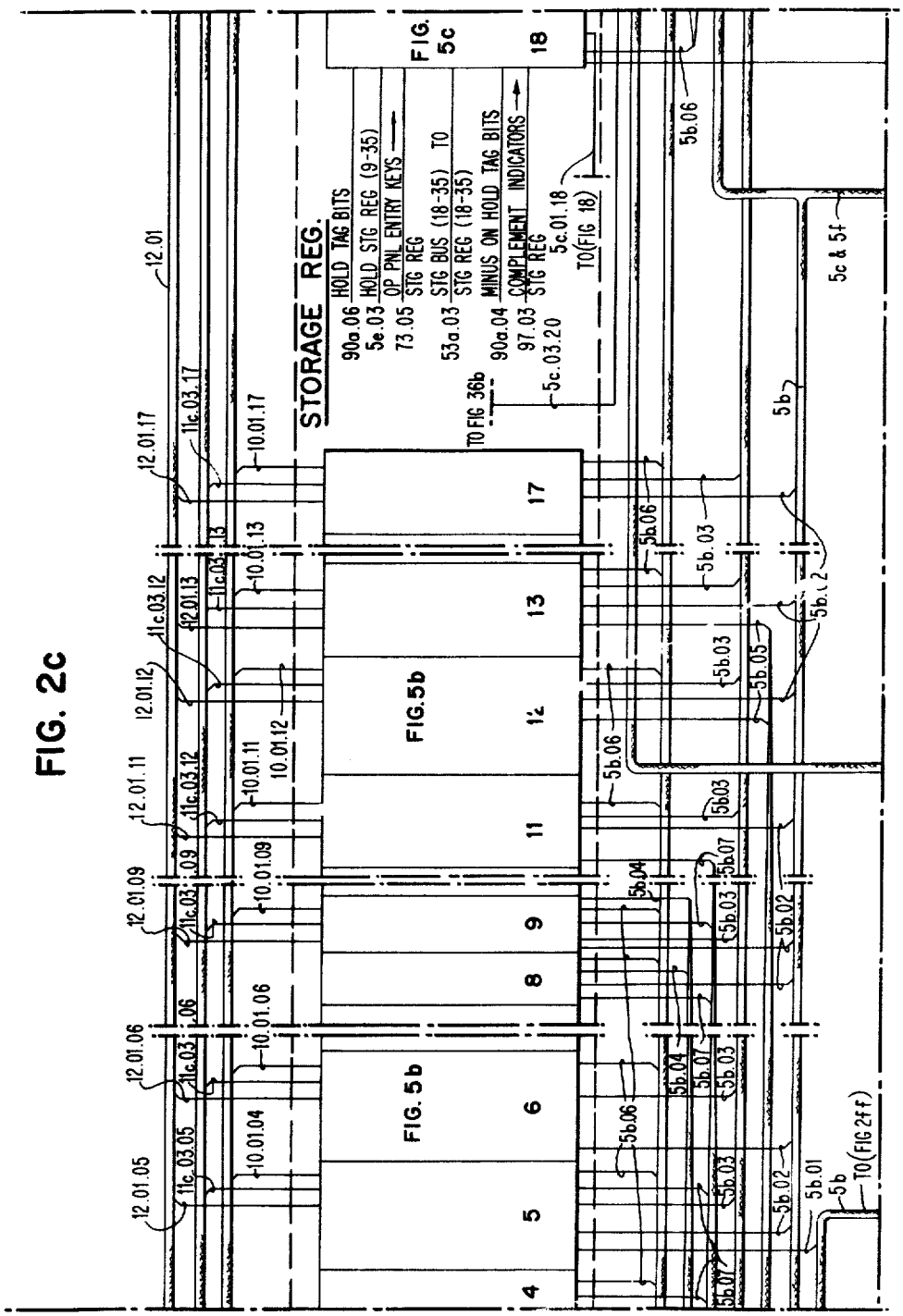
FIG. 2c



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INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

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FIG. 2d

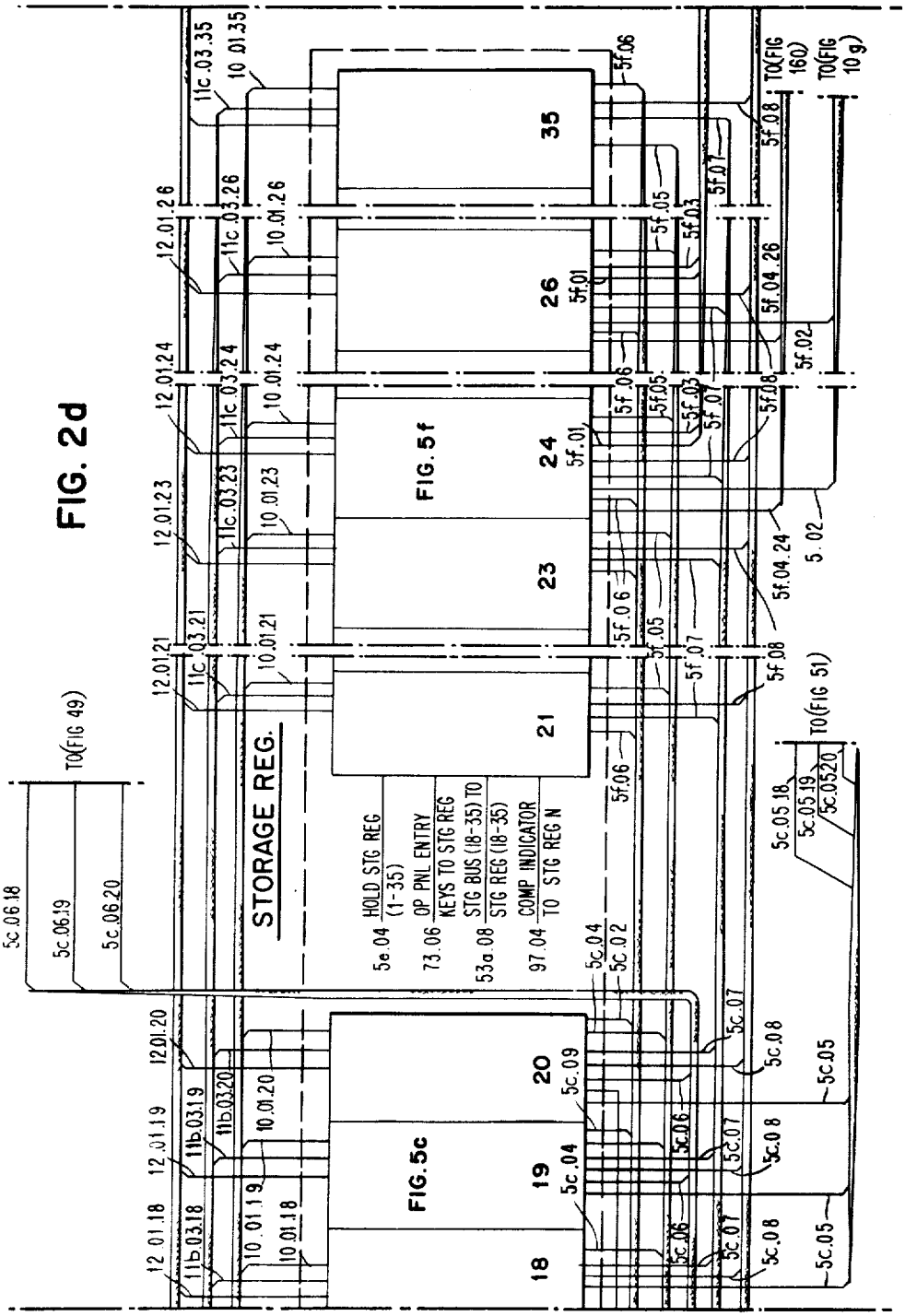
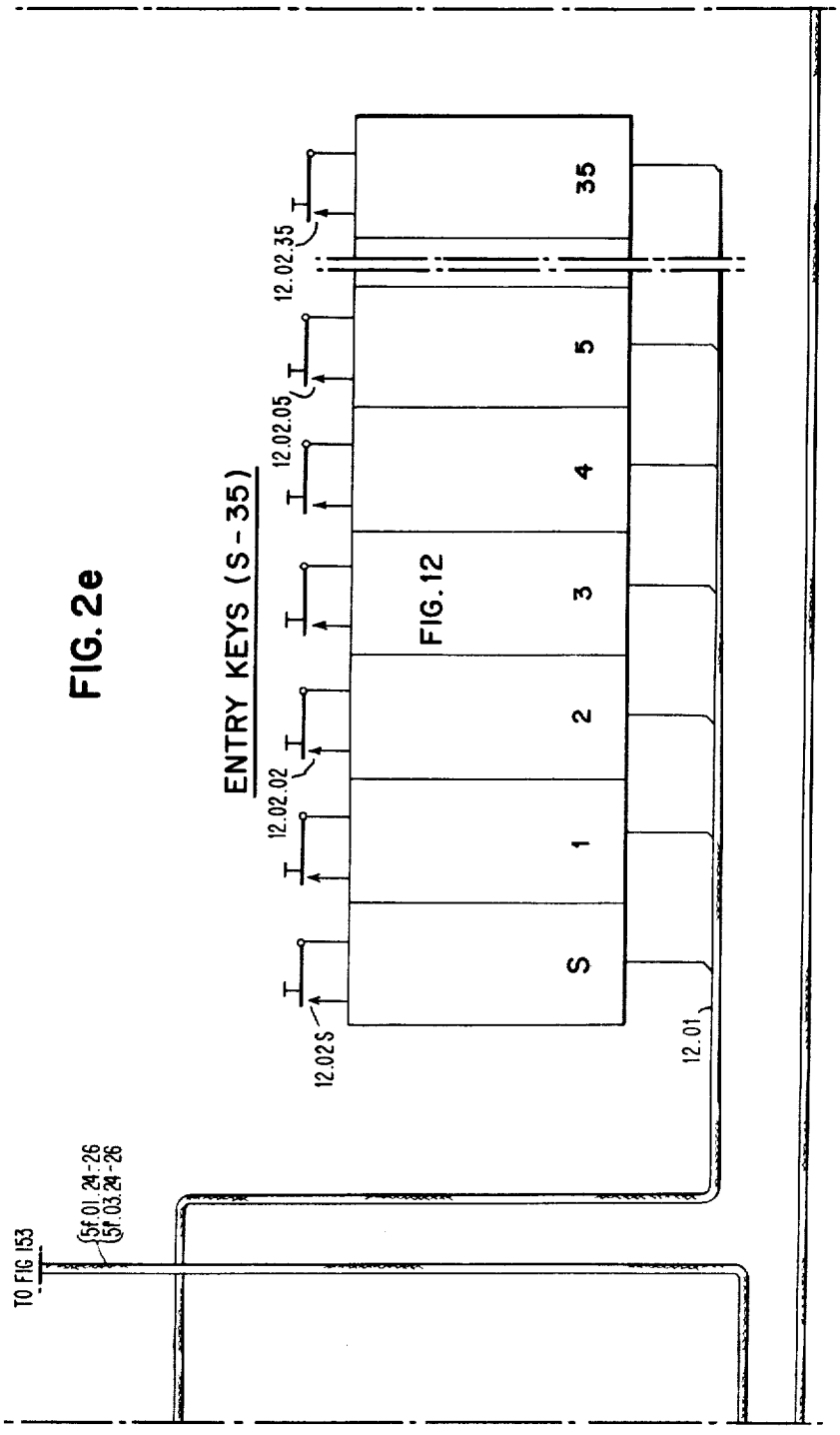


FIG. 2e


ENTRY KEYS (S-35)
12.02.35
12.02.05
12.02.02
12.02S
35
5
4
3
2
1
S
FIG. 12
12.01
TO FIG 153
(5f 01.24-26
5f 03.24-26)

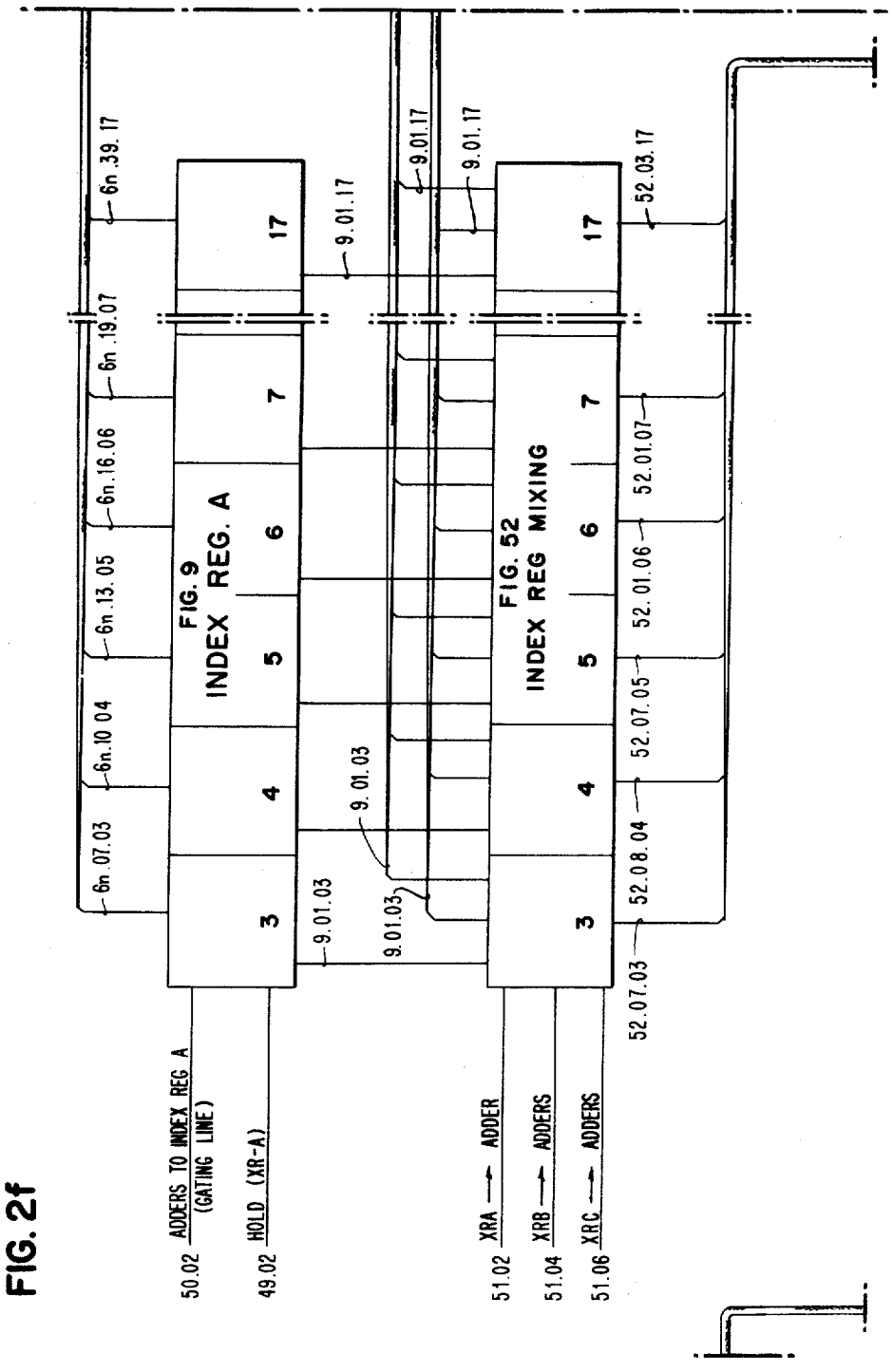


FIG. 9
INDEX REG. A
FIG. 52
INDEX REG MIXING
17
7
6
5
4
3
6n.39.17
6n.19.07
6n.16.06
6n.13.05
6n.10.04
6n.07.03
9.01.17
9.01.03
52.03.17
52.01.07
52.01.06
52.07.05
52.08.04
52.07.03
50.02 ADDERS TO INDEX REG A (GATING LINE)
49.02 HOLD (XR-A)
51.02 XRA → ADDER
51.04 XRB → ADDERS
51.06 XRC → ADDERS

FIG. 2f

FIG. 2g

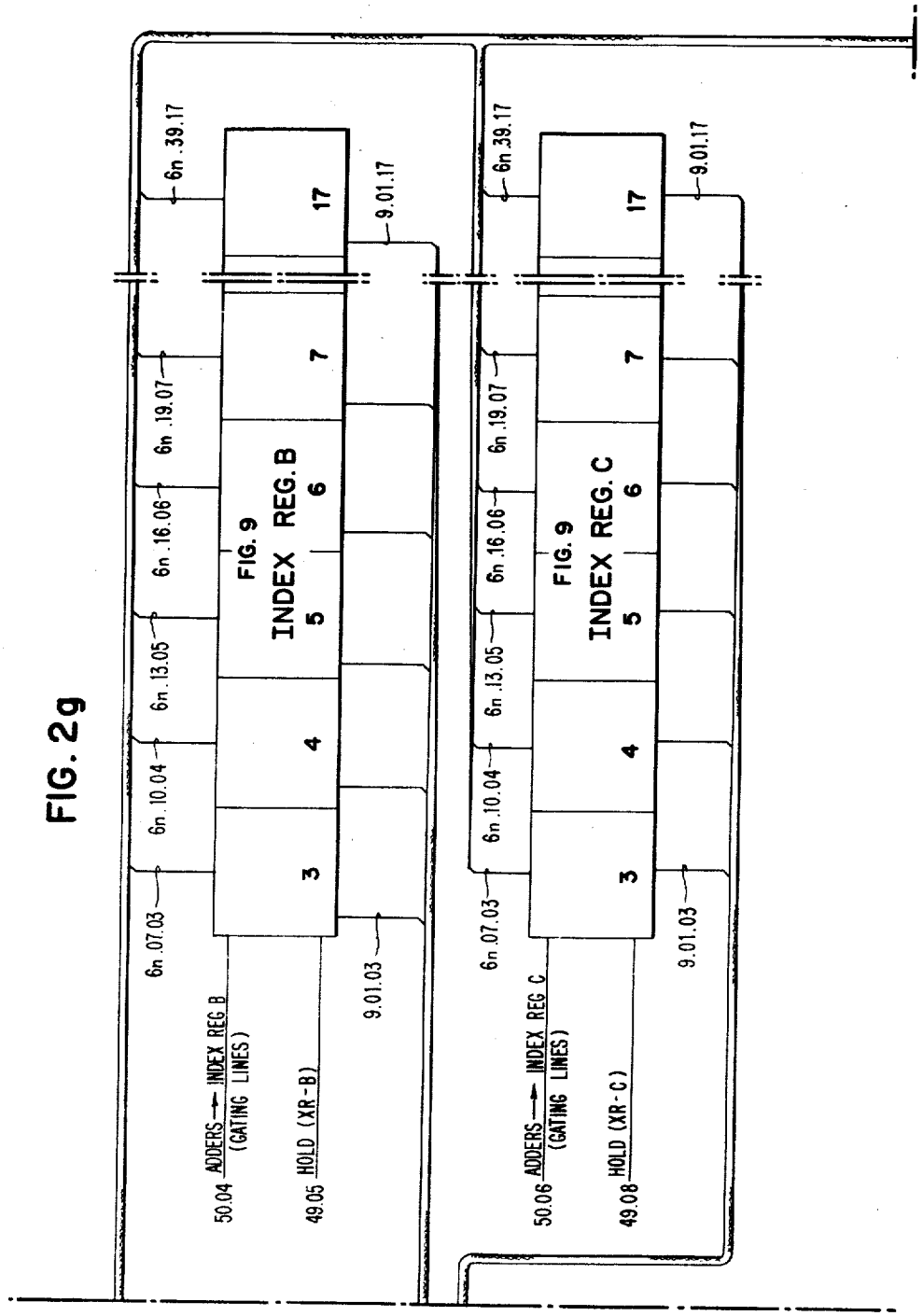


FIG. 9
INDEX REG. B
FIG. 9
INDEX REG. C
6n.39.17
9.01.17
6n.19.07
6n.16.06
6n.13.05
6n.10.04
6n.07.03
9.01.03
17
7
6
5
4
3
50.04 ADDERS → INDEX REG B (GATING LINES)
49.05 HOLD (XR-B)
50.06 ADDERS → INDEX REG C (GATING LINES)
49.08 HOLD (XR-C)

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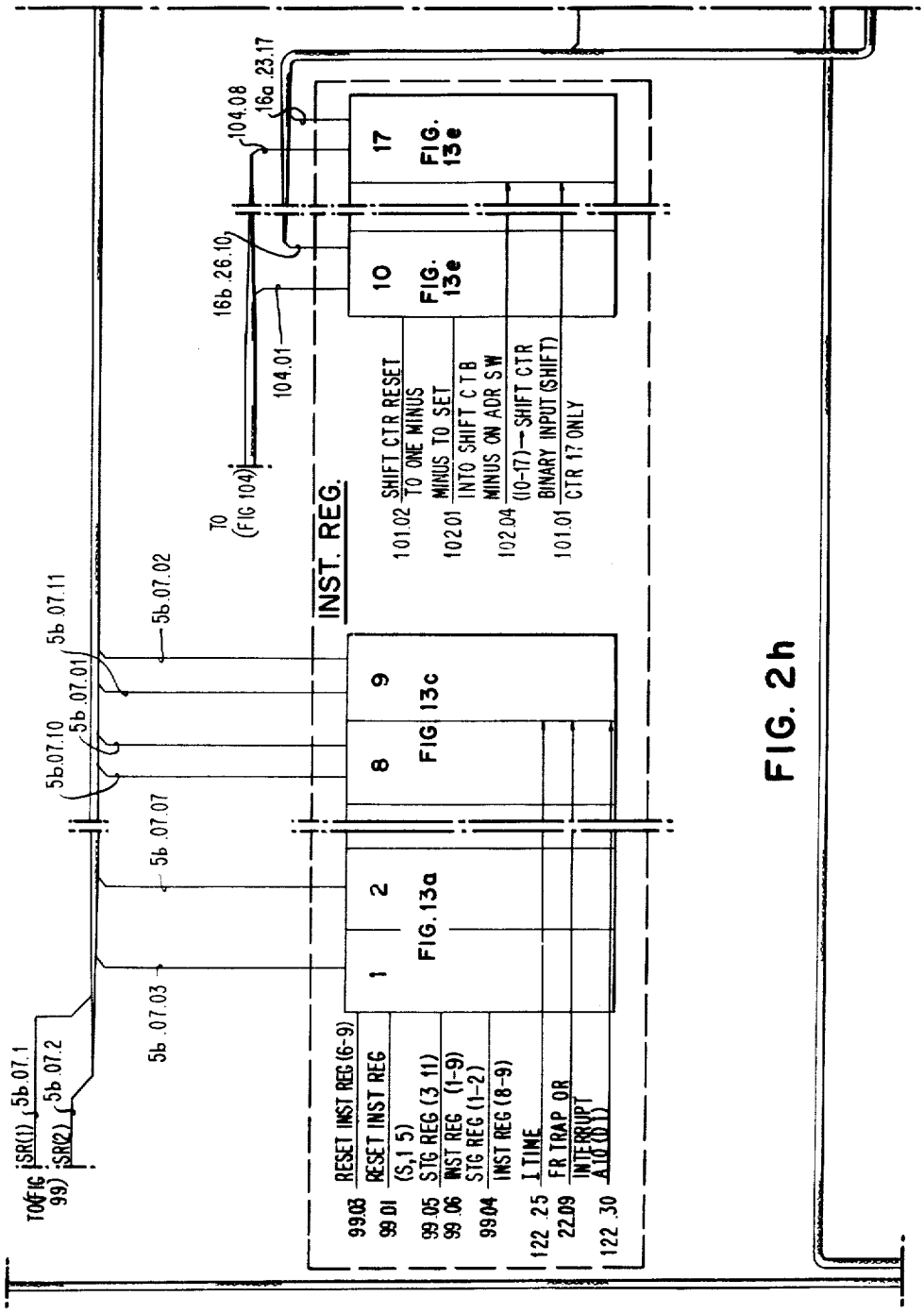

FIG. 2h

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INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

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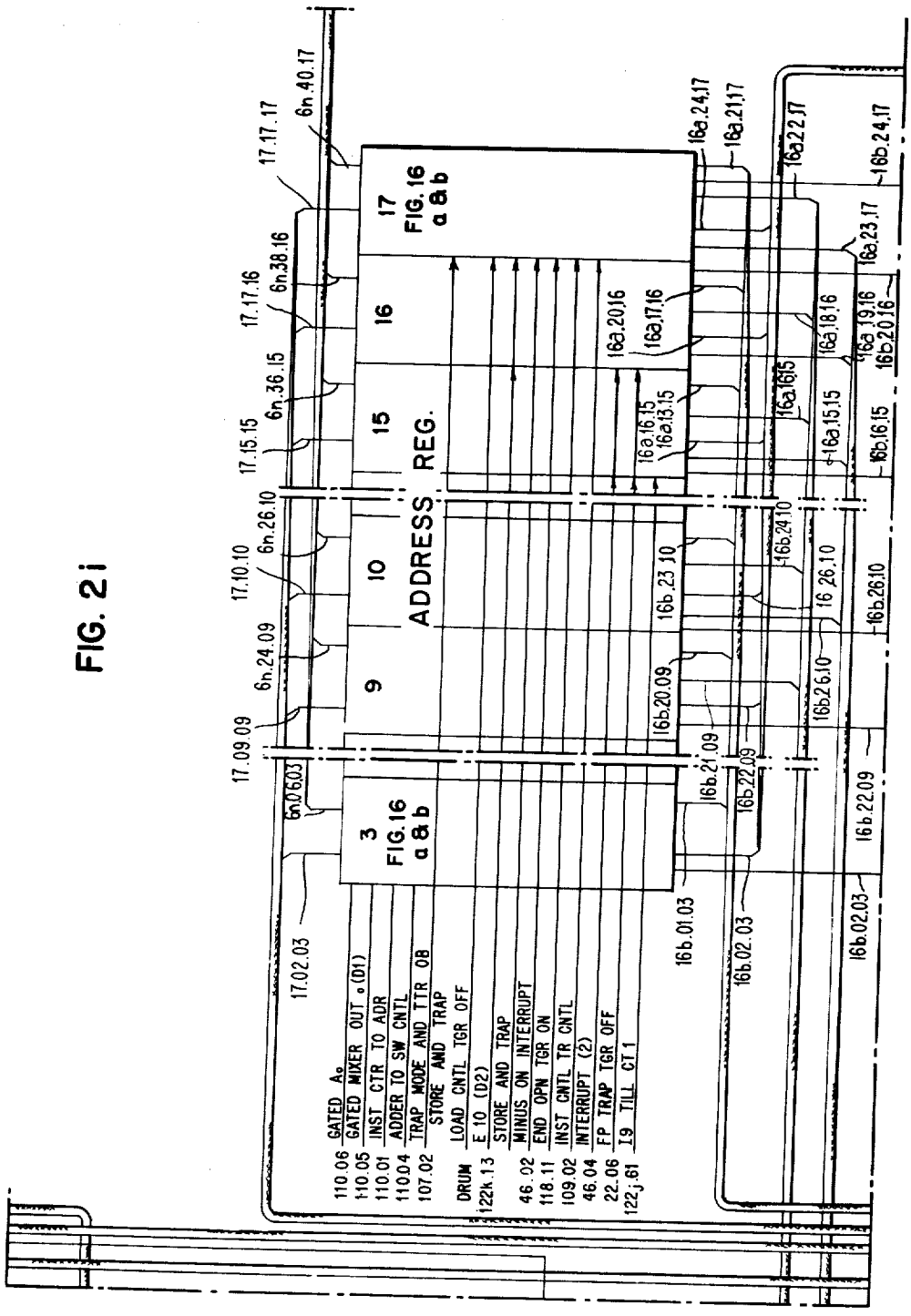
FIG. 2i



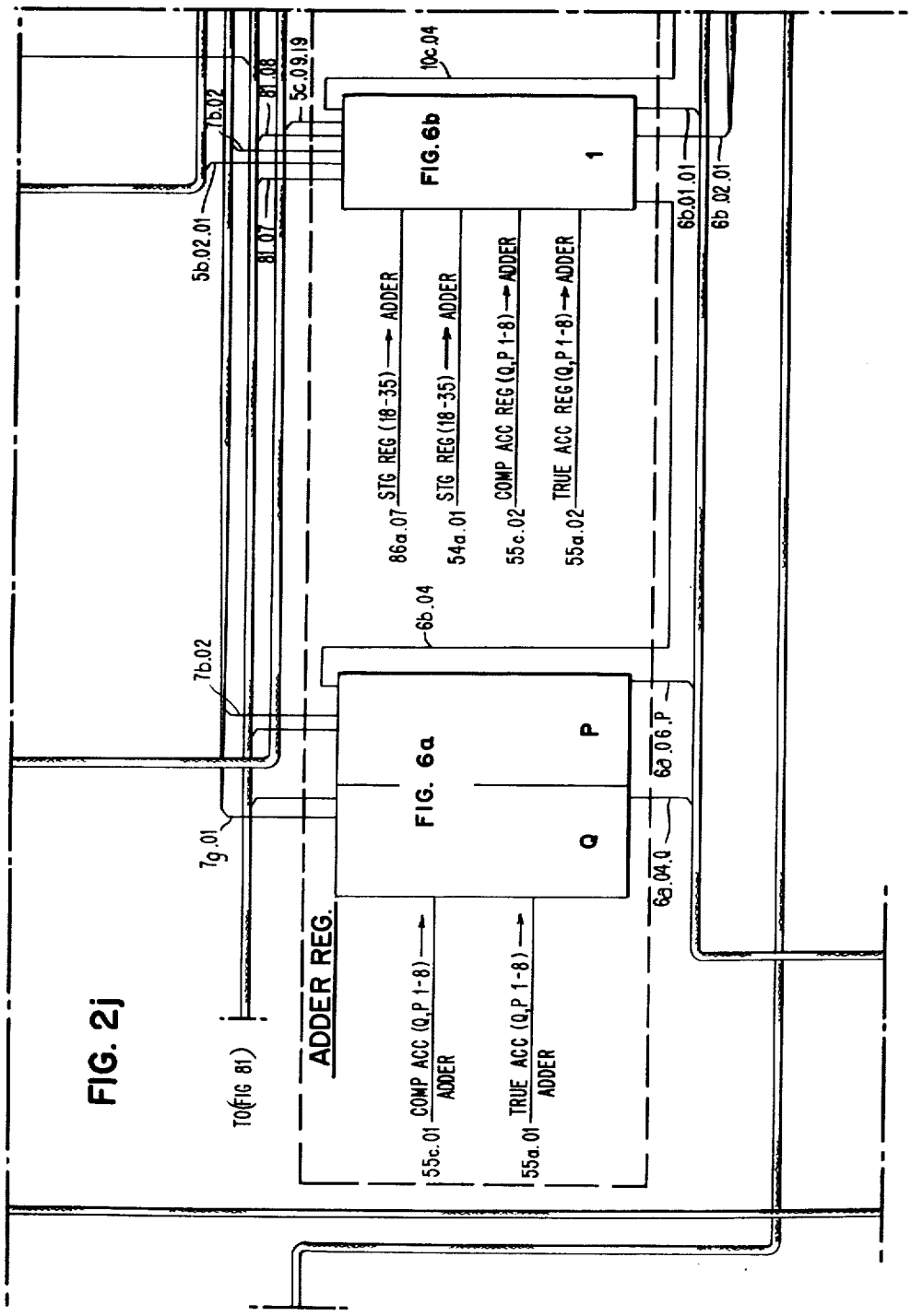


FIG. 2j
FIG. 6b
FIG. 6a
ADDER REG.
10c.04
5c.09.19
81.08
7b.02
81.07
5b.02.01
6b.01.01
6b.02.01
86a.07 STG REG (18-35) → ADDER
54a.01 STG REG (18-35) → ADDER
55c.02 COMP ACC REG (Q,P 1-8) → ADDER
55a.02 TRUE ACC REG (Q,P 1-8) → ADDER
6b.04
7b.02
7g.01
TO (FIG 81)
6a.06.P
6a.04.Q
55c.01 COMP ACC (Q,P 1-8) → ADDER
55a.01 TRUE ACC (Q,P 1-8) → ADDER

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INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE
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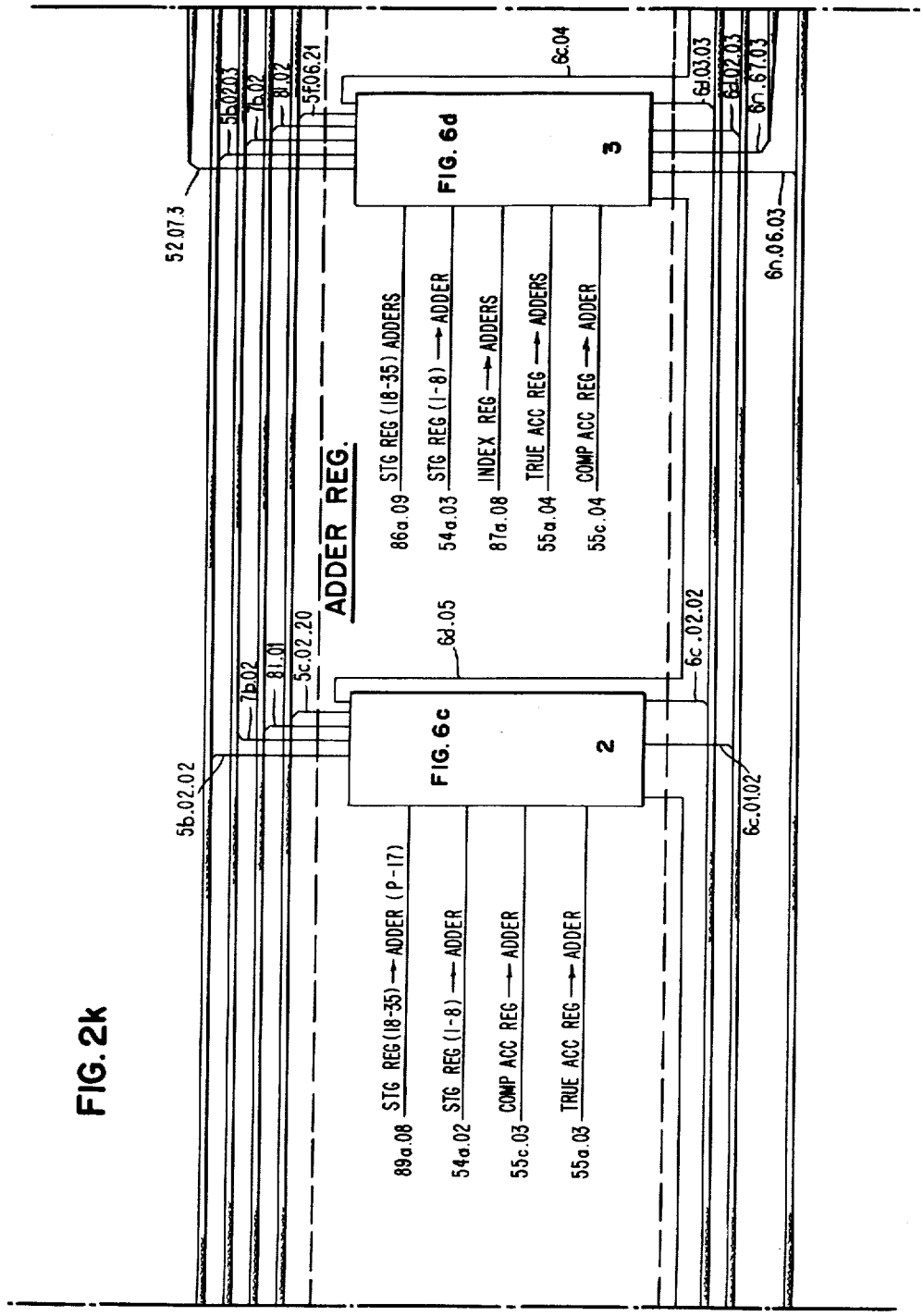
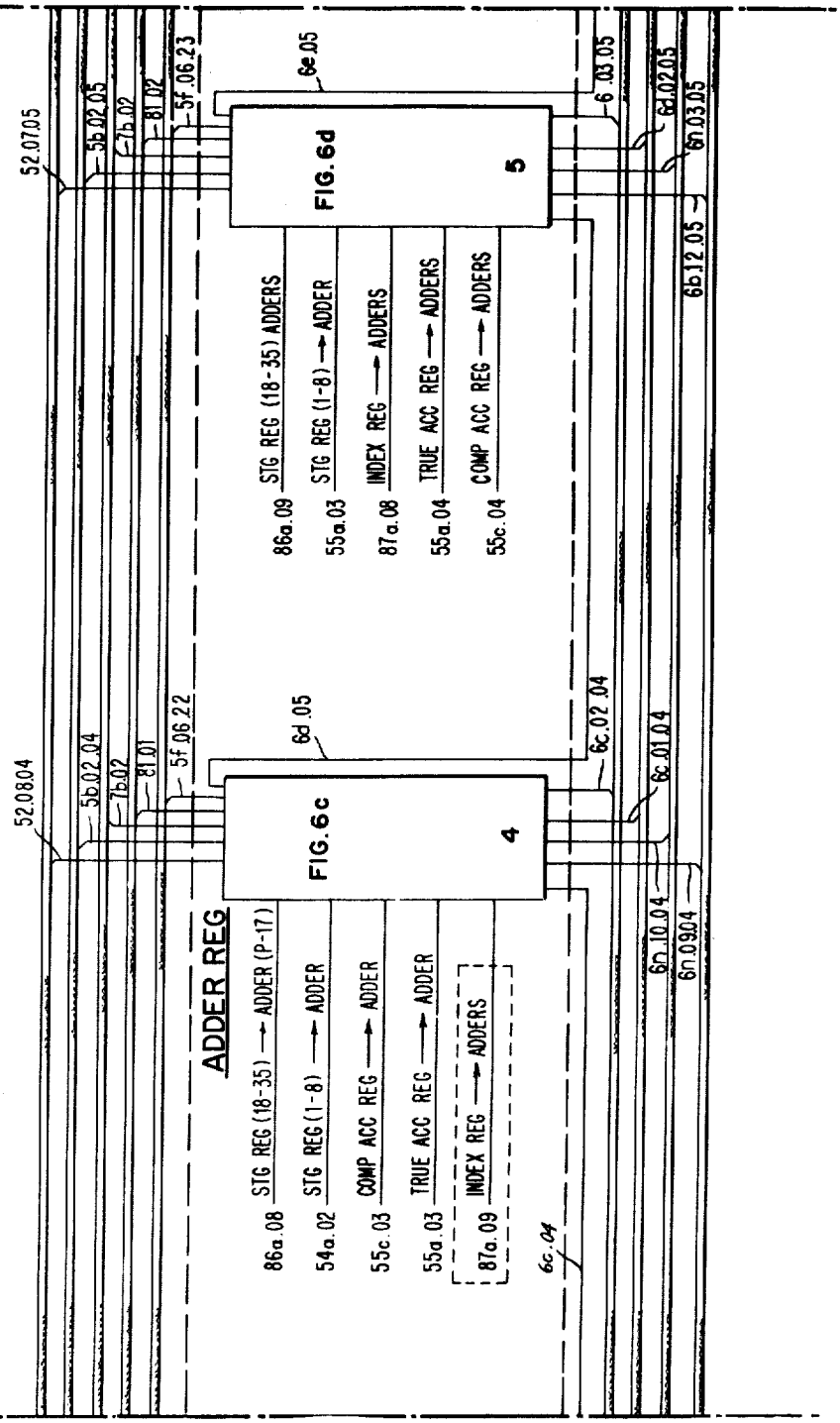


FIG. 2k

FIG. 21


52.07.05
52.08.04
5b.02.05
7b.02
81.02
5f.06.23
5b.02.04
7b.02
81.01
5f.06.22
6e.05
6d.05
FIG. 6d
FIG. 6c
5
4
6.03.05
6d.02.05
6n.03.05
6b12.05
6c.02.04
6c.01.04
6n.10.04
6n.09.04
ADDER REG
86a.09 STG REG (18-35) ADDERS
55a.03 STG REG (1-8) → ADDER
87a.08 INDEX REG → ADDERS
55a.04 TRUE ACC REG → ADDERS
55c.04 COMP ACC REG → ADDERS
86a.08 STG REG (18-35) → ADDER (P-17)
54a.02 STG REG (1-8) → ADDER
55c.03 COMP ACC REG → ADDER
55a.03 TRUE ACC REG → ADDER
87a.09 INDEX REG → ADDERS
6c.04

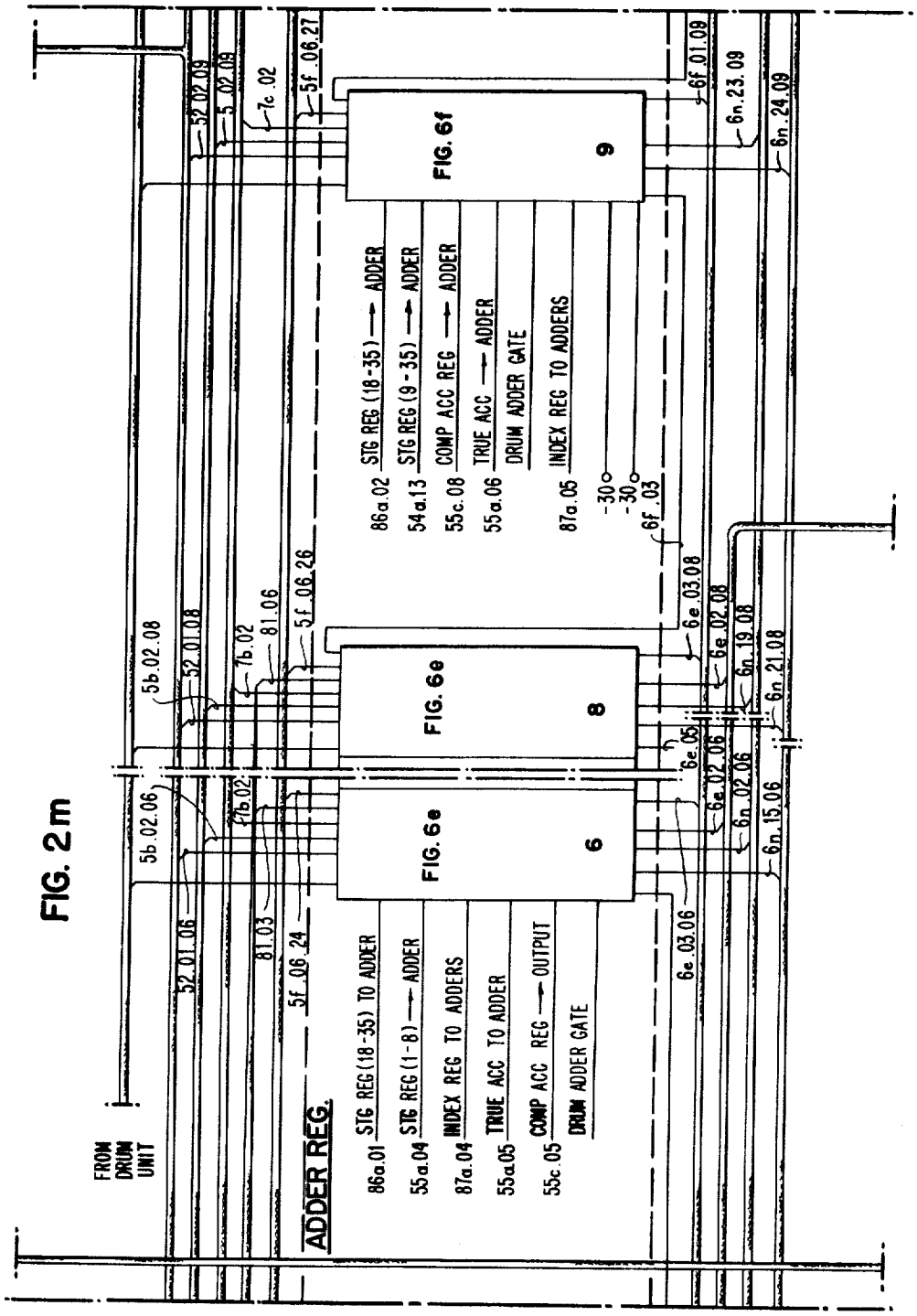


FIG. 2m
FROM DRUM UNIT
ADDER REG.
86a.01 STG REG (18-35) TO ADDER
55a.04 STG REG (1-8) → ADDER
87a.04 INDEX REG TO ADDERS
55a.05 TRUE ACC TO ADDER
55c.05 COMP ACC REG → OUTPUT
DRUM ADDER GATE
FIG. 6e
6
FIG. 6e
8
FIG. 6f
9
86a.02 STG REG (18-35) → ADDER
54a.13 STG REG (9-35) → ADDER
55c.08 COMP ACC REG → ADDER
55a.06 TRUE ACC → ADDER
DRUM ADDER GATE
87a.05 INDEX REG TO ADDERS
-30
-30
6f.03
5b.02.06
5b.02.08
52.01.06
52.01.08
81.03
81.06
5f.06.24
5f.06.26
5f.06.27
7b.02
7b.02
7c.02
52.02.09
5.02.09
6e.03.06
6e.03.08
6e.02.06
6e.02.06
6e.05
6e.02.08
6n.19.08
6n.21.08
6n.15.06
6n.02.06
6n.23.09
6n.24.09
6f.01.09

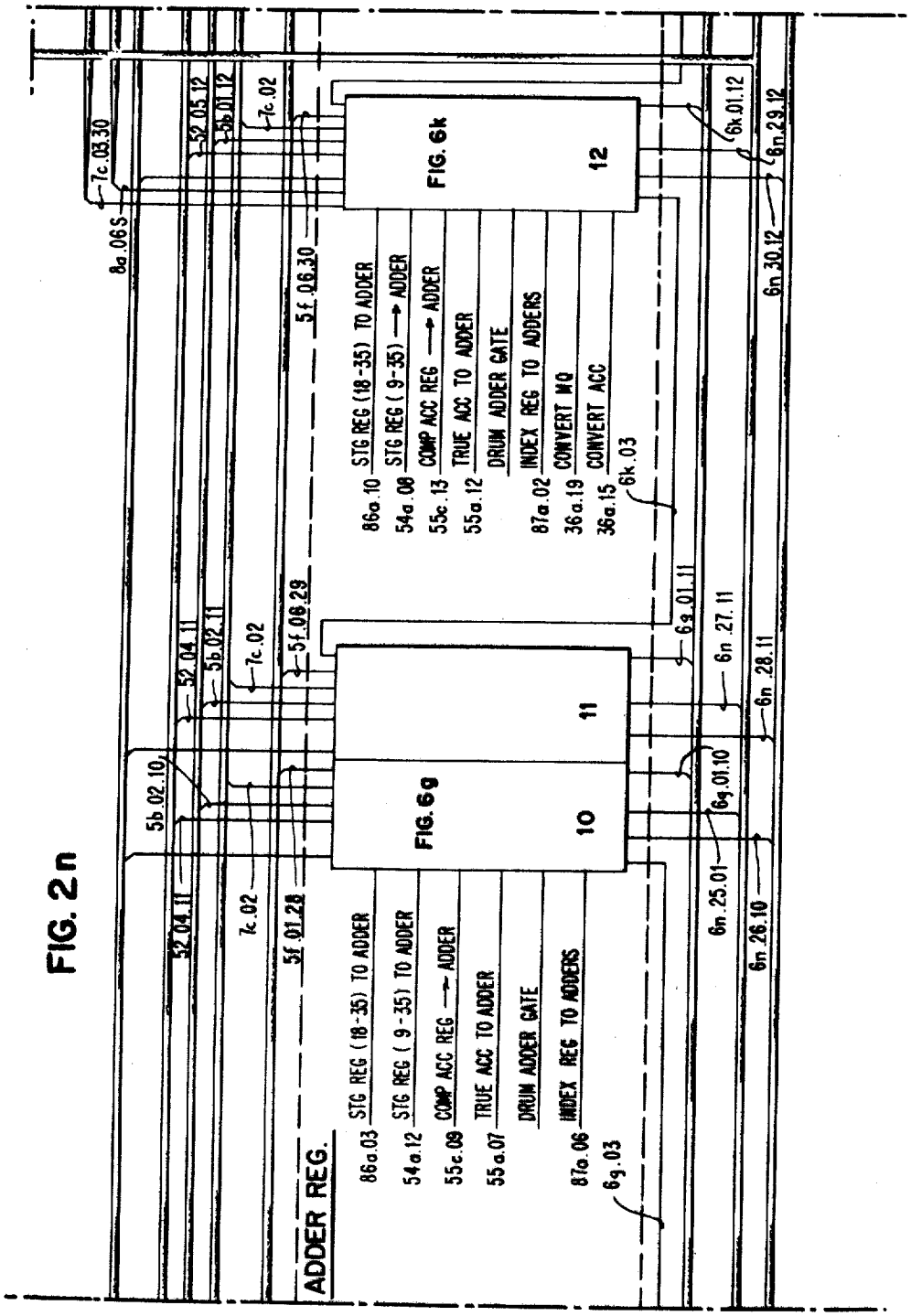


FIG. 2n
ADDER REG.
FIG. 6g
FIG. 6k
10
11
12
STG REG (18-35) TO ADDER
STG REG (9-35) → ADDER
COMP ACC REG → ADDER
TRUE ACC TO ADDER
DRUM ADDER GATE
INDEX REG TO ADDERS
CONVERT MQ
CONVERT ACC
86a.03
54a.12
55c.09
55a.07
87a.06
86a.10
54a.08
55c.13
55a.12
87a.02
36a.19
36a.15
6g.03
6k.03
8a.06S
7c.03.30
5b.02.10
52.04.11
5b.02.11
7c.02
5f.01.28
52.05.12
5b.01.12
5f.06.29
5f.06.30
6g.01.11
6g.01.10
6n.25.01
6n.26.10
6n.27.11
6n.28.11
6n.30.12
6n.29.12
6k.01.12

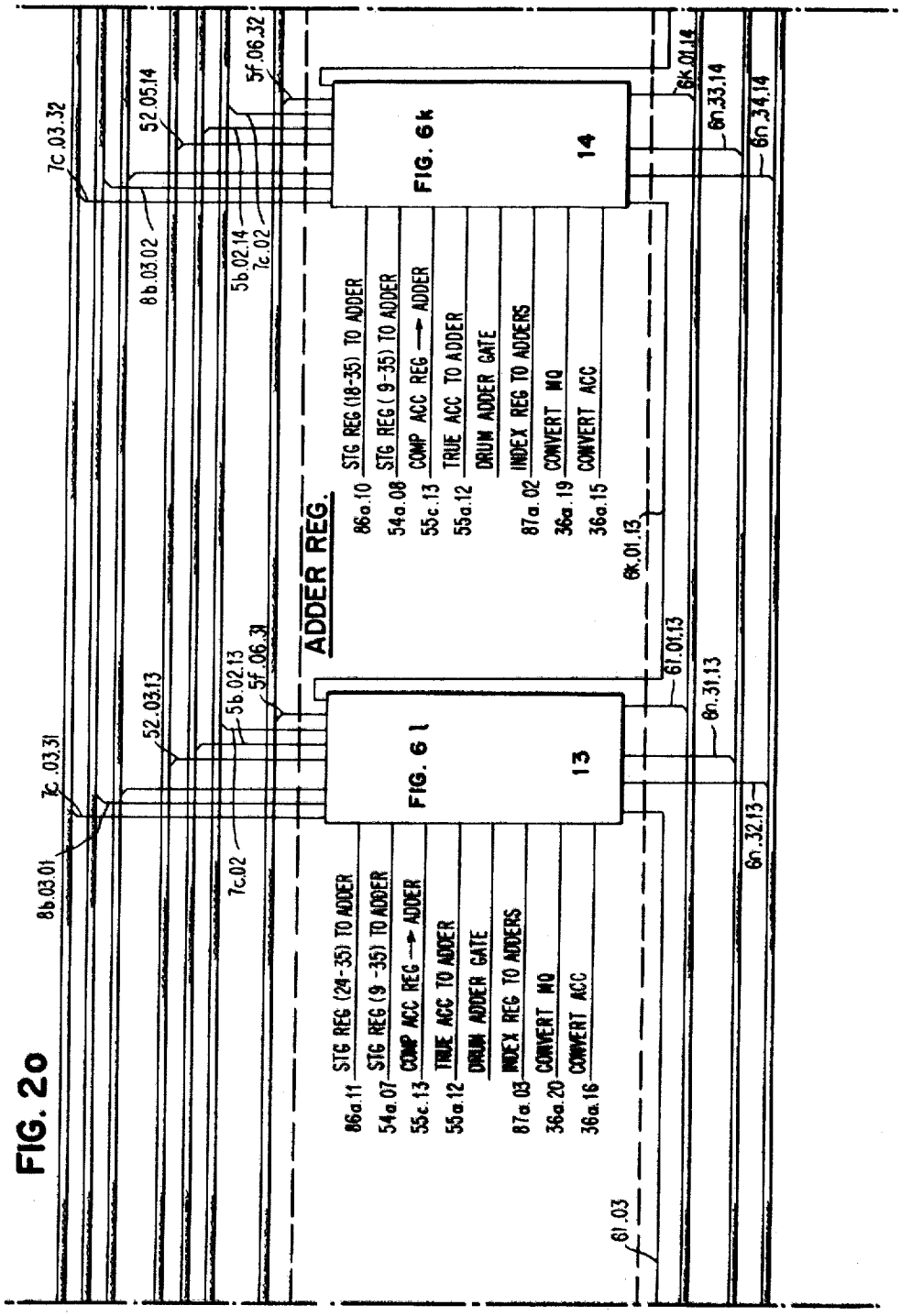


FIG. 20
ADDER REG.
FIG. 6k
14
FIG. 6l
13
STG REG (24-35) TO ADDER
STG REG (9-35) TO ADDER
COMP ACC REG → ADDER
TRUE ACC TO ADDER
DRUM ADDER GATE
INDEX REG TO ADDERS
CONVERT MQ
CONVERT ACC
STG REG (18-35) TO ADDER
STG REG (9-35) TO ADDER
COMP ACC REG → ADDER
TRUE ACC TO ADDER
DRUM ADDER GATE
INDEX REG TO ADDERS
CONVERT MQ
CONVERT ACC
7c.03.32
52.05.14
5f.06.32
8b.03.02
5b.02.14
7c.02
52.03.13
5b.02.13
5f.06.31
7c.03.31
8b.03.01
7c.02
86a.11
54a.07
55c.13
55a.12
87a.03
36a.20
36a.16
86a.10
54a.08
55c.13
55a.12
87a.02
36a.19
36a.15
6k.01.13
6l.01.13
6n.31.13
6n.32.13
6l.03
6k.01.14
6n.33.14
6n.34.14

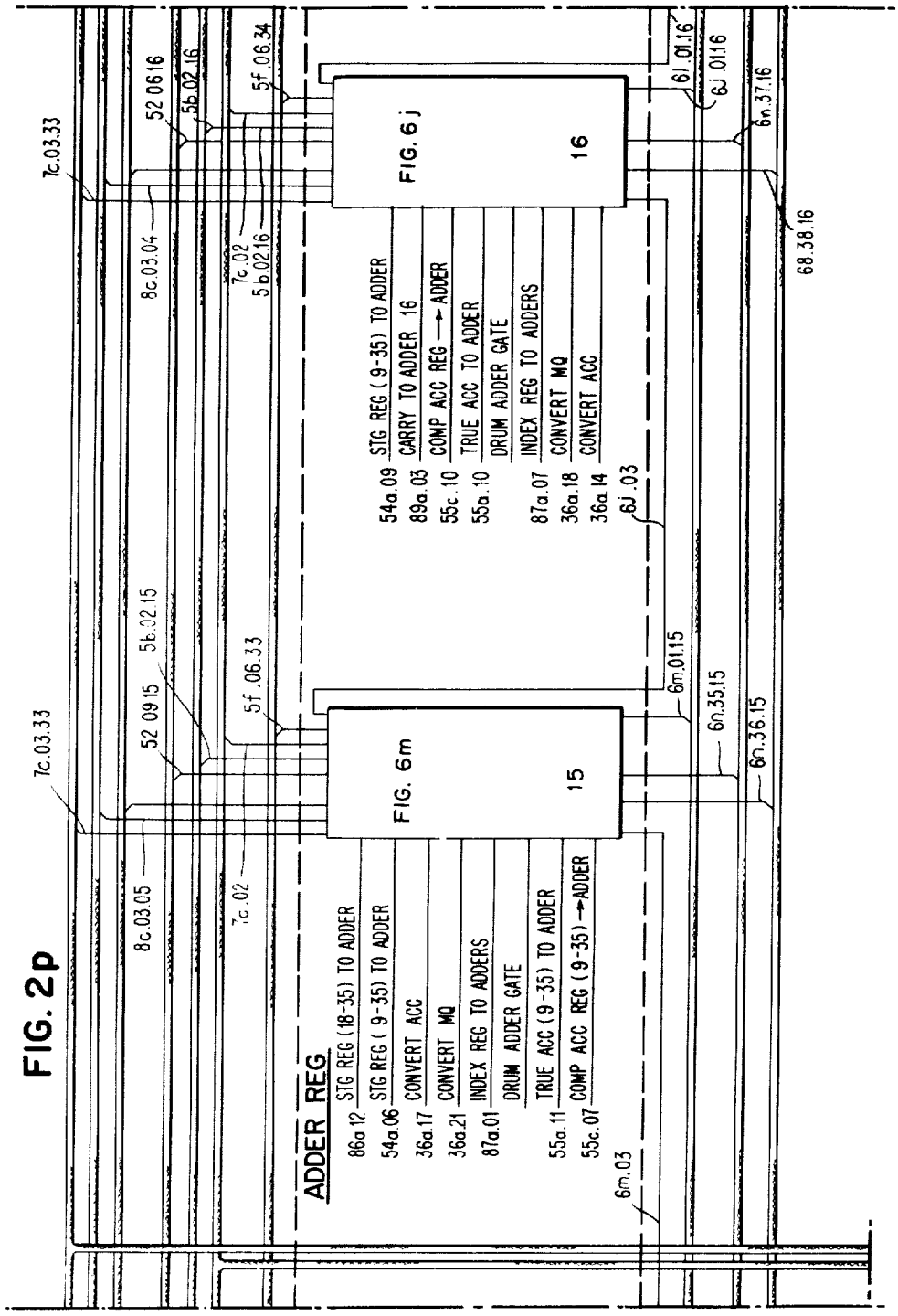
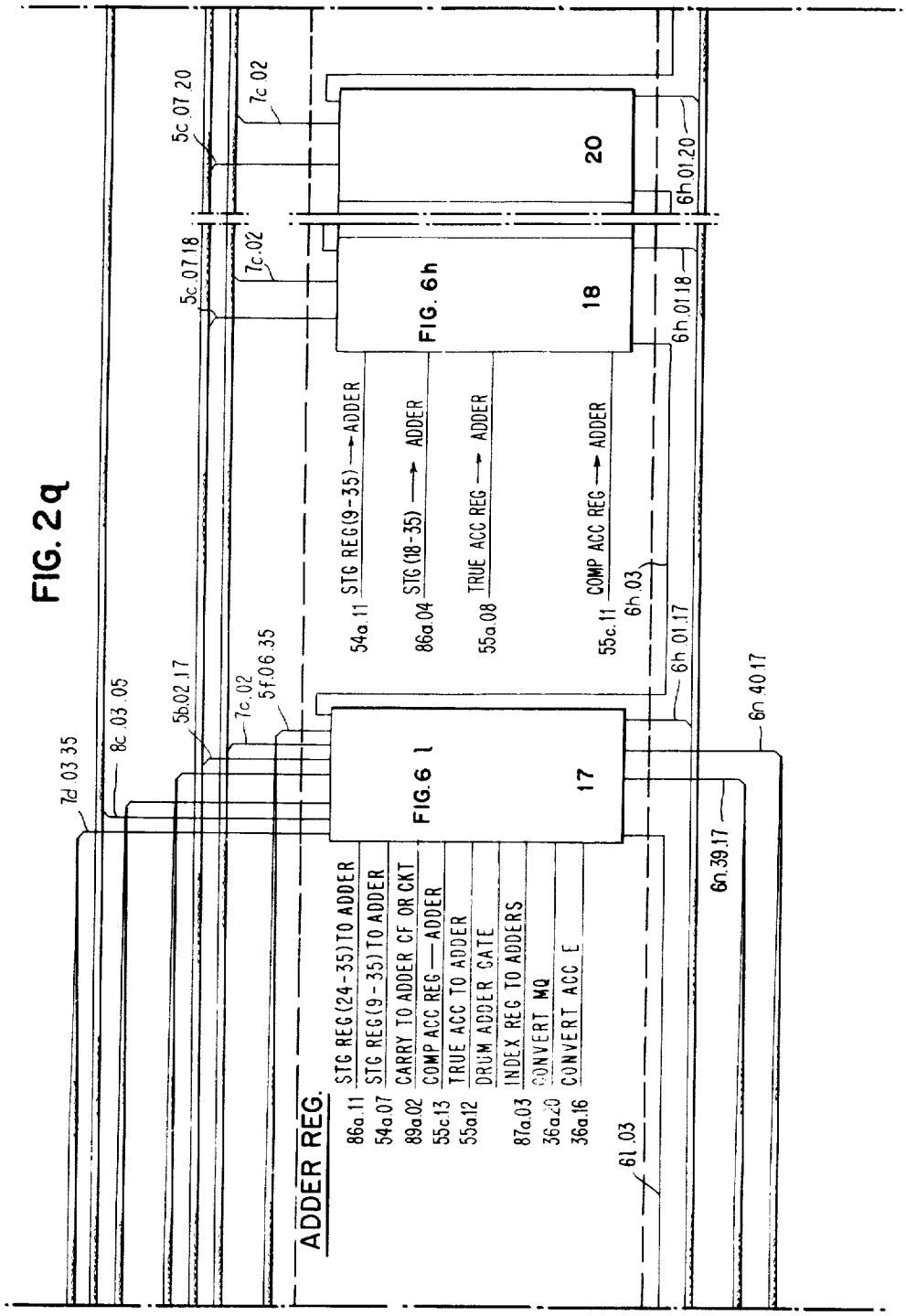


FIG. 2p
7c.03.33
8c.03.05
52 09 15
5b.02 15
7c.02
5f .06.33
ADDER REG
86a.12 STG REG (18-35) TO ADDER
54a.06 STG REG (9-35) TO ADDER
36a.17 CONVERT ACC
36a.21 CONVERT MQ
87a.01 INDEX REG TO ADDERS
DRUM ADDER GATE
55a.11 TRUE ACC (9-35) TO ADDER
55c.07 COMP ACC REG (9-35)→ADDER
6m.03
FIG. 6m
15
6m.01.15
6n.35.15
6n.36.15
8c.03.04
52 06 16
5b.02.16
5f .06.34
7c.02
5b.02.16
54a.09 STG REG (9-35) TO ADDER
89a.03 CARRY TO ADDER 16
55c.10 COMP ACC REG → ADDER
55a.10 TRUE ACC TO ADDER
DRUM ADDER GATE
87a.07 INDEX REG TO ADDERS
36a.18 CONVERT MQ
36a.14 CONVERT ACC
6J .03
FIG. 6 j
16
6l .01.16
6j .01.16
6n.37.16
68.38.16

FIG. 2q


5c.07 20
7c 02
20
6h.01 20
5c.07 18
7c.02
FIG. 6h
18
6h.01 18
54a.11 STG REG(9-35) → ADDER
86a.04 STG (18-35) → ADDER
55a.08 TRUE ACC REG → ADDER
55c.11 COMP ACC REG → ADDER
6h.03
6h.01.17
6n.40.17
7d.03.35
8c.03.05
5b.02.17
7c.02
5f.06.35
FIG. 6 l
17
6n.39.17
ADDER REG.
86a.11 STG REG(24-35) TO ADDER
54a.07 STG REG(9-35) TO ADDER
89a.02 CARRY TO ADDER CF OR CKT
55c.13 COMP ACC REG — ADDER
55a.12 TRUE ACC TO ADDER
DRUM ADDER GATE
87a.03 INDEX REG TO ADDERS
36a.20 CONVERT MQ
36a.16 CONVERT ACC E
61.03

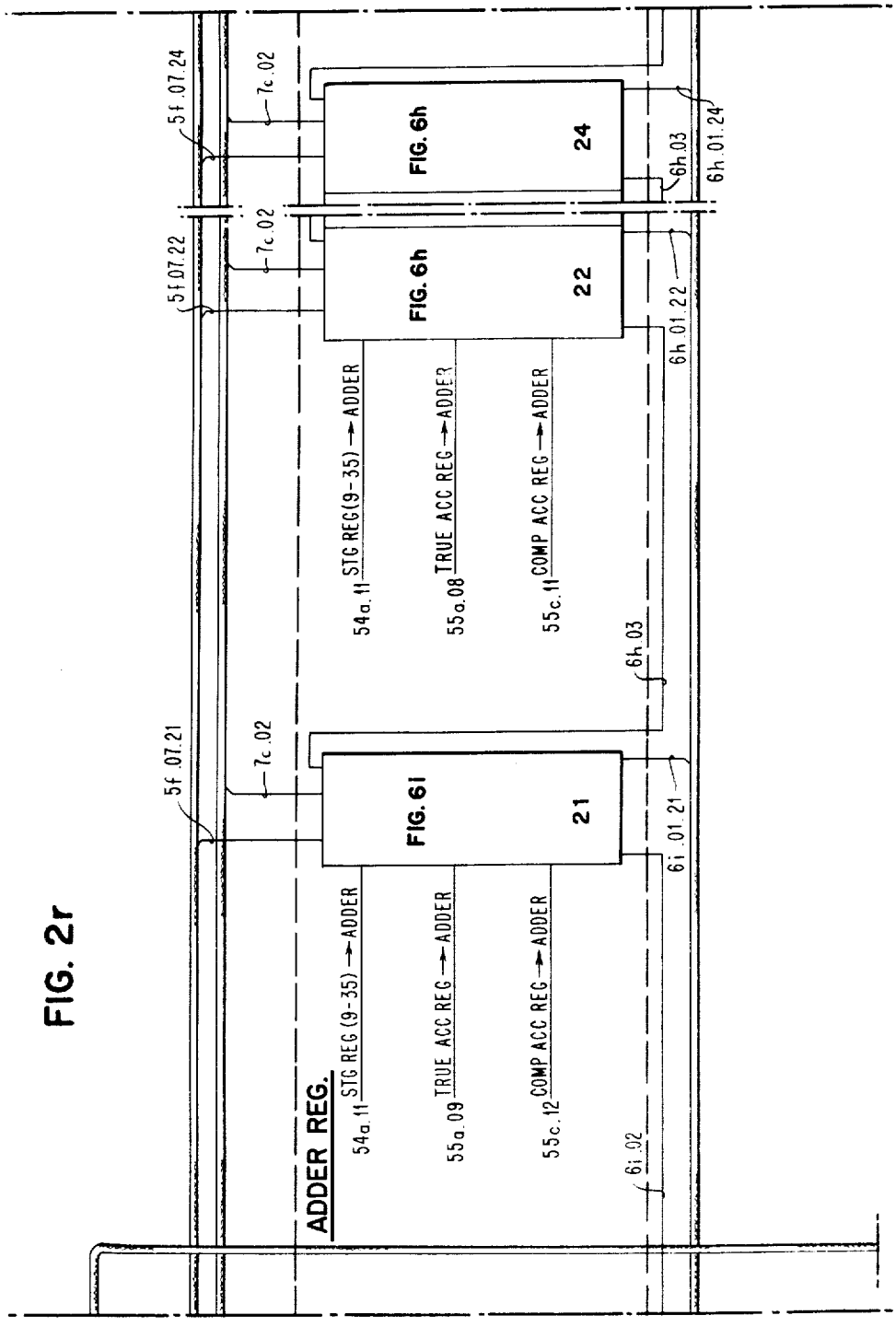

5f.07.24
7c.02
FIG. 6h
24
6h.03
6h.01.24
5f.07.22
7c.02
FIG. 6h
22
6h.01.22
54a.11 STG REG(9-35) → ADDER
55a.08 TRUE ACC REG → ADDER
55c.11 COMP ACC REG → ADDER
6h.03
5f.07.21
7c.02
FIG. 6i
21
6i.01.21
ADDER REG.
54a.11 STG REG (9-35) → ADDER
55a.09 TRUE ACC REG → ADDER
55c.12 COMP ACC REG → ADDER
6i.02

FIG. 2r

FIG. 2s

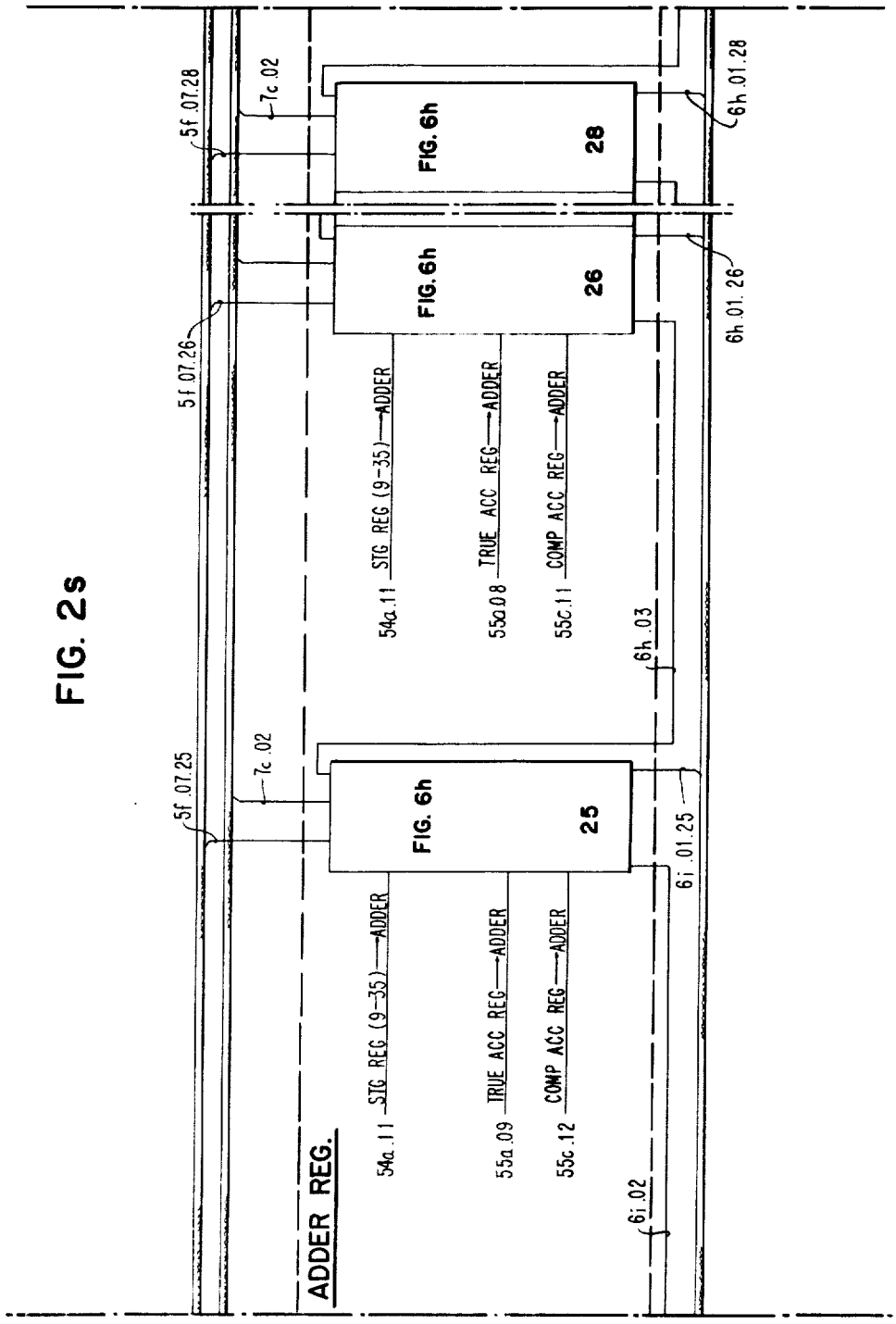

5f.07.28
7c.02
FIG. 6h
28
6h.01.28
FIG. 6h
26
6h.01.26
5f.07.26
54a.11 STG REG (9-35) → ADDER
55a.08 TRUE ACC REG → ADDER
55c.11 COMP ACC REG → ADDER
6h.03
5f.07.25
7c.02
FIG. 6h
25
6i.01.25
54a.11 STG REG (9-35) → ADDER
55a.09 TRUE ACC REG → ADDER
55c.12 COMP ACC REG → ADDER
6i.02
ADDER REG.

FIG. 2t

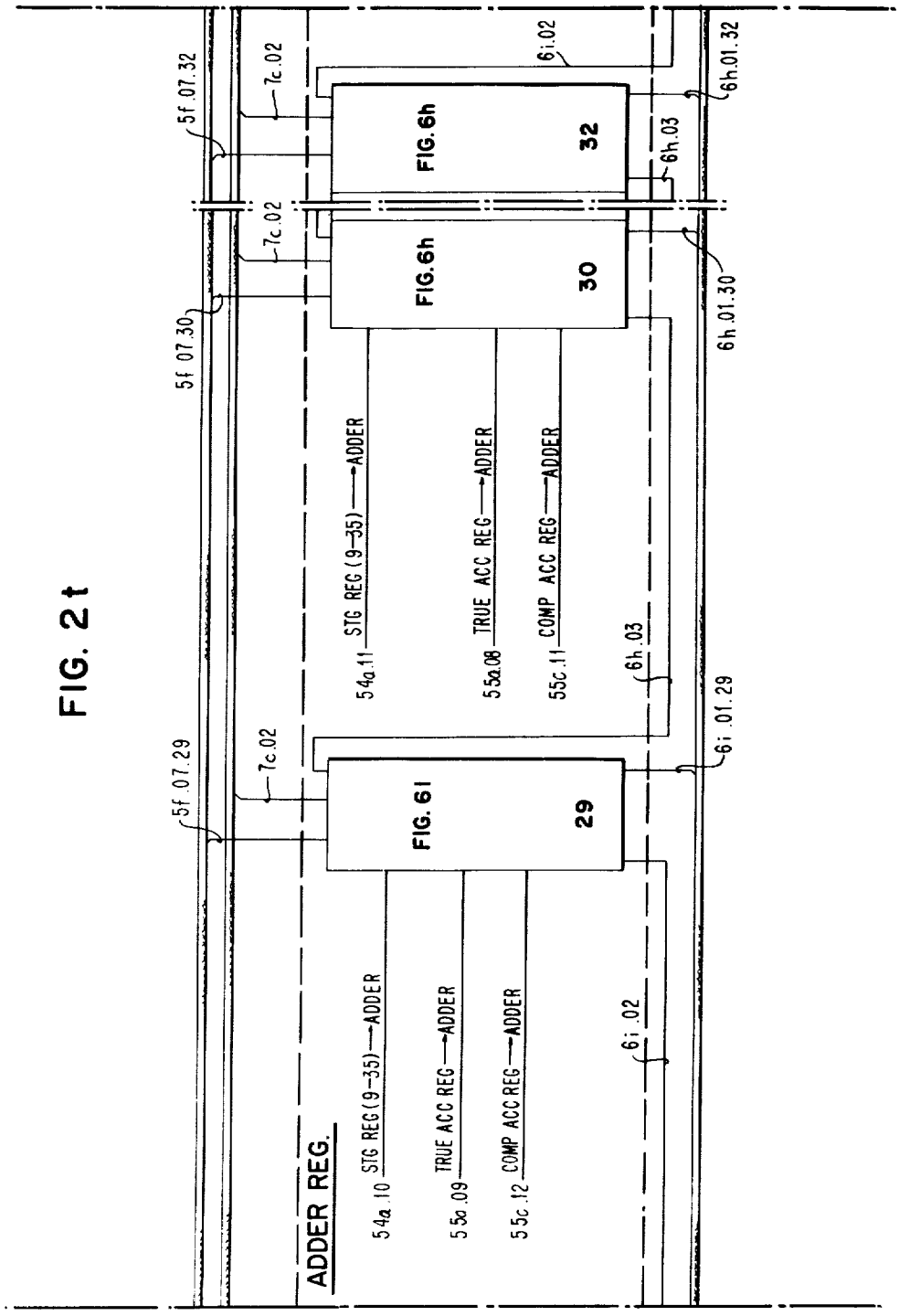
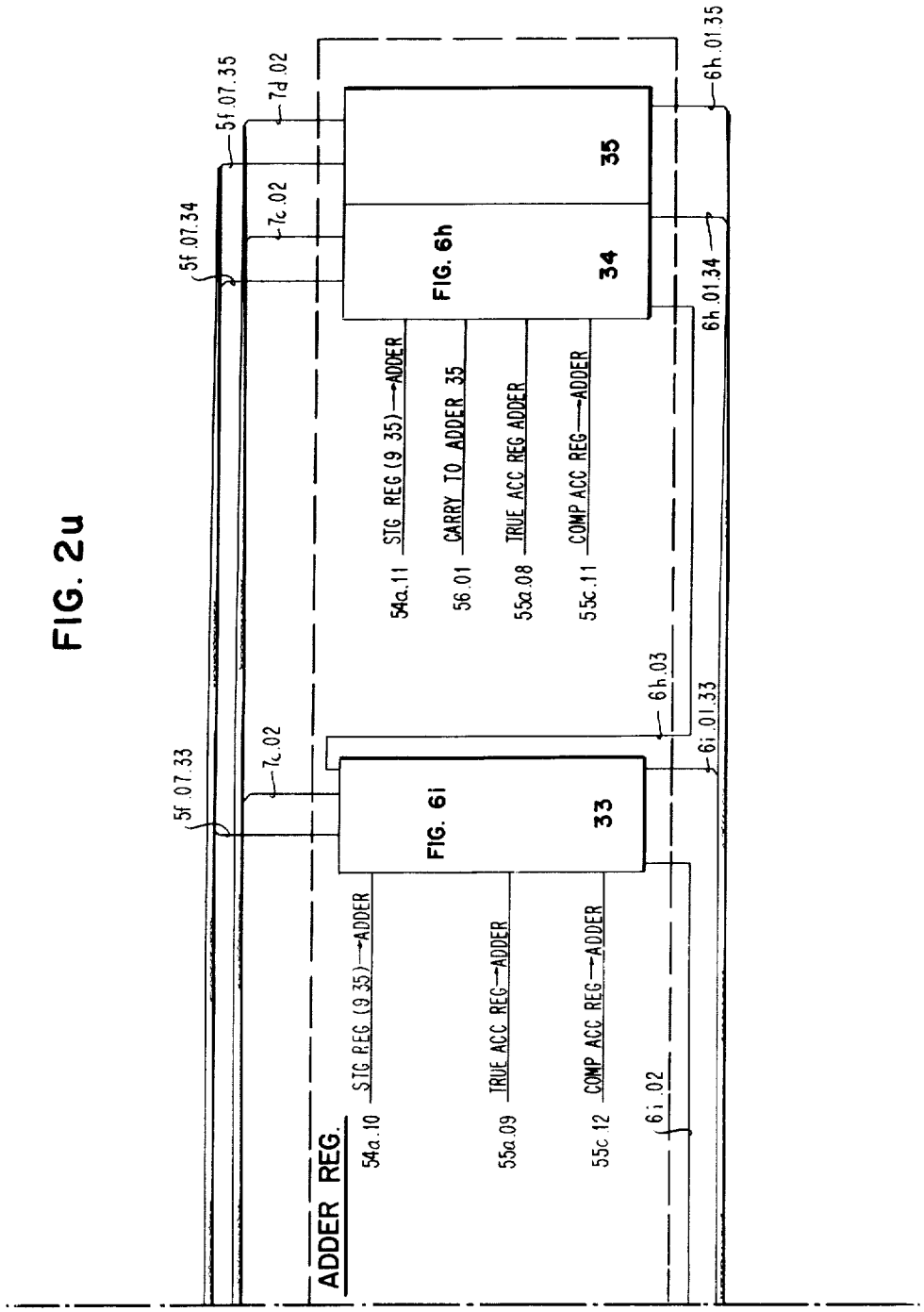

5f.07.32
7c.02
6i.02
6h.01.32
FIG.6h
32
6h.03
7c.02
FIG.6h
30
6h.01.30
5f.07.30
54a.11 STG REG (9-35) → ADDER
55a.08 TRUE ACC REG → ADDER
55c.11 COMP ACC REG → ADDER
6h.03
6i.01.29
7c.02
5f.07.29
FIG. 6I
29
ADDER REG.
54a.10 STG REG (9-35) → ADDER
55a.09 TRUE ACC REG → ADDER
55c.12 COMP ACC REG → ADDER
6i.02

FIG. 2u


5f.07.35
7d.02
6h.01.35
5f.07.34
7c.02
FIG. 6h
35
34
6h.01.34
54a.11 SIG REG (9 35)→ADDER
56.01 CARRY TO ADDER 35
55a.08 TRUE ACC REG ADDER
55c.11 COMP ACC REG→ADDER
6h.03
6i.01.33
5f.07.33
7c.02
FIG. 6i
33
ADDER REG.
54a.10 SIG REG (9 35)→ADDER
55a.09 TRUE ACC REG→ADDER
55c.12 COMP ACC REG→ADDER
6i.02

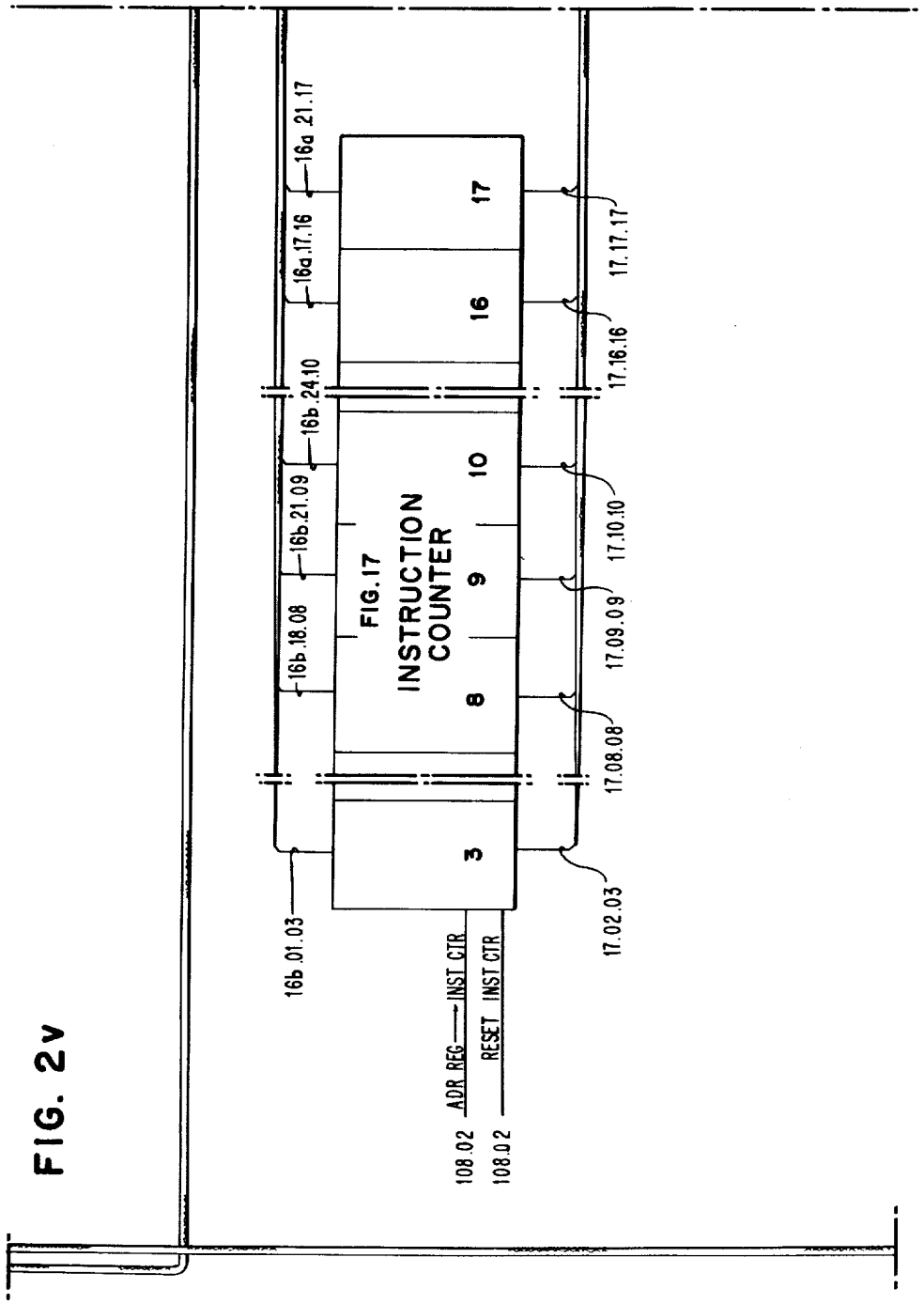

16a 21.17
16a.17.16
16b.24.10
16b.21.09
16b.18.08
16b.01.03
17
16
10
9
8
3
FIG. 17
INSTRUCTION
COUNTER
17.17.17
17.16.16
17.10.10
17.09.09
17.08.08
17.02.03
108.02 ADR REG — INST CTR
108.02 RESET INST CTR

FIG. 2v

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J. L. BROWN

INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

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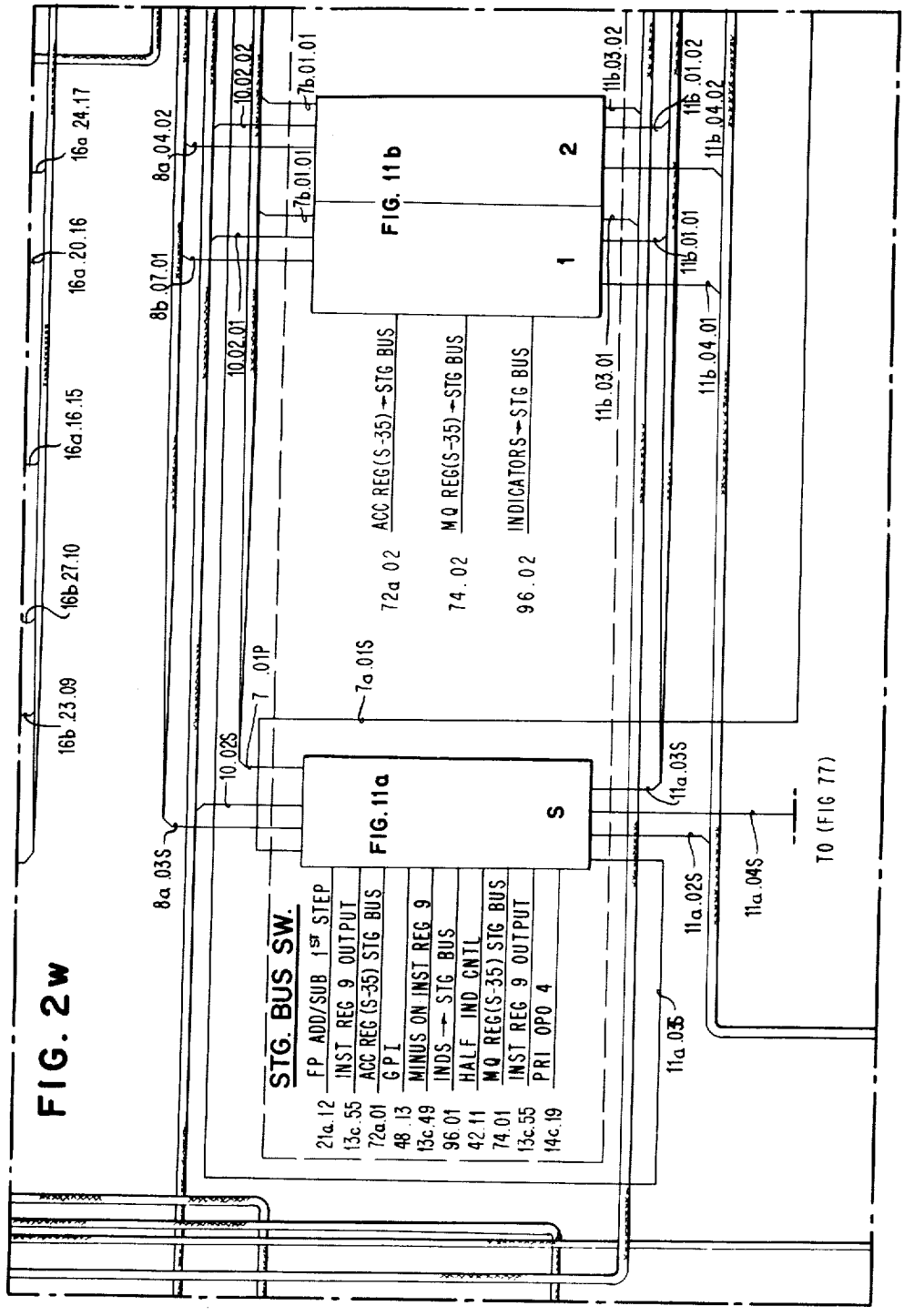
244 Sheets-Sheet 24



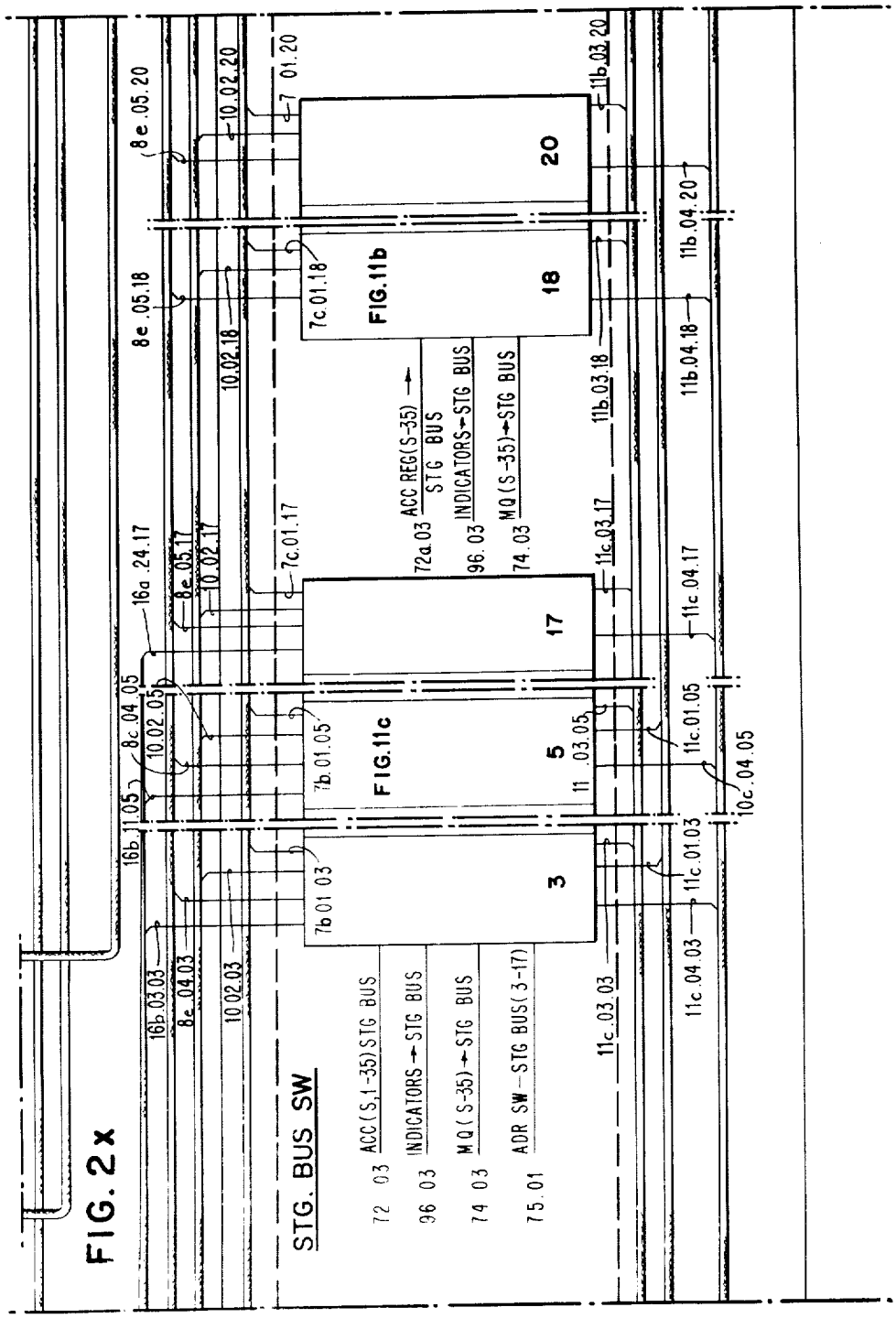


FIG. 2x
STG. BUS SW
72 03 ACC(S,1-35)STG BUS
96 03 INDICATORS→STG BUS
74 03 MQ(S-35)→STG BUS
75 01 ADR SW→STG BUS(3-17)
7b 01 03
7b 01.05
7c.01.17
7c.01.18
7 01.20
FIG.11c
FIG.11b
3
5
17
18
20
72a.03 ACC REG(S-35)→STG BUS
96. 03 INDICATORS→STG BUS
74. 03 MQ(S-35)→STG BUS
16b.11.05
16b.03.03
16a .24.17
8c .04 .05
8e .04.03
8e .05.17
8e .05.18
8e .05.20
10.02.03
10.02.05
10.02.17
10.02.18
10.02.20
11 .03.05
11c.03.03
11c.03.17
11b.03.18
11b.03.20
11c.01.03
11c.01.05
11c.04.03
11c.04.17
11b.04.18
11b.04.20
10c.04.05

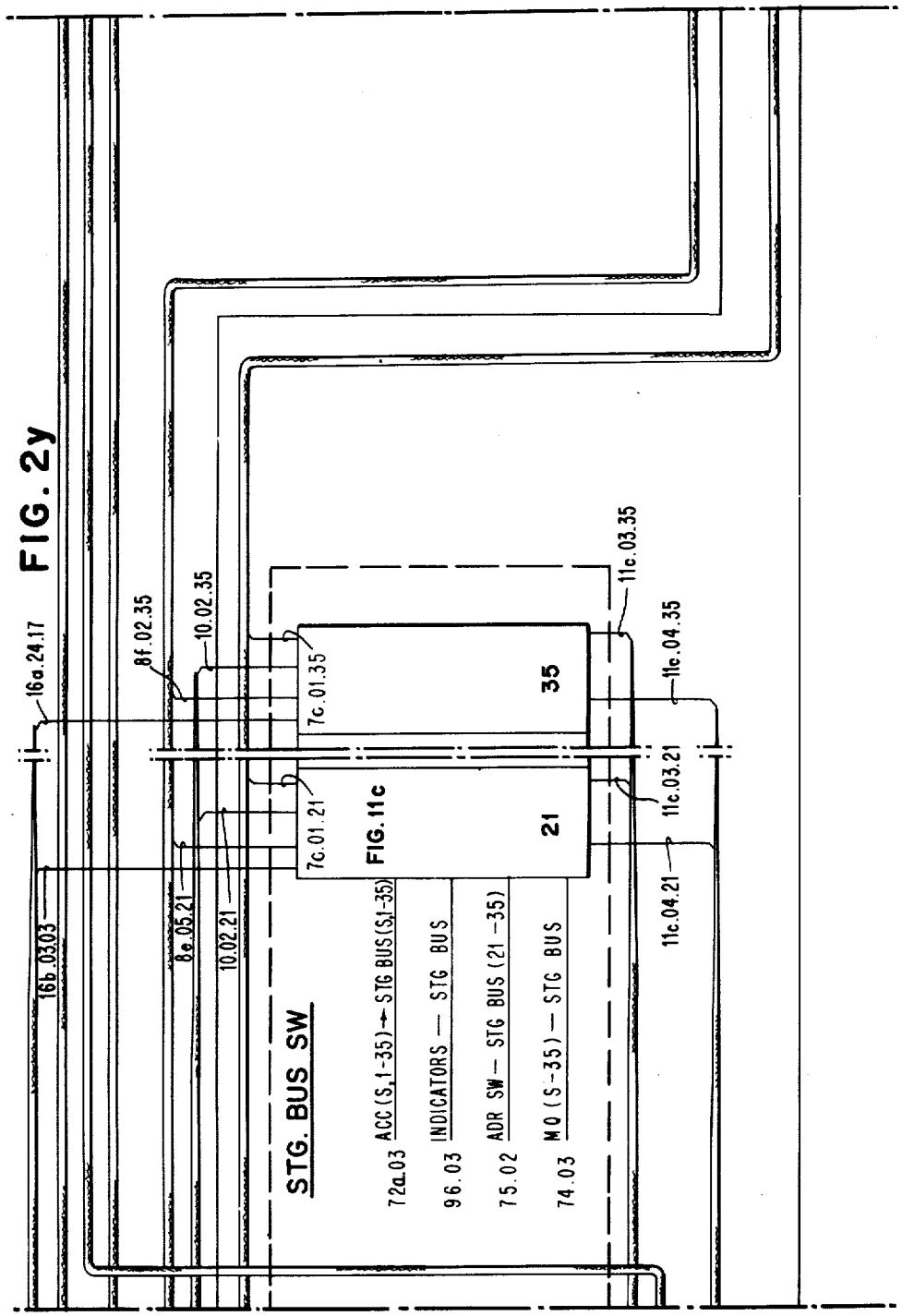


FIG. 2y
16a.24.17
8f.02.35
10.02.35
11c.03.35
11c.04.35
7c.01.35
35
7c.01.21
FIG. 11c
21
11c.03.21
11c.04.21
16b.03.03
8e.05.21
10.02.21
STG. BUS SW
72a.03 ACC (S,1-35) → STG BUS (S,1-35)
96.03 INDICATORS — STG BUS
75.02 ADR SW — STG BUS (21-35)
74.03 MQ (S-35) — STG BUS

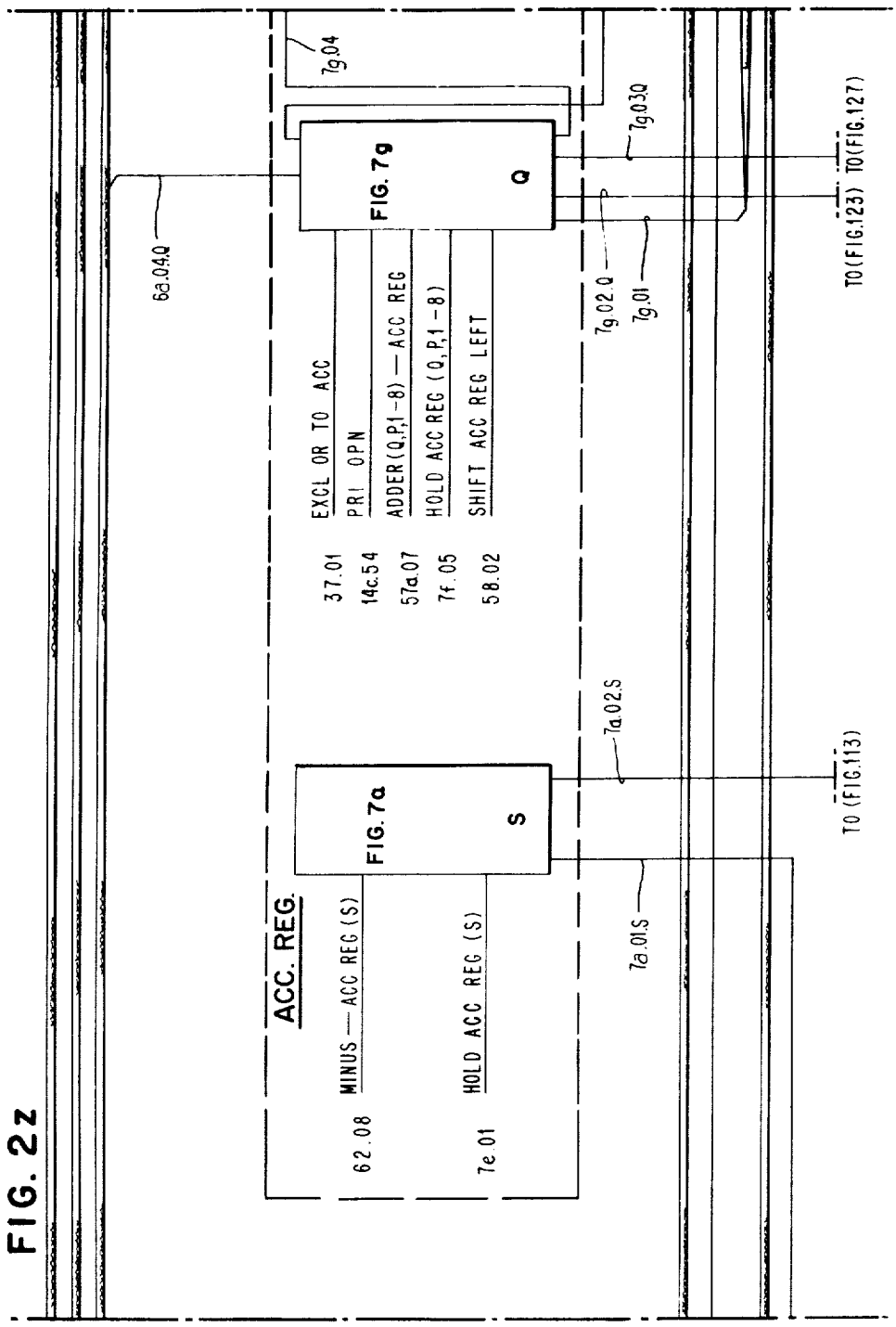


FIG. 2z
ACC. REG.
62.08 MINUS — ACC REG (S)
7e.01 HOLD ACC REG (S)
FIG. 7a
S
37.01 EXCL OR TO ACC
14c.54 PRI OPN
57a.07 ADDER (Q,P,1-8) — ACC REG
7f.05 HOLD ACC REG (Q,P,1-8)
58.02 SHIFT ACC REG LEFT
FIG. 7g
Q
6a.04Q
7g.04
7g.03Q
7g.02Q
7g.01
7a.02S
7a.01S
TO (FIG.113)
TO (FIG.123)
TO (FIG.127)

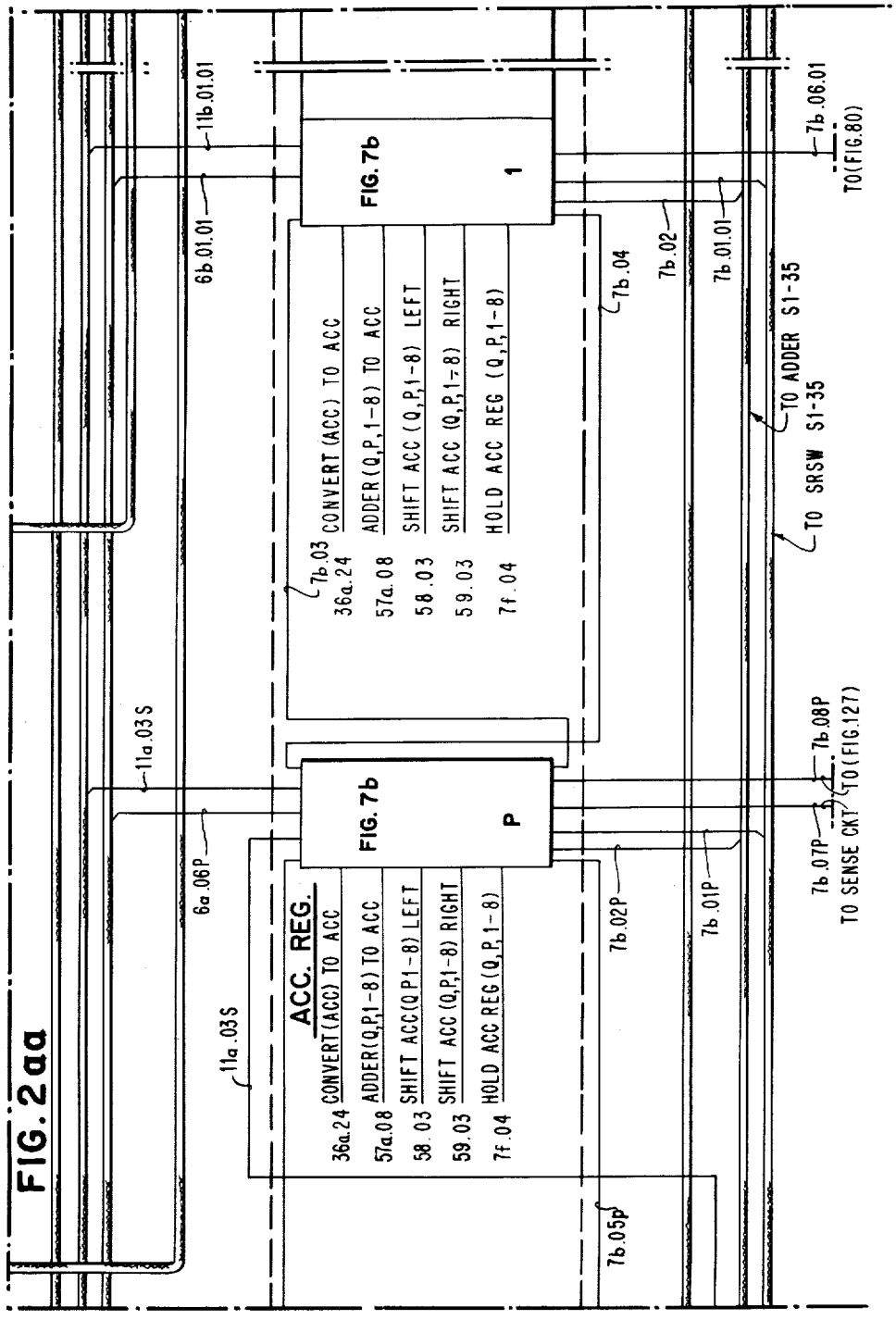


FIG. 2aa
ACC. REG.
CONVERT (ACC) TO ACC
ADDER (Q,P,1-8) TO ACC
SHIFT ACC (Q P1-8) LEFT
SHIFT ACC (Q,P,1-8) RIGHT
HOLD ACC REG (Q,P,1-8)
36a.24
57a.08
58.03
59.03
7f.04
FIG. 7b
P
FIG. 7b
1
CONVERT (ACC) TO ACC
ADDER (Q,P,1-8) TO ACC
SHIFT ACC (Q,P,1-8) LEFT
SHIFT ACC (Q,P,1-8) RIGHT
HOLD ACC REG (Q,P,1-8)
7b.03
36a.24
57a.08
58.03
59.03
7f.04
11a.03S
6a.06P
11a.03S
6b.01.01
11b.01.01
7b.05P
7b.02P
7b.01P
7b.04
7b.02
7b.01.01
7b.06.01
TO (FIG.80)
TO ADDER S1-35
TO SRSW S1-35
7b.08P
TO (FIG.127)
7b.07P
TO SENSE CKT

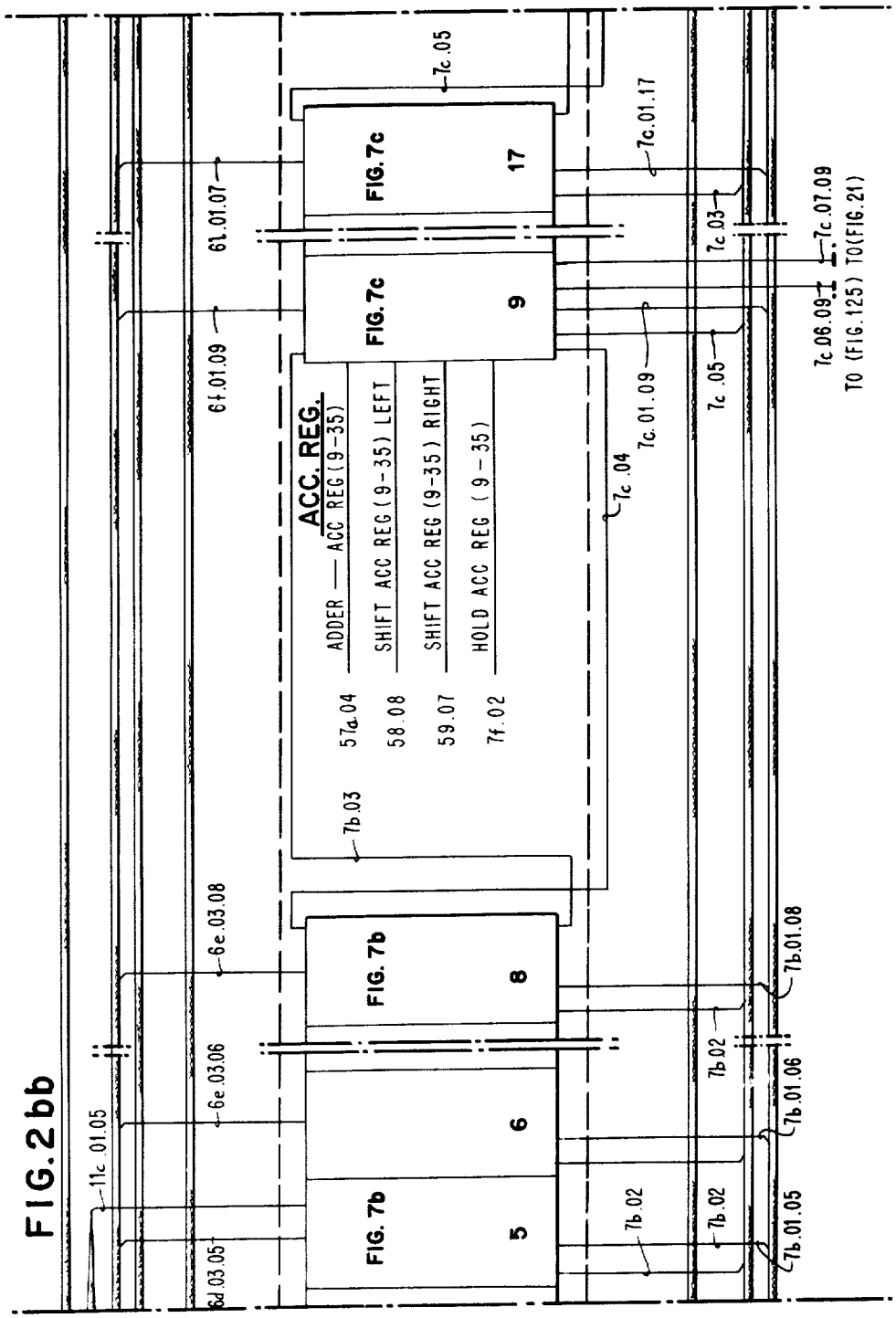


FIG. 2bb
FIG. 7b
5
6
8
FIG. 7c
9
17
ACC. REG.
ADDER — ACC REG (9-35)
SHIFT ACC REG (9-35) LEFT
SHIFT ACC REG (9-35) RIGHT
HOLD ACC REG (9-35)
57a.04
58.08
59.07
7f.02
7b.03
7c.04
7c.05
7c.01.09
7c.01.17
7c.03
7c.07.09
7c.06.09
TO (FIG.125) TO(FIG.21)
61.01.07
61.01.09
6e.03.08
6e.03.06
6d.03.05
11c.01.05
7b.01.08
7b.01.06
7b.01.05
7b.02

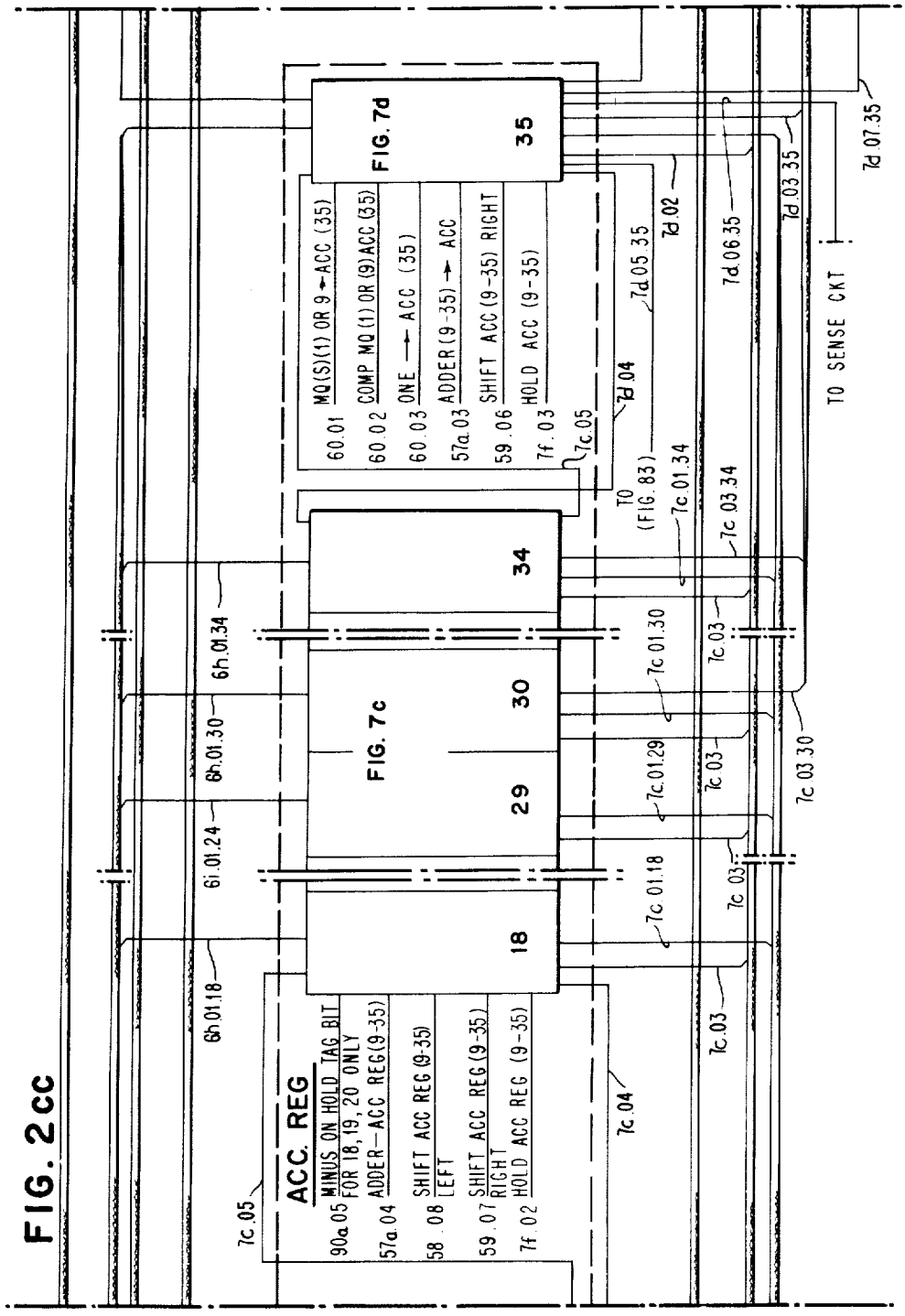
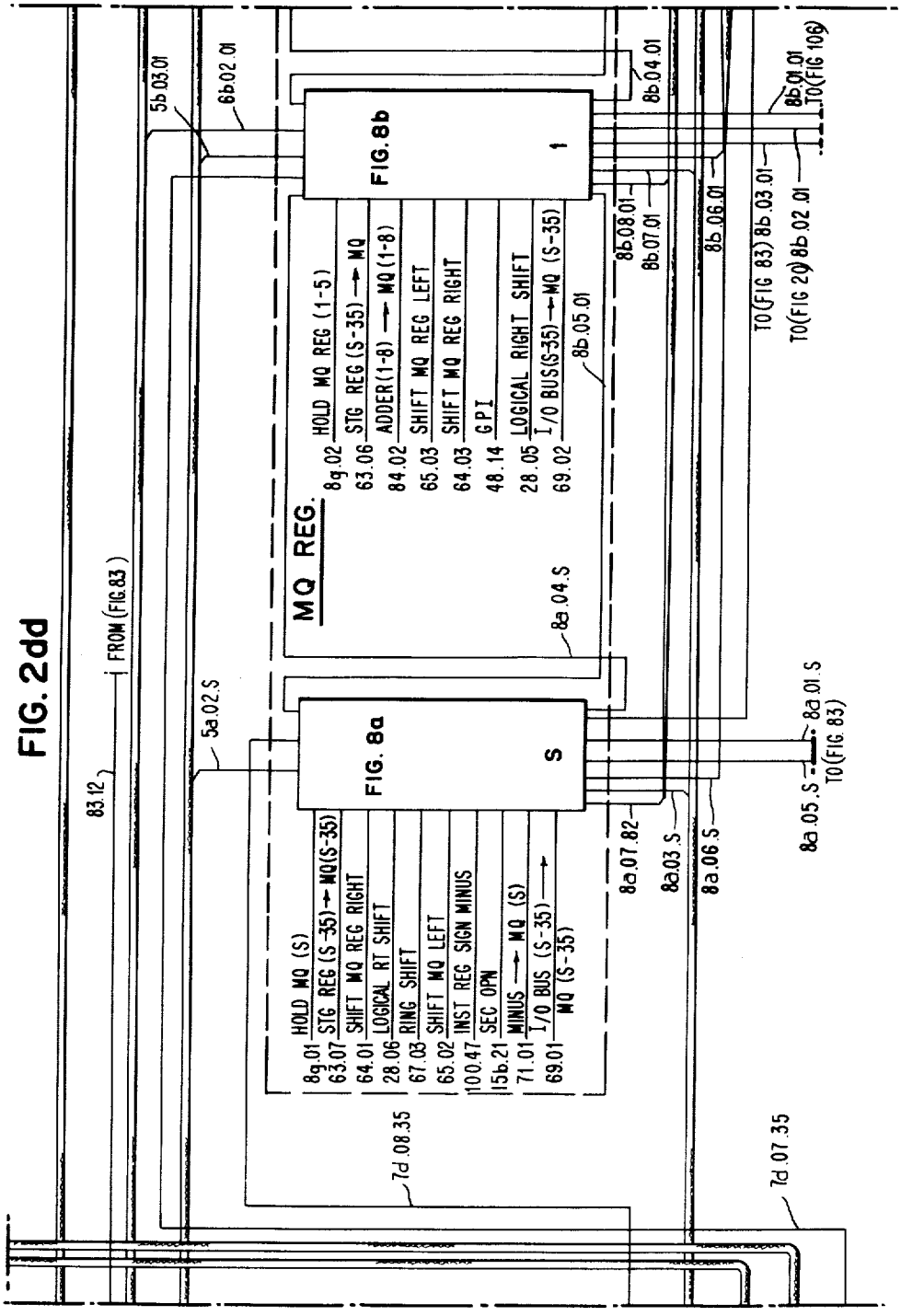


FIG. 2cc
ACC. REG
MINUS ON HOLD TAG BIT FOR 18, 19, 20 ONLY
90a 05
ADDER—ACC REG (9-35)
57a 04
SHIFT ACC REG (9-35) LEFT
58 08
SHIFT ACC REG (9-35) RIGHT
59 07
HOLD ACC REG (9-35)
7f 02
7c 05
6h 01 18
6i 01 24
6h 01 30
6h 01 34
FIG. 7c
18
29
30
34
FIG. 7d
35
MQ(S)(1) OR 9 → ACC (35)
60 01
COMP MQ (1) OR (9) ACC (35)
60 02
ONE → ACC (35)
60 03
ADDER (9-35) → ACC
57a 03
SHIFT ACC (9-35) RIGHT
59 06
HOLD ACC (9-35)
7f 03
7c 05
7d 04
7d 05 35
7d 02
TO (FIG. 83)
7c 01 34
7c 03 34
7c 01 30
7c 01 29
7c 01 18
7c 03
7c 04
7d 06 35
7d 03 35
7d 07 35
7c 03 30
TO SENSE CKT

FIG. 2dd


FROM (FIG. 83)
83.12
5a.02 S
5b.03.01
6b.02.01
FIG. 8b
1
FIG. 8a
S
MQ REG.
8g.02 HOLD MQ REG (1-5)
63.06 STG REG (S-35) → MQ
84.02 ADDER(1-8) → MQ (1-8)
65.03 SHIFT MQ REG LEFT
64.03 SHIFT MQ REG RIGHT
48.14 GPI
28.05 LOGICAL RIGHT SHIFT
69.02 I/O BUS(S-35) → MQ (S-35)
8b.05.01
8a.04.S
8g.01 HOLD MQ (S)
63.07 STG REG (S-35) → MQ(S-35)
64.01 SHIFT MQ REG RIGHT
28.06 LOGICAL RT SHIFT
67.03 RING SHIFT
65.02 SHIFT MQ LEFT
100.47 INST REG SIGN MINUS
15b.21 SEC OPN
71.01 MINUS → MQ (S)
69.01 I/O BUS (S-35) → MQ (S-35)
7d.08.35
8b.04.01
8b.01.01
TO(FIG 106)
8b.08.01
8b.07.01
8b.06.01
TO(FIG 83) 8b.03.01
TO(FIG 20) 8b.02.01
8a.01.S
TO(FIG 83)
8a.05.S
8a.07.82
8a.03.S
8a.06.S
7d.07.35

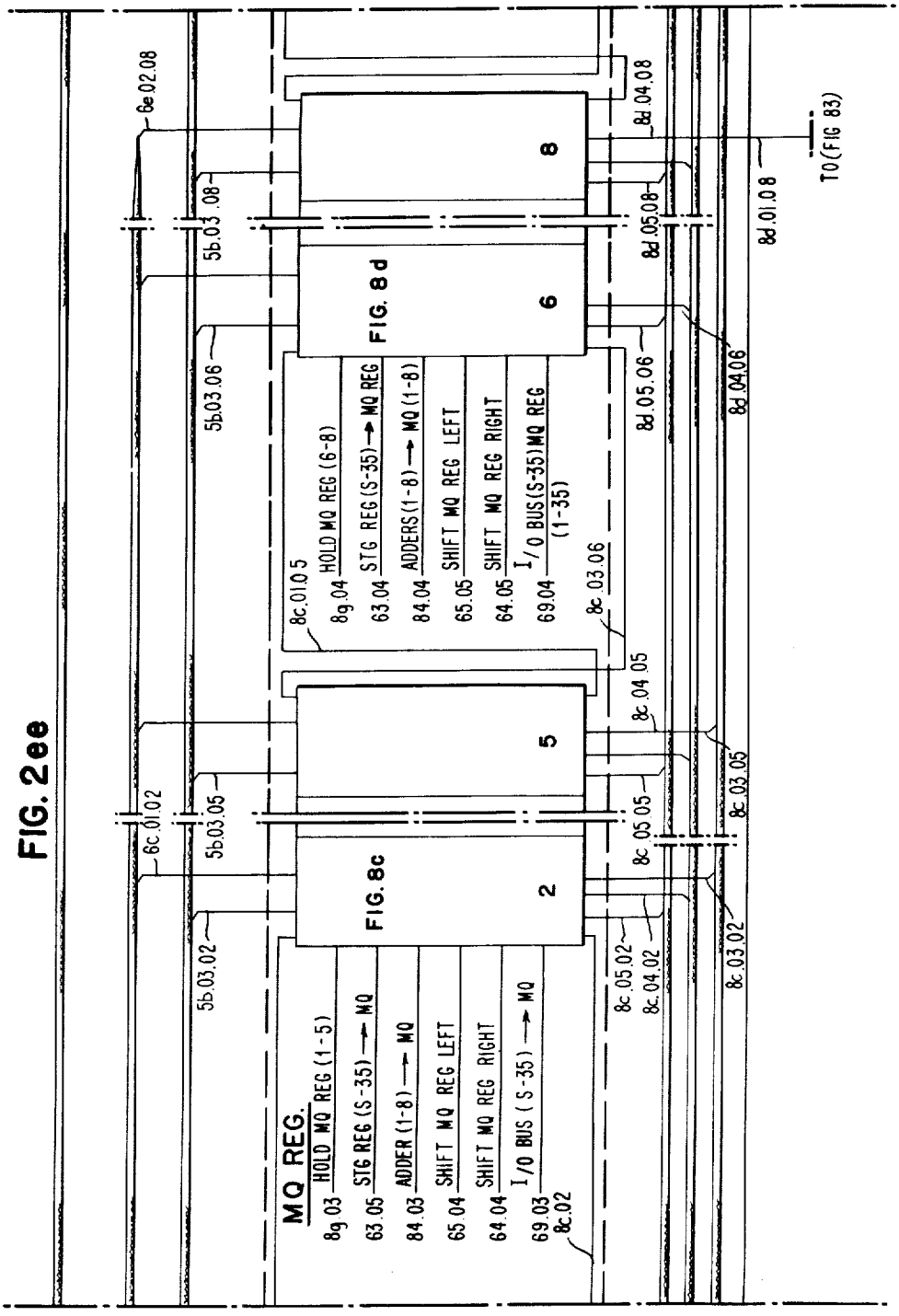


FIG. 2ee
MQ REG.
8g 03 HOLD MQ REG (1-5)
63 05 STG REG (S-35) → MQ
84 03 ADDER (1-8) → MQ
65 04 SHIFT MQ REG LEFT
64 04 SHIFT MQ REG RIGHT
69 03 I/O BUS (S-35) → MQ
8c.02
FIG. 8c
2
5
FIG. 8d
6
8
8g 04 HOLD MQ REG (6-8)
63 04 STG REG (S-35) → MQ REG
84 04 ADDERS (1-8) → MQ (1-8)
65 05 SHIFT MQ REG LEFT
64 05 SHIFT MQ REG RIGHT
69 04 I/O BUS (S-35) MQ REG (1-35)
8c.01.05
8c.03.06
8c.04.05
8c.05.05
8c.03.05
8c.05.02
8c.04.02
8c.03.02
6c.01.02
5b.03.05
5b.03.02
5b.03.06
5b.03.08
8e.02.08
8d.04.08
8d.05.08
8d.01.08
8d.05.06
8d.04.06
TO (FIG 83)

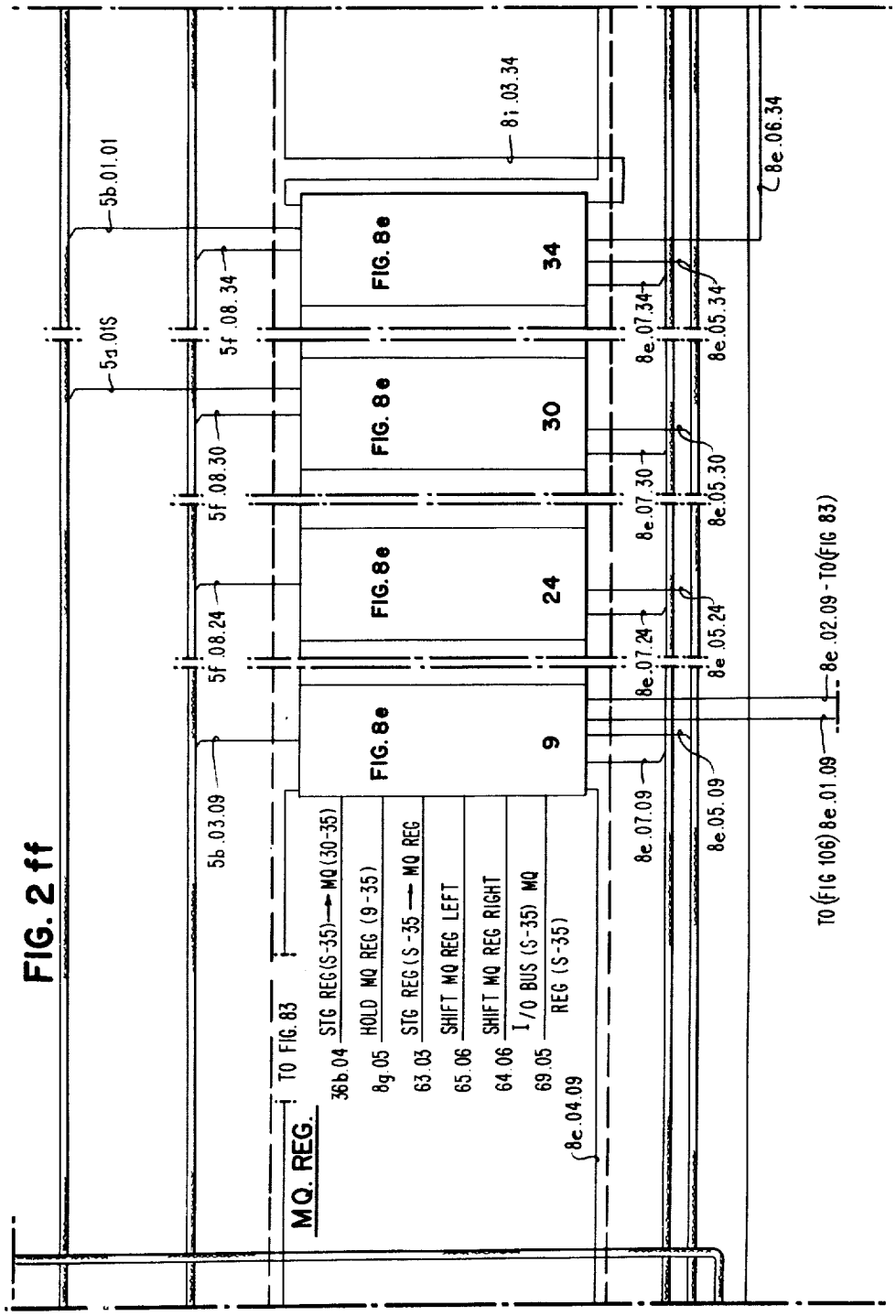
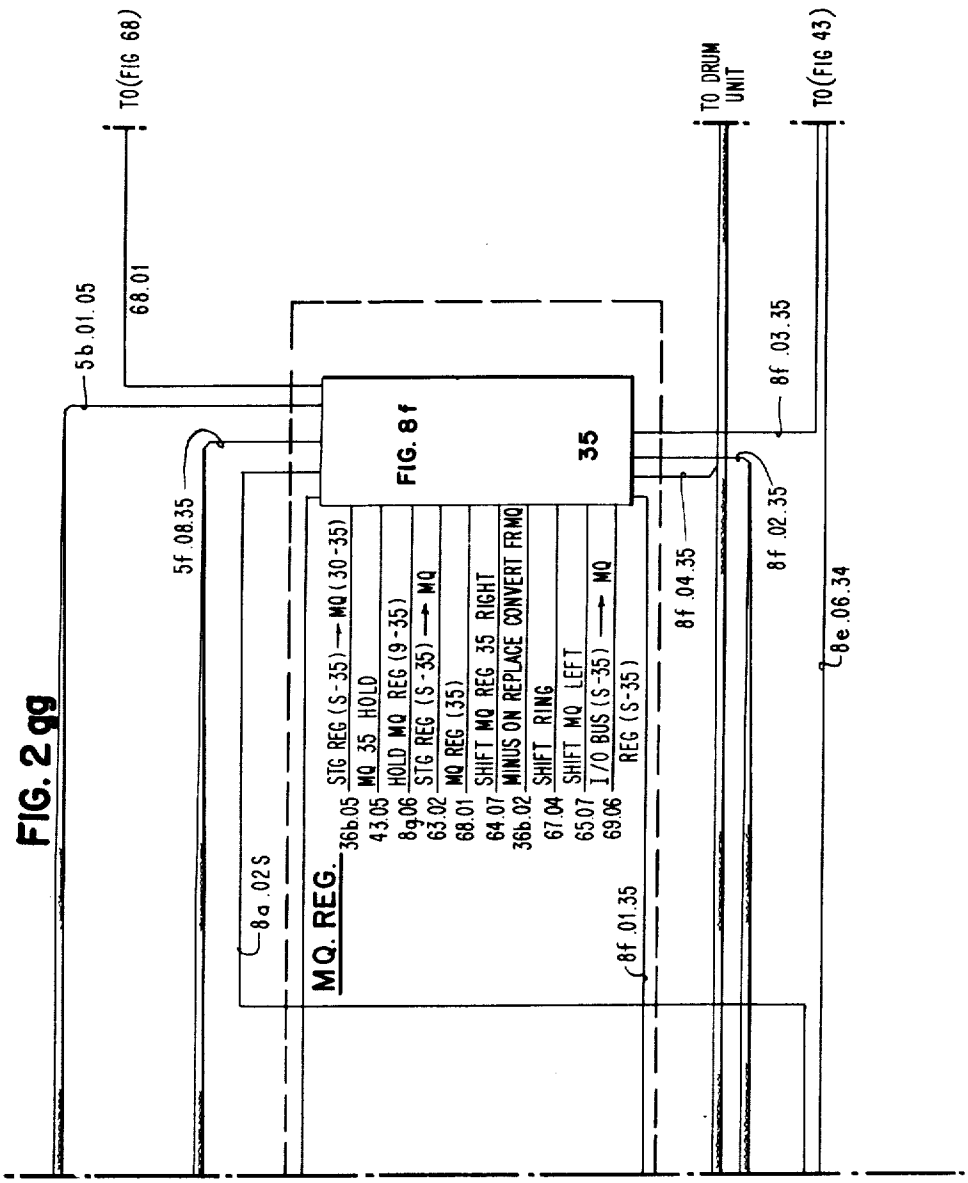


FIG. 2ff
MQ. REG.
TO FIG. 83
36b.04 STG REG(S-35)→MQ(30-35)
8g.05 HOLD MQ REG (9-35)
63.03 STG REG(S-35→MQ REG
65.06 SHIFT MQ REG LEFT
64.06 SHIFT MQ REG RIGHT
69.05 I/O BUS (S-35) MQ REG (S-35)
8e.04.09
5b.03.09
5f.08.24
5f.08.30
5a.01S
5b.01.01
5f.08.34
8i.03.34
FIG. 8e
9
24
30
34
8e.07.09
8e.07.24
8e.07.30
8e.07.34
8e.05.09
8e.05.24
8e.05.30
8e.05.34
8e.06.34
8e.02.09 - TO(FIG 83)
TO(FIG 106) 8e.01.09

FIG. 2gg


TO(FIG 68)
68.01
5b.01.05
TO DRUM UNIT
TO(FIG 43)
8f.03.35
FIG. 8f
35
5f.08.35
8f.02.35
8f.04.35
8e.06.34
MQ. REG.
8a.02S
8f.01.35
36b.05 STG REG (S-35) → MQ (30-35)
MQ 35 HOLD
43.05 HOLD MQ REG (9-35)
8g.06 STG REG (S-35) → MQ
63.02 MQ REG (35)
68.01 SHIFT MQ REG 35 RIGHT
64.07 MINUS ON REPLACE CONVERT FR MQ
36b.02 SHIFT RING
67.04 SHIFT MQ LEFT
65.07 I/O BUS (S-35) → MQ
69.06 REG (S-35)

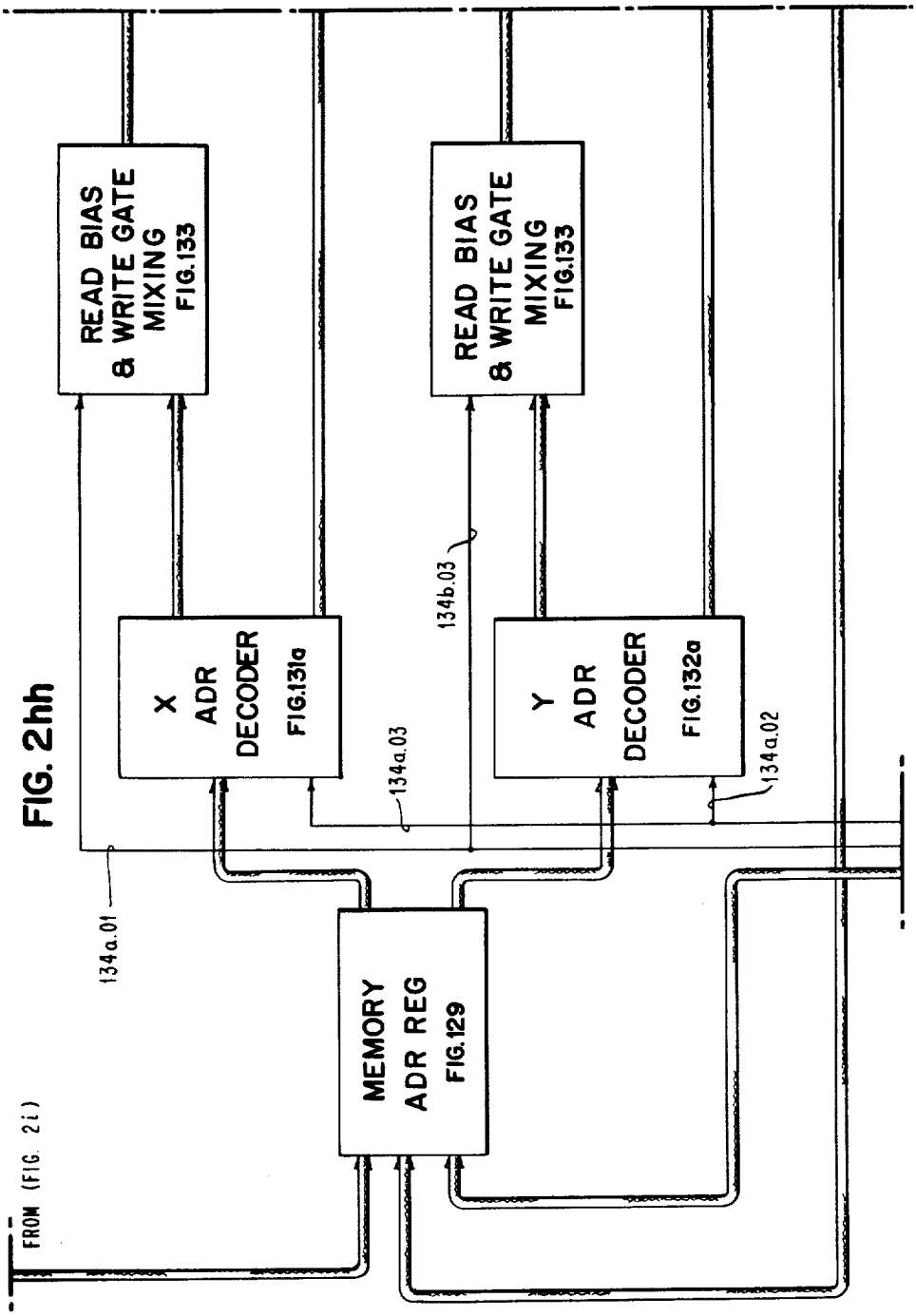

READ BIAS & WRITE GATE MIXING FIG.133
READ BIAS & WRITE GATE MIXING FIG.133
X ADR DECODER FIG.131a
Y ADR DECODER FIG.132a
MEMORY ADR REG FIG.129
134a.01
134a.03
134b.03
134a.02
FROM (FIG. 2i)

FIG. 2hh

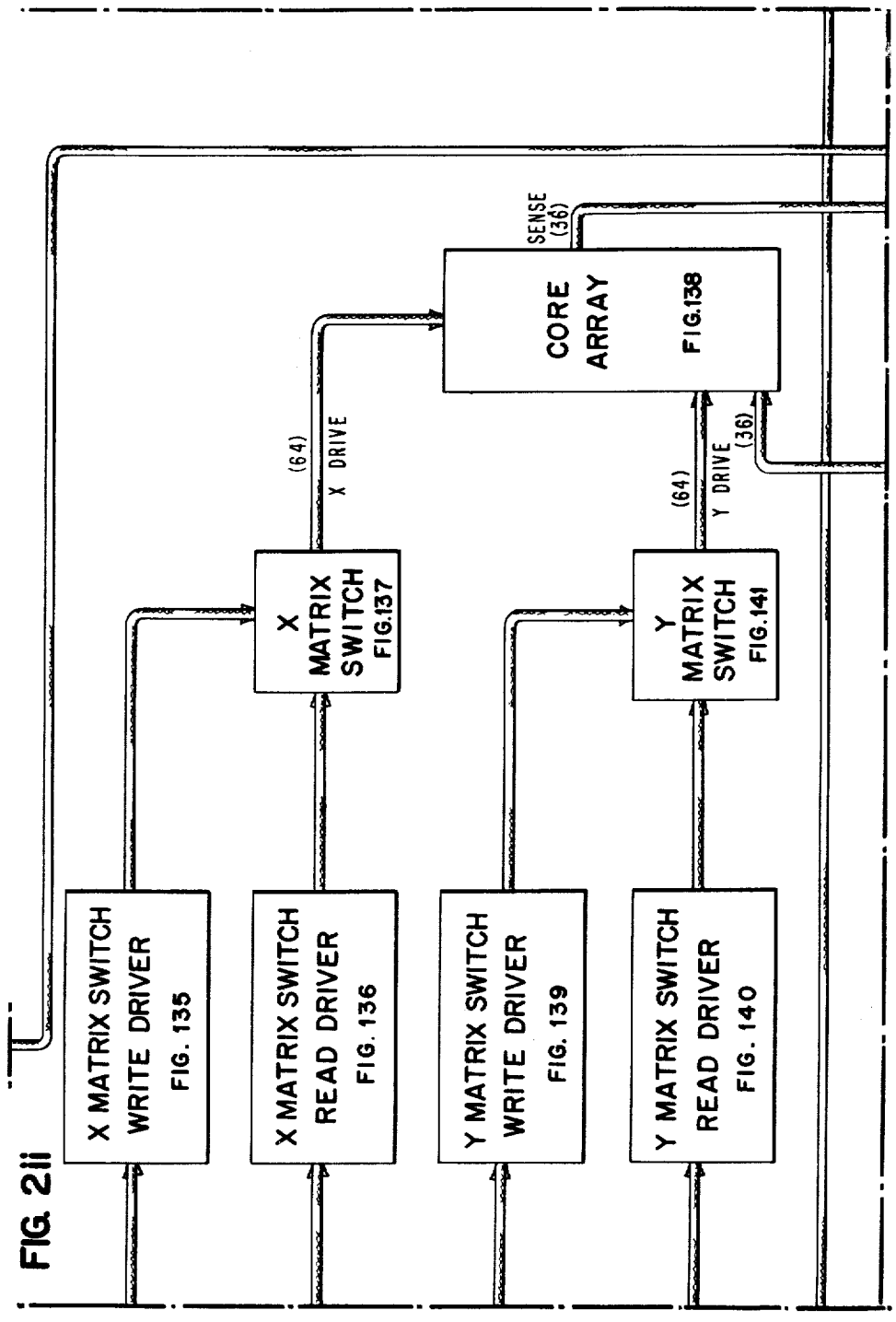

SENSE (36)
CORE ARRAY FIG.138
(64) X DRIVE
(64) Y DRIVE (36)
X MATRIX SWITCH FIG.137
Y MATRIX SWITCH FIG.141
X MATRIX SWITCH WRITE DRIVER FIG. 135
X MATRIX SWITCH READ DRIVER FIG. 136
Y MATRIX SWITCH WRITE DRIVER FIG. 139
Y MATRIX SWITCH READ DRIVER FIG. 140

FIG. 2ii

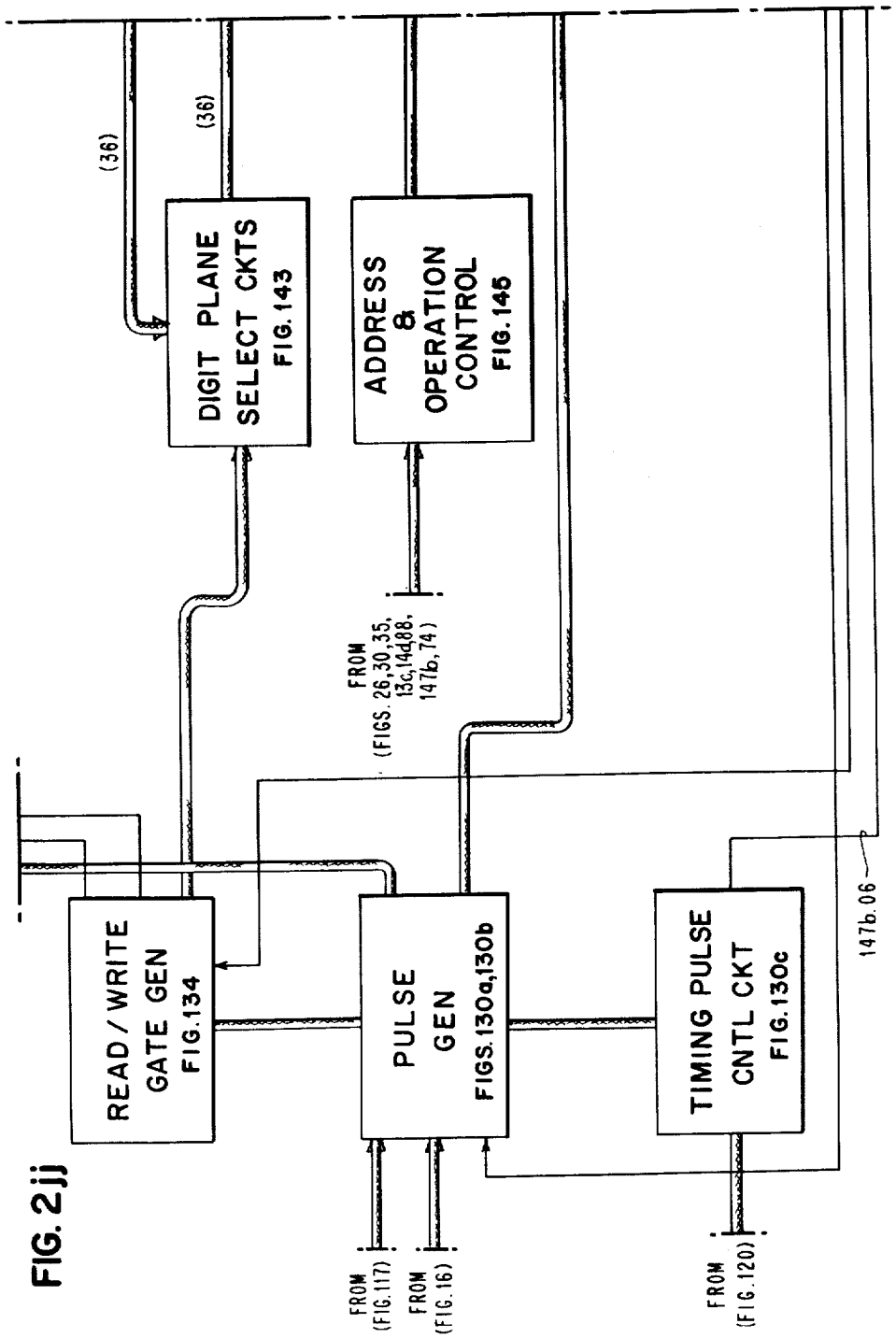

(36)
(36)
DIGIT PLANE SELECT CKTS FIG. 143
ADDRESS & OPERATION CONTROL FIG. 145
FROM (FIGS. 26,30,35, 13c,144,88, 147b,74)
READ / WRITE GATE GEN FIG. 134
PULSE GEN FIGS. 130a,130b
TIMING PULSE CNTL CKT FIG. 130c
147b.06
FROM (FIG. 117)
FROM (FIG. 16)
FROM (FIG. 120)

FIG. 2jj

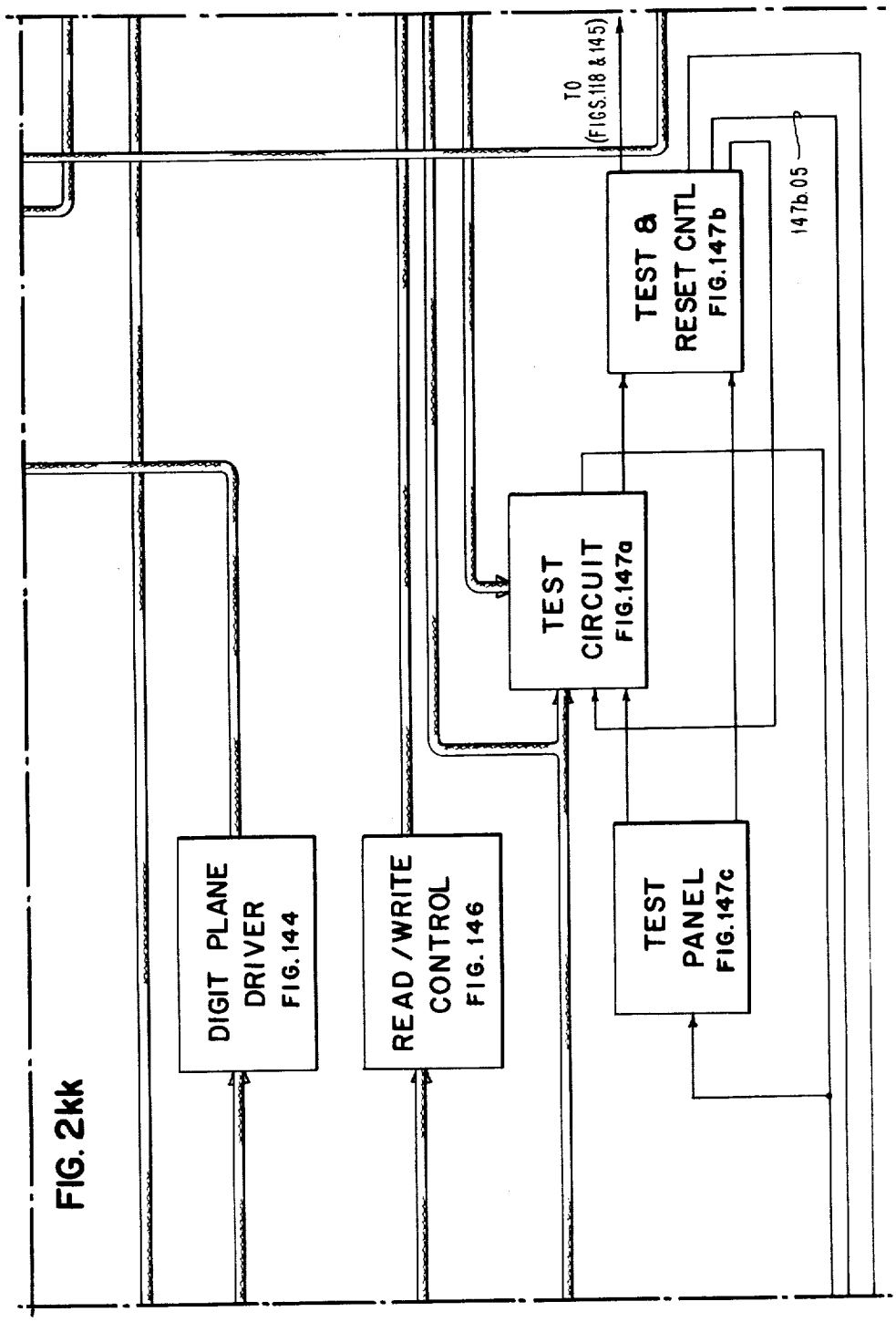

TO
(FIGS.118 & 145)
TEST & RESET CNTL FIG.147b
147b.05
TEST CIRCUIT FIG.147a
DIGIT PLANE DRIVER FIG.144
READ/WRITE CONTROL FIG.146
TEST PANEL FIG.147c

FIG. 2kk

FIG. 211

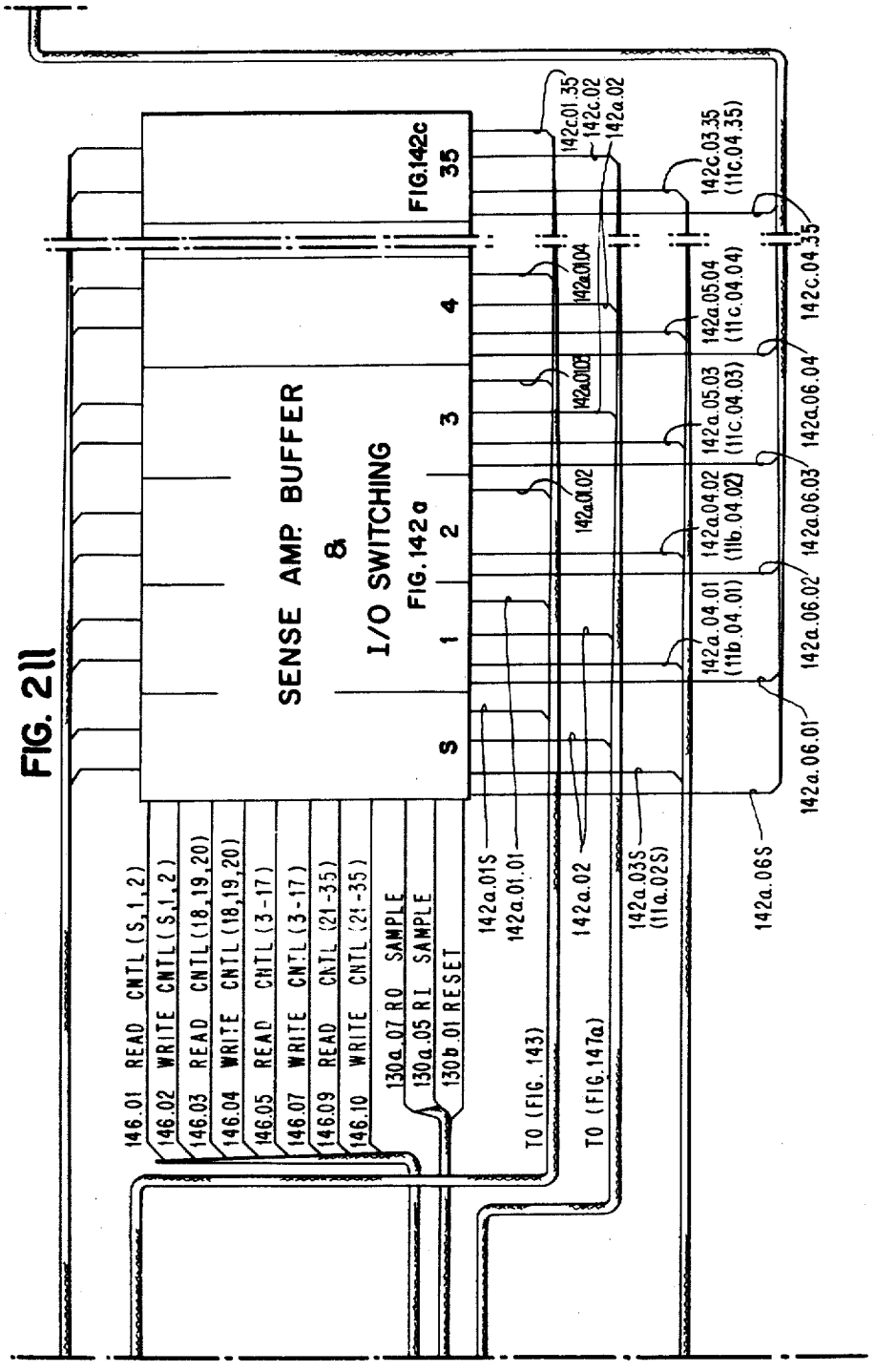

SENSE AMP. BUFFER & I/O SWITCHING
FIG. 142a
FIG. 142c 35
146.01 READ CNTL (S,1,2)
146.02 WRITE CNTL (S,1,2)
146.03 READ CNTL (18,19,20)
146.04 WRITE CNTL (18,19,20)
146.05 READ CNTL (3-17)
146.07 WRITE CNTL (3-17)
146.09 READ CNTL (21-35)
146.10 WRITE CNTL (21-35)
130a.07 RO SAMPLE
130a.05 RI SAMPLE
130b.01 RESET
TO (FIG. 143)
TO (FIG. 147a)
142a.01S
142a.01.01
142a.02
142a.03S (11a.02S)
142a.06S
142a.06.01
142a.06.02
142a.06.03
142a.06.04
142c.04.35
142a.04.01 (11b.04.01)
142a.04.02 (11b.04.02)
142a.05.03 (11c.04.03)
142a.05.04 (11c.04.04)
142c.03.35 (11c.04.35)
142c.01.35
142c.02
142a.02
142a.0104
142a.0103
142a.0102

FIG. 2mm

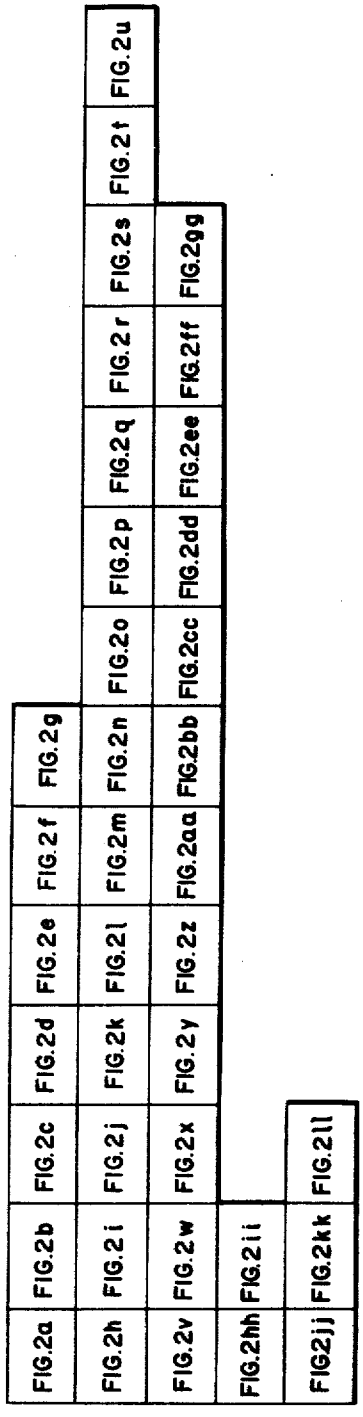
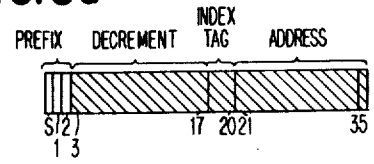


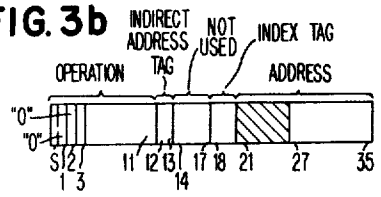
FIG.2a
FIG.2b
FIG.2c
FIG.2d
FIG.2e
FIG.2f
FIG.2g
FIG.2h
FIG.2i
FIG.2j
FIG.2k
FIG.2l
FIG.2m
FIG.2n
FIG.2o
FIG.2p
FIG.2q
FIG.2r
FIG.2s
FIG.2t
FIG.2u
FIG.2v
FIG.2w
FIG.2x
FIG.2y
FIG.2z
FIG.2aa
FIG.2bb
FIG.2cc
FIG.2dd
FIG.2ee
FIG.2ff
FIG.2gg
FIG.2hh
FIG.2ii
FIG.2jj
FIG.2kk
FIG.2ll

FIG. 3a



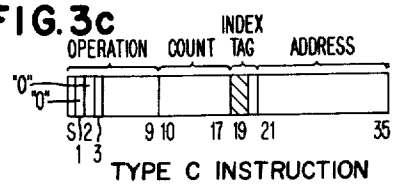
TYPE A INSTRUCTION

FIG. 3b



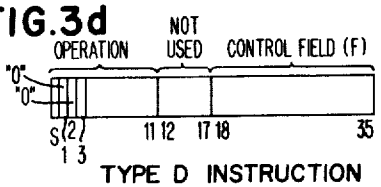
TYPE B INSTRUCTION

FIG. 3c



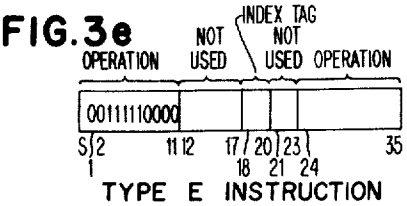
TYPE C INSTRUCTION

FIG. 3d



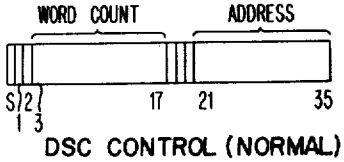
TYPE D INSTRUCTION

FIG. 3e



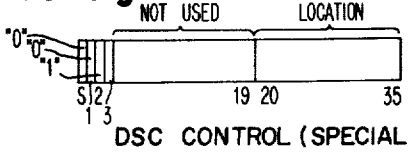
TYPE E INSTRUCTION

FIG. 3f



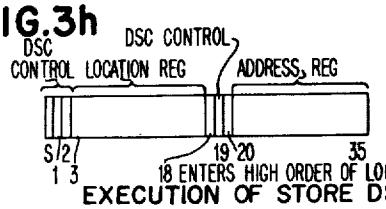
DSC CONTROL (NORMAL)

FIG. 3g



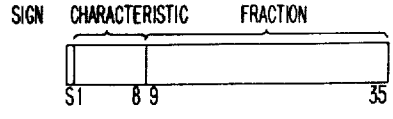
DSC CONTROL (SPECIAL)

FIG. 3h



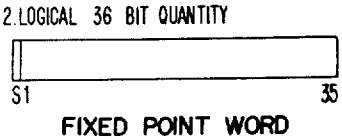
EXECUTION OF STORE DSC

FIG. 3i



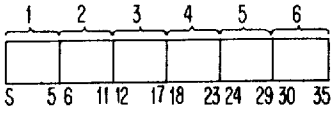
FLOATING POINT NUMBER

FIG. 3j



FIXED POINT WORD

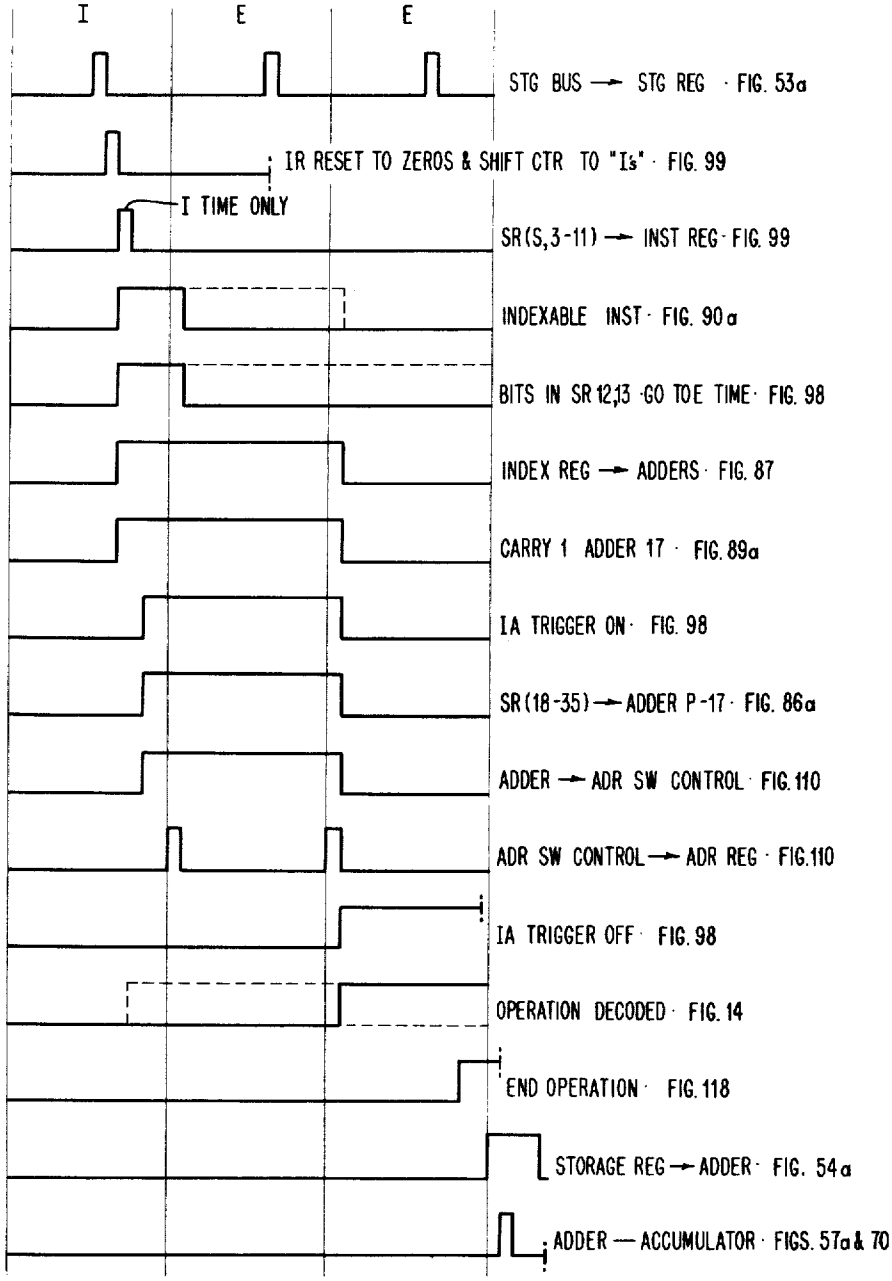
FIG. 3k



BCD 6 - CHARACTER WORD

CLA TO 500 WITH BITS IN 12 & 13, TAG IN 18,19 & 20

FIG. 4



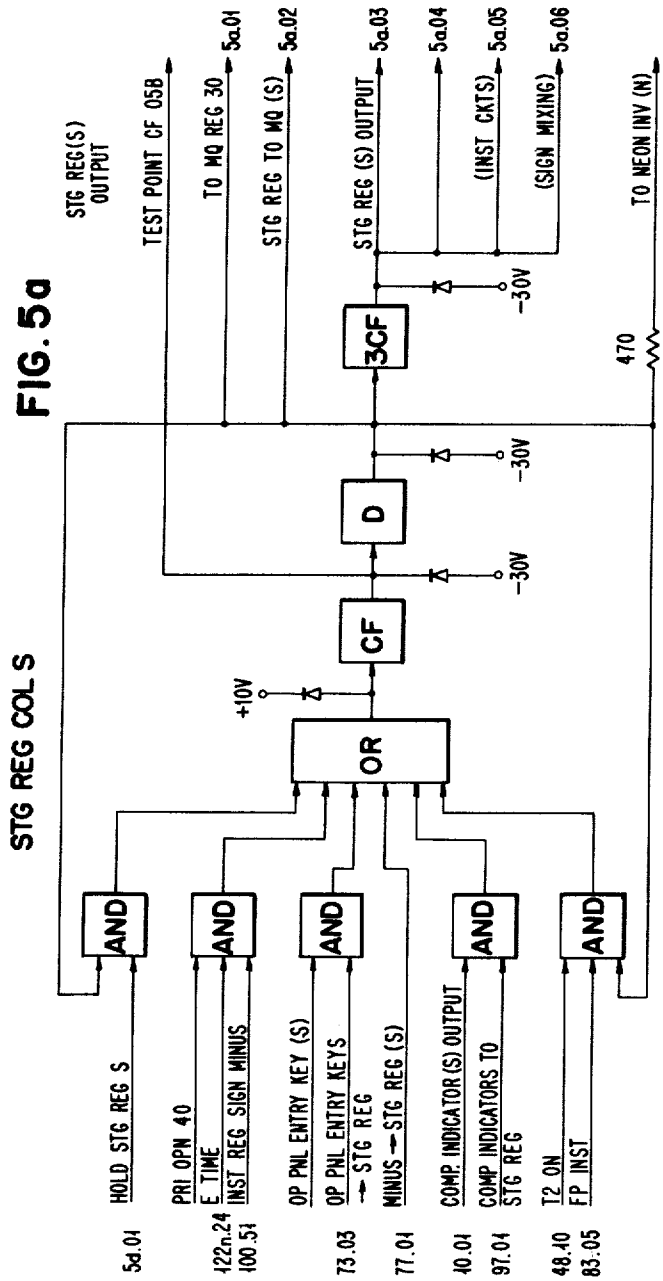

STG REG COL S
STG REG(S) OUTPUT
TEST POINT CF 05B
TO MQ REG 30
STG REG TO MQ (S)
STG REG (S) OUTPUT
(INST CKTS)
(SIGN MIXING)
TO MEON INV (N)
5a.01
5a.02
5a.03
5a.04
5a.05
5a.06
3CF
D
CF
OR
AND
+10V
-30V
470
HOLD STG REG S
PRI OPN 40
E TIME
INST REG SIGN MINUS
OP PNL ENTRY KEY (S)
OP PNL ENTRY KEYS → STG REG
MINUS → STG REG (S)
COMP. INDICATOR (S) OUTPUT
COMP INDICATORS TO STG REG
T2 ON
FP INST
5d.01
122n.24
100.51
73.03
77.01
40.01
97.01
48.10
83.05

FIG. 5a

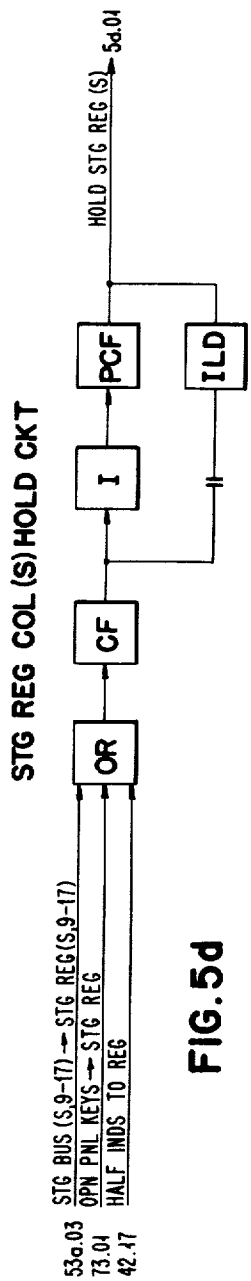

STG REG COL (S) HOLD CKT
HOLD STG REG (S)
5d.01
PCF
I
ILD
CF
OR
STG BUS (S,9-17) → STG REG (S,9-17)
OPN PNL KEYS → STG REG
HALF INDS TO REG
53a.03
73.01
42.17

FIG. 5d

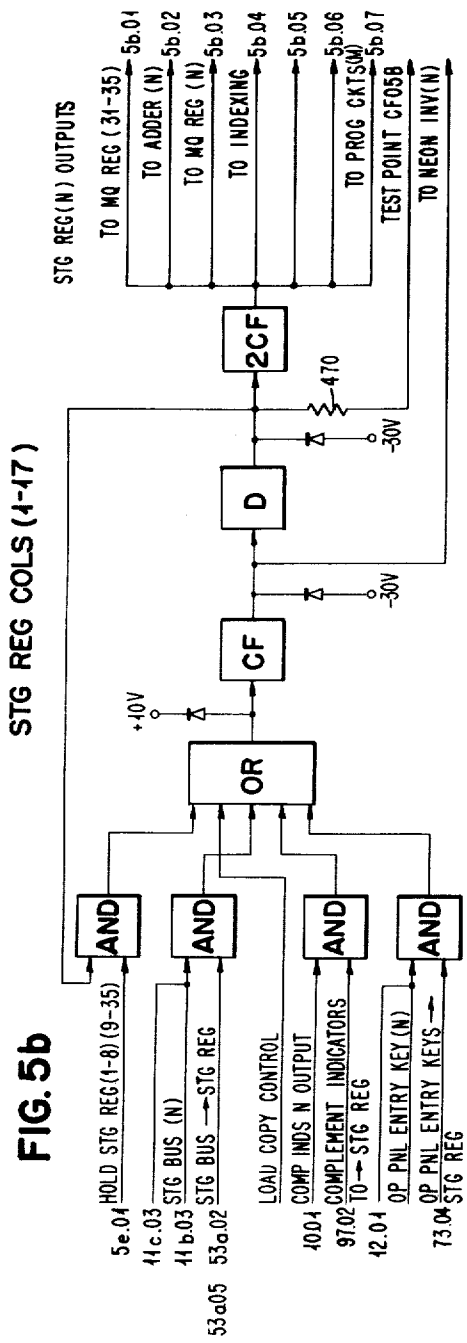

STG REG COLS (1-17)
STG REG(N) OUTPUTS
TO MQ REG (31-35) 5b.01
TO ADDER (N) 5b.02
TO MQ REG (N) 5b.03
TO INDEXING 5b.04
5b.05
TO PROG CKTS(M) 5b.06
TEST POINT CF05B 5b.07
TO NEON INV(N)
2CF
470
-30V
D
CF
+10V
OR
AND
5e.04 HOLD STG REG(1-8)(9-35)
41c.03 STG BUS (N)
41b.03 STG BUS →STG REG
53a05 53a02
LOAD COPY CONTROL
COMP INDS N OUTPUT 40.04
COMPLEMENT INDICATORS 97.02
TO→ STG REG
OP PNL ENTRY KEY(N) 12.04
OP PNL ENTRY KEYS→ STG REG 73.04

FIG. 5b

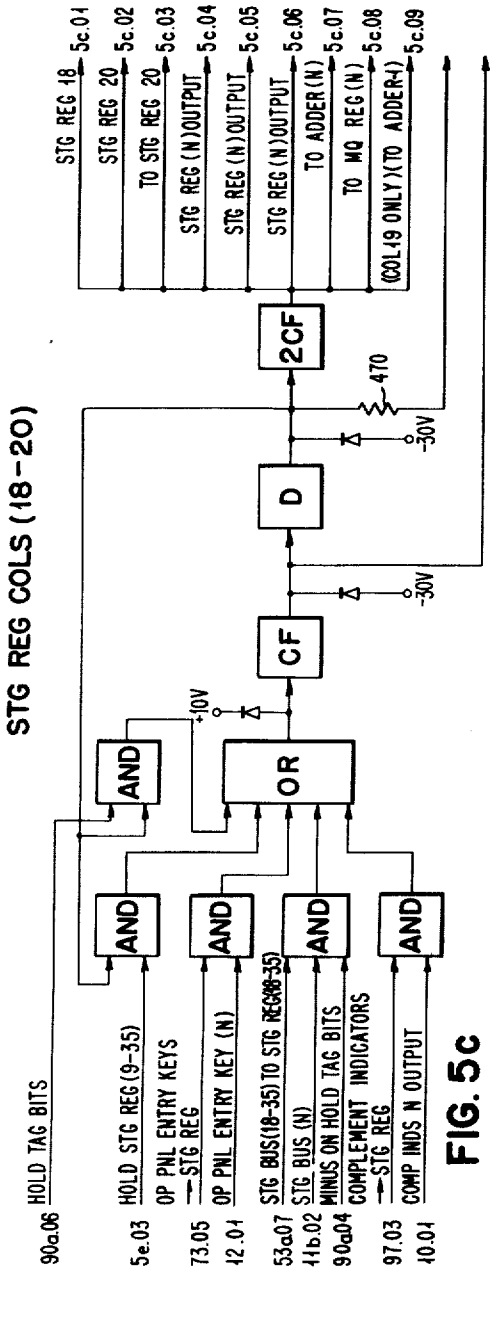

STG REG COLS (18-20)
STG REG 18 5c.01
STG REG 20 5c.02
TO STG REG 20 5c.03
STG REG (N) OUTPUT 5c.04
STG REG (N) OUTPUT 5c.05
STG REG (N) OUTPUT 5c.06
TO ADDER(N) 5c.07
TO MQ REG(N) 5c.08
(COL 19 ONLY)(TO ADDER-1) 5c.09
2CF
470
-30V
D
CF
+10V
OR
AND
HOLD TAG BITS 90a.06
5e.03 HOLD STG REG (9-35)
OP PNL ENTRY KEYS →STG REG 73.05
OP PNL ENTRY KEY (N) 12.04
53a07 STG BUS(18-35) TO STG REG(18-35)
41b.02 STG BUS (N)
MINUS ON HOLD TAG BITS 90a04
COMPLEMENT INDICATORS →STG REG 97.03
COMP INDS N OUTPUT 40.04

FIG. 5c

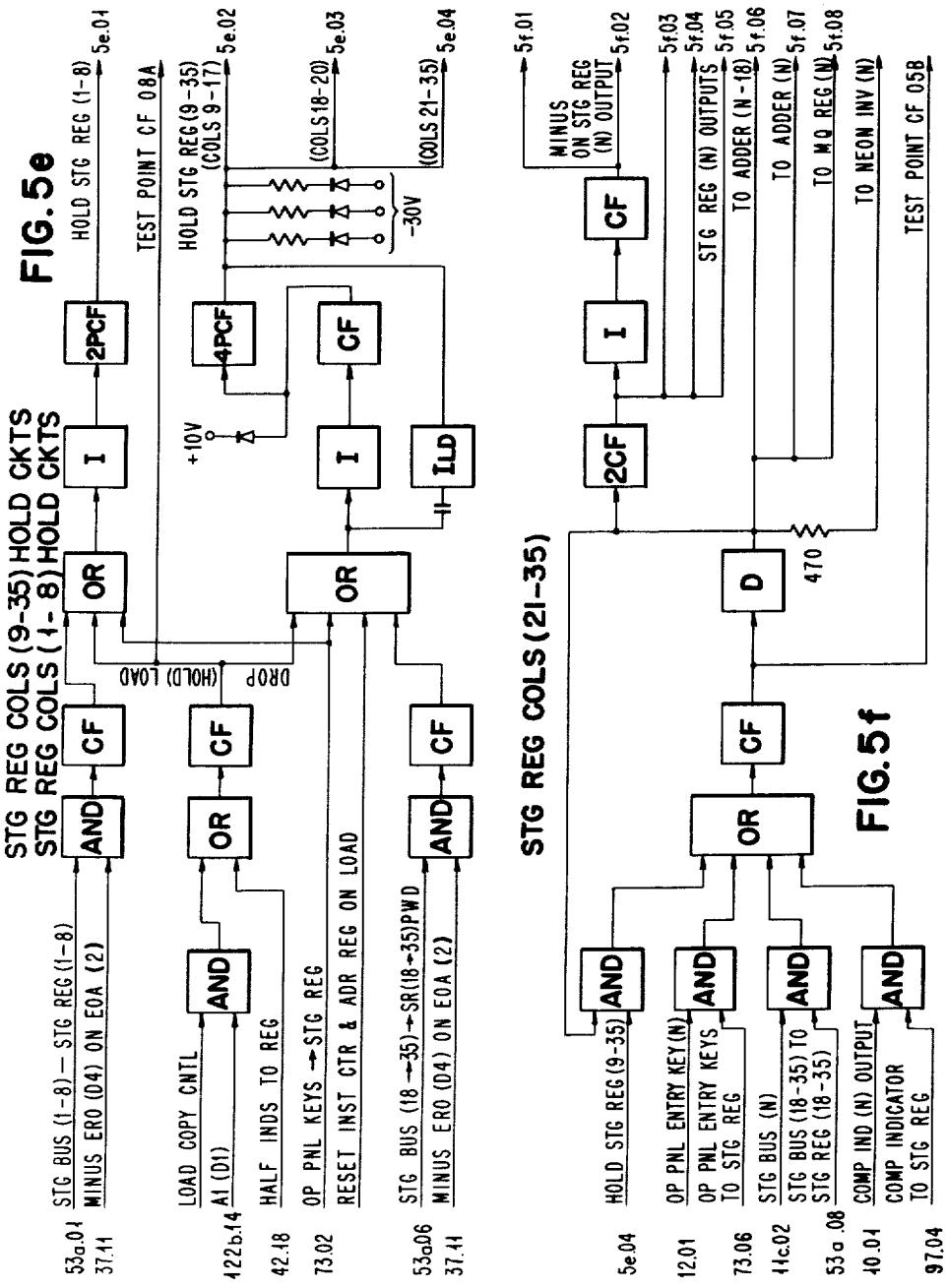


FIG. 5e
STG REG COLS (9-35) HOLD CKTS
STG REG COLS (1-8) HOLD CKTS
HOLD STG REG (1-8)
5e.01
TEST POINT CF 08A
HOLD STG REG (9-35) (COLS 9-17)
5e.02
(COLS 18-20)
5e.03
(COLS 21-35)
5e.04
2PCF
4PCF
I
CF
ILD
OR
AND
+10V
-30V
(HOLD) LOAD
DROP
STG BUS (1-8) — STG REG (1-8)
MINUS ERO (04) ON EOA (2)
53a.01
37.11
LOAD COPY CNTL
A1 (01)
422b.14
HALF INDS TO REG
42.18
OP PNL KEYS → STG REG
RESET INST CTR & ADR REG ON LOAD
73.02
STG BUS (18→35) → SR (18→35) PWD
MINUS ERO (04) ON EOA (2)
53a.06
37.11
STG REG COLS (21-35)
5f.01
MINUS ON STG REG (N) OUTPUT
5f.02
5f.03
5f.04
5f.05
5f.06
5f.07
5f.08
STG REG (N) OUTPUTS
TO ADDER (N-18)
TO ADDER (N)
TO MQ REG (N)
TO NEON INV (N)
TEST POINT CF 05B
2CF
D
470
HOLD STG REG (9-35)
5e.04
OP PNL ENTRY KEY (N)
OP PNL ENTRY KEYS TO STG REG
12.01
73.06
STG BUS (N)
STG BUS (18-35) TO STG REG (18-35)
44c.02
53a.08
COMP IND (N) OUTPUT
COMP INDICATOR TO STG REG
40.04
97.04
FIG. 5f

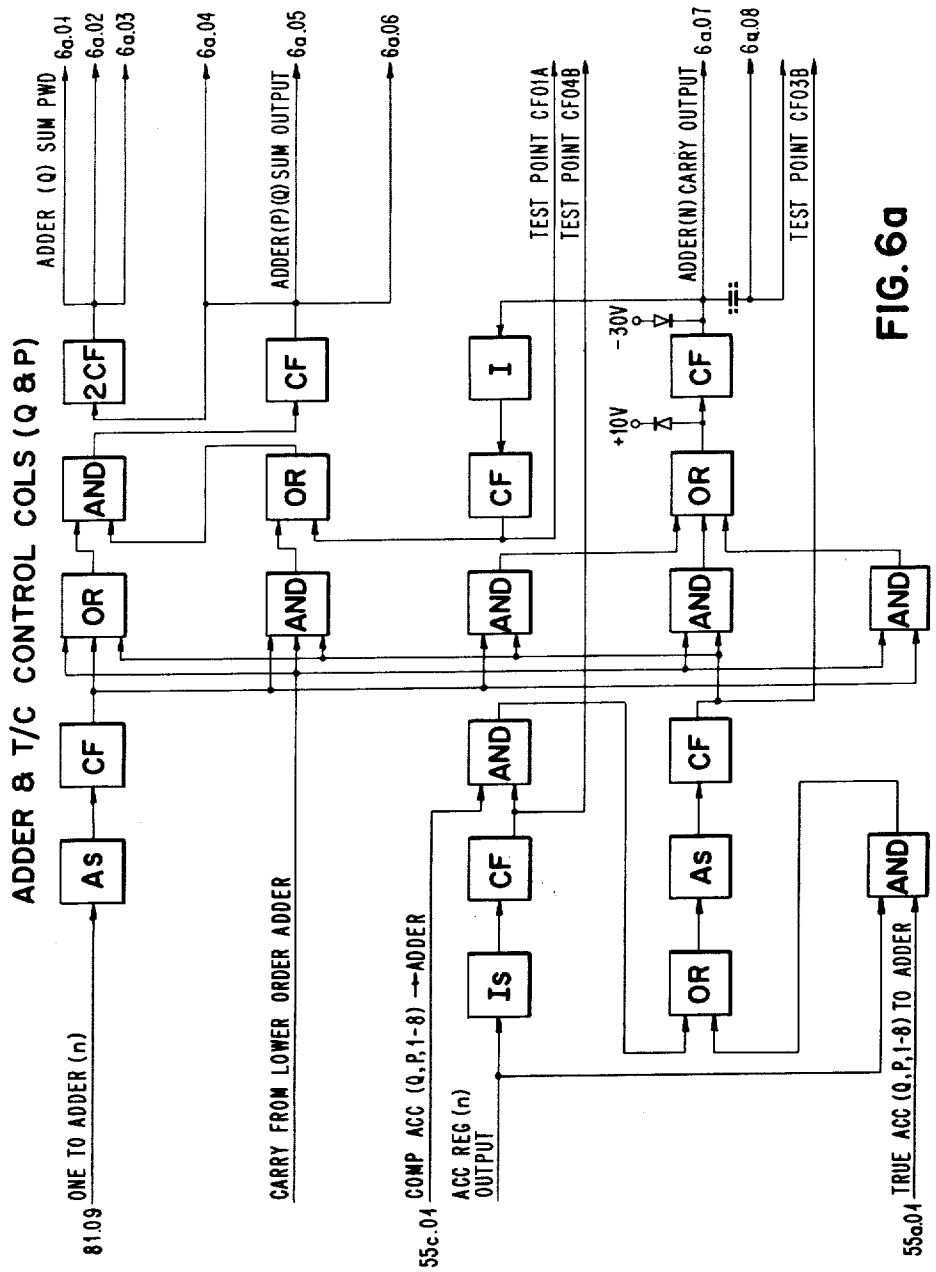

ADDER & T/C CONTROL COLS (Q & P)
ADDER (Q) SUM PWD
6a.01
6a.02
6a.03
6a.04
ADDER (P)(Q) SUM OUTPUT
6a.05
6a.06
TEST POINT CF01A
TEST POINT CF04B
ADDER (N) CARRY OUTPUT
6a.07
6a.08
TEST POINT CF03B
-30V
+10V
2CF
CF
I
AND
OR
As
Is
81.09 ONE TO ADDER (n)
CARRY FROM LOWER ORDER ADDER
55c.01 COMP ACC (Q,P,1-8) → ADDER
ACC REG (n) OUTPUT
55a.01 TRUE ACC (Q,P,1-8) TO ADDER

FIG. 6a

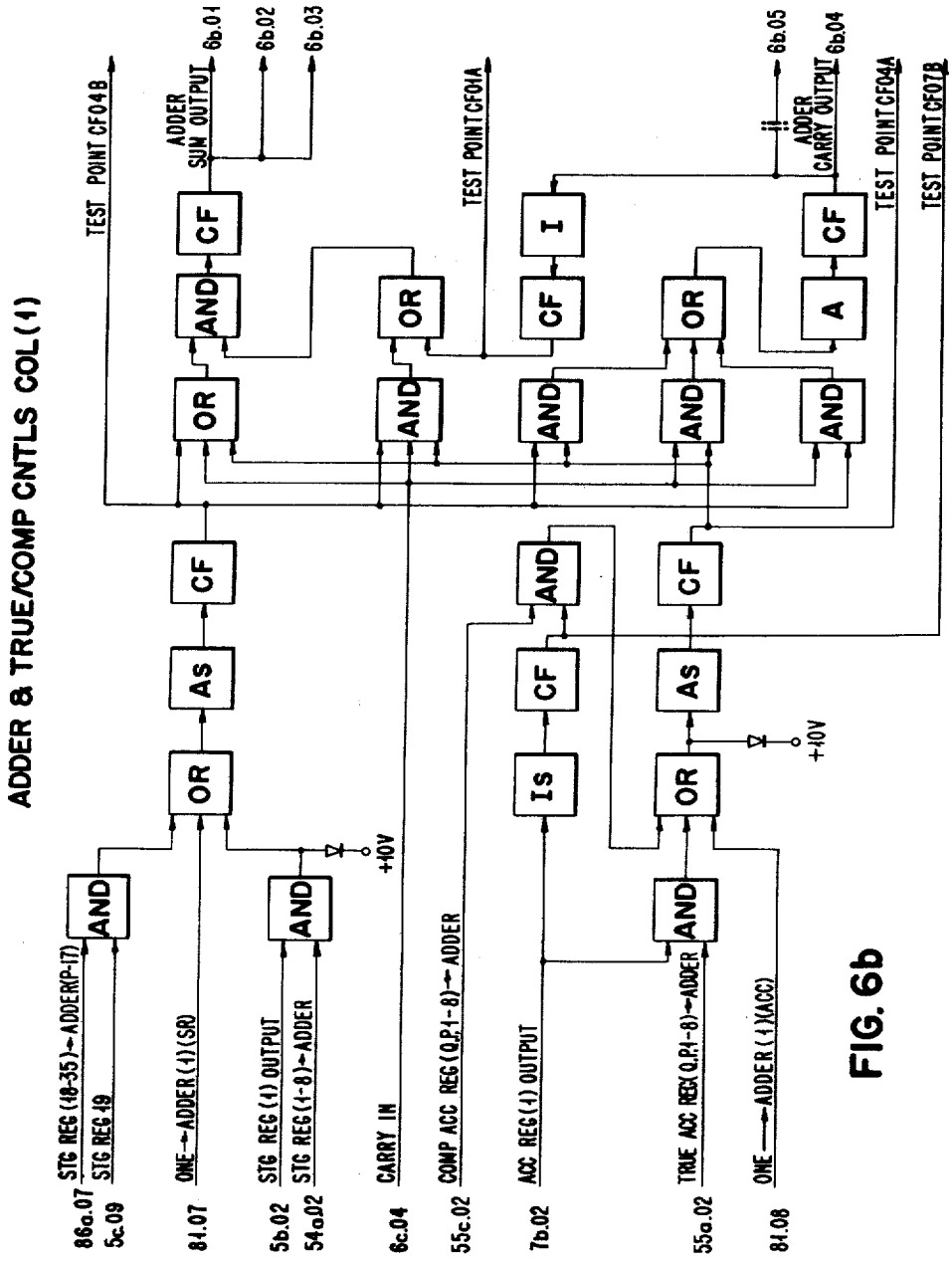
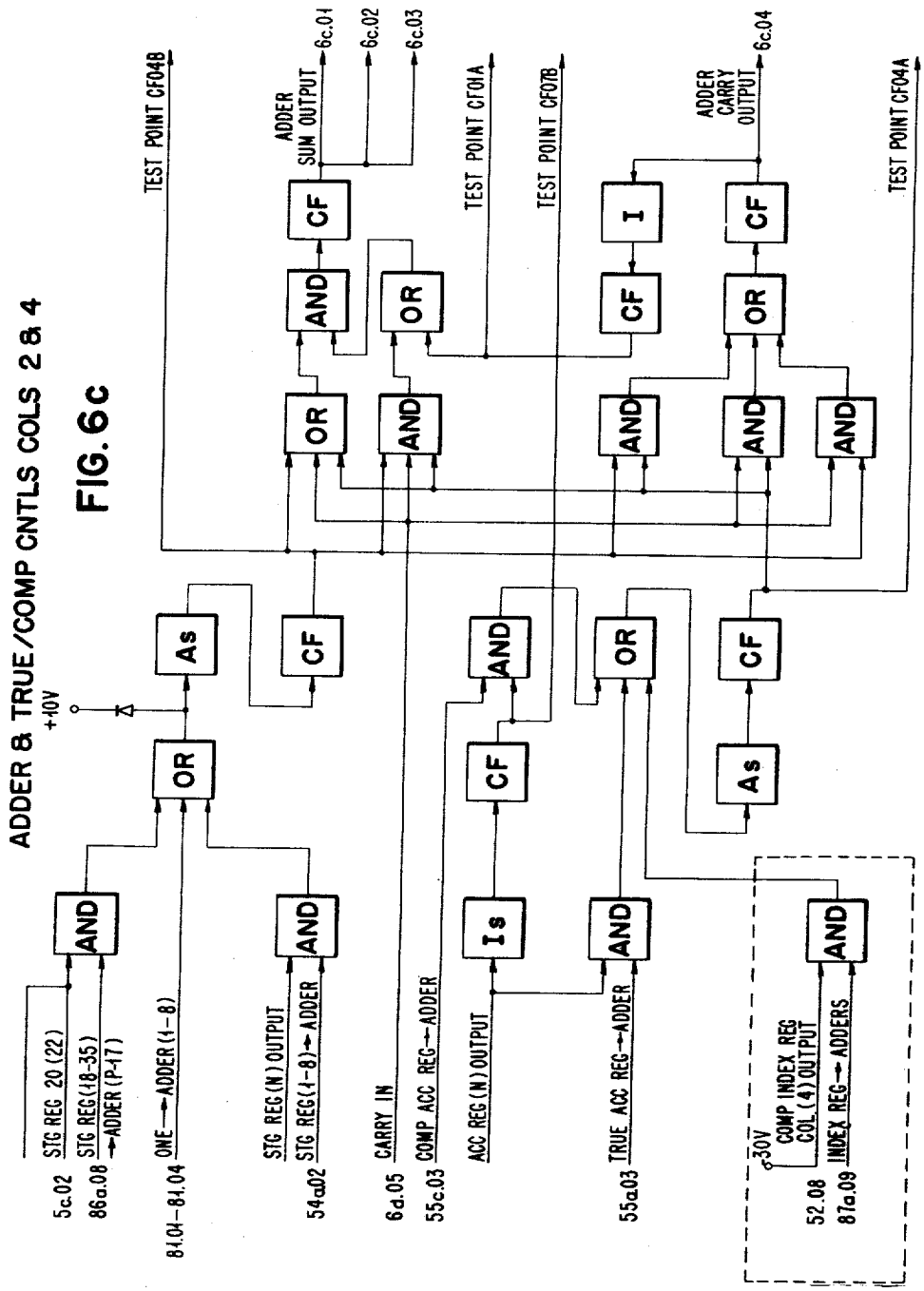

ADDER & TRUE/COMP CNTLS COL (1)
STG REG (48-35)→ADDER(P-17)
STG REG 49
ONE→ADDER (1) (SR)
STG REG (1) OUTPUT
STG REG (1-8)→ADDER
CARRY IN
COMP ACC REG (Q,P1-8)→ADDER
ACC REG (1) OUTPUT
TRUE ACC REG (Q,P1-8)→ADDER
ONE→ADDER (1) (ACC)
86a.07
5c.09
81.07
5b.02
54a.02
6c.04
55c.02
7b.02
55a.02
81.08
AND
OR
CF
As
Is
+10V
TEST POINT CF04B
TEST POINT CF04A
TEST POINT CF04A
TEST POINT CF07B
ADDER SUM OUTPUT
ADDER CARRY OUTPUT
6b.01
6b.02
6b.03
6b.04
6b.05
I
A

FIG. 6b


ADDER & TRUE/COMP CNTLS COLS 2 & 4
FIG. 6c
+10V
-30V
AND
OR
As
Is
CF
I
STG REG 20 (22)
STG REG (18-35) → ADDER (P-17)
ONE → ADDER (1-8)
STG REG (N) OUTPUT
STG REG (1-8) → ADDER
CARRY IN
COMP ACC REG → ADDER
ACC REG (N) OUTPUT
TRUE ACC REG → ADDER
COMP INDEX REG COL (4) OUTPUT
INDEX REG → ADDERS
ADDER SUM OUTPUT
ADDER CARRY OUTPUT
TEST POINT CF04B
TEST POINT CF01A
TEST POINT CF07B
TEST POINT CF04A
5c.02
86a.08
81.04-81.04
54a02
6d.05
55c.03
55a.03
52.08
87a.09
6c.01
6c.02
6c.03
6c.04

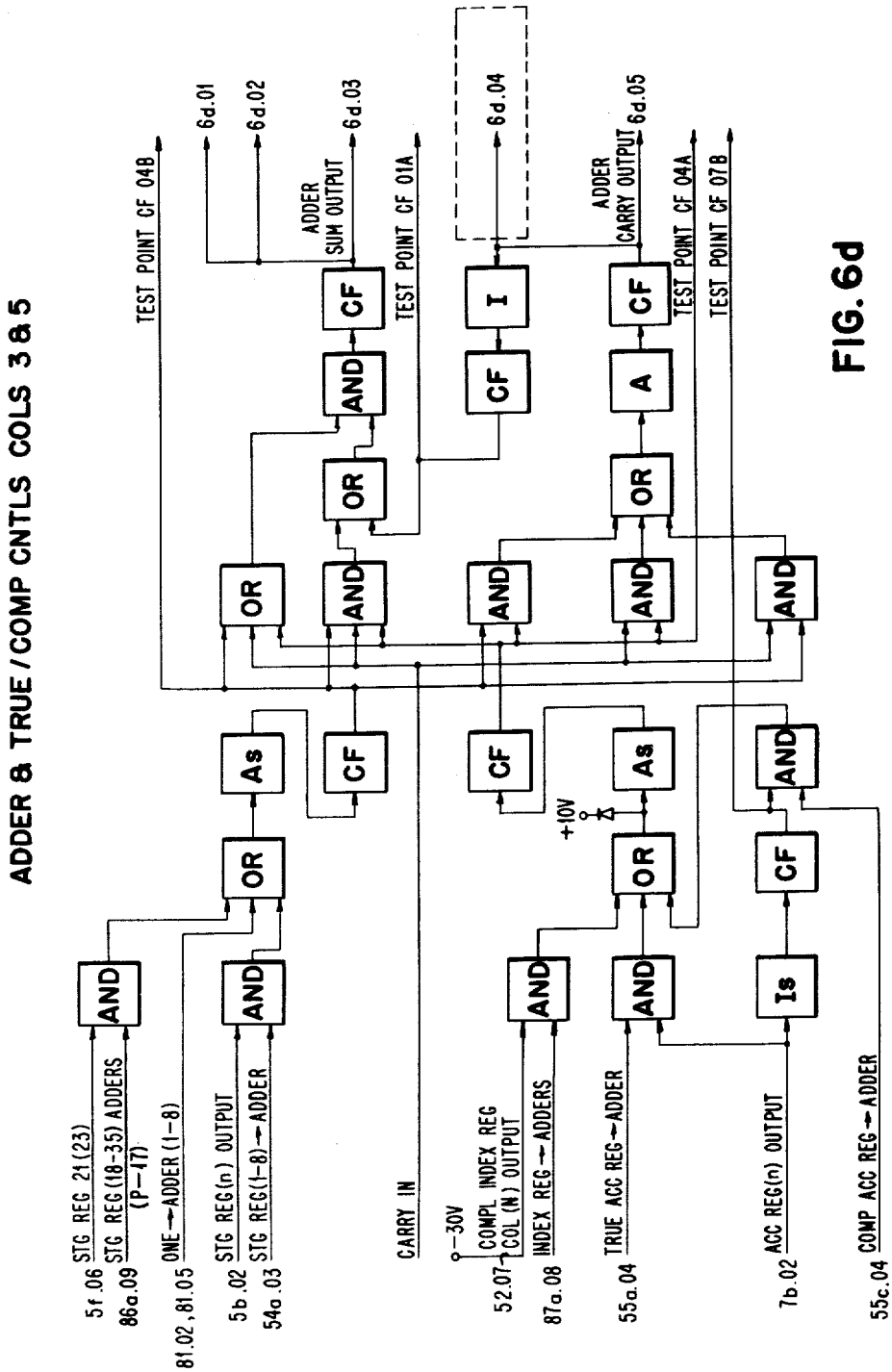

ADDER & TRUE / COMP CNTLS COLS 3 & 5
TEST POINT CF 04B
6d.01
6d.02
ADDER SUM OUTPUT
6d.03
TEST POINT CF 01A
6d.04
ADDER CARRY OUTPUT
6d.05
TEST POINT CF 04A
TEST POINT CF 07B
AND
OR
CF
I
A
As
Is
+10V
-30V
CARRY IN
5f.06 STG REG 21(23)
86a.09 STG REG(18-35) ADDERS (P-17)
81.02, 81.05 ONE→ADDER (1-8)
5b.02 STG REG(n) OUTPUT
54a.03 STG REG(1-8)→ADDER
52.07 COMPL INDEX REG COL (N) OUTPUT
87a.08 INDEX REG→ADDERS
55a.04 TRUE ACC REG→ADDER
7b.02 ACC REG(n) OUTPUT
55c.04 COMP ACC REG→ADDER

FIG. 6d

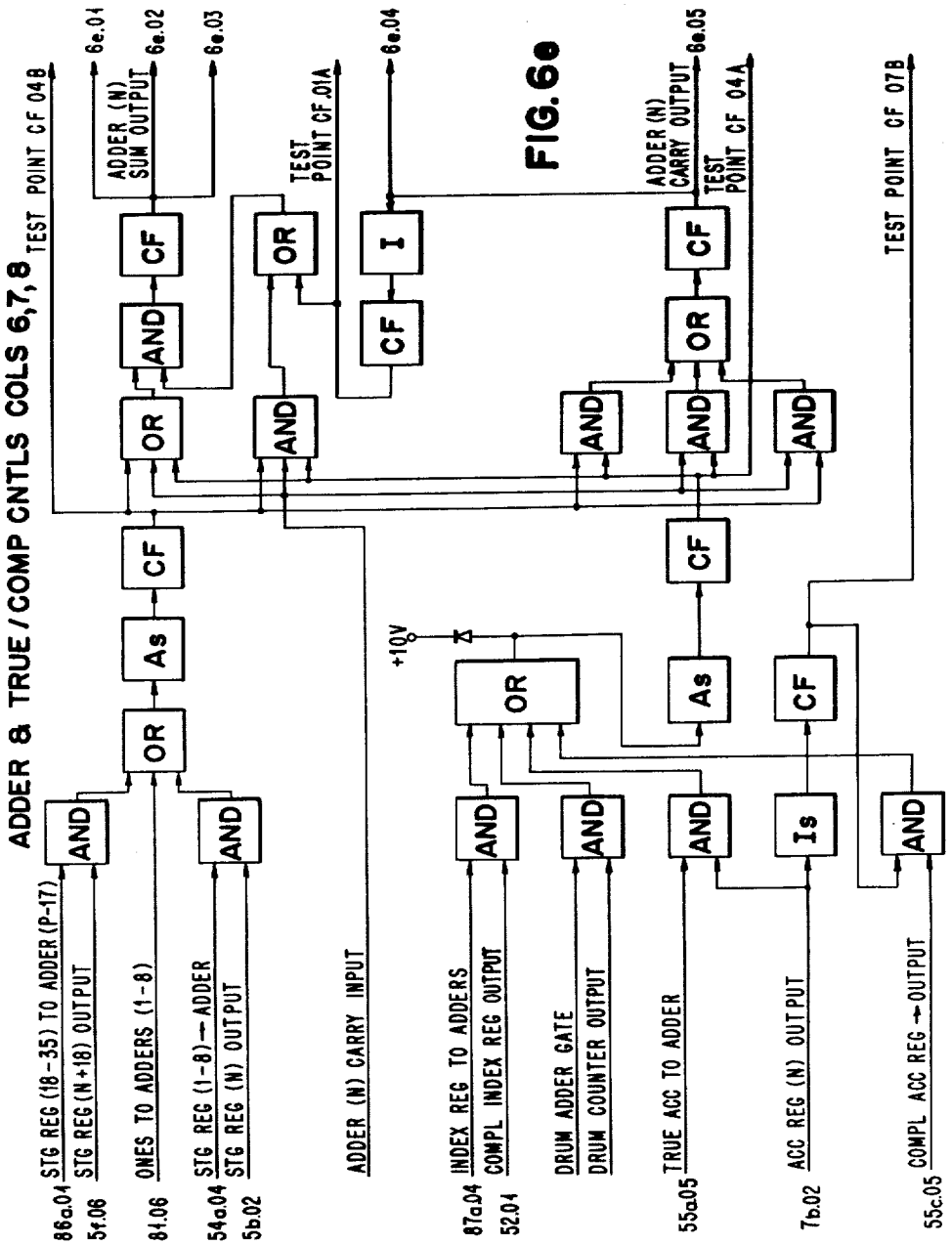

ADDER & TRUE / COMP CNTLS COLS 6,7,8
TEST POINT CF 04B
6a.01
ADDER (N) SUM OUTPUT
6a.02
6a.03
TEST POINT CF 01A
6a.04
ADDER (N) CARRY OUTPUT
6a.05
TEST POINT CF 04A
TEST POINT CF 07B
FIG. 6a
AND
OR
CF
As
Is
I
+10V
86a.04 STG REG (18-35) TO ADDER (P-17)
51.06 STG REG (N+18) OUTPUT
81.06 ONES TO ADDERS (1-8)
54a.04 STG REG (1-8) → ADDER
5b.02 STG REG (N) OUTPUT
ADDER (N) CARRY INPUT
87a.04 INDEX REG TO ADDERS
52.04 COMPL INDEX REG OUTPUT
DRUM ADDER GATE
DRUM COUNTER OUTPUT
55a.05 TRUE ACC TO ADDER
7b.02 ACC REG (N) OUTPUT
55c.05 COMPL ACC REG → OUTPUT

FIG. 6f

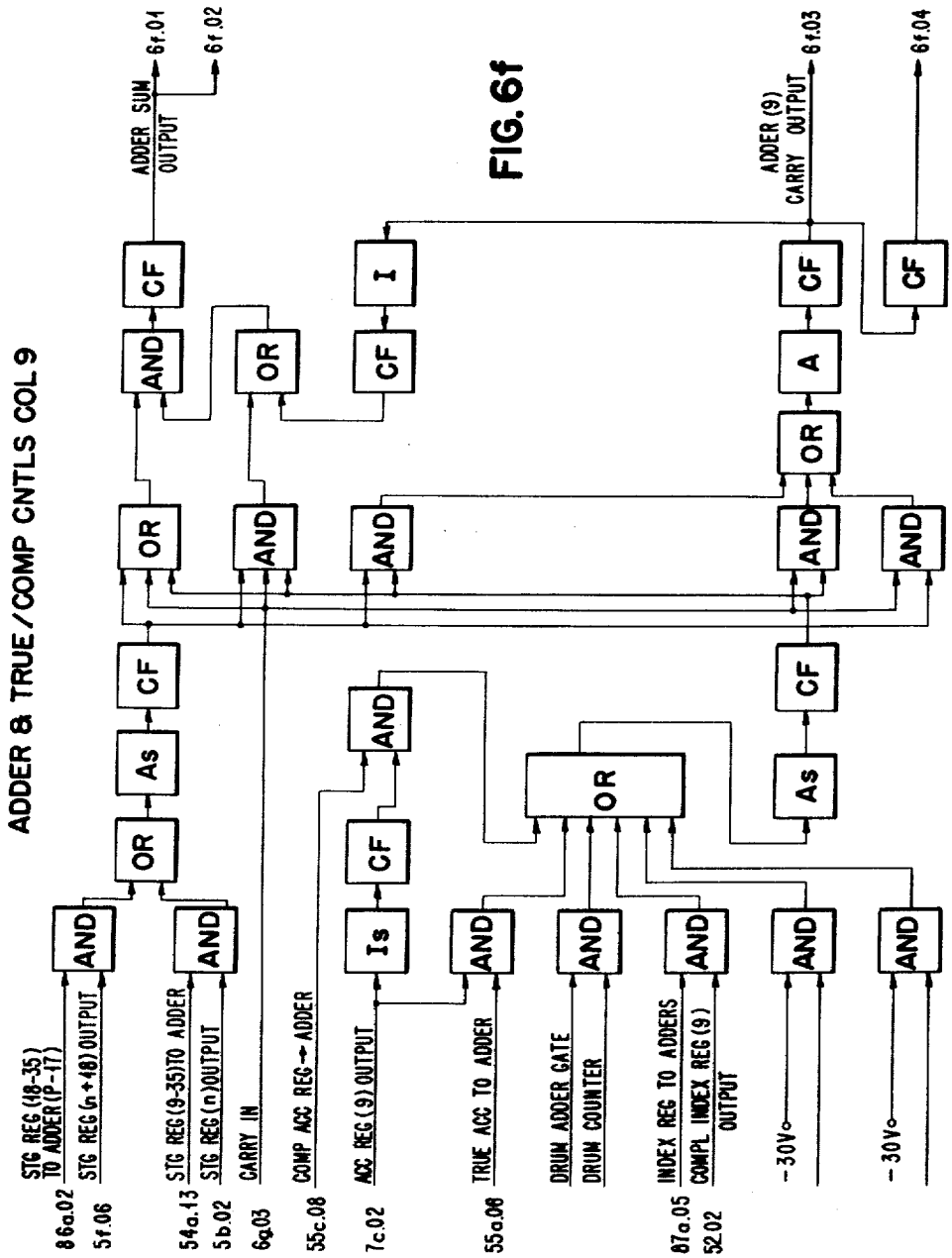
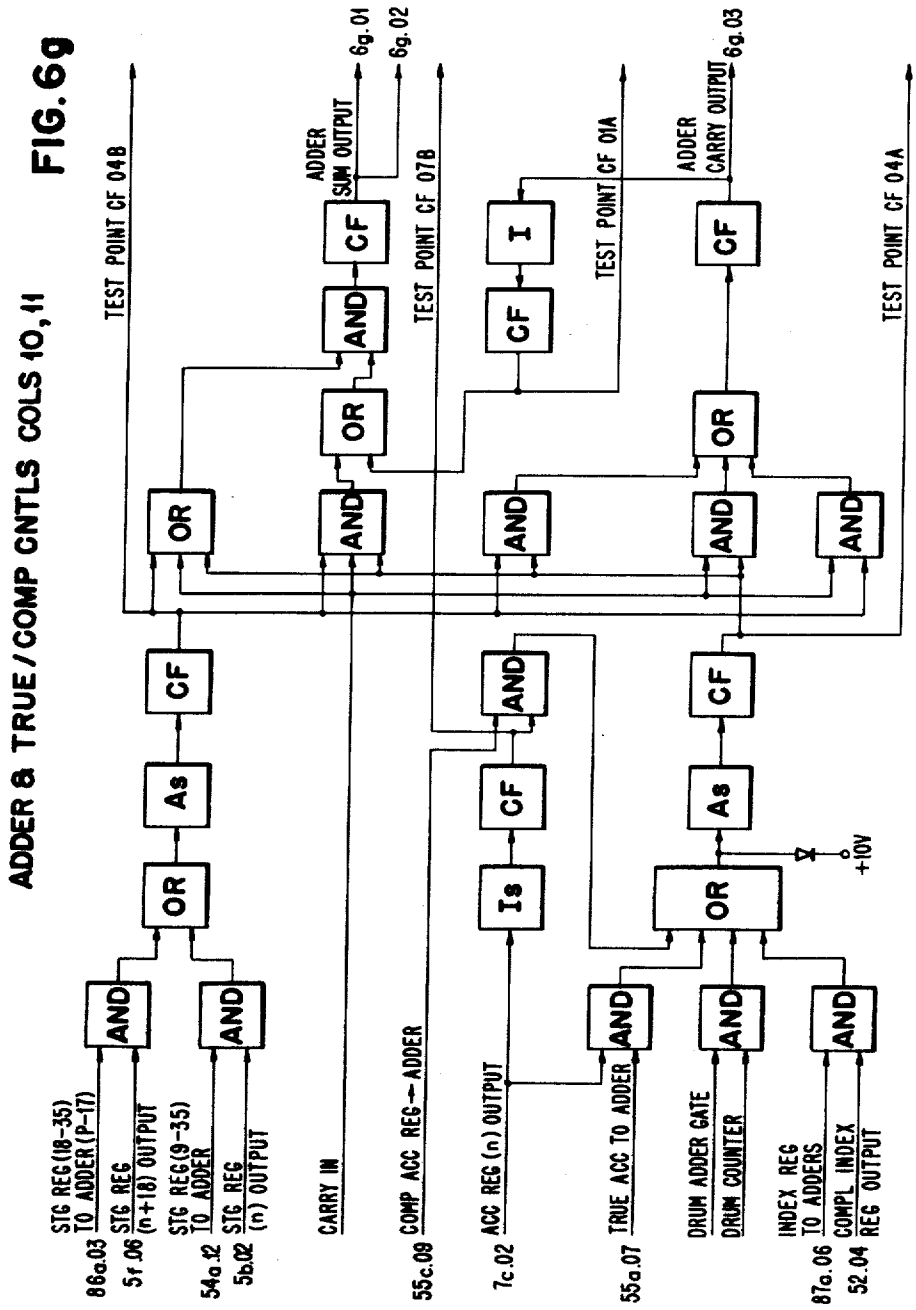

ADDER & TRUE/COMP CNTLS COL 9
STG REG (18-35) TO ADDER (P-17)
86a.02
STG REG (n+18) OUTPUT
5f.06
STG REG (9-35) TO ADDER
54a.13
STG REG (n) OUTPUT
5b.02
CARRY IN
6q.03
COMP ACC REG → ADDER
55c.08
ACC REG (9) OUTPUT
7c.02
TRUE ACC TO ADDER
55a.06
DRUM ADDER GATE
DRUM COUNTER
INDEX REG TO ADDERS
87a.05
COMPL INDEX REG (9) OUTPUT
52.02
-30V
-30V
ADDER SUM OUTPUT
6f.01
6f.02
ADDER (9) CARRY OUTPUT
6f.03
6f.04
AND
OR
CF
As
Is
I
A

FIG. 6g


ADDER & TRUE/COMP CNTLS COLS 10, 11
TEST POINT CF 04B
TEST POINT CF 07B
TEST POINT CF 01A
TEST POINT CF 04A
ADDER SUM OUTPUT
6g.01
6g.02
ADDER CARRY OUTPUT
6g.03
OR
AND
CF
I
As
Is
+10V
STG REG (18-35) TO ADDER (P-17)
86a.03
STG REG (n+18) OUTPUT
5f.06
STG REG (9-35) TO ADDER
54a.12
STG REG (n) OUTPUT
5b.02
CARRY IN
COMP ACC REG → ADDER
55c.09
ACC REG (n) OUTPUT
7c.02
TRUE ACC TO ADDER
55a.07
DRUM ADDER GATE
DRUM COUNTER
INDEX REG TO ADDERS
87a.06
COMPL INDEX REG OUTPUT
52.04

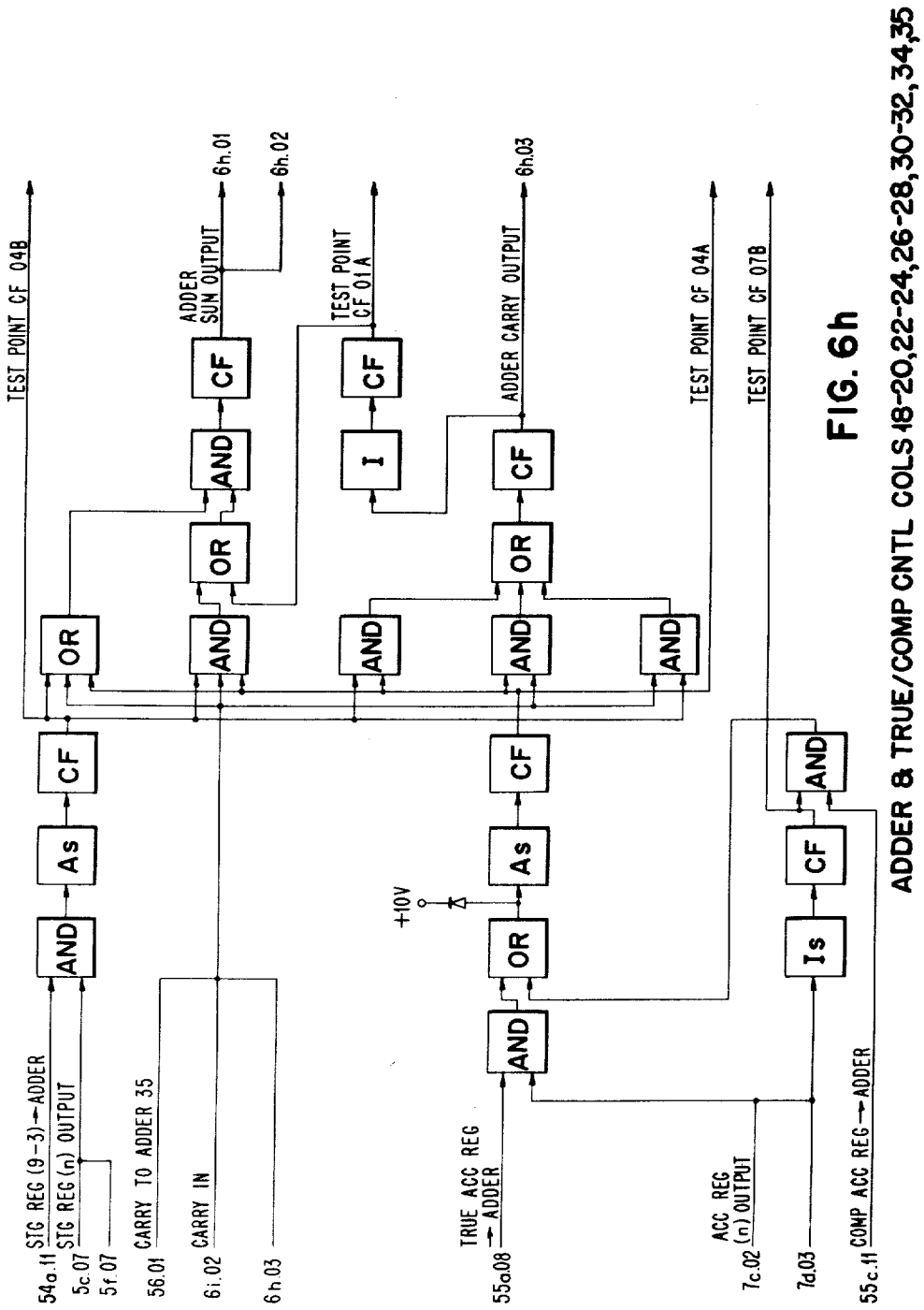

ADDER & TRUE/COMP CNTL COLS 18-20, 22-24, 26-28, 30-32, 34, 35
TEST POINT CF 04B
TEST POINT CF 04A
TEST POINT CF 07B
ADDER SUM OUTPUT
6h.01
6h.02
TEST POINT CF 01A
ADDER CARRY OUTPUT
6h.03
CF
AND
OR
I
As
Is
+10V
STG REG (9-3) → ADDER
STG REG (n) OUTPUT
CARRY TO ADDER 35
CARRY IN
TRUE ACC REG → ADDER
ACC REG (n) OUTPUT
COMP ACC REG → ADDER
54a.11
5c.07
5f.07
56.01
6i.02
6h.03
55a.08
7c.02
7d.03
55c.11

FIG. 6h

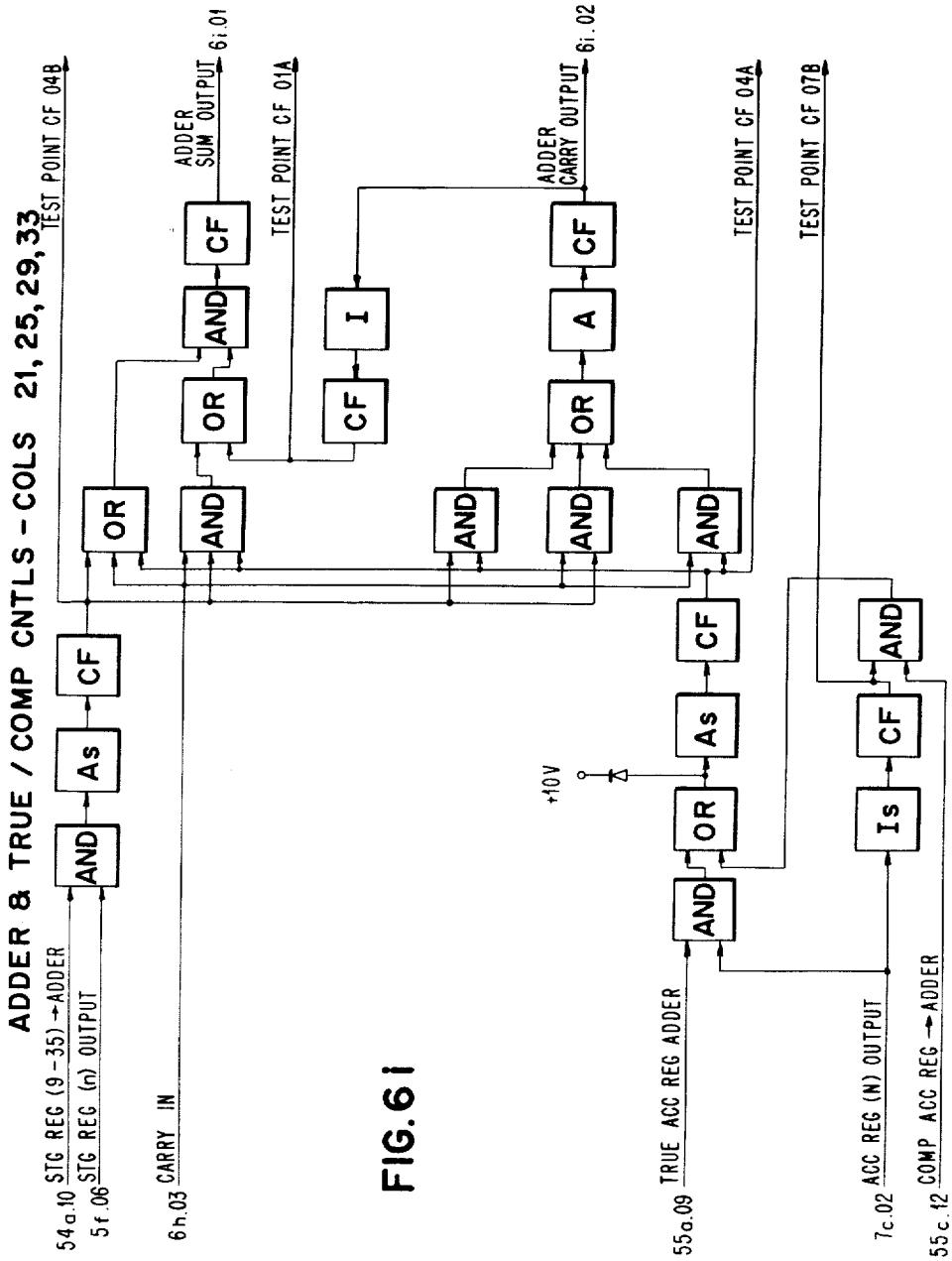

ADDER & TRUE / COMP CNTLS - COLS 21, 25, 29, 33
54a.10 STG REG (9-35) → ADDER
5f.06 STG REG (n) OUTPUT
6h.03 CARRY IN
AND
As
CF
OR
AND
OR
CF
I
CF
TEST POINT CF 04B
TEST POINT CF 01A
ADDER SUM OUTPUT 6i.01
AND
A
CF
ADDER CARRY OUTPUT 6i.02
TEST POINT CF 04A
TEST POINT CF 07B
+10V
AND
OR
As
CF
AND
Is
CF
AND
55a.09 TRUE ACC REG ADDER
7c.02 ACC REG (N) OUTPUT
55c.12 COMP ACC REG → ADDER

FIG. 6i

ADDER & TRUE / COMP CNTLS COL 16

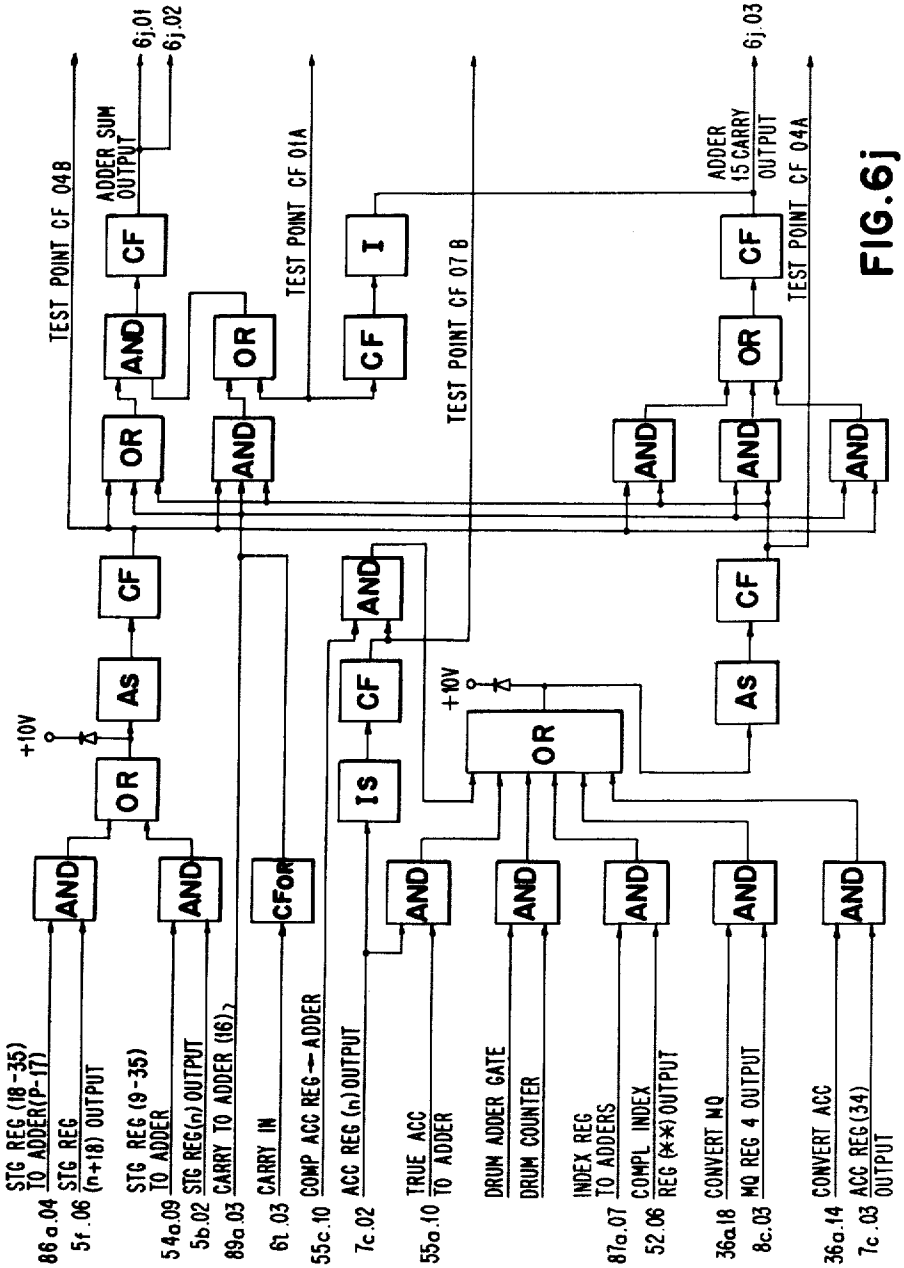
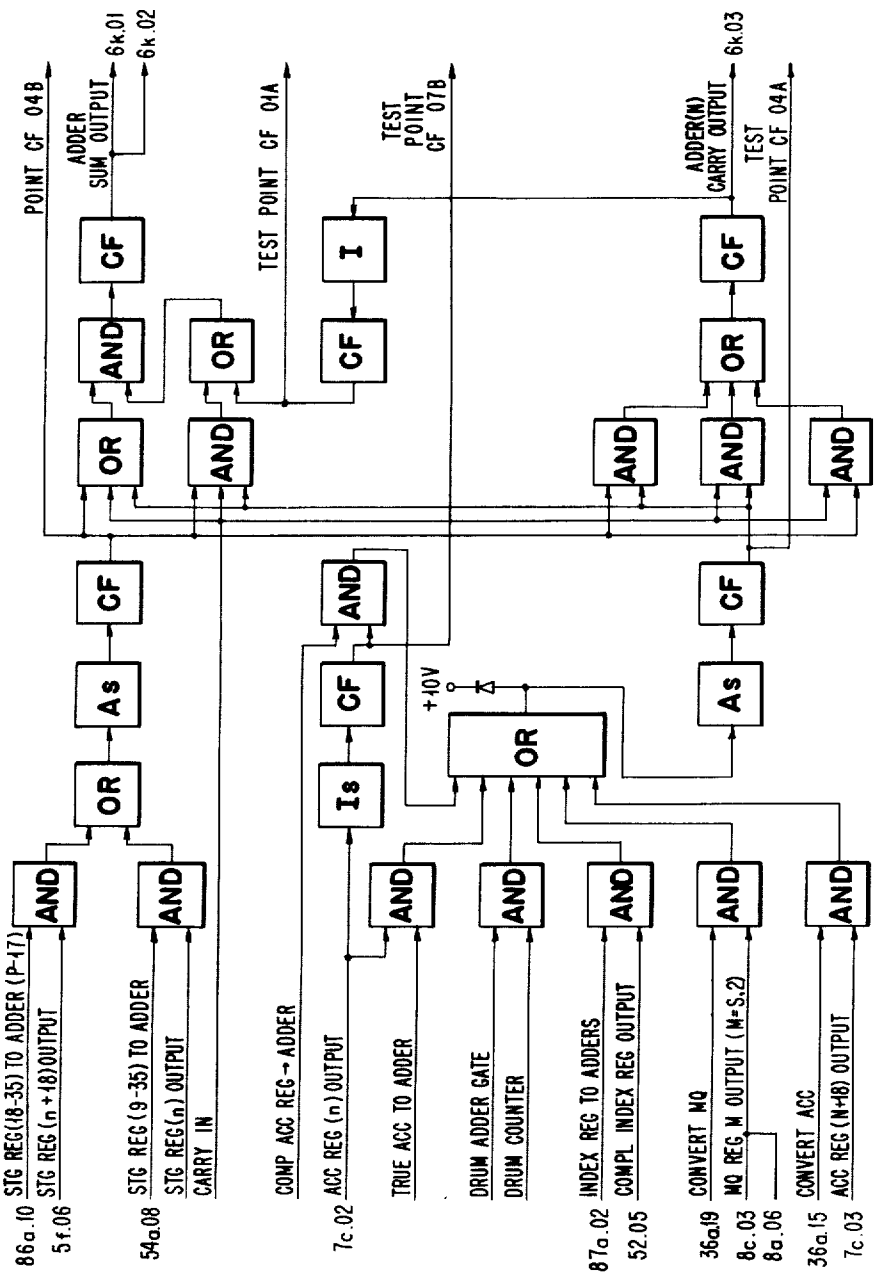


FIG.6j

FIG. 6k ADDER & TRUE/COMP CNTLS COLS 12,14



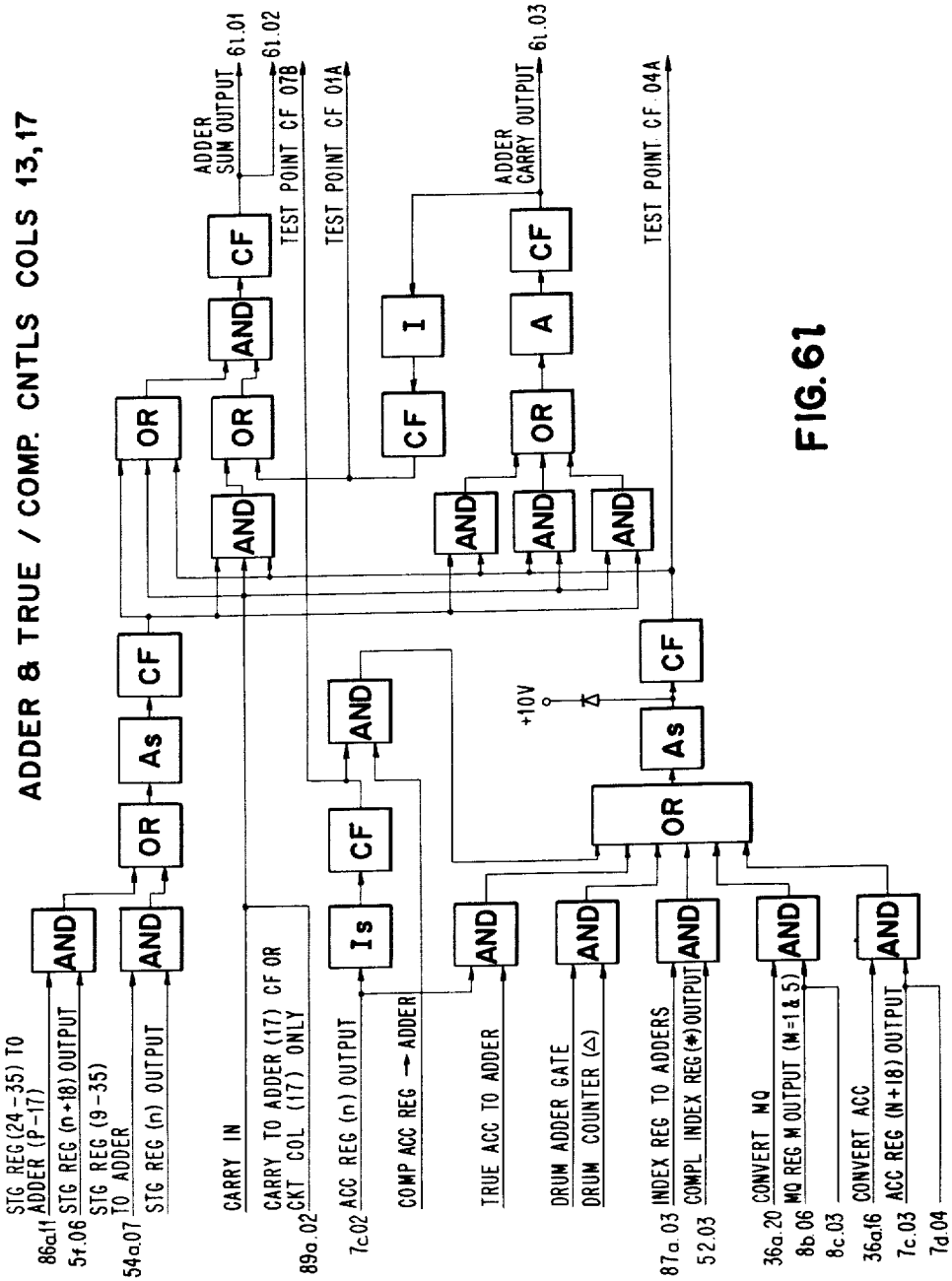

ADDER & TRUE / COMP. CNTLS COLS 13,17
STG REG (24-35) TO ADDER (P-17)
86a.11
STG REG (n+18) OUTPUT
5f.06
STG REG (9-35) TO ADDER
54a.07
STG REG (n) OUTPUT
CARRY IN
CARRY TO ADDER (17) CF OR CKT COL (17) ONLY
89a.02
ACC REG (n) OUTPUT
7c.02
COMP ACC REG → ADDER
TRUE ACC TO ADDER
DRUM ADDER GATE
DRUM COUNTER (△)
INDEX REG TO ADDERS
87a.03
COMPL INDEX REG (*) OUTPUT
52.03
CONVERT MQ
36a.20
MQ REG M OUTPUT (M=1 & 5)
8b.06
8c.03
CONVERT ACC
36a.16
ACC REG (N+18) OUTPUT
7c.03
7d.04
ADDER SUM OUTPUT
61.01
TEST POINT CF 07B
61.02
TEST POINT CF 01A
ADDER CARRY OUTPUT
61.03
TEST POINT CF 04A
+10V
AND
OR
As
Is
CF
I
A

FIG. 61

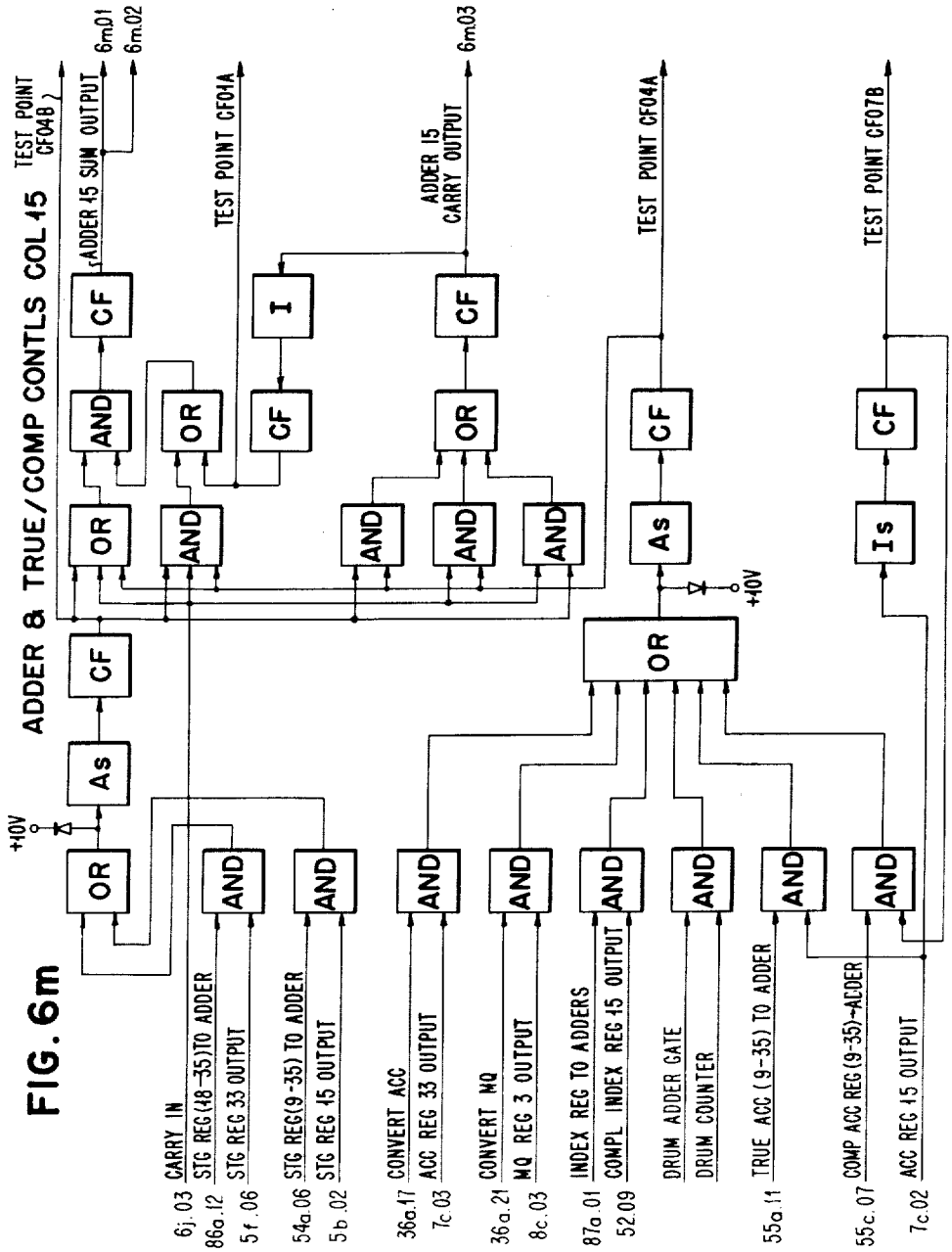

ADDER & TRUE/COMP CONTLS COL 45
TEST POINT CF04B
ADDER 45 SUM OUTPUT
6m.01
6m.02
TEST POINT CF04A
ADDER 15 CARRY OUTPUT
6m.03
TEST POINT CF04A
TEST POINT CF07B
+10V
OR
As
CF
AND
I
Is
6j.03 CARRY IN
86a.12 STG REG(48-35)TO ADDER
5f.06 STG REG 33 OUTPUT
54a.06 STG REG(9-35) TO ADDER
5b.02 STG REG 45 OUTPUT
36a.17 CONVERT ACC
7c.03 ACC REG 33 OUTPUT
36a.21 CONVERT MQ
8c.03 MQ REG 3 OUTPUT
87a.01 INDEX REG TO ADDERS
52.09 COMPL INDEX REG 45 OUTPUT
DRUM ADDER GATE
DRUM COUNTER
55a.11 TRUE ACC (9-35) TO ADDER
55c.07 COMP ACC REG (9-35)→ACDER
7c.02 ACC REG 15 OUTPUT

FIG. 6m

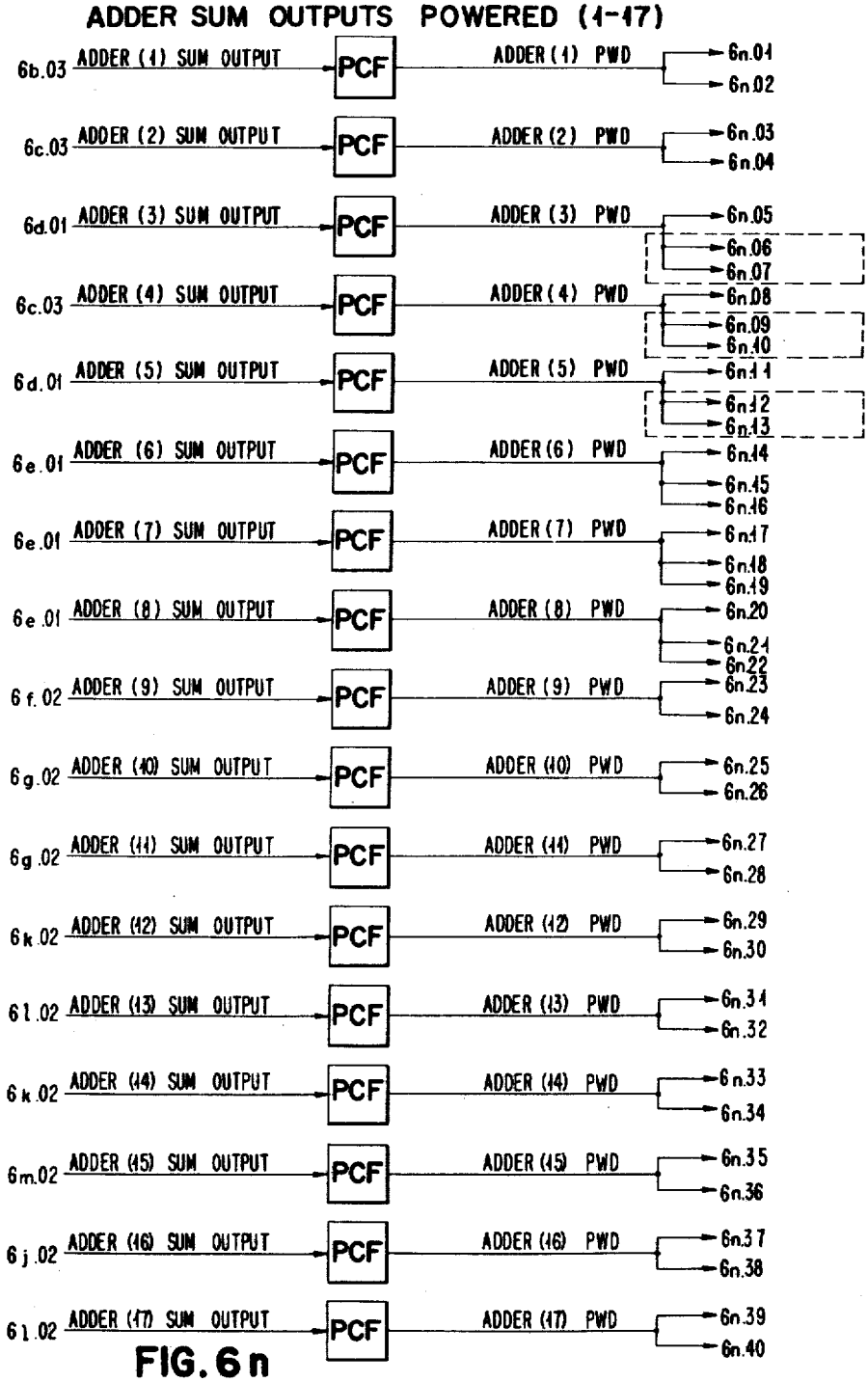

ADDER SUM OUTPUTS POWERED (1-17)
6b.03 ADDER (1) SUM OUTPUT
PCF
ADDER (1) PWD
6n.01
6n.02
6c.03 ADDER (2) SUM OUTPUT
PCF
ADDER (2) PWD
6n.03
6n.04
6d.01 ADDER (3) SUM OUTPUT
PCF
ADDER (3) PWD
6n.05
6n.06
6n.07
6c.03 ADDER (4) SUM OUTPUT
PCF
ADDER (4) PWD
6n.08
6n.09
6n.10
6d.01 ADDER (5) SUM OUTPUT
PCF
ADDER (5) PWD
6n.11
6n.12
6n.13
6e.01 ADDER (6) SUM OUTPUT
PCF
ADDER (6) PWD
6n.14
6n.15
6n.16
6e.01 ADDER (7) SUM OUTPUT
PCF
ADDER (7) PWD
6n.17
6n.18
6n.19
6e.01 ADDER (8) SUM OUTPUT
PCF
ADDER (8) PWD
6n.20
6n.21
6n.22
6f.02 ADDER (9) SUM OUTPUT
PCF
ADDER (9) PWD
6n.23
6n.24
6g.02 ADDER (10) SUM OUTPUT
PCF
ADDER (10) PWD
6n.25
6n.26
6g.02 ADDER (11) SUM OUTPUT
PCF
ADDER (11) PWD
6n.27
6n.28
6k.02 ADDER (12) SUM OUTPUT
PCF
ADDER (12) PWD
6n.29
6n.30
6l.02 ADDER (13) SUM OUTPUT
PCF
ADDER (13) PWD
6n.31
6n.32
6k.02 ADDER (14) SUM OUTPUT
PCF
ADDER (14) PWD
6n.33
6n.34
6m.02 ADDER (15) SUM OUTPUT
PCF
ADDER (15) PWD
6n.35
6n.36
6j.02 ADDER (16) SUM OUTPUT
PCF
ADDER (16) PWD
6n.37
6n.38
6l.02 ADDER (17) SUM OUTPUT
PCF
ADDER (17) PWD
6n.39
6n.40

FIG. 6n

May 29, 1962 J. L. BROWN 3,036,773
INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE
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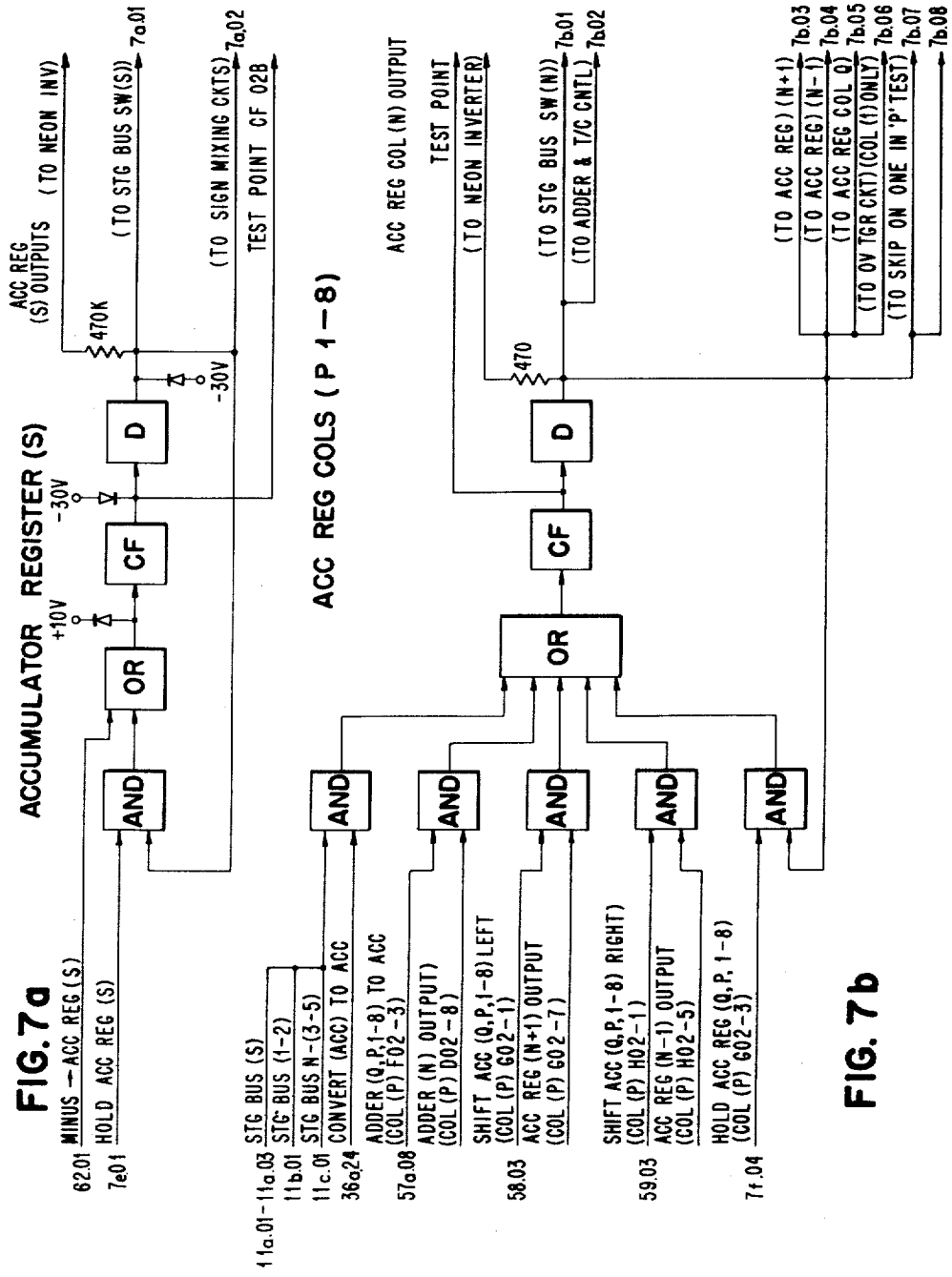

FIG. 7a

FIG. 7b

FIG. 7c

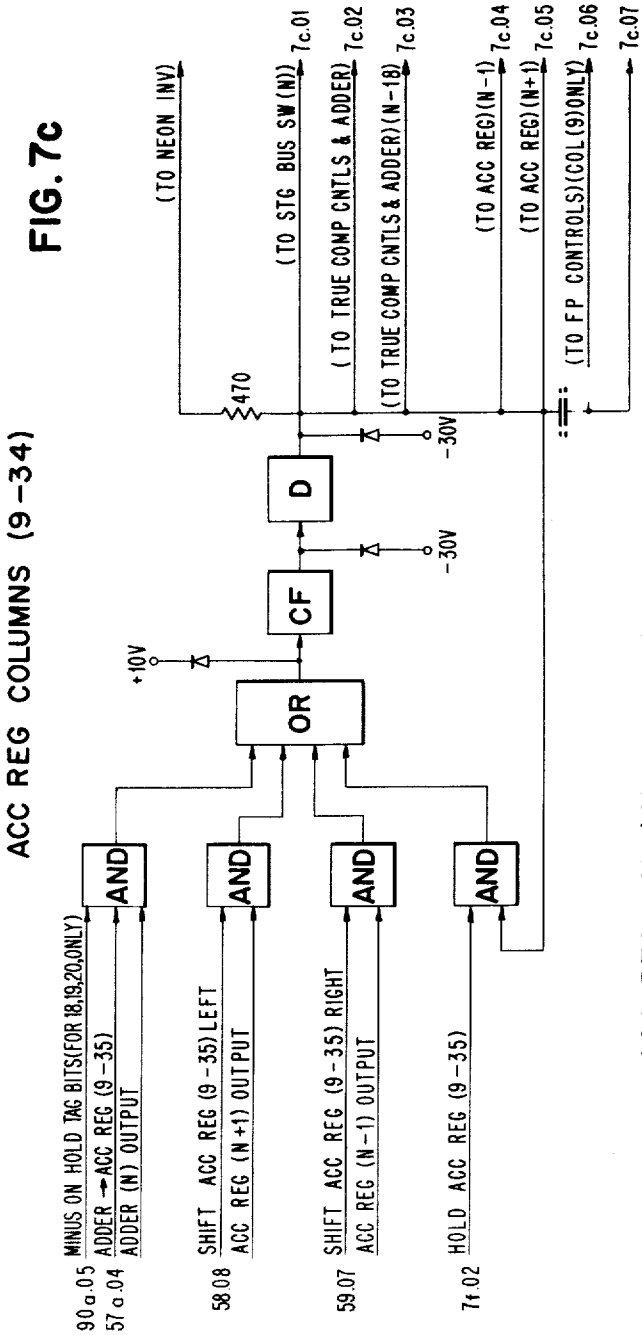
ACC REG COLUMNS (9-34)
(TO NEON INV)
(TO STG BUS SW (N)) 7c.01
(TO TRUE COMP CNTLS & ADDER) 7c.02
(TO TRUE COMP CNTLS & ADDER)(N-18) 7c.03
(TO ACC REG)(N-1) 7c.04
(TO ACC REG)(N+1) 7c.05
(TO F P CONTROLS)(COL(9)ONLY) 7c.06
7c.07
470
-30V
-30V
D
CF
+10V
OR
AND
AND
AND
AND
90 a.05 MINUS ON HOLD TAG BITS(FOR 18,19,20,ONLY)
57 a.04 ADDER → ACC REG (9-35)
ADDER (N) OUTPUT
58.08 SHIFT ACC REG (9-35) LEFT
ACC REG (N+1) OUTPUT
59.07 SHIFT ACC REG (9-35) RIGHT
ACC REG (N-1) OUTPUT
7t.02 HOLD ACC REG (9-35)

FIG. 7e

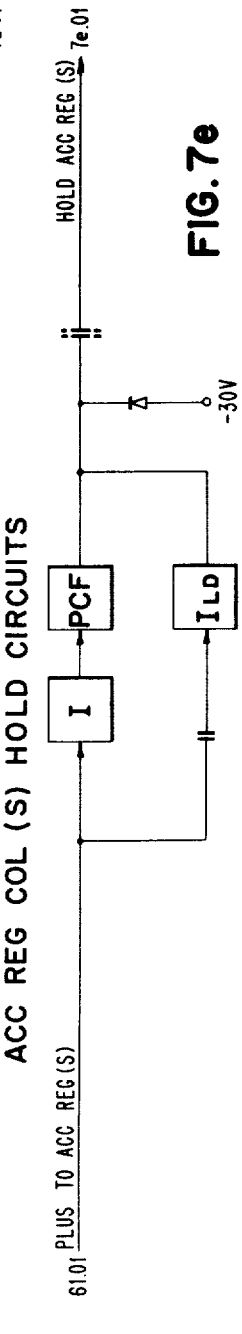
HOLD ACC REG (S) 7e.01
-30V
PCF
I
ILD
ACC REG COL (S) HOLD CIRCUITS
61.01 PLUS TO ACC REG (S)

FIG. 7d

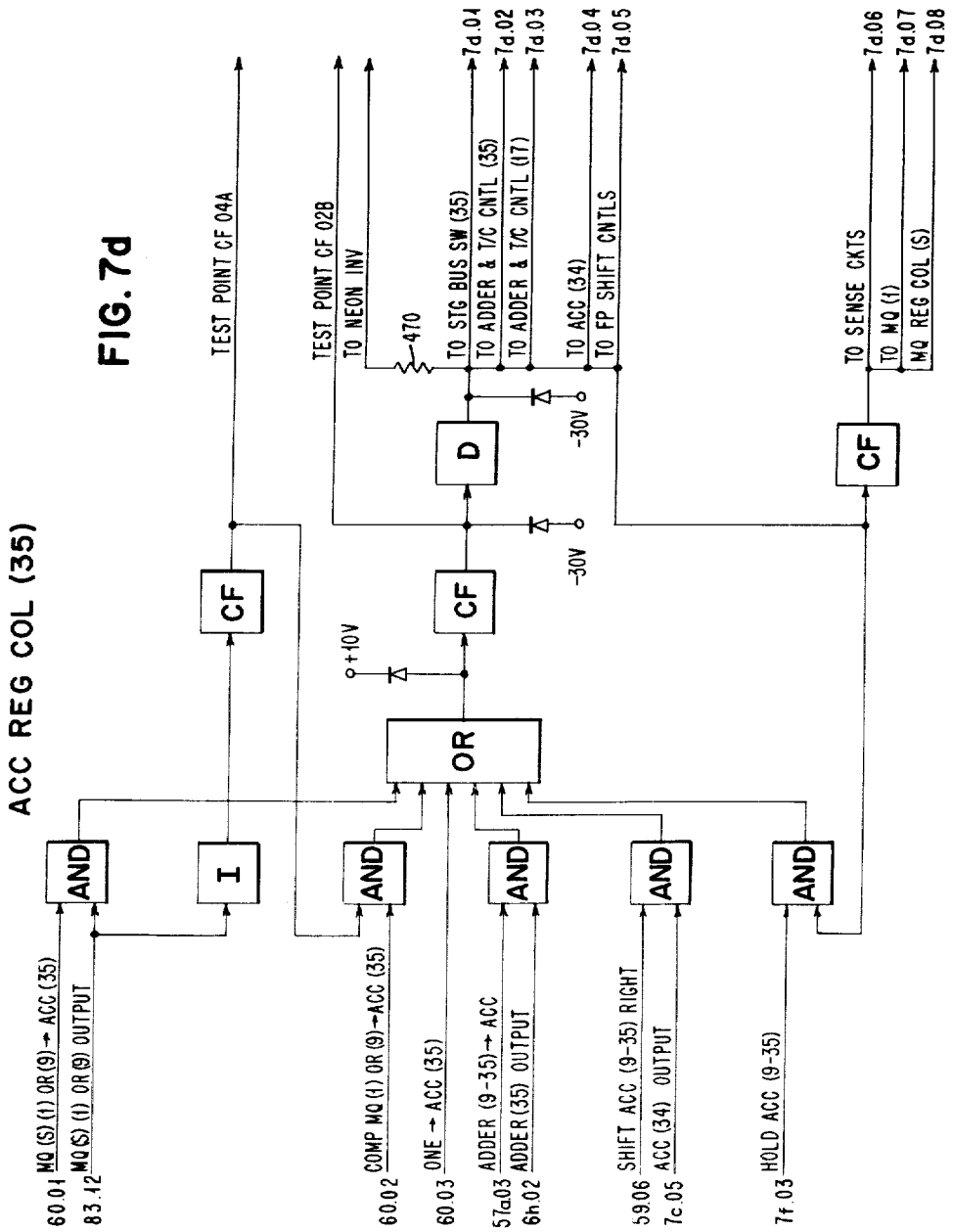
ACC REG COL (35)
AND
I
CF
OR
+10V
D
-30V
TEST POINT CF 04A
TEST POINT CF 02B
TO NEON INV
470
TO STG BUS SW (35)
TO ADDER & T/C CNTL (35)
TO ADDER & T/C CNTL (17)
TO ACC (34)
TO FP SHIFT CNTLS
TO SENSE CKTS
TO MQ (1)
MQ REG COL (S)
7d.01
7d.02
7d.03
7d.04
7d.05
7d.06
7d.07
7d.08
60.01 MQ (S) (1) OR (9) → ACC (35)
83.12 MQ (S) (1) OR (9) OUTPUT
60.02 COMP MQ (1) OR (9) → ACC (35)
60.03 ONE → ACC (35)
57a.03 ADDER (9-35) → ACC
6h.02 ADDER (35) OUTPUT
59.06 SHIFT ACC (9-35) RIGHT
7c.05 ACC (34) OUTPUT
7f.03 HOLD ACC (9-35)

FIG. 7f

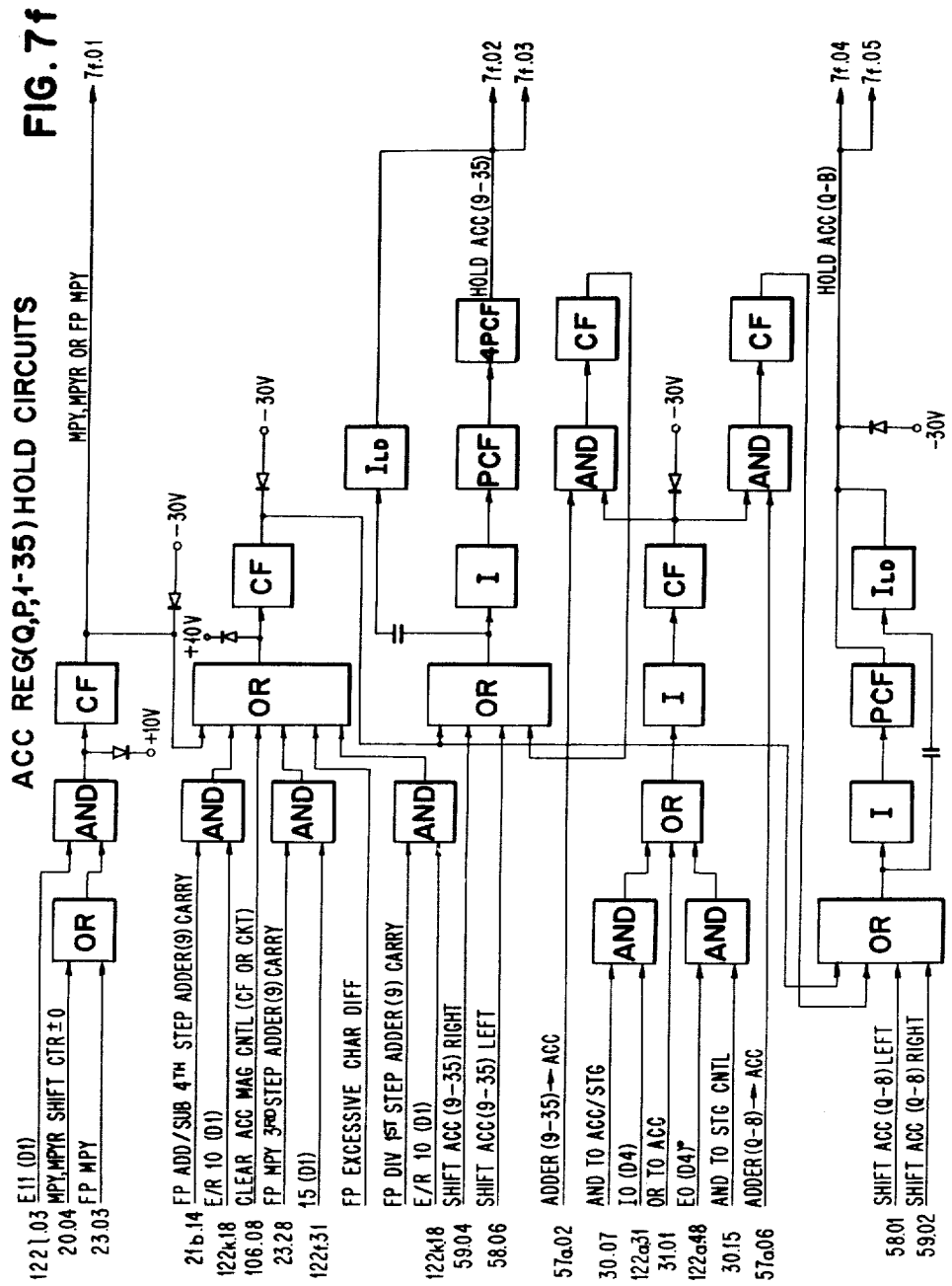
ACC REG(Q,P,1-35) HOLD CIRCUITS
MPY, MPYR OR FP MPY
7f.01
7f.02
7f.03
7f.04
7f.05
HOLD ACC (9-35)
HOLD ACC (Q-8)
CF
AND
OR
I
PCF
ILD
+10V
-30V
122l.03 E11 (D1)
20.04 MPY, MPYR SHIFT CTR ± 0
23.03 FP MPY
21b.14 FP ADD/SUB 4TH STEP ADDER(9) CARRY
122k.18 E/R 10 (D1)
106.08 CLEAR ACC MAG CNTL (CF OR CKT)
23.28 FP MPY 3RD STEP ADDER(9) CARRY
122t.31 15 (D1)
FP EXCESSIVE CHAR DIFF
FP DIV 1ST STEP ADDER(9) CARRY
122k.18 E/R 10 (D1)
59.04 SHIFT ACC (9-35) RIGHT
58.06 SHIFT ACC (9-35) LEFT
57a.02 ADDER (9-35) → ACC
30.07 AND TO ACC/STG
122a.31 IO (D4)
31.01 OR TO ACC
122a.48 EO (D4)*
30.15 AND TO STG CNTL
57a.06 ADDER (Q-8) → ACC
58.01 SHIFT ACC (Q-8) LEFT
59.02 SHIFT ACC (Q-8) RIGHT

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FIG. 7g

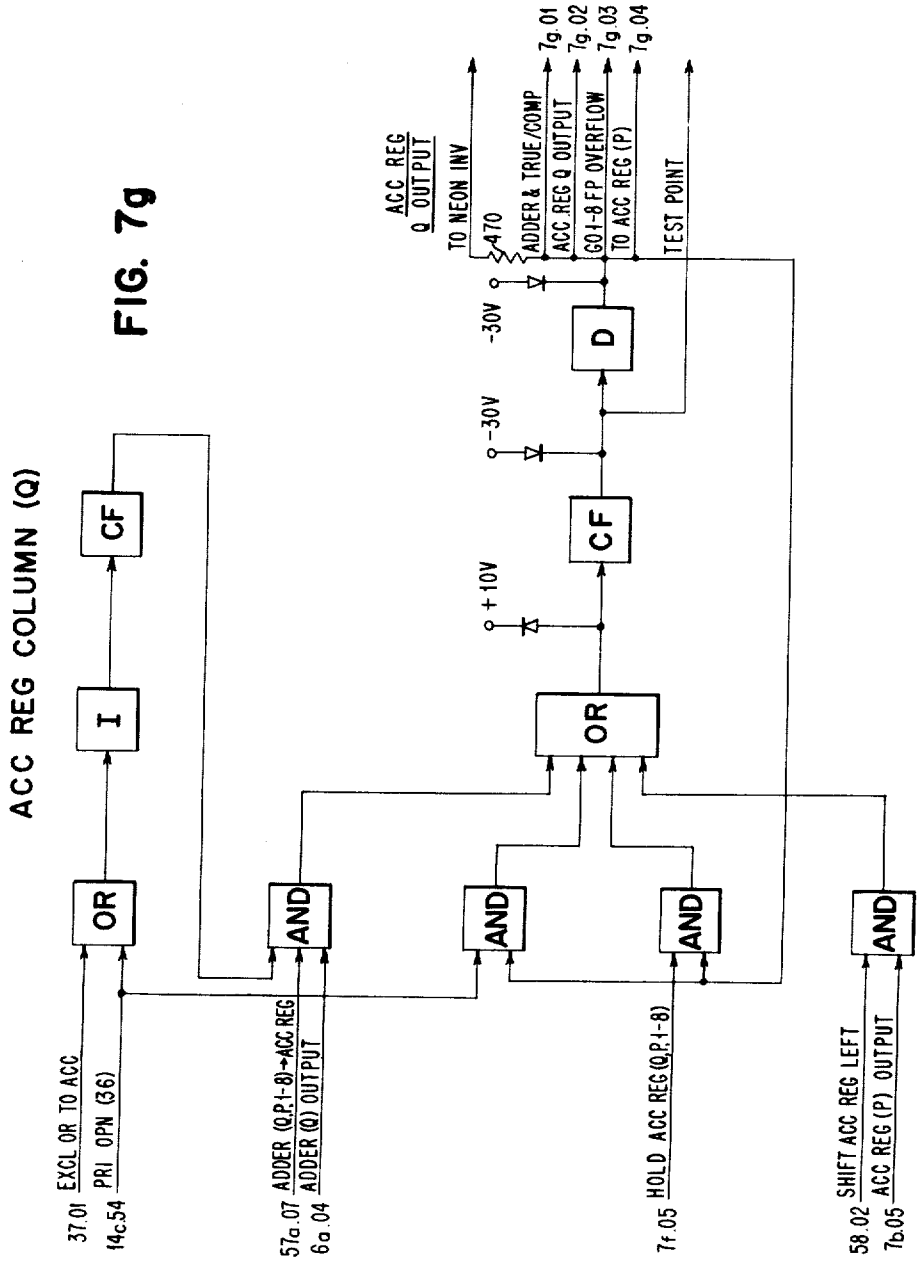


FIG. 8a

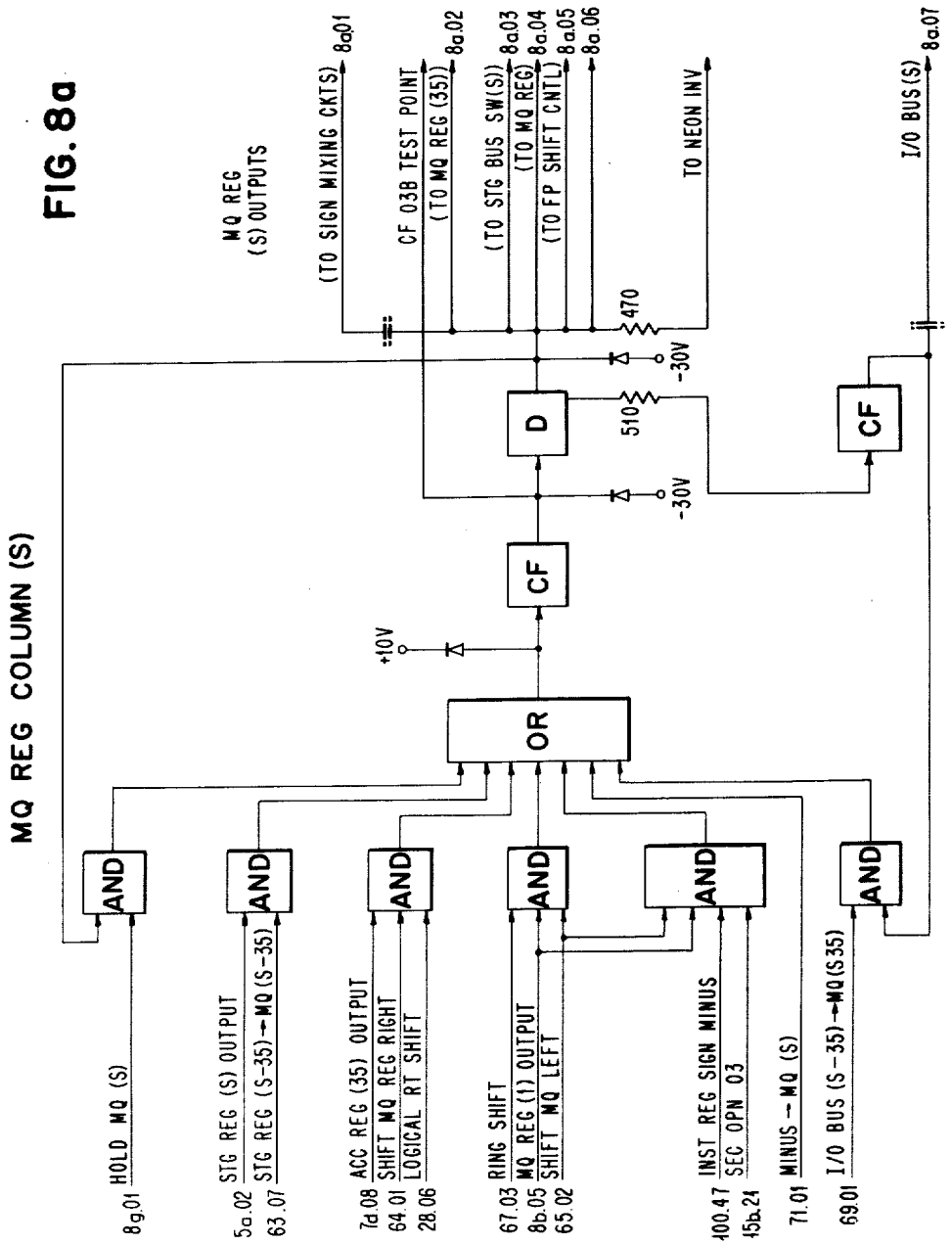
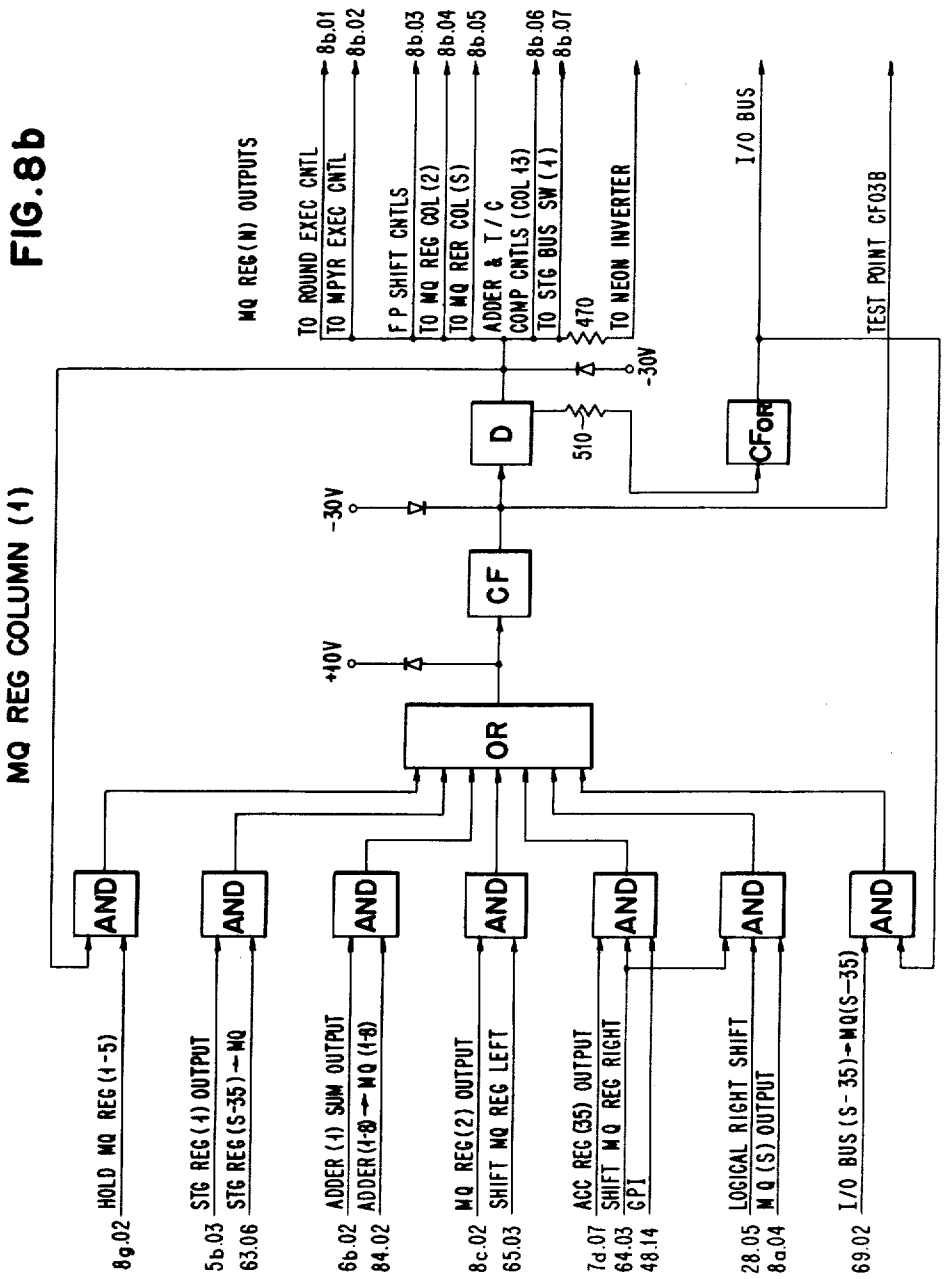

MQ REG COLUMN (S)
MQ REG (S) OUTPUTS
(TO SIGN MIXING CKTS) 8a.01
CF 03B TEST POINT (TO MQ REG (35)) 8a.02
(TO STG BUS SW(S)) 8a.03
(TO MQ REG) 8a.04
(TO FP SHIFT CNTL) 8a.05
8a.06
TO NEON INV
I/O BUS(S) 8a.07
470
-30V
510
D
CF
-30V
CF
+10V
OR
AND
8g.01 HOLD MQ (S)
5a.02 STG REG (S) OUTPUT
63.07 STG REG (S-35)→MQ (S-35)
7d.08 ACC REG (35) OUTPUT
64.01 SHIFT MQ REG RIGHT
28.06 LOGICAL RT SHIFT
67.03 RING SHIFT
8b.05 MQ REG (1) OUTPUT
65.02 SHIFT MQ LEFT
400.47 INST REG SIGN MINUS
45b.24 SEC OPN 03
71.01 MINUS→MQ (S)
69.01 I/O BUS (S-35)→MQ(S35)

FIG. 8b


MQ REG COLUMN (1)
MQ REG(N) OUTPUTS
TO ROUND EXEC CNTL
TO MPYR EXEC CNTL
F P SHIFT CNTLS
TO MQ REG COL (2)
TO MQ RER COL (S)
ADDER & T / C
COMP CNTLS (COL 43)
TO STG BUS SW (4)
TO NEON INVERTER
I/O BUS
TEST POINT CF03B
8b.01
8b.02
8b.03
8b.04
8b.05
8b.06
8b.07
470
-30V
510
D
CF
OR
+10V
AND
HOLD MQ REG (1-5)
8g.02
STG REG (4) OUTPUT
STG REG (S-35) → MQ
5b.03
63.06
ADDER (4) SUM OUTPUT
ADDER (1-8) → MQ (1-8)
6b.02
84.02
MQ REG (2) OUTPUT
SHIFT MQ REG LEFT
8c.02
65.03
ACC REG (35) OUTPUT
SHIFT M Q REG RIGHT
GPI
7d.07
64.03
48.14
LOGICAL RIGHT SHIFT
M Q (S) OUTPUT
28.05
8a.04
I/O BUS (S-35) → MQ (S-35)
69.02

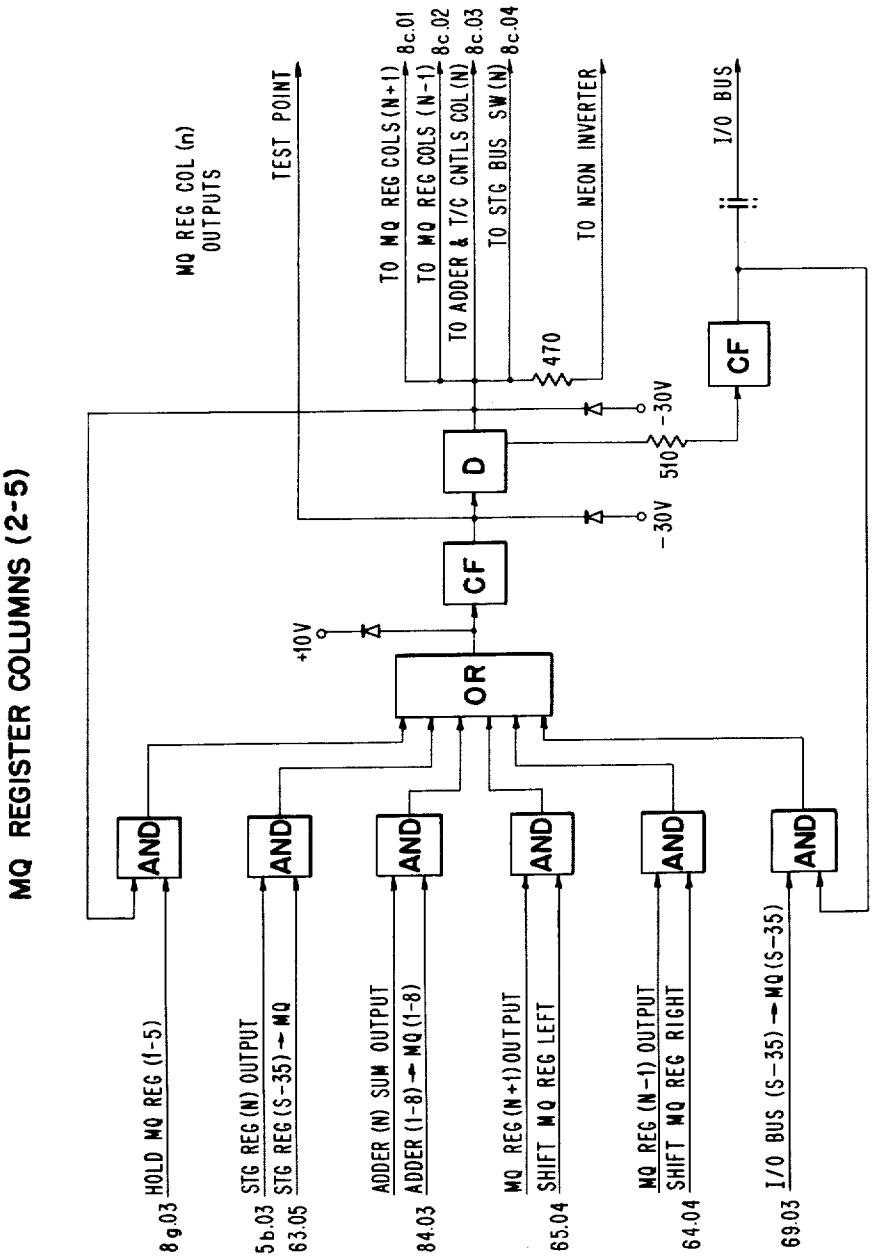

MQ REGISTER COLUMNS (2-5)
MQ REG COL (n) OUTPUTS
TEST POINT
TO MQ REG COLS (N+1) 8c.01
TO MQ REG COLS (N-1) 8c.02
TO ADDER & T/C CNTLS COL (N) 8c.03
TO STG BUS SW (N) 8c.04
TO NEON INVERTER
I/O BUS
470
510
-30V
-30V
+10V
CF
D
CF
OR
AND
AND
AND
AND
AND
AND
8g.03 HOLD MQ REG (1-5)
5b.03 STG REG (N) OUTPUT
63.05 STG REG (S-35) → MQ
84.03 ADDER (N) SUM OUTPUT
ADDER (1-8) → MQ (1-8)
65.04 MQ REG (N+1) OUTPUT
SHIFT MQ REG LEFT
64.04 MQ REG (N-1) OUTPUT
SHIFT MQ REG RIGHT
69.03 I/O BUS (S-35) → MQ (S-35)

FIG. 8c

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FIG. 8d

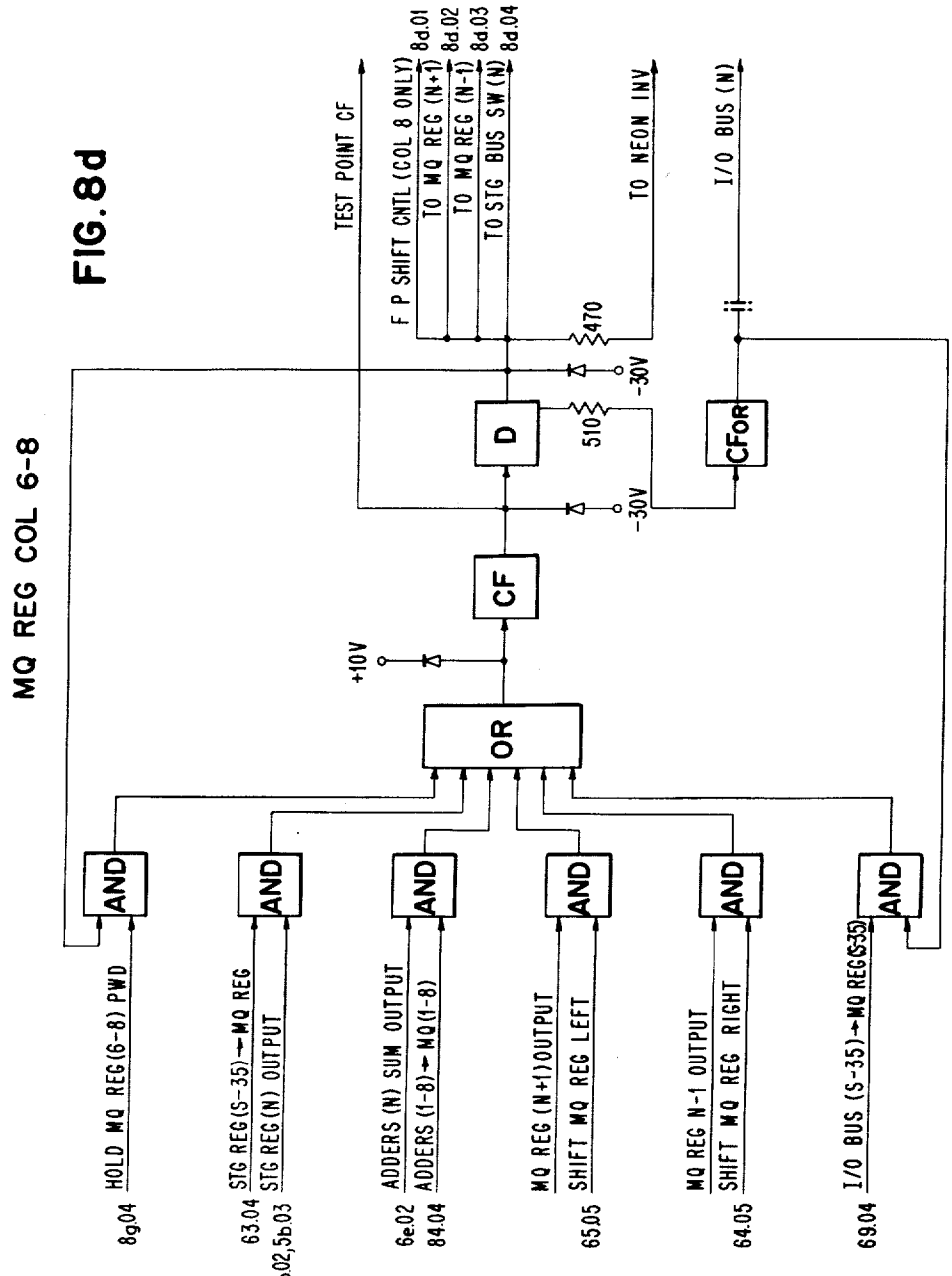


FIG. 8e

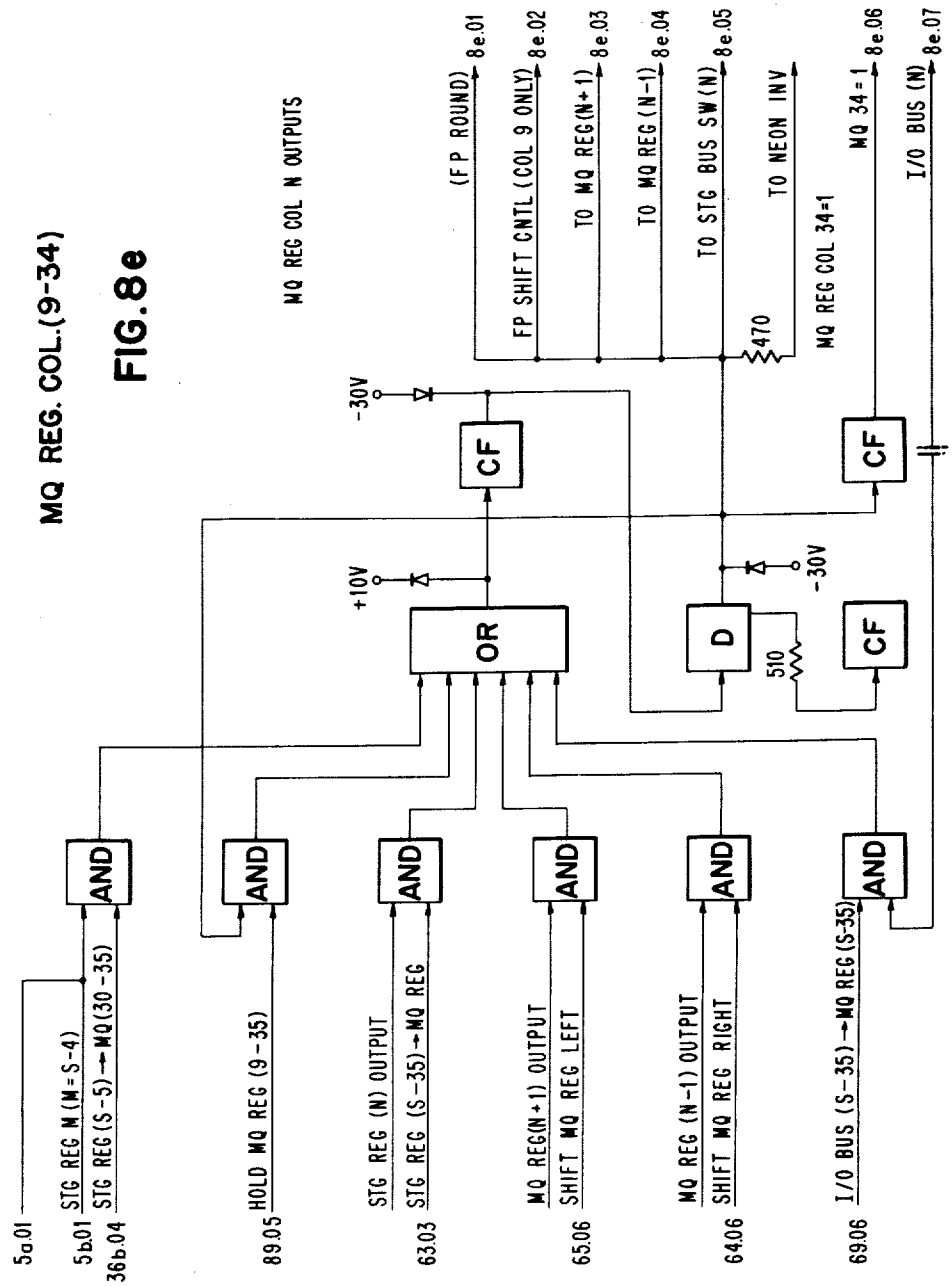

MQ REG. COL.(9-34)
MQ REG COL N OUTPUTS
(F P ROUND) 8e.01
FP SHIFT CNTL (COL 9 ONLY) 8e.02
TO MQ REG(N+1) 8e.03
TO MQ REG (N-1) 8e.04
TO STG BUS SW(N) 8e.05
TO NEON INV
MQ REG COL 34=1
MQ 34=1 8e.06
I/O BUS (N) 8e.07
-30V
+10V
CF
OR
D
AND
470
510
5a.01
5b.01 STG REG M (M=S-4)
36b.04 STG REG (S-5)→MQ (30-35)
89.05 HOLD MQ REG (9-35)
63.03 STG REG (N) OUTPUT
STG REG (S-35)→MQ REG
65.06 MQ REG(N+1) OUTPUT
SHIFT MQ REG LEFT
64.06 MQ REG (N-1) OUTPUT
SHIFT MQ REG RIGHT
69.06 I/O BUS (S-35)→MQ REG (S-35)

FIG. 8f

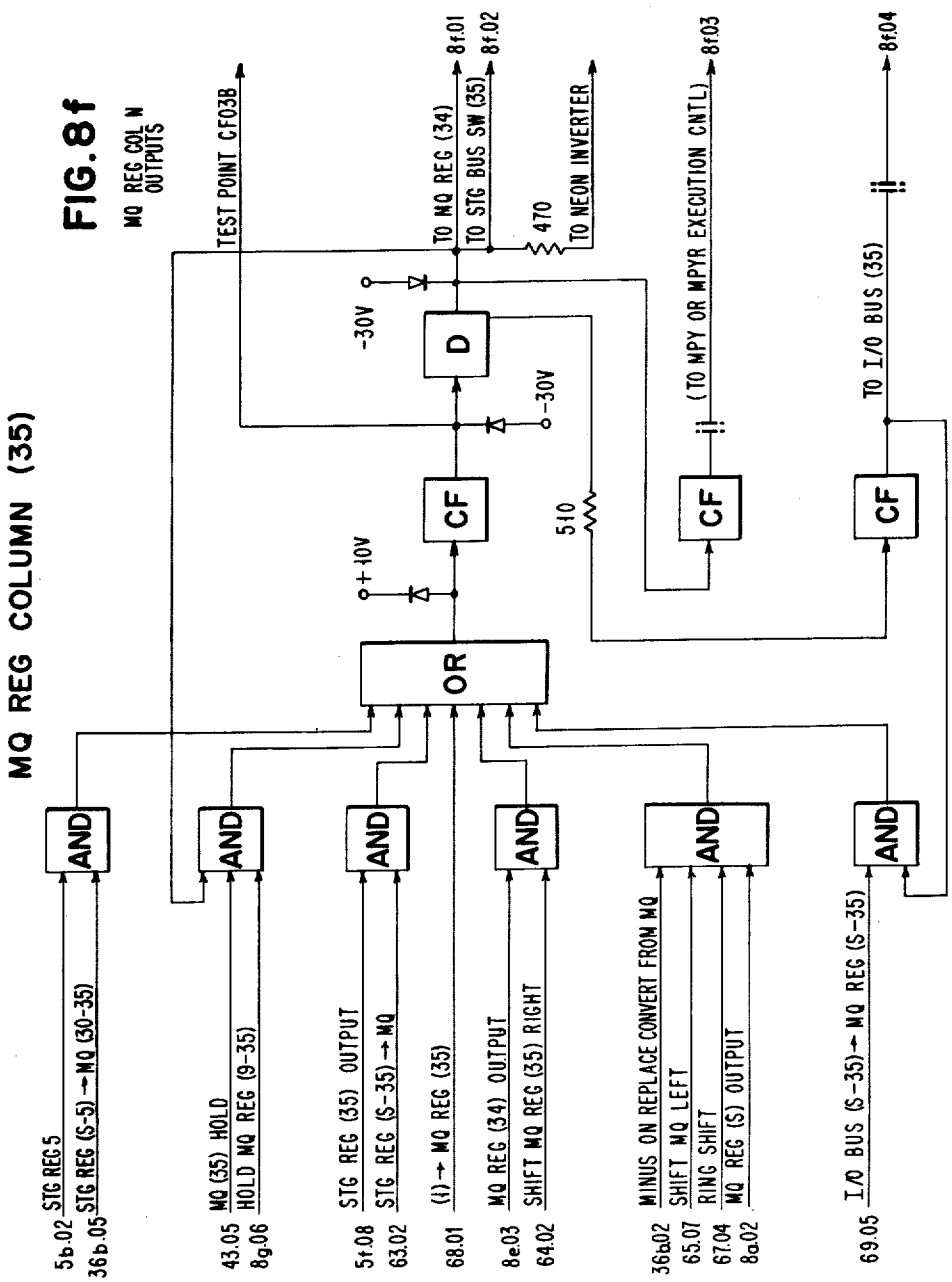
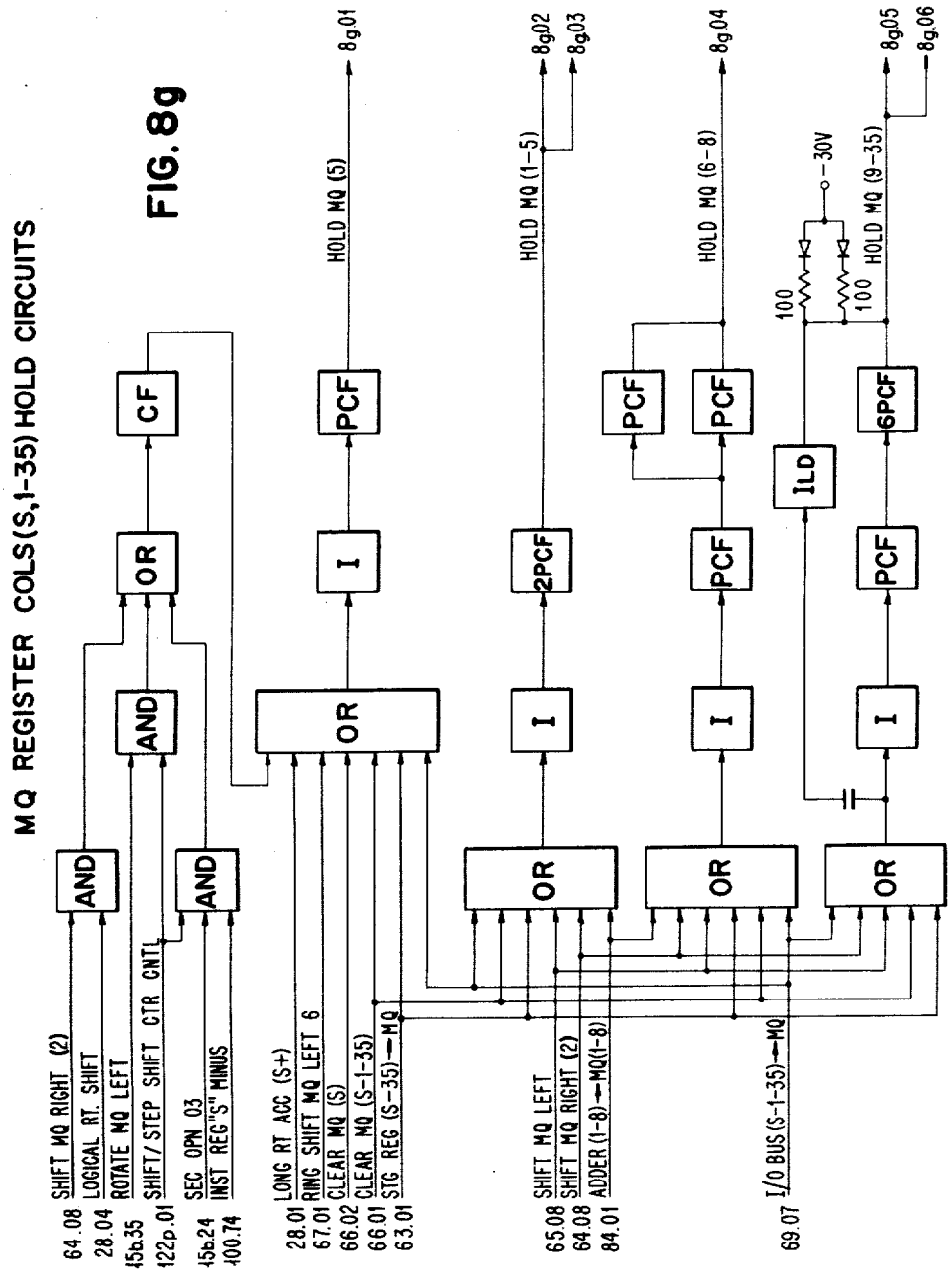

MQ REG COLUMN (35)
MQ REG COL N OUTPUTS
TEST POINT CF03B
TO MQ REG (34) 8f.01
TO STG BUS SW (35) 8f.02
470
TO NEON INVERTER
-30V
D
-30V
(TO MPY OR MPYR EXECUTION CNTL) 8f.03
TO I/O BUS (35) 8f.04
+10V
CF
510
CF
CF
OR
AND
AND
AND
AND
AND
AND
5b.02 STG REG 5
36b.05 STG REG (S-5) → MQ (30-35)
43.05 MQ (35) HOLD
8g.06 HOLD MQ REG (9-35)
5f.08 STG REG (35) OUTPUT
63.02 STG REG (S-35) → MQ
68.01 (1) → MQ REG (35)
8e.03 MQ REG (34) OUTPUT
64.02 SHIFT MQ REG (35) RIGHT
36a.02 MINUS ON REPLACE CONVERT FROM MQ
65.07 SHIFT MQ LEFT
67.04 RING SHIFT
8a.02 MQ REG (S) OUTPUT
69.05 I/O BUS (S-35) → MQ REG (S-35)

FIG. 8g


MQ REGISTER COLS(S,1-35) HOLD CIRCUITS
64.08 SHIFT MQ RIGHT (2)
28.04 LOGICAL RT. SHIFT
45b.35 ROTATE MQ LEFT
122p.01 SHIFT/STEP SHIFT CTR CNTL
45b.24 SEC OPN 03
100.74 INST REG"S" MINUS
AND
AND
OR
CF
AND
28.01 LONG RT ACC (S+)
67.01 RING SHIFT MQ LEFT 6
66.02 CLEAR MQ (S)
66.01 CLEAR MQ (S-1-35)
63.01 STG REG (S-35)→MQ
OR
I
PCF
HOLD MQ (5)
8g.01
65.08 SHIFT MQ LEFT
64.08 SHIFT MQ RIGHT (2)
84.01 ADDER (1-8)→MQ(1-8)
OR
I
2PCF
HOLD MQ (1-5)
8g.02
8g.03
69.07 I/O BUS (S-1-35)→MQ
OR
I
PCF
PCF
HOLD MQ (6-8)
8g.04
OR
I
PCF
PCF
ILD
100
-30V
100
HOLD MQ (9-35)
8g.05
8g.06

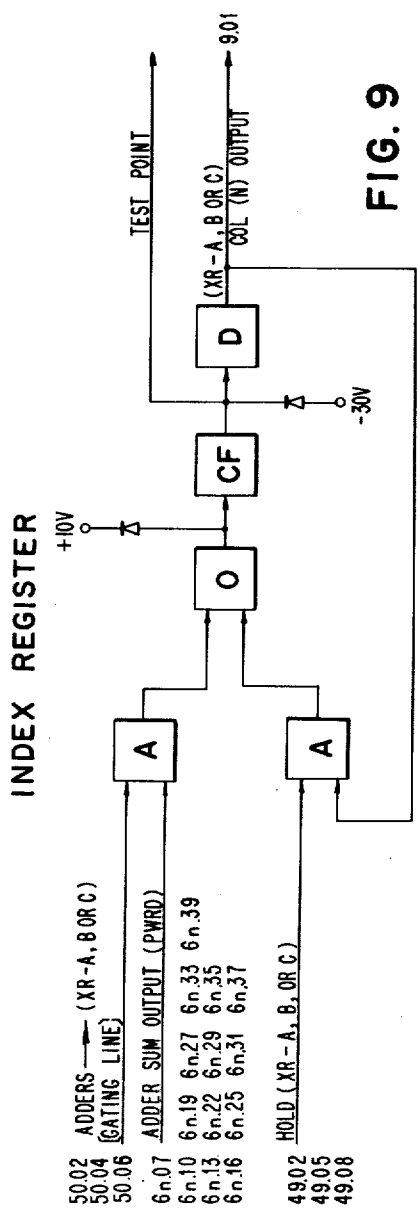

INDEX REGISTER
50.02 ADDERS (XR-A, B OR C)
50.04 (GATING LINE)
50.06
6n.07 ADDER SUM OUTPUT (PWRD)
6n.10 6n.19 6n.27 6n.33 6n.39
6n.13 6n.22 6n.29 6n.35
6n.16 6n.25 6n.31 6n.37
49.02 HOLD (XR-A, B, OR C)
49.05
49.08
A
A
O
CF
D
+10V
-30V
TEST POINT
(XR-A, B OR C) COL (N) OUTPUT
9.01

FIG. 9

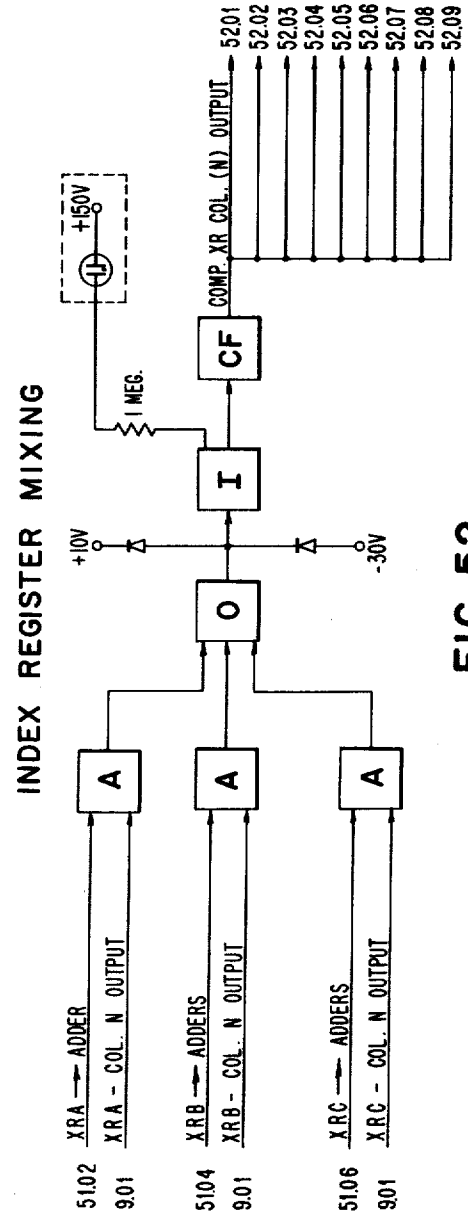

INDEX REGISTER MIXING
51.02 XRA ADDER
9.01 XRA - COL. N OUTPUT
51.04 XRB ADDERS
9.01 XRB - COL. N OUTPUT
51.06 XRC ADDERS
9.01 XRC - COL. N OUTPUT
A
A
A
O
I
CF
+10V
-30V
+150V
1 MEG.
COMP. XR COL. (N) OUTPUT
52.01
52.02
52.03
52.04
52.05
52.06
52.07
52.08
52.09

FIG. 52

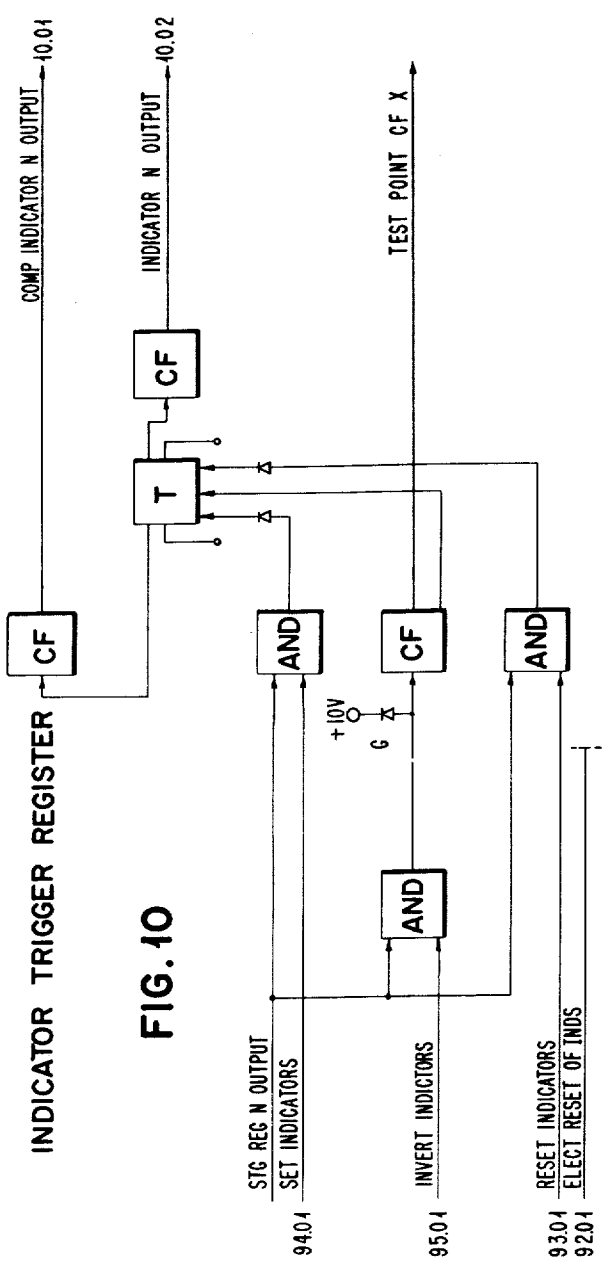

INDICATOR TRIGGER REGISTER
CF
COMP INDICATOR N OUTPUT 10.01
INDICATOR N OUTPUT 10.02
CF
T
TEST POINT CF X
AND
CF
AND
+10V
G
AND
STG REG N OUTPUT
SET INDICATORS
94.01
INVERT INDICTORS
95.01
RESET INDICATORS
ELECT RESET OF INDS
93.01
92.01

FIG. 10

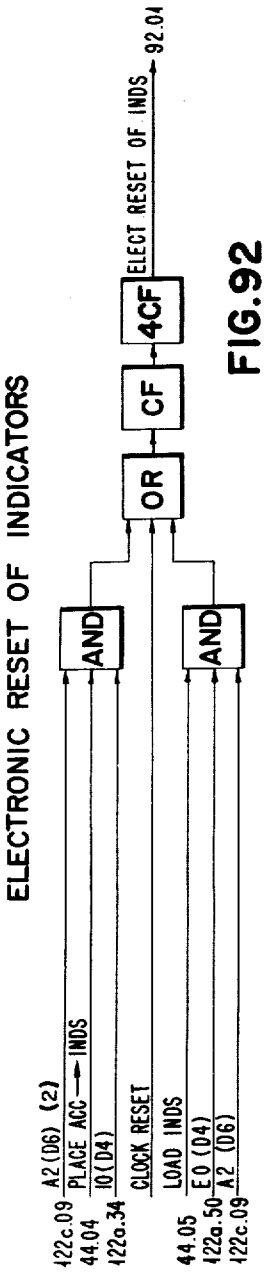
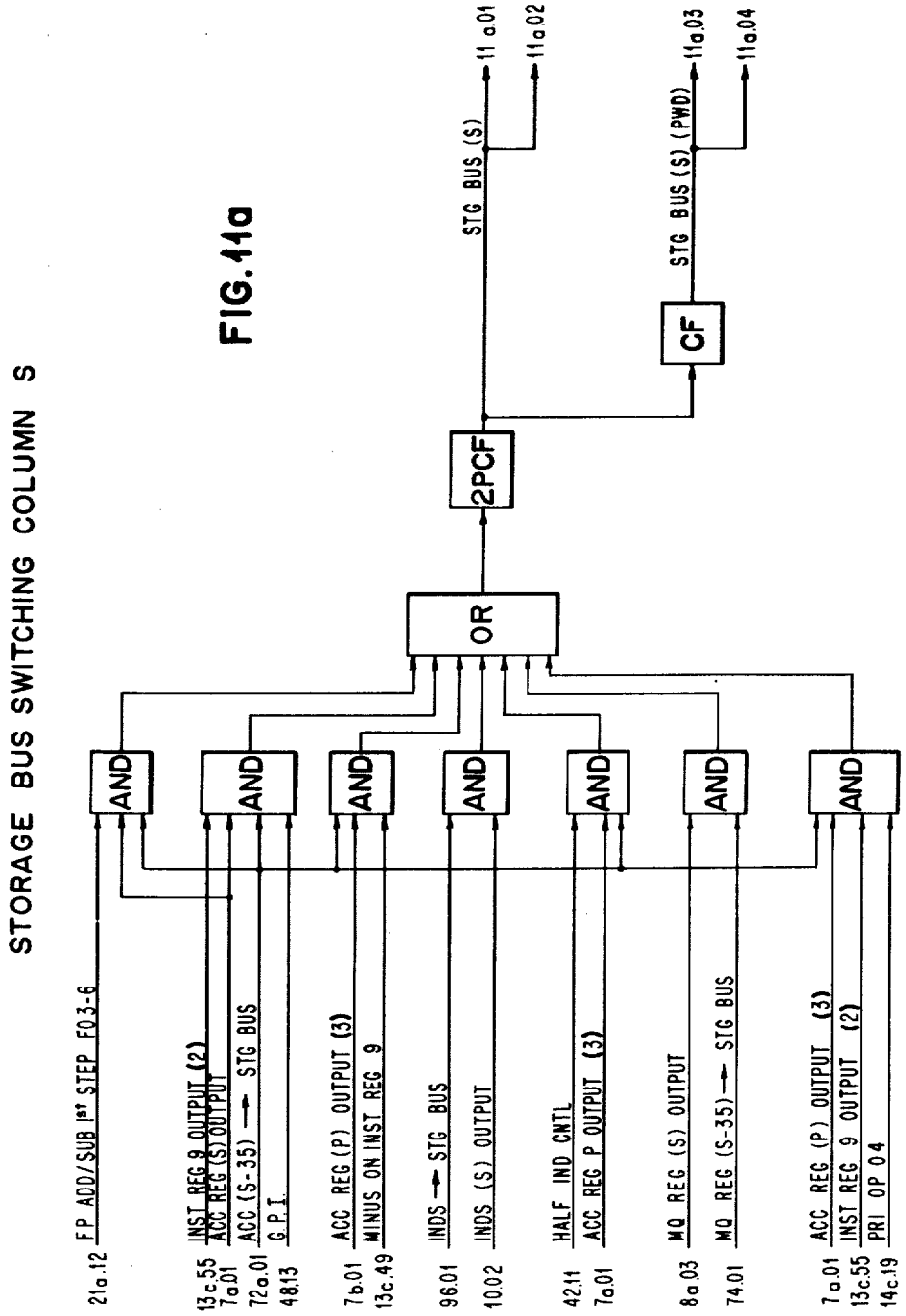

ELECTRONIC RESET OF INDICATORS
AND
AND
AND
OR
CF
4CF
ELECT RESET OF INDS 92.04
122c.09 A2 (D6) (2)
44.04 PLACE ACC → INDS
122a.34 10 (D4)
CLOCK RESET
44.05 LOAD INDS
122a.50 E0 (D4)
122c.09 A2 (D6)

FIG. 92

FIG. 11a


STORAGE BUS SWITCHING COLUMN S
STG BUS (S)
11 a.01
11a.02
STG BUS (S) (PWD)
11a.03
11a.04
CF
2PCF
OR
AND
AND
AND
AND
AND
AND
AND
21a.12 FP ADD/SUB 1st STEP F03-6
13c.55 INST REG 9 OUTPUT (2)
7a.01 ACC REG (S) OUTPUT
72a.01 ACC (S-35) → STG BUS
48.13 G.P.I.
7b.01 ACC REG (P) OUTPUT (3)
13c.49 MINUS ON INST REG 9
96.01 INDS → STG BUS
10.02 INDS (S) OUTPUT
42.11 HALF IND CNTL
7a.01 ACC REG P OUTPUT (3)
8a.03 MQ REG (S) OUTPUT
74.01 MQ REG (S-35) → STG BUS
7a.01 ACC REG (P) OUTPUT (3)
13c.55 INST REG 9 OUTPUT (2)
14c.19 PRI OP 04

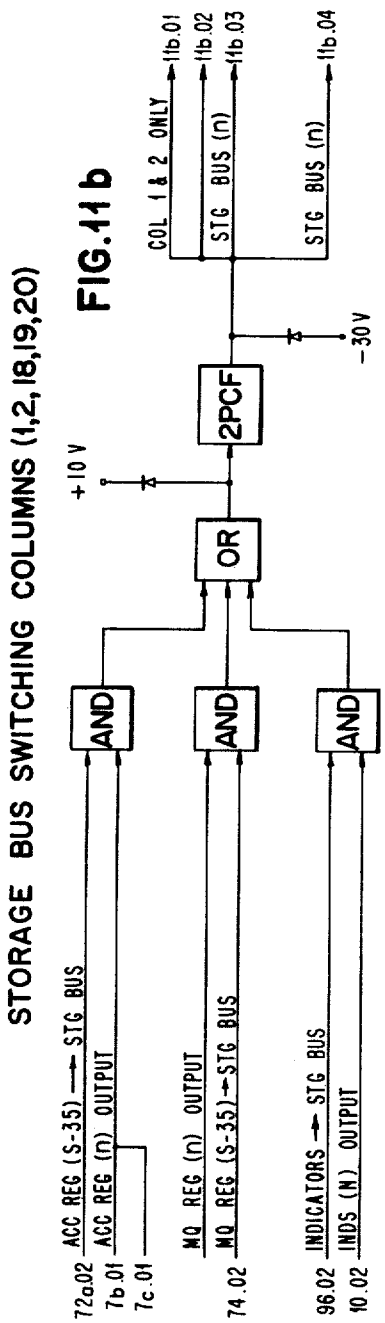


FIG. 11b

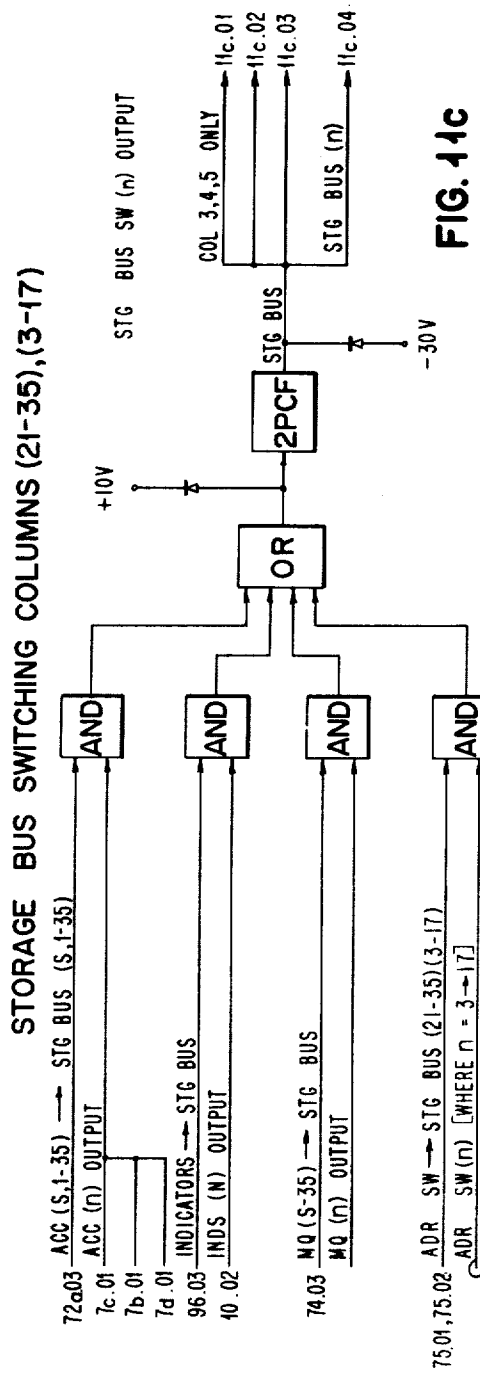


FIG. 11c

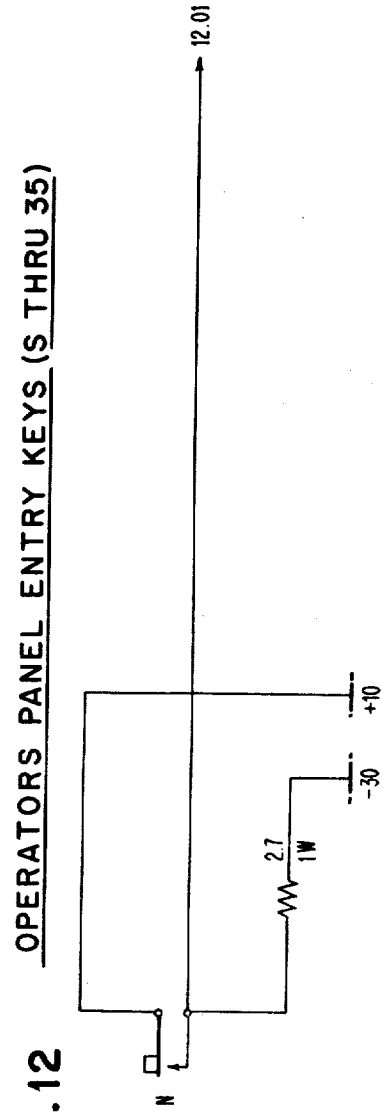


FIG. 12

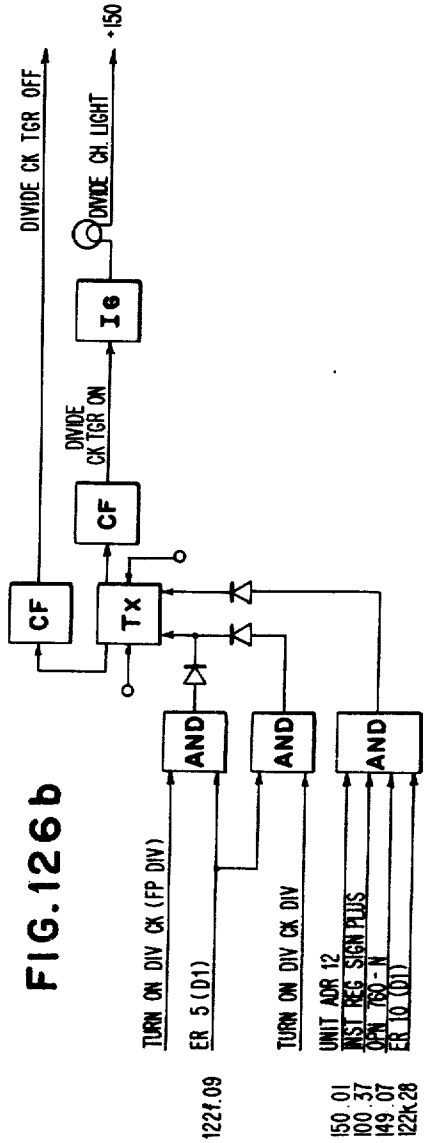
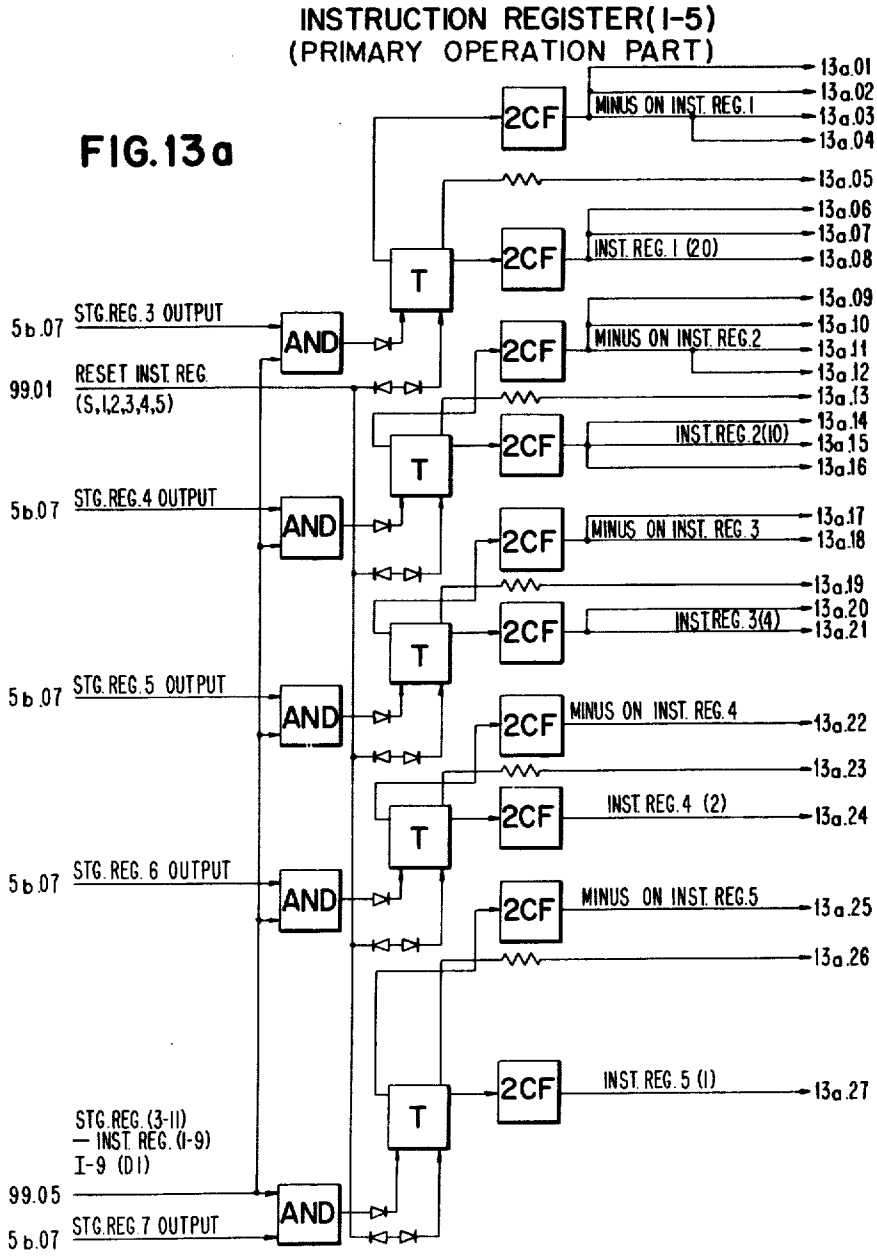


FIG. 126b

FIG. 13a


INSTRUCTION REGISTER(I-5)
(PRIMARY OPERATION PART)
5b.07 STG.REG.3 OUTPUT
99.01 RESET INST.REG. (S,1,2,3,4,5)
5b.07 STG.REG.4 OUTPUT
5b.07 STG.REG.5 OUTPUT
5b.07 STG.REG.6 OUTPUT
STG.REG.(3-11) — INST.REG.(1-9) I-9 (D1)
99.05
5b.07 STG.REG.7 OUTPUT
AND
T
2CF
MINUS ON INST.REG.1
INST.REG.1 (20)
MINUS ON INST.REG.2
INST.REG.2(10)
MINUS ON INST.REG.3
INST.REG.3(4)
MINUS ON INST.REG.4
INST.REG.4 (2)
MINUS ON INST.REG.5
INST.REG.5 (1)
13a.01
13a.02
13a.03
13a.04
13a.05
13a.06
13a.07
13a.08
13a.09
13a.10
13a.11
13a.12
13a.13
13a.14
13a.15
13a.16
13a.17
13a.18
13a.19
13a.20
13a.21
13a.22
13a.23
13a.24
13a.25
13a.26
13a.27

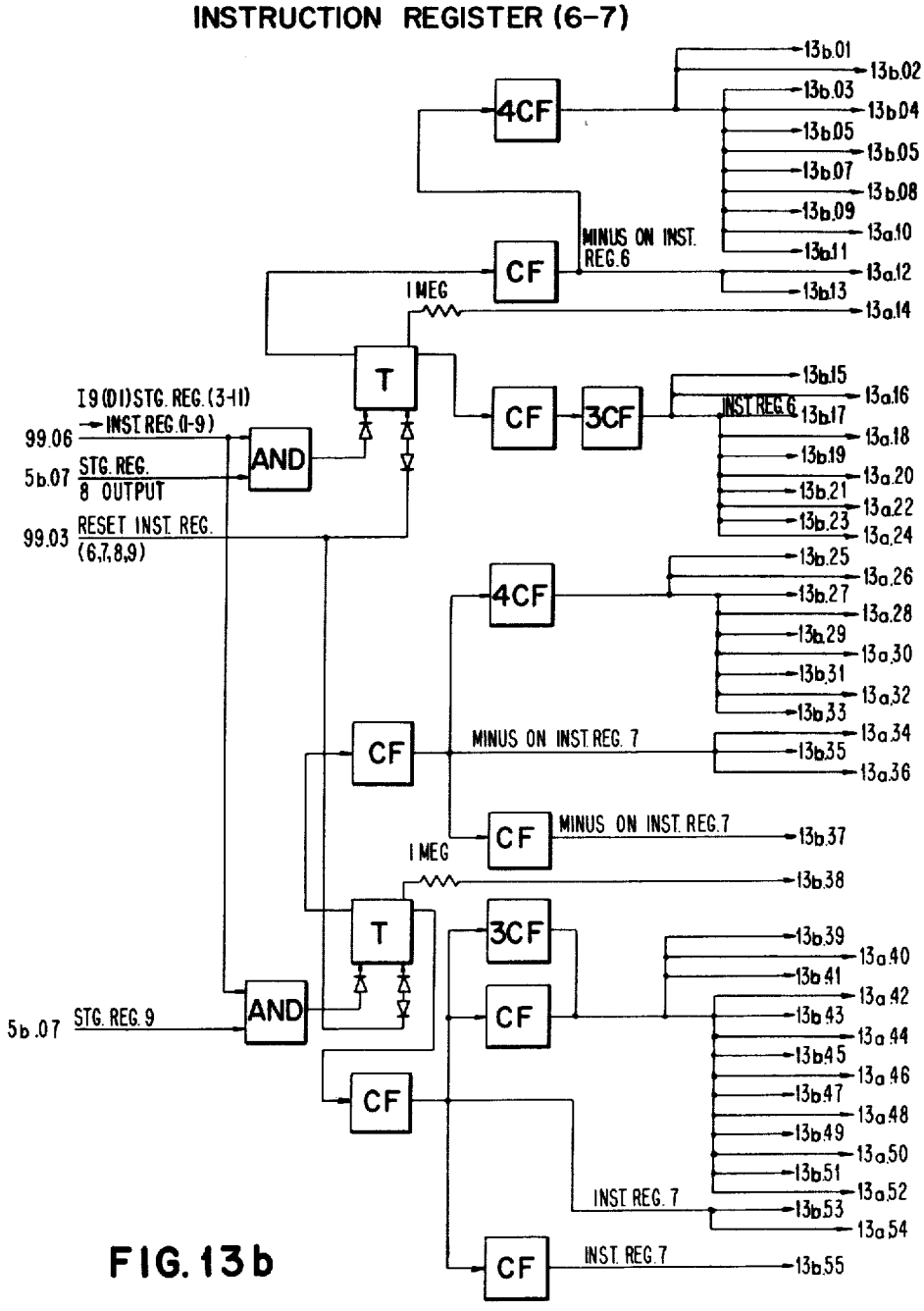

INSTRUCTION REGISTER (6-7)
4CF
13b.01
13b.02
13b.03
13b.04
13b.05
13b.05
13b.07
13b.08
13b.09
13a.10
13b.11
13a.12
13b.13
13a.14
MINUS ON INST. REG.6
CF
1 MEG
T
13b.15
13a.16
13b.17
13a.18
13b.19
13a.20
13b.21
13a.22
13b.23
13a.24
INST REG.6
CF
3CF
I 9 (01) STG. REG. (3-11)
INST REG. (1-9)
99.06
5b.07
STG. REG. 8 OUTPUT
99.03
RESET INST. REG. (6,7,8,9)
AND
4CF
13b.25
13a.26
13b.27
13a.28
13b.29
13a.30
13b.31
13a.32
13b.33
13a.34
13b.35
13a.36
CF
MINUS ON INST. REG. 7
CF
MINUS ON INST. REG.7
13b.37
1 MEG
13b.38
T
3CF
13b.39
13a.40
13b.41
13a.42
13b.43
13a.44
13b.45
13a.46
13b.47
13a.48
13b.49
13a.50
13b.51
13a.52
13b.53
13a.54
5b.07
STG. REG. 9
AND
CF
CF
INST. REG. 7
CF
INST. REG. 7
13b.55

FIG. 13b

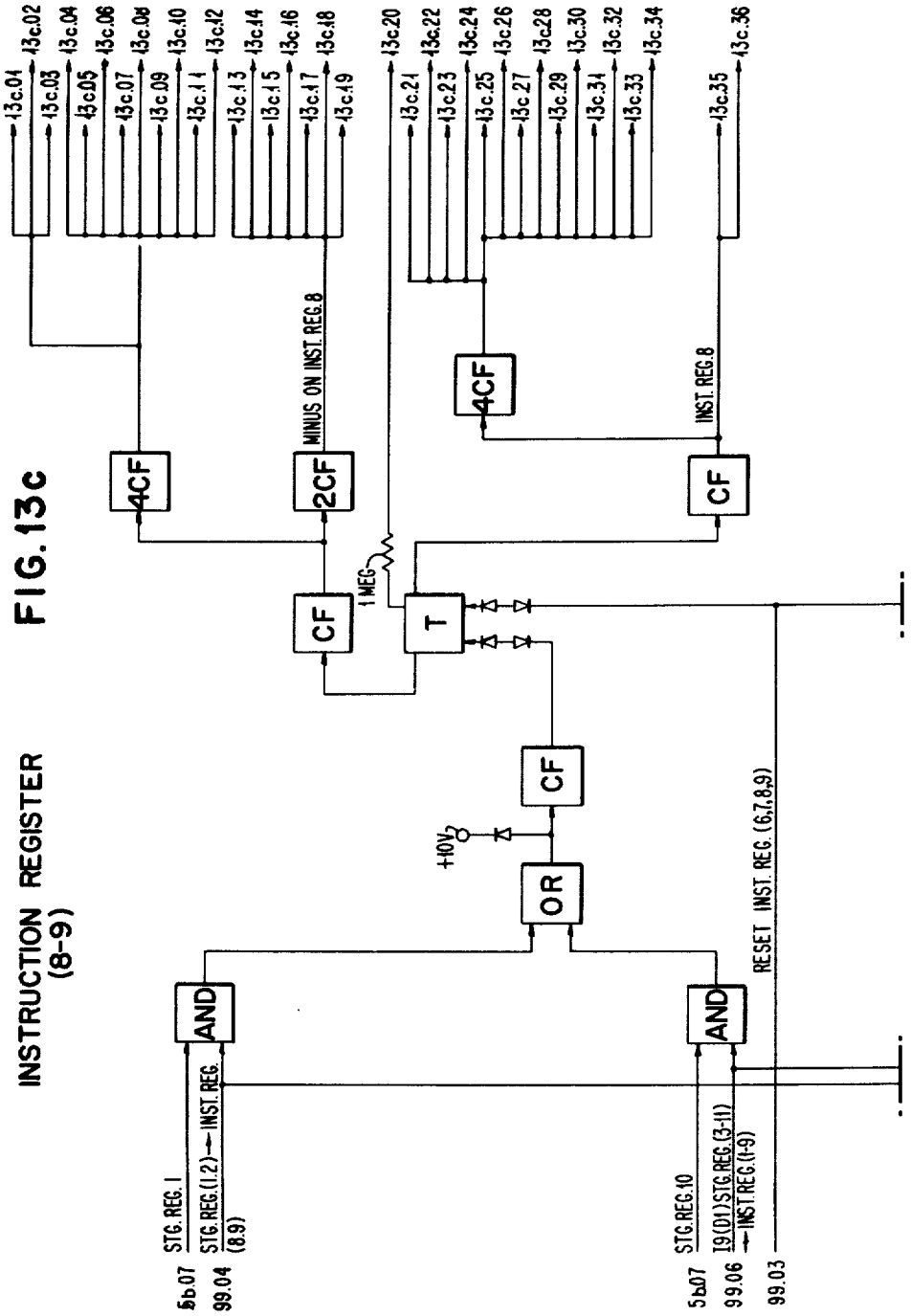


FIG. 13c

INSTRUCTION REGISTER (8-9)

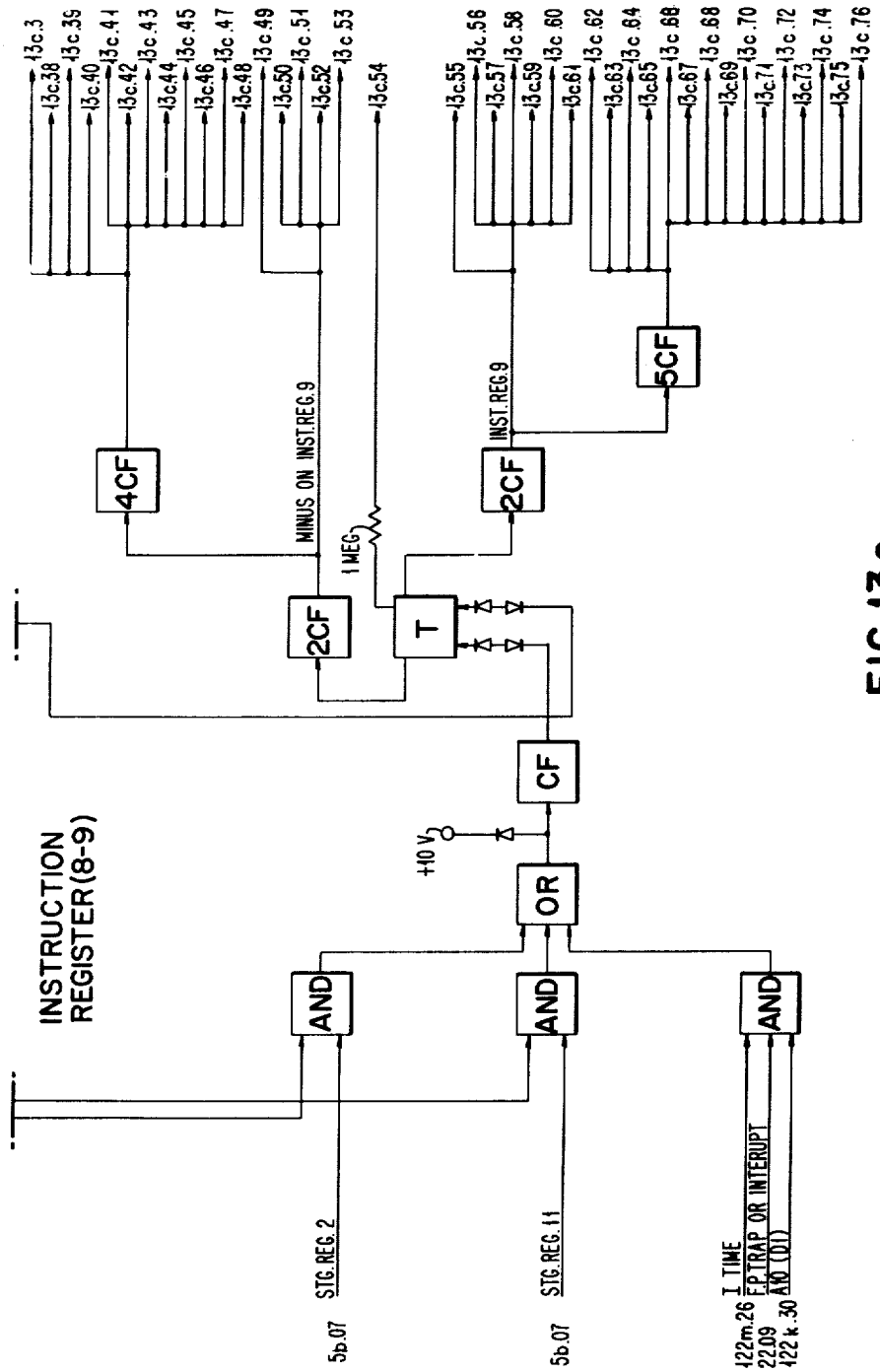

13c.3
13c.38
13c.39
13c.40
13c.41
13c.42
13c.43
13c.44
13c.45
13c.46
13c.47
13c.48
13c.49
13c.50
13c.51
13c.52
13c.53
13c.54
13c.55
13c.56
13c.57
13c.58
13c.59
13c.60
13c.61
13c.62
13c.63
13c.64
13c.65
13c.66
13c.67
13c.68
13c.69
13c.70
13c.71
13c.72
13c.73
13c.74
13c.75
13c.76
4CF
MINUS ON INST.REG.9
1 MEG
2CF
T
INST.REG.9
2CF
5CF
CF
+10 V
OR
AND
AND
AND
INSTRUCTION REGISTER(8-9)
STG.REG.2
5b.07
STG.REG.11
5b.07
122m.26 I TIME
22.09 F.P.TRAP OR INTERUPT
122 k.30 AND (01)

FIG. 13c

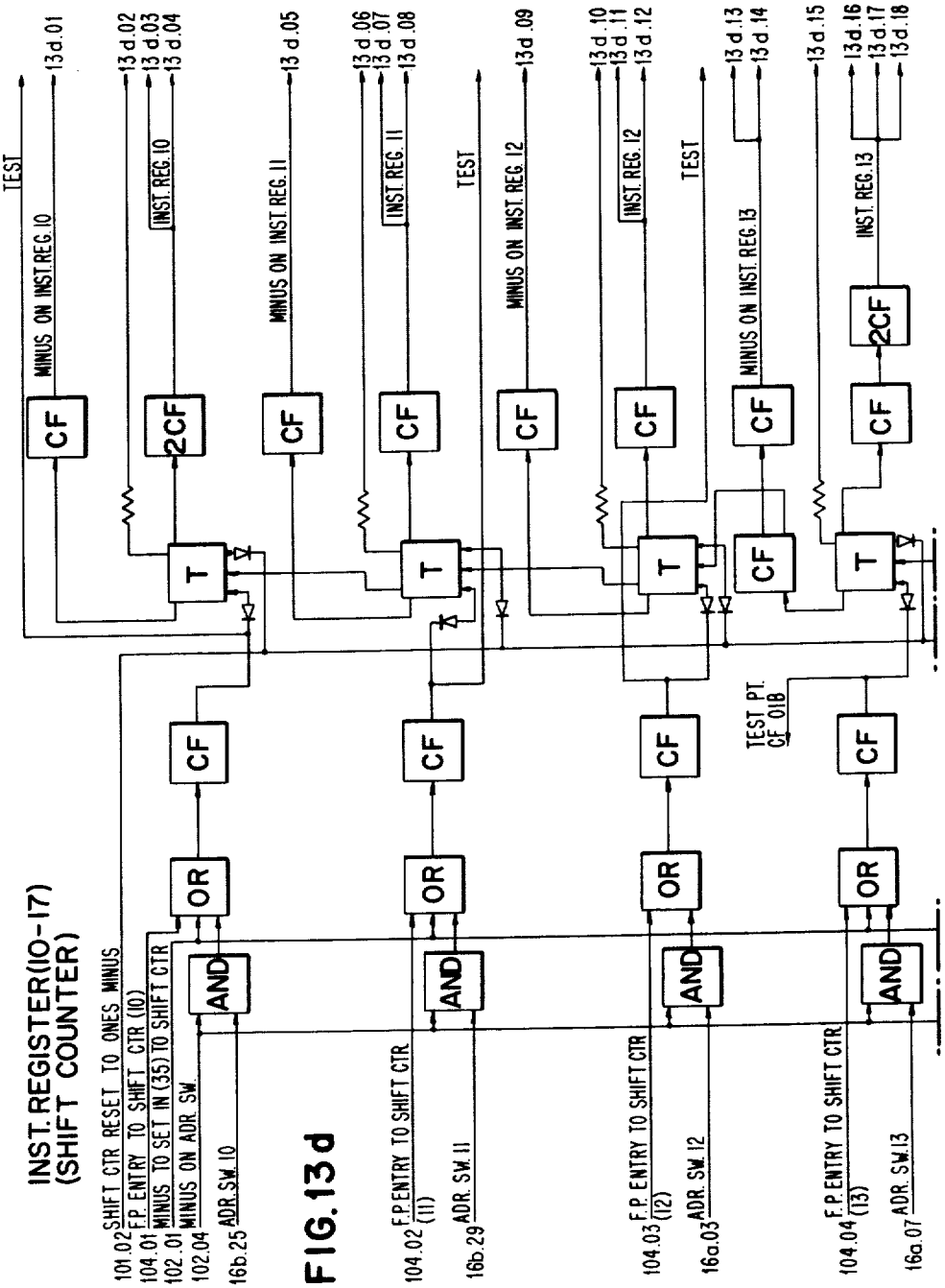

INST. REGISTER(IO-17)
(SHIFT COUNTER)
101.02 SHIFT CTR RESET TO ONES MINUS
104.01 F.P. ENTRY TO SHIFT CTR (10)
102.01 MINUS TO SET IN (35) TO SHIFT CTR
102.04 MINUS ON ADR SW
16b.25 ADR. SW. 10
104.02 F.P. ENTRY TO SHIFT CTR (11)
16b.29 ADR. SW. 11
104.03 F.P. ENTRY TO SHIFT CTR (12)
16a.03 ADR. SW. 12
104.04 F.P. ENTRY TO SHIFT CTR (13)
16a.07 ADR. SW. 13
TEST
MINUS ON INST. REG. 10
INST. REG. 10
MINUS ON INST. REG. 11
INST. REG. 11
MINUS ON INST. REG. 12
INST. REG. 12
MINUS ON INST. REG. 13
INST. REG. 13
13d.01
13d.02
13d.03
13d.04
13d.05
13d.06
13d.07
13d.08
13d.09
13d.10
13d.11
13d.12
13d.13
13d.14
13d.15
13d.16
13d.17
13d.18
CF
2CF
T
OR
AND
TEST PT. CF 01B

FIG. 13d

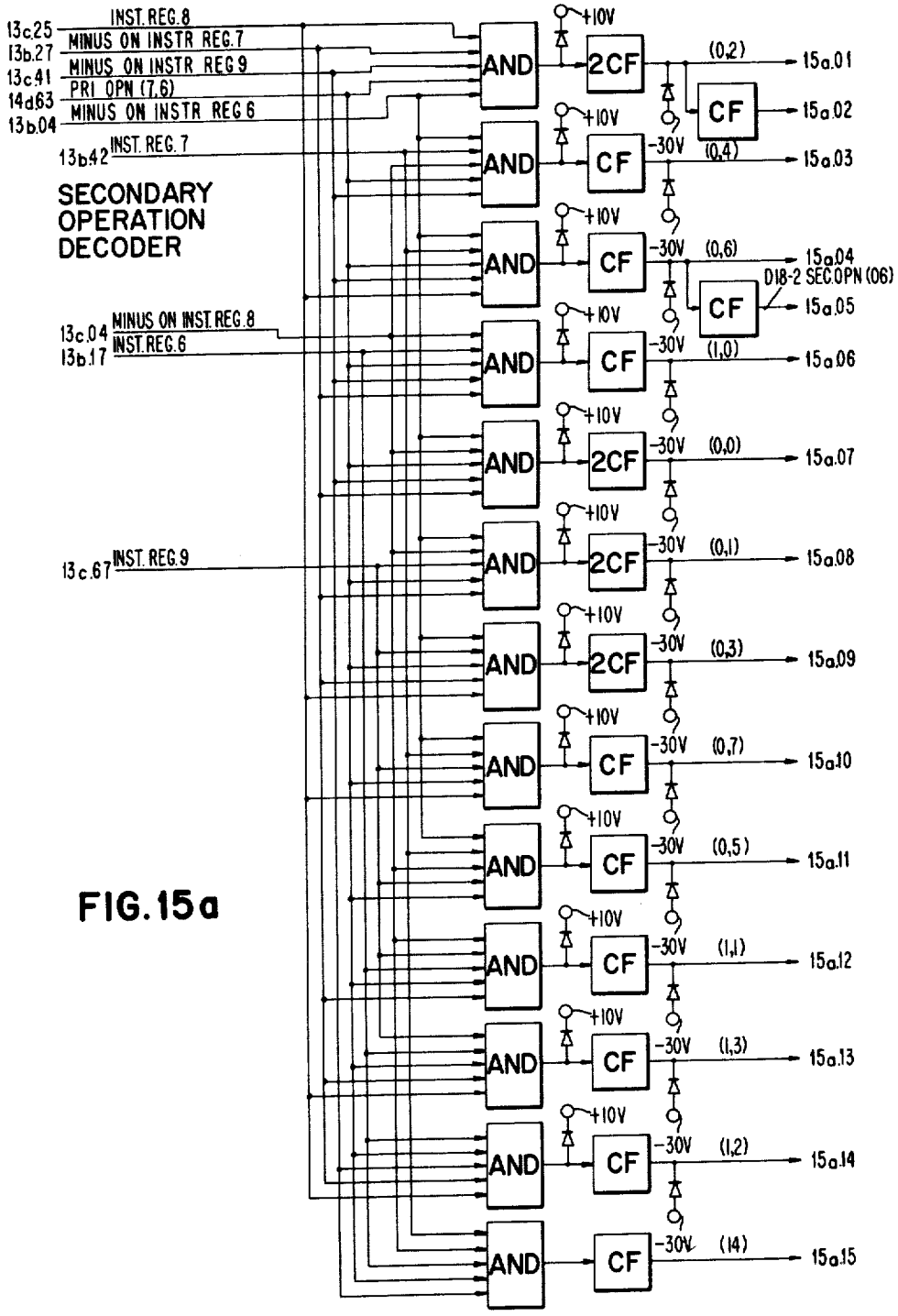

13c.25 INST. REG. 8
13b.27 MINUS ON INSTR REG. 7
13c.41 MINUS ON INSTR REG 9
14d.63 PRI OPN (7,6)
13b.04 MINUS ON INSTR REG 6
13b.42 INST. REG. 7
SECONDARY OPERATION DECODER
13c.04 MINUS ON INST. REG. 8
13b.17 INST. REG. 6
13c.67 INST. REG. 9
AND
2CF
CF
+10V
-30V
(0,2)
(0,4)
(0,6)
(1,0)
(0,0)
(0,1)
(0,3)
(0,7)
(0,5)
(1,1)
(1,3)
(1,2)
(14)
15a.01
15a.02
15a.03
15a.04
D18-2 SEC.OPN (06)
15a.05
15a.06
15a.07
15a.08
15a.09
15a.10
15a.11
15a.12
15a.13
15a.14
15a.15

FIG. 15a

SECONDARY OPERATION DECODER

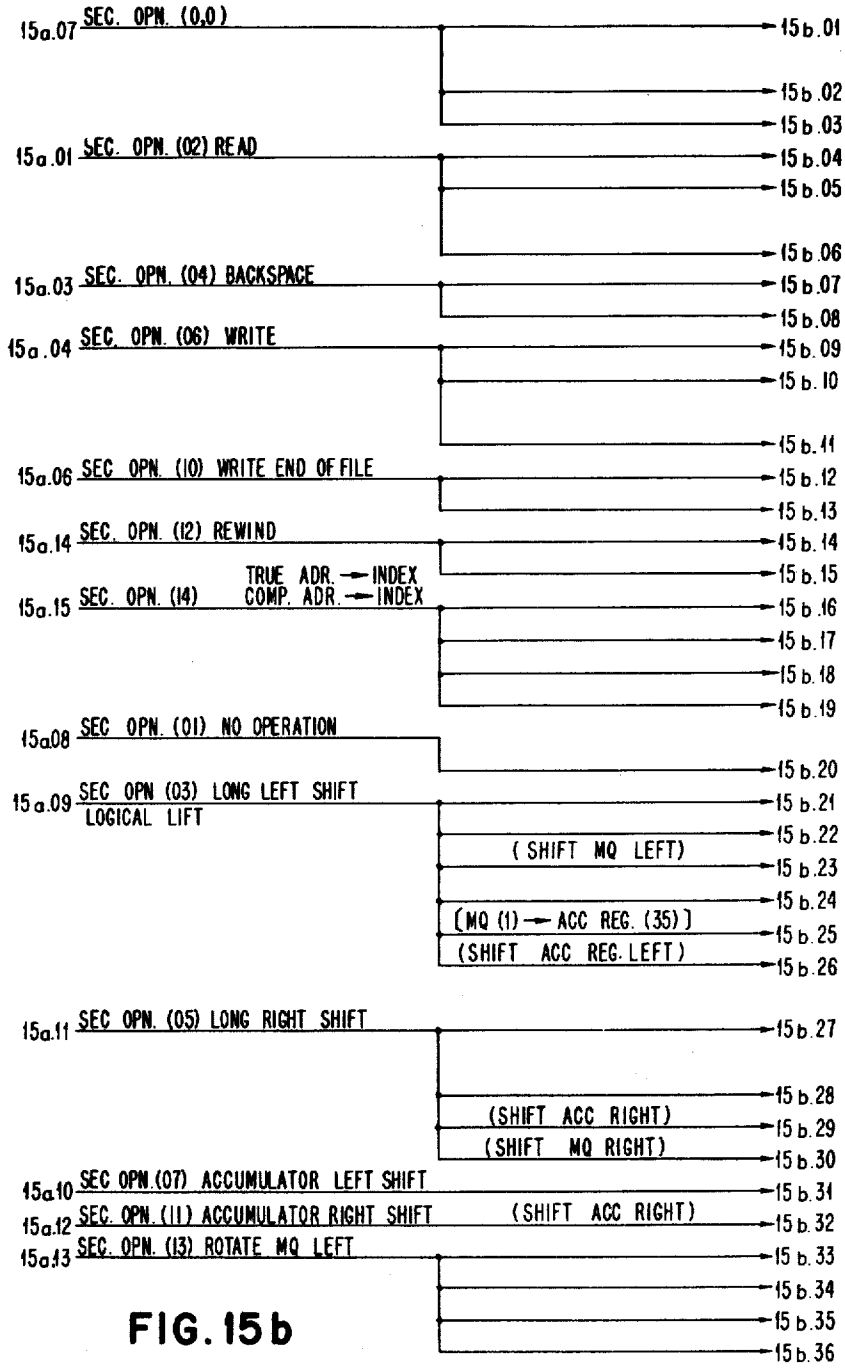


FIG. 15b

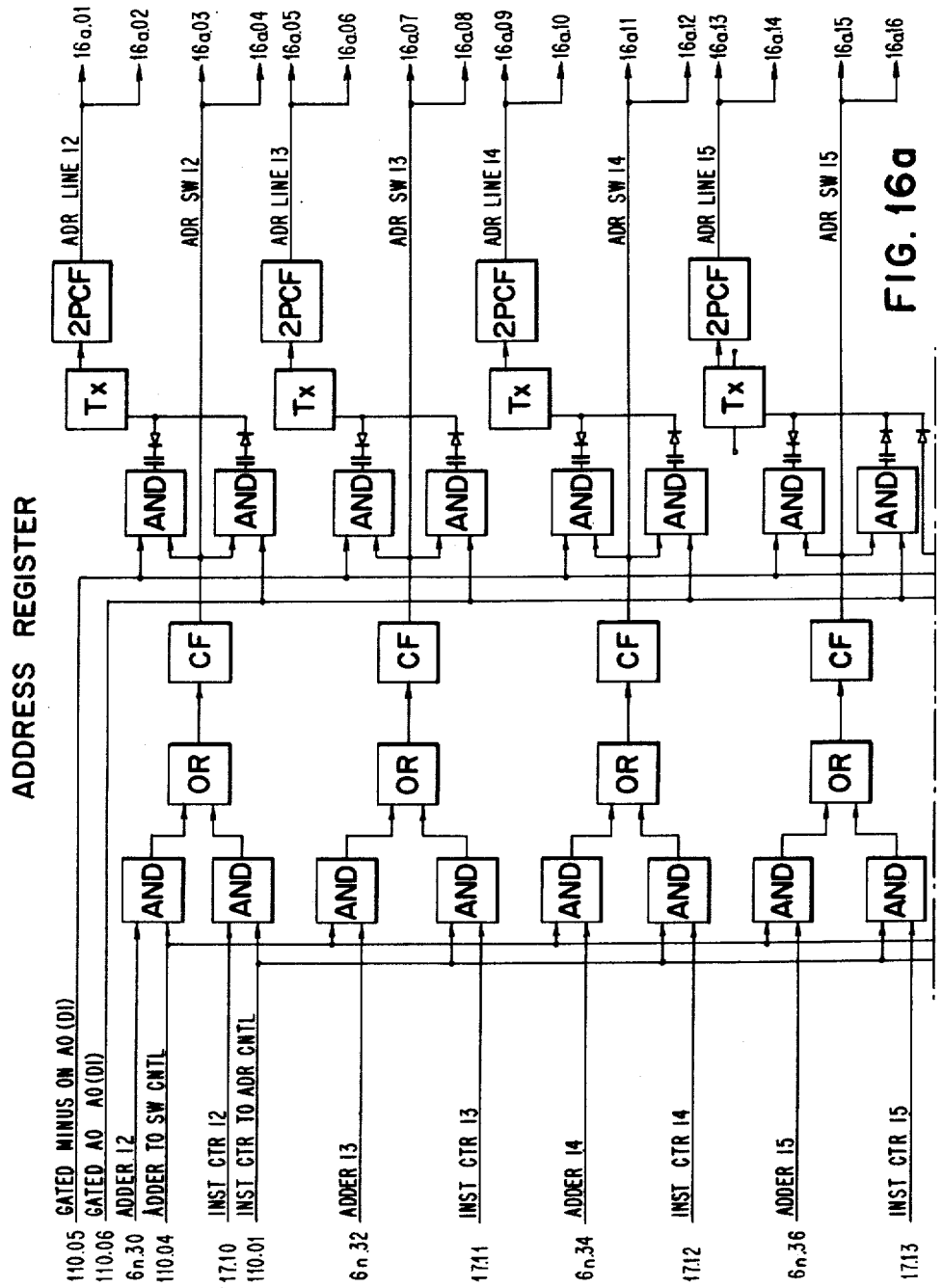

ADDRESS REGISTER
110.05 GATED MINUS ON A0 (01)
110.06 GATED A0 A0 (01)
6n.30 ADDER 12
110.04 ADDER TO SW CNTL
17.10 INST CTR 12
110.01 INST CTR TO ADR CNTL
6n.32 ADDER 13
17.11 INST CTR 13
6n.34 ADDER 14
17.12 INST CTR 14
6n.36 ADDER 15
17.13 INST CTR 15
AND
OR
CF
Tx
2PCF
ADR LINE 12
ADR SW 12
ADR LINE 13
ADR SW 13
ADR LINE 14
ADR SW 14
ADR LINE 15
ADR SW 15
16a.01
16a.02
16a.03
16a.04
16a.05
16a.06
16a.07
16a.08
16a.09
16a.10
16a.11
16a.12
16a.13
16a.14
16a.15
16a.16

FIG. 16a

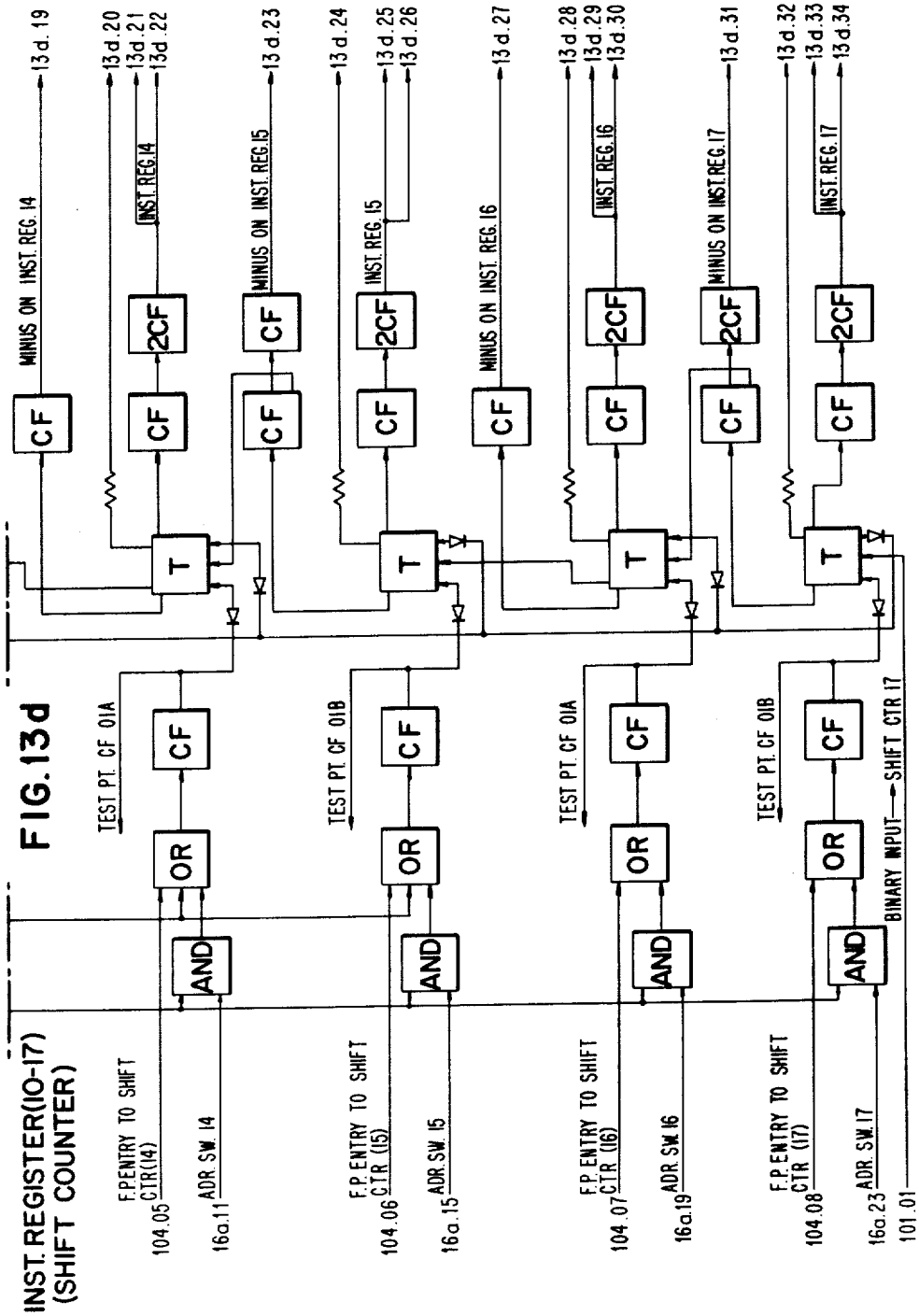

INST. REGISTER(10-17) (SHIFT COUNTER)
F.P. ENTRY TO SHIFT CTR (14)
104.05
ADR. SW. 14
16a.11
F.P. ENTRY TO SHIFT CTR (15)
104.06
ADR. SW. 15
16a.15
F.P. ENTRY TO SHIFT CTR (16)
104.07
ADR. SW. 16
16a.19
F.P. ENTRY TO SHIFT CTR (17)
104.08
ADR. SW. 17
16a.23
101.01
BINARY INPUT
SHIFT CTR. 17
TEST PT. CF 01A
TEST PT. CF 01B
TEST PT. CF 01A
TEST PT. CF 01B
AND
OR
CF
2CF
T
MINUS ON INST. REG. 14
MINUS ON INST. REG. 15
MINUS ON INST. REG. 16
MINUS ON INST. REG. 17
INST. REG. 14
INST. REG. 15
INST. REG. 16
INST. REG. 17
13d.19
13d.20
13d.21
13d.22
13d.23
13d.24
13d.25
13d.26
13d.27
13d.28
13d.29
13d.30
13d.31
13d.32
13d.33
13d.34

FIG. 13d

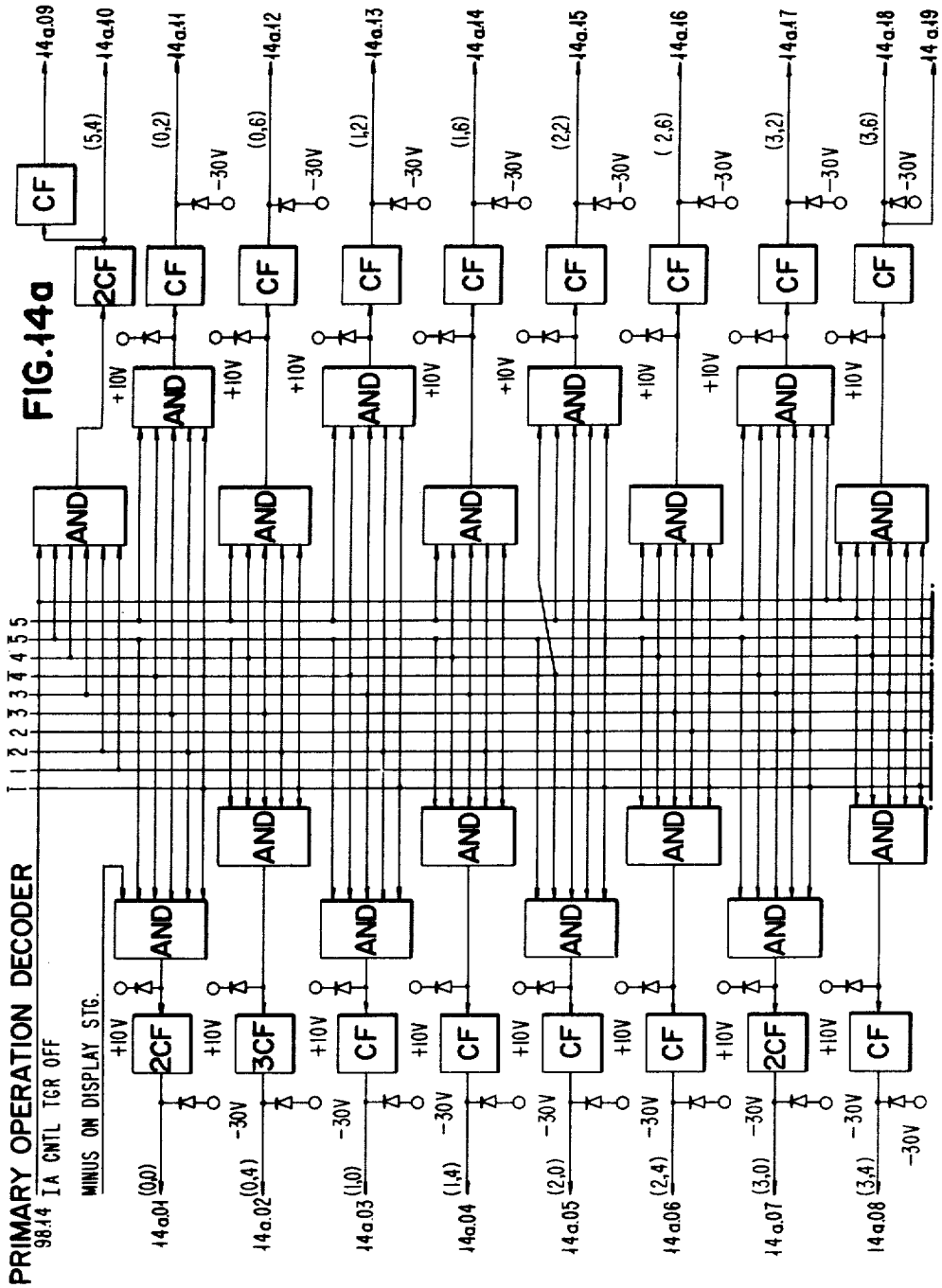


FIG. 14a
PRIMARY OPERATION DECODER
98.14 IA CNTL TGR OFF
MINUS ON DISPLAY STG.
AND
CF
2CF
3CF
+10V
-30V
1 2 3 4 5 5
14a.09
14a.10
14a.11
14a.12
14a.13
14a.14
14a.15
14a.16
14a.17
14a.18
14a.19
14a.04
14a.02
14a.03
14a.04
14a.05
14a.06
14a.07
14a.08
(5,4)
(0,2)
(0,6)
(1,2)
(1,6)
(2,2)
(2,6)
(3,2)
(3,6)
(0,0)
(0,4)
(1,0)
(1,4)
(2,0)
(2,4)
(3,0)
(3,4)

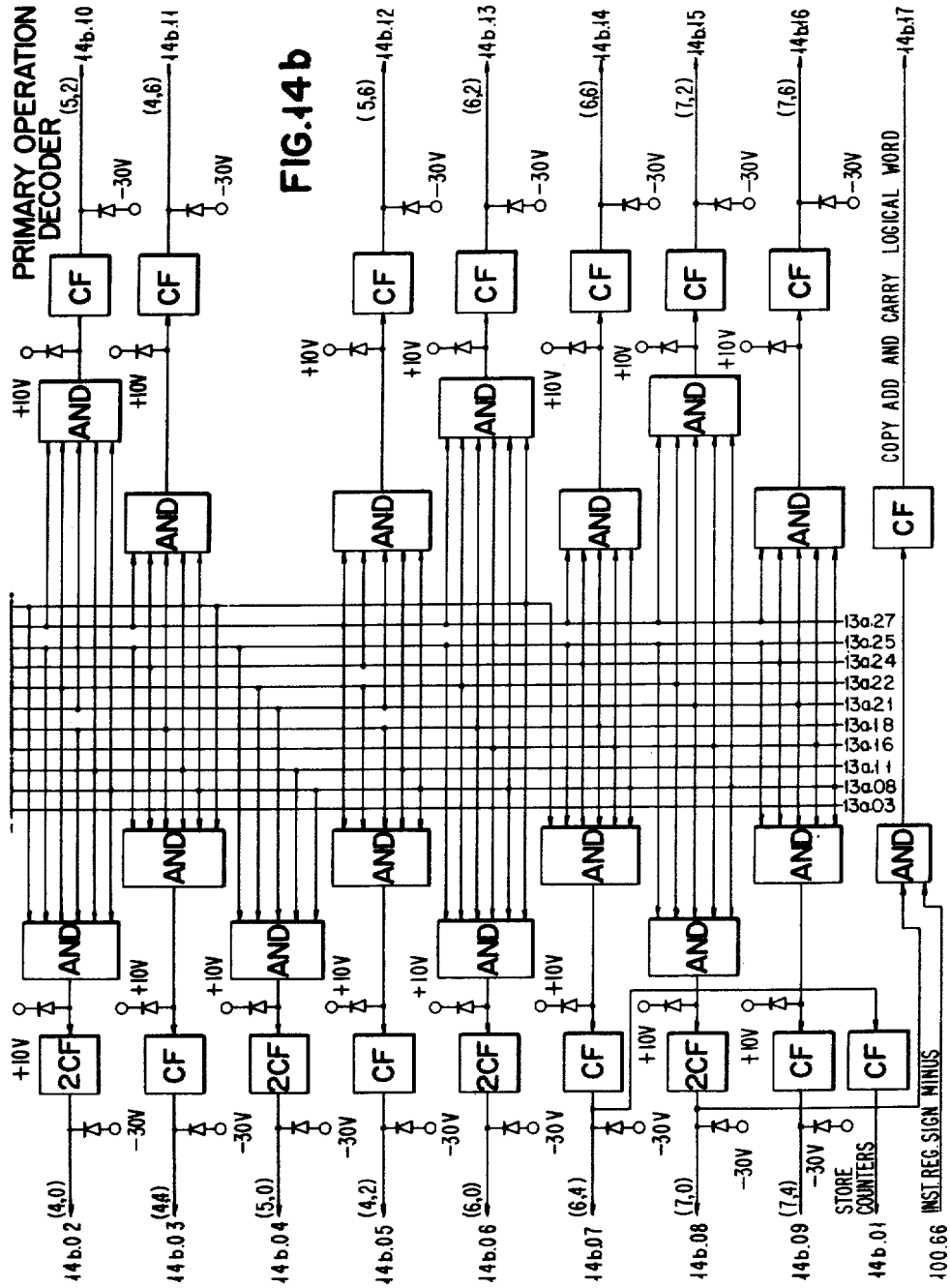

PRIMARY OPERATION DECODER
(5,2)
14b.10
(4,6)
14b.11
(5,6)
14b.12
(6,2)
14b.13
(6,6)
14b.14
(7,2)
14b.15
(7,6)
14b.16
14b.17
COPY ADD AND CARRY LOGICAL WORD
CF
AND
2CF
+10V
-30V
13a.27
13a.25
13a.24
13a.22
13a.21
13a.18
13a.16
13a.11
13a.08
13a.03
(4,0)
14b.02
(4,4)
14b.03
(5,0)
14b.04
(4,2)
14b.05
(6,0)
14b.06
(6,4)
14b.07
(7,0)
14b.08
(7,4)
14b.09
STORE COUNTERS
14b.01
INST. REG. SIGN MINUS
100.66

FIG. 14b

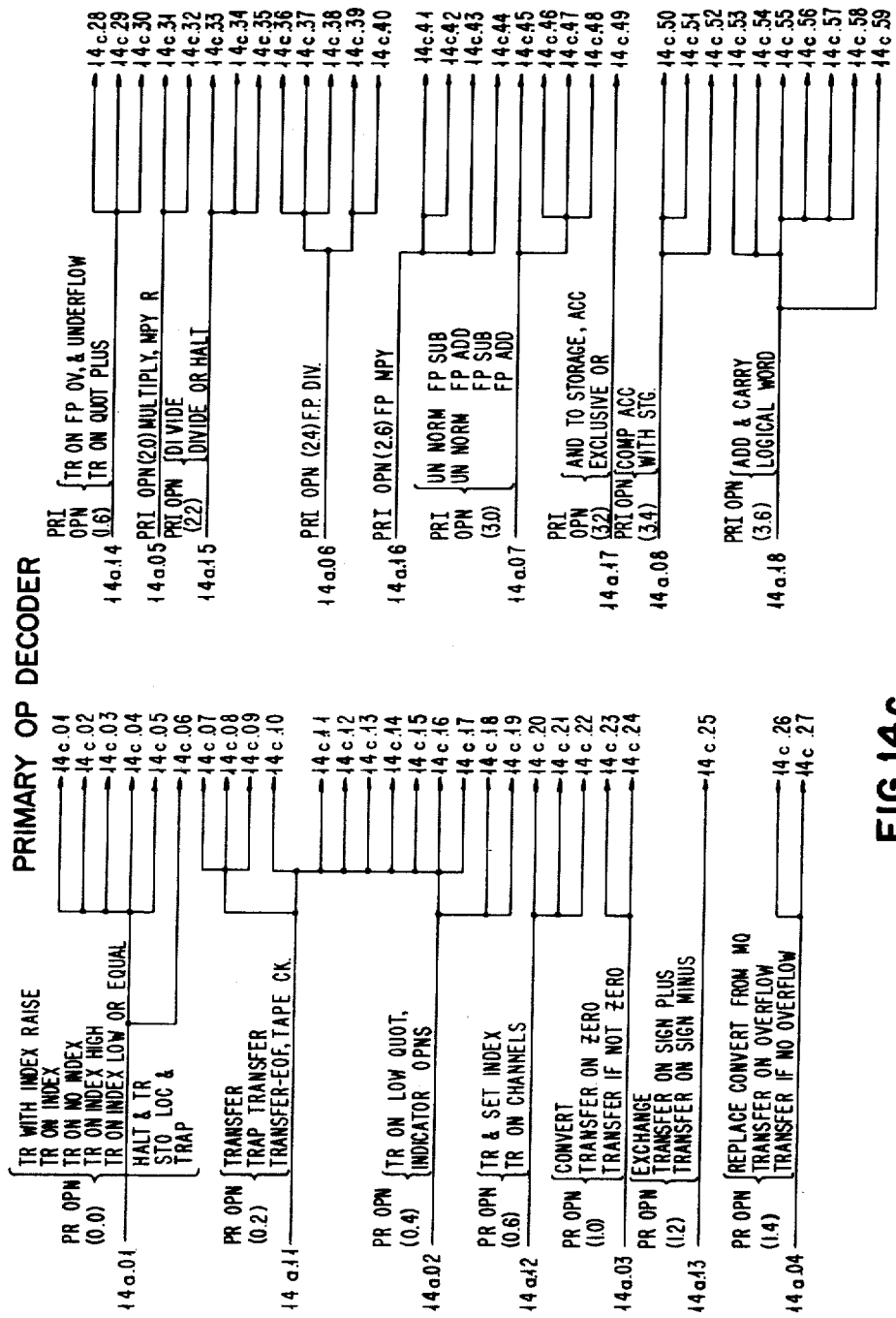

PRIMARY OP DECODER
14a.01
PR OPN (0.0)
TR WITH INDEX RAISE
TR ON INDEX
TR ON NO INDEX
TR ON INDEX HIGH
TR ON INDEX LOW OR EQUAL
HALT & TR
STO LOC &
TRAP
14a.11
PR OPN (0.2)
TRANSFER
TRAP TRANSFER
TRANSFER-EOF, TAPE CK.
14a.02
PR OPN (0.4)
TR ON LOW QUOT, INDICATOR OPNS
14a.12
PR OPN (0.6)
TR & SET INDEX
TR ON CHANNELS
14a.03
PR OPN (1.0)
CONVERT
TRANSFER ON ZERO
TRANSFER IF NOT ZERO
14a.13
PR OPN (1.2)
EXCHANGE
TRANSFER ON SIGN PLUS
TRANSFER ON SIGN MINUS
14a.04
PR OPN (1.4)
REPLACE CONVERT FROM MQ
TRANSFER ON OVERFLOW
TRANSFER IF NO OVERFLOW
14a.14
PRI OPN (1.6)
TR ON FP OV, & UNDERFLOW
TR ON QUOT PLUS
14a.05
PRI OPN (2.0)
MULTIPLY, MPY R
14a.15
PRI OPN (2.2)
DIVIDE
DIVIDE OR HALT
14a.06
PRI OPN (2.4)
F.P. DIV.
14a.16
PRI OPN (2.6)
FP MPY
14a.07
PRI OPN (3.0)
UN NORM FP SUB
UN NORM FP ADD
FP SUB
FP ADD
14a.17
PRI OPN (3.2)
AND TO STORAGE, ACC
EXCLUSIVE OR
14a.08
PRI OPN (3.4)
COMP ACC
WITH STG.
14a.18
PRI OPN (3.6)
ADD & CARRY
LOGICAL WORD
14c.01
14c.02
14c.03
14c.04
14c.05
14c.06
14c.07
14c.08
14c.09
14c.10
14c.11
14c.12
14c.13
14c.14
14c.15
14c.16
14c.17
14c.18
14c.19
14c.20
14c.21
14c.22
14c.23
14c.24
14c.25
14c.26
14c.27
14c.28
14c.29
14c.30
14c.31
14c.32
14c.33
14c.34
14c.35
14c.36
14c.37
14c.38
14c.39
14c.40
14c.41
14c.42
14c.43
14c.44
14c.45
14c.46
14c.47
14c.48
14c.49
14c.50
14c.51
14c.52
14c.53
14c.54
14c.55
14c.56
14c.57
14c.58
14c.59

FIG. 14c

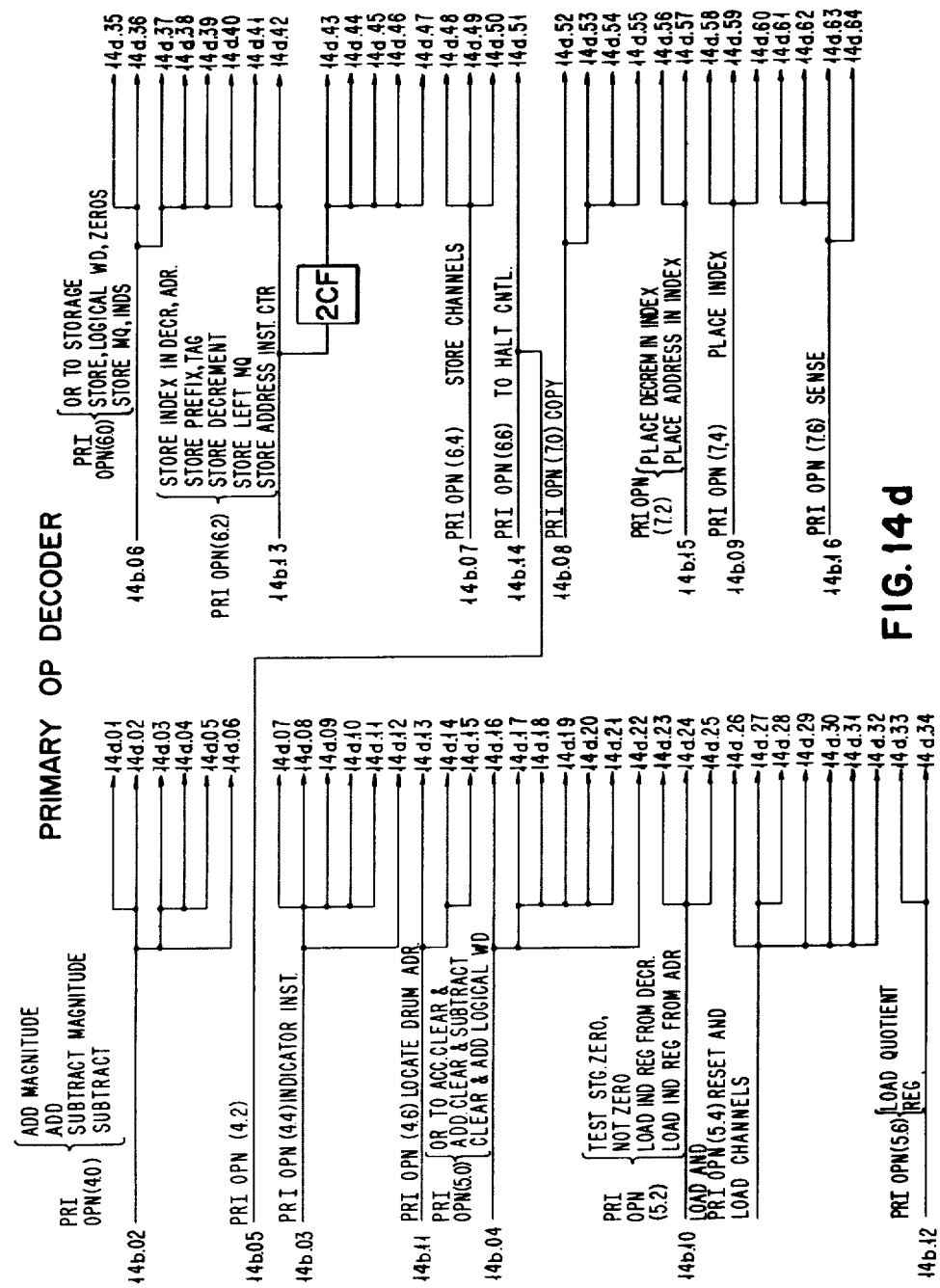

PRIMARY OP DECODER
PRI OPN(40) ADD MAGNITUDE, ADD, SUBTRACT MAGNITUDE, SUBTRACT
PRI OPN (4.2)
PRI OPN (44) INDICATOR INST.
PRI OPN (4.6) LOCATE DRUM ADR
PRI OPN(5.0) OR TO ACC. CLEAR & ADD, CLEAR & SUBTRACT, CLEAR & ADD LOGICAL WD
PRI OPN (5.2) TEST STG. ZERO, NOT ZERO, LOAD IND REG FROM DECR., LOAD IND REG FROM ADR
LOAD AND PRI OPN (5.4) RESET AND LOAD CHANNELS
PRI OPN(5.6) LOAD QUOTIENT REG.
PRI OPN(6.0) OR TO STORAGE, STORE, LOGICAL WD, ZEROS, STORE MQ, INDS
PRI OPN(6.2) STORE INDEX IN DECR, ADR., STORE PREFIX, TAG, STORE DECREMENT, STORE LEFT MQ, STORE ADDRESS INST CTR
2CF
PRI OPN (6.4) STORE CHANNELS
PRI OPN (6.6) TO HALT CNTL.
PRI OPN (7.0) COPY
PRI OPN (7.2) PLACE DECREM IN INDEX, PLACE ADDRESS IN INDEX
PRI OPN (7.4) PLACE INDEX
PRI OPN (7.6) SENSE
14b.02
14b.05
14b.03
14b.11
14b.04
14b.10
14b.12
14b.06
14b.13
14b.07
14b.14
14b.08
14b.15
14b.09
14b.16
14d.01 14d.02 14d.03 14d.04 14d.05 14d.06
14d.07 14d.08 14d.09 14d.10 14d.11 14d.12
14d.13 14d.14 14d.15 14d.16 14d.17 14d.18 14d.19 14d.20 14d.21 14d.22 14d.23 14d.24 14d.25 14d.26 14d.27 14d.28 14d.29 14d.30 14d.31 14d.32 14d.33 14d.34
14d.35 14d.36 14d.37 14d.38 14d.39 14d.40 14d.41 14d.42
14d.43 14d.44 14d.45 14d.46 14d.47
14d.48 14d.49 14d.50 14d.51
14d.52 14d.53 14d.54 14d.55 14d.56 14d.57
14d.58 14d.59 14d.60 14d.61 14d.62 14d.63 14d.64

FIG. 14d

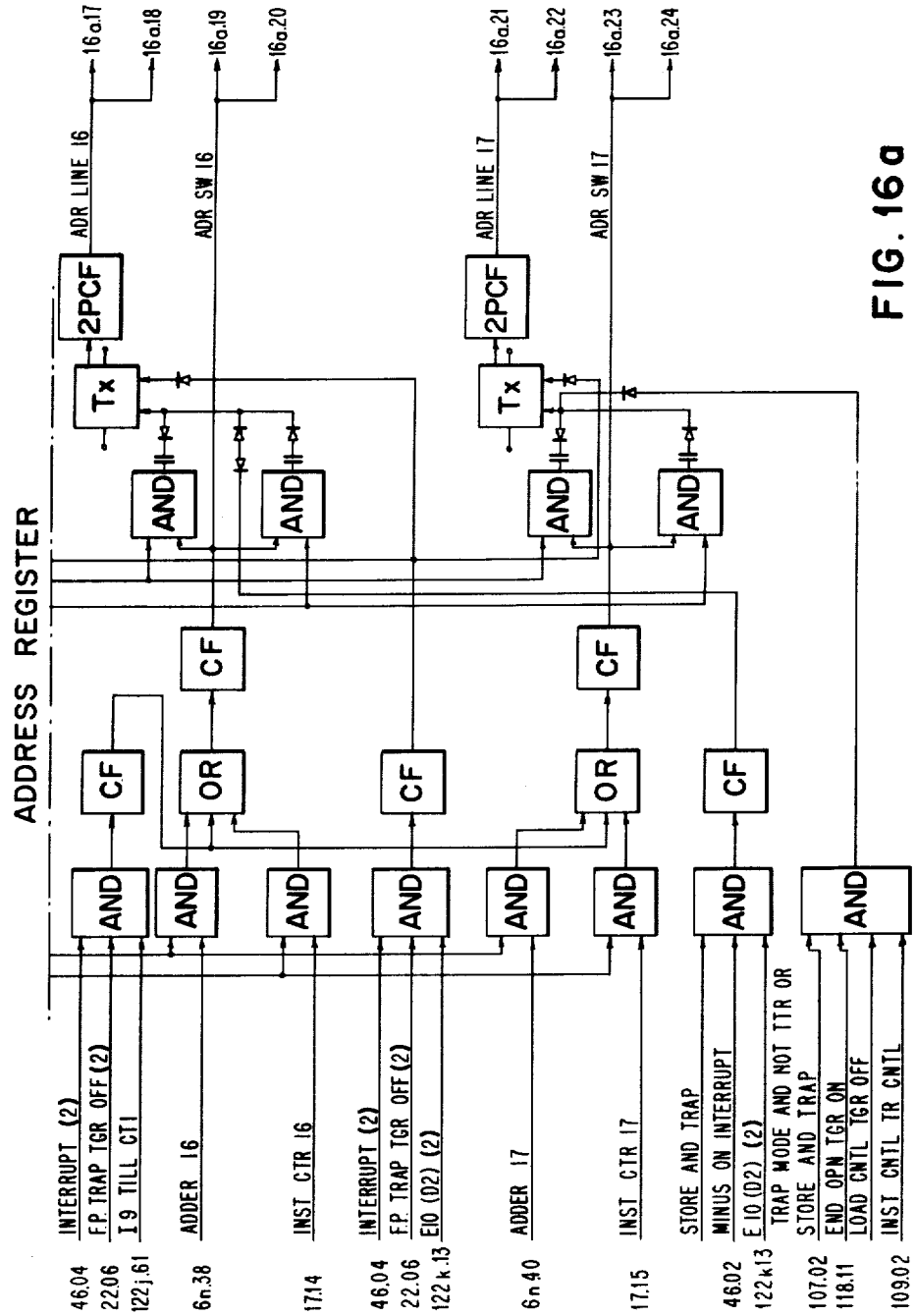

ADDRESS REGISTER
16a.17
16a.18
16a.19
16a.20
16a.21
16a.22
16a.23
16a.24
ADR LINE 16
ADR SW 16
ADR LINE 17
ADR SW 17
2PCF
Tx
AND
CF
OR
INTERRUPT (2)
F.P. TRAP TGR OFF (2)
I 9 TILL CT1
ADDER 16
INST CTR 16
INTERRUPT (2)
F.P. TRAP TGR OFF (2)
EIO (D2) (2)
ADDER 17
INST CTR 17
STORE AND TRAP
MINUS ON INTERRUPT
E IO (D2) (2)
TRAP MODE AND NOT TTR OR
STORE AND TRAP
END OPN TGR ON
LOAD CNTL TGR OFF
INST CNTL TR CNTL
46.04
22.06
122j.61
6n.38
17.14
46.04
22.06
122k.13
6n.40
17.15
46.02
122k13
107.02
118.11
109.02

FIG. 16a

May 29, 1962

J. L. BROWN

INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

3,036,773

Filed Dec. 26, 1957

244 Sheets-Sheet 91

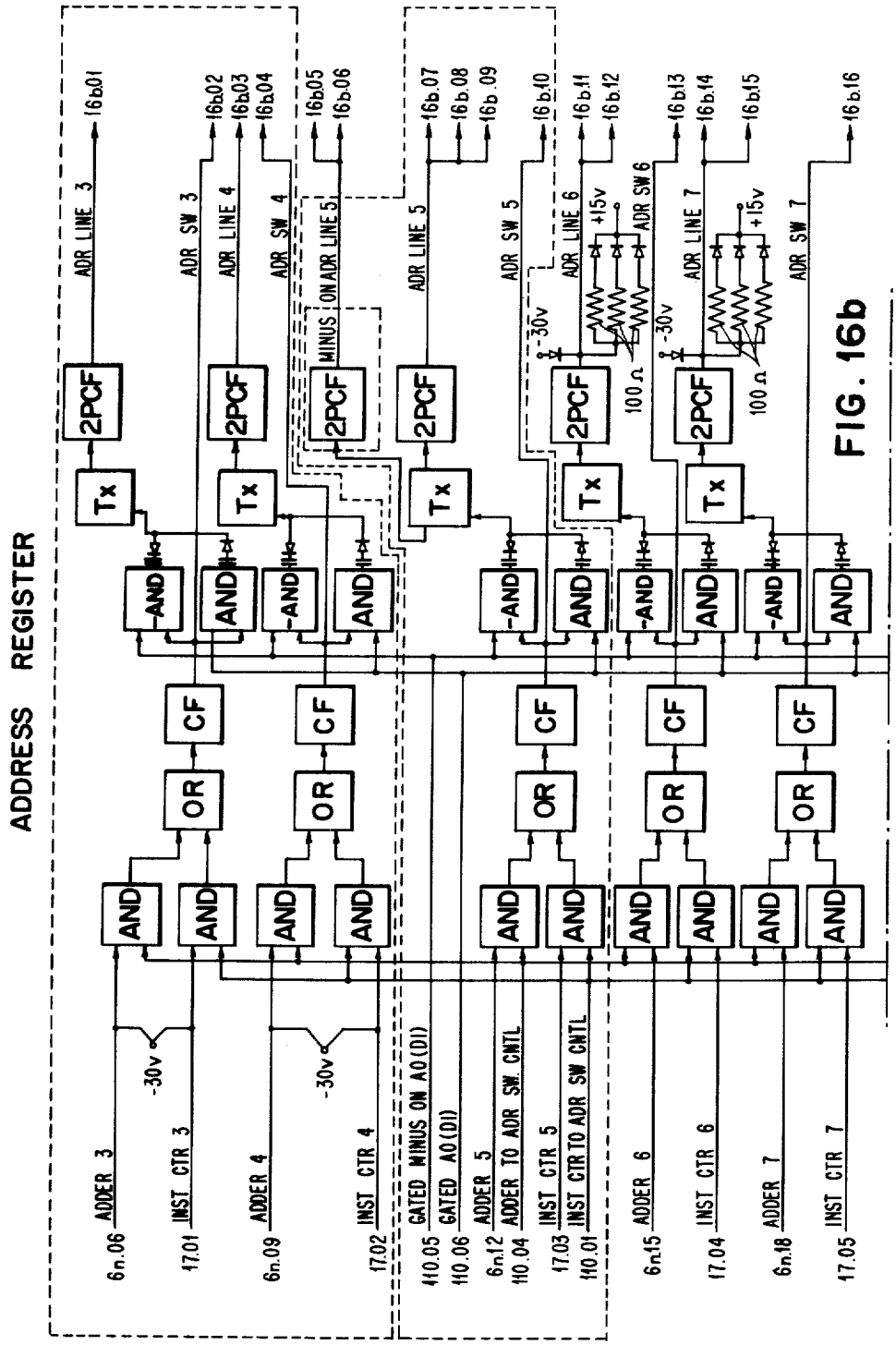


FIG. 16b

May 29, 1962 J. L. BROWN 3,036,773
INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE
Filed Dec. 26, 1957 244 Sheets-Sheet 92

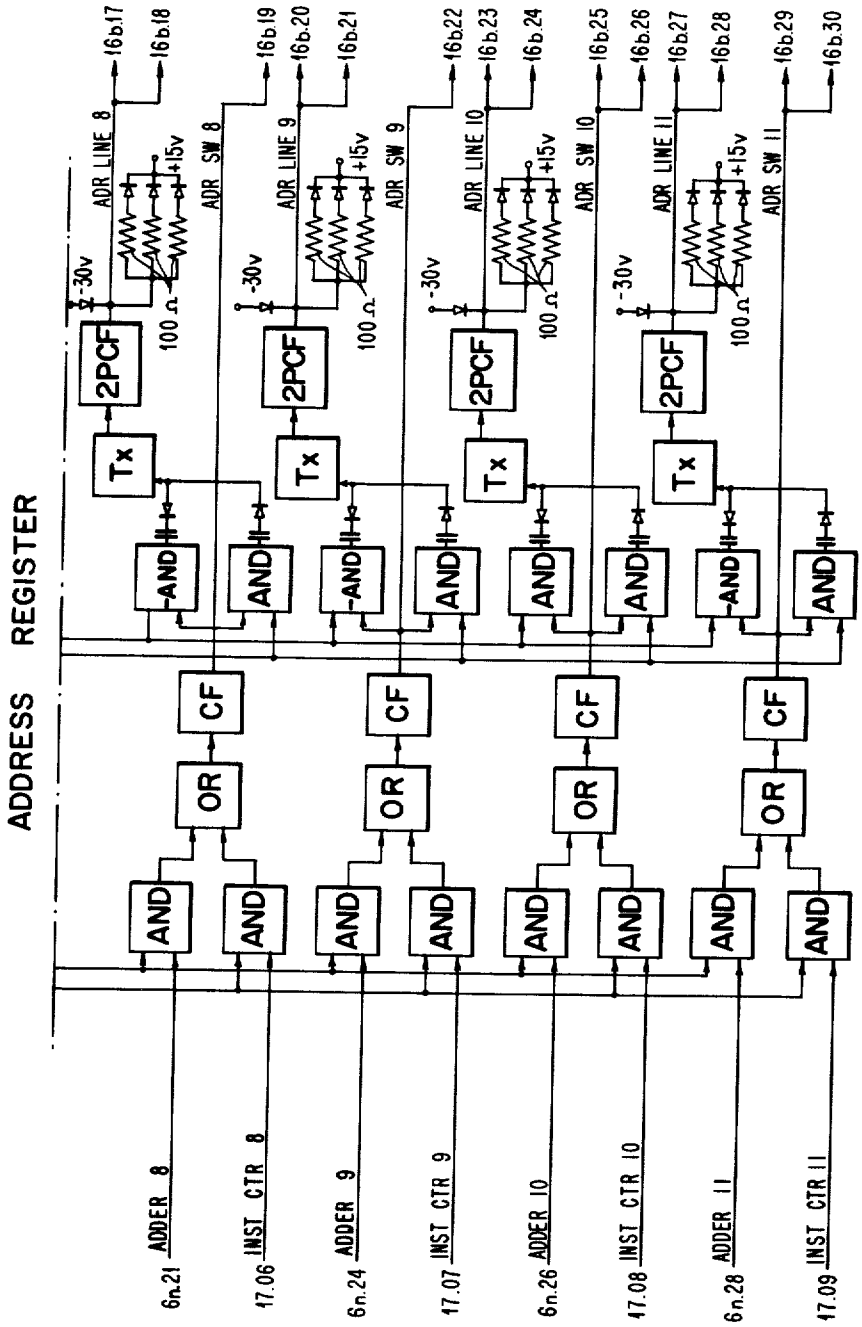


FIG. 16b

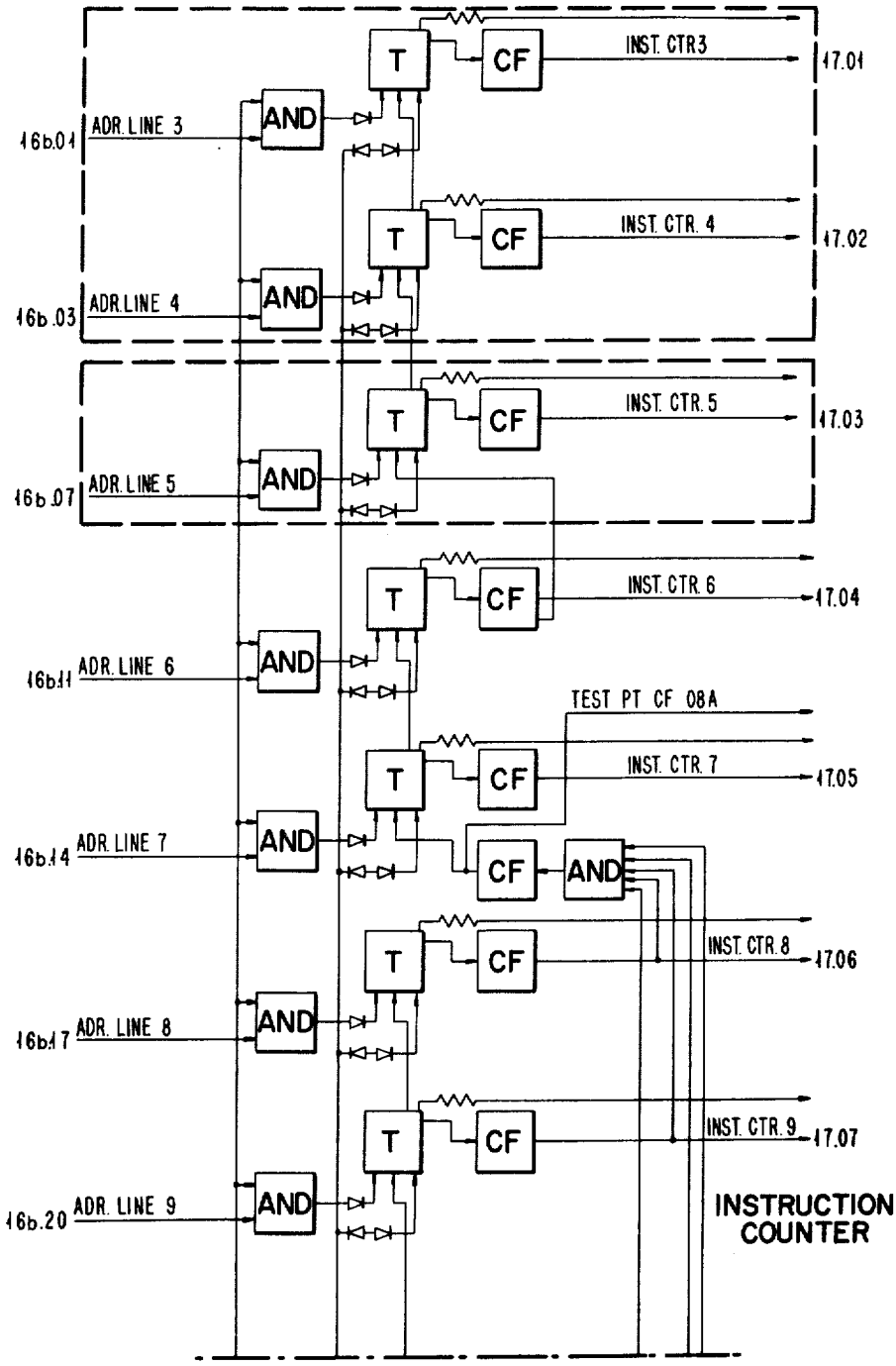

T
CF
INST. CTR3
17.01
16b.01
ADR. LINE 3
AND
INST. CTR. 4
17.02
16b.03
ADR. LINE 4
INST. CTR. 5
17.03
16b.07
ADR. LINE 5
INST. CTR. 6
17.04
16b.11
ADR. LINE 6
TEST PT CF 08A
INST. CTR. 7
17.05
16b.14
ADR. LINE 7
INST. CTR. 8
17.06
16b.17
ADR. LINE 8
INST. CTR. 9
17.07
16b.20
ADR. LINE 9
INSTRUCTION COUNTER

FIG.17

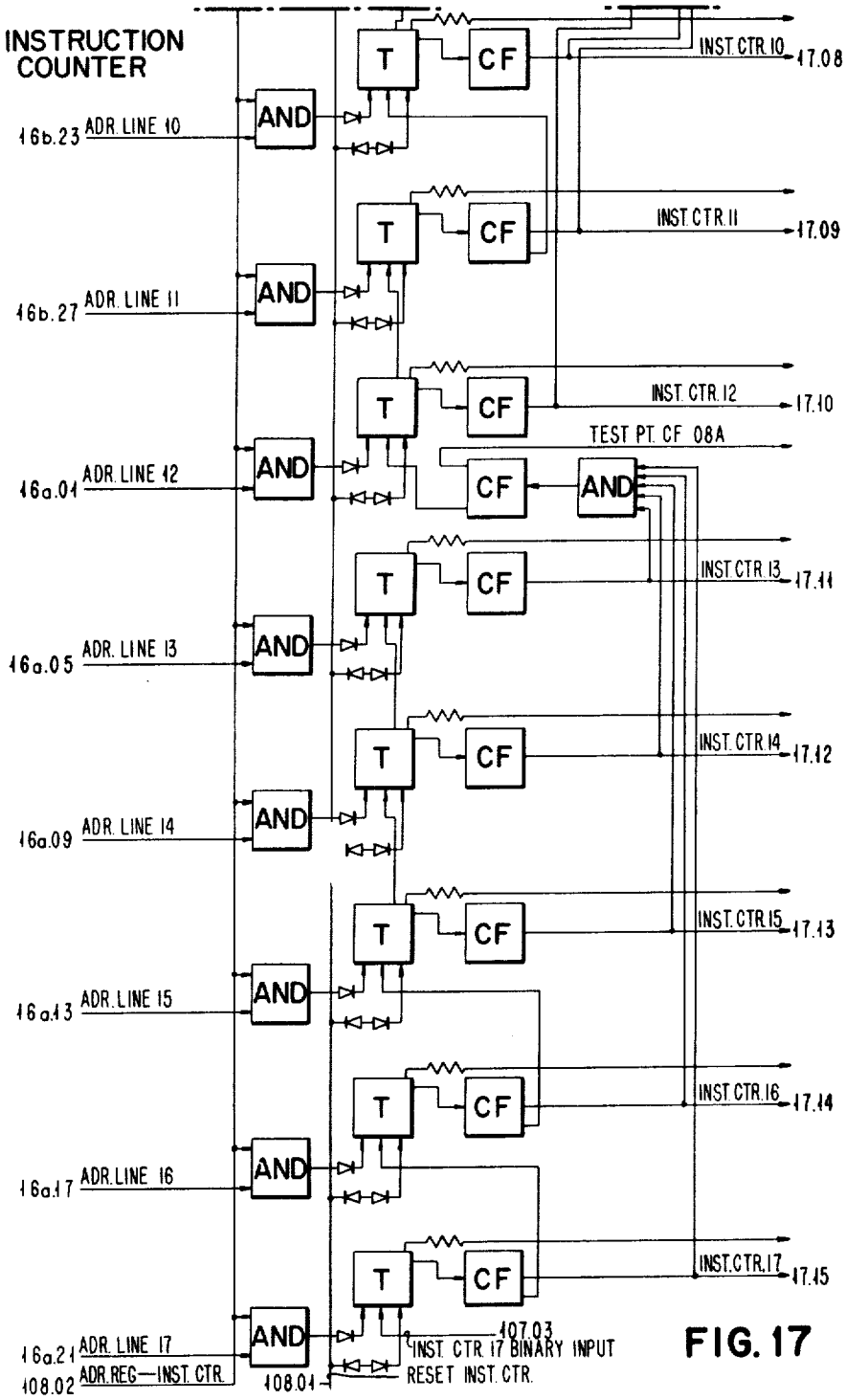

INSTRUCTION COUNTER
16b.23 ADR. LINE 10
16b.27 ADR. LINE 11
16a.01 ADR. LINE 12
16a.05 ADR. LINE 13
16a.09 ADR. LINE 14
16a.13 ADR. LINE 15
16a.17 ADR. LINE 16
16a.21 ADR. LINE 17
108.02 ADR. REG—INST. CTR.
AND
T
CF
INST. CTR. 10 17.08
INST. CTR. 11 17.09
INST. CTR. 12 17.10
TEST PT. CF 08A
INST. CTR. 13 17.11
INST. CTR. 14 17.12
INST. CTR. 15 17.13
INST. CTR. 16 17.14
INST. CTR. 17 17.15
107.03 INST. CTR. 17 BINARY INPUT
108.04 RESET INST. CTR.

FIG. 17

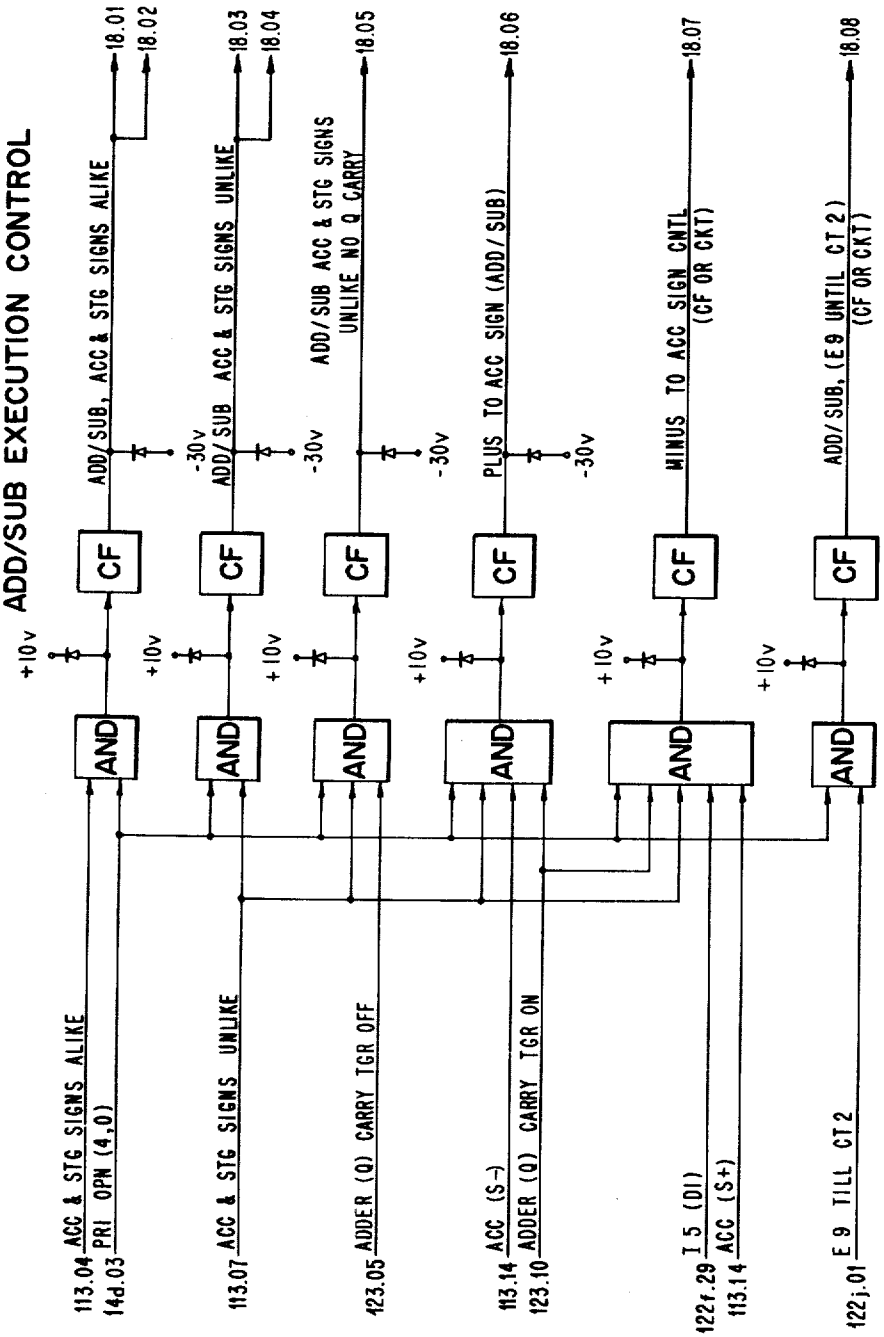

ADD/SUB EXECUTION CONTROL
+10v
AND
CF
-30v
ADD/SUB, ACC & STG SIGNS ALIKE
ADD/SUB ACC & STG SIGNS UNLIKE
ADD/SUB ACC & STG SIGNS UNLIKE NO Q CARRY
PLUS TO ACC SIGN (ADD/SUB)
MINUS TO ACC SIGN CNTL (CF OR CKT)
ADD/SUB, (E9 UNTIL CT 2) (CF OR CKT)
18.01
18.02
18.03
18.04
18.05
18.06
18.07
18.08
113.04 ACC & STG SIGNS ALIKE
14d.03 PRI OPN (4,0)
113.07 ACC & STG SIGNS UNLIKE
123.05 ADDER (Q) CARRY TGR OFF
113.14 ACC (S-)
123.10 ADDER (Q) CARRY TGR ON
122f.29 I 5 (01)
113.14 ACC (S+)
122j.01 E 9 TILL CT 2

FIG. 18

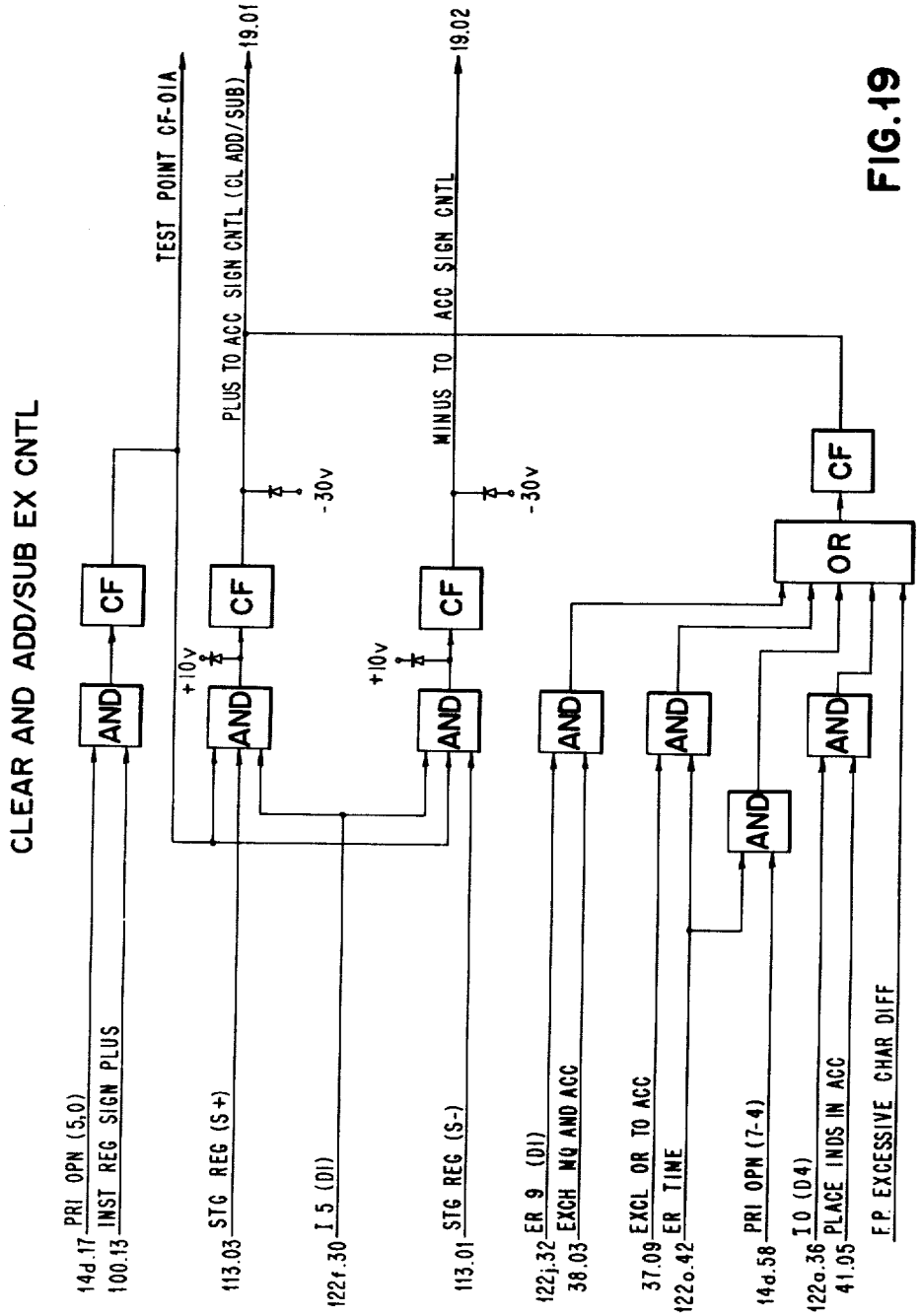
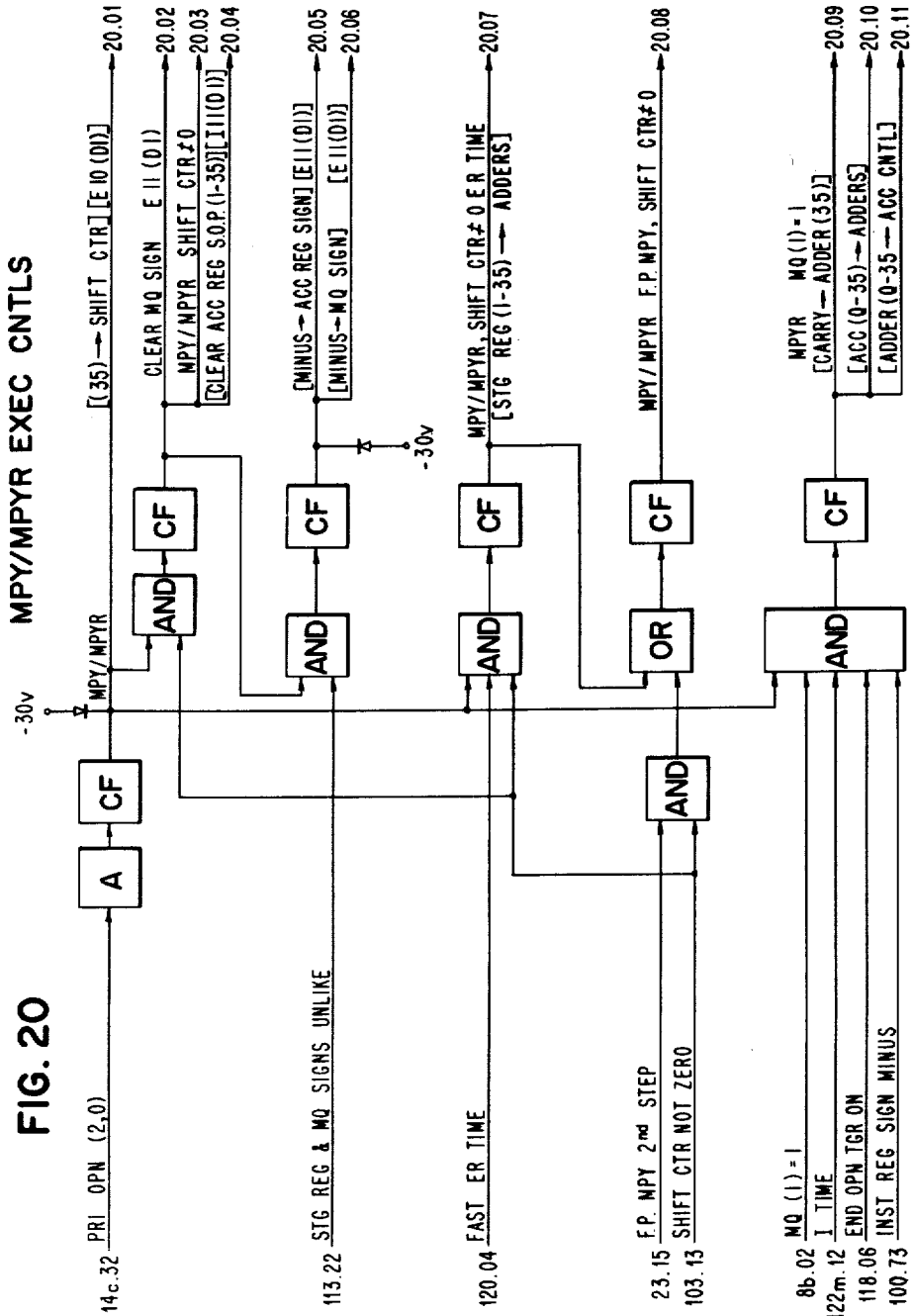

CLEAR AND ADD/SUB EX CNTL
TEST POINT CF-01A
PLUS TO ACC SIGN CNTL (CL ADD/SUB) 19.01
MINUS TO ACC SIGN CNTL 19.02
+10v
-30v
CF
AND
OR
14d.17 PRI OPN (5,0)
100.13 INST REG SIGN PLUS
113.03 STG REG (S+)
122f.30 I 5 (01)
113.01 STG REG (S-)
122j.32 ER 9 (01)
38.03 EXCH MQ AND ACC
37.09 EXCL OR TO ACC
122o.42 ER TIME
14d.58 PRI OPN (7-4)
122o.36 I 0 (04)
41.05 PLACE INDS IN ACC
F.P. EXCESSIVE CHAR DIFF

FIG. 19

FIG. 20


MPY/MPYR EXEC CNTLS
-30v
MPY/MPYR
A
CF
AND
CF
AND
CF
AND
CF
OR
AND
CF
AND
[(35)→ SHIFT CTR] [E 10 (D1)]
CLEAR MQ SIGN E 11 (D1)
MPY/MPYR SHIFT CTR≠0
[CLEAR ACC REG S.O.P.(1-35)] [1111(D1)]
[MINUS→ ACC REG SIGN] [E11(D1)]
[MINUS→ MQ SIGN] [E11(D1)]
-30v
MPY/MPYR, SHIFT CTR≠0 E.R. TIME
[STG REG (1-35)→ ADDERS]
MPY/MPYR F.P. MPY, SHIFT CTR≠0
MPYR MQ(1)=1
[CARRY→ ADDER (35)]
[ACC (0-35)→ ADDERS]
[ADDER (0-35→ ACC CNTL]
20.01
20.02
20.03
20.04
20.05
20.06
20.07
20.08
20.09
20.10
20.11
14c.32 PRI OPN (2,0)
113.22 STG REG & MQ SIGNS UNLIKE
120.04 FAST ER TIME
23.15 F.P. MPY 2nd STEP
103.13 SHIFT CTR NOT ZERO
8b.02 MQ (1)=1
122m.12 I TIME
118.06 END OPN TGR ON
100.73 INST REG SIGN MINUS

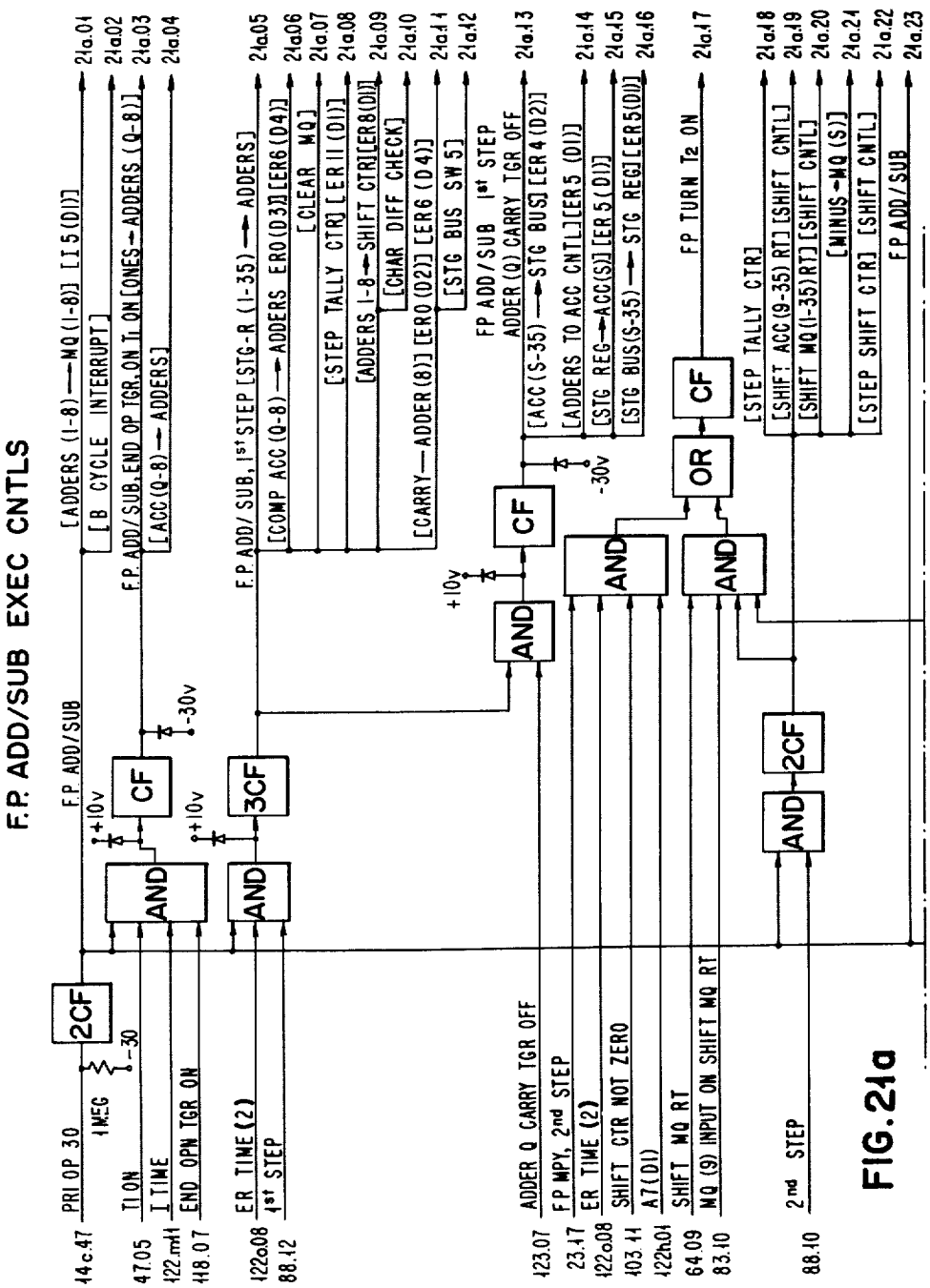

F.P. ADD/SUB EXEC CNTLS
F.P. ADD/SUB
PRI OP 30
1 MEG
-30
TI ON
I TIME
END OPN TGR ON
ER TIME (2)
1st STEP
2nd STEP
ADDER Q CARRY TGR OFF
FP MPY, 2nd STEP
ER TIME (2)
SHIFT CTR NOT ZERO
A7(D1)
SHIFT MQ RT
MQ (9) INPUT ON SHIFT MQ RT
+10v
-30v
2CF
CF
3CF
AND
OR
[ADDERS (1-8) → MQ (1-8)] [I 5 (D1)]
[B CYCLE INTERRUPT]
F.P. ADD/SUB. END OP TGR. ON Ti ON [ONES → ADDERS (Q-8)]
[ACC (Q-8) → ADDERS]
F.P. ADD/SUB, 1st STEP [STG-R (1-35) → ADDERS]
[COMP ACC (Q-8) → ADDERS ER0 (D3)] [ER6 (D4)]
[CLEAR MQ]
[STEP TALLY CTR] [ER 11 (D1)]
[ADDERS 1-8 → SHIFT CTR] [ER8 (D1)]
[CHAR DIFF CHECK]
[CARRY → ADDER (8)] [ER0 (D2)] [ER6 (D4)]
[STG BUS SW 5]
FP ADD/SUB 1st STEP
ADDER (Q) CARRY TGR OFF
[ACC (S-35) → STG BUS] [ER4 (D2)]
[ADDERS TO ACC CNTL] [ER5 (D1)]
[STG REG → ACC (S)] [ER5 (D1)]
[STG BUS (S-35) → STG REG] [ER5 (D1)]
FP TURN T2 ON
[STEP TALLY CTR]
[SHIFT ACC (9-35) RT] [SHIFT CNTL]
[SHIFT MQ (1-35) RT] [SHIFT CNTL]
[MINUS → MQ (S)]
[STEP SHIFT CTR] [SHIFT CNTL]
F.P. ADD/SUB
14c.47
47.05
122.m11
118.07
122a.08
88.12
123.07
23.17
122a.08
103.11
122h.01
64.09
83.10
88.10
21a.01
21a.02
21a.03
21a.04
21a.05
21a.06
21a.07
21a.08
21a.09
21a.10
21a.11
21a.12
21a.13
21a.14
21a.15
21a.16
21a.17
21a.18
21a.19
21a.20
21a.21
21a.22
21a.23

FIG. 21a

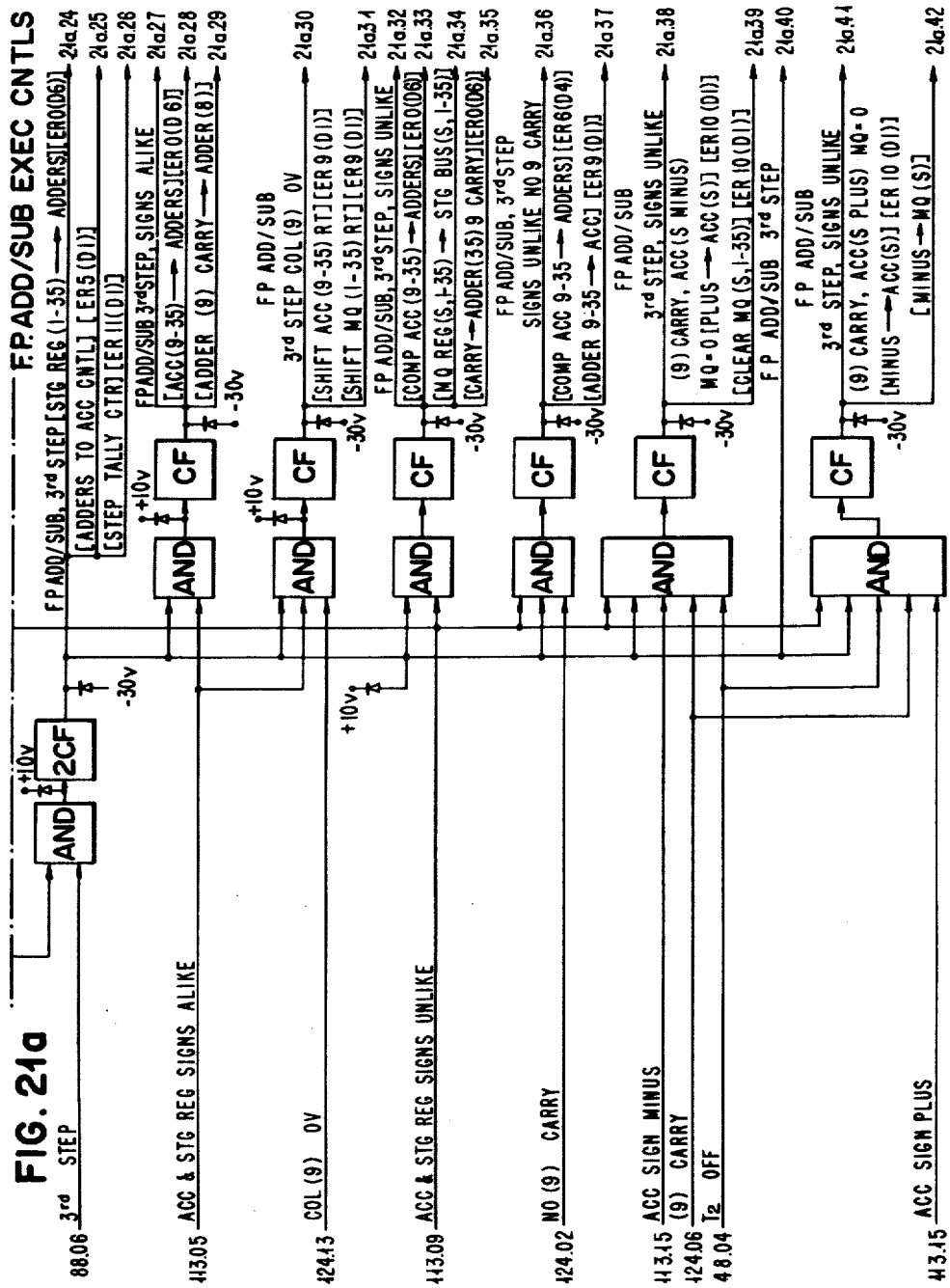

F.P.ADD/SUB EXEC CNTLS
FP ADD/SUB, 3rd STEP [STG REG (1-35) → ADDERS] [ER0(06)] 21a.24
[ADDERS TO ACC CNTL] [ER5(01)] 21a.25
[STEP TALLY CTR] [ER11(01)] 21a.26
FP ADD/SUB 3rd STEP, SIGNS ALIKE
[ACC(9-35) → ADDERS] [ER0(01)] 21a.27
[ADDER (9) CARRY → ADDER(8)] 21a.28
21a.29
FP ADD/SUB
3rd STEP COL(9) 0V 21a.30
[SHIFT ACC (9-35) RT] [ER9(01)] 21a.31
[SHIFT MQ (1-35) RT] [ER9(01)] 21a.32
FP ADD/SUB, 3rd STEP, SIGNS UNLIKE
[COMP ACC (9-35) → ADDERS] [ER0(06)] 21a.33
[MQ REG (S, 1-35) → STG BUS (S, 1-35)] 21a.34
[CARRY → ADDER (35) 9 CARRY] [ER0(06)] 21a.35
FP ADD/SUB, 3rd STEP
SIGNS UNLIKE NO 9 CARRY
[COMP ACC 9-35 → ADDERS] [ER6(04)] 21a.36
[ADDER 9-35 → ACC] [ER9(01)] 21a.37
FP ADD/SUB
3rd STEP, SIGNS UNLIKE 21a.38
(9) CARRY, ACC (S MINUS)
MQ-0 [PLUS → ACC (S)] [ER10(01)]
[CLEAR MQ (S, 1-35)] [ER10(01)] 21a.39
F P ADD/SUB 3rd STEP 21a.40
F P ADD/SUB
3rd STEP, SIGNS UNLIKE 21a.41
(9) CARRY, ACC (S PLUS) MQ-0
[MINUS → ACC (S)] [ER10(01)]
[MINUS → MQ (S)] 21a.42
AND
CF
2CF
+10v
-30v
88.06 3rd STEP
113.05 ACC & STG REG SIGNS ALIKE
424.13 COL (9) 0V
113.09 ACC & STG REG SIGNS UNLIKE
424.02 NO (9) CARRY
113.15 ACC SIGN MINUS
424.06 (9) CARRY
48.04 I2 OFF
113.15 ACC SIGN PLUS

FIG. 21a

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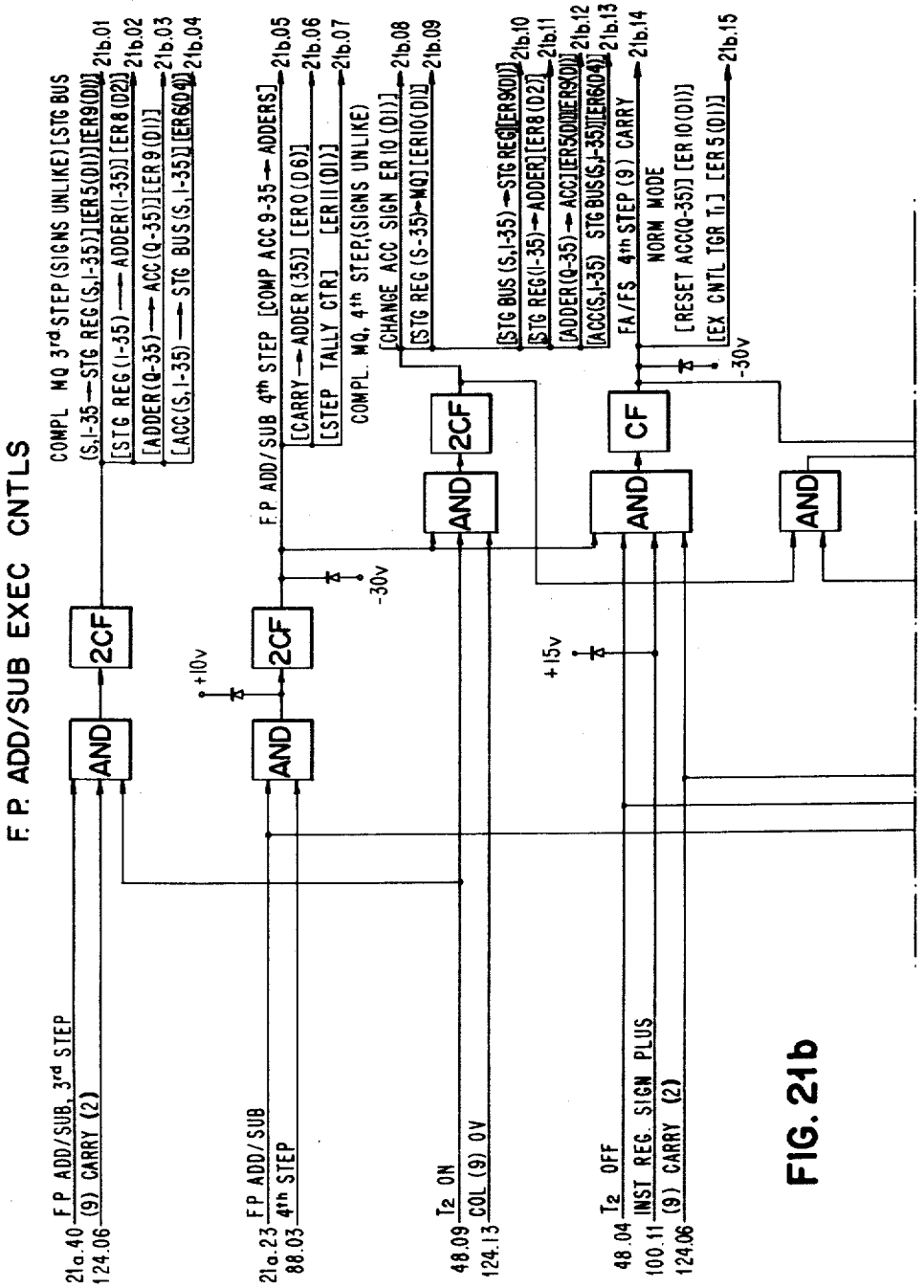

FIG. 21b

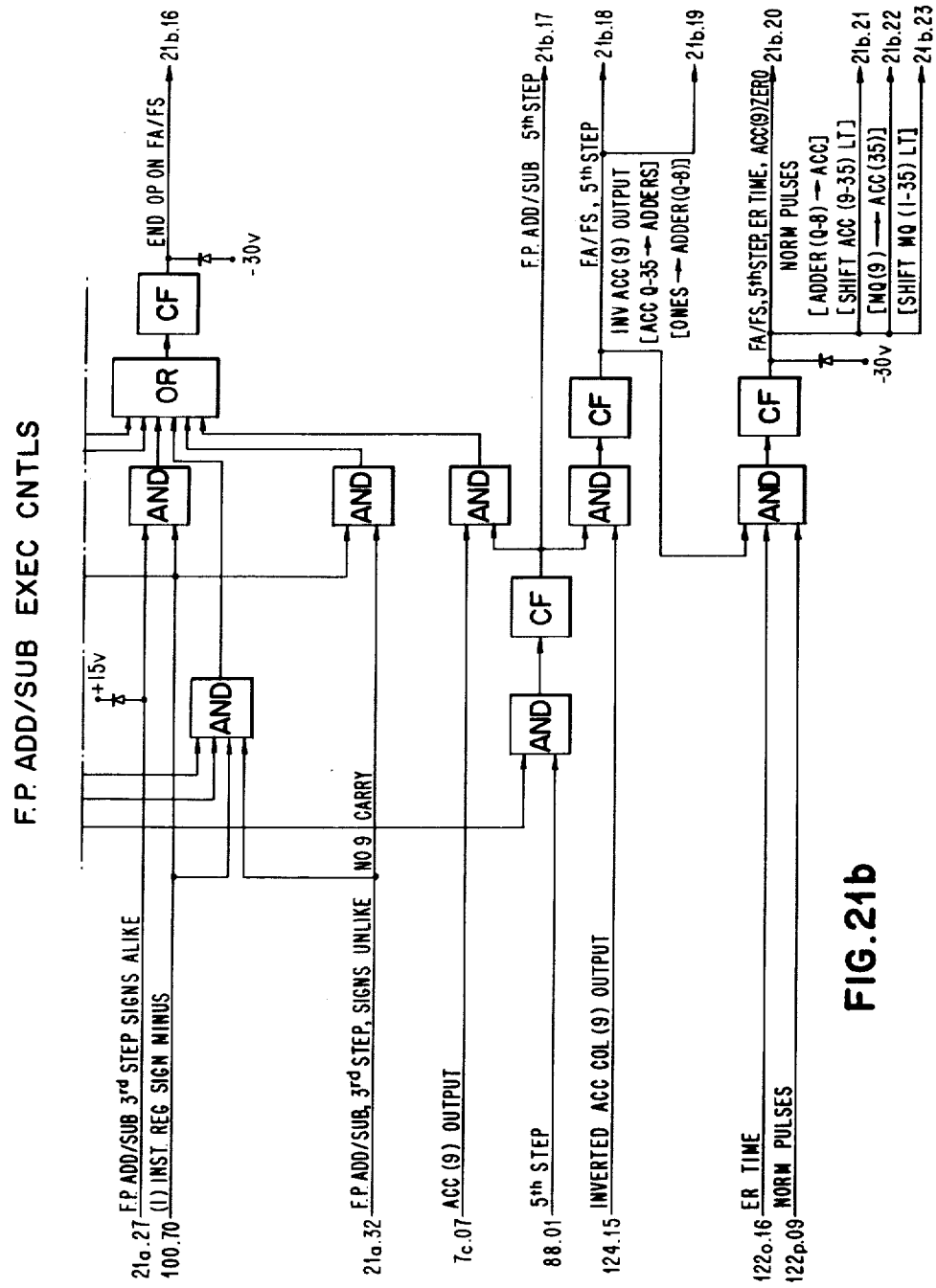
F.P. ADD/SUB EXEC CNTLS
21a.27 F.P. ADD/SUB 3rd STEP SIGNS ALIKE
100.70 (1) INST REG SIGN MINUS
21a.32 F.P. ADD/SUB, 3rd STEP, SIGNS UNLIKE
NO 9 CARRY
7c.07 ACC (9) OUTPUT
88.01 5th STEP
124.15 INVERTED ACC COL (9) OUTPUT
122o.16 ER TIME
122p.09 NORM PULSES
+15v
AND
OR
CF
-30v
END OP ON FA/FS 21b.16
F.P. ADD/SUB 5th STEP 21b.17
FA/FS, 5th STEP 21b.18
INV ACC (9) OUTPUT
[ACC 0-35 → ADDERS]
[ONES → ADDER (0-8)] 21b.19
FA/FS, 5th STER, ER TIME, ACC(9)ZERO 21b.20
NORM PULSES
[ADDER (0-8) → ACC]
[SHIFT ACC (9-35) LT] 21b.21
[MQ(9) → ACC(35)] 21b.22
[SHIFT MQ (1-35) LT] 21b.23

FIG. 21b

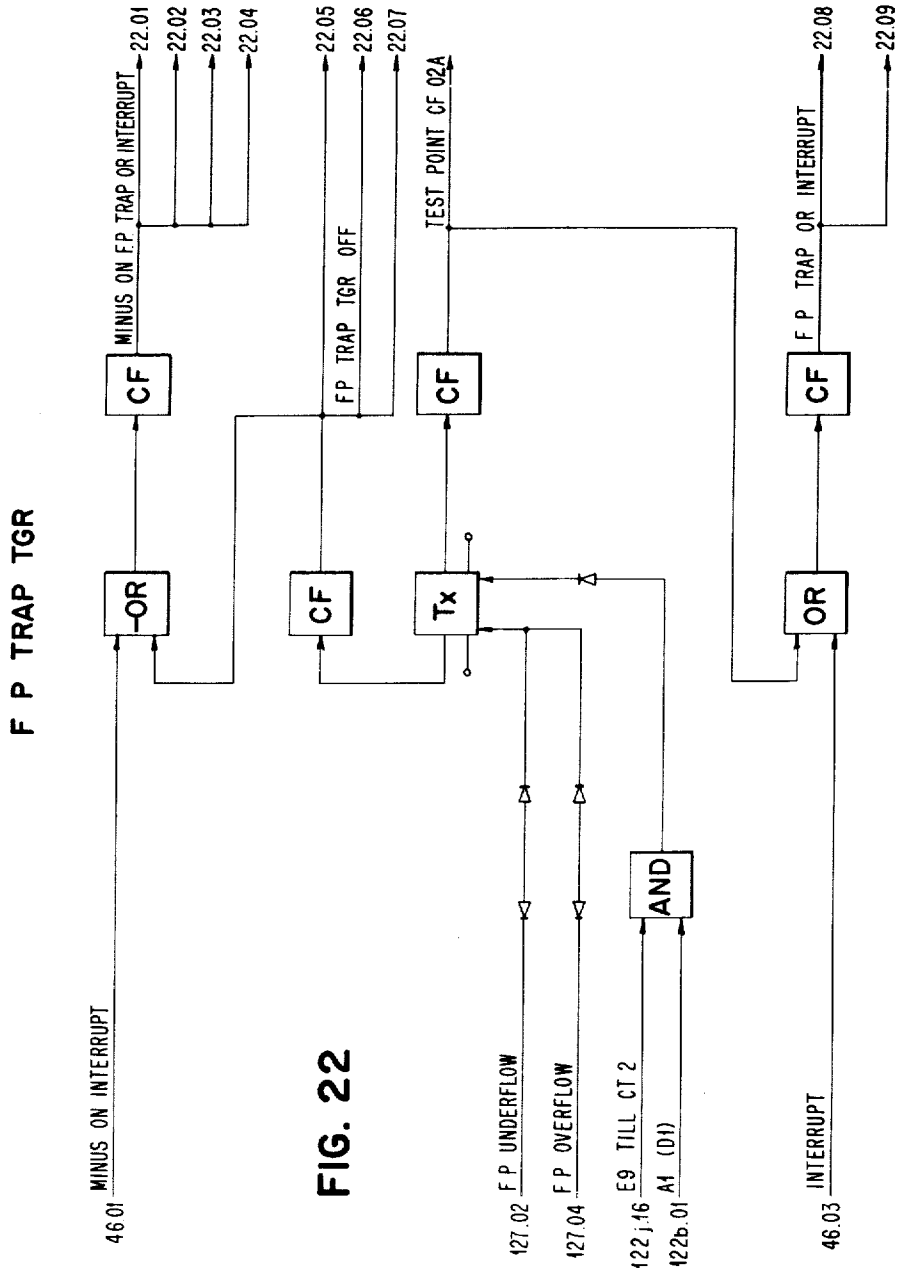
F P TRAP TGR
MINUS ON INTERRUPT
46.01
OR
CF
MINUS ON F.P. TRAP OR INTERRUPT
22.01
22.02
22.03
22.04
CF
F.P. TRAP TGR OFF
22.05
22.06
22.07
CF
TEST POINT CF 02A
Tx
F P UNDERFLOW
127.02
F P OVERFLOW
127.04
AND
E9 TILL CT 2
122 j.16
A1 (D1)
122b.01
OR
CF
F P TRAP OR INTERRUPT
22.08
22.09
INTERRUPT
46.03

FIG. 22

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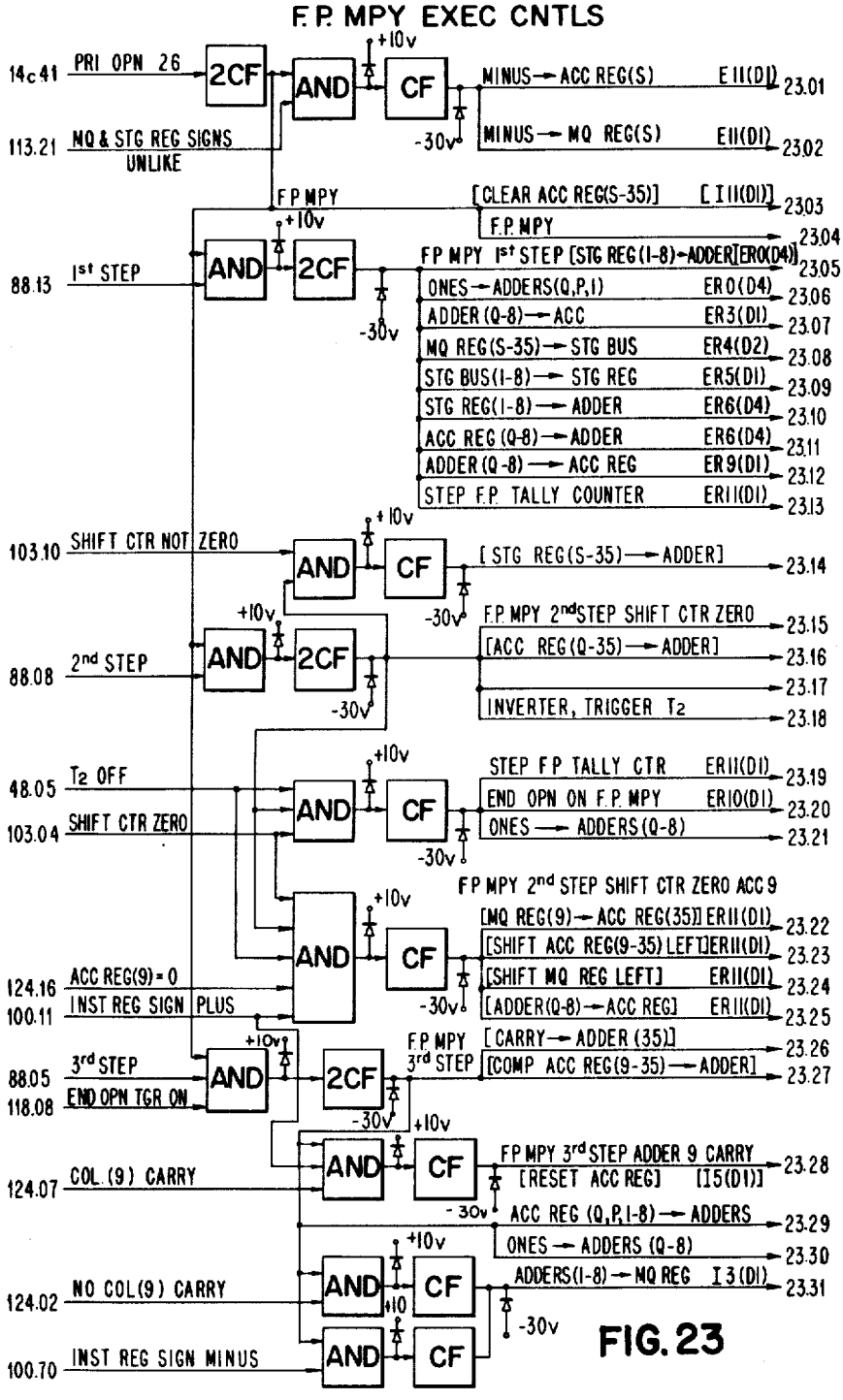


FIG. 23

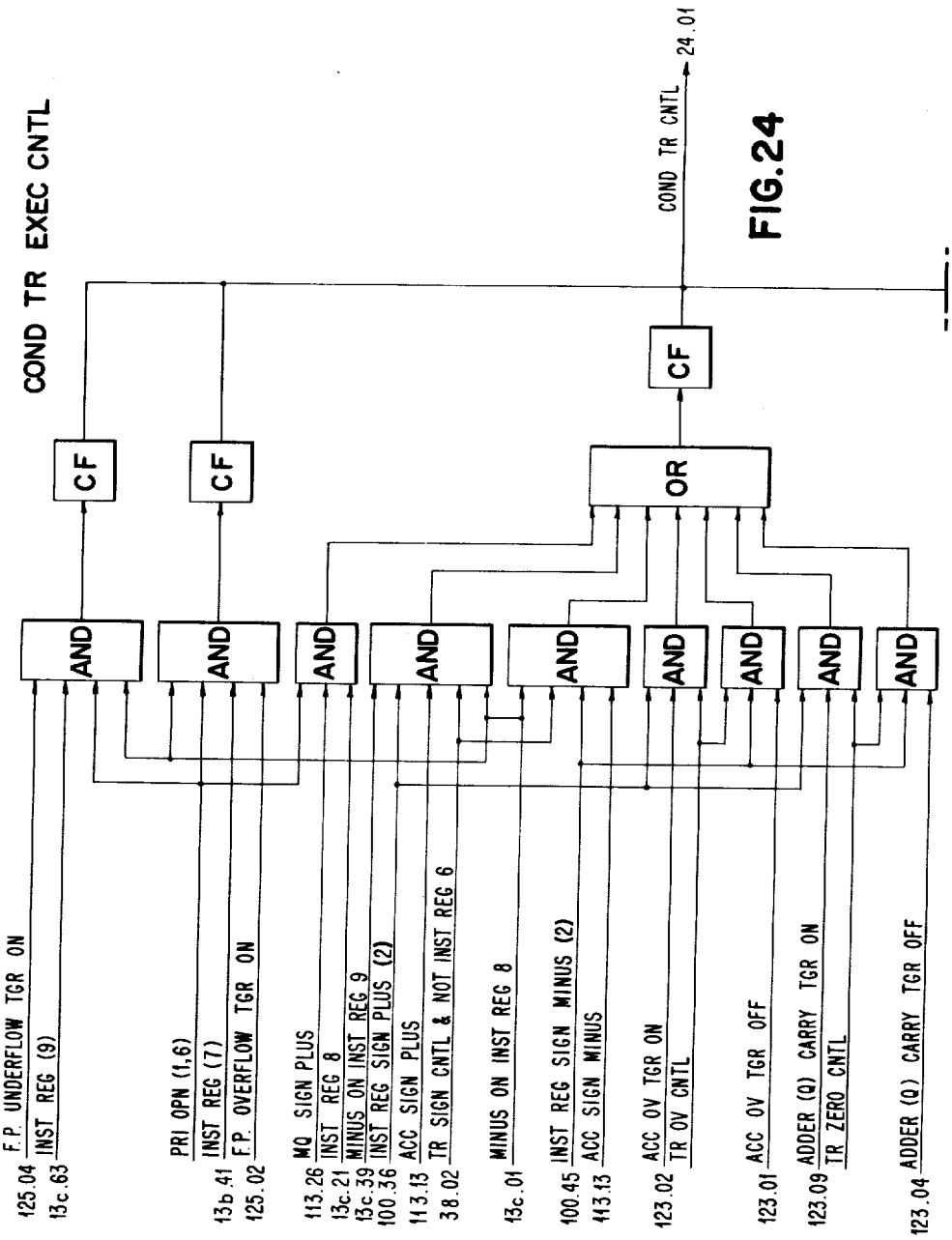

COND TR EXEC CNTL
CF
CF
CF
OR
AND
AND
AND
AND
AND
AND
AND
AND
AND
COND TR CNTL 24.01
F.P. UNDERFLOW TGR ON 125.04
INST REG (9) 13c.63
PRI OPN (1,6)
INST REG (7) 13b.41
F.P. OVERFLOW TGR ON 125.02
MQ SIGN PLUS 113.26
INST REG 8 13c.21
MINUS ON INST REG 9 13c.39
INST REG SIGN PLUS (2) 100.36
ACC SIGN PLUS 113.13
TR SIGN CNTL & NOT INST REG 6 38.02
MINUS ON INST REG 8 13c.01
INST REG SIGN MINUS (2) 100.45
ACC SIGN MINUS 113.13
ACC OV TGR ON 123.02
TR OV CNTL
ACC OV TGR OFF 123.01
ADDER (Q) CARRY TGR ON 123.09
TR ZERO CNTL
ADDER (Q) CARRY TGR OFF 123.04

FIG.24

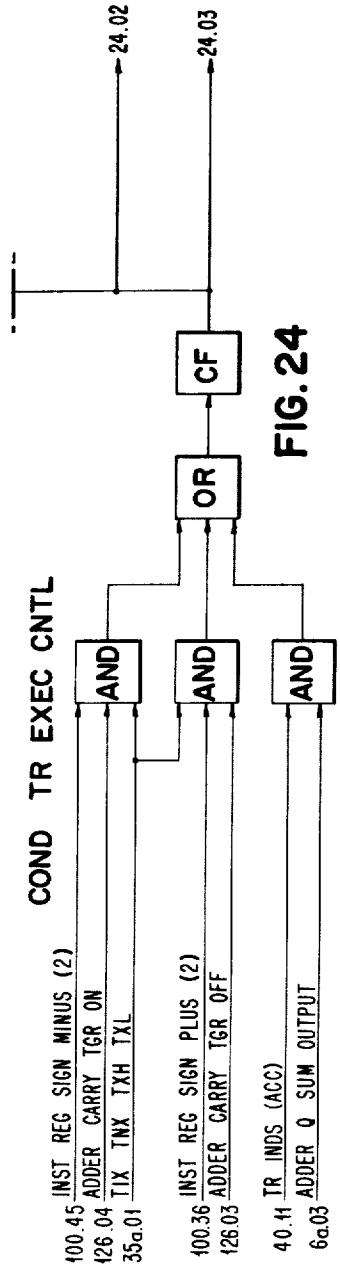

COND TR EXEC CNTL
24.02
24.03
CF
OR
AND
AND
AND
100.45 INST REG SIGN MINUS (2)
126.04 ADDER CARRY TGR ON
35a.01 TIX TNX TXH TXL
100.36 INST REG SIGN PLUS (2)
126.03 ADDER CARRY TGR OFF
40.11 TR INDS (ACC)
6a.03 ADDER Q SUM OUTPUT

FIG. 24

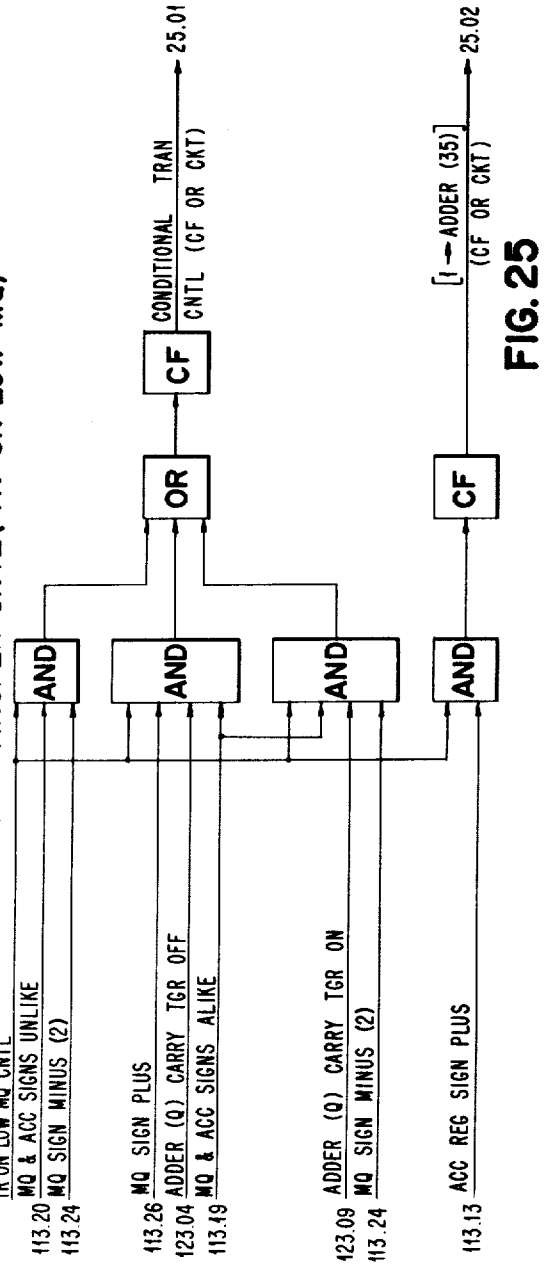
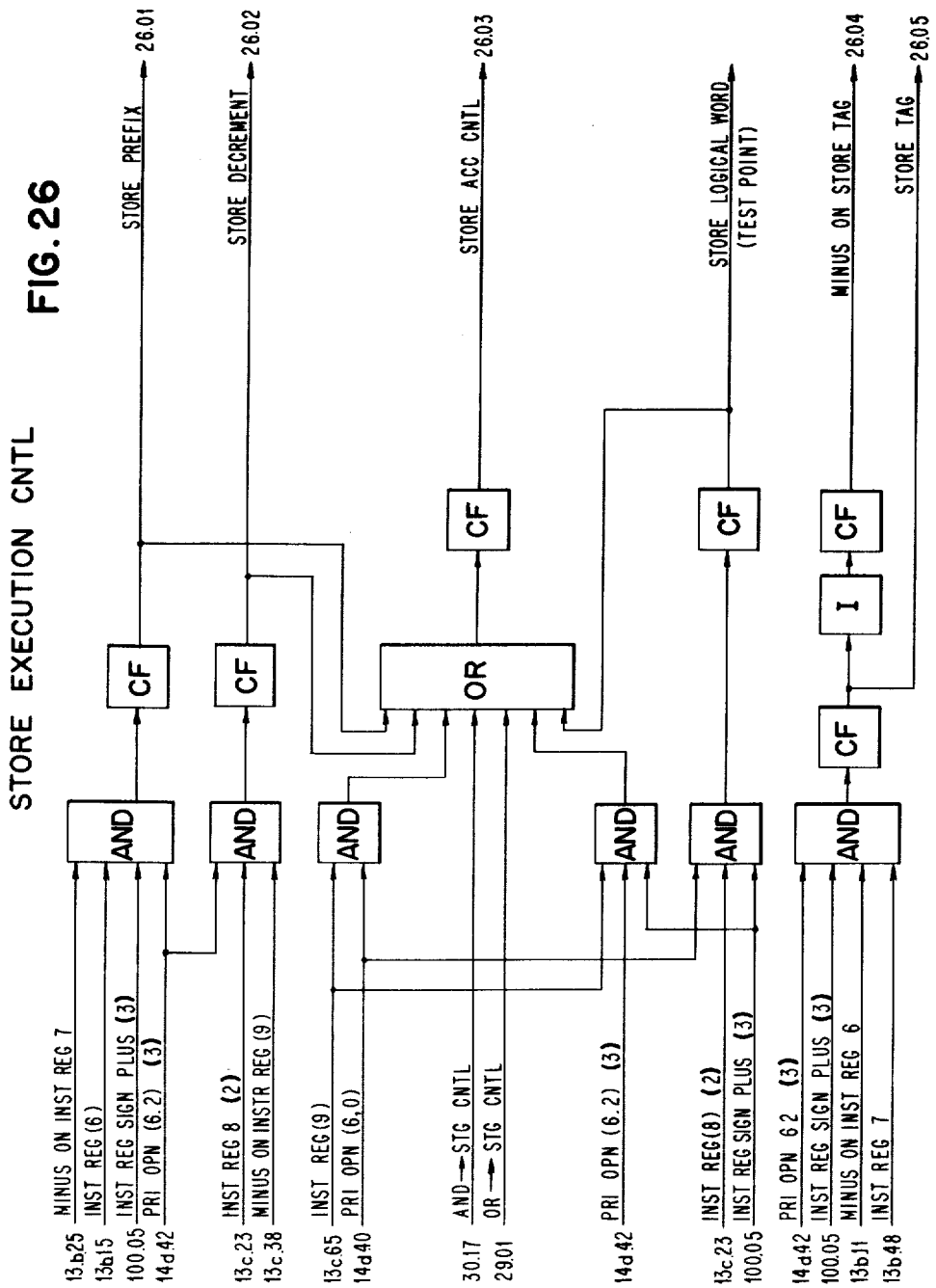
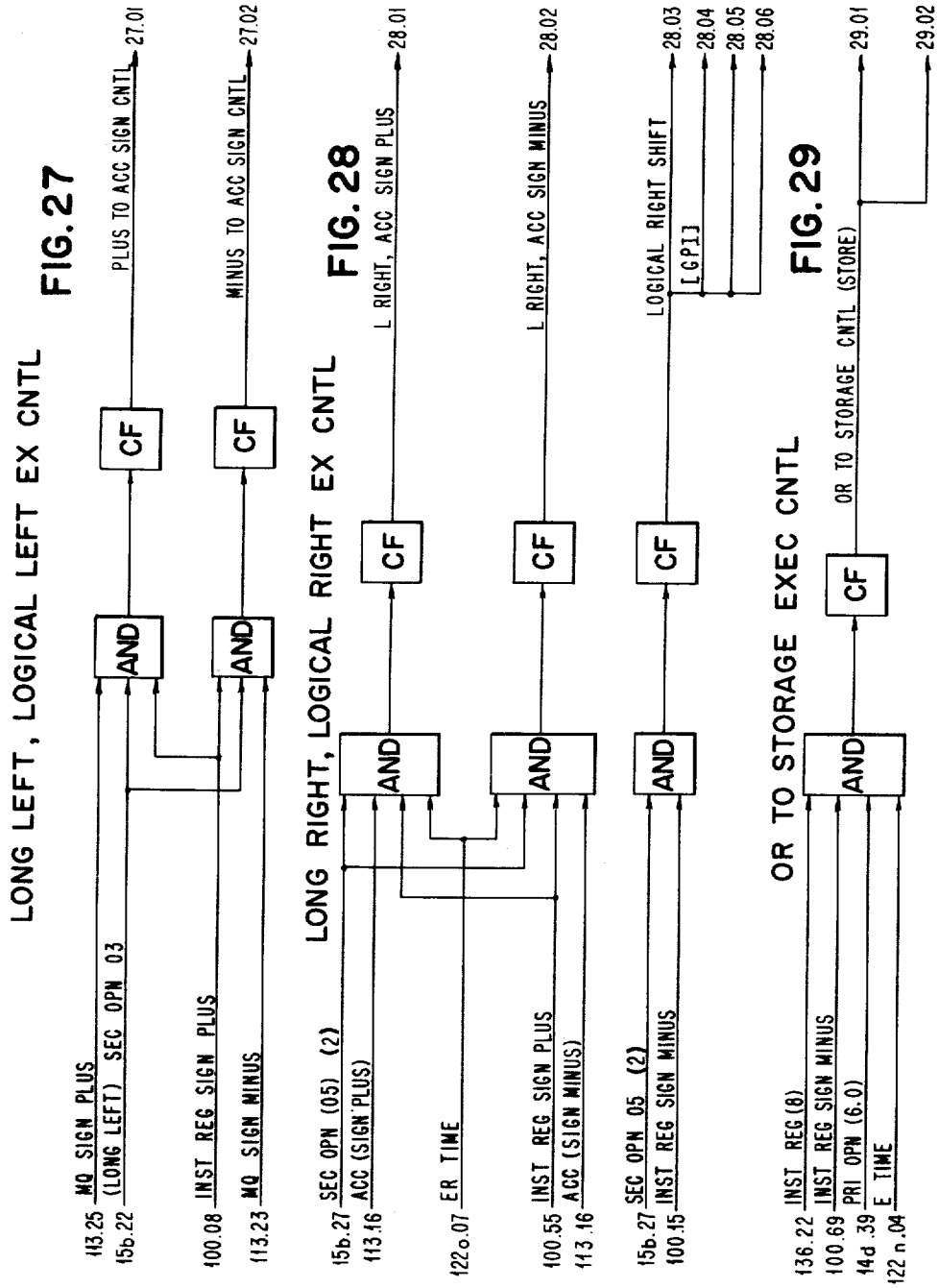

CONDITIONAL TRANSFER CNTL (TR ON LOW MQ)
CF
OR
AND
AND
AND
AND
CONDITIONAL TRAN CNTL (CF OR CKT)
25.01
[1 → ADDER (35)] (CF OR CKT)
25.02
TR ON LOW MQ CNTL
113.20 MQ & ACC SIGNS UNLIKE
113.24 MQ SIGN MINUS (2)
113.26 MQ SIGN PLUS
123.04 ADDER (Q) CARRY TGR OFF
113.19 MQ & ACC SIGNS ALIKE
123.09 ADDER (Q) CARRY TGR ON
113.24 MQ SIGN MINUS (2)
113.13 ACC REG SIGN PLUS

FIG. 25

FIG. 26


STORE EXECUTION CNTL
STORE PREFIX 26.01
STORE DECREMENT 26.02
STORE ACC CNTL 26.03
STORE LOGICAL WORD (TEST POINT)
MINUS ON STORE TAG 26.04
STORE TAG 26.05
CF
AND
OR
I
13b25 MINUS ON INST REG 7
13b15 INST REG (6)
100.05 INST REG SIGN PLUS (3)
14d42 PRI OPN (6.2) (3)
13c23 INST REG 8 (2)
13c38 MINUS ON INSTR REG (9)
13c65 INST REG (9)
14d40 PRI OPN (6,0)
30.17 AND→STG CNTL
29.01 OR→STG CNTL
14d42 PRI OPN (6.2) (3)
13c23 INST REG(8) (2)
100.05 INST REG SIGN PLUS (3)
14d42 PRI OPN 6 2 (3)
100.05 INST REG SIGN PLUS (3)
13b11 MINUS ON INST REG 6
13b48 INST REG 7


LONG LEFT, LOGICAL LEFT EX CNTL
FIG. 27
MQ SIGN PLUS
(LONG LEFT) SEC OPN 03
INST REG SIGN PLUS
MQ SIGN MINUS
AND
CF
PLUS TO ACC SIGN CNTL
MINUS TO ACC SIGN CNTL
LONG RIGHT, LOGICAL RIGHT EX CNTL
FIG. 28
SEC OPN (05) (2)
ACC (SIGN PLUS)
ER TIME
INST REG SIGN PLUS
ACC (SIGN MINUS)
L RIGHT, ACC SIGN PLUS
L RIGHT, ACC SIGN MINUS
OR TO STORAGE EXEC CNTL
FIG. 29
SEC OPN 05 (2)
INST REG SIGN MINUS
LOGICAL RIGHT SHIFT
[LGPI]
INST REG (8)
INST REG SIGN MINUS
PRI OPN (6.0)
E TIME
OR TO STORAGE CNTL (STORE)

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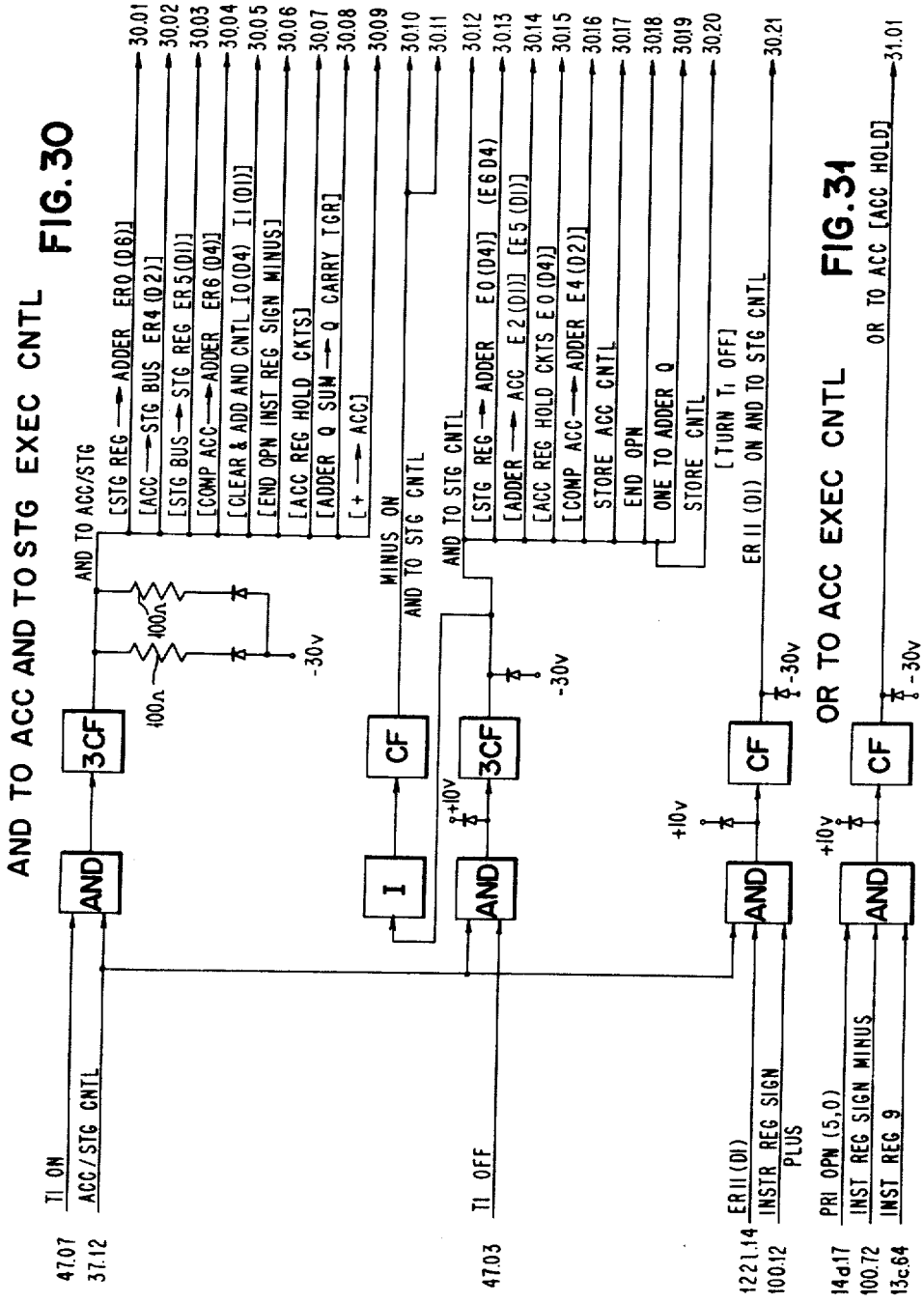


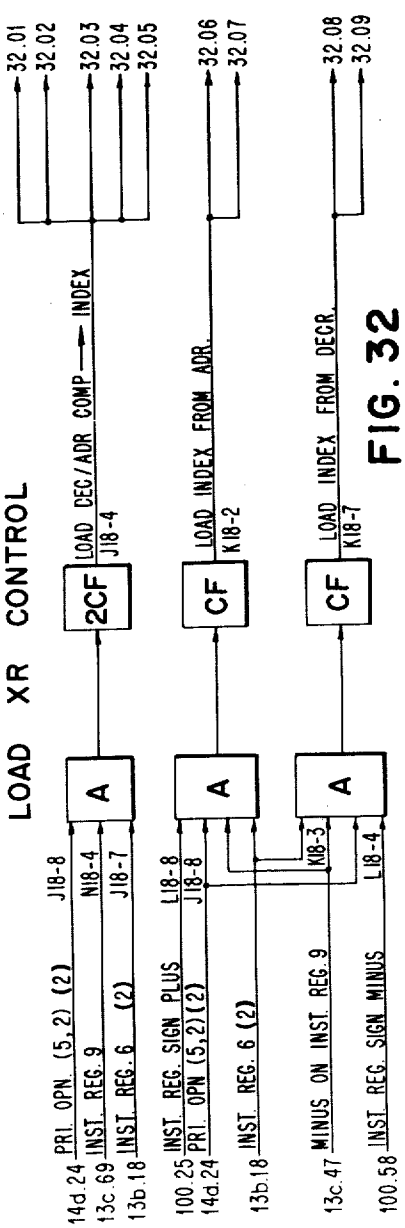

LOAD XR CONTROL
32.01
32.02
32.03
32.04
32.05
32.06
32.07
32.08
32.09
2CF
CF
CF
A
LOAD DEC/ADR COMP → INDEX
J18-4
LOAD INDEX FROM ADR.
K18-2
LOAD INDEX FROM DECR.
K18-7
14d.24 PRI. OPN. (5,2) (2) J18-8
13c.69 INST. REG. 9 N18-4
13b.18 INST. REG. 6 (2) J18-7
100.25 INST. REG. SIGN PLUS L18-8
14d.24 PRI. OPN (5,2) (2) J18-8
13b.18 INST. REG. 6 (2)
13c.47 MINUS ON INST. REG. 9 K18-3
100.58 INST. REG. SIGN MINUS L18-4

FIG. 32

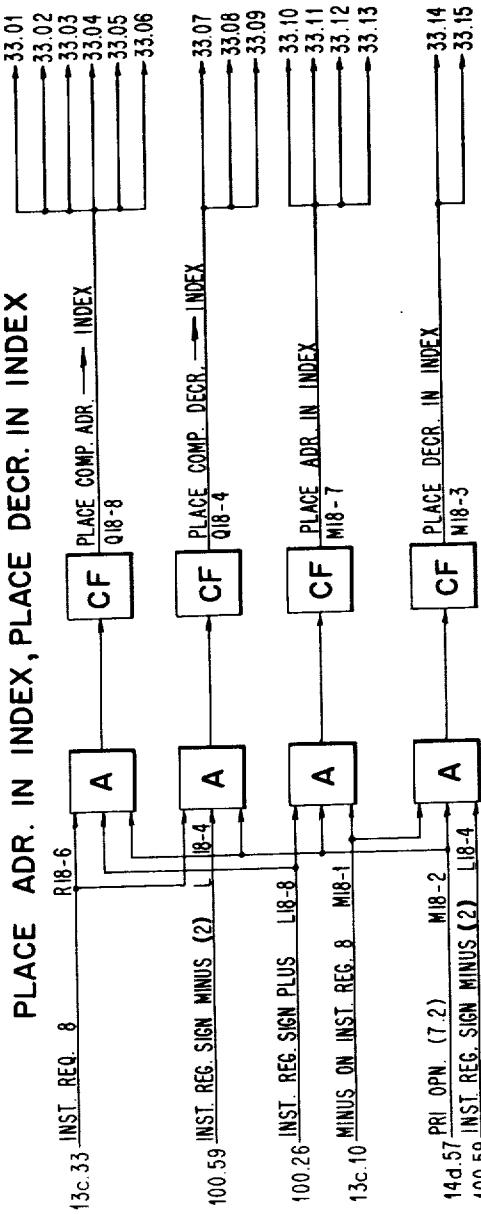

PLACE ADR. IN INDEX, PLACE DECR. IN INDEX
33.01
33.02
33.03
33.04
33.05
33.06
33.07
33.08
33.09
33.10
33.11
33.12
33.13
33.14
33.15
CF
A
PLACE COMP. ADR. → INDEX
Q18-8
PLACE COMP. DECR. → INDEX
Q18-4
PLACE ADR. IN INDEX
M18-7
PLACE DECR. IN INDEX
M18-3
13c.33 INST. REQ. 8 R18-6
100.59 INST. REG. SIGN MINUS (2) L18-4
100.26 INST. REG. SIGN PLUS L18-8
13c.10 MINUS ON INST. REG. 8 M18-1
14d.57 PRI. OPN. (7,2) M18-2
100.59 INST. REG. SIGN MINUS (2) L18-4

FIG. 33

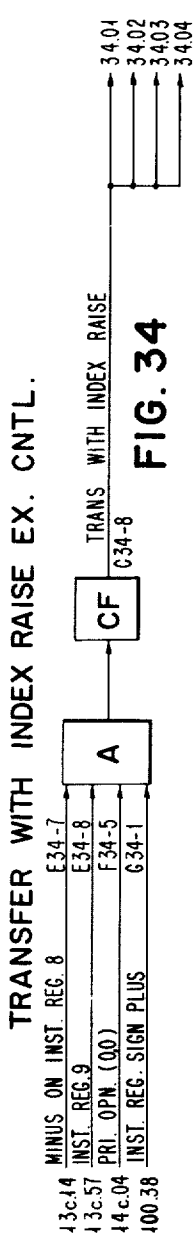


FIG. 34

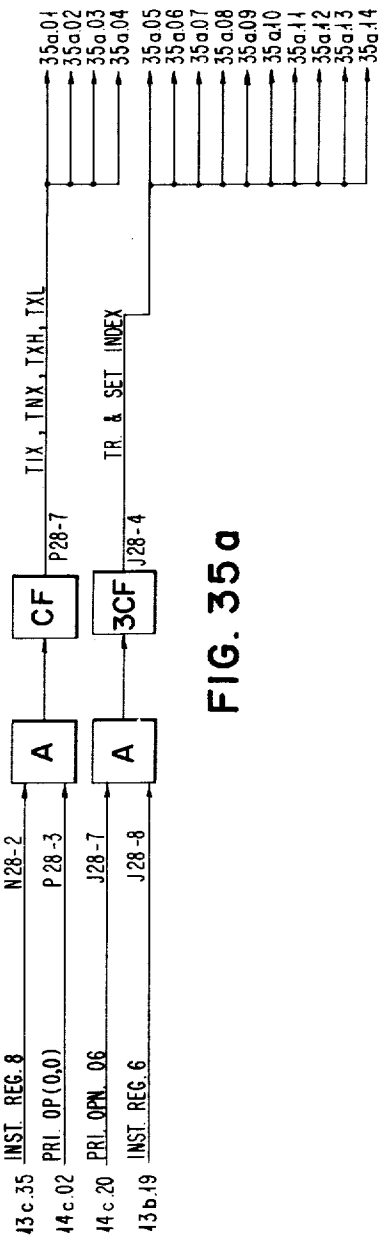


FIG. 35a

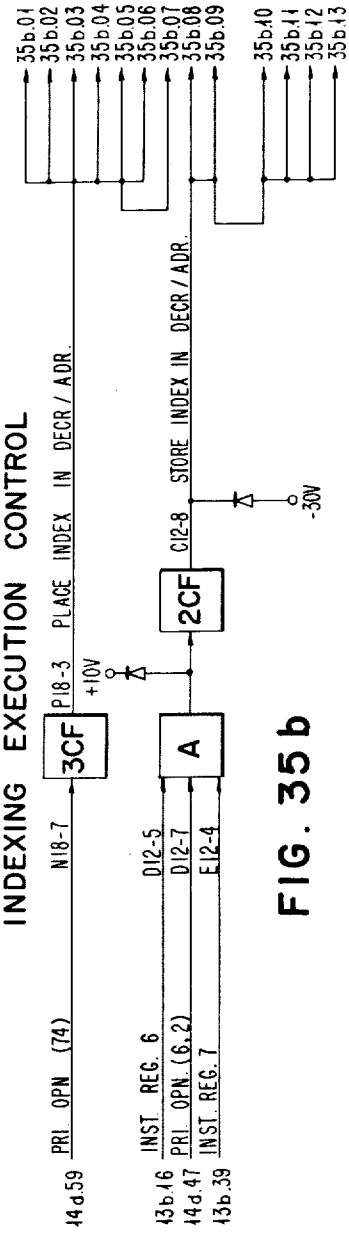


FIG. 35b

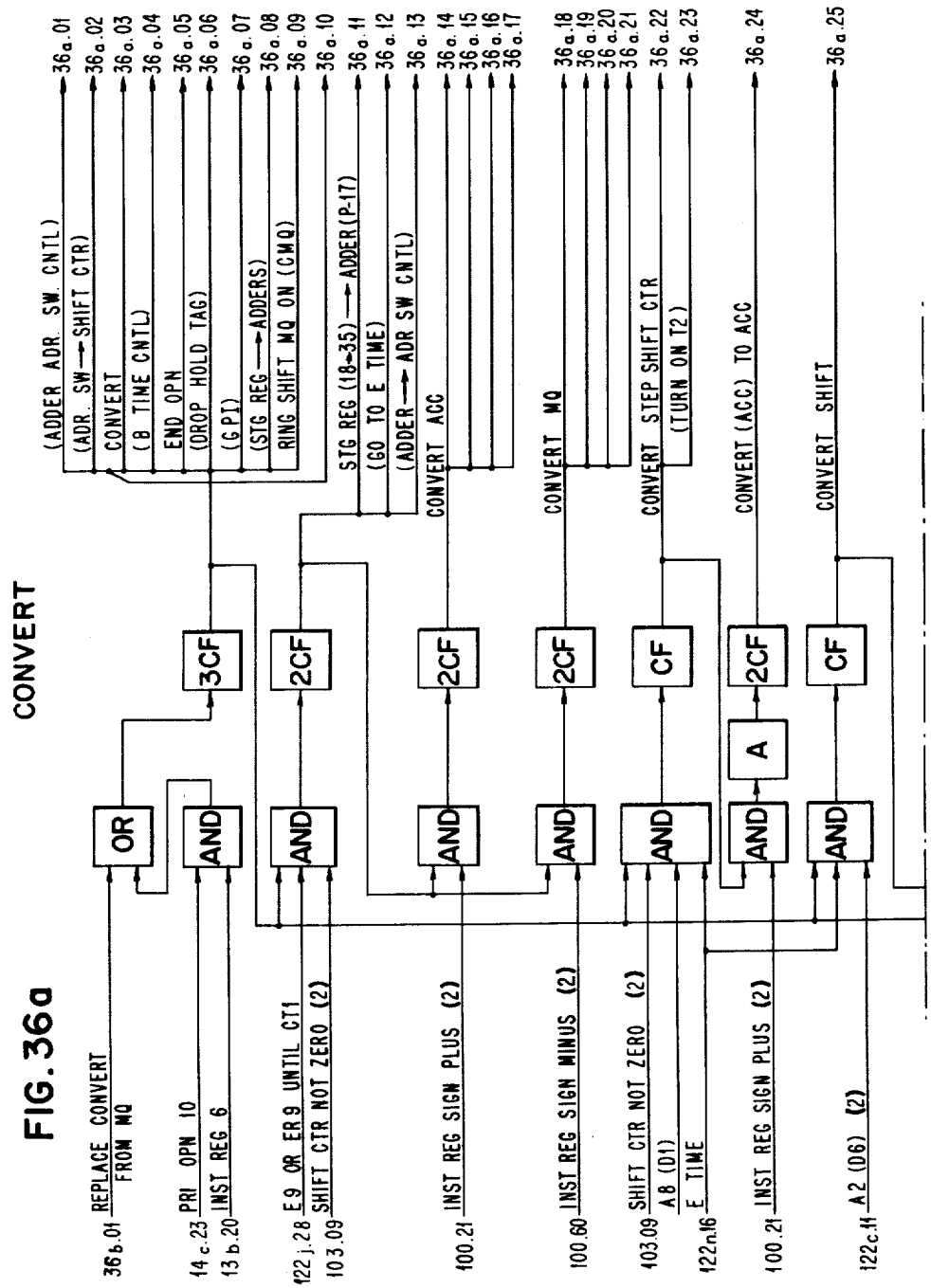

CONVERT
(ADDER ADR SW CNTL) 36a.01
(ADR SW→SHIFT CTR) 36a.02
CONVERT 36a.03
(8 TIME CNTL) 36a.04
END OPN 36a.05
(DROP HOLD TAG) 36a.06
(G P1) 36a.07
(STG REG→ADDERS) 36a.08
RING SHIFT MQ ON (CMQ) 36a.09
STG REG (18-35)→ADDER(P-17) 36a.11
(GO TO E TIME) 36a.12
(ADDER→ADR SW CNTL) 36a.13
CONVERT ACC 36a.14 36a.15 36a.16 36a.17
CONVERT MQ 36a.18 36a.19 36a.20 36a.21
CONVERT STEP SHIFT CTR 36a.22
(TURN ON T2) 36a.23
CONVERT (ACC) TO ACC 36a.24
CONVERT SHIFT 36a.25
OR
AND
3CF
2CF
CF
A
36b.01 REPLACE CONVERT FROM MQ
14 c.23 PRI OPN 10
13 b.20 INST REG 6
122 j.28 E 9 OR ER 9 UNTIL CT1
103.09 SHIFT CTR NOT ZERO (2)
100.21 INST REG SIGN PLUS (2)
100.60 INST REG SIGN MINUS (2)
103.09 SHIFT CTR NOT ZERO (2)
A 8 (D1)
E TIME
122n.16
100.21 INST REG SIGN PLUS (2)
122c.11 A2 (D6) (2)

FIG. 36a

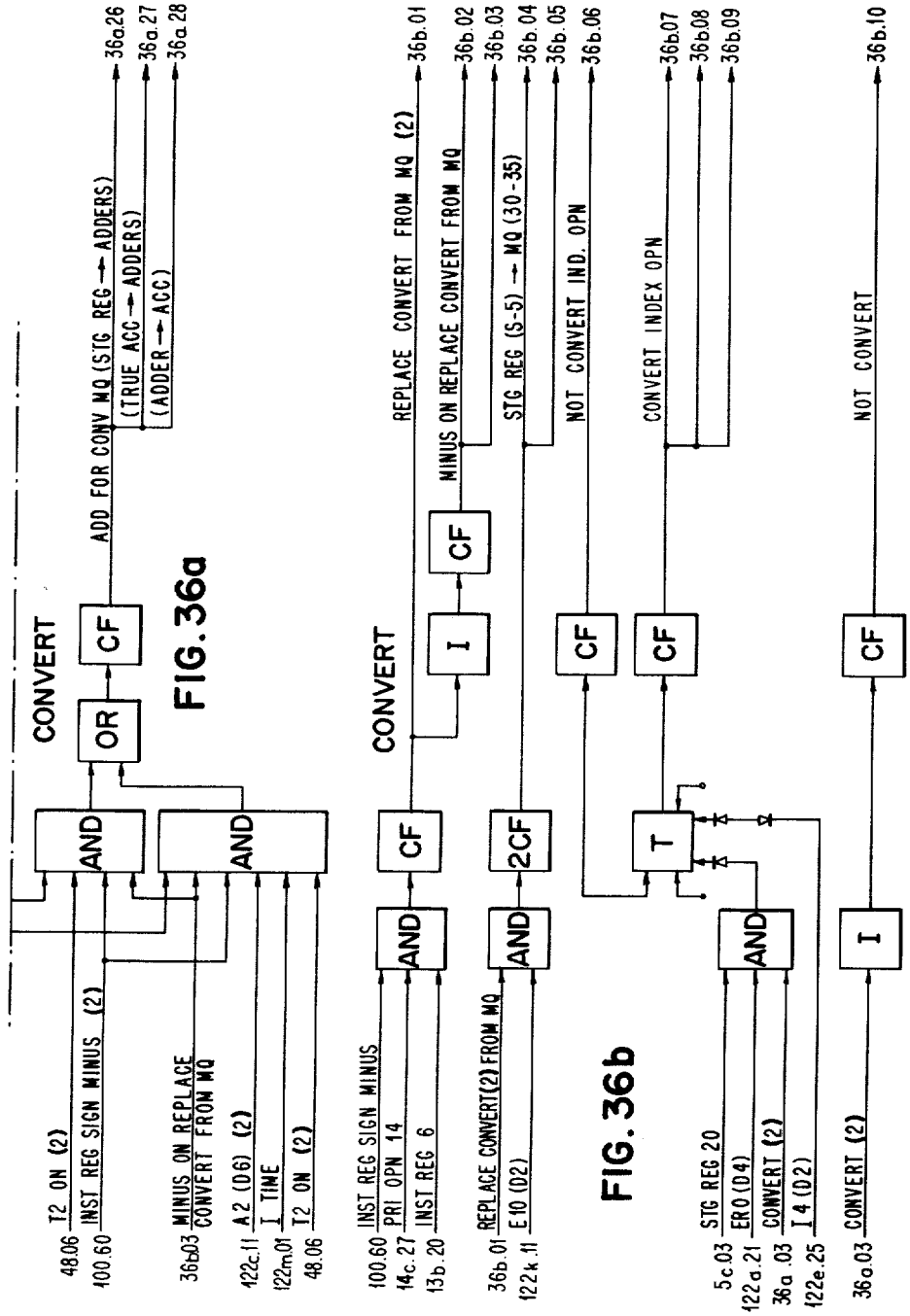

CONVERT
AND
OR
CF
ADD FOR CONV MQ (STG REG → ADDERS)
(TRUE ACC → ADDERS)
(ADDER → ACC)
36a.26
36a.27
36a.28
48.06 I2 ON (2)
100.60 INST REG SIGN MINUS (2)
36b03 MINUS ON REPLACE CONVERT FROM MQ
122c.11 A2 (06) (2)
122m.01 I TIME
48.06 I2 ON (2)
FIG. 36a
CONVERT
CF
I
REPLACE CONVERT FROM MQ (2)
MINUS ON REPLACE CONVERT FROM MQ
36b.01
36b.02
100.60 INST REG SIGN MINUS
14c.27 PRI OPN 14
13b.20 INST REG 6
AND
2CF
STG REG (S-5) → MQ (30-35)
36b.03
36b.04
36b.01 REPLACE CONVERT(2) FROM MQ
122k.11 E10 (02)
NOT CONVERT IND. OPN
36b.05
36b.06
T
CONVERT INDEX OPN
36b.07
36b.08
36b.09
5c.03 STG REG 20
122a.21 ERO (04)
36a.03 CONVERT (2)
122e.25 I4 (02)
NOT CONVERT
36b.10
36a.03 CONVERT (2)
FIG. 36b

FIG.37

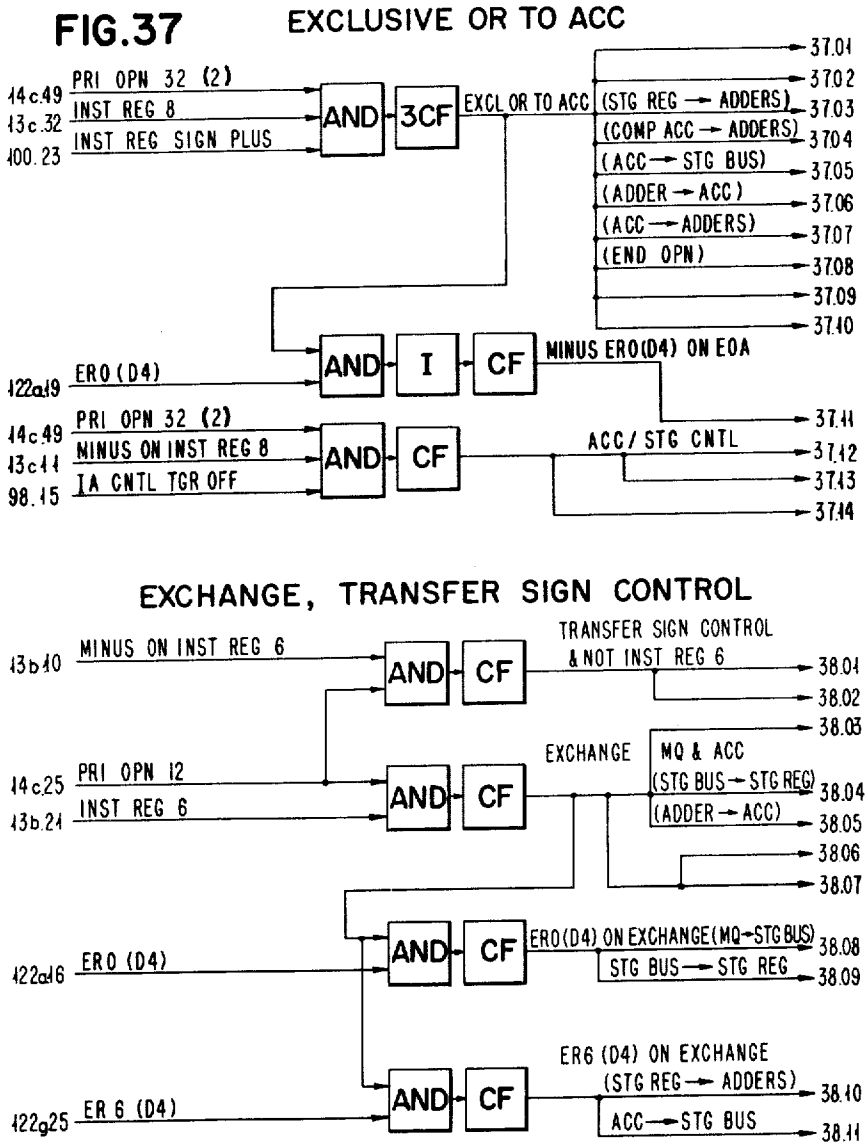
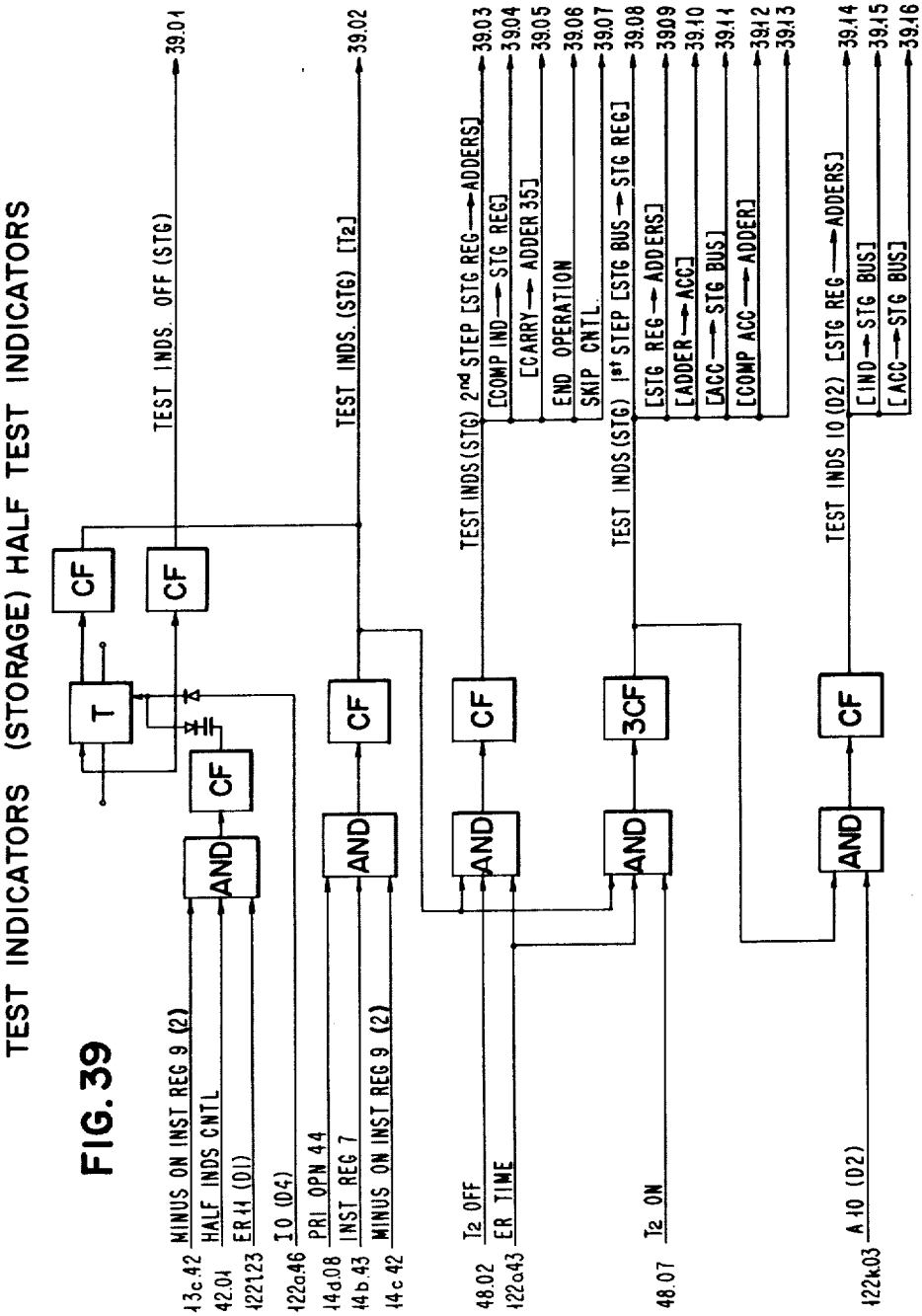
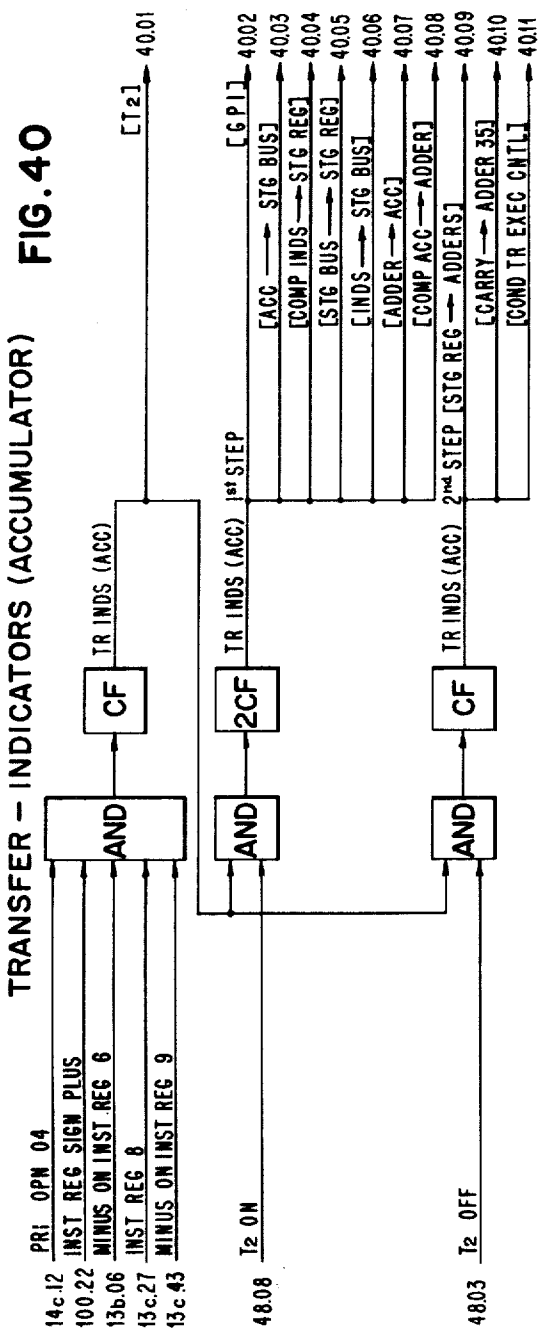
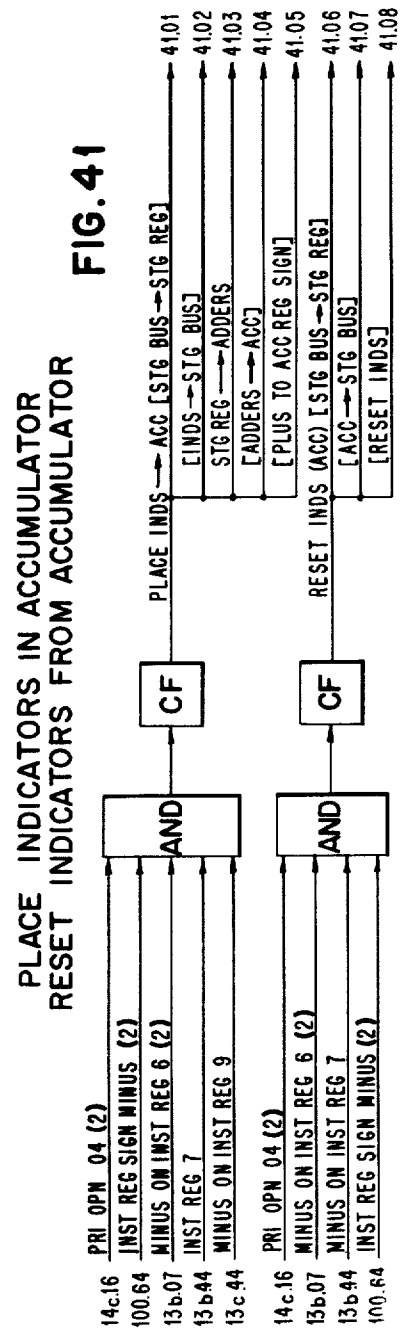

EXCLUSIVE OR TO ACC
14c49 PRI OPN 32 (2)
13c32 INST REG 8
100.23 INST REG SIGN PLUS
AND
3CF
EXCL OR TO ACC
(STG REG → ADDERS)
(COMP ACC → ADDERS)
(ACC → STG BUS)
(ADDER → ACC)
(ACC → ADDERS)
(END OPN)
37.01
37.02
37.03
37.04
37.05
37.06
37.07
37.08
37.09
37.10
122a19 ERO (D4)
AND
I
CF
MINUS ERO(D4) ON EOA
37.11
14c49 PRI OPN 32 (2)
13c11 MINUS ON INST REG 8
98.15 IA CNTL TGR OFF
AND
CF
ACC/STG CNTL
37.12
37.13
37.14
EXCHANGE, TRANSFER SIGN CONTROL
13b10 MINUS ON INST REG 6
AND
CF
TRANSFER SIGN CONTROL & NOT INST REG 6
38.01
38.02
38.03
14c25 PRI OPN 12
13b21 INST REG 6
AND
CF
EXCHANGE
MQ & ACC (STG BUS → STG REG)
(ADDER → ACC)
38.04
38.05
38.06
38.07
122a16 ERO (D4)
AND
CF
ERO(D4) ON EXCHANGE (MQ → STG BUS)
STG BUS → STG REG
38.08
38.09
122g25 ER 6 (D4)
AND
CF
ER6 (D4) ON EXCHANGE (STG REG → ADDERS)
ACC → STG BUS
38.10
38.11

FIG. 38

FIG. 39


TEST INDICATORS (STORAGE) HALF TEST INDICATORS
TEST INDS. OFF (STG) 39.01
TEST INDS. (STG) [T2] 39.02
TEST INDS(STG) 2nd STEP [STG REG→ADDERS] 39.03
[COMP IND→STG REG] 39.04
[CARRY→ADDER 35] 39.05
END OPERATION 39.06
SKIP CNTL. 39.07
TEST INDS(STG) 1st STEP [STG BUS→STG REG] 39.08
[STG REG→ADDERS] 39.09
[ADDER→ACC] 39.10
[ACC→STG BUS] 39.11
[COMP ACC→ADDER] 39.12
39.13
TEST INDS 10 (D2) [STG REG→ADDERS] 39.14
[IND→STG BUS] 39.15
[ACC→STG BUS] 39.16
T
CF
CF
CF
CF
CF
3CF
AND
AND
AND
AND
13c.42 MINUS ON INST REG 9 (2)
42.04 HALF INDS CNTL
122123 ER 14 (01)
122a46 IO (04)
14d.08 PRI OPN 44
14b.43 INST REG 7
14c.42 MINUS ON INST REG 9 (2)
48.02 T2 OFF
122a43 ER TIME
48.07 T2 ON
122k03 A 10 (02)


TRANSFER – INDICATORS (ACCUMULATOR)
FIG. 40
14c.12 PRI OPN 04
100.22 INST REG SIGN PLUS
13b.06 MINUS ON INST REG 6
13c.27 INST REG 8
13c.43 MINUS ON INST REG 9
AND
CF
TR INDS (ACC)
[T2] 40.01
48.08 T2 ON
AND
2CF
TR INDS (ACC) 1st STEP
[G P1] 40.02
[ACC → STG BUS] 40.03
[COMP INDS → STG REG] 40.04
[STG BUS → STG REG] 40.05
[INDS → STG BUS] 40.06
[ADDER → ACC] 40.07
[COMP ACC → ADDER] 40.08
48.03 T2 OFF
AND
CF
TR INDS (ACC) 2nd STEP [STG REG → ADDERS] 40.09
[CARRY → ADDER 35] 40.10
[COND TR EXEC CNTL] 40.11


PLACE INDICATORS IN ACCUMULATOR
RESET INDICATORS FROM ACCUMULATOR
FIG. 41
14c.16 PRI OPN 04 (2)
100.64 INST REG SIGN MINUS (2)
13b.07 MINUS ON INST REG 6 (2)
13b44 INST REG 7
13c.44 MINUS ON INST REG 9
AND
CF
PLACE INDS → ACC [STG BUS → STG REG] 41.01
[INDS → STG BUS] 41.02
STG REG → ADDERS 41.03
[ADDERS → ACC] 41.04
[PLUS TO ACC REG SIGN] 41.05
14c.16 PRI OPN 04 (2)
13b.07 MINUS ON INST REG 6 (2)
13b44 MINUS ON INST REG 7
100.64 INST REG SIGN MINUS (2)
AND
CF
RESET INDS (ACC) [STG BUS → STG REG] 41.06
[ACC → STG BUS] 41.07
[RESET INDS] 41.08

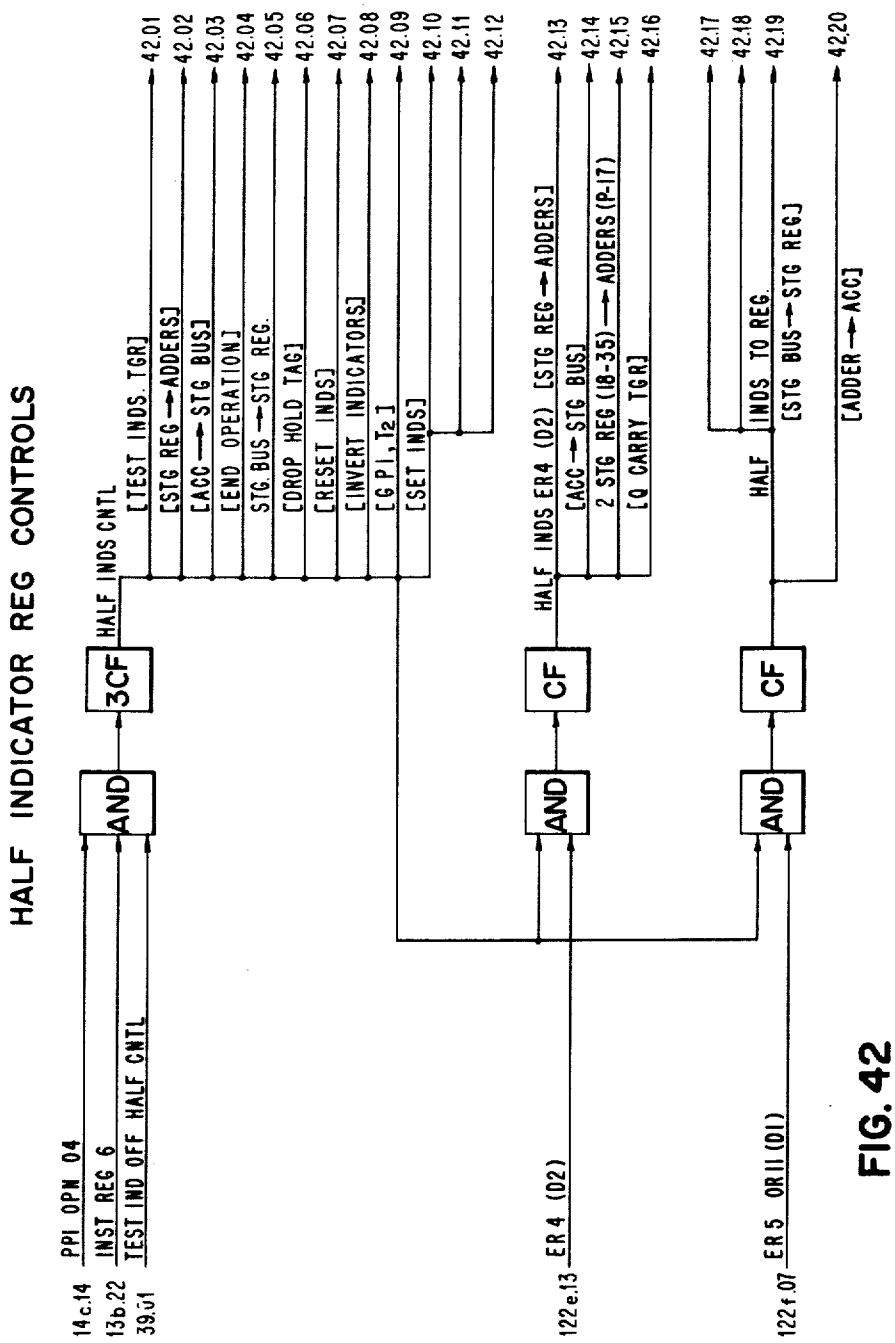

HALF INDICATOR REG CONTROLS
14c.14 PPI OPN 04
13b.22 INST REG 6
39.01 TEST IND OFF HALF CNTL
AND
3CF
HALF INDS CNTL
[TEST INDS. TGR] 42.01
[STG REG → ADDERS] 42.02
[ACC → STG BUS] 42.03
[END OPERATION] 42.04
STG. BUS → STG REG. 42.05
[DROP HOLD TAG] 42.06
[RESET INDS] 42.07
[INVERT INDICATORS] 42.08
[G P1, T2.] 42.09
[SET INDS] 42.10
42.11
42.12
122e.13 ER 4 (D2)
AND
CF
HALF INDS ER4 (D2) [STG REG → ADDERS] 42.13
[ACC → STG BUS] 42.14
2 STG REG (18-35) → ADDERS (P-17) 42.15
[Q CARRY TGR] 42.16
122f.07 ER 5 OR 11 (D1)
AND
CF
42.17
HALF INDS TO REG. 42.18
[STG BUS → STG REG.] 42.19
[ADDER → ACC] 42.20

FIG. 42

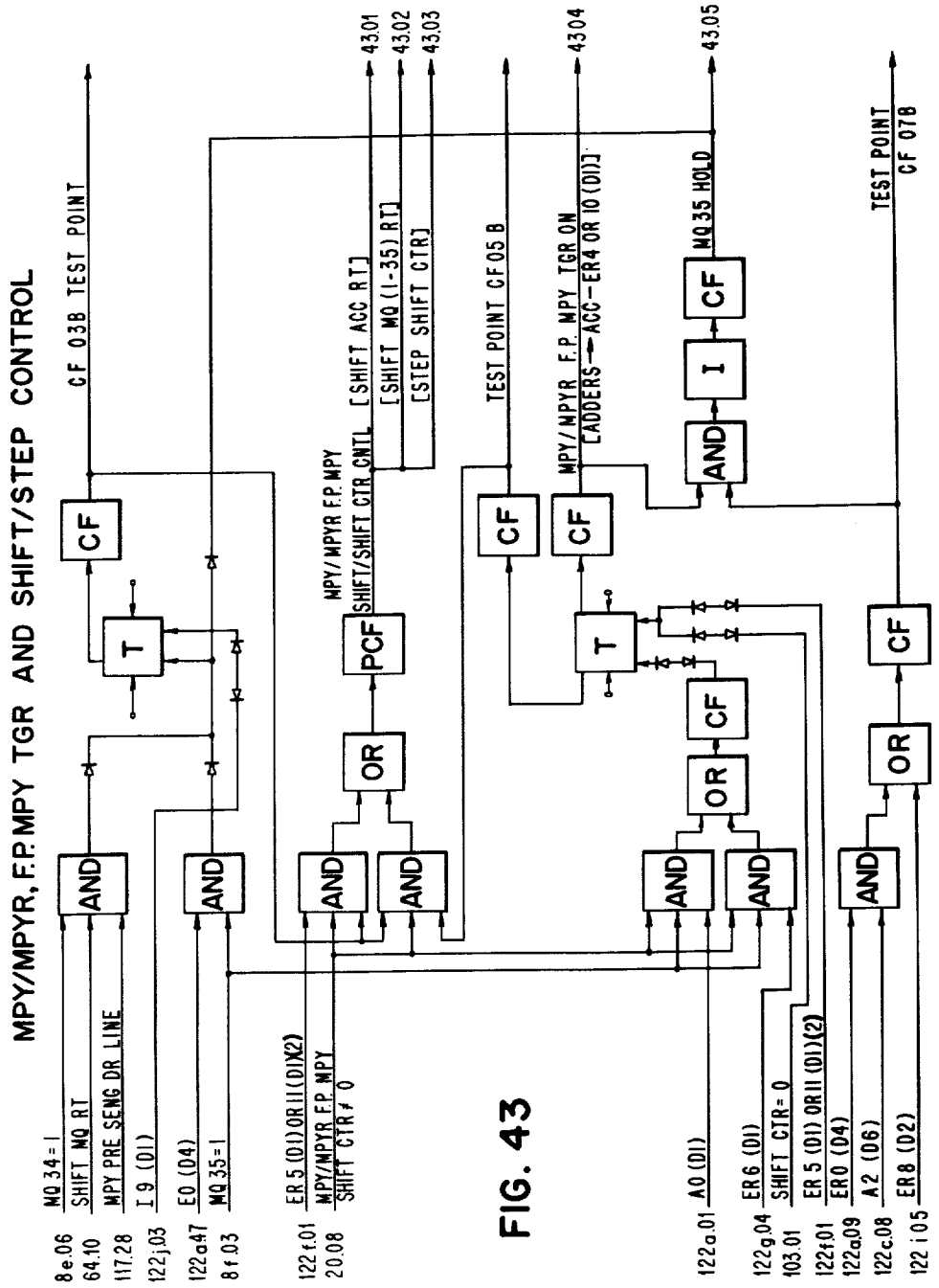
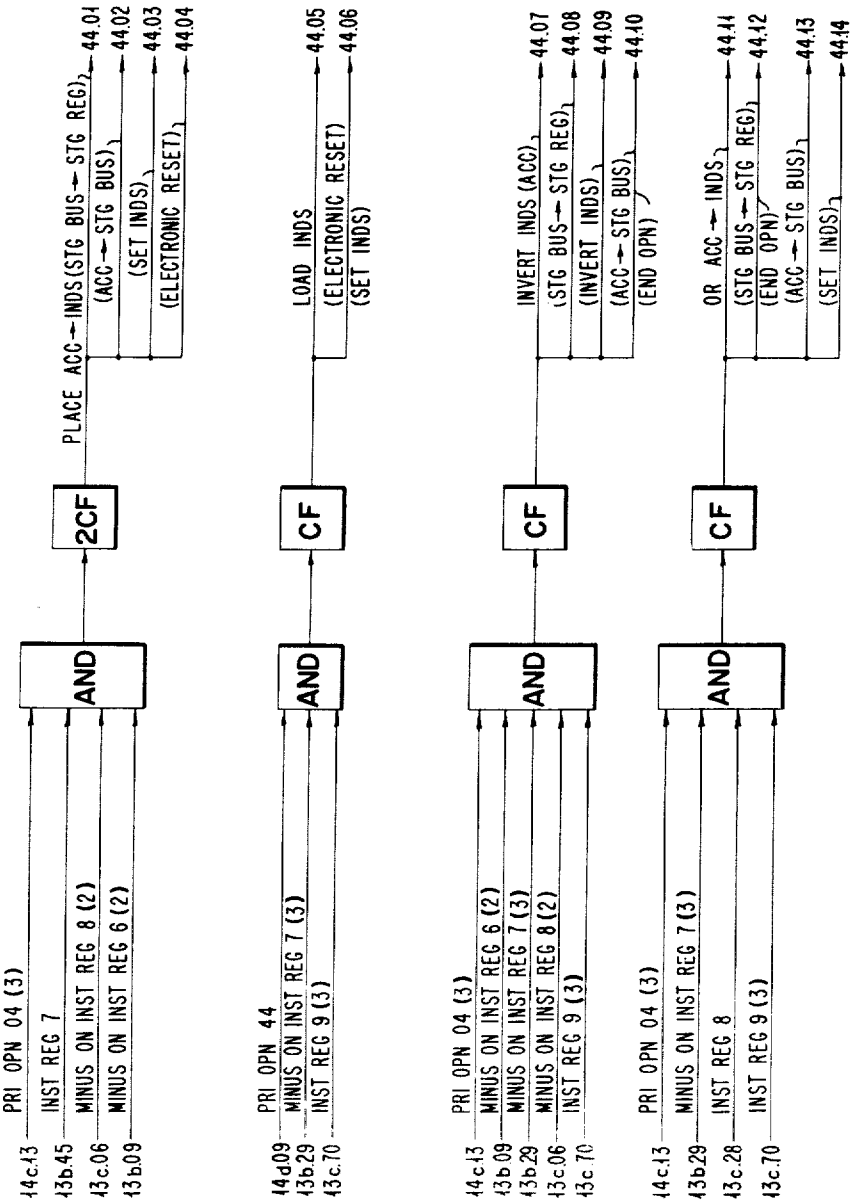
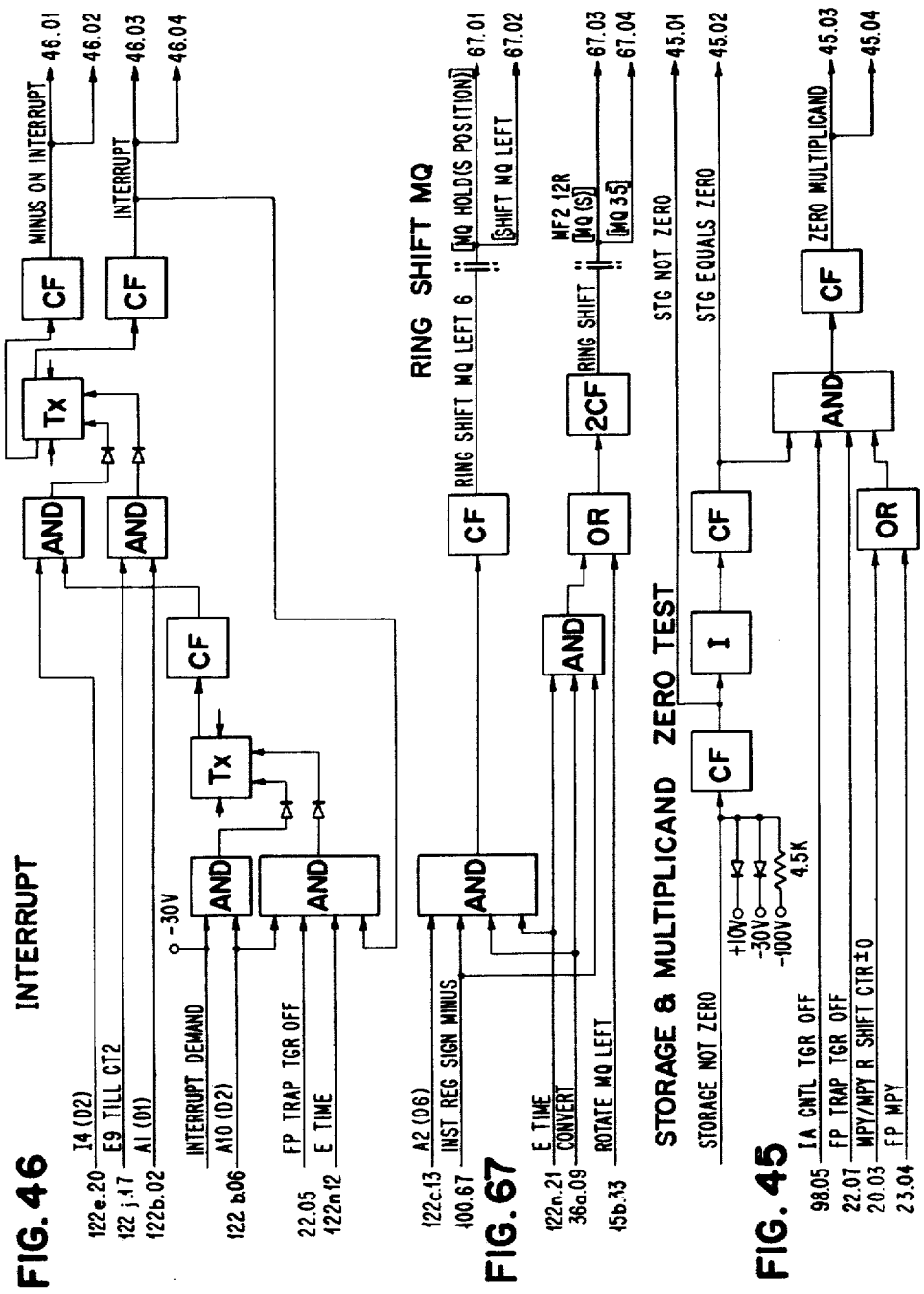

MPY/MPYR, F.P. MPY TGR AND SHIFT/STEP CONTROL
CF 03B TEST POINT
43.01
43.02
43.03
43.04
43.05
MPY/MPYR F.P. MPY
[SHIFT/SHIFT CTR CNTL
[SHIFT ACC RT]
[SHIFT MQ (1-35) RT]
[STEP SHIFT CTR]
TEST POINT CF 05 B
MPY/MPYR F.P. MPY TGR ON
[ADDERS → ACC-ER4 OR 10 (D1)]
MQ 35 HOLD
TEST POINT
CF 07B
CF
T
PCF
OR
AND
I
8e.06 MQ 34 = 1
64.10 SHIFT MQ RT
117.28 MPY PRE SENG DR LINE
122j.03 I 9 (D1)
122a.47 E0 (04)
8f.03 MQ 35 = 1
122f.01 ER 5 (01) OR 11 (D1)X2)
20.08 MPY/MPYR F.P. MPY
SHIFT CTR ≠ 0
122a.01 A0 (D1)
122g.04 ER 6 (D1)
103.01 SHIFT CTR = 0
122f.01 ER 5 (D1) OR 11 (D1)(2)
122a.09 ER0 (04)
122c.08 A2 (06)
122 i 05 ER 8 (D2)

FIG. 43

FIG. 44

PLACE ACCUMULATOR IN INDICATORS
LOAD INDICATORS, INVERT INDICATORS,
OR ACCUMULATOR TO INDICATORS




INTERRUPT
I4 (02)
E9 TILL CT2
A1 (01)
INTERRUPT DEMAND
A10 (02)
FP TRAP TGR OFF
E TIME
-30V
AND
Tx
CF
MINUS ON INTERRUPT
INTERRUPT
46.01
46.02
46.03
46.04
122e.20
122j.17
122b.02
122b.06
22.05
122n12
FIG. 46
RING SHIFT MQ
A2 (06)
INST REG SIGN MINUS
RING SHIFT MQ LEFT 6
MQ HOLD/S POSITION
SHIFT MQ LEFT
67.01
67.02
122c.13
100.67
FIG. 67
E TIME
CONVERT
ROTATE MQ LEFT
OR
2CF
MF2 12R
RING SHIFT
MQ (S)
MQ 35
67.03
67.04
122n.21
36a.09
15b.33
STORAGE & MULTIPLICAND ZERO TEST
STORAGE NOT ZERO
STG NOT ZERO
STG EQUALS ZERO
I
+10V
-30V
-100V
4.5K
ZERO MULTIPLICAND
45.01
45.02
45.03
45.04
FIG. 45
IA CNTL TGR OFF
FP TRAP TGR OFF
MPY/MPY R SHIFT CTR±0
FP MPY
98.05
22.07
20.03
23.04

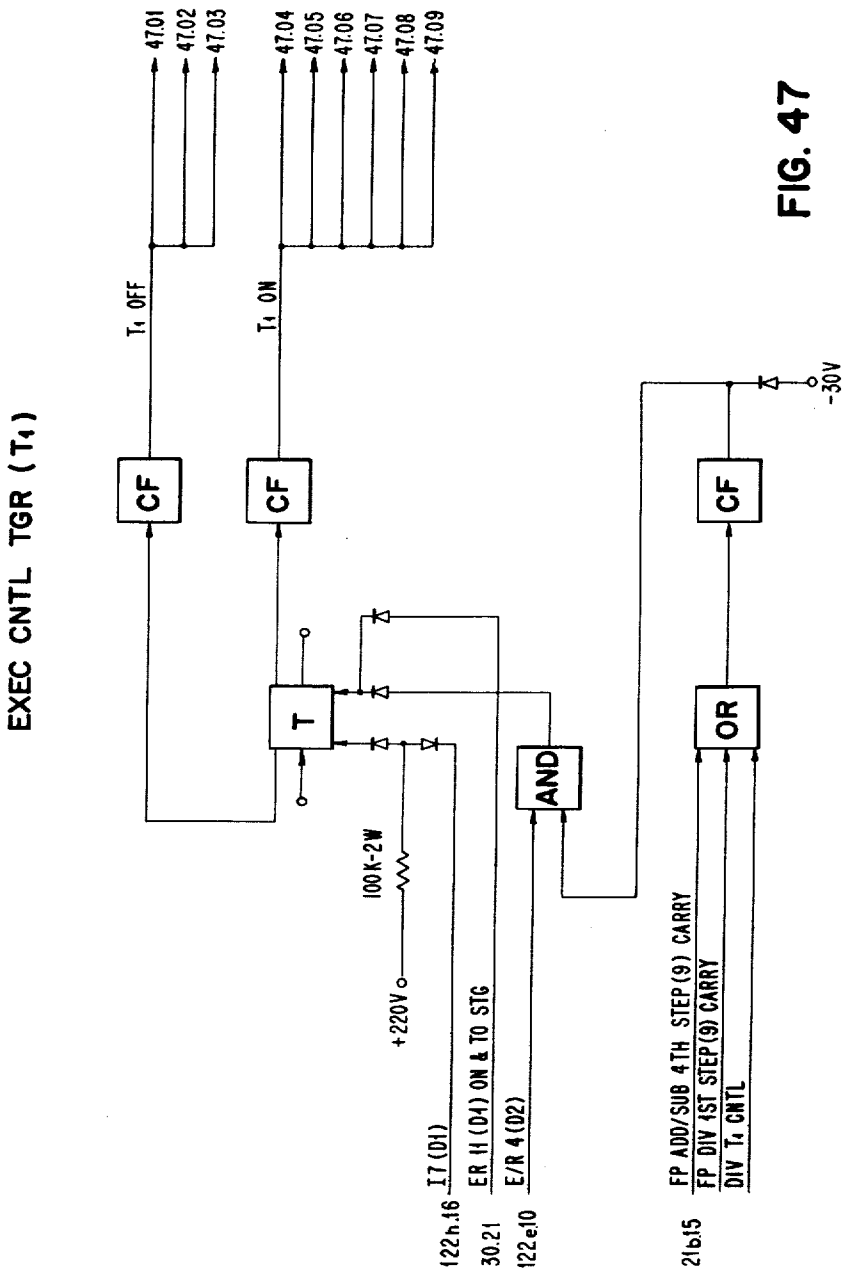

EXEC CNTL TGR (T1)
47.01
47.02
47.03
47.04
47.05
47.06
47.07
47.08
47.09
T1 OFF
T1 ON
CF
CF
CF
T
AND
OR
-30V
100K-2W
+220V
I7 (D1)
ER 11 (D4) ON & TO STG
E/R 4 (D2)
122h.16
30.21
122e.10
FP ADD/SUB 4TH STEP (9) CARRY
FP DIV 1ST STEP (9) CARRY
DIV T1 CNTL
21b.15

FIG. 47

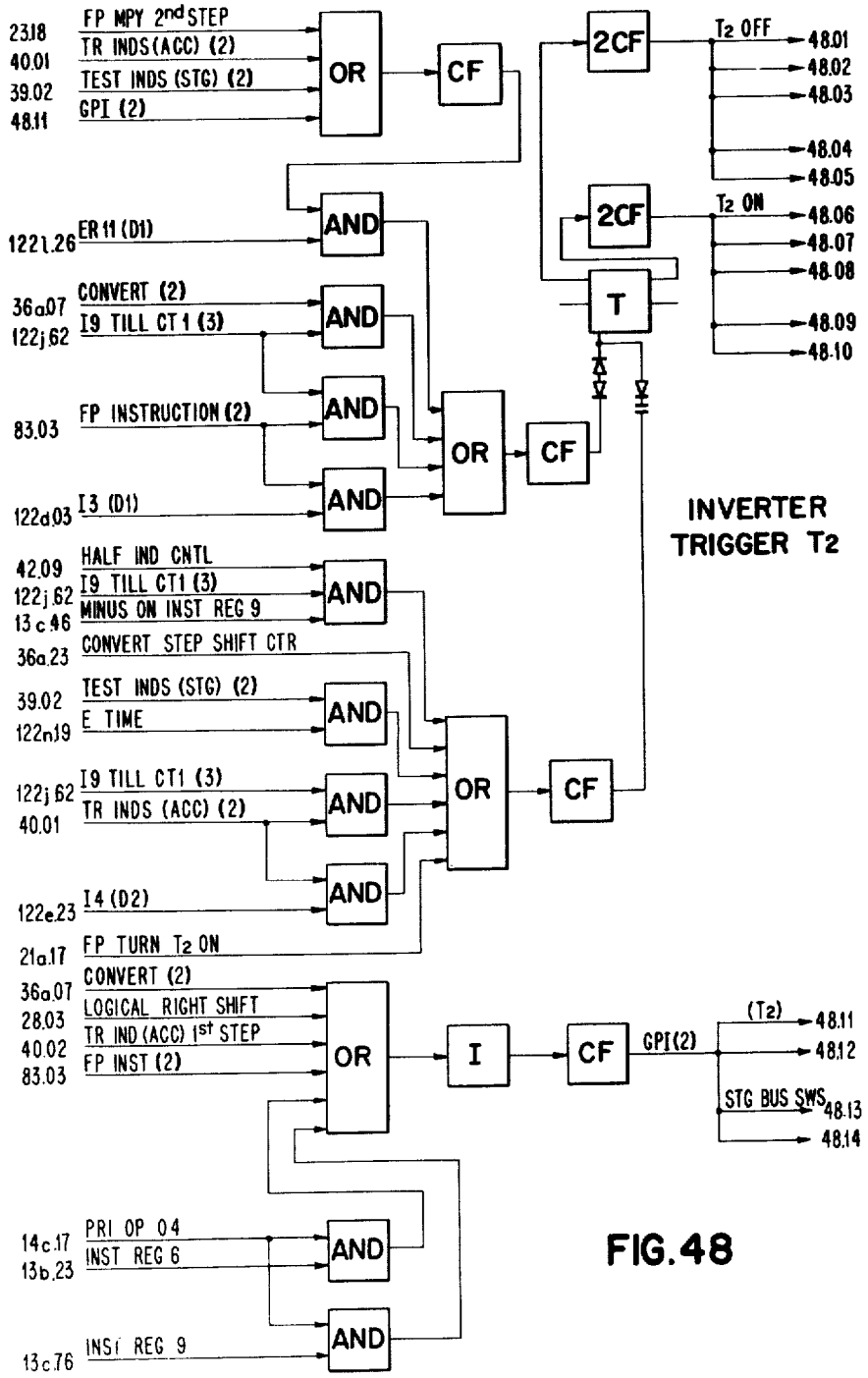

23J8
40.01
39.02
48.11
FP MPY 2nd STEP
TR INDS (ACC) (2)
TEST INDS (STG) (2)
GPI (2)
OR
CF
2CF
T2 OFF
48.01
48.02
48.03
48.04
48.05
2CF
T2 ON
48.06
48.07
48.08
48.09
48.10
T
1221.26
ER 11 (D1)
AND
36a.07
122j.62
CONVERT (2)
I9 TILL CT 1 (3)
AND
83.03
FP INSTRUCTION (2)
AND
122d.03
I3 (D1)
AND
OR
CF
INVERTER TRIGGER T2
42.09
122j.62
13c.46
HALF IND CNTL
I9 TILL CT1 (3)
MINUS ON INST REG 9
AND
36a.23
CONVERT STEP SHIFT CTR
39.02
122n.19
TEST INDS (STG) (2)
E TIME
AND
122j.62
40.01
I9 TILL CT1 (3)
TR INDS (ACC) (2)
AND
122e.23
I4 (D2)
AND
OR
CF
21a.17
FP TURN T2 ON
36a.07
28.03
40.02
83.03
CONVERT (2)
LOGICAL RIGHT SHIFT
TR IND (ACC) 1st STEP
FP INST (2)
OR
I
CF
GPI(2)
(T2)
48.11
48.12
STG BUS SWS
48.13
48.14
14c.17
13b.23
PRI OP 04
INST REG 6
AND
13c.76
INST REG 9
AND

FIG. 48

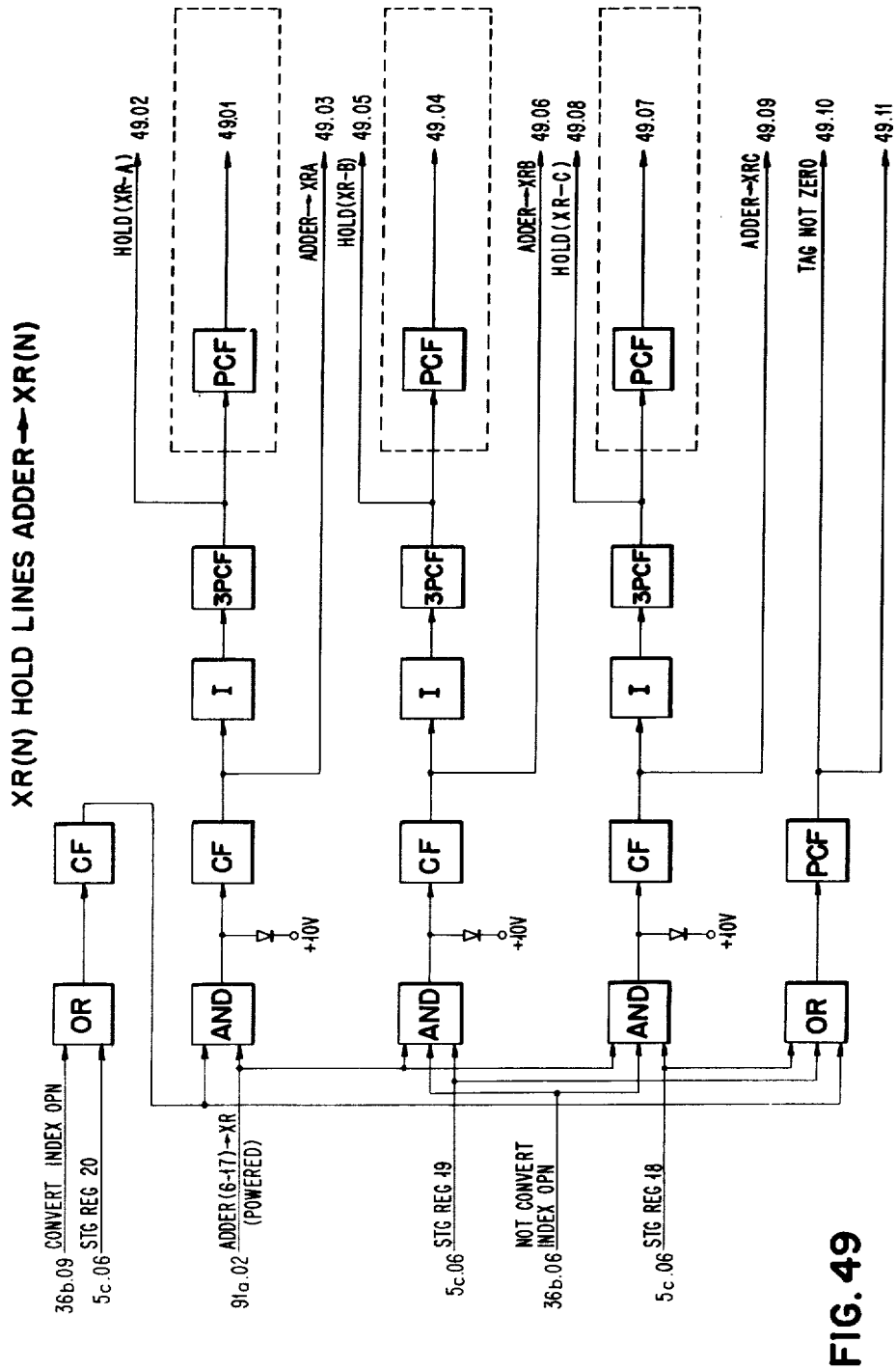
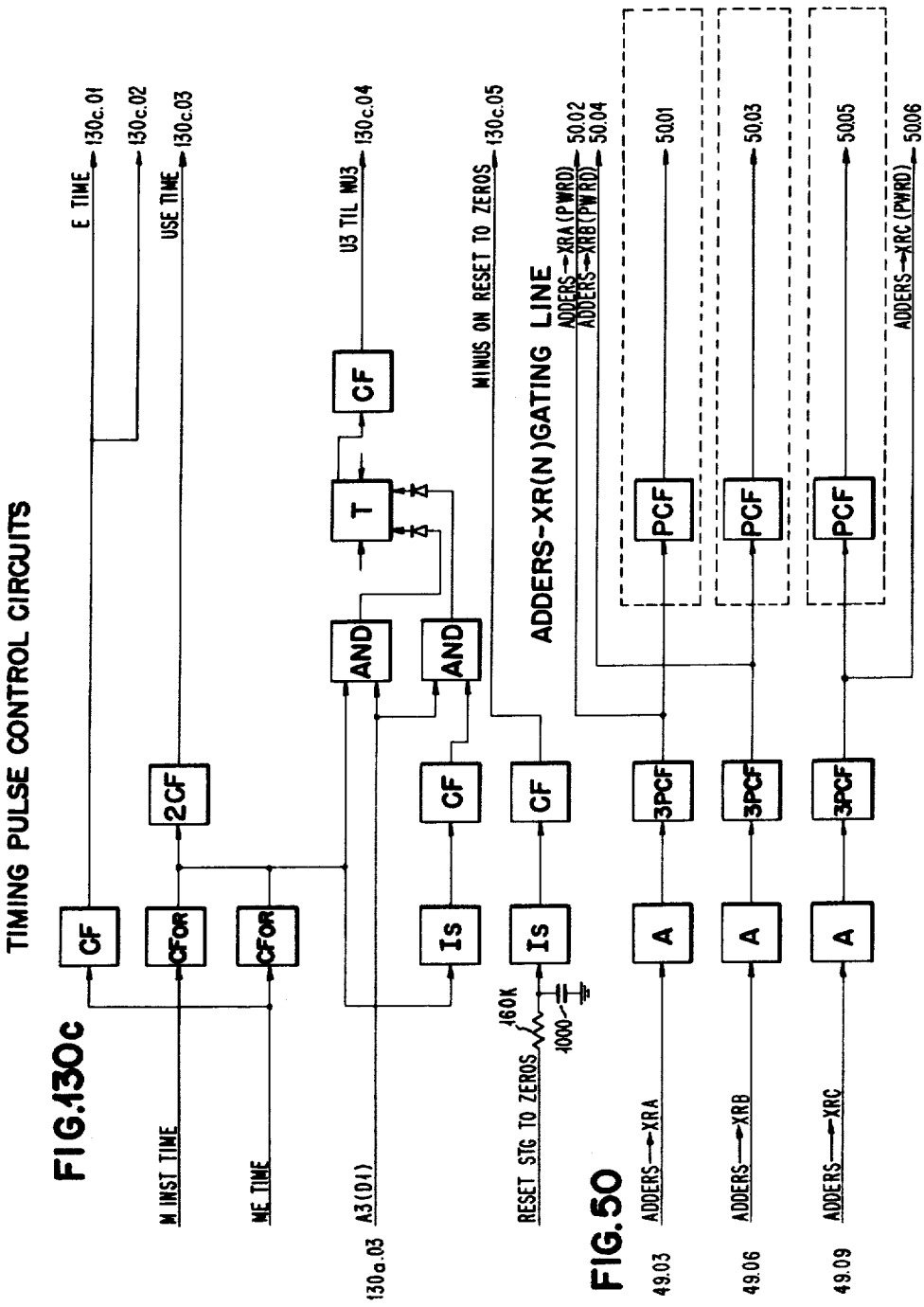

XR(N) HOLD LINES ADDER→XR(N)
HOLD(XR-A) 49.02
49.01
ADDER→XRA 49.03
HOLD(XR-B) 49.05
49.04
ADDER→XRB 49.06
HOLD(XR-C) 49.08
49.07
ADDER→XRC 49.09
TAG NOT ZERO 49.10
49.11
PCF
3PCF
I
CF
AND
OR
+10V
36b.09 CONVERT INDEX OPN
5c.06 STG REG 20
91a.02 ADDER(6-17)→XR (POWERED)
5c.06 STG REG 19
36b.06 NOT CONVERT INDEX OPN
5c.06 STG REG 18

FIG. 49


TIMING PULSE CONTROL CIRCUITS
FIG.130c
E TIME
130c.01
130c.02
USE TIME
130c.03
U3 TIL MU3
130c.04
MINUS ON RESET TO ZEROS
130c.05
ADDERS-XR(N)GATING LINE
ADDERS→XRA(PWRD)
ADDERS→XRB(PWRD)
50.02
50.04
ADDERS→XRC(PWRD)
5006
5001
5003
5005
CF
2CF
CFOR
CFOR
T
AND
AND
CF
CF
PCF
PCF
PCF
Is
Is
3PCF
3PCF
3PCF
A
A
A
M INST TIME
ME TIME
130a.03 A3(01)
RESET STG TO ZEROS
460K
1000
ADDERS→XRA
ADDERS→XRB
ADDERS→XRC
FIG.50
49.03
49.06
49.09

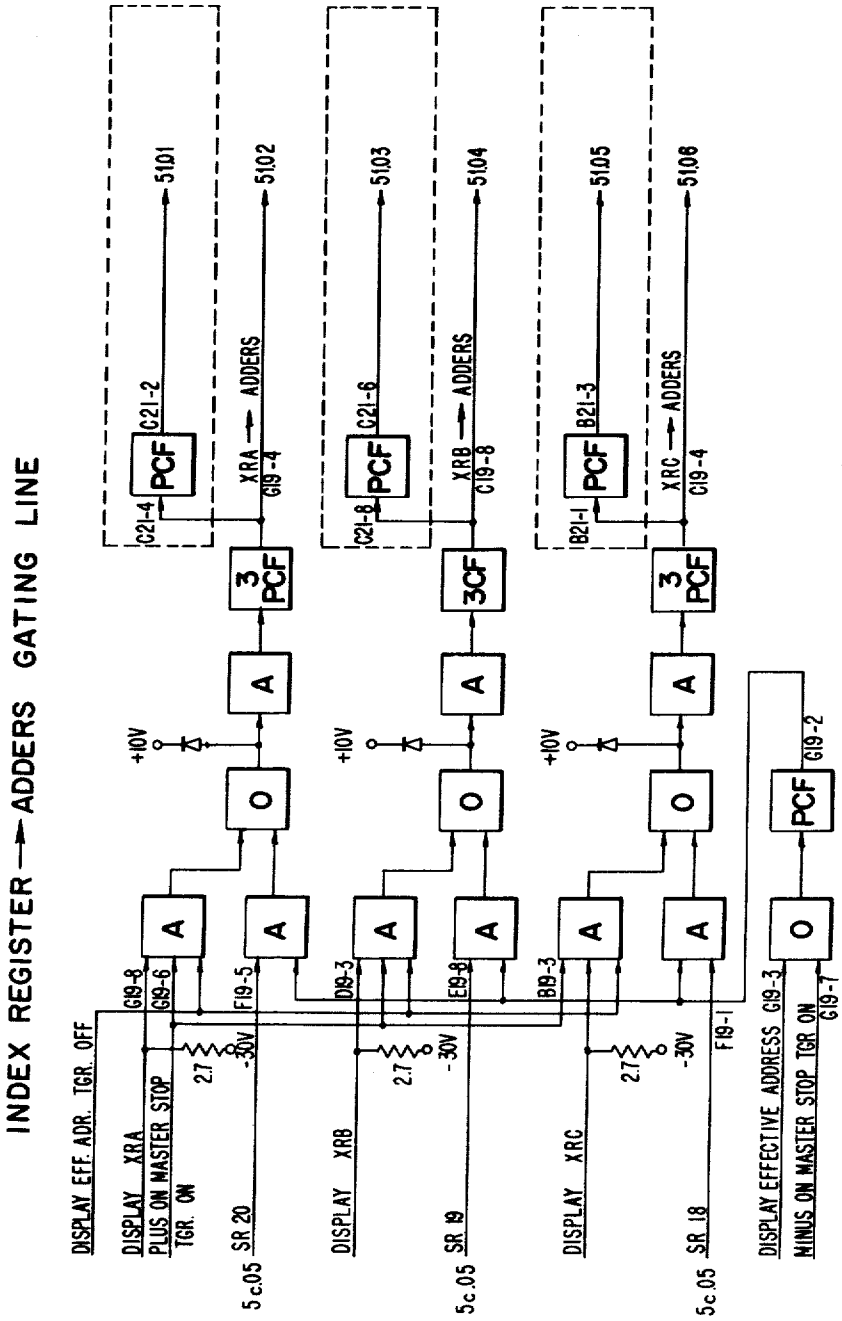
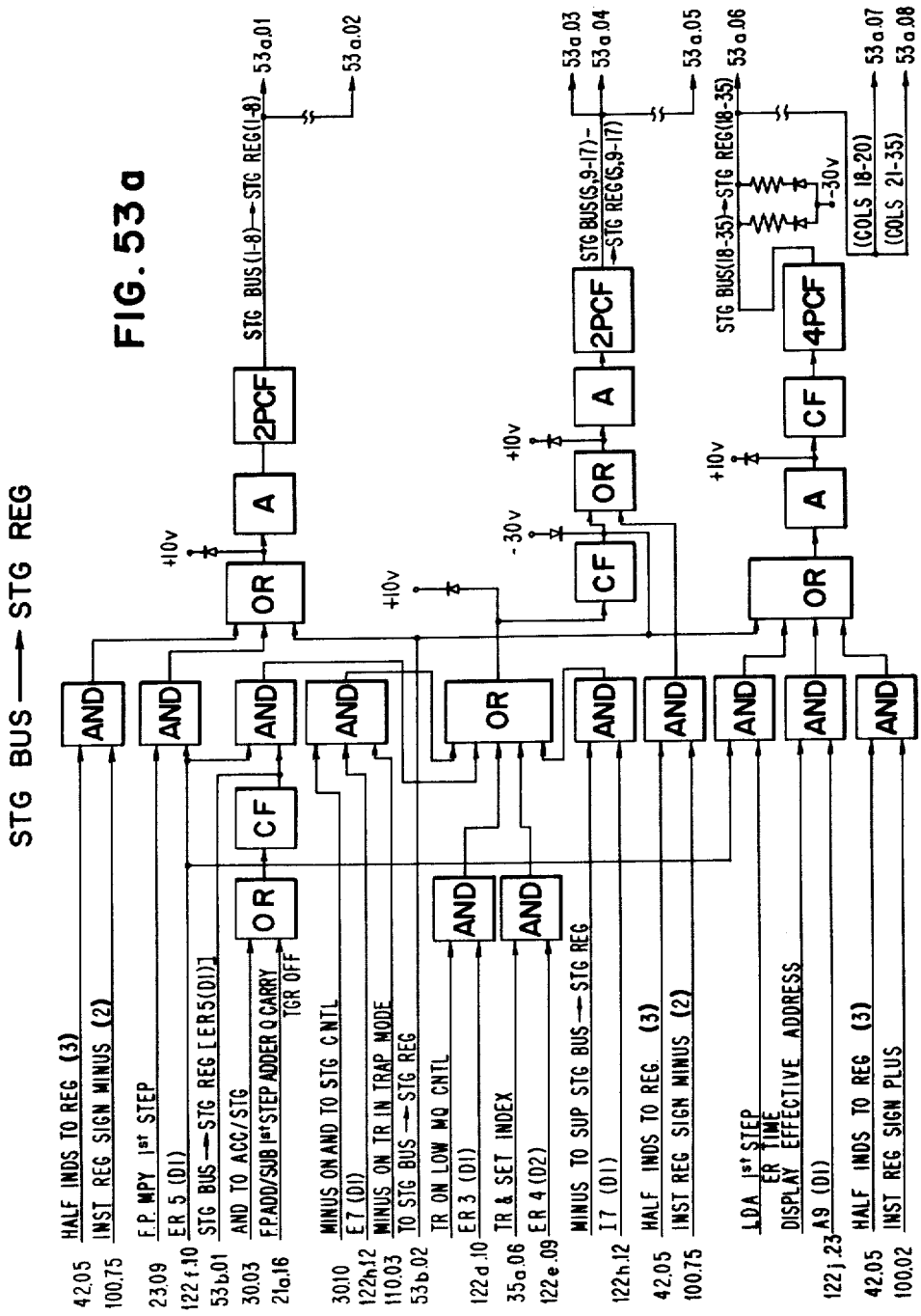

INDEX REGISTER → ADDERS GATING LINE
DISPLAY EFF. ADR. TGR. OFF
DISPLAY XRA
PLUS ON MASTER STOP TGR. ON
SR 20
5c.05
DISPLAY XRB
SR 19
DISPLAY XRC
SR 18
DISPLAY EFFECTIVE ADDRESS
MINUS ON MASTER STOP TGR ON
+10V
-30V
2.7
PCF
3 PCF
A
O
XRA → ADDERS
XRB → ADDERS
XRC → ADDERS
5101
5102
5103
5104
5105
5106

FIG. 51

FIG. 53a


STG BUS → STG REG
AND
OR
CF
A
2PCF
4PCF
+10v
-30v
HALF INDS TO REG (3)
INST REG SIGN MINUS (2)
F.P. MPY 1st STEP
ER 5 (01)
STG BUS → STG REG [ER5(01)]
AND TO ACC/STG
F.P.ADD/SUB 1st STEP ADDER Q CARRY
TGR OFF
MINUS ON AND TO STG CNTL
E 7 (01)
MINUS ON TR IN TRAP MODE
TO STG BUS → STG REG
TR ON LOW MQ CNTL
ER 3 (01)
TR & SET INDEX
ER 4 (02)
MINUS TO SUP STG BUS → STG REG
I 7 (01)
HALF INDS TO REG. (3)
INST REG SIGN MINUS (2)
LDA 1st STEP
ER TIME
DISPLAY EFFECTIVE ADDRESS
A 9 (01)
HALF INDS TO REG (3)
INST REG SIGN PLUS
STG BUS(1-8) → STG REG(1-8)
STG BUS(S,9-17) → STG REG(S,9-17)
STG BUS(18-35) → STG REG(18-35)
(COLS 18-20)
(COLS 21-35)
42.05
100.75
23.09
122 f.10
53b.01
30.03
21a.16
30.10
122h.12
110.03
53b.02
122d.10
35a.06
122e.09
122h.12
42.05
100.75
122j.23
42.05
100.02
53a.01
53a.02
53a.03
53a.04
53a.05
53a.06
53a.07
53a.08

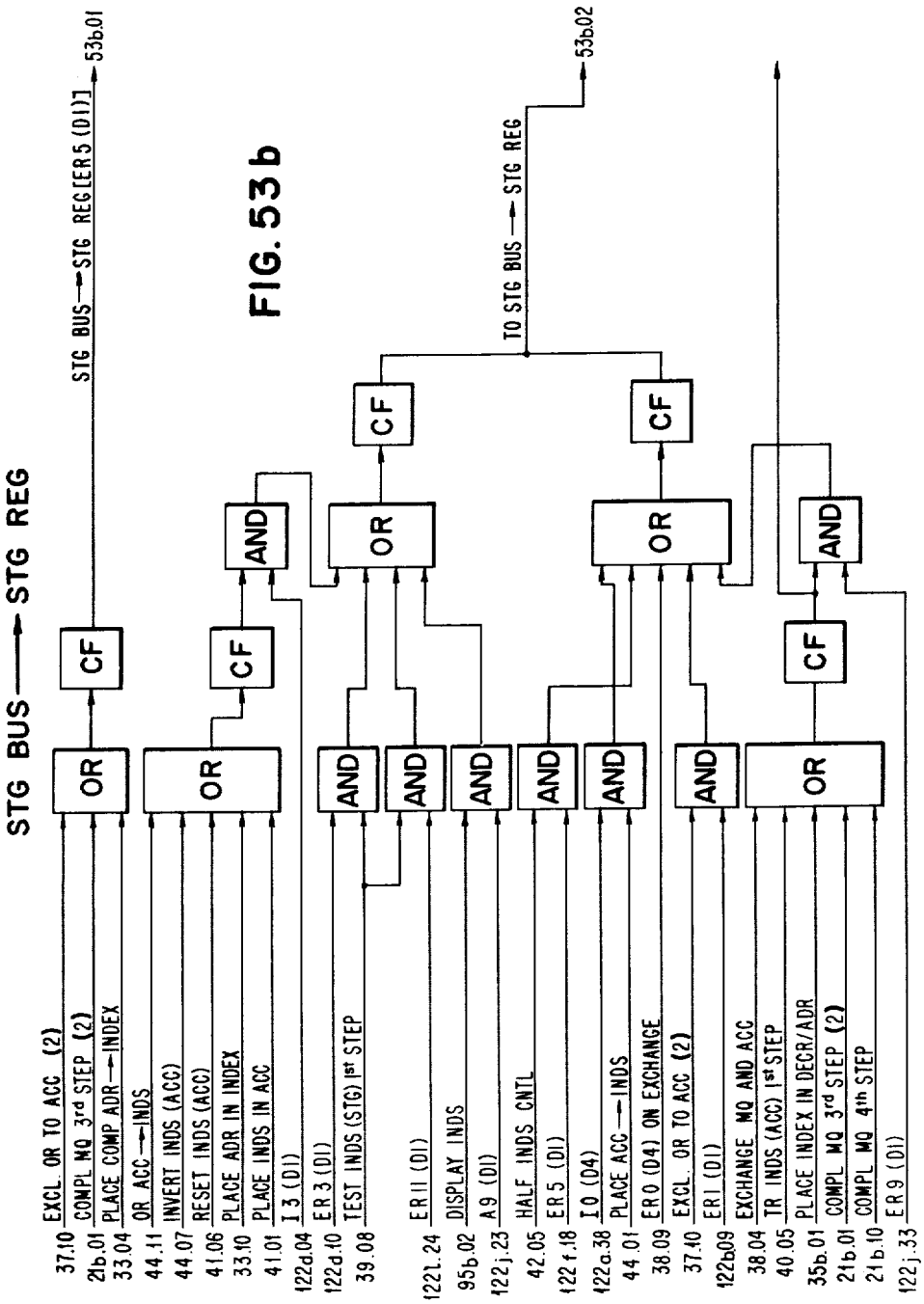
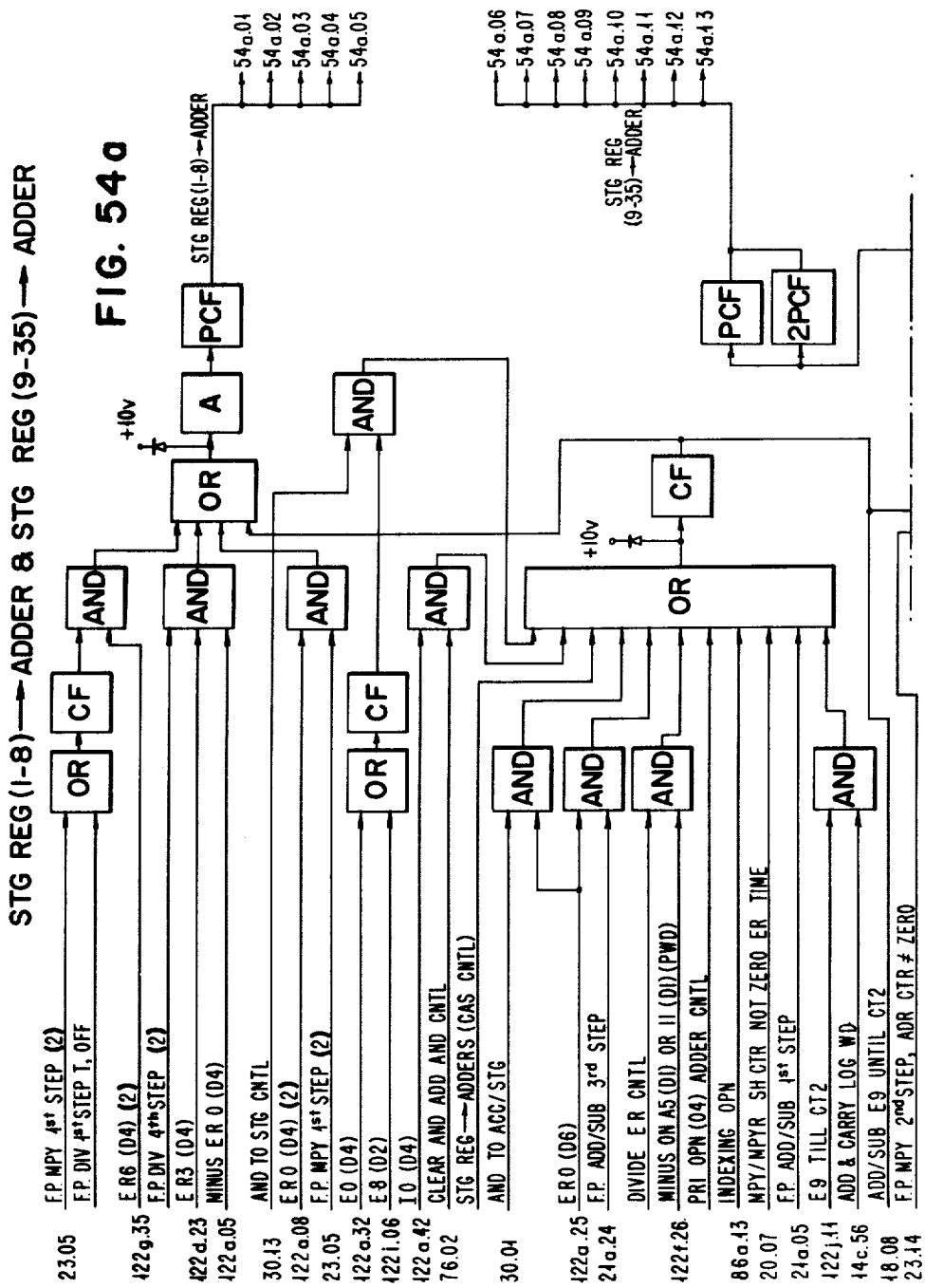

STG BUS → STG REG
37.10 EXCL. OR TO ACC (2)
21b.01 COMPL MQ 3rd STEP (2)
33.04 PLACE COMP ADR → INDEX
44.11 OR ACC → INDS
44.07 INVERT INDS (ACC)
41.06 RESET INDS (ACC)
33.10 PLACE ADR IN INDEX
41.01 PLACE INDS IN ACC
122d.04 I 3 (D1)
122d.10 ER 3 (D1)
39.08 TEST INDS (STG) 1st STEP
1221.24 ER 11 (D1)
95b.02 DISPLAY INDS
122j.23 A 9 (D1)
42.05 HALF INDS CNTL
122f.18 ER 5 (D1)
122a.38 I 0 (D4)
44.01 PLACE ACC → INDS
38.09 ER 0 (D4) ON EXCHANGE
37.40 EXCL. OR TO ACC (2)
122b09 ER 1 (D1)
38.04 EXCHANGE MQ AND ACC
40.05 TR INDS (ACC) 1st STEP
35b.01 PLACE INDEX IN DECR/ADR
21b.01 COMPL MQ 3rd STEP (2)
21b.10 COMPL MQ 4th STEP
122j.33 ER 9 (D1)
OR
CF
AND
STG BUS → STG REG (ER 5 (D1)) → 53b.01
TO STG BUS → STG REG → 53b.02

FIG. 53b

FIG. 54a


STG REG (1-8) → ADDER & STG REG (9-35) → ADDER
F.P MPY 4st STEP (2)
F.P. DIV 4st STEP I, OFF
E R6 (D4) (2)
F.P.DIV 4th STEP (2)
E R3 (D4)
MINUS E R 0 (D4)
AND TO STG CNTL
E R 0 (D4) (2)
F.P. MPY 4st STEP (2)
E0 (D4)
E 8 (D2)
I 0 (D4)
CLEAR AND ADD AND CNTL
STG REG → ADDERS (CAS CNTL)
AND TO ACC/STG
E R 0 (D6)
F.P. ADD/SUB 3rd STEP
DIVIDE E R CNTL
MINUS ON A5 (D1) OR 11 (D1) (PWD)
PRI OPN (04) ADDER CNTL
INDEXING OPN
MPY/MPYR SH CTR NOT ZERO ER TIME
F.P. ADD/SUB 1st STEP
E 9 TILL CT2
ADD & CARRY LOG WD
ADD/SUB E9 UNTIL CT2
F.P MPY 2nd STEP, ADR CTR ≠ ZERO
23.05
422g.35
422d.23
422a.05
30.13
422a.08
23.05
422a.32
422i.06
422a.42
76.02
30.04
422a.25
21a.24
422f.26
86a.13
20.07
21a.05
422j.11
14c.56
18.08
23.14
AND
OR
CF
A
PCF
2PCF
+10v
STG REG (1-8) → ADDER
STG REG (9-35) → ADDER
54a.01
54a.02
54a.03
54a.04
54a.05
54a.06
54a.07
54a.08
54a.09
54a.10
54a.11
54a.12
54a.13

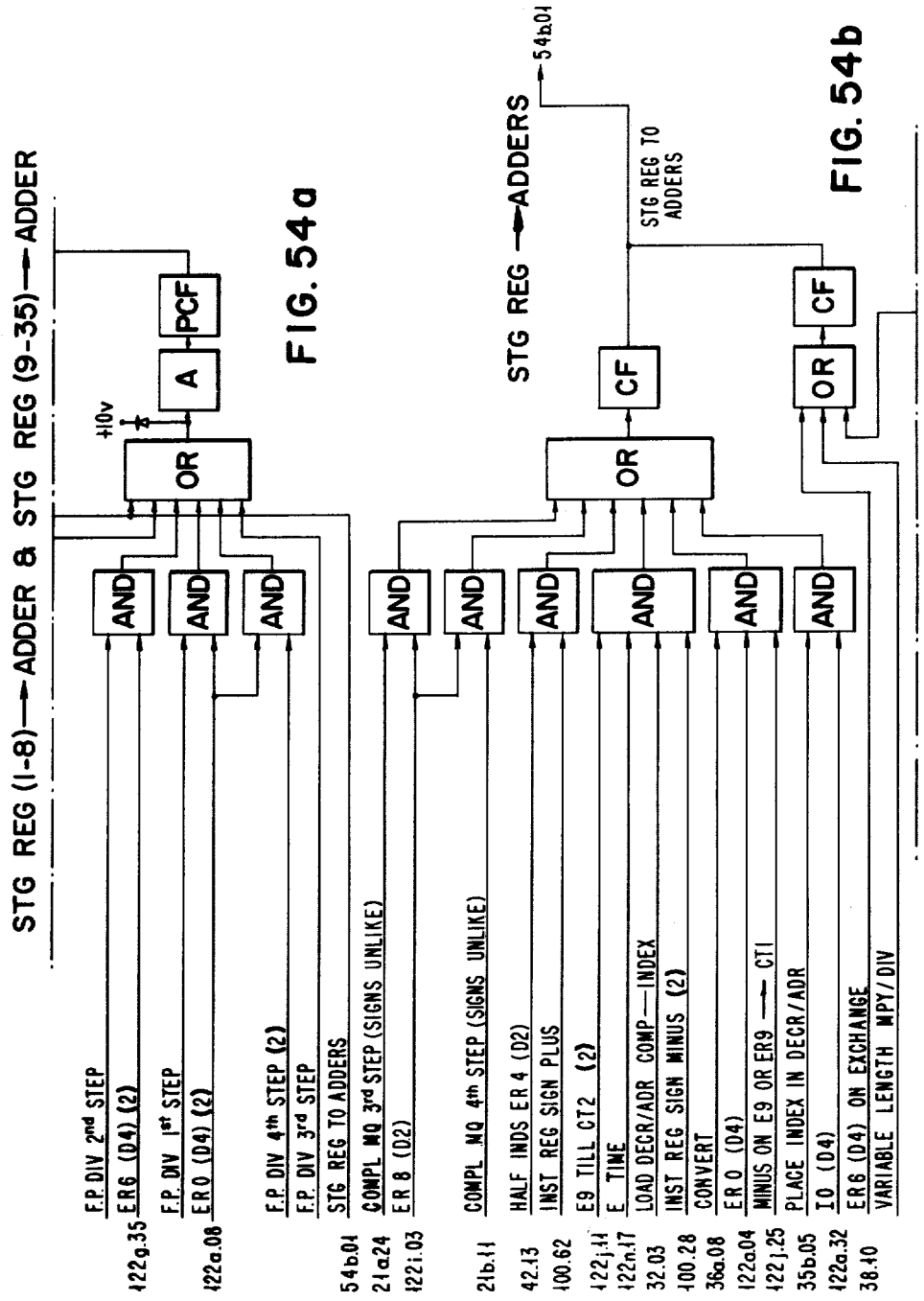


FIG. 54a

FIG. 54b

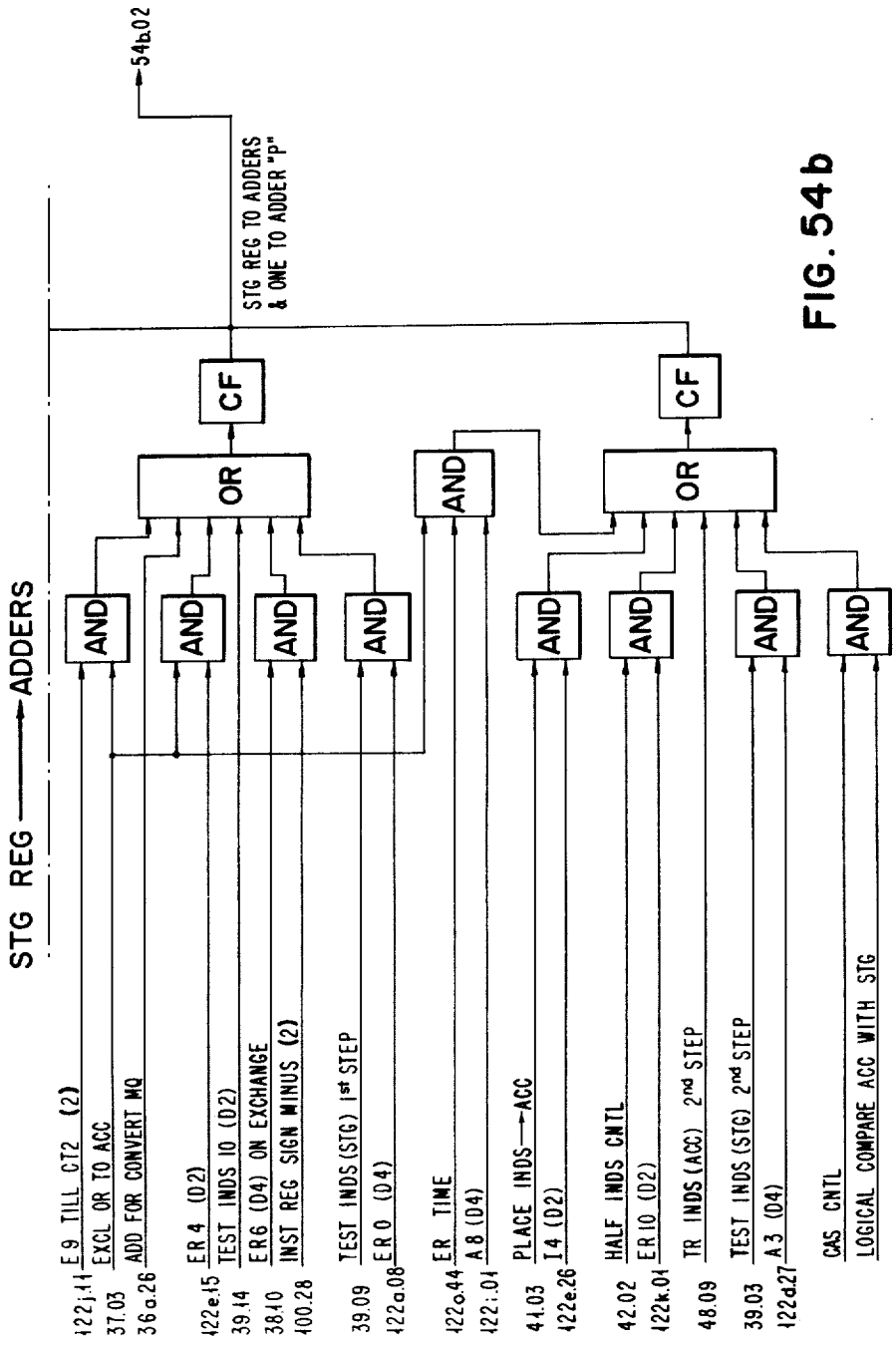

54b.02
STG REG TO ADDERS & ONE TO ADDER "P"
CF
OR
AND
STG REG
ADDERS
122j.11 E 9 TILL CT2 (2)
37.03 EXCL OR TO ACC
36a.26 ADD FOR CONVERT MQ
122e.15 ER 4 (D2)
39.14 TEST INDS 10 (D2)
38.10 ER6 (D4) ON EXCHANGE
100.28 INST REG SIGN MINUS (2)
39.09 TEST INDS (STG) 1st STEP
122a.08 ER 0 (D4)
122a.44 ER TIME
122i.01 A 8 (D4)
41.03 PLACE INDS → ACC
122e.26 I 4 (D2)
42.02 HALF INDS CNTL
122k.01 ER 10 (D2)
48.09 TR INDS (ACC) 2nd STEP
39.03 TEST INDS (STG) 2nd STEP
122d.27 A 3 (D4)
CAS CNTL
LOGICAL COMPARE ACC WITH STG

FIG. 54b

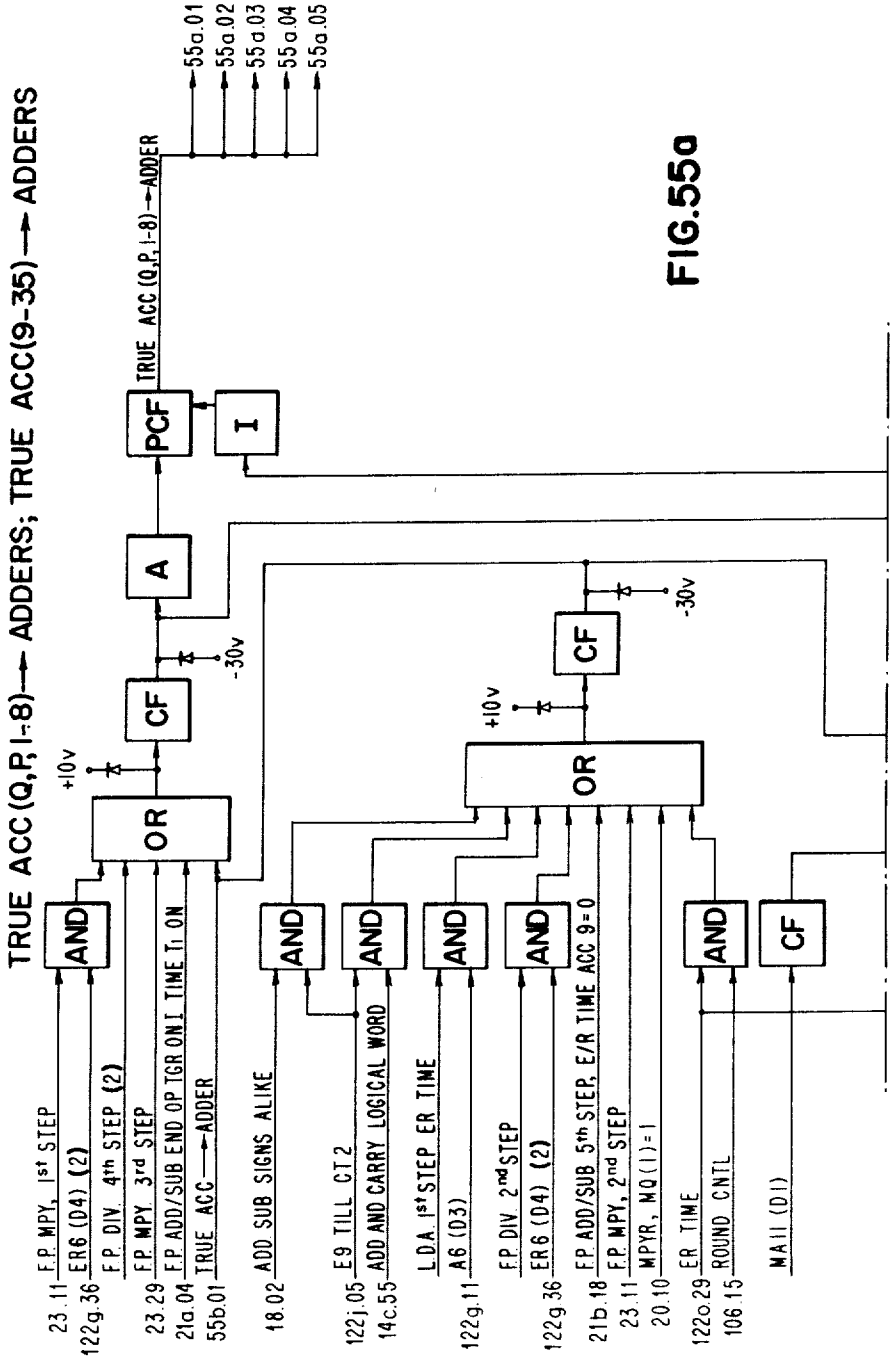

TRUE ACC (Q,P,1-8)→ ADDERS; TRUE ACC(9-35)→ ADDERS
55a.01
55a.02
55a.03
55a.04
55a.05
TRUE ACC (Q,P,1-8)→ADDER
PCF
I
A
CF
-30v
+10v
OR
AND
23.11 F.P. MPY, 1st STEP
122g.36 ER6 (D4) (2)
F.P. DIV. 4th STEP (2)
23.29 F.P. MPY. 3rd STEP
21a.04 F.P ADD/SUB END OP TGR ON 1 TIME T1 ON
55b.01 TRUE ACC→ADDER
18.02 ADD SUB SIGNS ALIKE
122j.05 E9 TILL CT 2
14c.55 ADD AND CARRY LOGICAL WORD
L.D.A. 1st STEP ER TIME
122g.11 A6 (D3)
F.P DIV 2nd STEP
122g 36 ER6 (D4) (2)
21b.18 F.P ADD/SUB 5th STEP, E/R TIME ACC 9=0
23.11 F.P. MPY, 2nd STEP
20.10 MPYR, MQ(1)=1
122o.29 ER TIME
106 15 ROUND CNTL
MAII (D1)

FIG.55a

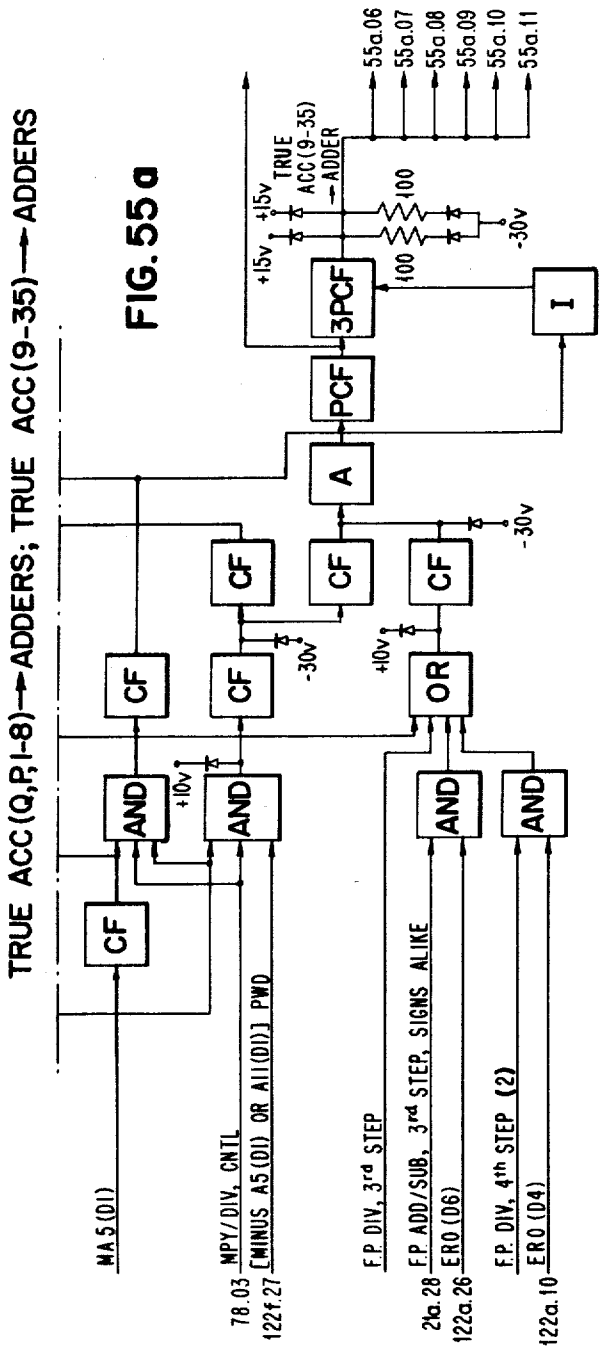


FIG. 55a

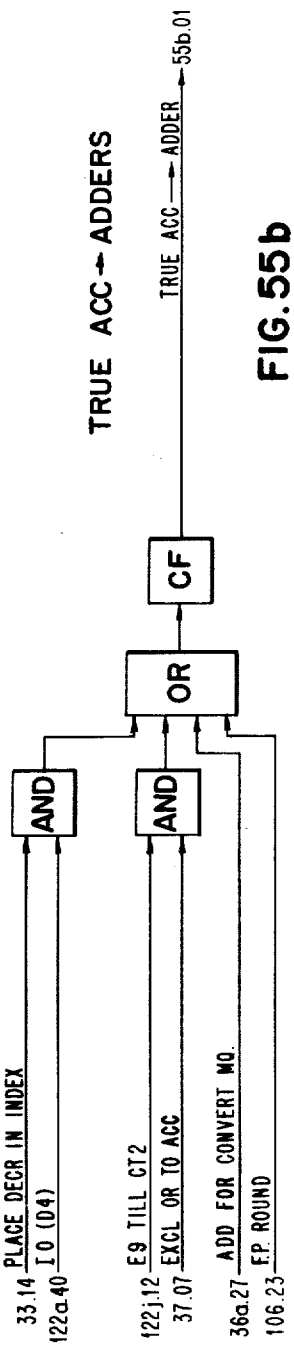


FIG. 55b

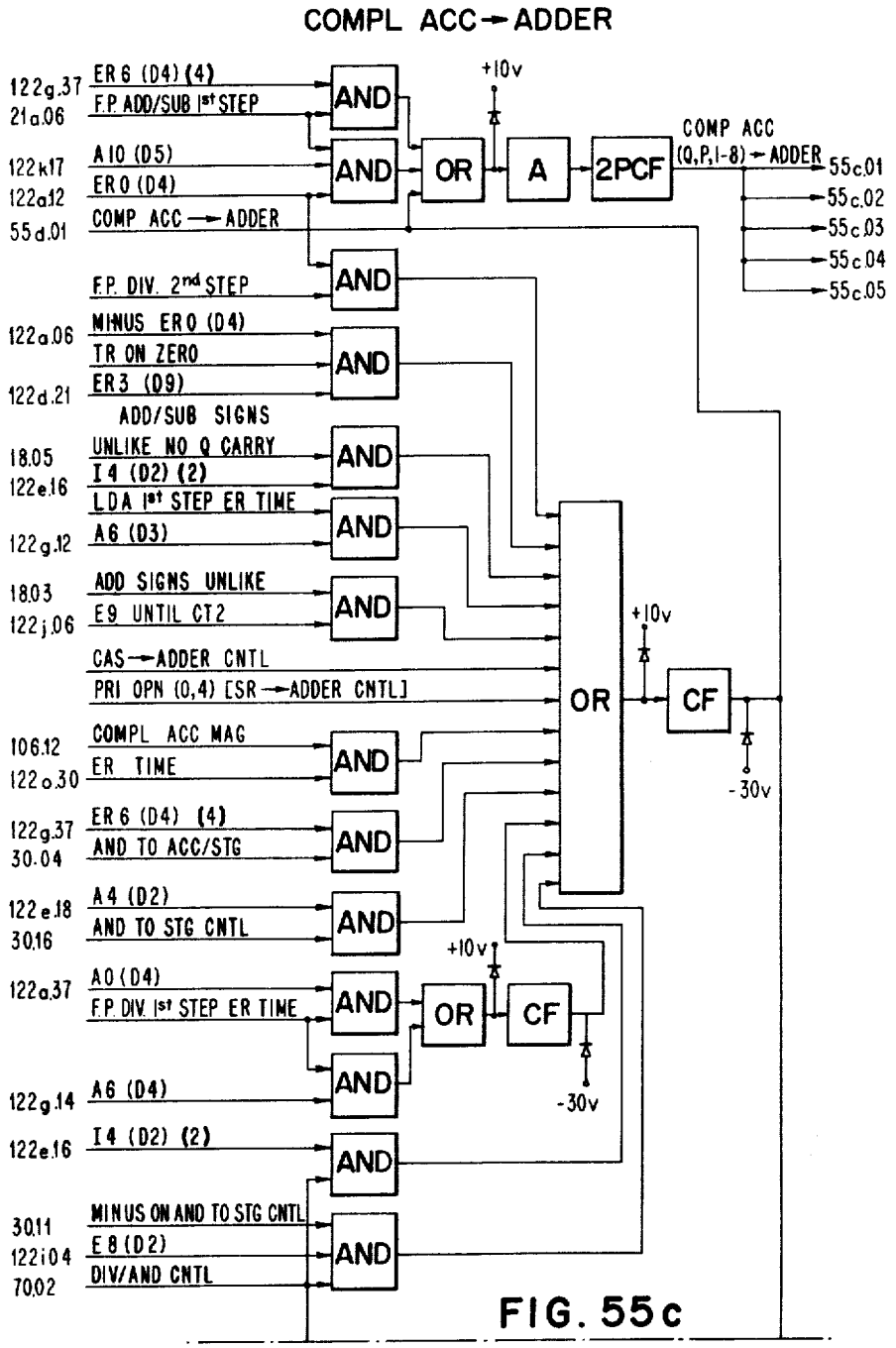

COMPL ACC → ADDER
122g.37 ER 6 (D4) (4)
21a.06 F.P. ADD/SUB 1st STEP
122k17 A 10 (D5)
122a12 ER 0 (D4)
55d.01 COMP ACC → ADDER
F.P. DIV. 2nd STEP
122a.06 MINUS ER 0 (D4)
TR ON ZERO
122d.21 ER 3 (D9)
ADD/SUB SIGNS
18.05 UNLIKE NO Q CARRY
122e.16 I 4 (D2) (2)
LDA 1st STEP ER TIME
122g.12 A 6 (D3)
18.03 ADD SIGNS UNLIKE
122j.06 E 9 UNTIL CT 2
CAS → ADDER CNTL
PRI OPN (0,4) [SR → ADDER CNTL]
106.12 COMPL ACC MAG
122o.30 ER TIME
122g.37 ER 6 (D4) (4)
30.04 AND TO ACC/STG
122e.18 A 4 (D2)
30.16 AND TO STG CNTL
122a.37 A 0 (D4)
F.P. DIV. 1st STEP ER TIME
122g.14 A 6 (D4)
122e.16 I 4 (D2) (2)
30.11 MINUS ON AND TO STG CNTL
122i04 E 8 (D2)
70.02 DIV/AND CNTL
AND
OR
A
2PCF
CF
+10v
-30v
COMP ACC (Q,P,1-8) → ADDER
55c.01
55c.02
55c.03
55c.04
55c.05

FIG. 55c

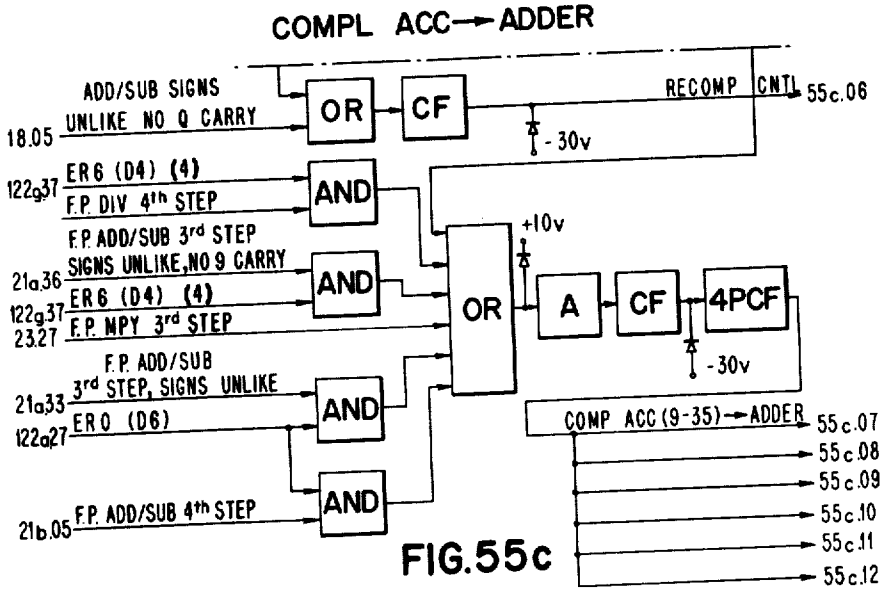


FIG.55c

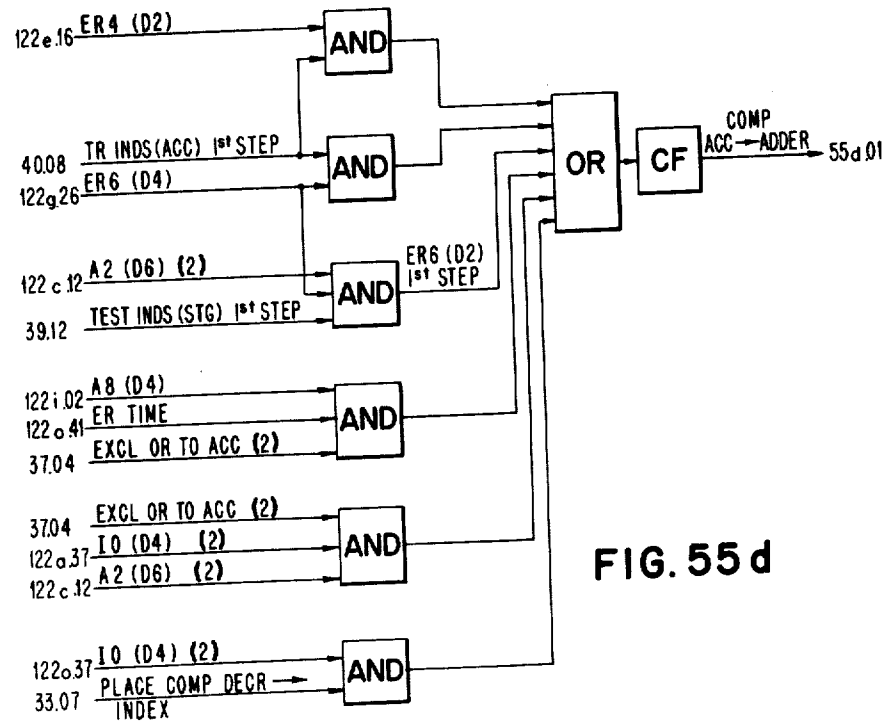
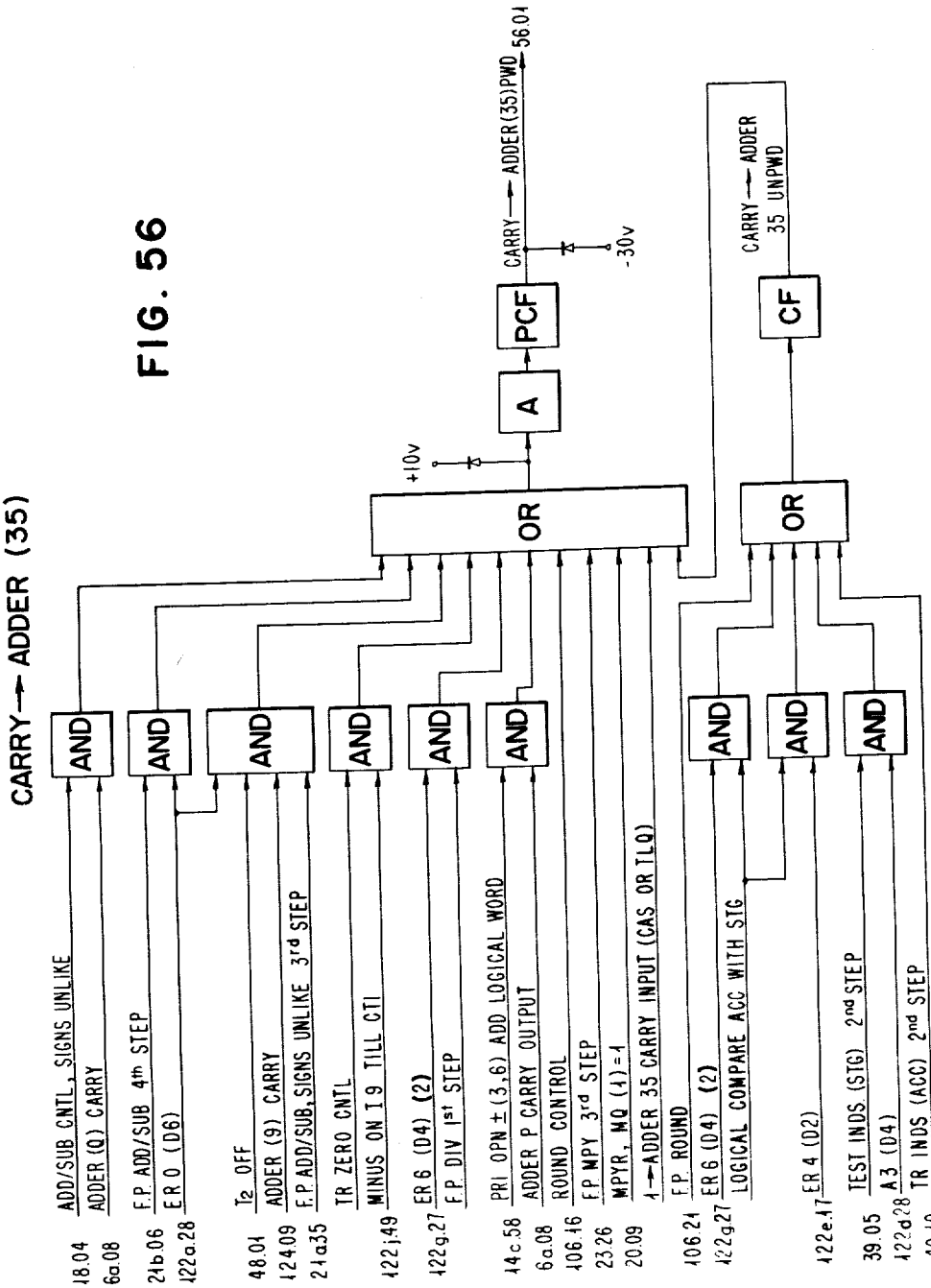


FIG. 55d

FIG. 56


CARRY → ADDER (35)
AND
OR
A
PCF
+10v
-30v
CARRY → ADDER(35)PWD 56.04
CF
CARRY → ADDER 35 UNPWD
18.04 ADD/SUB CNTL, SIGNS UNLIKE
6a.08 ADDER (Q) CARRY
21b.06 F.P ADD/SUB 4th STEP
122a.28 E R 0 (D6)
48.01 T2 OFF
124.09 ADDER (9) CARRY
21a.35 F.P ADD/SUB, SIGNS UNLIKE 3rd STEP
TR ZERO CNTL
122j.49 MINUS ON I 9 TILL CTI
122g.27 ER 6 (D4) (2)
F.P DIV 1st STEP
14c.58 PRI OPN ± (3,6) ADD LOGICAL WORD
6a.08 ADDER P CARRY OUTPUT
106.16 ROUND CONTROL
23.26 F.P MPY 3rd STEP
20.09 MPYR, MQ (1)=1
1 → ADDER 35 CARRY INPUT (CAS OR TLQ)
106.21 F.P ROUND
122g.27 ER 6 (D4) (2)
LOGICAL COMPARE ACC WITH STG
122e.17 ER 4 (D2)
39.05 TEST INDS (STG) 2nd STEP
122a.28 A3 (D4)
40.10 TR INDS (ACC) 2nd STEP

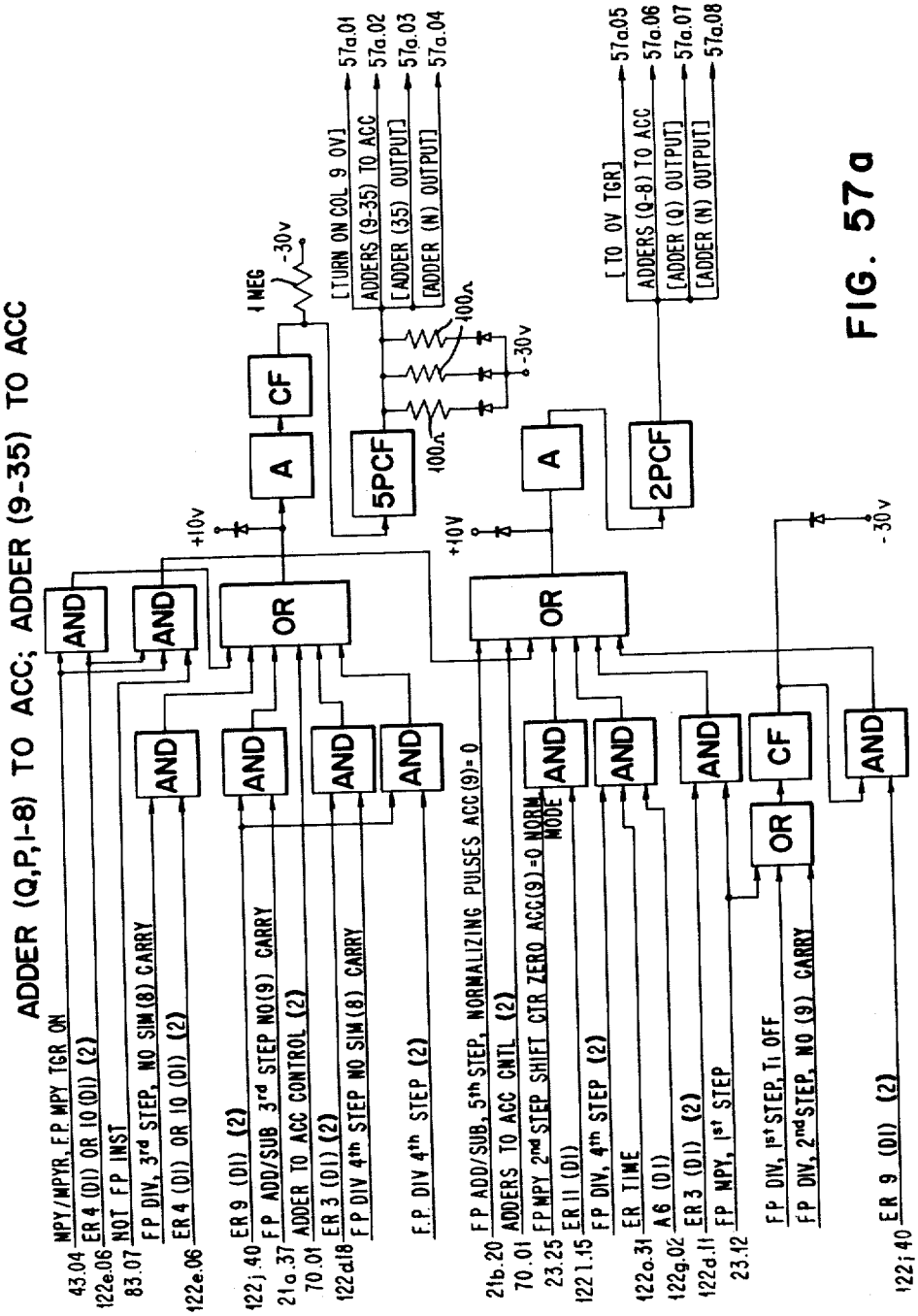

ADDER (Q,P,I-8) TO ACC; ADDER (9-35) TO ACC
MPY/MPYR, F.P. MPY TGR ON
ER 4 (01) OR 10 (01) (2)
NOT F.P. INST
F.P. DIV, 3rd STEP, NO SIM (8) CARRY
ER 4 (01) OR 10 (01) (2)
ER 9 (01) (2)
F.P. ADD/SUB 3rd STEP NO (9) CARRY
ADDER TO ACC CONTROL (2)
ER 3 (01) (2)
F.P. DIV 4th STEP NO SIM (8) CARRY
F.P. DIV 4th STEP (2)
F.P. ADD/SUB, 5th STEP, NORMALIZING PULSES ACC (9) = 0
ADDERS TO ACC CNTL (2)
F.P. MPY 2nd STEP SHIFT CTR ZERO ACC (9) = 0 NORM MODE
ER 11 (01)
F.P. DIV, 4th STEP (2)
ER TIME
A6 (01)
ER 3 (01) (2)
F.P. MPY, 1st STEP
F.P. DIV, 1st STEP, T1 OFF
F.P. DIV, 2nd STEP, NO (9) CARRY
ER 9 (01) (2)
AND
OR
CF
A
5PCF
2PCF
+10v
-30v
1 MEG
100Ω
[TURN ON COL 9 OV]
ADDERS (9-35) TO ACC
[ADDER (35) OUTPUT]
[ADDER (N) OUTPUT]
[TO OV TGR]
ADDERS (Q-8) TO ACC
[ADDER (Q) OUTPUT]
[ADDER (N) OUTPUT]
57a.01
57a.02
57a.03
57a.04
57a.05
57a.06
57a.07
57a.08

FIG. 57a

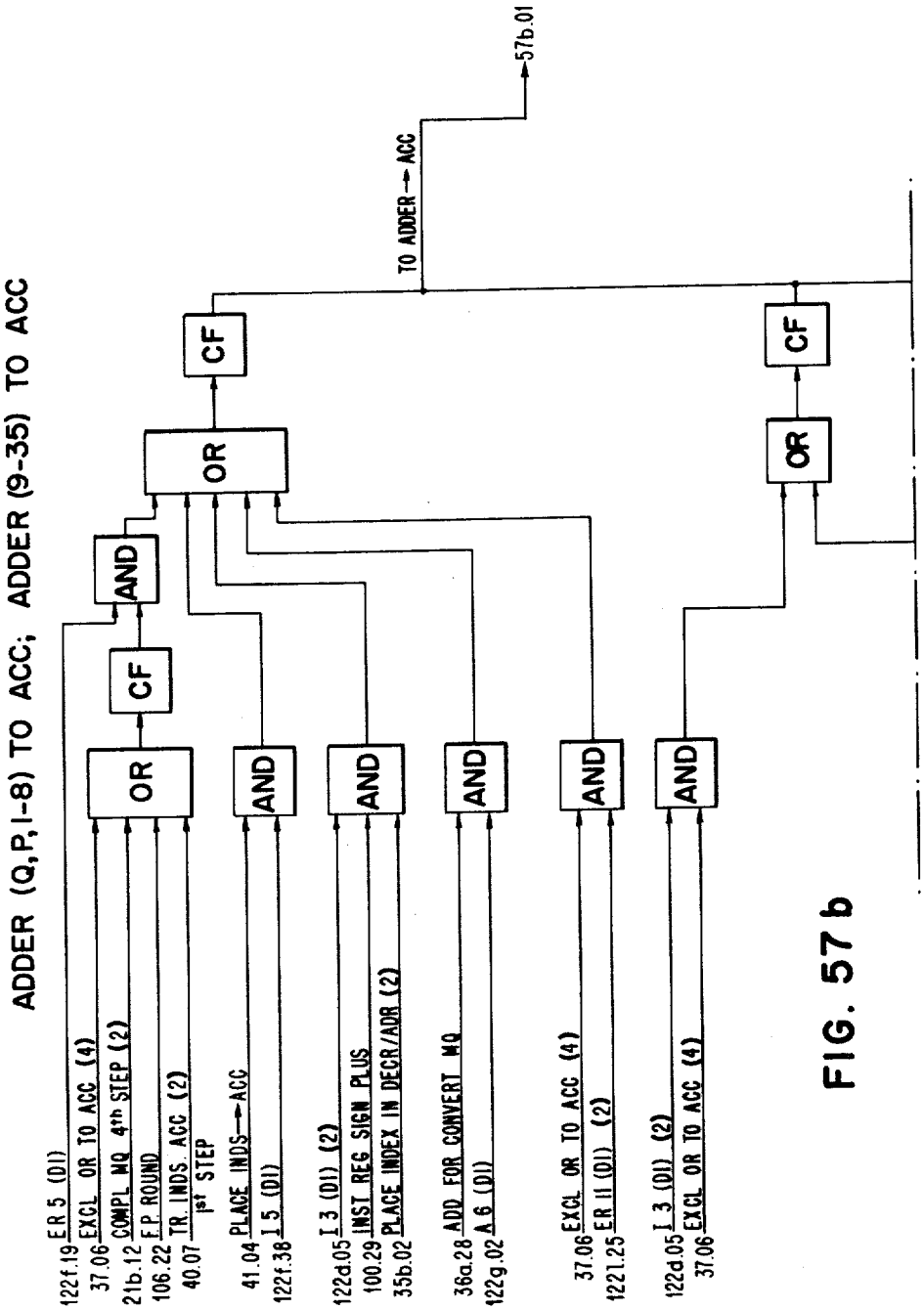

ADDER (Q,P,1-8) TO ACC; ADDER (9-35) TO ACC
TO ADDER → ACC
57b.01
CF
OR
AND
CF
OR
AND
AND
AND
AND
AND
122f.19 ER 5 (01)
37.06 EXCL OR TO ACC (4)
21b.12 COMPL MQ 4th STEP (2)
106.22 F.P. ROUND
40.07 TR. INDS. ACC (2) 1st STEP
41.04 PLACE INDS → ACC
122f.38 I 5 (01)
122d.05 I 3 (01) (2)
100.29 INST REG SIGN PLUS
35b.02 PLACE INDEX IN DECR/ADR (2)
36a.28 ADD FOR CONVERT MQ
122g.02 A 6 (01)
37.06 EXCL OR TO ACC (4)
1221.25 ER 11 (01) (2)
122d.05 I 3 (01) (2)
37.06 EXCL OR TO ACC (4)

FIG. 57b

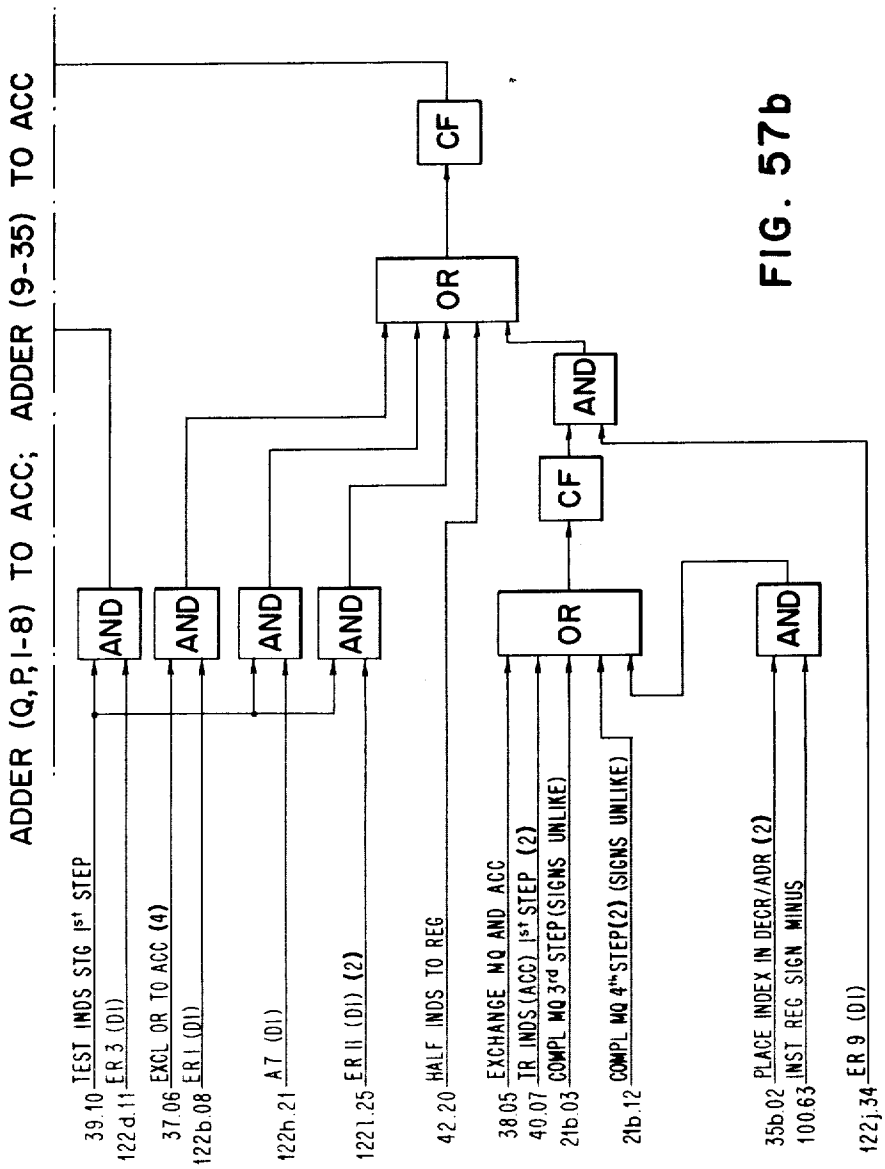
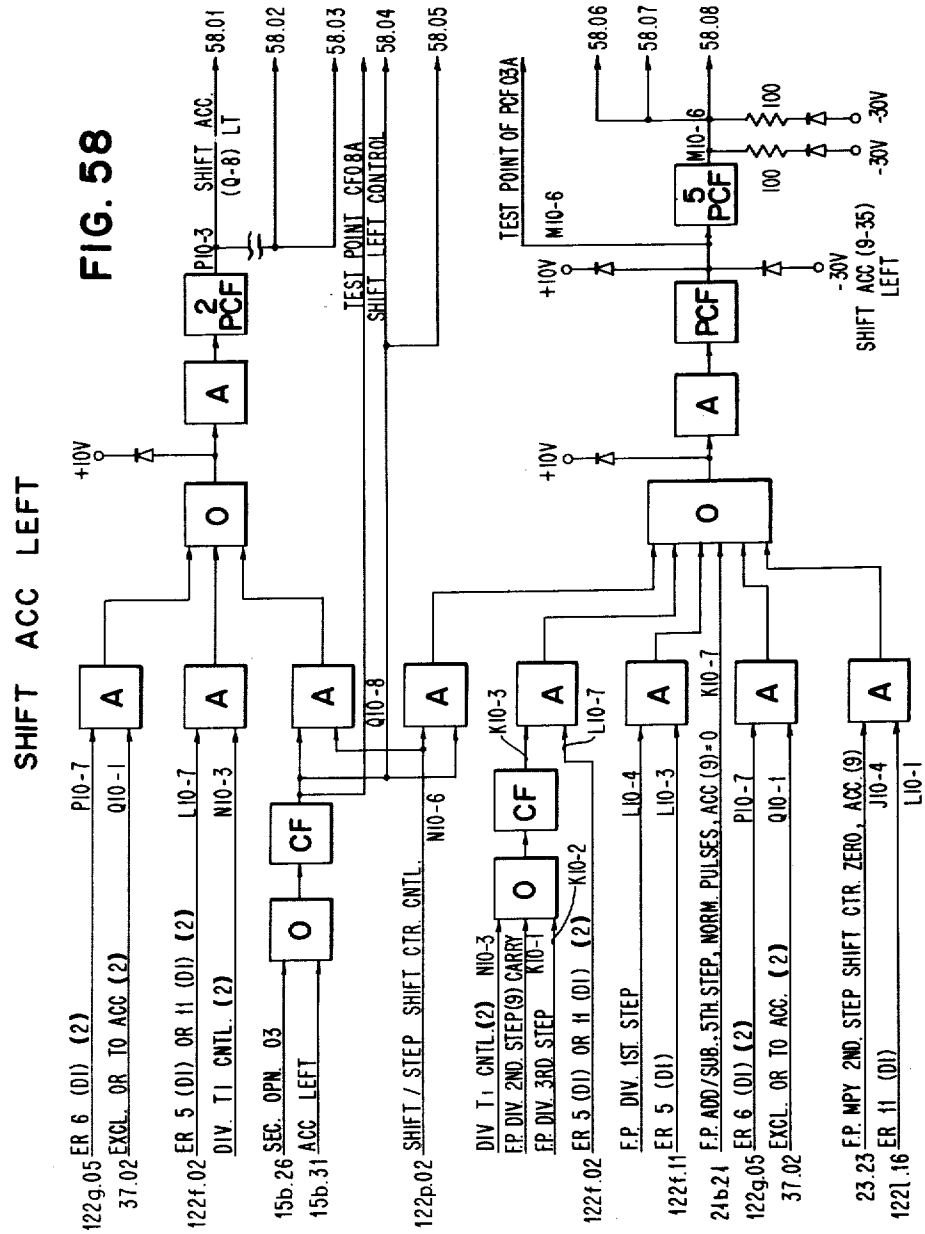

ADDER (Q,P,1-8) TO ACC; ADDER (9-35) TO ACC
CF
OR
AND
AND
AND
AND
AND
CF
OR
AND
39.10 TEST INDS STG 1st STEP
122d.11 ER 3 (D1)
37.06 EXCL OR TO ACC (4)
122b.08 ER 1 (D1)
122h.21 A 7 (D1)
122l.25 ER 11 (D1) (2)
42.20 HALF INDS TO REG
38.05 EXCHANGE MQ AND ACC
40.07 IR INDS (ACC) 1st STEP (2)
21b.03 COMPL MQ 3rd STEP (SIGNS UNLIKE)
21b.12 COMPL MQ 4th STEP (2) (SIGNS UNLIKE)
35b.02 PLACE INDEX IN DECR/ADR (2)
100.63 INST REG SIGN MINUS
122j.34 ER 9 (D1)

FIG. 57b

FIG. 58


SHIFT ACC LEFT
122g.05 ER 6 (D1) (2)
37.02 EXCL. OR TO ACC (2)
122f.02 ER 5 (D1) OR 11 (D1) (2)
DIV. T1 CNTL. (2)
15b.26 SEC. OPN. 03
15b.31 ACC LEFT
122p.02 SHIFT / STEP SHIFT CTR. CNTL.
DIV T1 CNTL.(2) N10-3
F.P. DIV. 2ND. STEP(9) CARRY K10-3
F.P. DIV. 3RD STEP K10-1
122f.02 ER 5 (D1) OR 11 (D1) (2) K10-2
F.P. DIV. 1ST. STEP
122f.11 ER 5 (D1)
24b.21 F.P. ADD/SUB..5TH.STEP, NORM. PULSES, ACC (9)=0 K10-7
122g.05 ER 6 (D1) (2)
37.02 EXCL. OR TO ACC. (2)
23.23 F.P. MPY 2ND. STEP SHIFT CTR. ZERO, ACC (9)
122l.16 ER 11 (D1)
P10-7
Q10-1
L10-7
N10-3
Q10-8
N10-6
L10-7
L10-4
L10-3
K10-7
P10-7
Q10-1
J10-4
L10-1
+10V
A
O
CF
2 PCF
5 PCF
P10-3 SHIFT ACC. (Q-8) LT
58.01
58.02
58.03
58.04
58.05
58.06
58.07
58.08
TEST POINT CF0.8A
SHIFT LEFT CONTROL
TEST POINT OF PCF03A
M10-6
100
-30V
SHIFT ACC (9-35) LEFT

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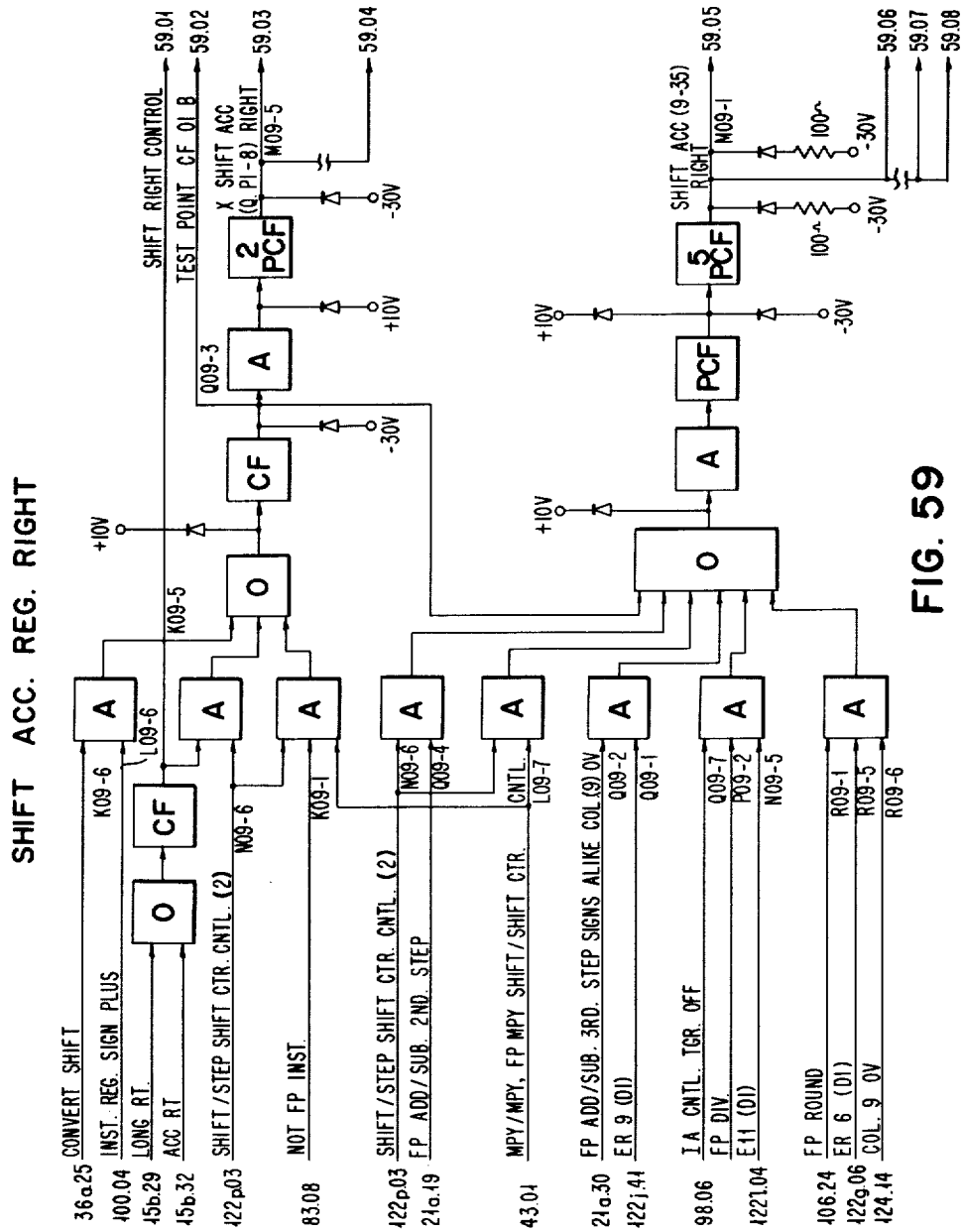


FIG. 59

FIG. 60

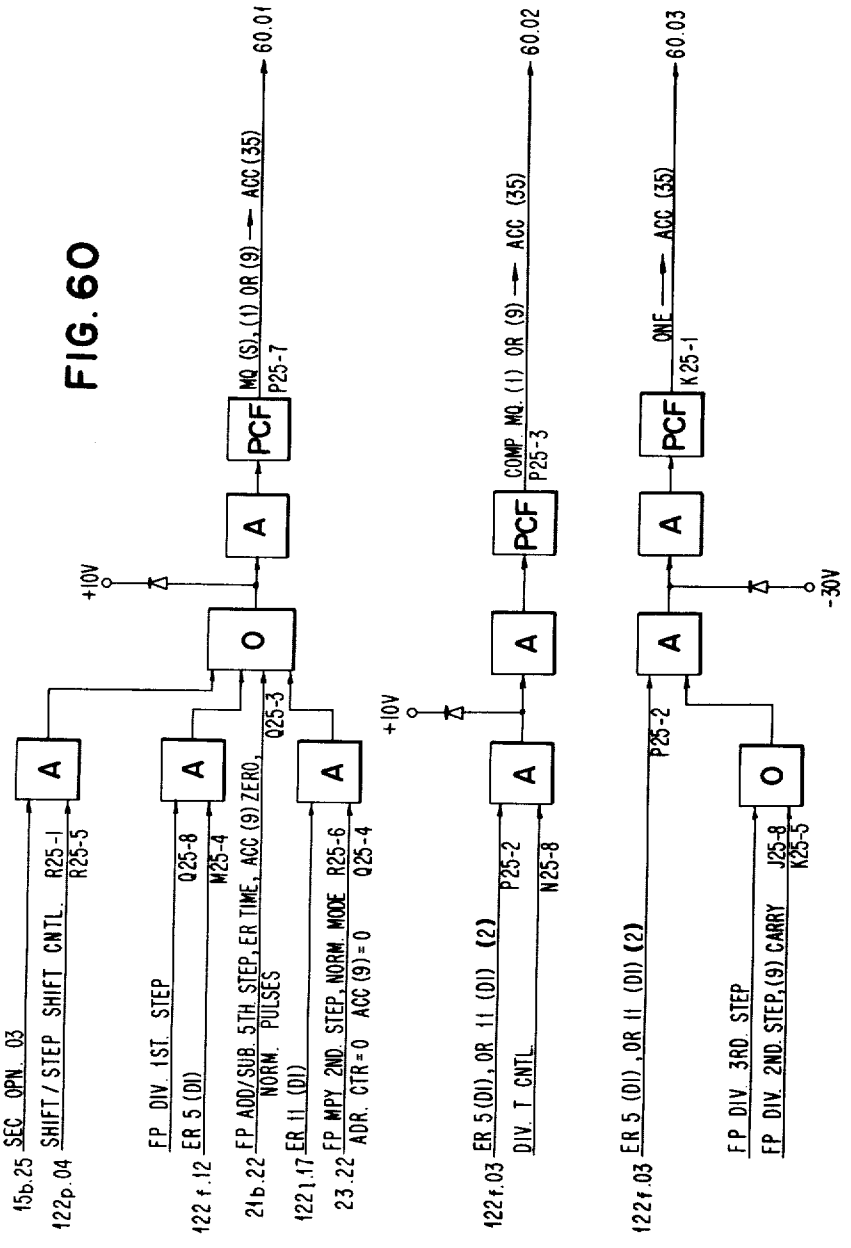
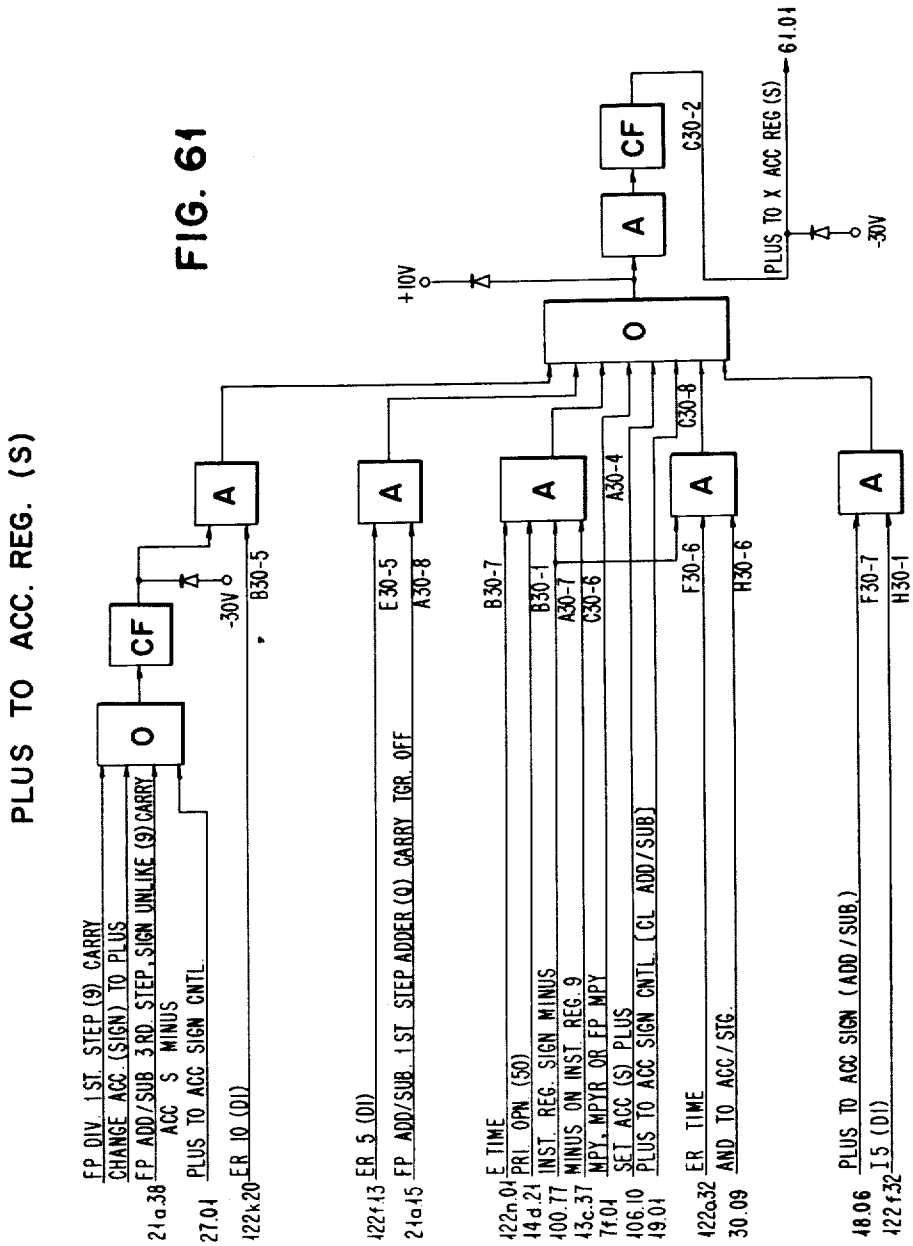

MQ (S), (1) OR (9) TO ACC. (35), 1 TO ACC. (35)
15b.25 SEC OPN. 03
122p.04 SHIFT / STEP SHIFT CNTL. R25-1 R25-5
122f.12 FP DIV. 1ST. STEP ER 5 (D1) Q25-8 M25-4
21b.22 FP ADD/SUB. 5TH. STEP, ER TIME, ACC (9) ZERO, NORM. PULSES Q25-3
122l.17 ER 11 (D1)
23.22 FP MPY 2ND. STEP, NORM. MODE R25-6 ADR. CTR = 0 ACC (9) = 0 Q25-4
+10V
A
O
PCF
MQ (S), (1) OR (9) → ACC (35) P25-7
60.01
122f.03 ER 5 (D1), OR 11 (D1) (2) P25-2 DIV. T CNTL M25-8
COMP MQ. (1) OR (9) → ACC (35) P25-3
60.02
122f.03 ER 5 (D1), OR 11 (D1) (2) P25-2
FP DIV. 3RD. STEP FP DIV. 2ND. STEP, (9) CARRY J25-8 K25-5
-30V
ONE → ACC (35) K25-1
60.03

FIG. 61


PLUS TO ACC. REG. (S)
FP DIV. 1ST. STEP (9) CARRY
CHANGE ACC. (SIGN) TO PLUS
21a.38 FP ADD/SUB 3RD. STEP, SIGN UNLIKE (9) CARRY
ACC S MINUS
27.01 PLUS TO ACC SIGN CNTL
122k20 ER 10 (01)
O
CF
A
-30V
B30-5
122f13 ER 5 (01)
21a15 FP ADD/SUB 1ST STEP ADDER (Q) CARRY TGR. OFF
E30-5
A30-8
122n.04 E TIME
14d.21 PRI OPN (50)
100.77 INST. REG. SIGN MINUS
43c.37 MINUS ON INST REG. 9
71.04 MPY, MPYR OR FP MPY
106.10 SET ACC (S) PLUS
19.04 PLUS TO ACC SIGN CNTL (CL ADD/SUB)
B30-7
B30-1
A30-7
C30-6
A30-4
C30-8
F30-6
H30-6
422a.32 ER TIME
30.09 AND TO ACC/STG.
48.06 PLUS TO ACC SIGN (ADD/SUB.)
122f32 I5 (01)
F30-7
H30-1
+10V
C30-2
PLUS TO X ACC REG (S)
61.01
-30V

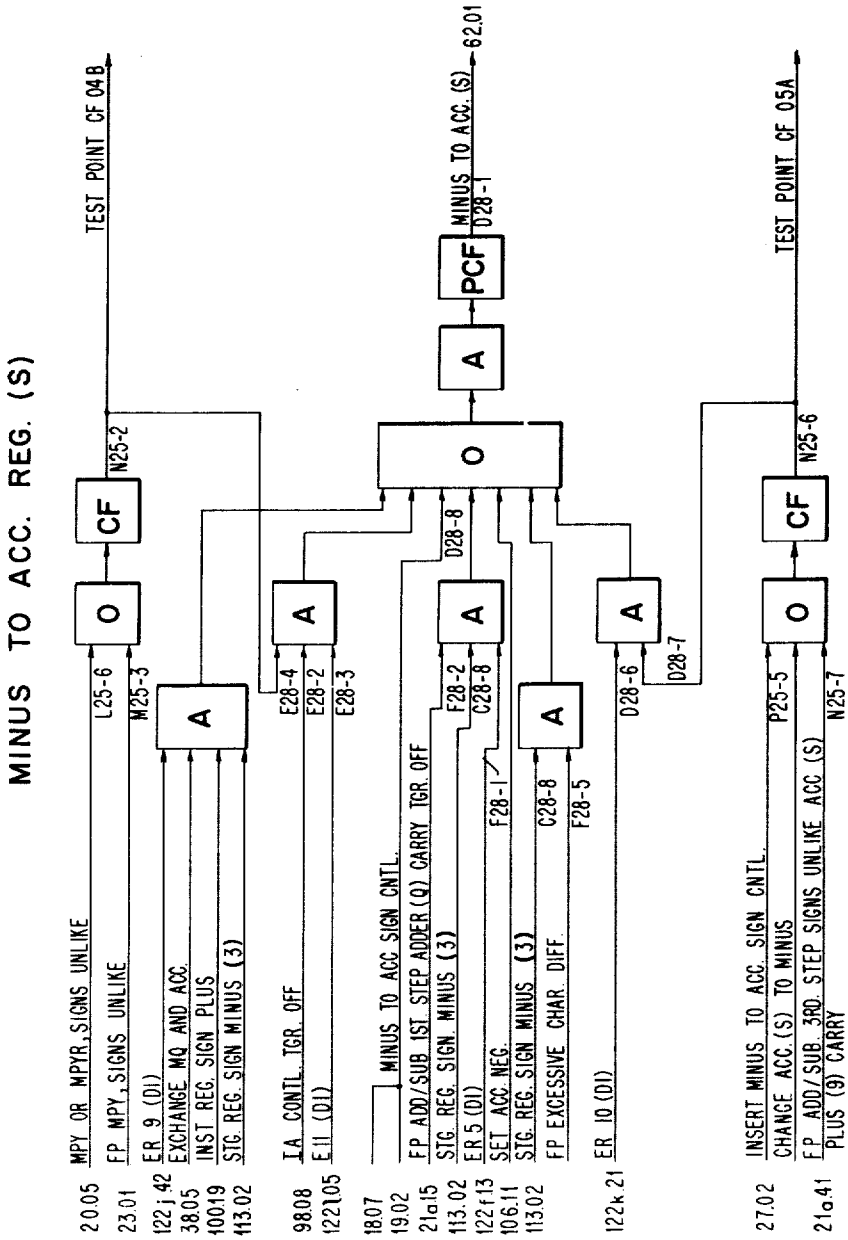
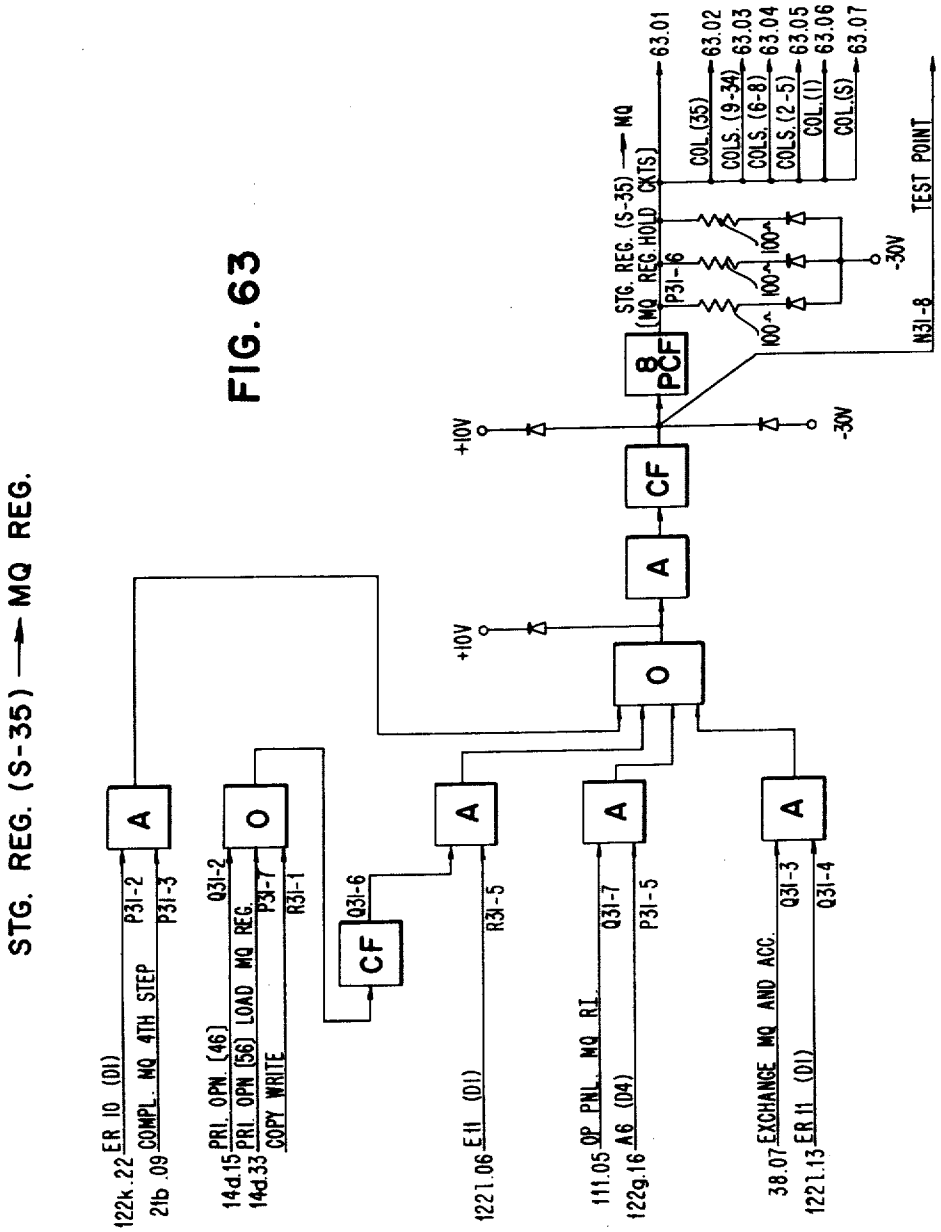

MINUS TO ACC. REG. (S)
TEST POINT CF 04B
TEST POINT CF 05A
62.01
MINUS TO ACC. (S) D28-1
PCF
CF
N25-2
N25-6
O
A
L25-6
M25-3
E28-4
E28-2
E28-3
D28-8
F28-2
C28-8
F28-1
F28-5
D28-6
D28-7
P25-5
N25-7
20.05 MPY OR MPYR, SIGNS UNLIKE
23.01 FP MPY, SIGNS UNLIKE
122 j 42 ER 9 (D1)
38.05 EXCHANGE MQ AND ACC.
10019 INST REG. SIGN PLUS
113.02 STG. REG. SIGN MINUS (3)
98.08 IA CONTL. TGR. OFF
122105 E 11 (D1)
18.07 MINUS TO ACC SIGN CNTL.
19.02 FP ADD/SUB 1ST. STEP ADDER (Q) CARRY TGR. OFF
21a15 STG. REG. SIGN. MINUS (3)
113.02 ER 5 (D1)
122f13 SET ACC NEG.
106.11 STG. REG. SIGN MINUS (3)
113.02 FP EXCESSIVE CHAR. DIFF.
122k 21 ER 10 (D1)
27.02 INSERT MINUS TO ACC. SIGN CNTL.
CHANGE ACC. (S) TO MINUS
21a41 FP ADD/SUB. 3RD. STEP SIGNS UNLIKE ACC (S)
PLUS (9) CARRY

FIG. 62

FIG. 63


STG. REG. (S-35) → MQ REG.
122k.22 ER 10 (01)
21b .09 COMPL. MQ 4TH STEP
P31-2
P31-3
A
14d.15 PRI. OPN. (46)
14d.33 PRI OPN (56) LOAD MQ REG.
COPY WRITE
Q31-2
P31-7
R31-1
O
Q31-6
CF
1221.06 E11 (01)
R31-5
A
111.05 OP PNL. MQ RI.
122g.16 A6 (04)
Q31-7
P31-5
A
38.07 EXCHANGE MQ AND ACC.
1221.13 ER 11 (01)
Q31-3
Q31-4
A
+10V
O
+10V
A
CF
8 PCF
+10V
-30V
STG. REG. (S-35) → MQ
(MQ REG HOLD CKTS)
P31-6
100Ω
100Ω
100Ω
-30V
N31-8
TEST POINT
COL. (35) 63.01
COLS. (9-34) 63.02
COLS. (6-8) 63.03
COLS. (2-5) 63.04
COL. (1) 63.05
COL. (S) 63.06
63.07

SHIFT MQ RIGHT

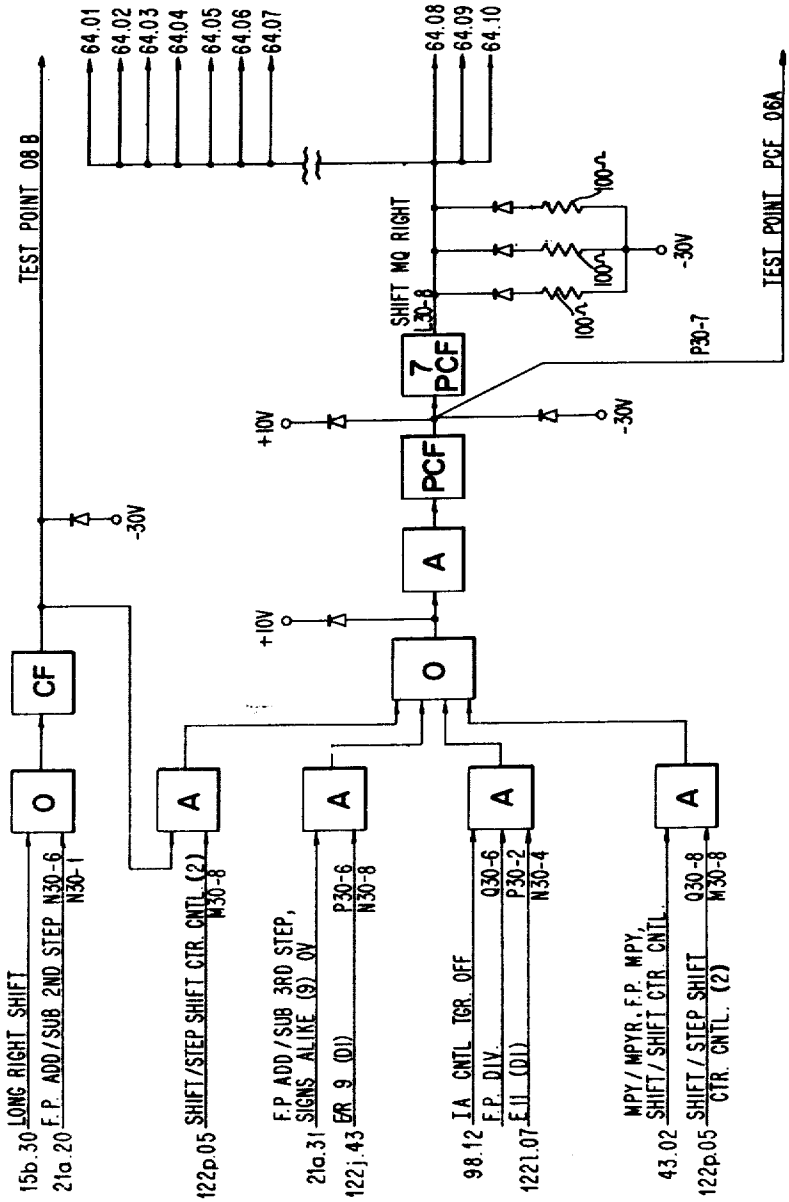


FIG. 64

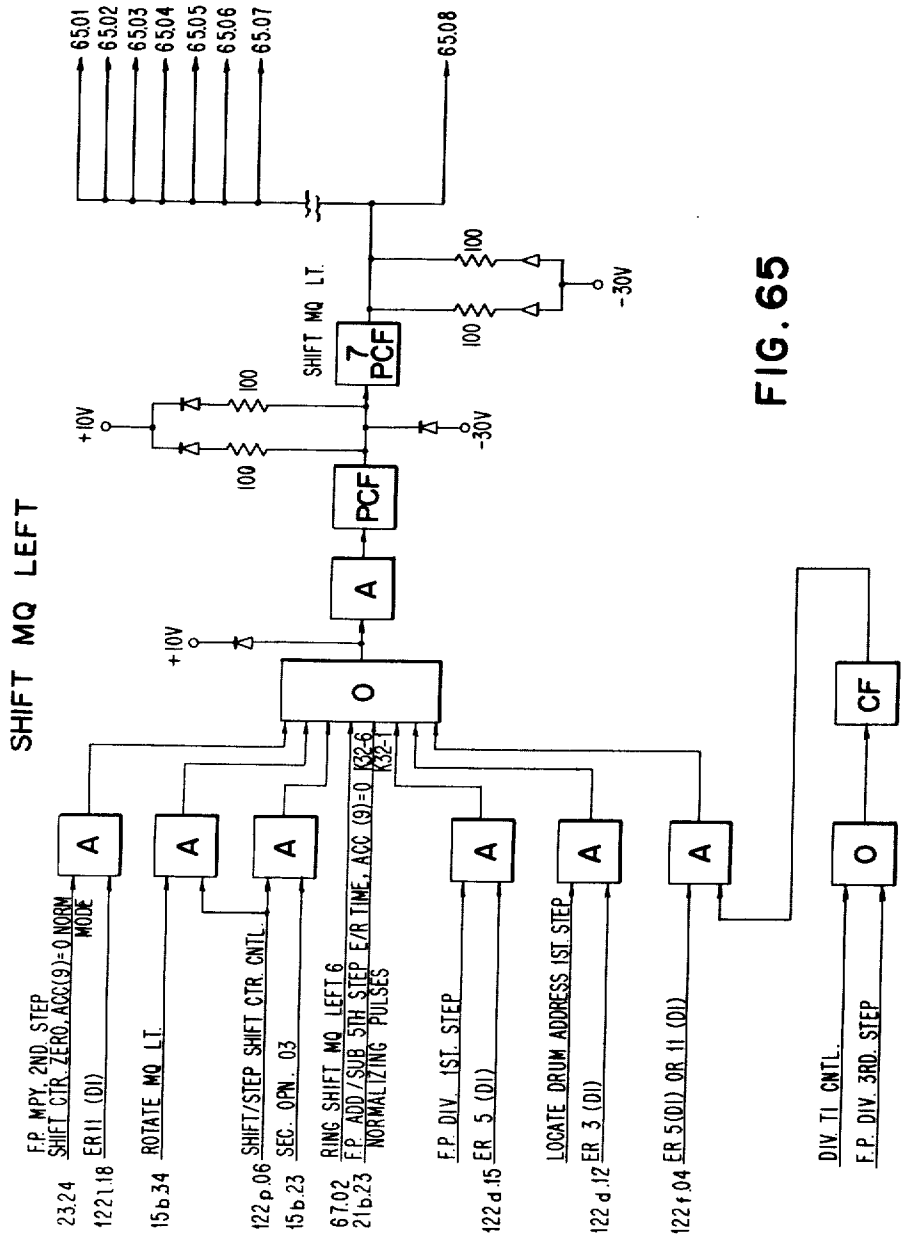

SHIFT MQ LEFT
65.01
65.02
65.03
65.04
65.05
65.06
65.07
65.08
SHIFT MQ LT.
7 PCF
100
100
-30V
+10V
100
100
-30V
PCF
A
+10V
O
A
A
A
A
A
A
O
CF
F.P. MPY. 2ND. STEP
23.24 SHIFT CTR. ZERO, ACC(9)=0 NORM MODE
122 l.18 ER 11 (D1)
15 b.34 ROTATE MQ LT.
122 p.06 SHIFT/STEP SHIFT CTR. CNTL.
15 b.23 SEC. OPN. 03
67.02 RING SHIFT MQ LEFT 6
21 b.23 F.P. ADD/SUB 5TH STEP E/R TIME, ACC (9)=0 K32-6
NORMALIZING PULSES K32-1
F.P. DIV. 1ST. STEP
122 d.15 ER 5 (D1)
LOCATE DRUM ADDRESS 1ST. STEP
122 d.12 ER 3 (D1)
122 f.04 ER 5 (D1) OR 11 (D1)
DIV. T1 CNTL.
F.P. DIV. 3RD. STEP

FIG. 65

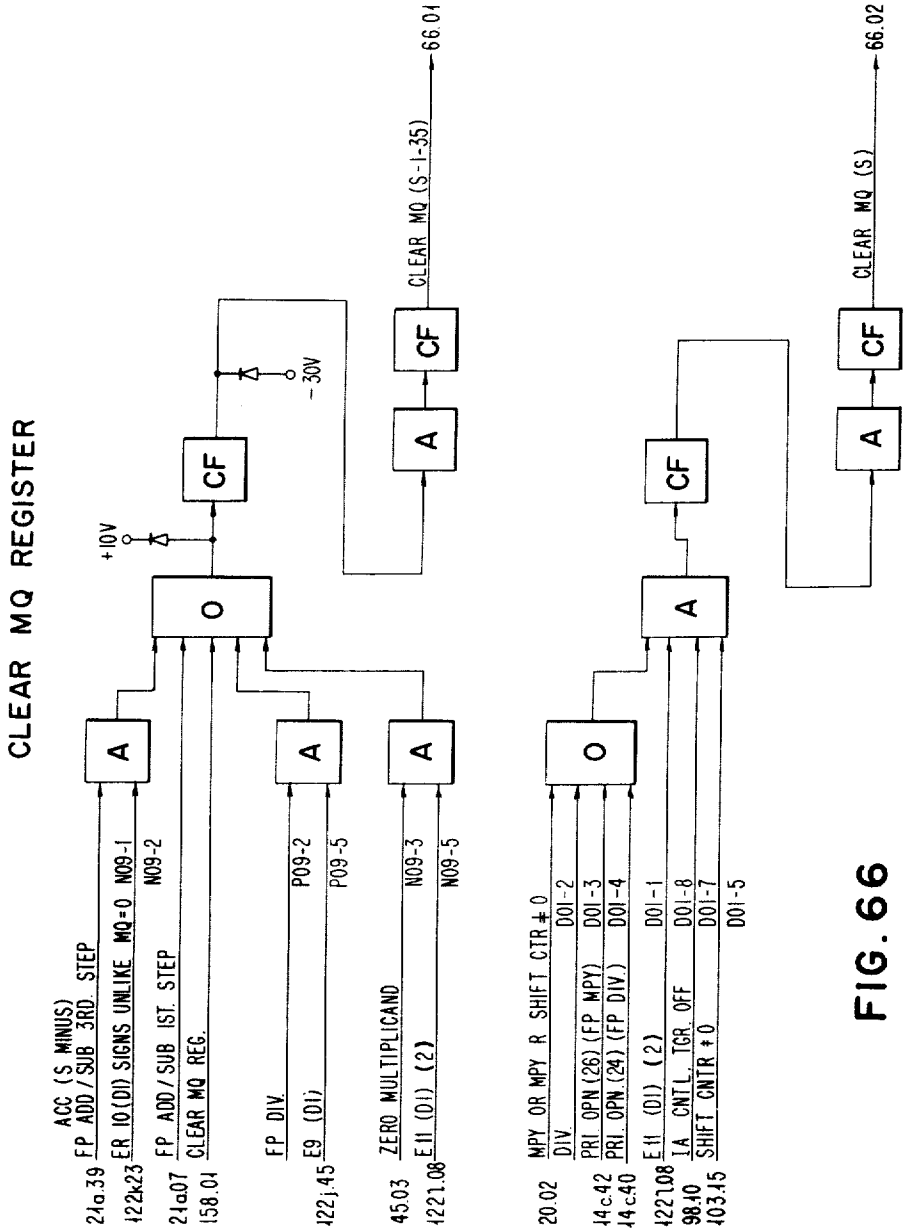

CLEAR MQ REGISTER
ACC (S MINUS)
FP ADD / SUB 3RD. STEP
21a.39
ER 10 (D1) SIGNS UNLIKE MQ=0 N09-1
122k23
FP ADD / SUB 1ST. STEP N09-2
21a.07
CLEAR MQ REG.
158.01
FP DIV.
P09-2
E9 (D1)
P09-5
122j.45
ZERO MULTIPLICAND
N09-3
45.03
E11 (D1) (2)
N09-5
4221.08
A
O
CF
+10V
-30V
A
CF
CLEAR MQ (S-1-35)
66.01
MPY OR MPY R SHIFT CTR ≠ 0
DIV
D01-2
20.02
PRI OPN (26) (FP MPY)
D01-3
14c.42
PRI OPN (24) (FP DIV.)
D01-4
14c.40
E11 (D1) (2)
D01-1
4221.08
IA CNTL TGR. OFF
D01-8
98.10
SHIFT CNTR ≠ 0
D01-7
403.15
D01-5
O
A
CF
CLEAR MQ (S)
66.02
A
CF

FIG. 66

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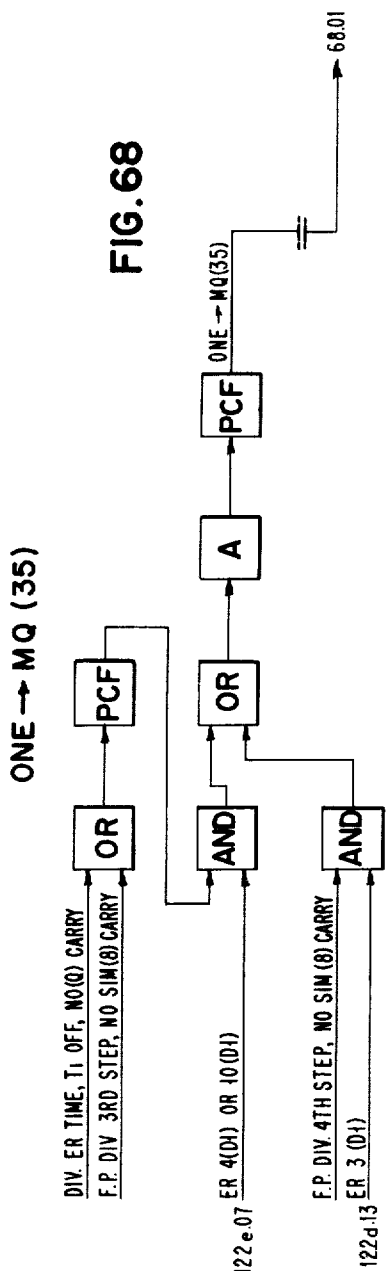
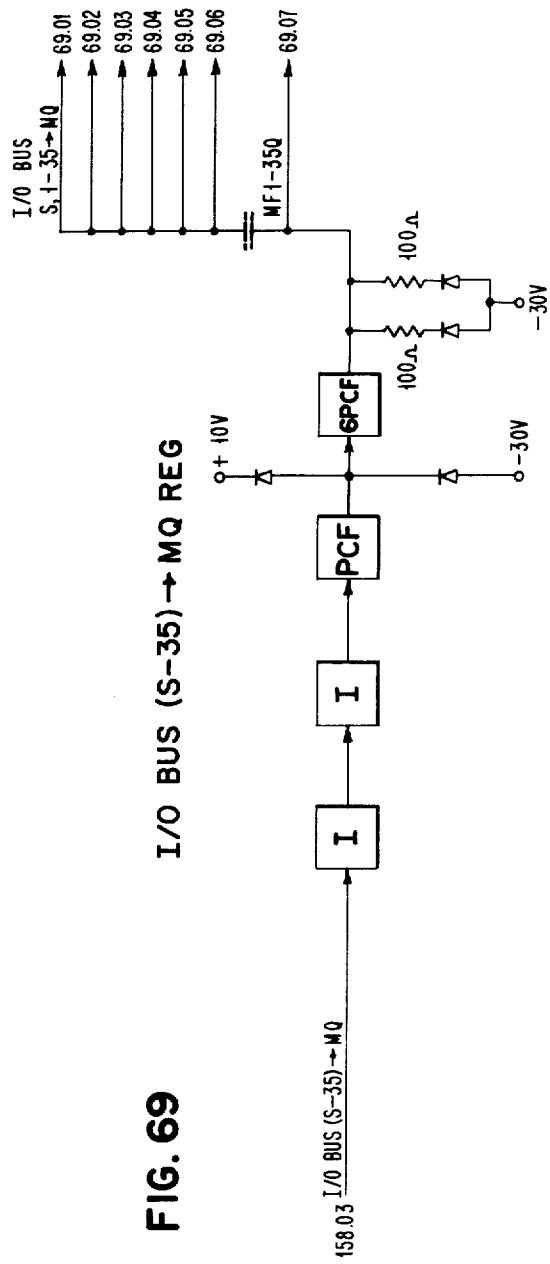


FIG. 68



I/O BUS (S-35) → MQ REG

FIG. 69

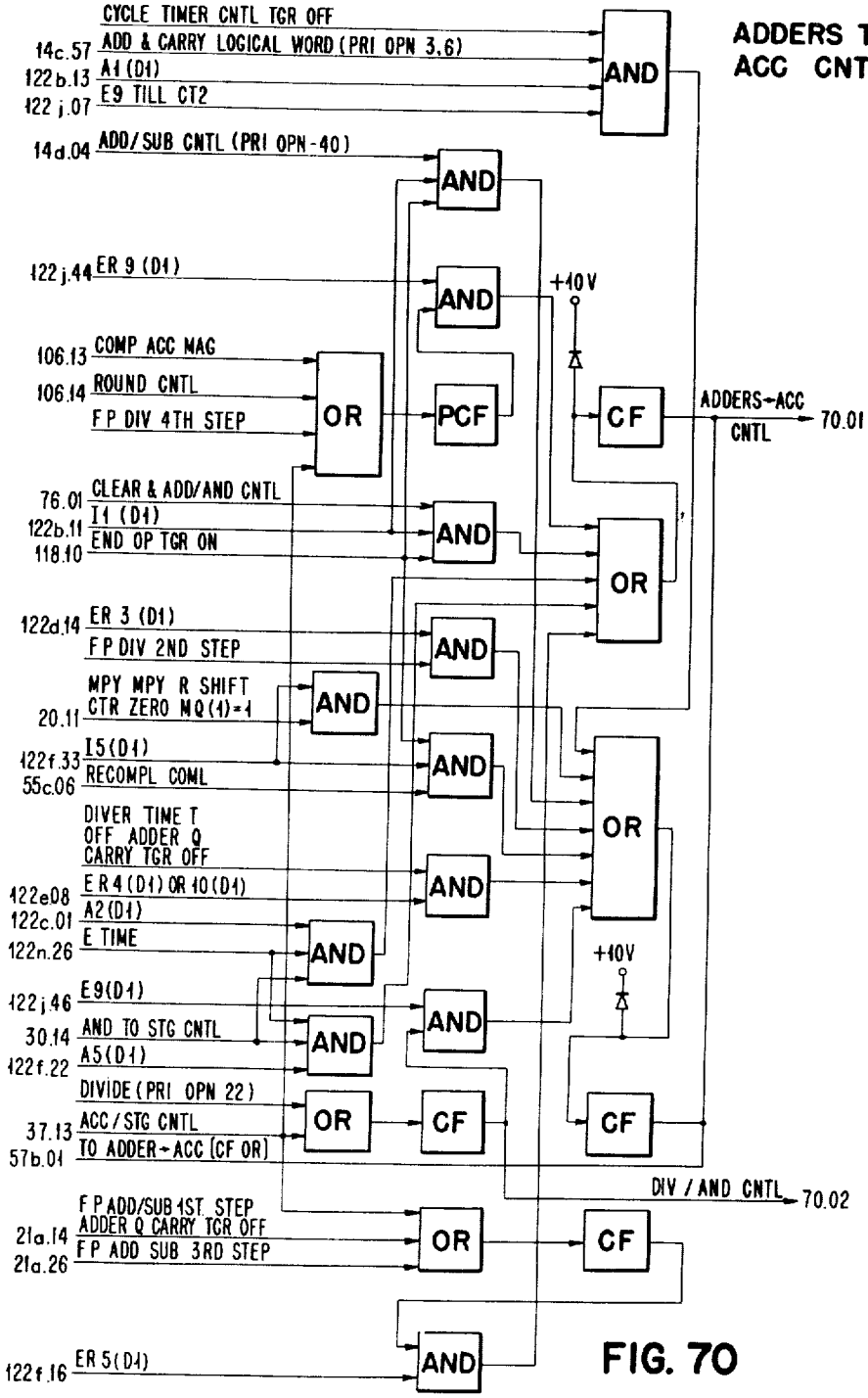

CYCLE TIMER CNTL TGR OFF
14c.57 ADD & CARRY LOGICAL WORD (PRI OPN 3,6)
122b.13 A1 (D1)
122j.07 E9 TILL CT2
AND
ADDERS TO ACC CNTL
14d.04 ADD/SUB CNTL (PRI OPN-40)
AND
122j.44 ER 9 (D1)
AND
+40V
106.13 COMP ACC MAG
106.14 ROUND CNTL
F P DIV 4TH STEP
OR
PCF
CF
ADDERS→ACC CNTL
70.01
76.01 CLEAR & ADD/AND CNTL
122b.11 I1 (D1)
118.10 END OP TGR ON
AND
OR
122d.14 ER 3 (D1)
F P DIV 2ND STEP
AND
MPY MPY R SHIFT
20.11 CTR ZERO MQ(1)=1
AND
122f.33 I5(D1)
55c.06 RECOMPL COML
AND
DIVER TIME T
OFF ADDER Q
CARRY TGR OFF
AND
OR
122e08 E R 4 (D1) OR 10 (D1)
122c.01 A2(D1)
122n.26 E TIME
AND
+40V
122j.46 E9(D1)
30.14 AND TO STG CNTL
122f.22 A5(D1)
AND
AND
DIVIDE (PRI OPN 22)
37.13 ACC/STG CNTL
57b.01 TO ADDER→ACC (CF OR)
OR
CF
CF
DIV / AND CNTL
70.02
F P ADD/SUB 1ST STEP
21a.14 ADDER Q CARRY TGR OFF
21a.26 F P ADD SUB 3RD STEP
OR
CF
122f.16 ER 5(D1)
AND

FIG. 70

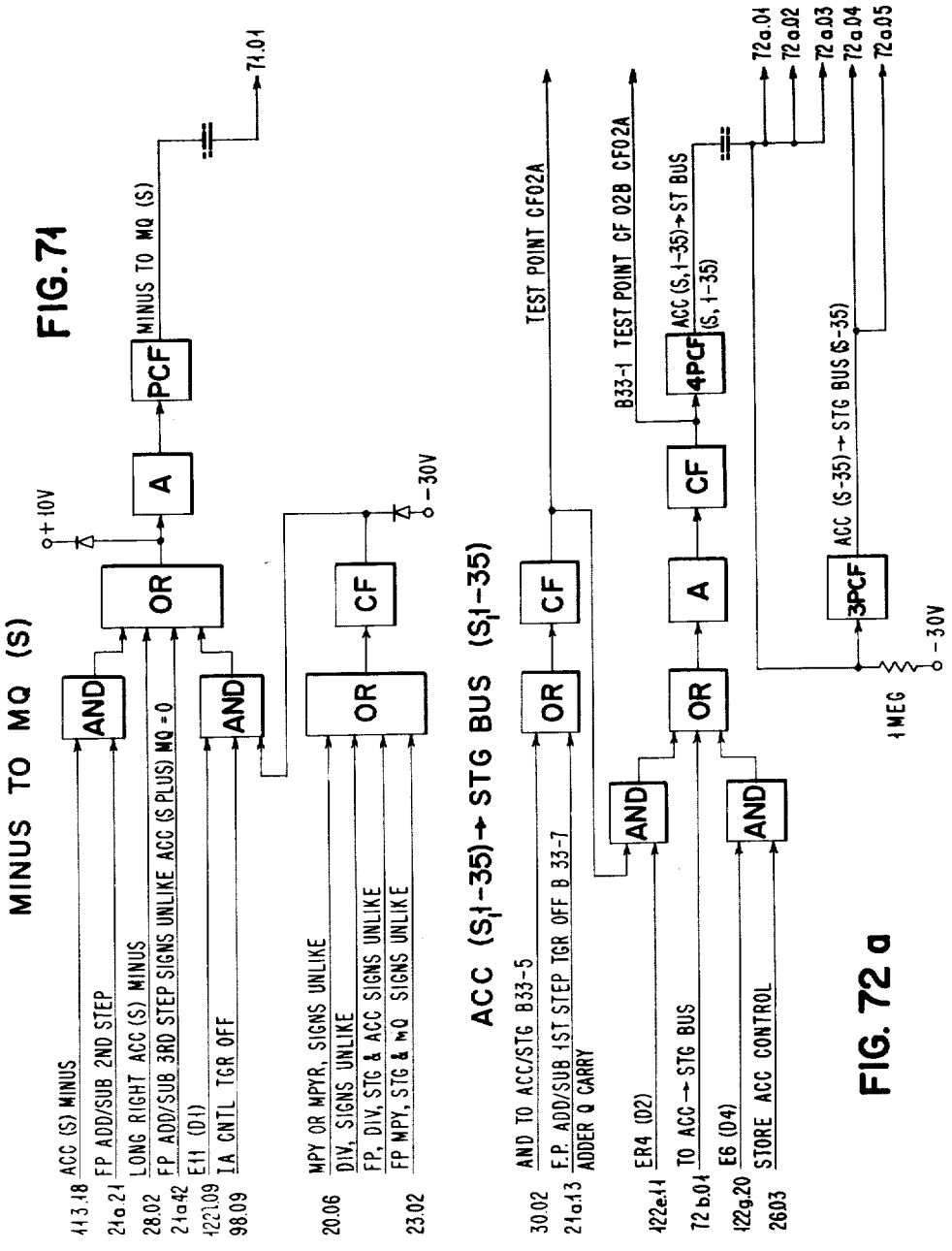


FIG. 71

FIG. 72a

FIG. 72b

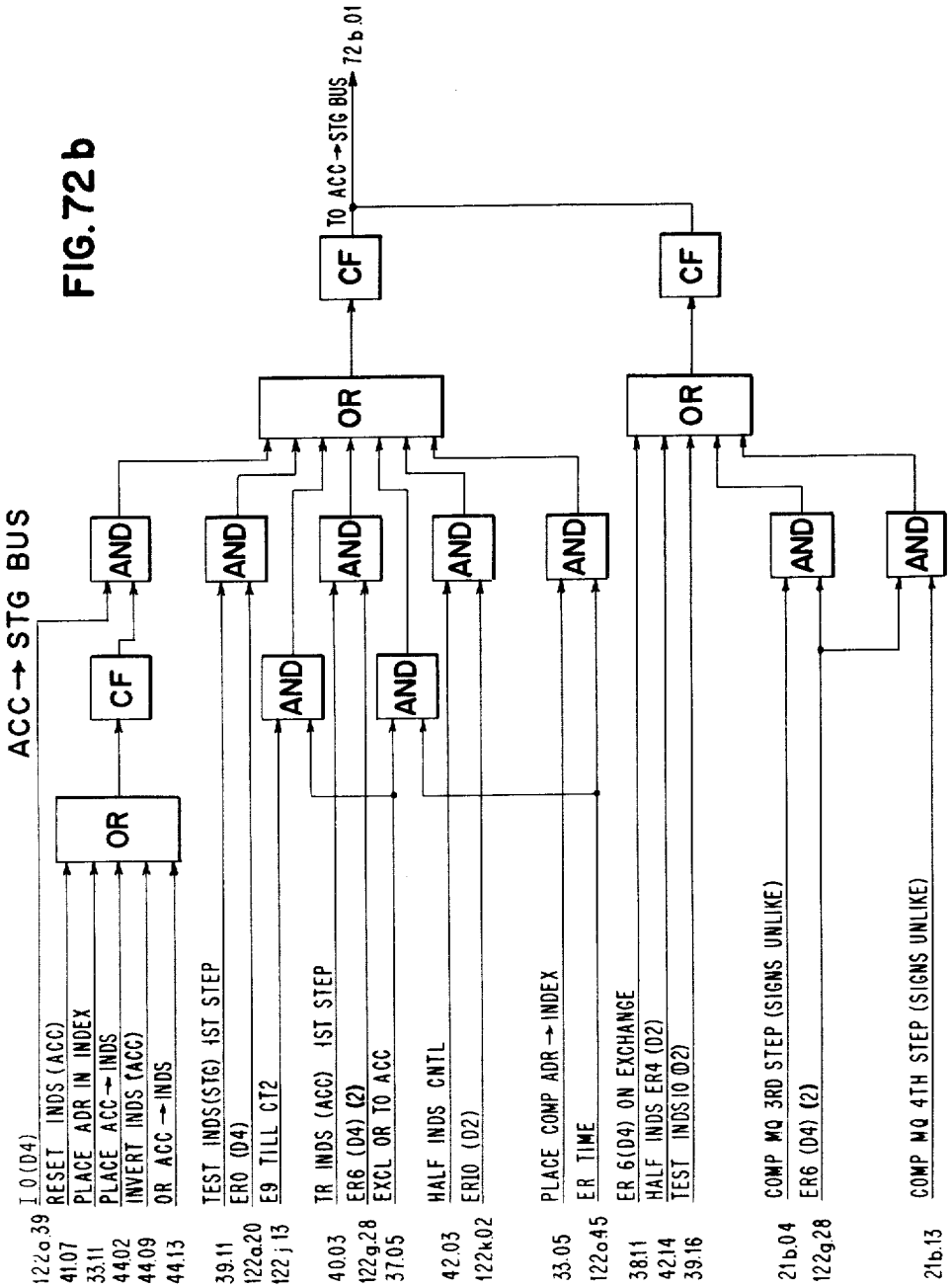

ACC→STG BUS
I 0 (D4)
RESET INDS (ACC)
PLACE ADR IN INDEX
PLACE ACC→INDS
INVERT INDS (ACC)
OR ACC→INDS
TEST INDS(STG) 1ST STEP
ER0 (D4)
E9 TILL CT2
TR INDS (ACC) 1ST STEP
ER6 (D4) (2)
EXCL OR TO ACC
HALF INDS CNTL
ER10 (02)
PLACE COMP ADR→INDEX
ER TIME
ER 6(D4) ON EXCHANGE
HALF INDS ER4 (02)
TEST INDS 10 (02)
COMP MQ 3RD STEP (SIGNS UNLIKE)
ER6 (D4) (2)
COMP MQ 4TH STEP (SIGNS UNLIKE)
AND
OR
CF
TO ACC→STG BUS 72b.01
122a.39
41.07
33.11
44.02
44.09
44.13
39.11
122a.20
122j.13
40.03
122g.28
37.05
42.03
122k.02
33.05
122a.45
38.11
42.14
39.16
21b.04
122g.28
21b.13

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FIG 73

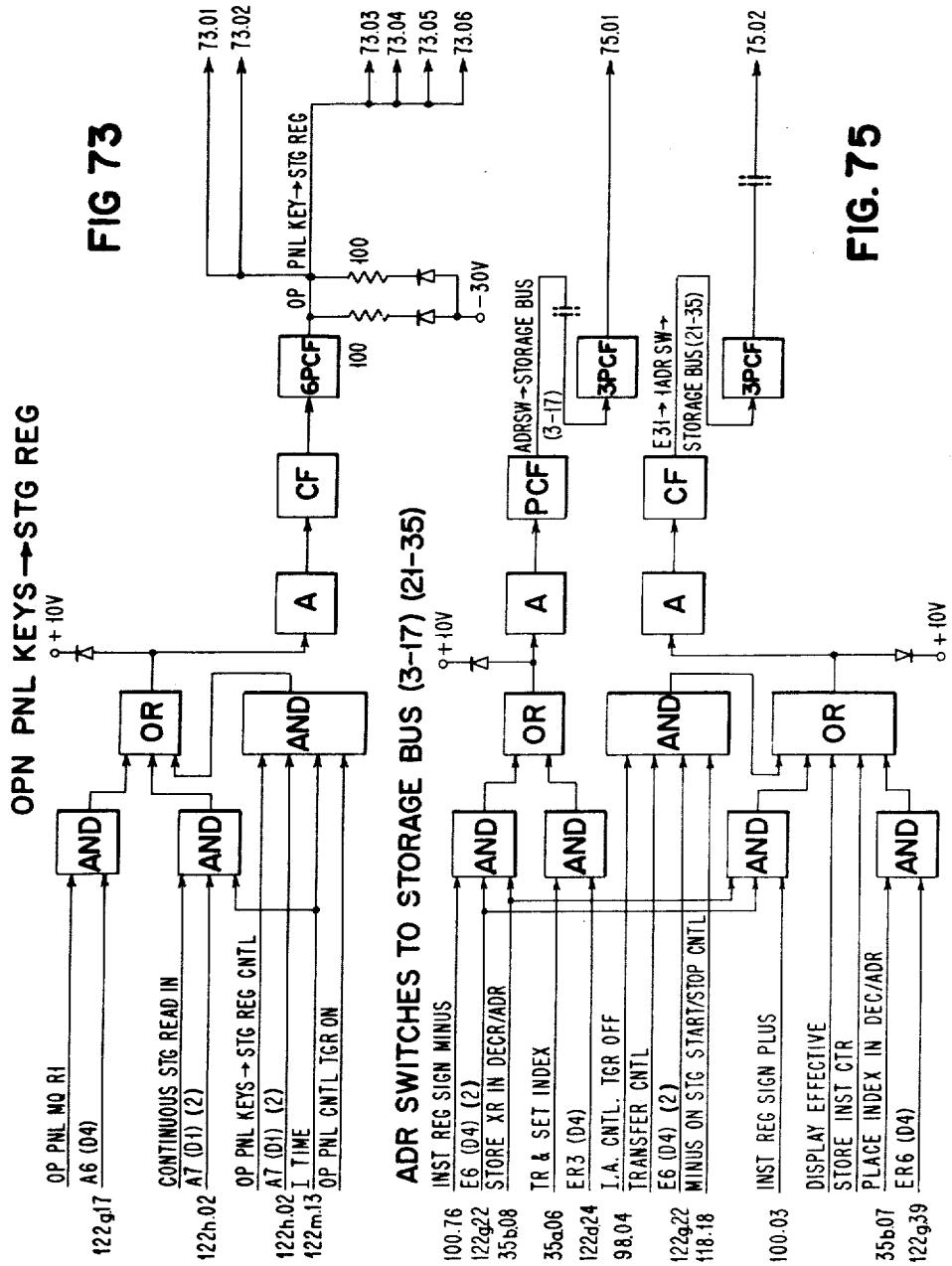


FIG. 75

FIG. 74

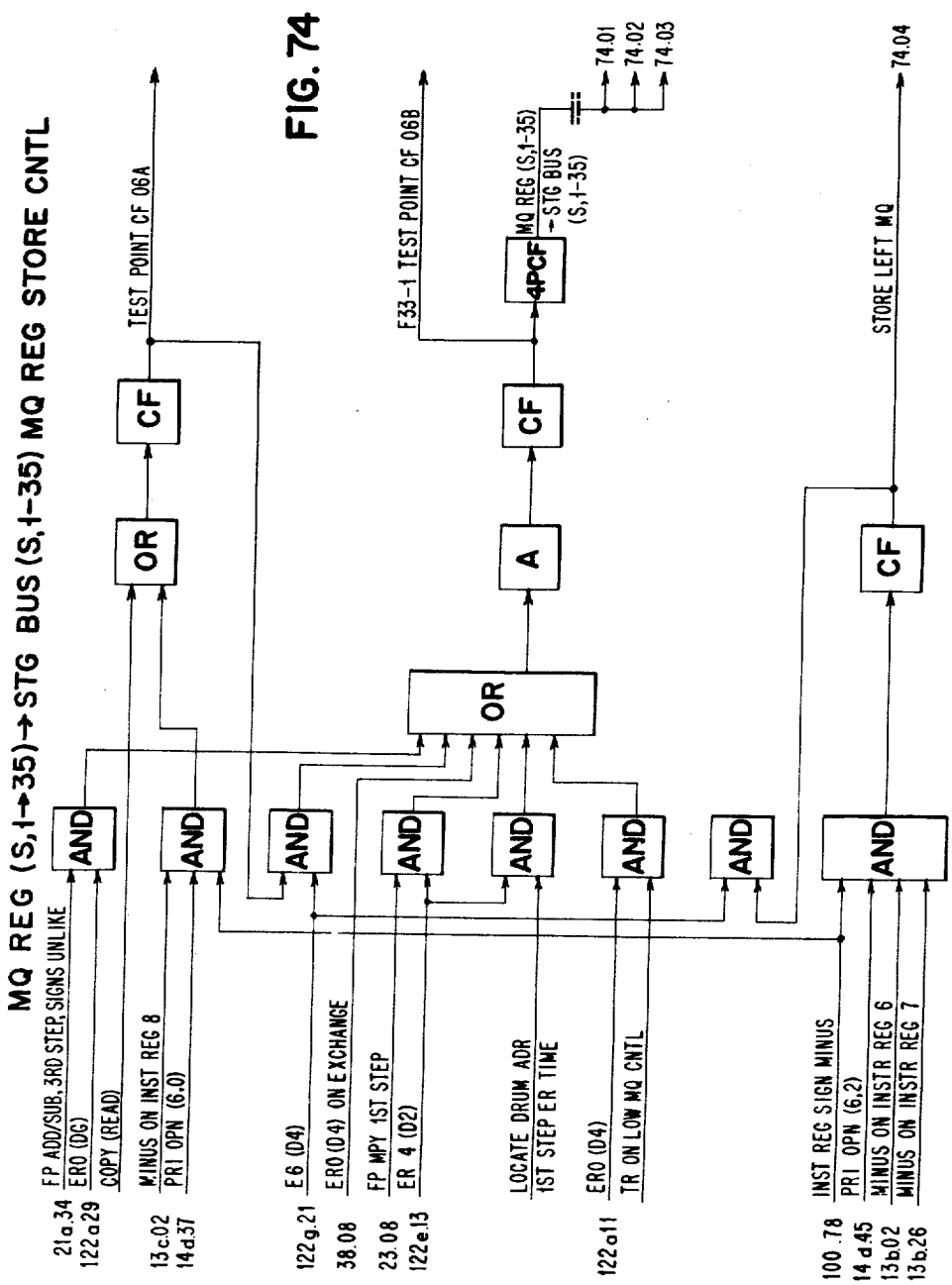

MQ REG (S,1→35)→STG BUS (S,1-35) MQ REG STORE CNTL
21a.34 FP ADD/SUB, 3RD STEP, SIGNS UNLIKE
122a29 ERO (DG)
COPY (READ)
13c.02 MINUS ON INST REG 8
14d37 PR1 OPN (6.0)
122g.21 E6 (D4)
38.08 ERO (D4) ON EXCHANGE
23.08 FP MPY 1ST STEP
122e13 ER 4 (D2)
LOCATE DRUM ADR
1ST STEP ER TIME
122a11 ERO (D4)
TR ON LOW MQ CNTL
100.78 INST REG SIGN MINUS
14a45 PR1 OPN (6,2)
13b02 MINUS ON INSTR REG 6
13b26 MINUS ON INSTR REG 7
AND
OR
CF
A
4PCF
TEST POINT CF 06A
F33-1 TEST POINT CF 06B
MQ REG (S,1-35) → STG BUS (S,1-35)
74.01
74.02
74.03
74.04
STORE LEFT MQ

FIG. 76

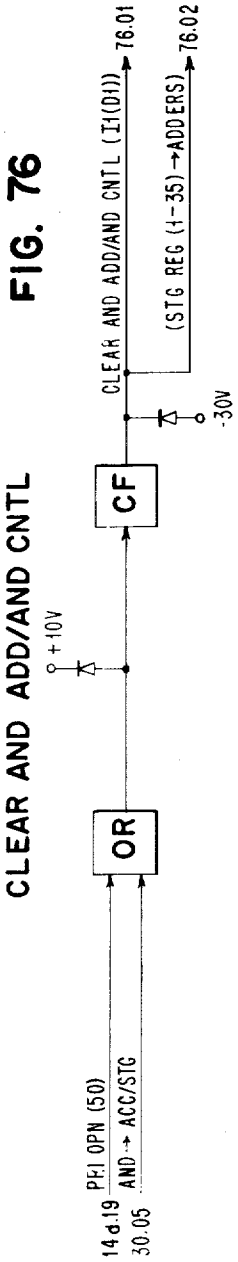
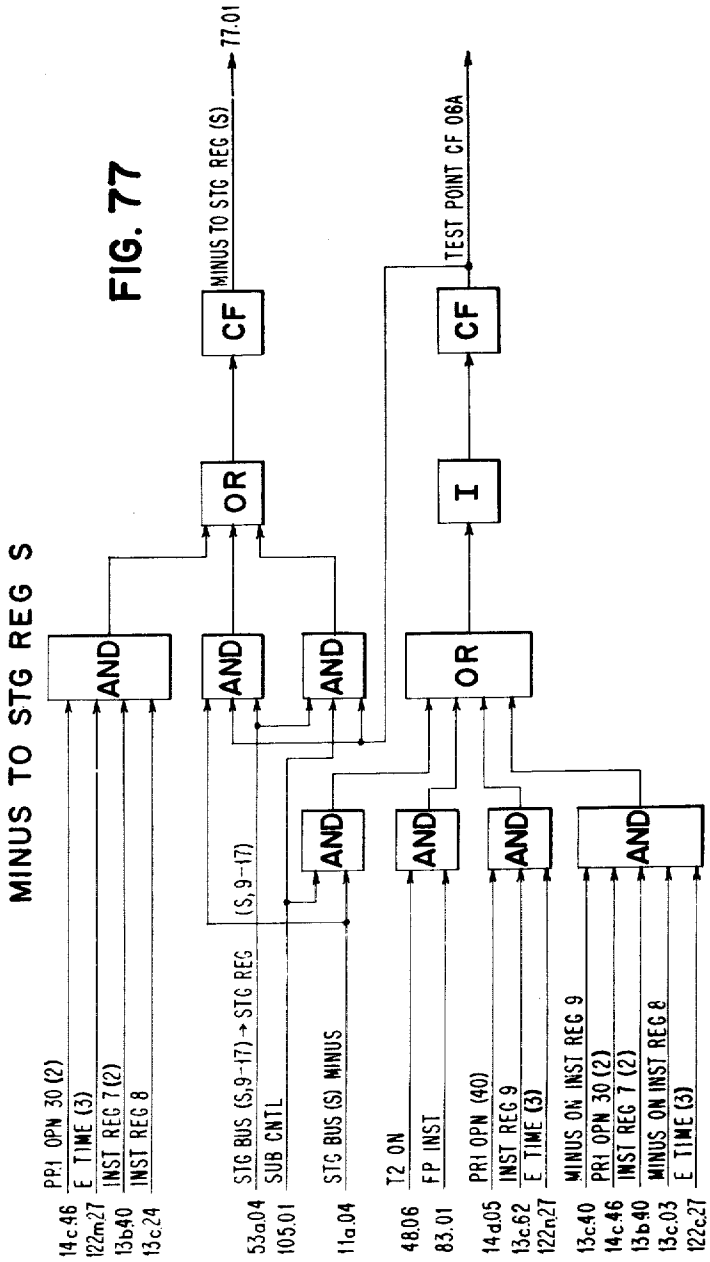

CLEAR AND ADD/AND CNTL
+10V
OR
CF
CLEAR AND ADD/AND CNTL (I1(01)) → 76.01
(STG REG (1-35) → ADDERS) → 76.02
-30V
14d.19 PR1 OPN (50)
30.05 AND → ACC/STG

FIG. 77


MINUS TO STG REG S
AND
OR
CF
MINUS TO STG REG (S) → 77.01
14c.46 PR1 OPN 30 (2)
122m27 E TIME (3)
13b40 INST REG 7 (2)
13c24 INST REG 8
53a.04 STG BUS (S,9-17) → STG REG (S,9-17)
105.01 SUB CNTL
11a.04 STG BUS (S) MINUS
I
TEST POINT CF 06A
48.06 T2 ON
83.01 FP INST
14d.05 PR1 OPN (40)
13c.62 INST REG 9
122n27 E TIME (3)
13c.40 MINUS ON INST REG 9
14c.46 PR1 OPN 30 (2)
13b.40 INST REG 7 (2)
13c.03 MINUS ON INST REG 8
122c.27 E TIME (3)

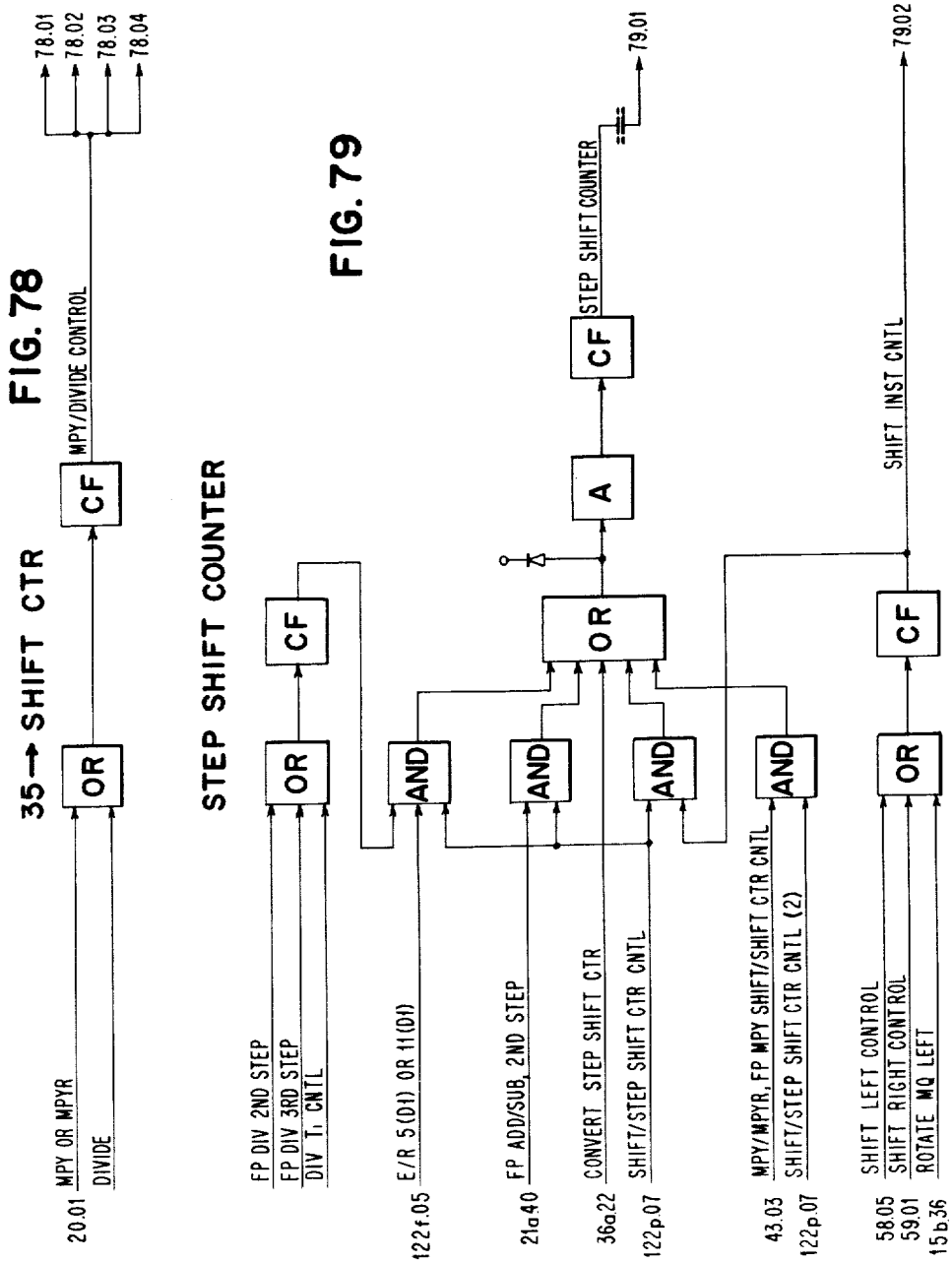

35→ SHIFT CTR
OR
CF
MPY/DIVIDE CONTROL
78.01
78.02
78.03
78.04
20.01 MPY OR MPYR
DIVIDE
STEP SHIFT COUNTER
OR
CF
FP DIV 2ND STEP
FP DIV 3RD STEP
DIV T1 CNTL
AND
122f.05 E/R 5(D1) OR 11(D1)
AND
21a40 FP ADD/SUB, 2ND STEP
AND
36a22 CONVERT STEP SHIFT CTR
122p.07 SHIFT/STEP SHIFT CTR CNTL
AND
43.03 MPY/MPYR, FP MPY SHIFT/SHIFT CTR CNTL
122p.07 SHIFT/STEP SHIFT CTR CNTL (2)
OR
A
CF
STEP SHIFT COUNTER
79.01
CF
SHIFT INST CNTL
79.02
OR
58.05 SHIFT LEFT CONTROL
59.01 SHIFT RIGHT CONTROL
15b36 ROTATE MQ LEFT

FIG. 78

FIG. 79

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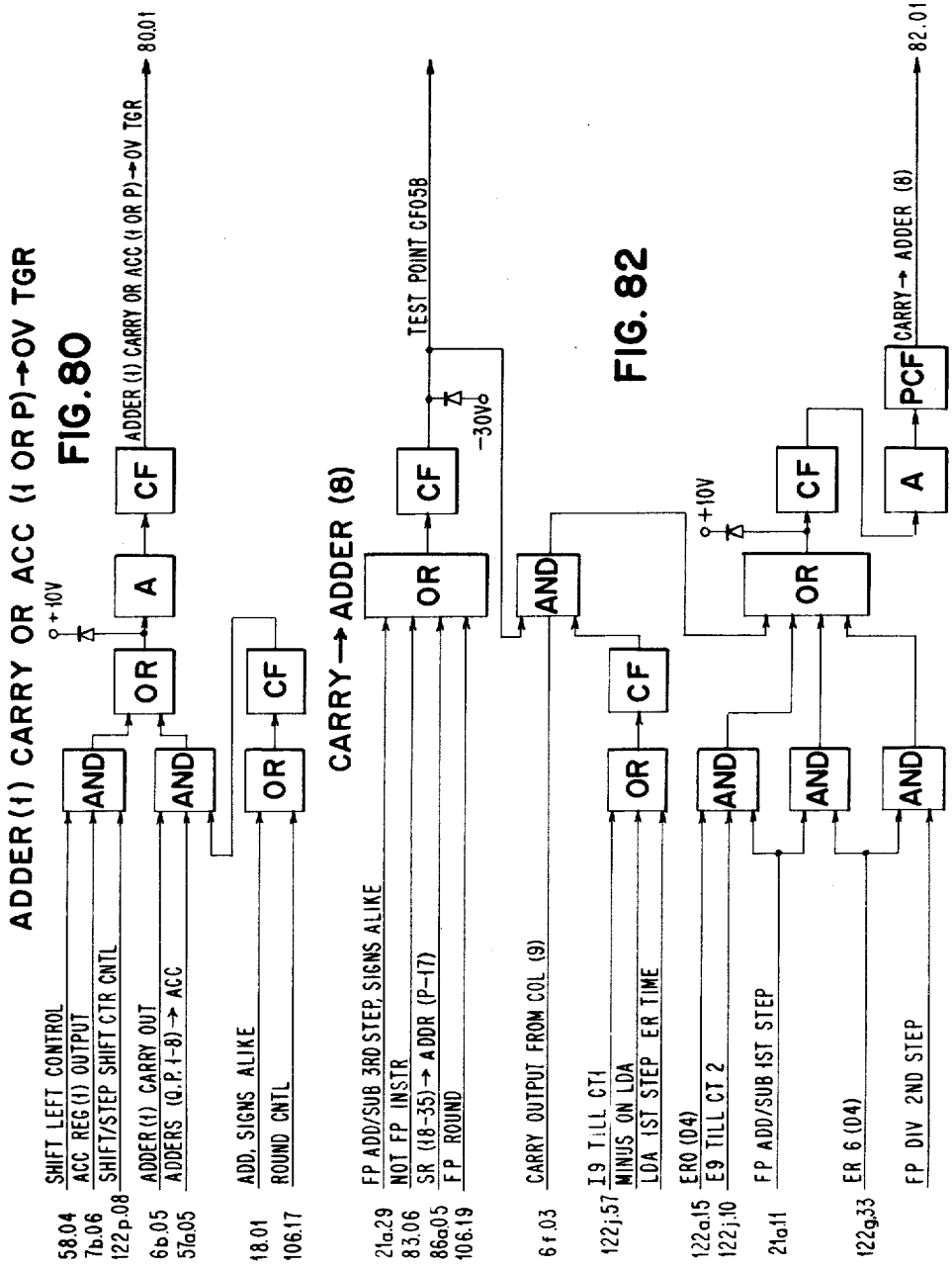

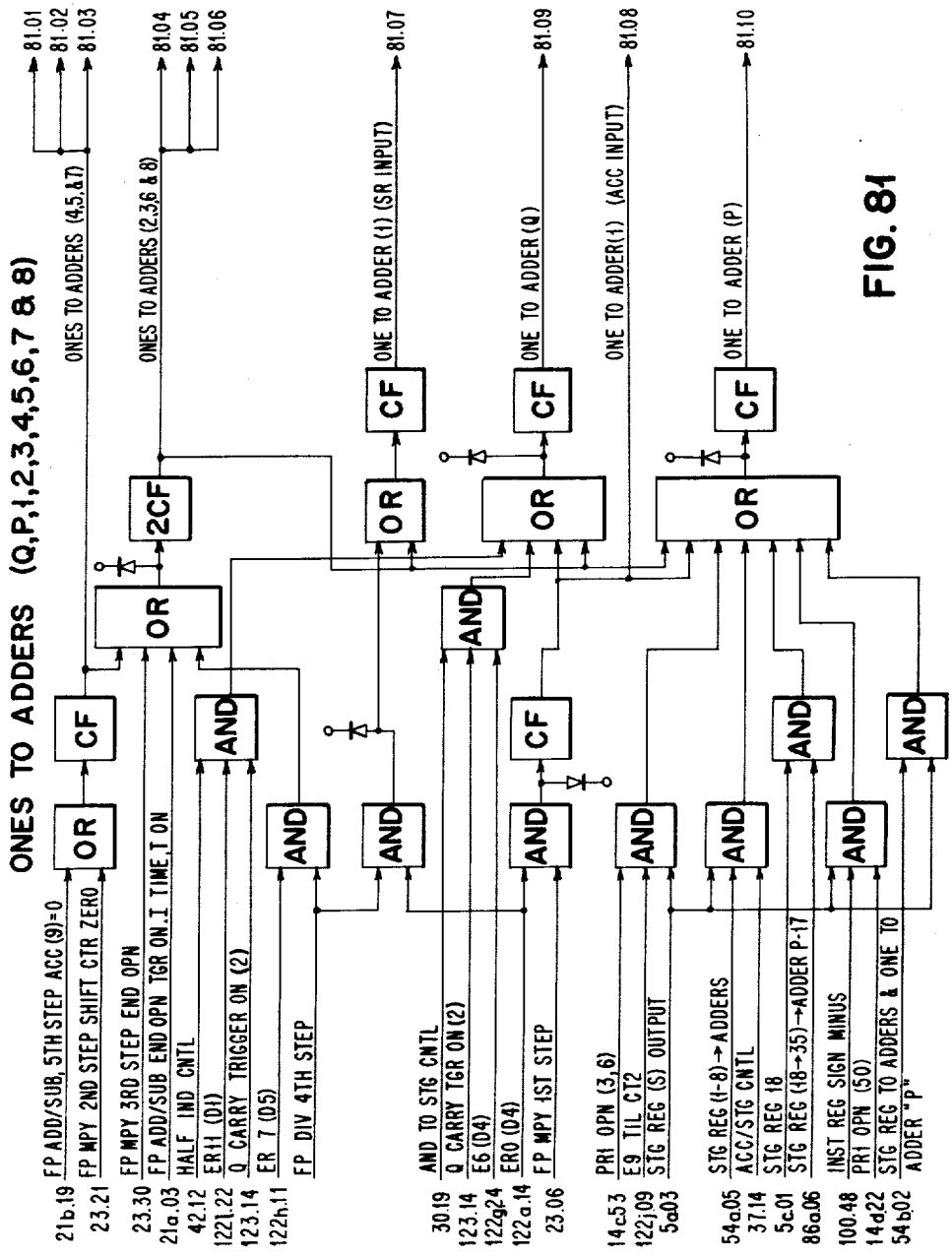
ONES TO ADDERS (Q,P,1,2,3,4,5,6,7 & 8)
81.01
81.02
81.03
ONES TO ADDERS (4,5,&7)
81.04
81.05
81.06
ONES TO ADDERS (2,3,6 & 8)
81.07
ONE TO ADDER (1) (SR INPUT)
81.09
ONE TO ADDER (Q)
81.08
ONE TO ADDER(1) (ACC INPUT)
81.10
ONE TO ADDER (P)
CF
2CF
OR
AND
21b.19 FP ADD/SUB, 5TH STEP ACC (9)=0
23.21 FP MPY 2ND STEP SHIFT CTR ZERO
23.30 FP MPY 3RD STEP END OPN
21a.03 FP ADD/SUB END OPN TGR ON.I TIME,I ON
42.12 HALF IND CNTL
1221.22 ER11 (D1)
123.14 Q CARRY TRIGGER ON (2)
122h.11 ER 7 (D5)
FP DIV 4TH STEP
30.19 AND TO STG CNTL
123.14 Q CARRY TGR ON (2)
122g24 E6 (D4)
122a.14 ER0 (D4)
23.06 FP MPY 1ST STEP
14c53 PRI OPN (3,6)
122j09 E9 TIL C12
5a03 STG REG (S) OUTPUT
54a05 STG REG (1-8)→ADDERS
37.14 ACC/STG CNTL
5c01 STG REG 18
86a06 STG REG (18→35)→ADDER P-17
100.48 INST REG SIGN MINUS
14d22 PRI OPN (50)
54b02 STG REG TO ADDERS & ONE TO ADDER "P"

FIG. 84

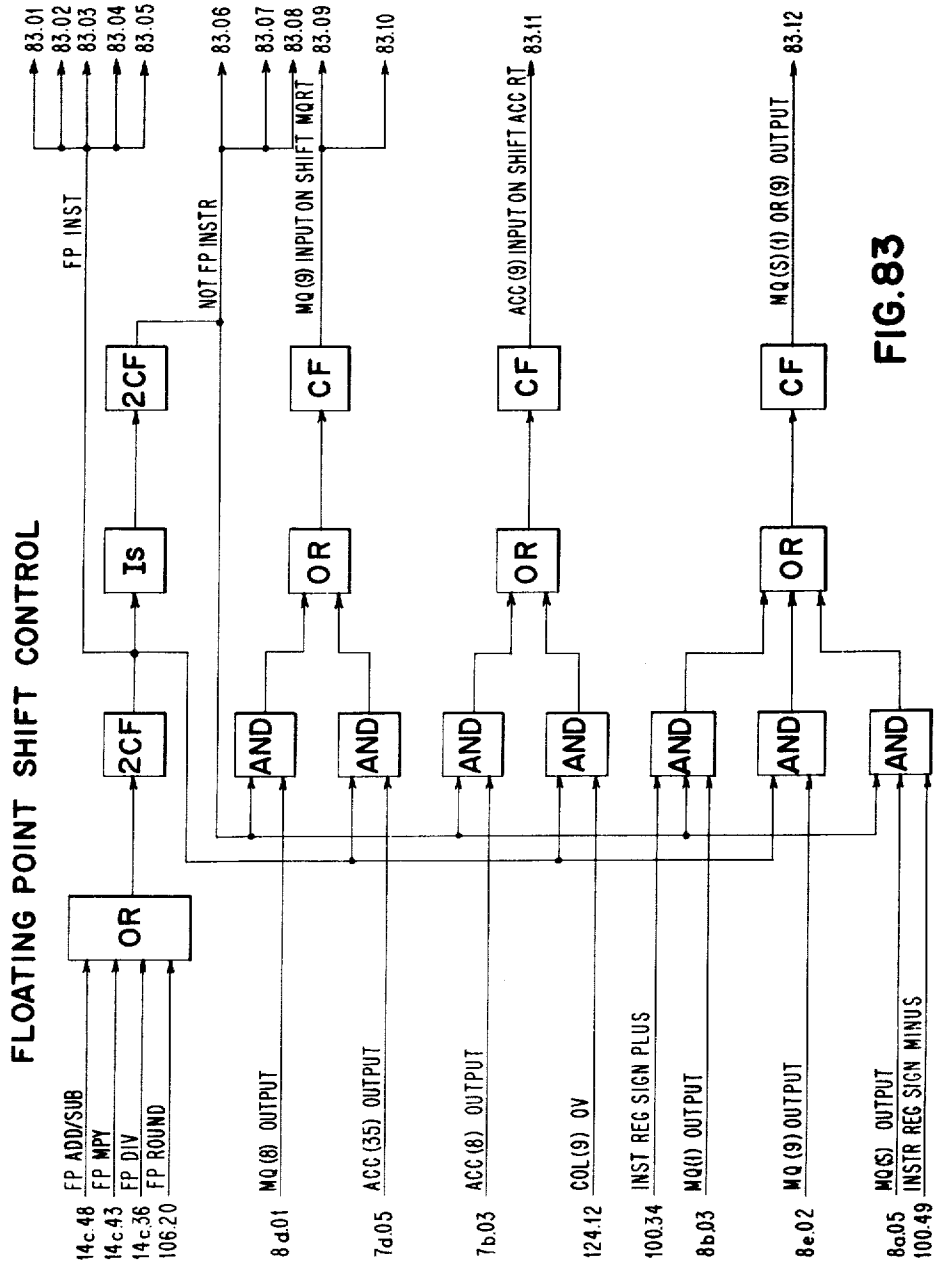
FLOATING POINT SHIFT CONTROL
14c.48 FP ADD/SUB
14c.43 FP MPY
14c.36 FP DIV
106.20 FP ROUND
OR
2CF
Is
2CF
FP INST
NOT FP INSTR
8d.01 MQ(8) OUTPUT
7d.05 ACC(35) OUTPUT
7b.03 ACC(8) OUTPUT
124.12 COL(9) OV
100.34 INST REG SIGN PLUS
8b.03 MQ(1) OUTPUT
8e.02 MQ(9) OUTPUT
8a.05 MQ(S) OUTPUT
100.49 INSTR REG SIGN MINUS
AND
AND
AND
AND
AND
AND
AND
OR
OR
OR
CF
CF
CF
MQ(9) INPUT ON SHIFT MQRT
ACC(9) INPUT ON SHIFT ACC RT
MQ(S)(1) OR(9) OUTPUT
83.01
83.02
83.03
83.04
83.05
83.06
83.07
83.08
83.09
83.10
83.11
83.12

FIG.83

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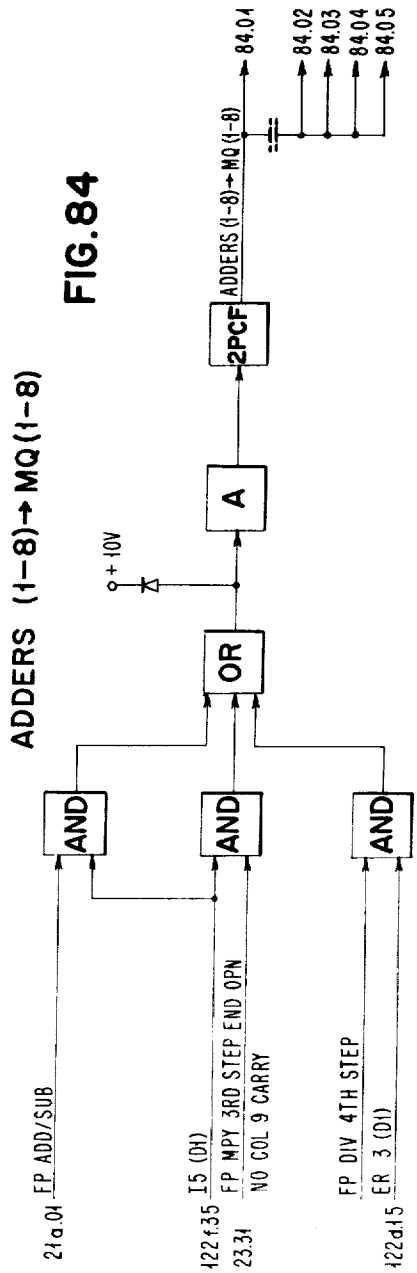

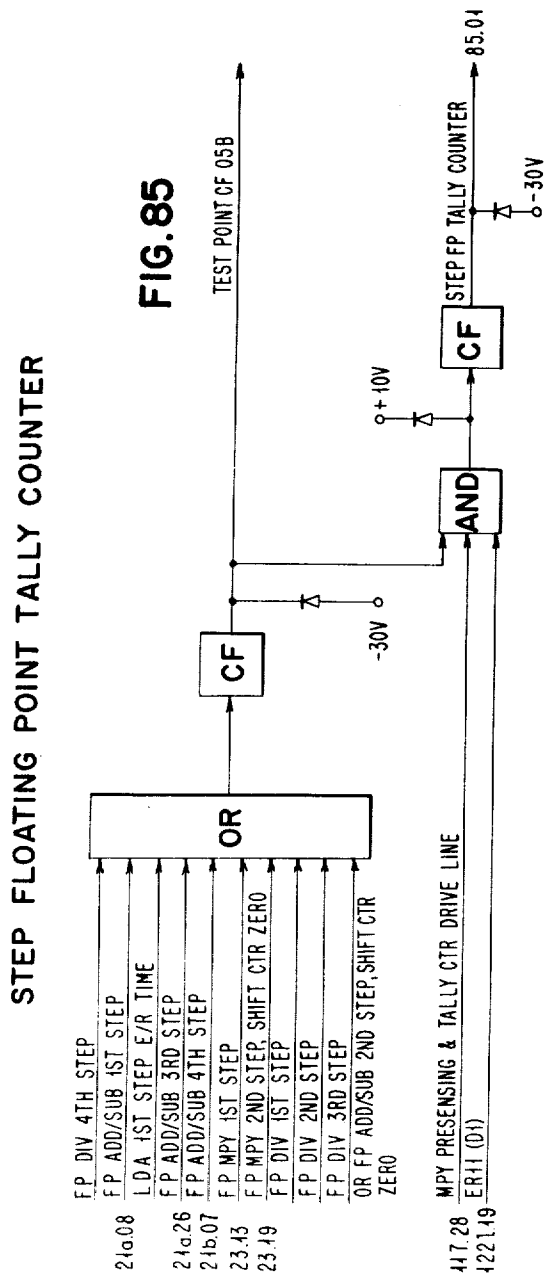

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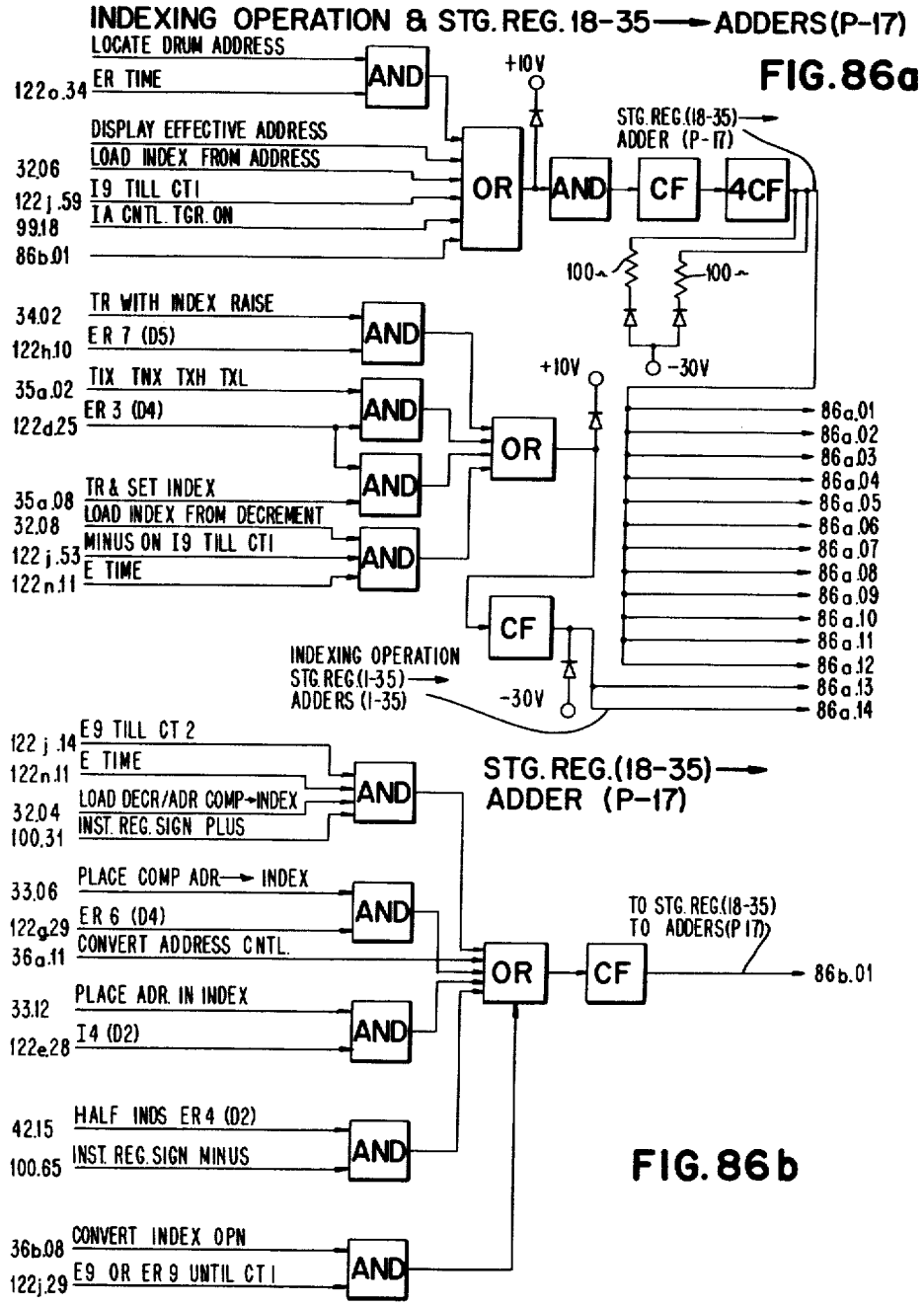

FIG. 86a

FIG. 86b

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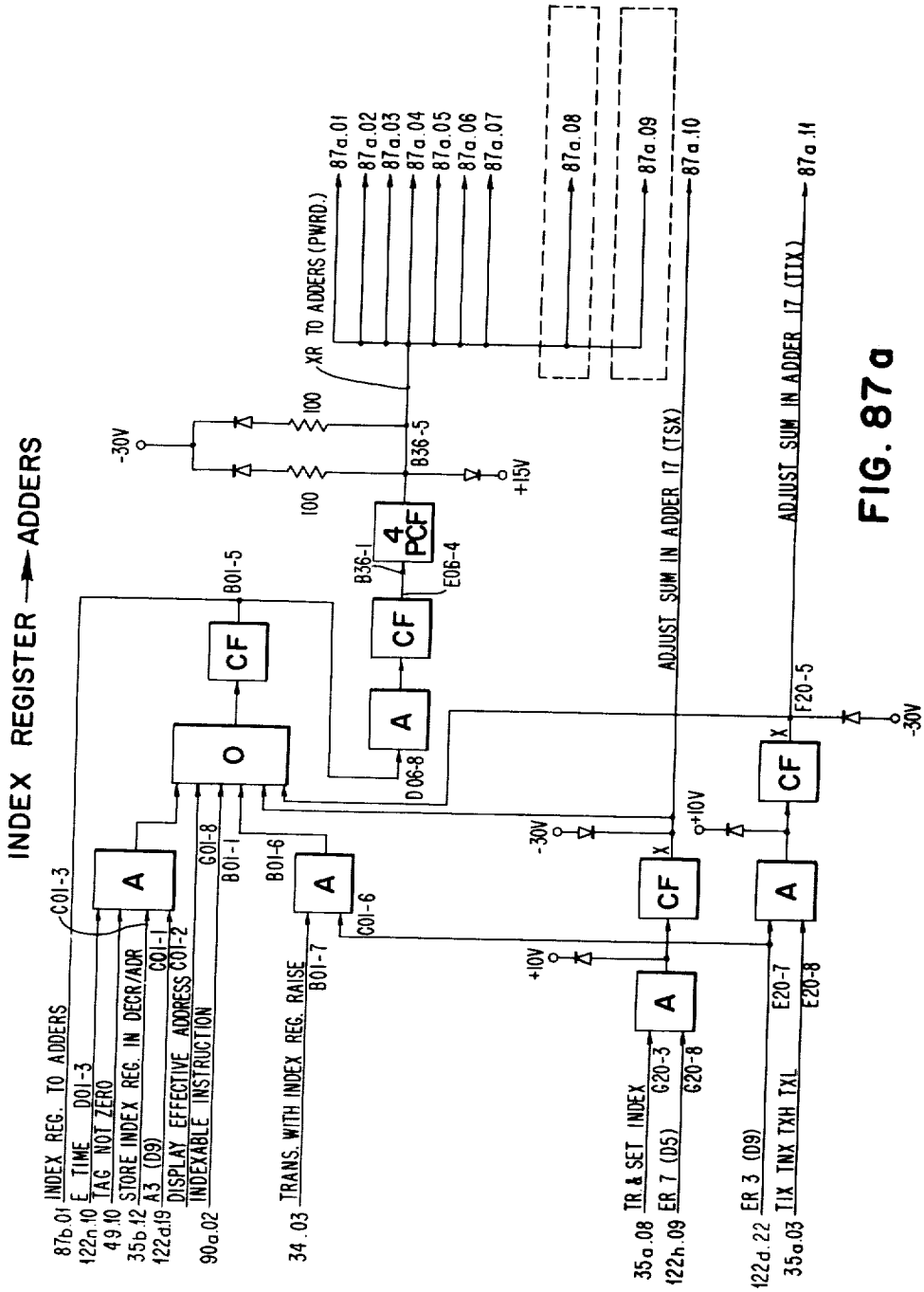


FIG. 87a

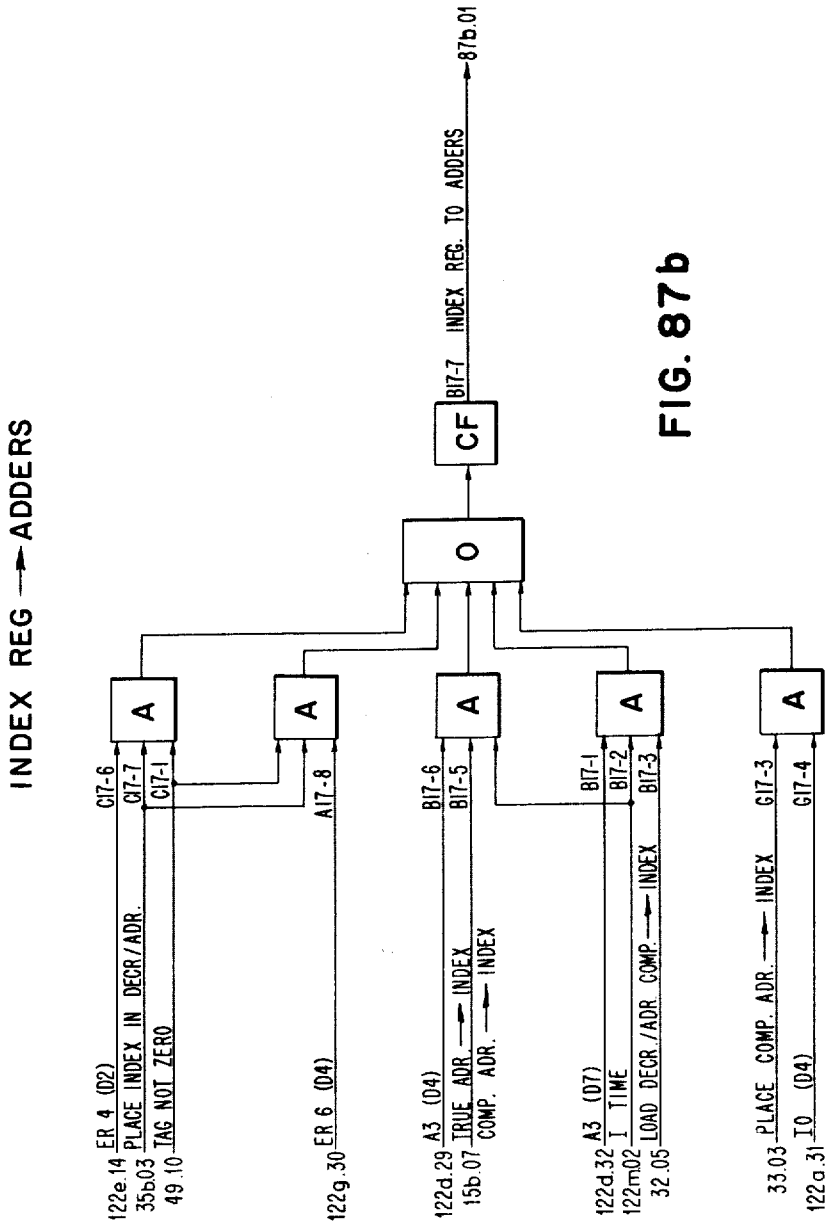

INDEX REG → ADDERS
A
A
A
A
A
O
CF
BI7-7 INDEX REG. TO ADDERS
87b.01
C17-6
C17-7
C17-1
A17-8
BI7-6
BI7-5
BI7-1
BI7-2
BI7-3
G17-3
G17-4
122e.14 ER 4 (D2)
35b.03 PLACE INDEX IN DECR/ADR.
49.10 TAG NOT ZERO
122g.30 ER 6 (D4)
122d.29 A3 (D4)
15b.07 TRUE ADR. → INDEX
COMP. ADR. → INDEX
122d.32 A3 (D7)
122m02 I TIME
32.05 LOAD DECR./ADR COMP → INDEX
33.03 PLACE COMP. ADR. → INDEX
122a.31 IO (D4)

FIG. 87b

FLOATING POINT TALLY COUNTER

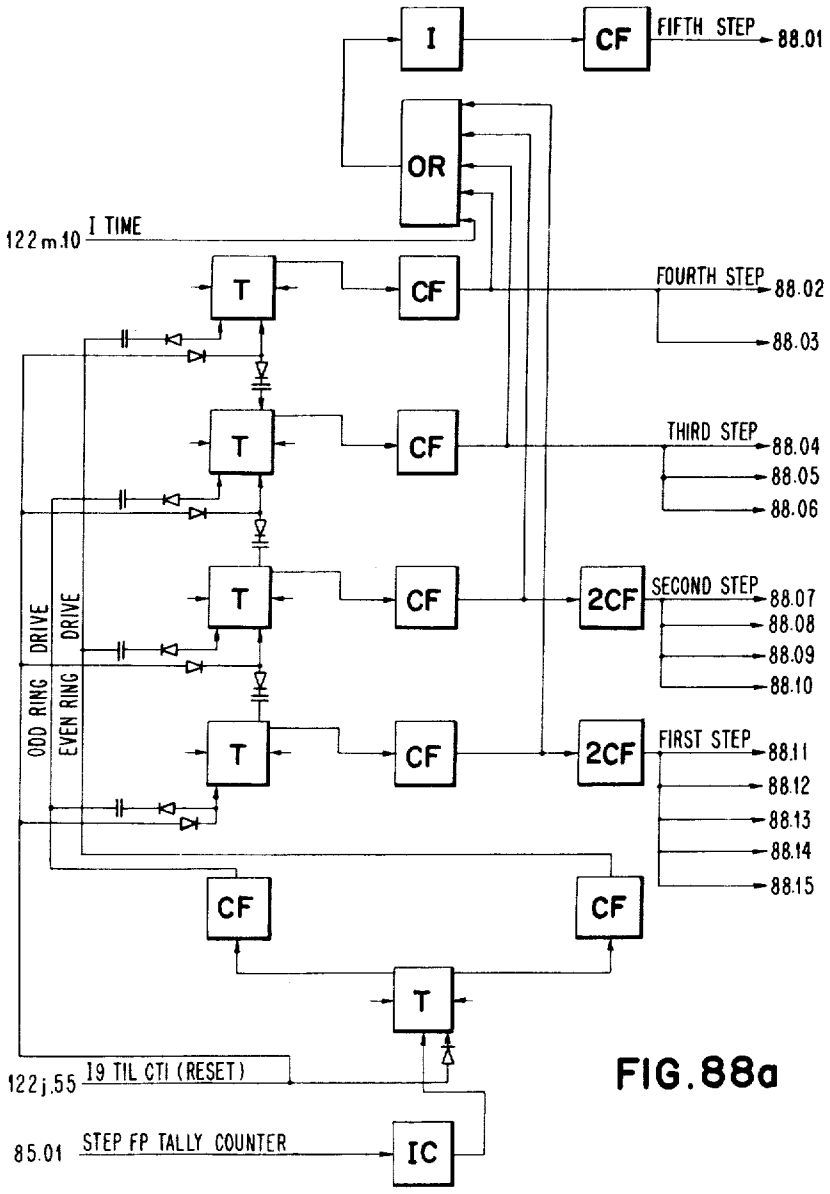


FIG. 88a

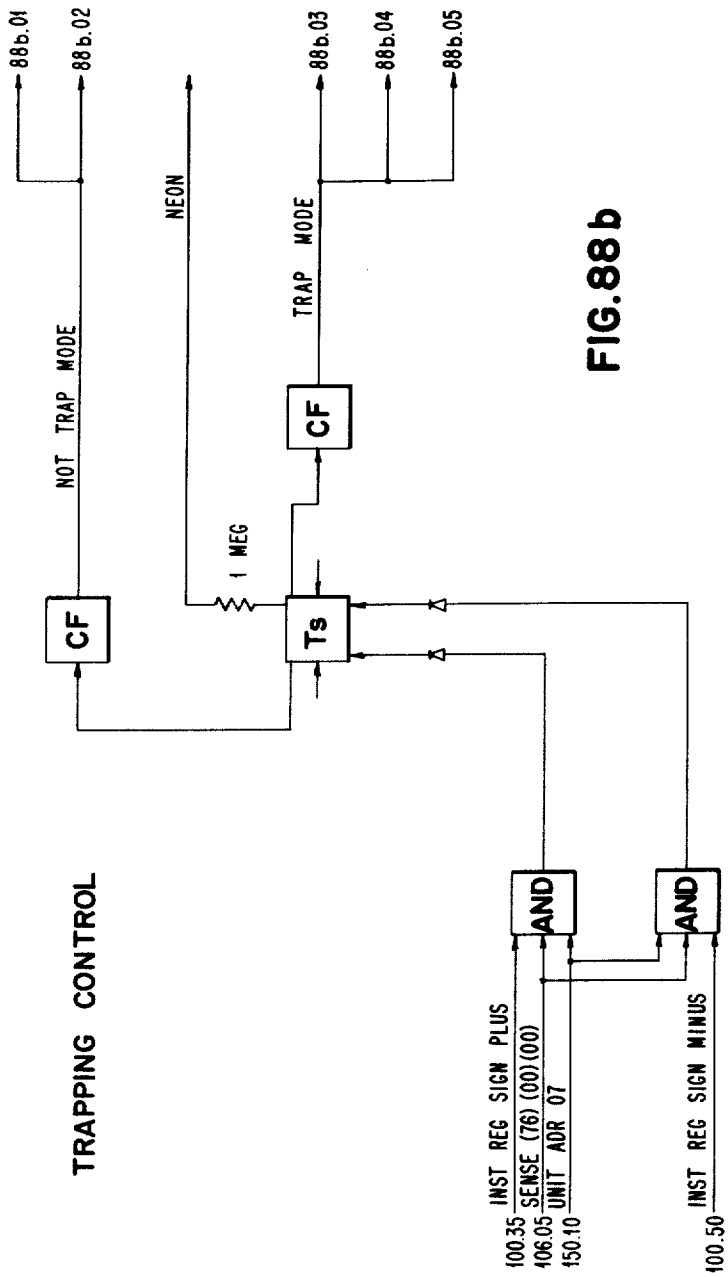

88b.01
88b.02
88b.03
88b.04
88b.05
NEON
TRAP MODE
NOT TRAP MODE
CF
CF
1 MEG
Ts
AND
AND
TRAPPING CONTROL
INST REG SIGN PLUS
100.35
SENSE (76) (00) (00)
106.05
UNIT ADR 07
150.10
INST REG SIGN MINUS
100.50

FIG. 88b

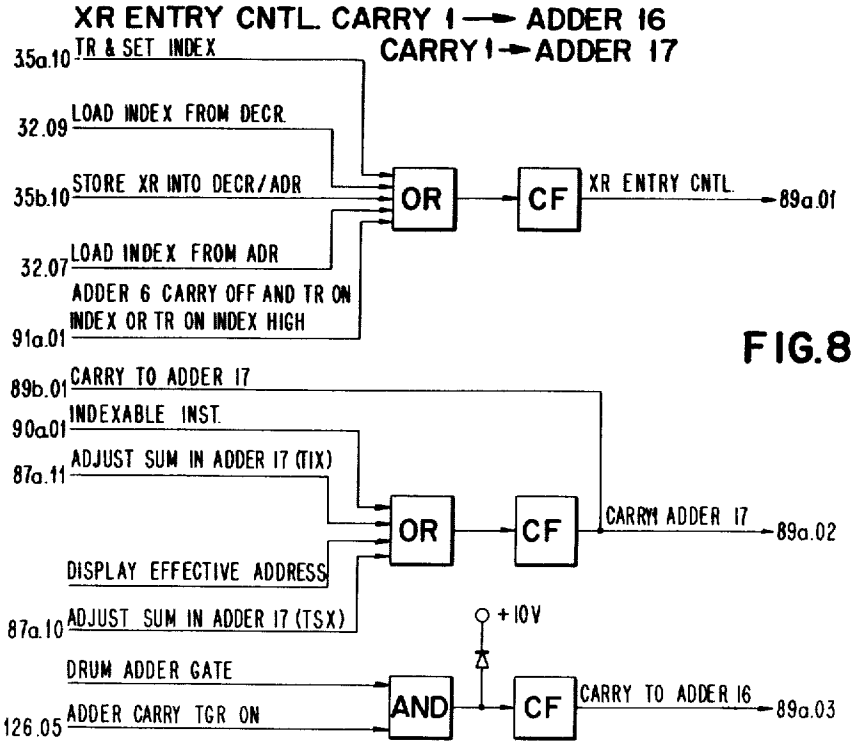


FIG.89a

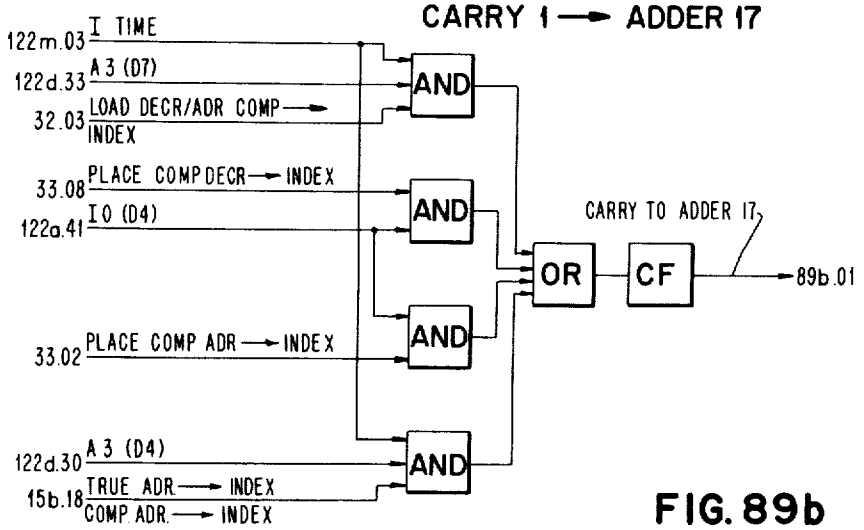
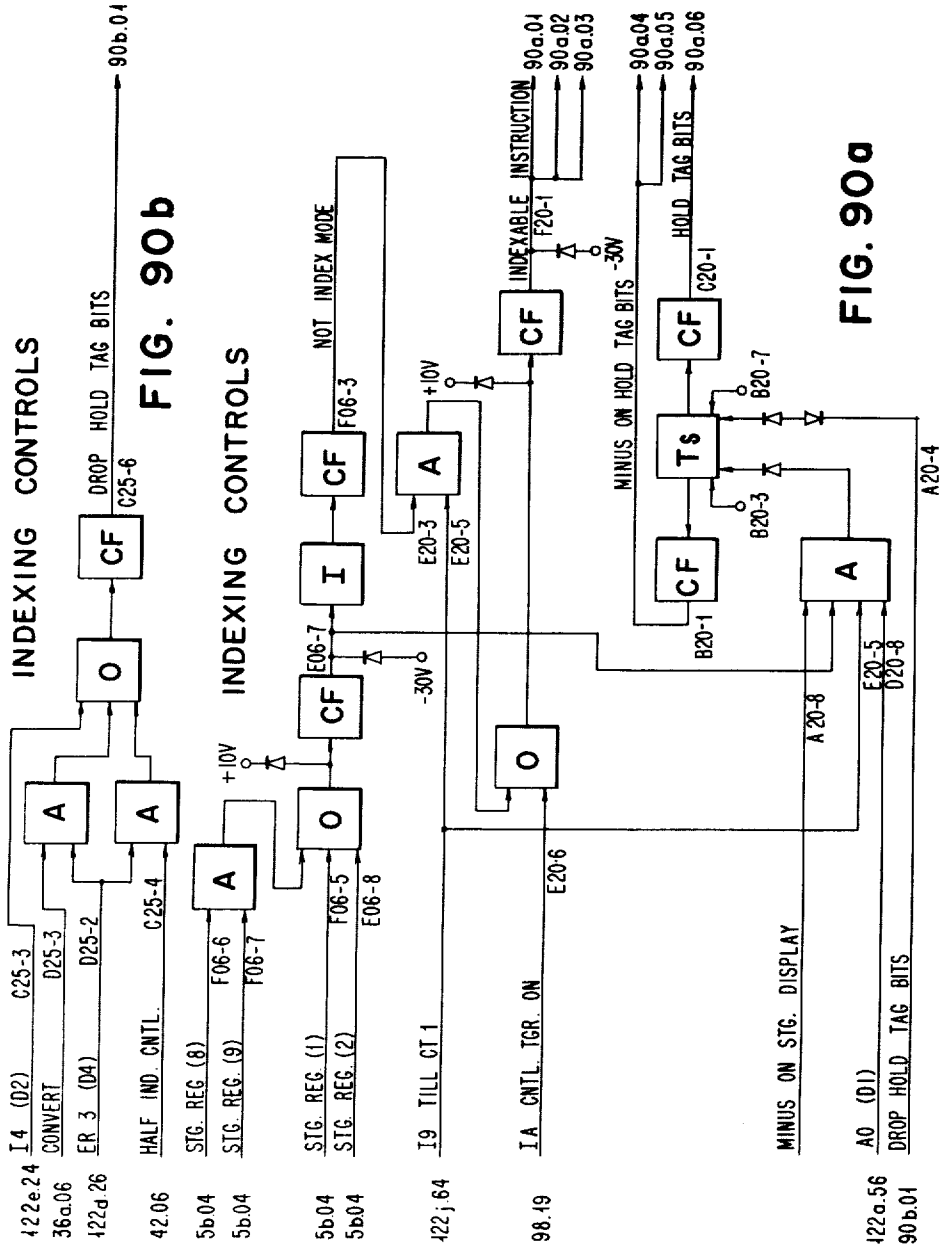


FIG. 89b


INDEXING CONTROLS
I4 (02) C25-3
CONVERT D25-3
ER 3 (04) D25-2
HALF IND. CNTL. C25-4
A
O
CF
DROP HOLD TAG BITS C25-6
90b.01
FIG. 90b
INDEXING CONTROLS
STG. REG (8) F06-6
STG. REG (9) F06-7
STG. REG (1) F06-5
STG. REG (2) E06-8
+10V
-30V
E06-7
I
F06-3
NOT INDEX MODE
I9 TILL CT 1
E20-3
E20-5
IA CNTL. TGR. ON E20-6
INDEXABLE INSTRUCTION F20-1
90a.01
90a.02
90a.03
MINUS ON HOLD TAG BITS
90a.04
90a.05
90a.06
HOLD TAG BITS C20-1
Ts
B20-7
B20-3
B20-1
MINUS ON STG. DISPLAY
A20-8
A20-4
E20-5
D20-8
AO (01)
DROP HOLD TAG BITS
FIG. 90a

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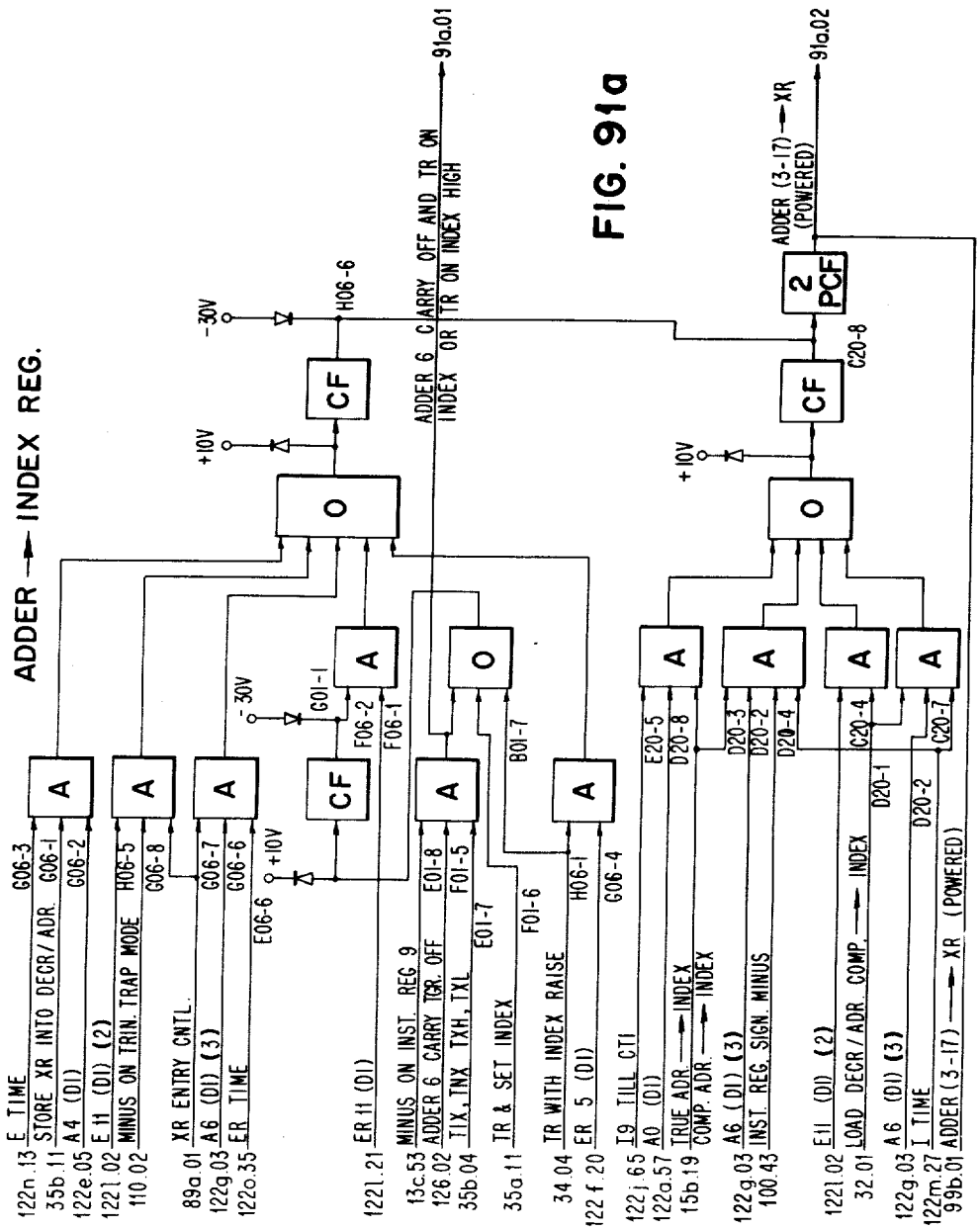

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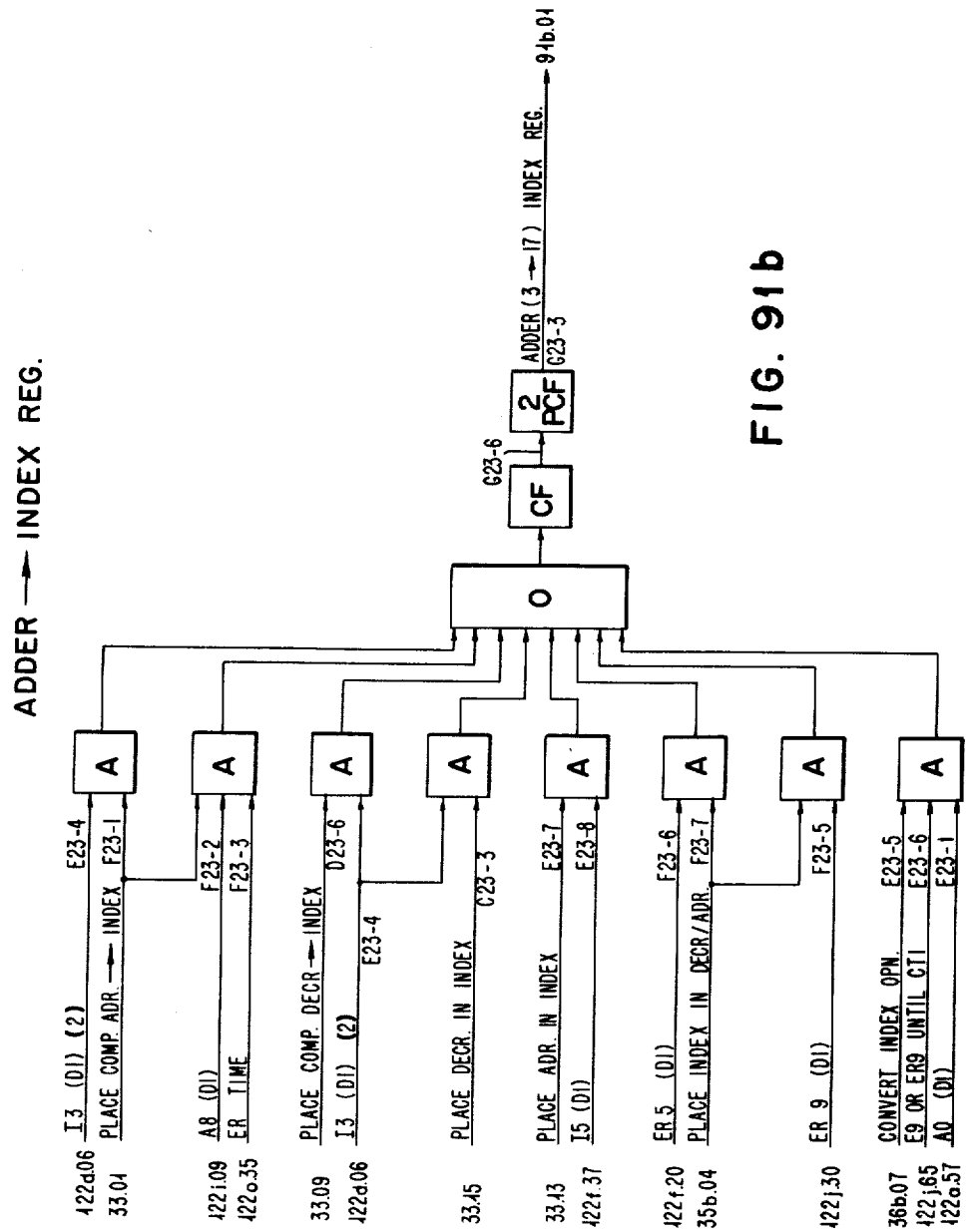


FIG. 91b

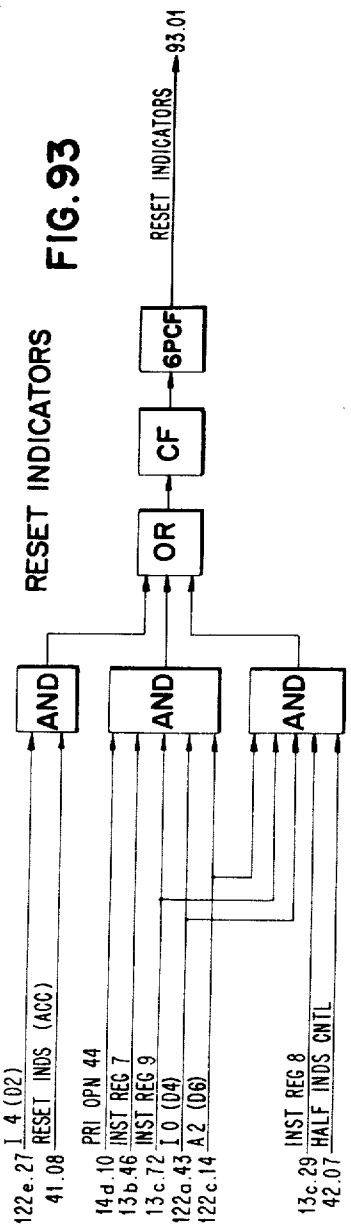

RESET INDICATORS
AND
OR
CF
6PCF
RESET INDICATORS
93.01
122e.27 I 4 (02)
41.08 RESET INDS (ACC)
14d.10 PRI OPN 44
13b.46 INST REG 7
13c.72 INST REG 9
122a.43 I 0 (04)
122c.14 A 2 (06)
13c.29 INST REG 8
42.07 HALF INDS CNTL

FIG. 93

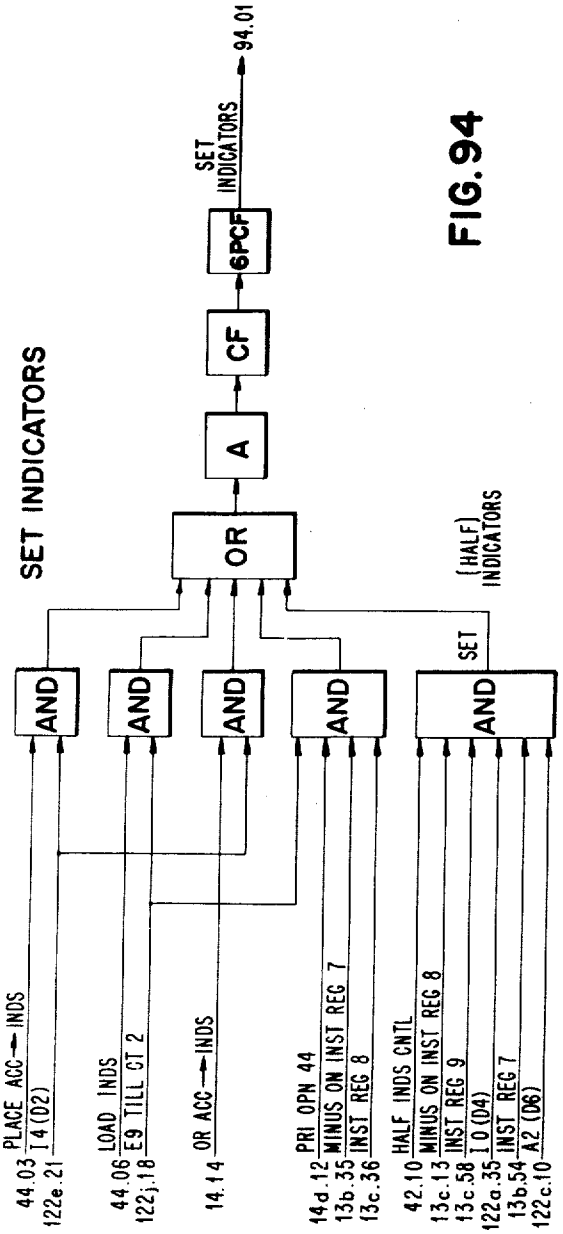

SET INDICATORS
AND
OR
A
CF
6PCF
SET INDICATORS
94.01
(HALF) INDICATORS
SET
44.03 PLACE ACC → INDS
122e.21 I 4 (02)
44.06 LOAD INDS
122j.18 E9 TILL CT 2
14.14 OR ACC → INDS
14d.12 PRI OPN 44
13b.35 MINUS ON INST REG 7
13c.36 INST REG 8
42.10 HALF INDS CNTL
13c.13 MINUS ON INST REG 8
13c.58 INST REG 9
122a.35 I 0 (04)
13b.54 INST REG 7
122c.10 A 2 (06)

FIG. 94

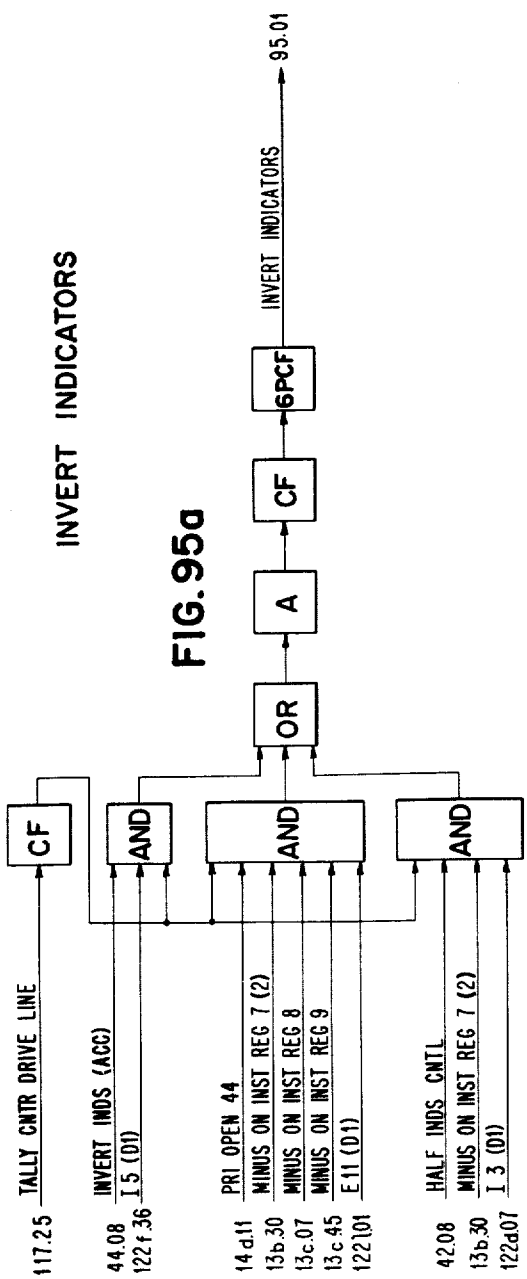


FIG. 95a

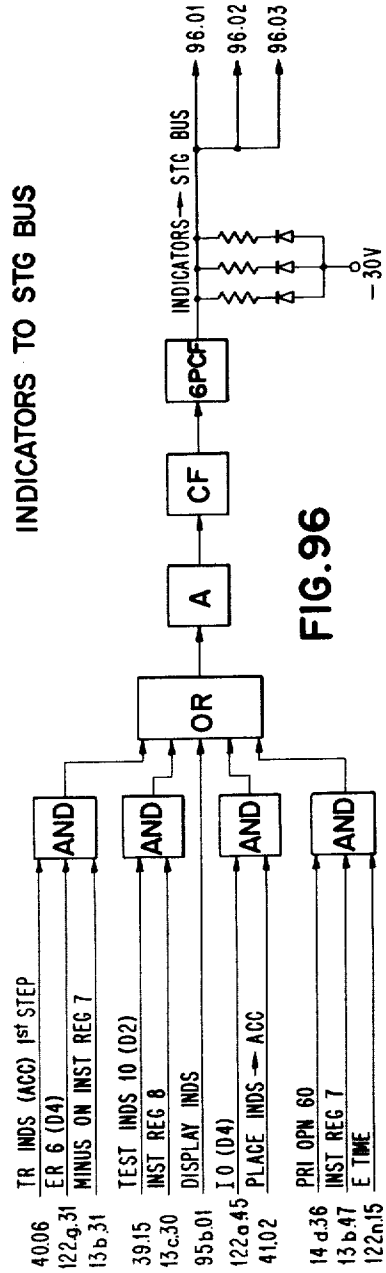


FIG. 96

FIG. 97
COMPLEMENT INDICATORS TO STG REG

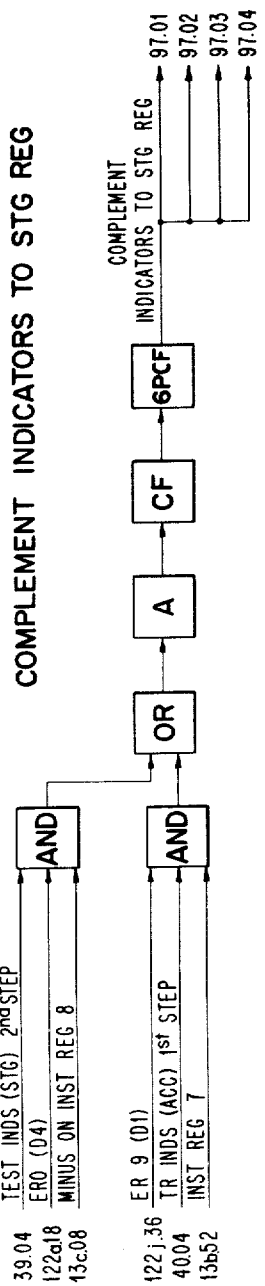


FIG. 95b
DISPLAY INDICATORS

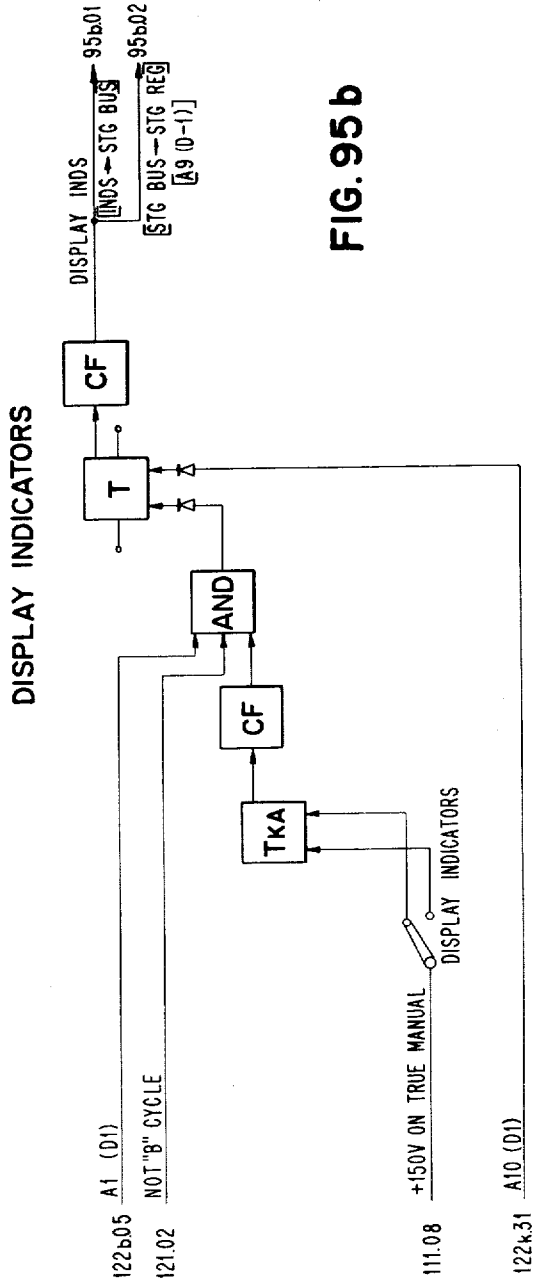
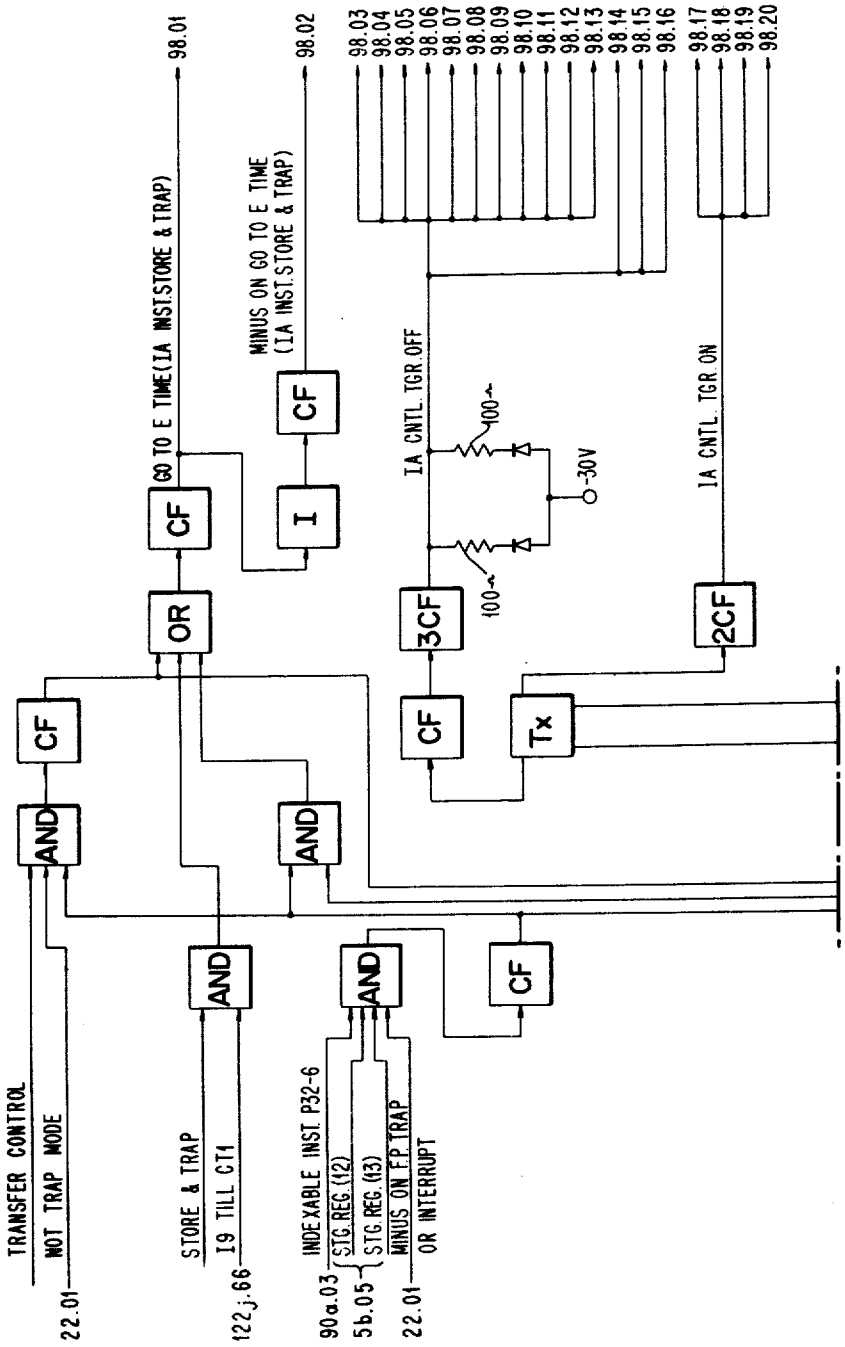


FIG. 98 INDIRECT ADDRESSING CONTROLS



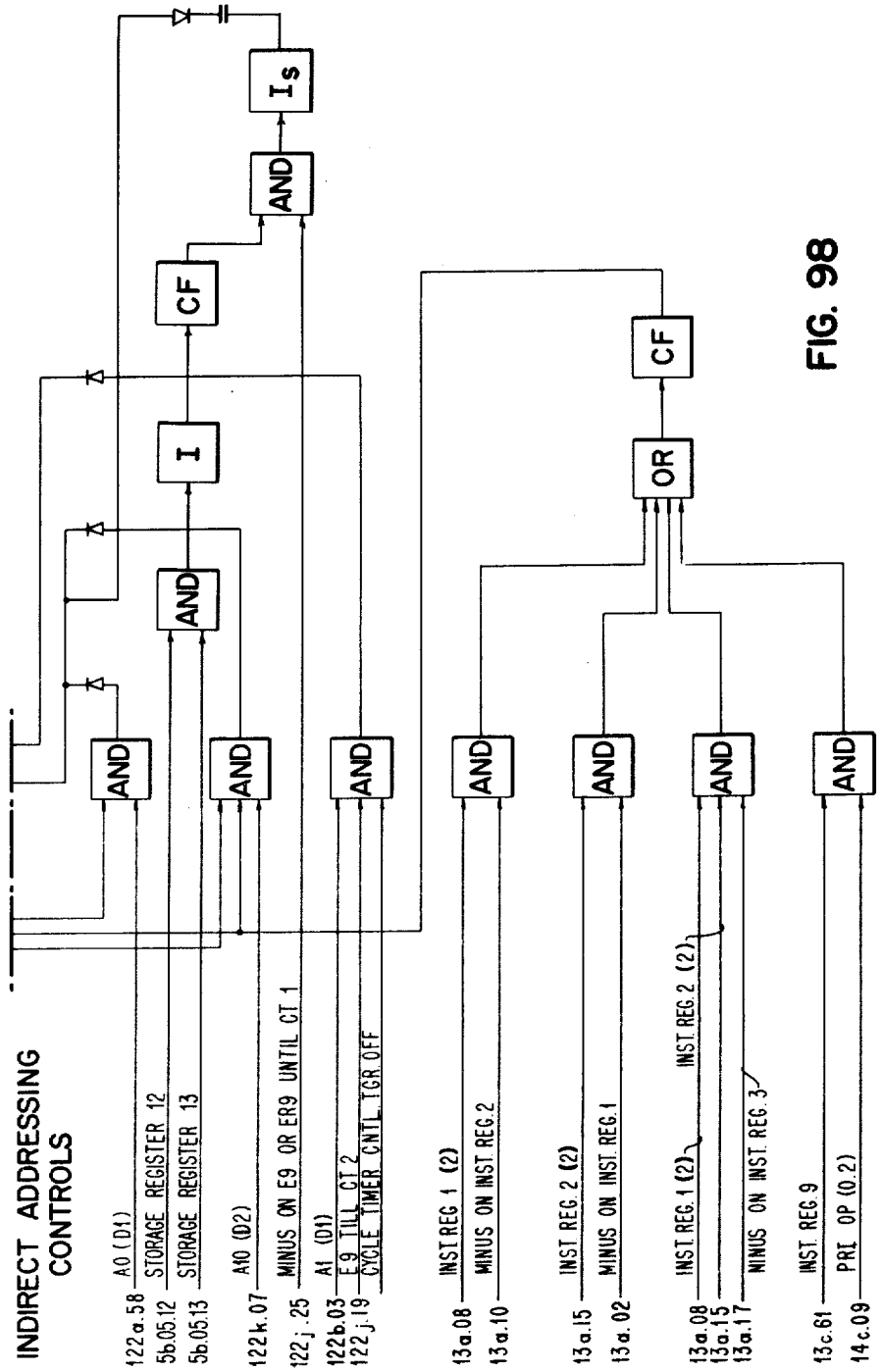

INDIRECT ADDRESSING CONTROLS
122a.58 A0 (D1)
5b.05.12 STORAGE REGISTER 12
5b.05.13 STORAGE REGISTER 13
122k.07 A10 (D2)
122j.25 MINUS ON E9 OR ER9 UNTIL CT 1
122b.03 A1 (D1)
122j.19 E9 TILL CT 2
CYCLE TIMER CNTL TGR OFF
13a.08 INST REG 1 (2)
13a.10 MINUS ON INST REG 2
13a.15 INST REG 2 (2)
13a.02 MINUS ON INST REG 1
13a.08 INST REG 1 (2)
13a.15 INST REG 2 (2)
13a.17 MINUS ON INST REG 3
13c.61 INST REG 9
14c.09 PRI OP (0.2)
AND
I
CF
Is
OR

FIG. 98

INSTRUCTION REGISTER PULSE GENERATOR

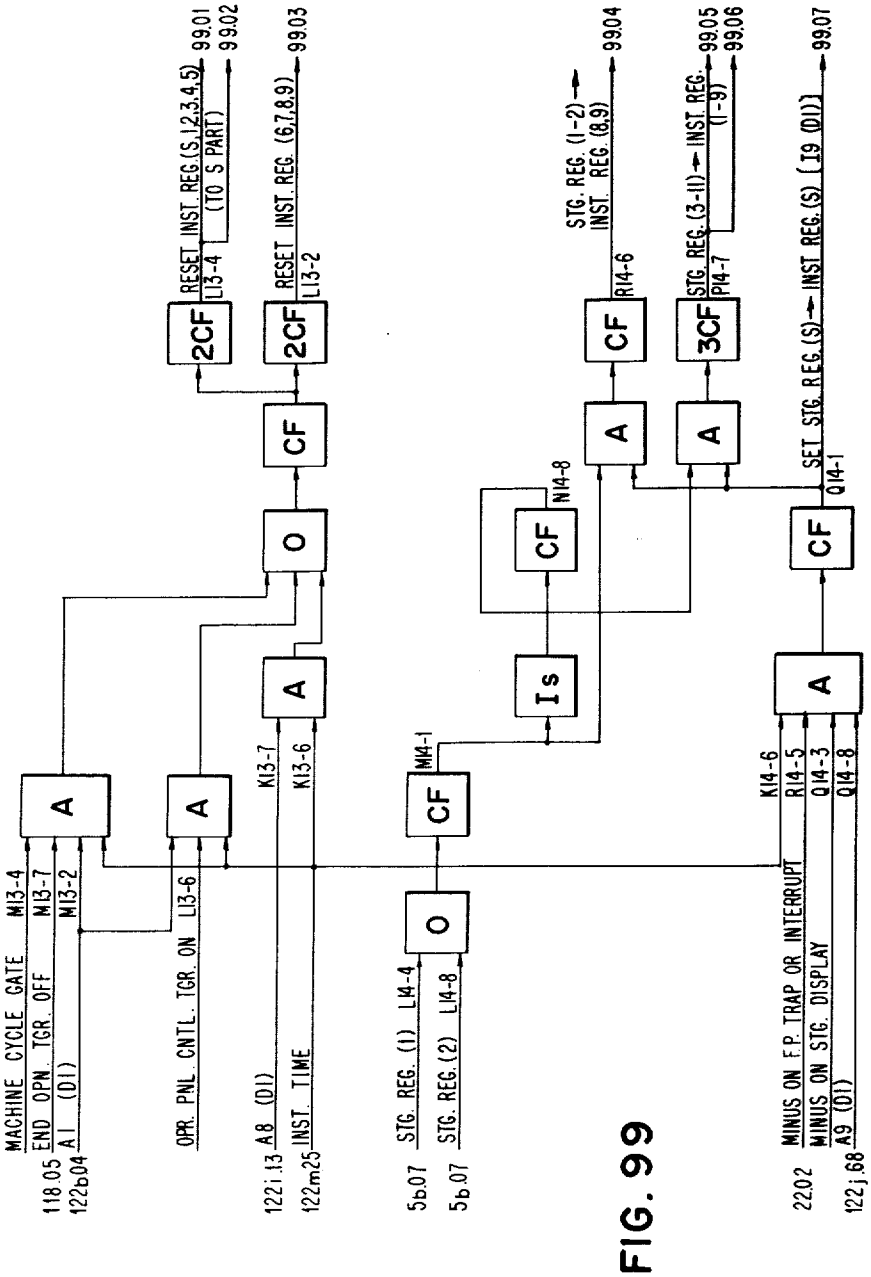


FIG. 99

INSTRUCTION REGISTER SIGN PLUS & MINUS

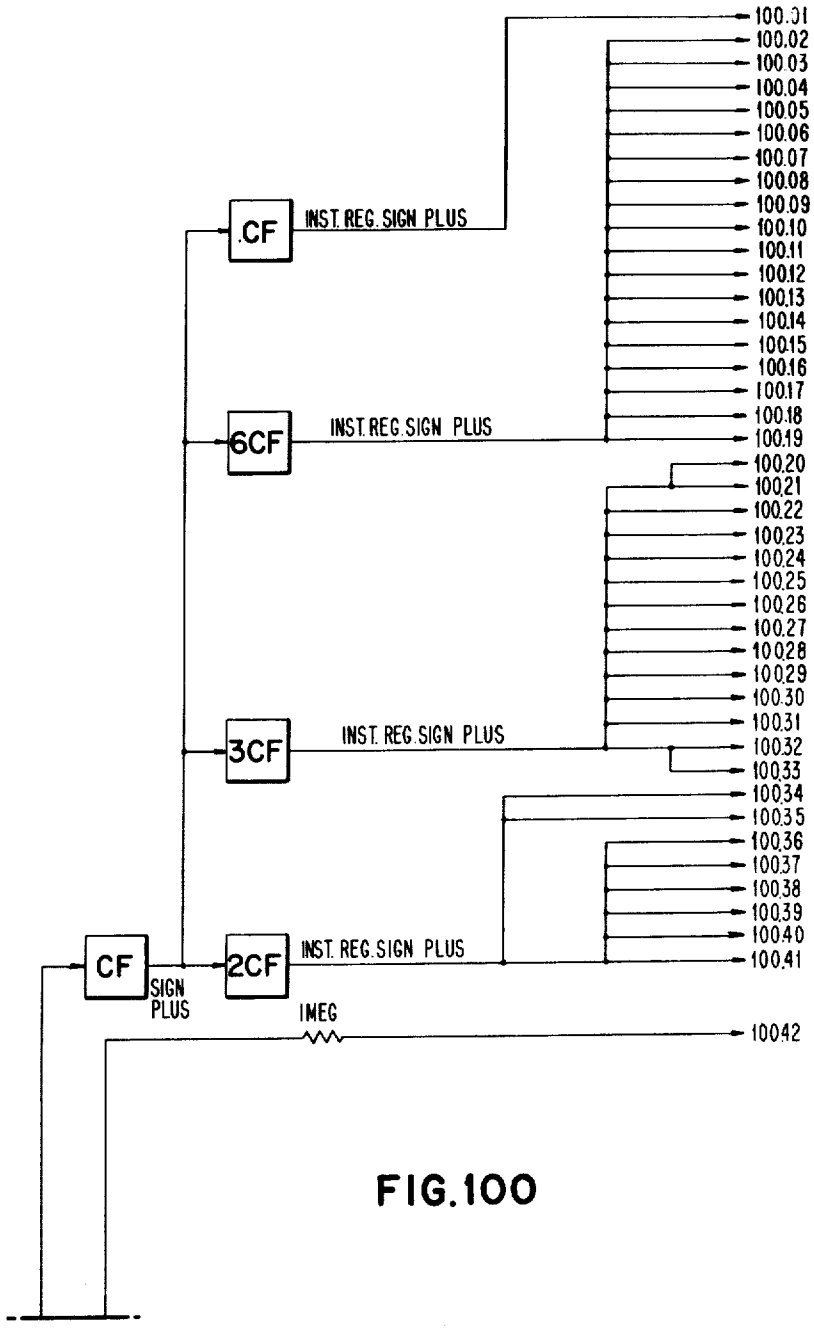


FIG. 100

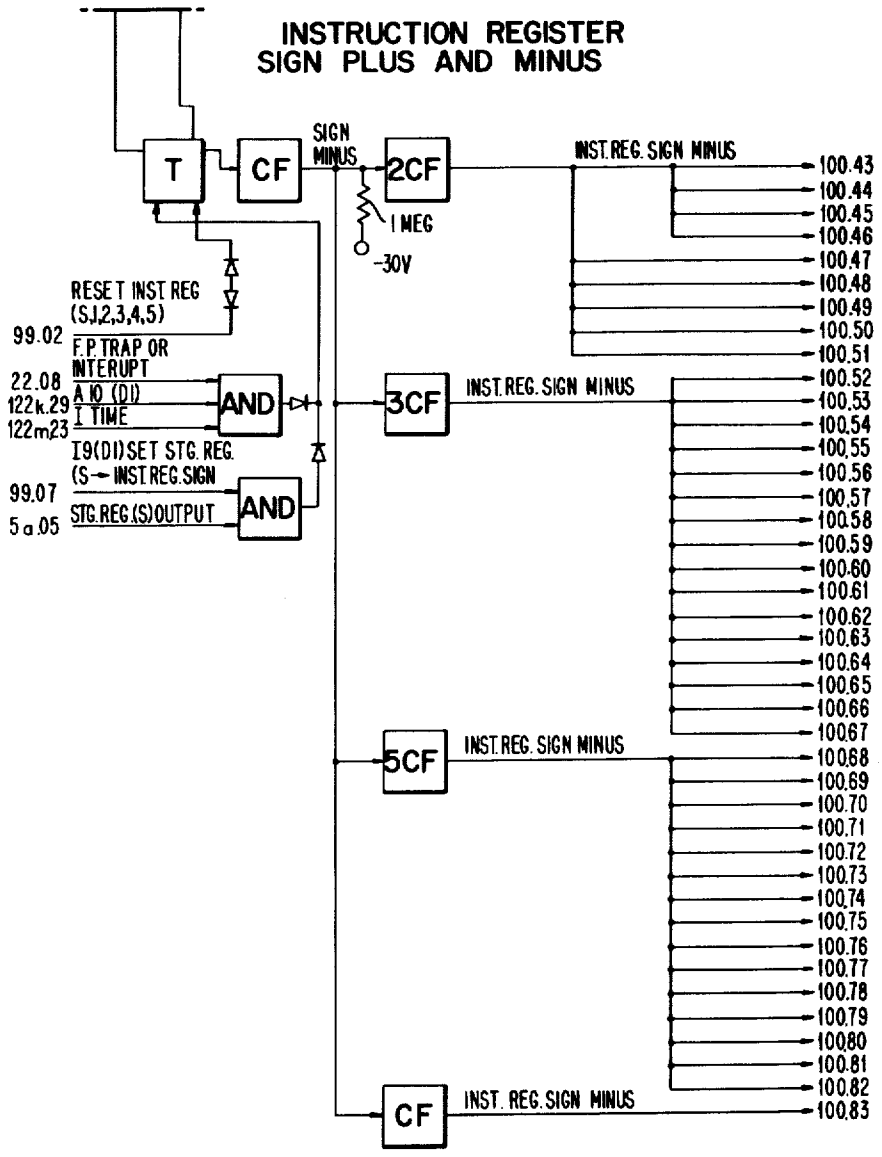

INSTRUCTION REGISTER
SIGN PLUS AND MINUS
T
CF
SIGN MINUS
2CF
1 MEG
-30V
INST. REG. SIGN MINUS
100.43
100.44
100.45
100.46
100.47
100.48
100.49
100.50
100.51
RESET INST REG (S,1,2,3,4,5)
99.02
F.P. TRAP OR INTERUPT
22.08
A 10 (DI)
122k.29
1 TIME
122m23
AND
3CF
INST. REG. SIGN MINUS
100.52
100.53
100.54
100.55
100.56
100.57
100.58
100.59
100.60
100.61
100.62
100.63
100.64
100.65
100.66
100.67
I9(DI) SET STG. REG. (S ← INST. REG. SIGN
99.07
STG. REG. (S) OUTPUT
5a.05
AND
5CF
INST. REG. SIGN MINUS
100.68
100.69
100.70
100.71
100.72
100.73
100.74
100.75
100.76
100.77
100.78
100.79
100.80
100.81
100.82
CF
INST. REG. SIGN MINUS
100.83

FIG. 100

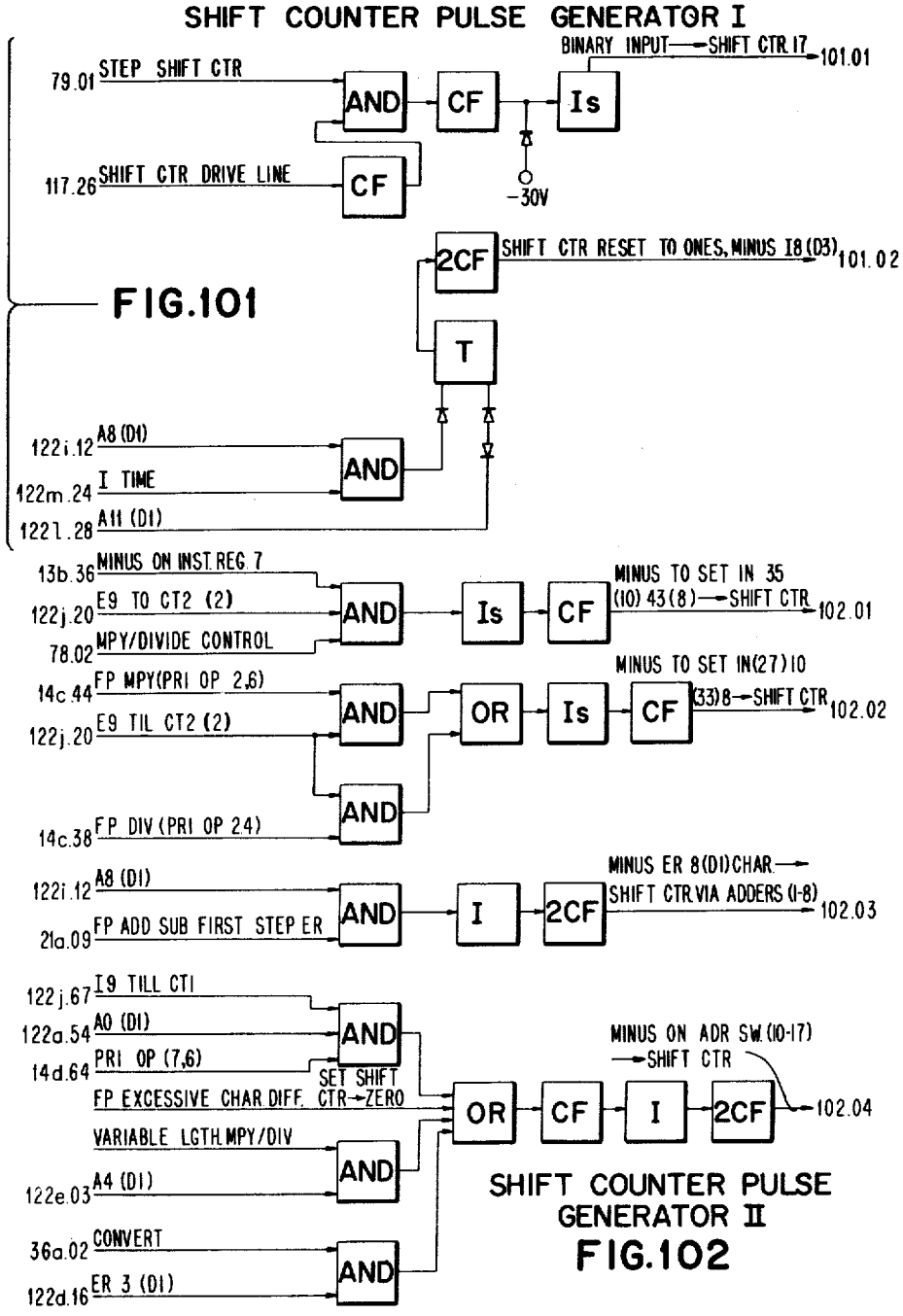


FIG.101

SHIFT COUNTER PULSE GENERATOR II

FIG.102

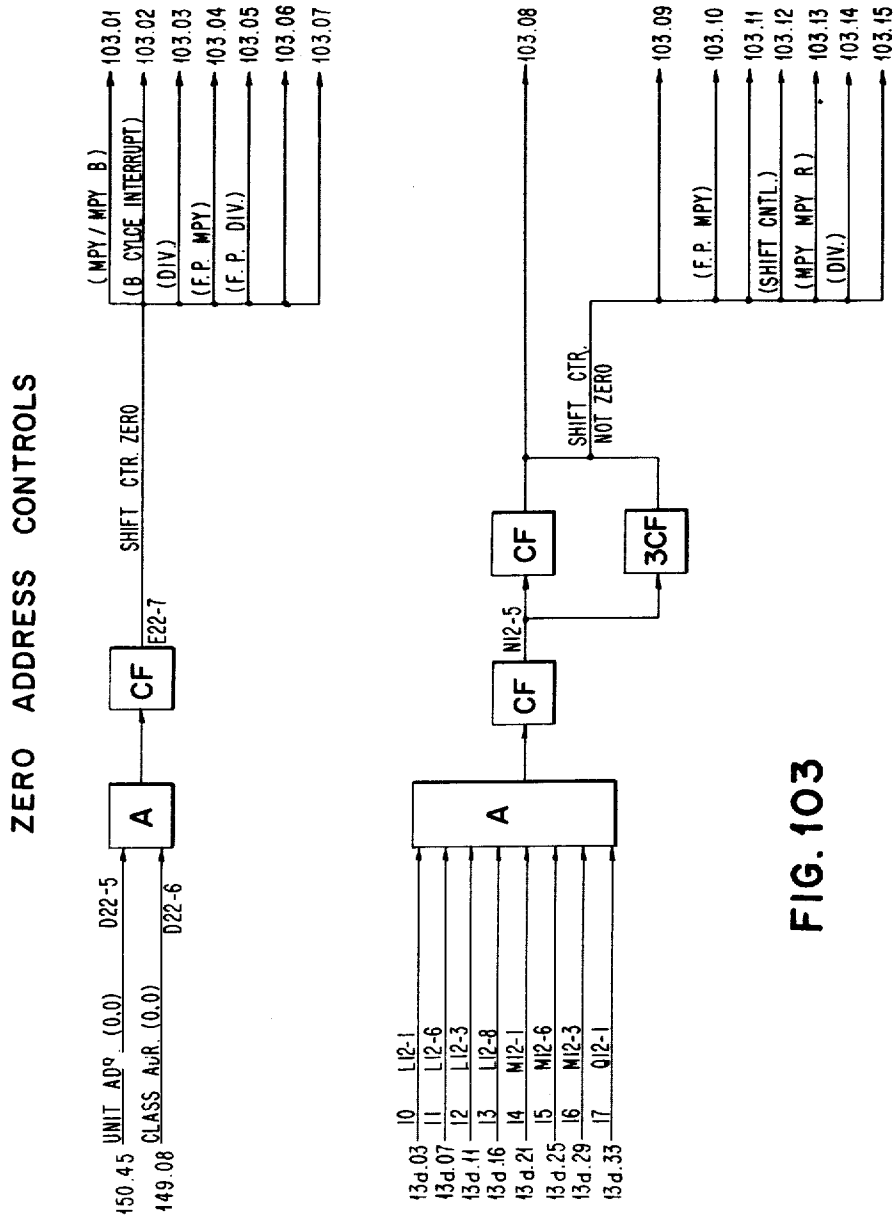

ZERO ADDRESS CONTROLS
150.45 UNIT AD9 (0,0)
149.08 CLASS A,R. (0,0)
D22-5
D22-6
A
CF
F22-7
SHIFT CTR. ZERO
103.01 (MPY / MPY B)
103.02 (B CYLCE INTERRUPT)
103.03 (DIV.)
103.04 (F.P. MPY)
103.05 (F.P. DIV.)
103.06
103.07
13d.03 10 L12-1
13d.07 11 L12-6
13d.11 12 L12-3
13d.16 13 L12-8
13d.21 14 M12-1
13d.25 15 M12-6
13d.29 16 M12-3
13d.33 17 Q12-1
A
CF
N12-5
CF
3CF
SHIFT CTR. NOT ZERO
103.08
103.09 (F.P. MPY)
103.10
103.11 (SHIFT CNTL.)
103.12 (MPY MPY R)
103.13 (DIV.)
103.14
103.15

FIG. 103

F.P. ENTRY TO SHIFT CTR. (10-17)

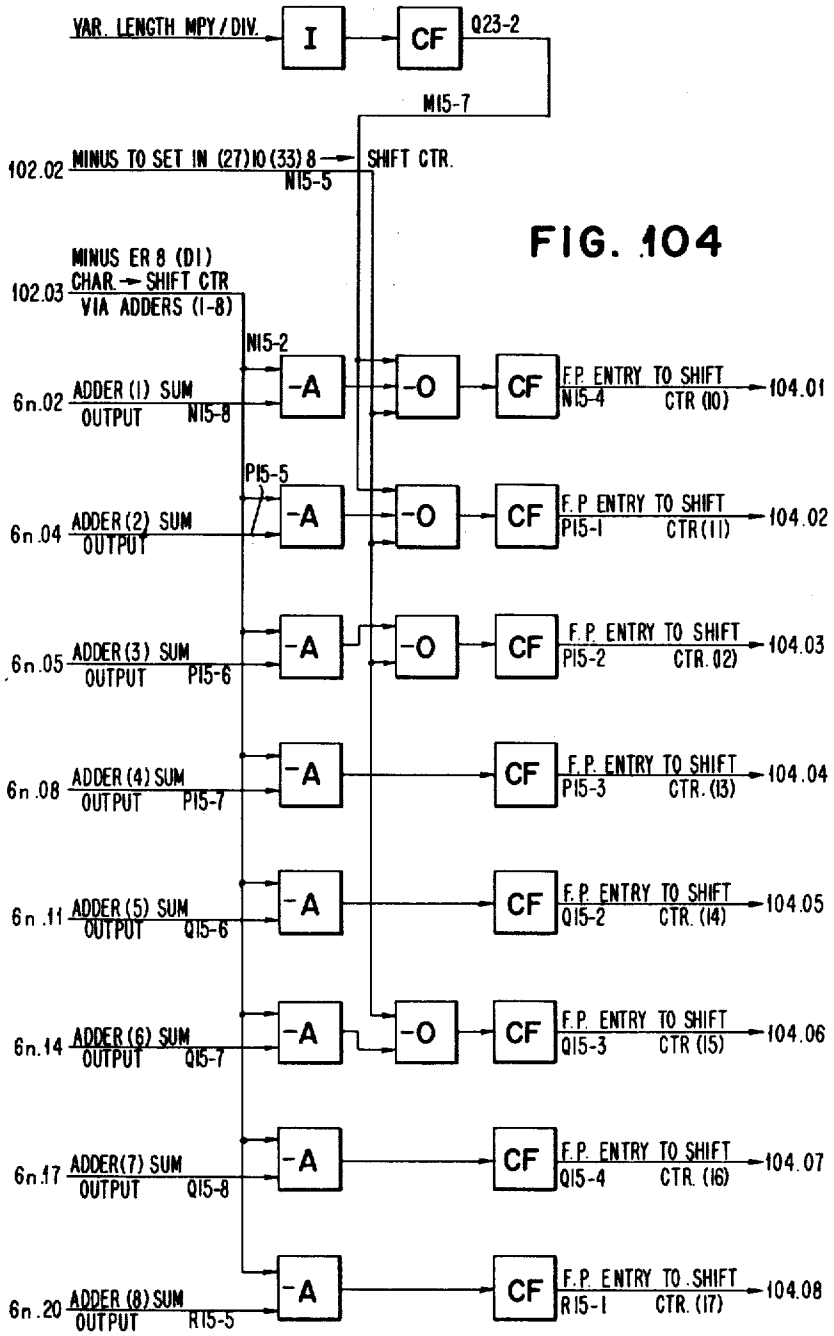


FIG. 104

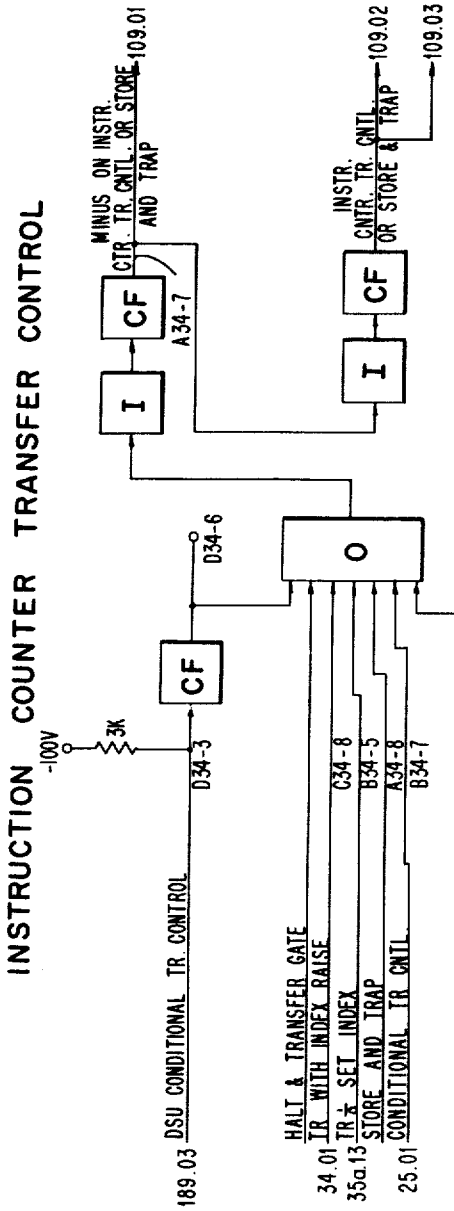


FIG. 109

FIG. 105

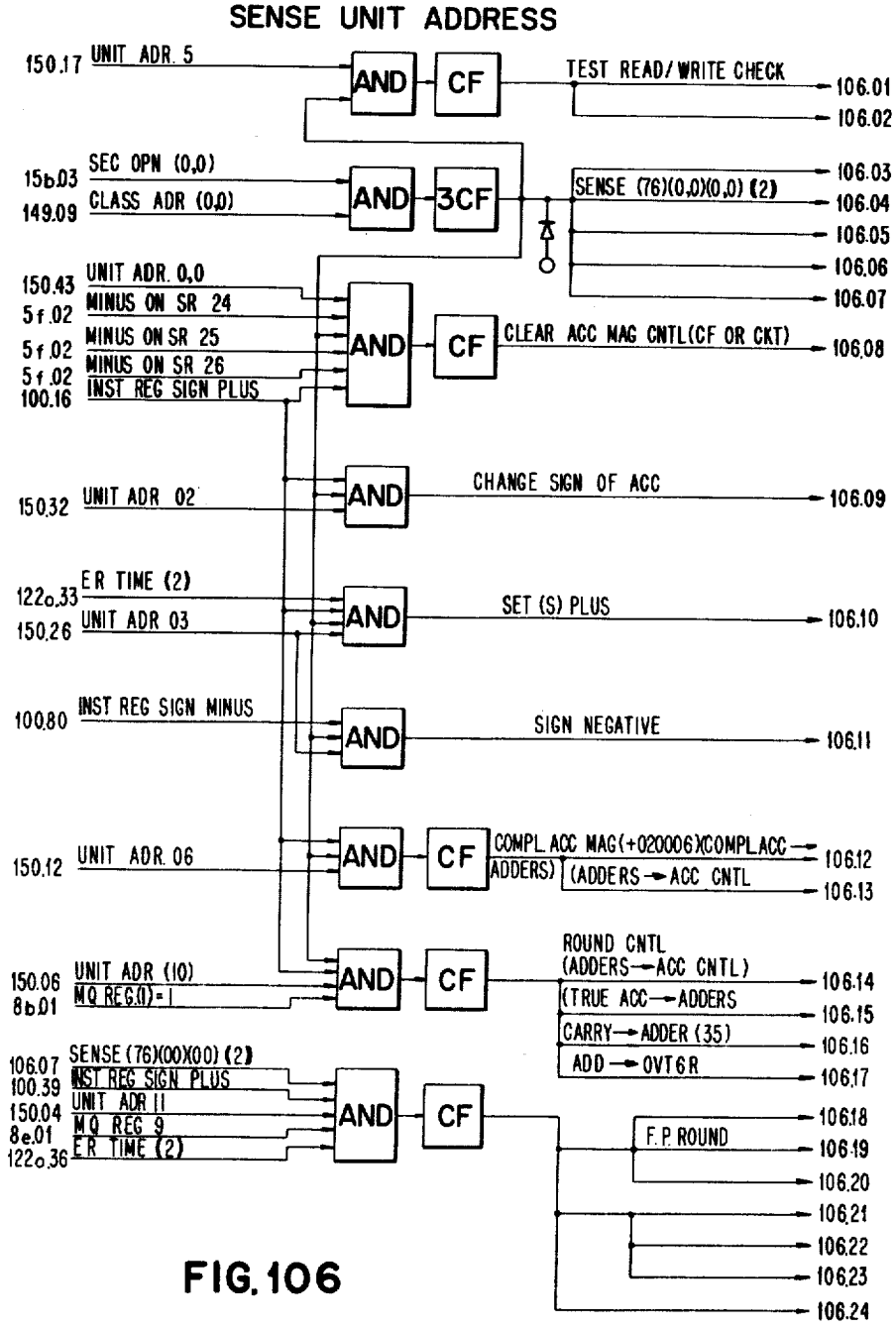
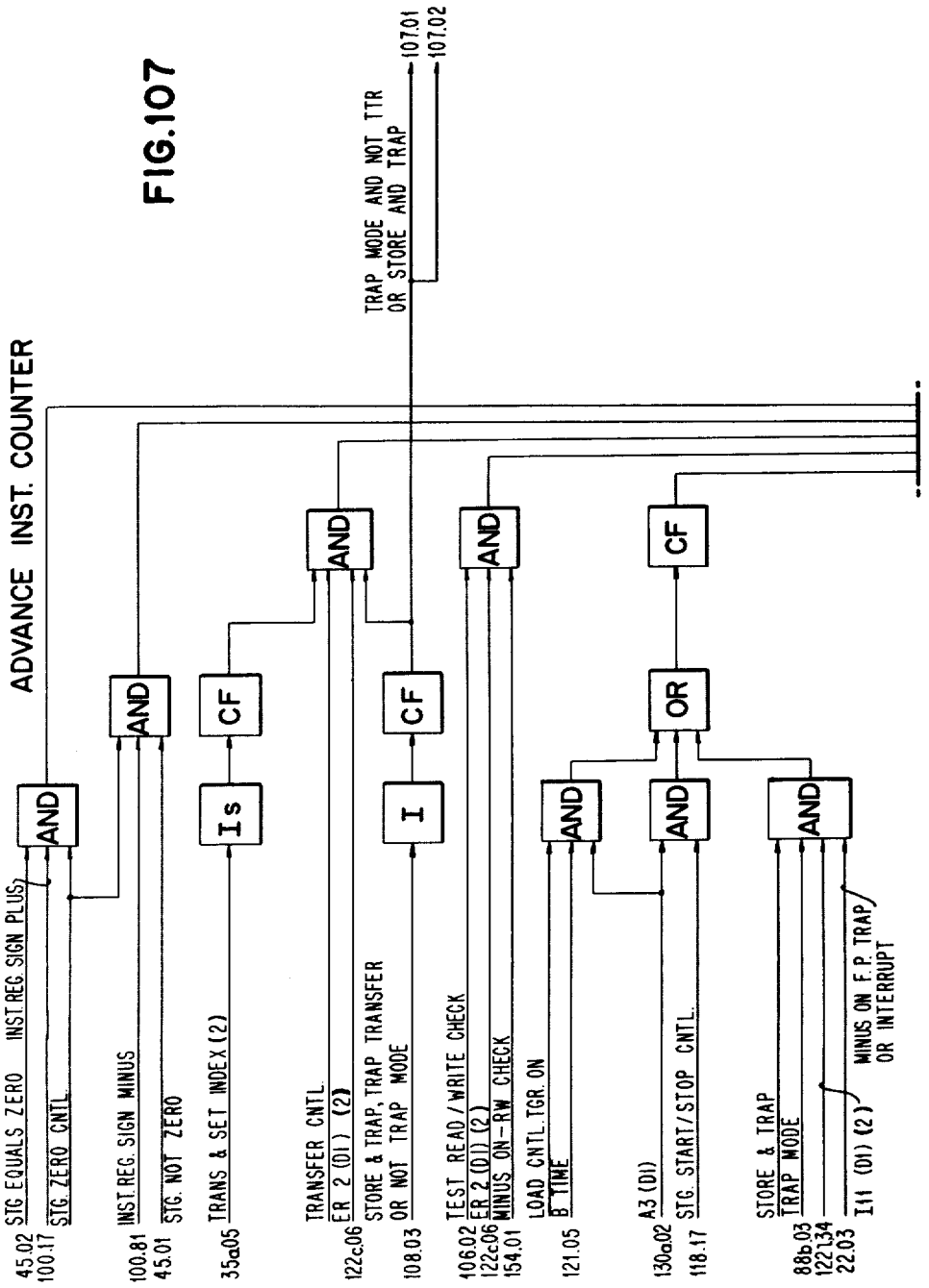

SENSE UNIT ADDRESS
150.17 UNIT ADR. 5
AND
CF
TEST READ/WRITE CHECK
106.01
106.02
15b.03 SEC OPN (0,0)
149.09 CLASS ADR (0,0)
AND
3CF
SENSE (76)(0,0)(0,0) (2)
106.03
106.04
106.05
106.06
106.07
150.43 UNIT ADR. 0,0
5f.02 MINUS ON SR 24
5f.02 MINUS ON SR 25
5f.02 MINUS ON SR 26
100.16 INST REG SIGN PLUS
AND
CF
CLEAR ACC MAG CNTL(CF OR CKT)
106.08
150.32 UNIT ADR 02
AND
CHANGE SIGN OF ACC
106.09
122o.33 ER TIME (2)
150.26 UNIT ADR 03
AND
SET (S) PLUS
106.10
100.80 INST REG SIGN MINUS
AND
SIGN NEGATIVE
106.11
150.12 UNIT ADR 06
AND
CF
COMPL ACC MAG(+020006)COMPL ACC
ADDERS)
(ADDERS→ACC CNTL
106.12
106.13
150.06 UNIT ADR (10)
8b.01 MQ REG(1)=1
AND
CF
ROUND CNTL
(ADDERS→ACC CNTL)
(TRUE ACC→ADDERS
CARRY→ADDER (35)
ADD→OVT6R
106.14
106.15
106.16
106.17
106.07 SENSE (76)(00)(00) (2)
100.39 INST REG SIGN PLUS
150.04 UNIT ADR 11
8e.01 MQ REG 9
122o.36 ER TIME (2)
AND
CF
F.P. ROUND
106.18
106.19
106.20
106.21
106.22
106.23
106.24

FIG. 106

FIG.107


ADVANCE INST. COUNTER
AND
AND
AND
AND
AND
CF
CF
CF
OR
Is
I
TRAP MODE AND NOT TTR OR STORE AND TRAP
107.01
107.02
45.02 STG EQUALS ZERO INST.REG SIGN PLUS
100.17 STG ZERO CNTL
100.81 INST.REG. SIGN MINUS
45.01 STG. NOT ZERO
35a05 TRANS & SET INDEX (2)
TRANSFER CNTL
122c06 ER 2 (01) (2)
STORE & TRAP, TRAP TRANSFER
108.03 OR NOT TRAP MODE
106.02 TEST READ/WRITE CHECK
122c06 ER 2 (01) (2)
154.01 MINUS ON-RW CHECK
LOAD CNTL TGR. ON
121.05 B TIME
130a02 A3 (01)
118.17 STG. START/STOP CNTL.
STORE & TRAP
88b.03 TRAP MODE
122134
22.03 I11 (01) (2)
MINUS ON F.P. TRAP OR INTERRUPT

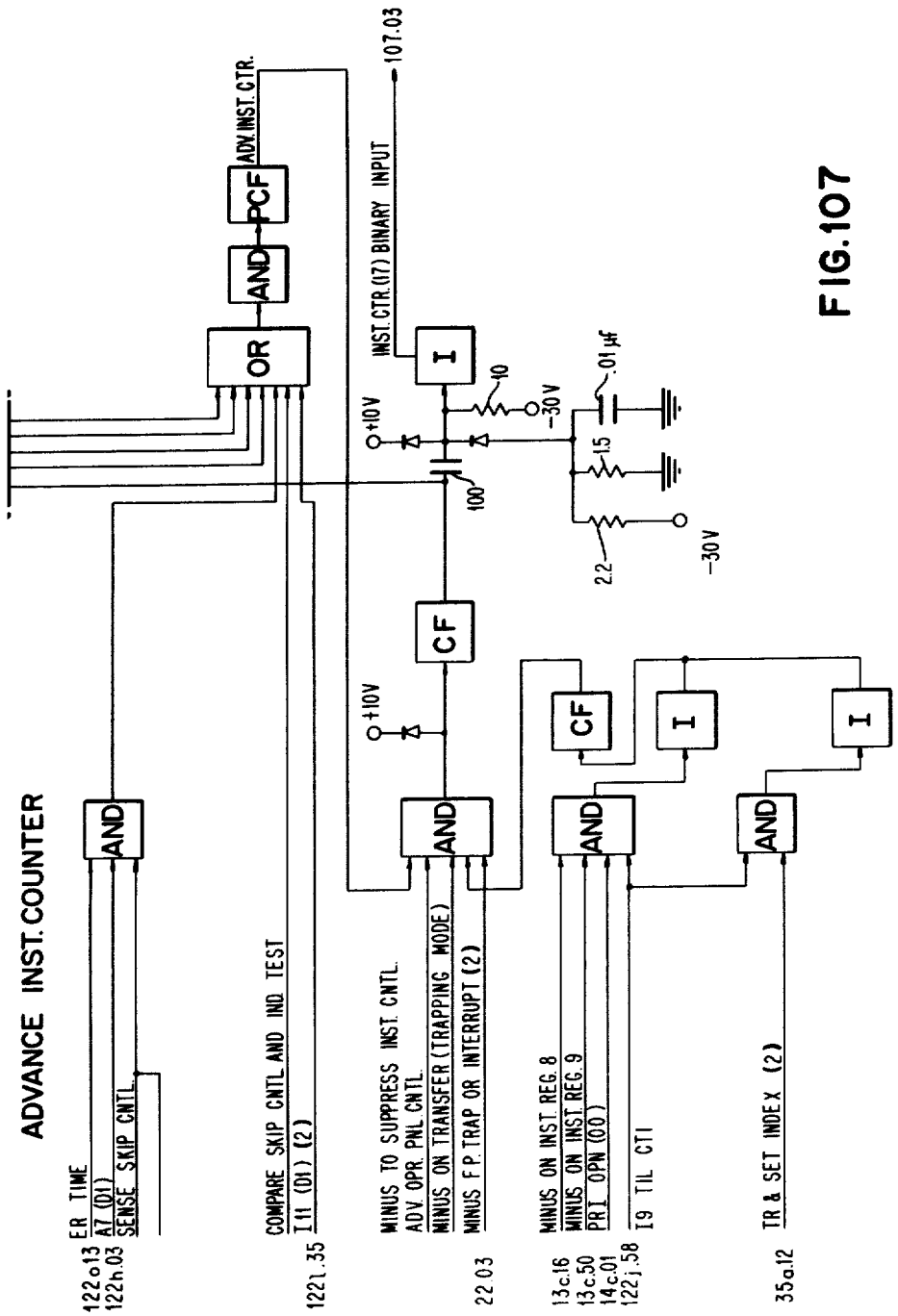

ADVANCE INST. COUNTER
ER TIME
AT (01)
SENSE SKIP CNTL.
122o.13
122h.03
AND
COMPARE SKIP CNTL AND IND TEST
I11 (01) (2)
1221.35
OR
AND
PCF
ADV. INST. CTR.
INST. CTR. (17) BINARY INPUT
107.03
I
+10V
10
-30V
.01 μf
1.5
2.2
-30V
100
CF
+10V
MINUS TO SUPPRESS INST. CNTL.
ADV. OPR. PNL. CNTL.
MINUS ON TRANSFER (TRAPPING MODE)
MINUS F.P. TRAP OR INTERRUPT (2)
AND
22.03
CF
I
MINUS ON INST. REG. 8
MINUS ON INST. REG. 9
PRI OPN (00)
I9 TIL CTI
13c.16
13c.50
14c.01
122j.58
AND
I
TR & SET INDEX (2)
35a.12

FIG. 107

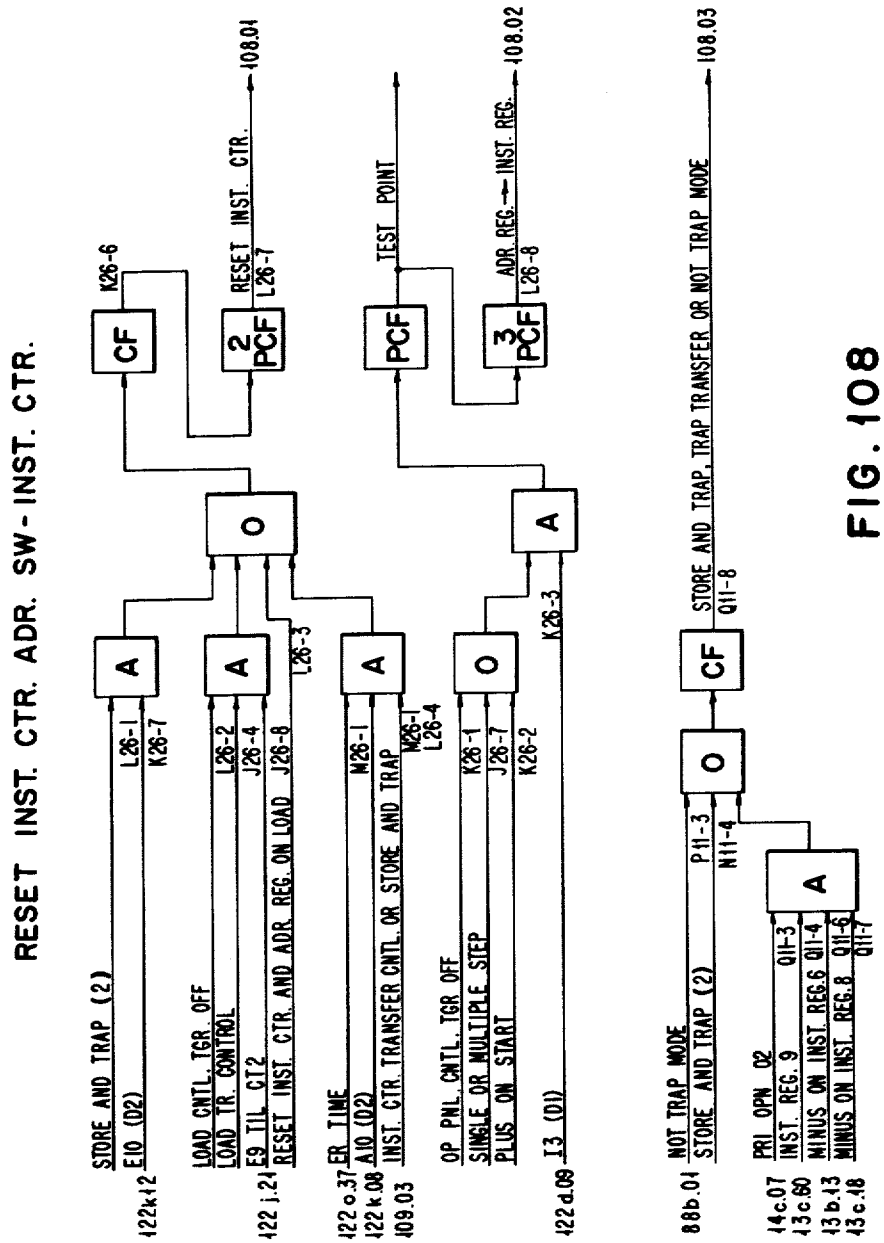

RESET INST. CTR. ADR. SW - INST. CTR.
STORE AND TRAP (2)
E10 (02)
122k.12
L26-1
K26-7
A
LOAD CNTL. TGR. OFF
LOAD TR. CONTROL
E9 TIL CT2
RESET INST. CTR. AND ADR REG. ON LOAD
122 j.21
L26-2
J26-4
J26-8
L26-3
A
ER TIME
A10 (02)
INST. CTR TRANSFER CNTL. OR STORE AND TRAP
122 o.37
122 k.08
409.03
M26-1
M26-1
L26-4
A
OP PNL. CNTL. TGR OFF
SINGLE OR MULTIPLE STEP
PLUS ON START
I3 (01)
122 a.09
K26-1
J26-7
K26-2
K26-3
O
CF
K26-6
2 PCF
RESET INST. CTR.
L26-7
108.01
PCF
TEST POINT
3 PCF
ADR. REG. → INST. REG.
L26-8
108.02
A
NOT TRAP MODE
STORE AND TRAP (2)
88b.01
P11-3
N11-4
O
CF
STORE AND TRAP, TRAP TRANSFER OR NOT TRAP MODE
Q11-8
108.03
A
PRI OPN 02
INST. REG. 9
MINUS ON INST. REG. 6
MINUS ON INST. REG. 8
14c.07
13c.80
13b.13
13c.18
Q11-3
Q11-4
Q11-6
Q11-7

FIG. 108

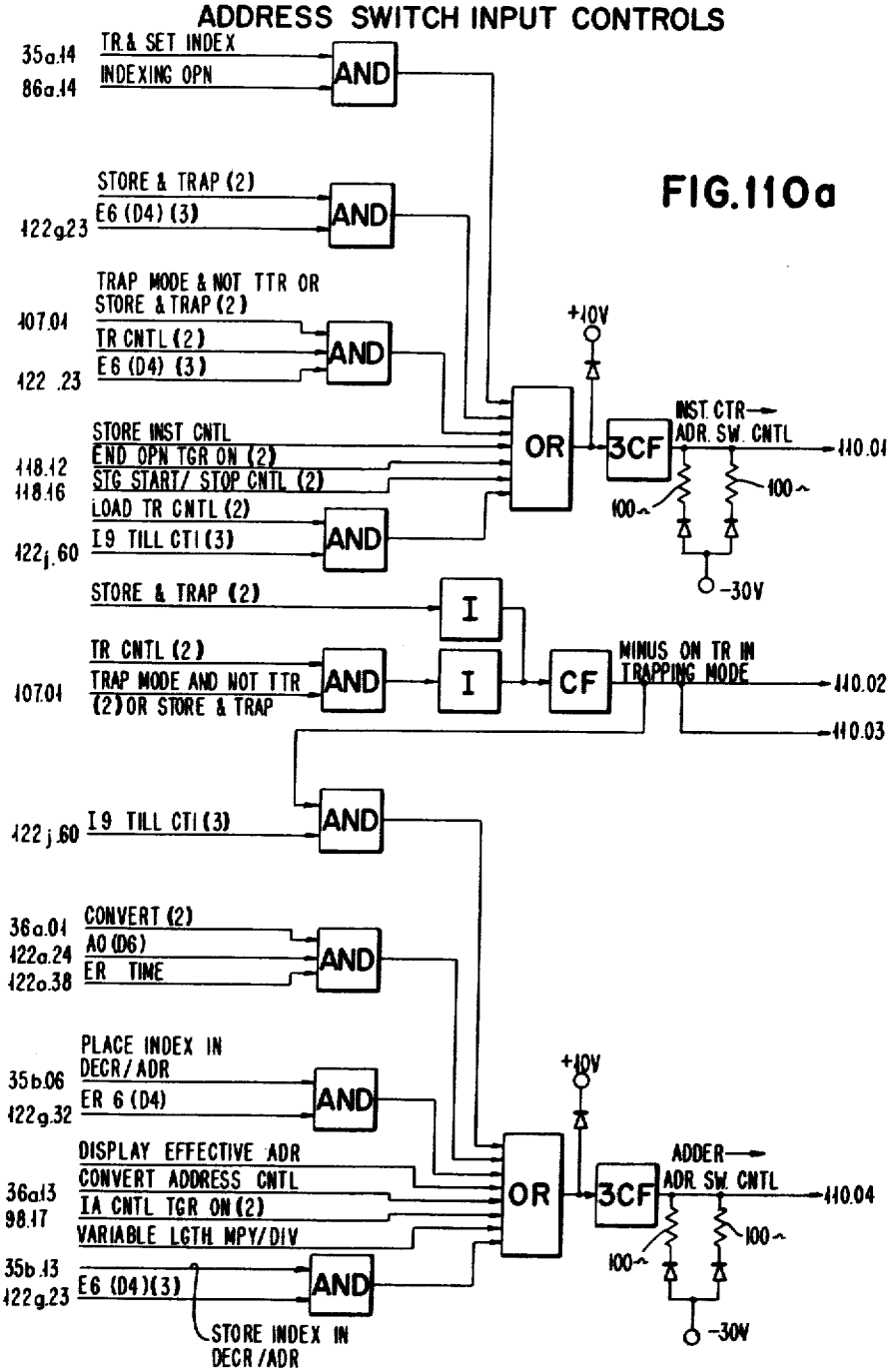

ADDRESS SWITCH INPUT CONTROLS
35a.14
86a.14
TR & SET INDEX
INDEXING OPN
AND
STORE & TRAP (2)
422g.23
E6 (D4) (3)
AND
TRAP MODE & NOT TTR OR STORE & TRAP (2)
107.04
TR CNTL (2)
422 .23
E6 (D4) (3)
AND
+10V
STORE INST CNTL
118.12
END OPN TGR ON (2)
118.16
STG START/ STOP CNTL (2)
OR
3CF
INST CTR ADR. SW. CNTL
110.01
100
100
LOAD TR CNTL (2)
422j.60
I9 TILL CTI (3)
AND
-30V
STORE & TRAP (2)
I
TR CNTL (2)
107.04
TRAP MODE AND NOT TTR (2) OR STORE & TRAP
AND
I
CF
MINUS ON TR IN TRAPPING MODE
110.02
110.03
422j.60
I9 TILL CTI (3)
AND
36a.04
422a.24
422a.38
CONVERT (2)
AO (D6)
ER TIME
AND
PLACE INDEX IN DECR/ADR
35b.06
422g.32
ER 6 (D4)
AND
+10V
DISPLAY EFFECTIVE ADR
CONVERT ADDRESS CNTL
36a.13
98.17
IA CNTL TGR ON (2)
VARIABLE LGTH MPY/DIV
OR
3CF
ADDER ADR SW CNTL
110.04
100
100
35b.13
422g.23
E6 (D4)(3)
AND
-30V
STORE INDEX IN DECR/ADR

FIG.110a

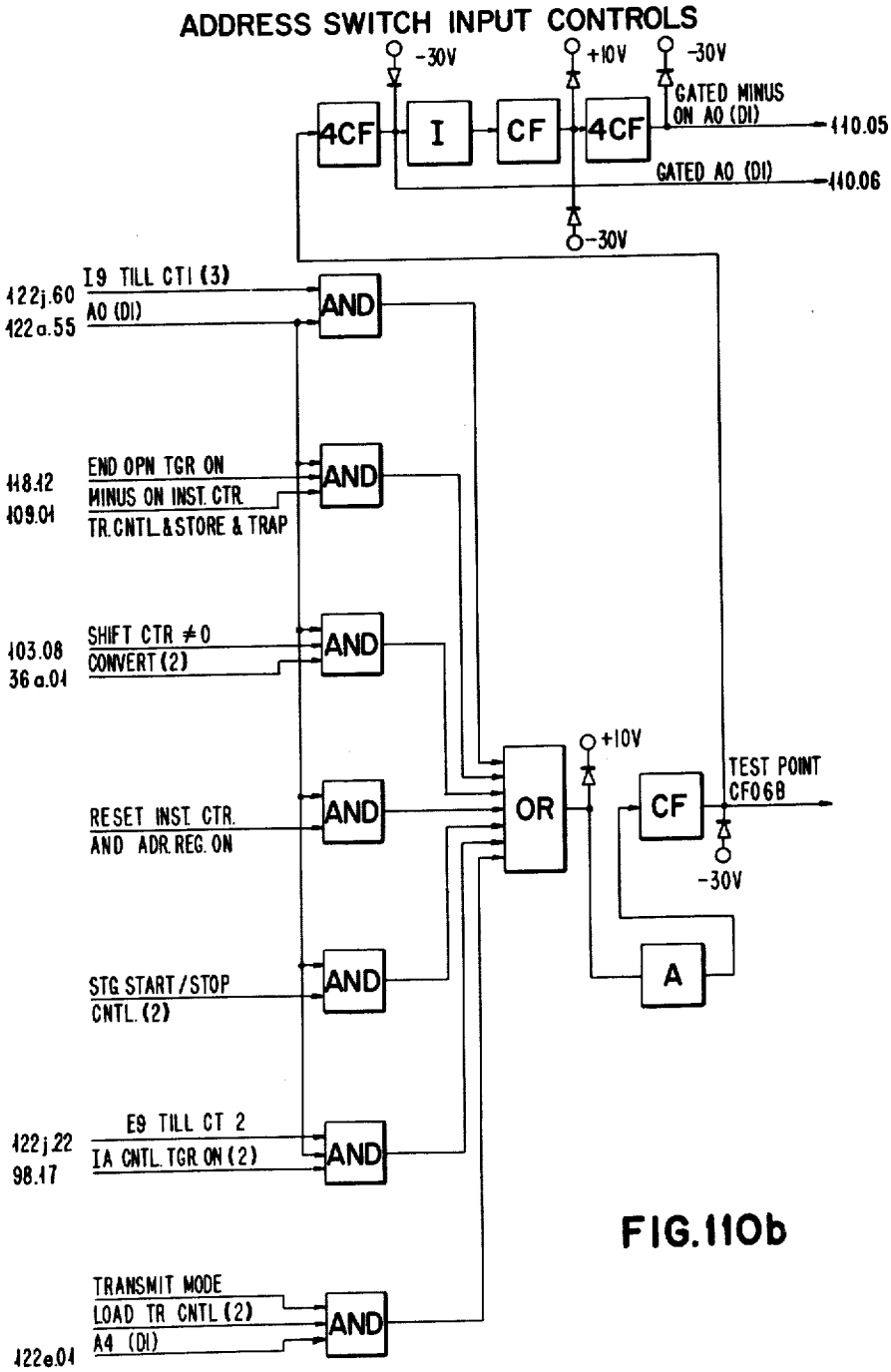

ADDRESS SWITCH INPUT CONTROLS
-30V
+10V
-30V
GATED MINUS ON A0 (DI)
4CF
I
CF
4CF
110.05
GATED A0 (DI)
110.06
-30V
I9 TILL CTI (3)
422j.60
A0 (DI)
422a.55
AND
END OPN TGR ON
118.12
MINUS ON INST. CTR.
109.04
TR. CNTL. & STORE & TRAP
AND
SHIFT CTR ≠ 0
103.08
CONVERT (2)
36a.04
AND
+10V
TEST POINT CF06B
RESET INST. CTR. AND ADR. REG. ON
AND
OR
CF
-30V
STG START/STOP CNTL. (2)
AND
A
E9 TILL CT 2
422j.22
IA CNTL. TGR ON (2)
98.17
AND
TRANSMIT MODE
LOAD TR CNTL (2)
A4 (DI)
422e.04
AND

FIG. 110b

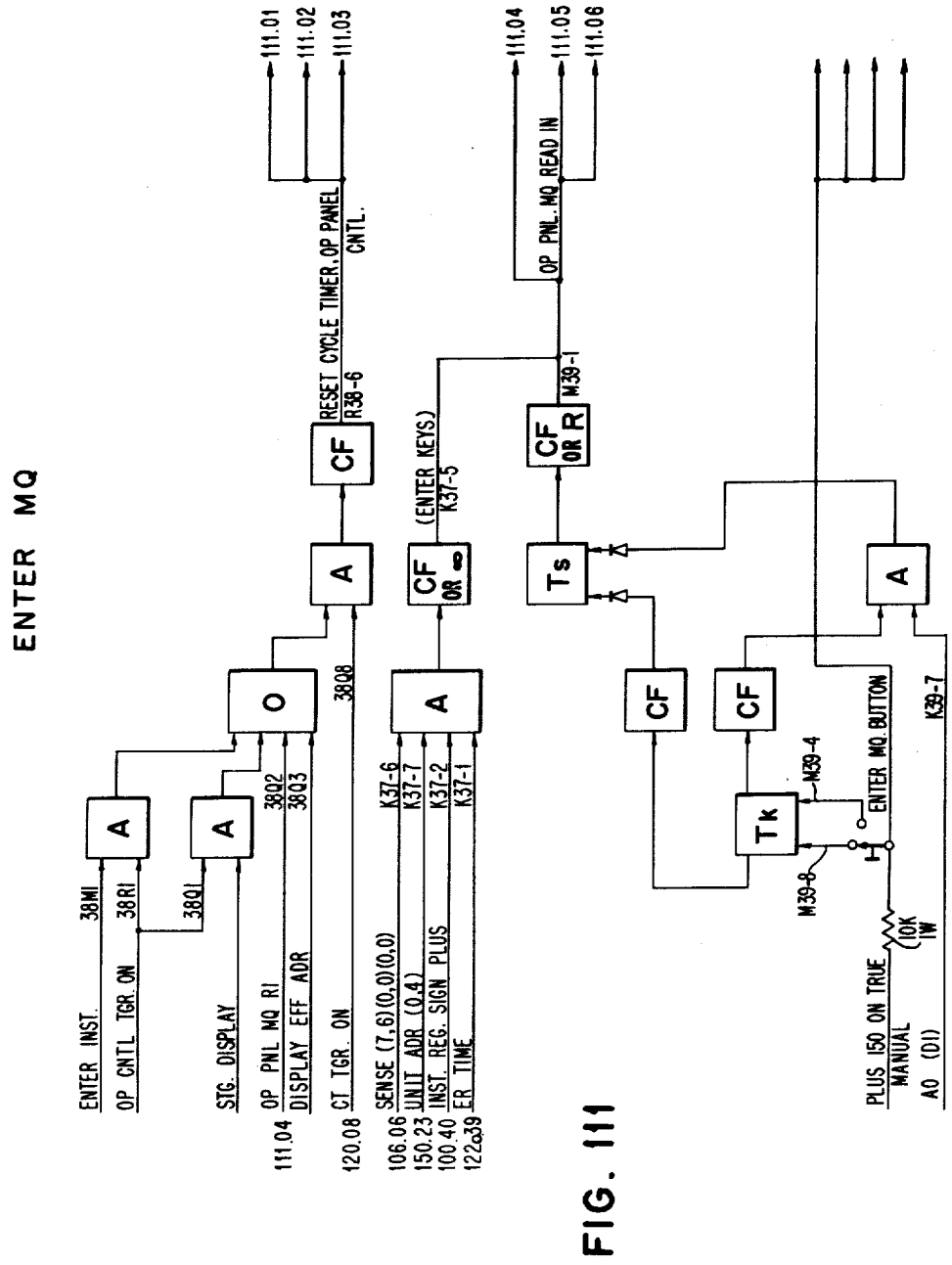
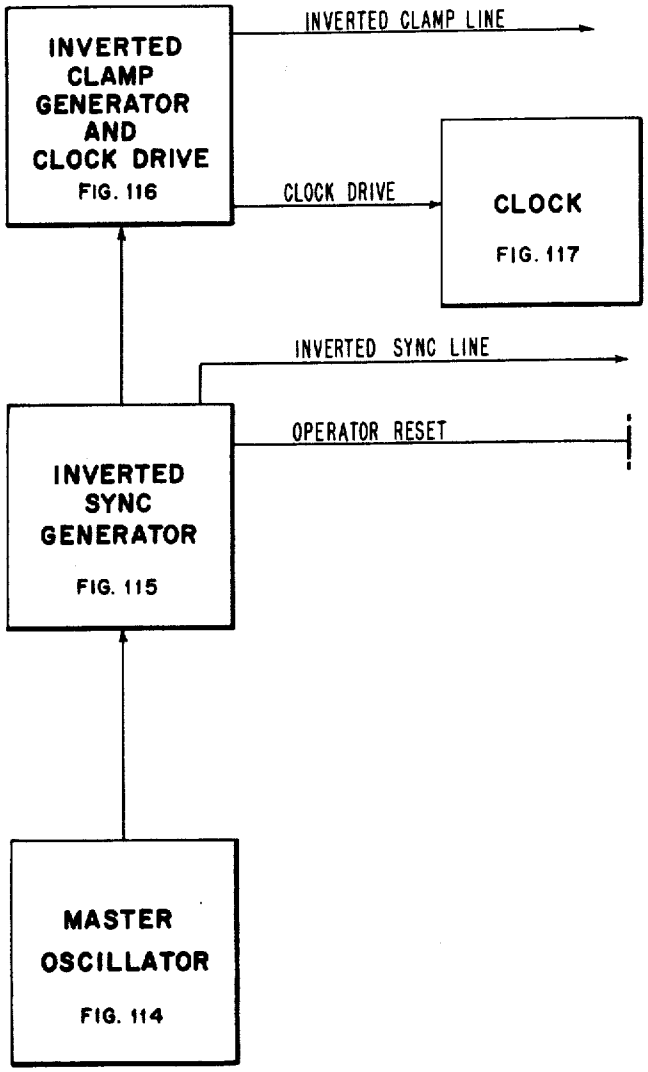

ENTER MQ
ENTER INST. 38MI
OP CNTL TGR ON 38RI
STG. DISPLAY 38QI
111.04 OP PNL MQ RI 3802
DISPLAY EFF ADR 3803
120.08 CI TGR ON 3808
106.06 SENSE (7,6)(0,0)(0,0) K37-6
150.23 UNIT ADR (0,4) K37-7
100.40 INST. REG. SIGN PLUS K37-2
122a39 ER TIME K37-1
A
A
O
A
CF
RESET CYCLE TIMER, OP PANEL CNTL.
R38-6
111.01
111.02
111.03
CF
OR ∞
(ENTER KEYS)
K37-5
Ts
CF
OR R
M39-1
OP PNL. MQ READ IN
111.04
111.05
111.06
CF
CF
Tk
M39-4
M39-8
ENTER MQ BUTTON
A
K39-7
PLUS 150 ON TRUE
MANUAL
A0 (01)
10K
1W

FIG. 111

FIG. 112

PRIMARY DRIVE CIRCUITS



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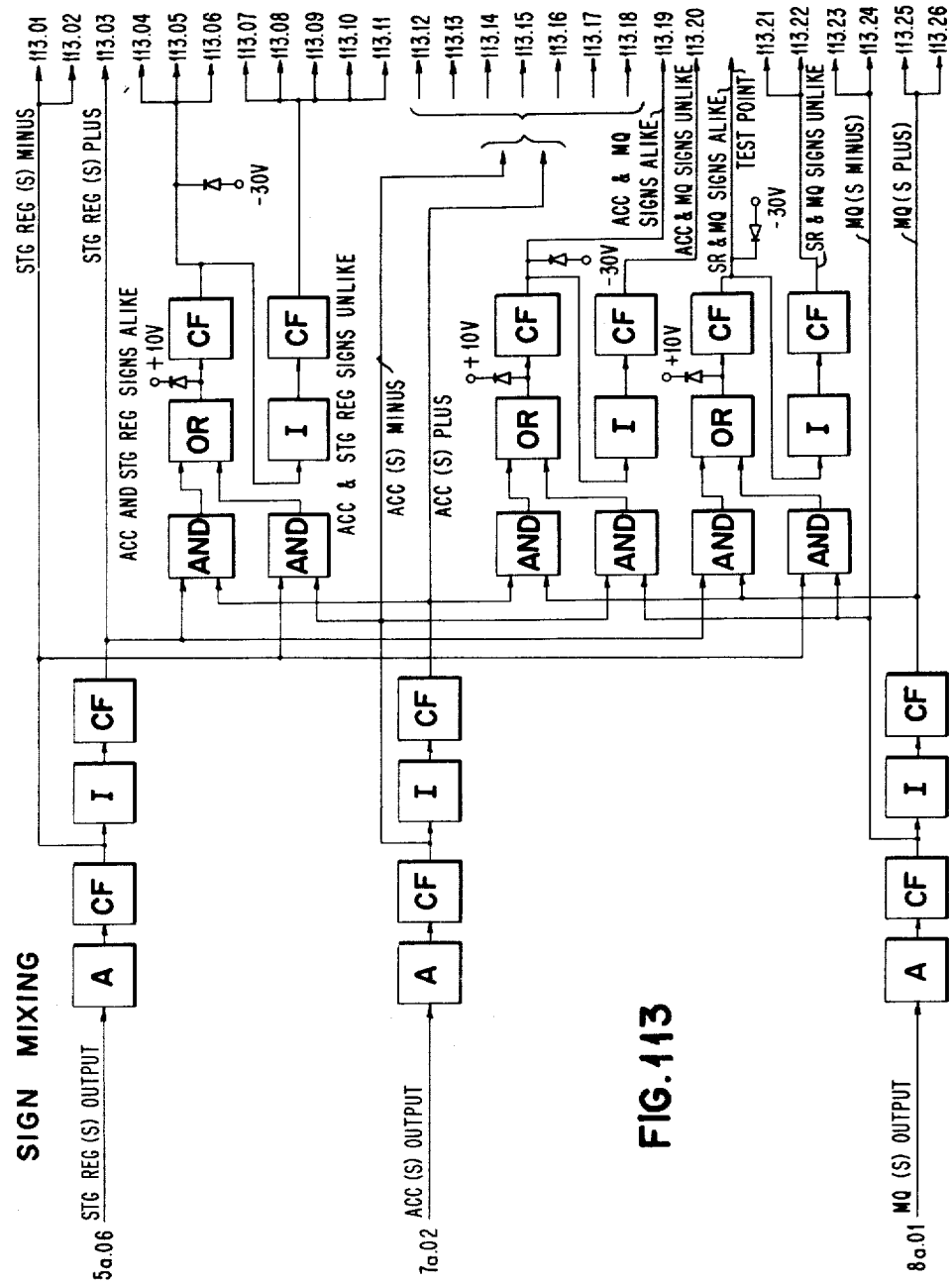
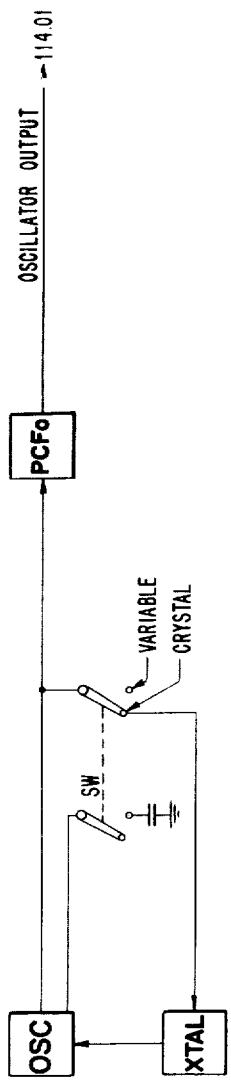


FIG. 113

FIG. 114



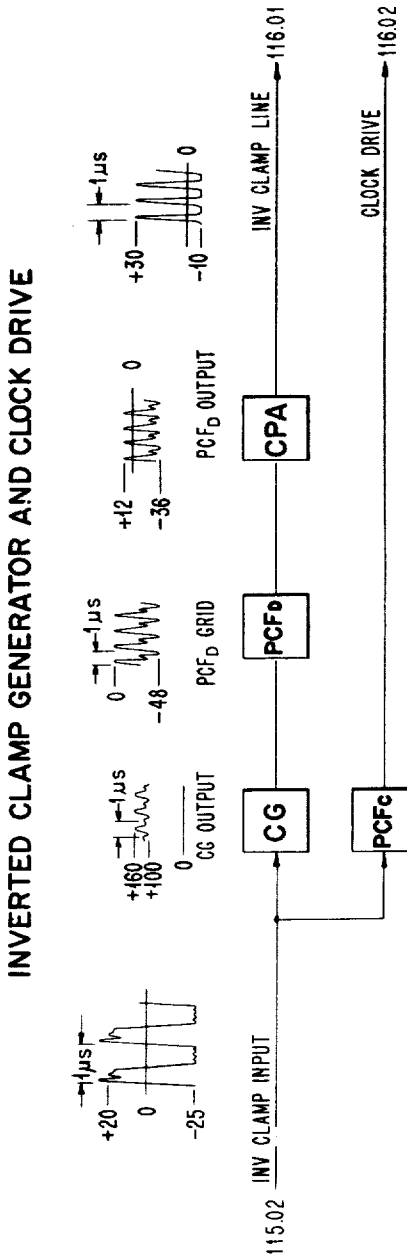


FIG. 116

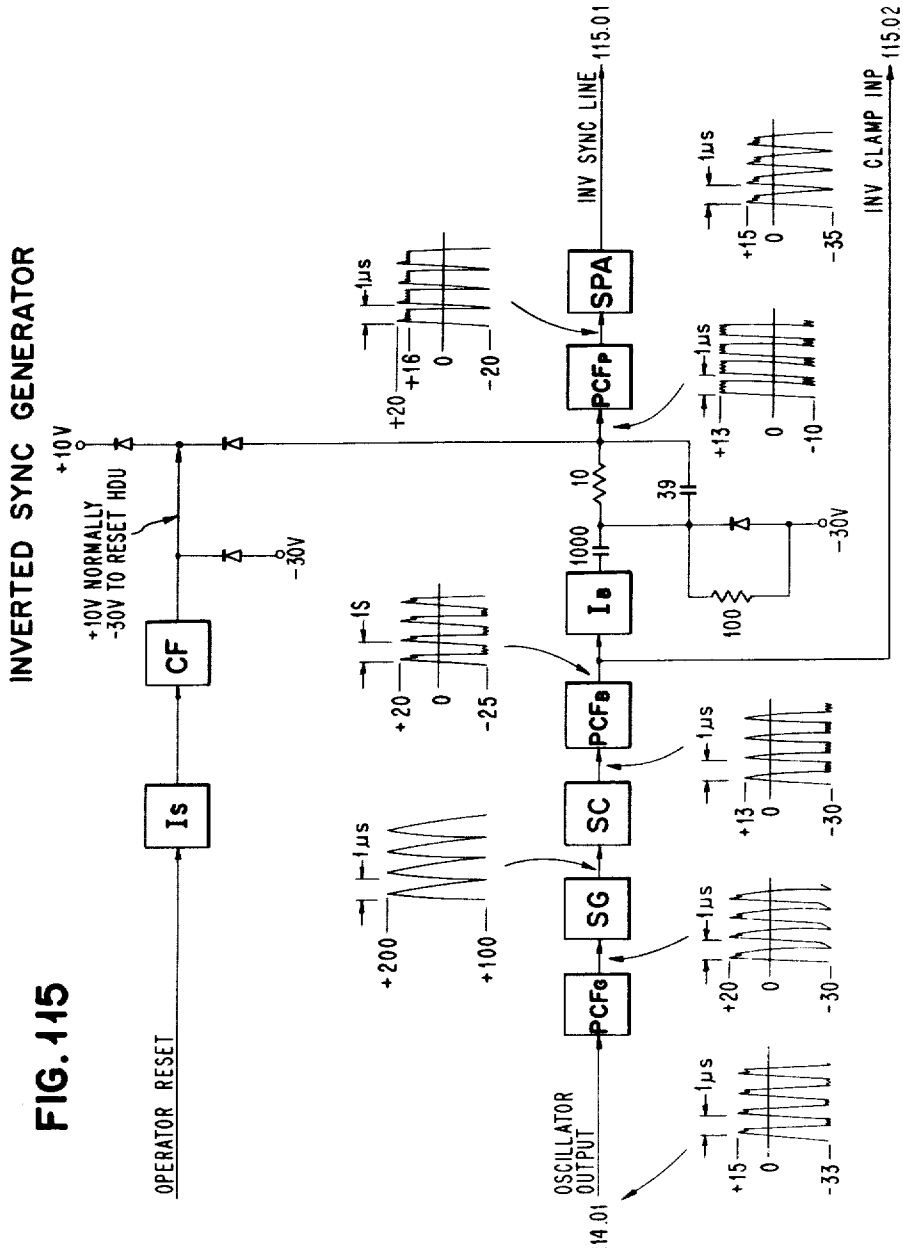

INVERTED SYNC GENERATOR
OPERATOR RESET
Is
CF
+10V NORMALLY
-30V TO RESET HDU
+10V
-30V
SPA
PCFP
PCFB
SC
SG
PCFG
IB
10
1000
39
100
-30V
INV SYNC LINE 115.01
INV CLAMP INP 115.02
OSCILLATOR OUTPUT
114.01
1μs
1S
+20
+16
0
-20
+15
-35
+13
-10
-25
+200
+100
-30
-33

FIG. 115

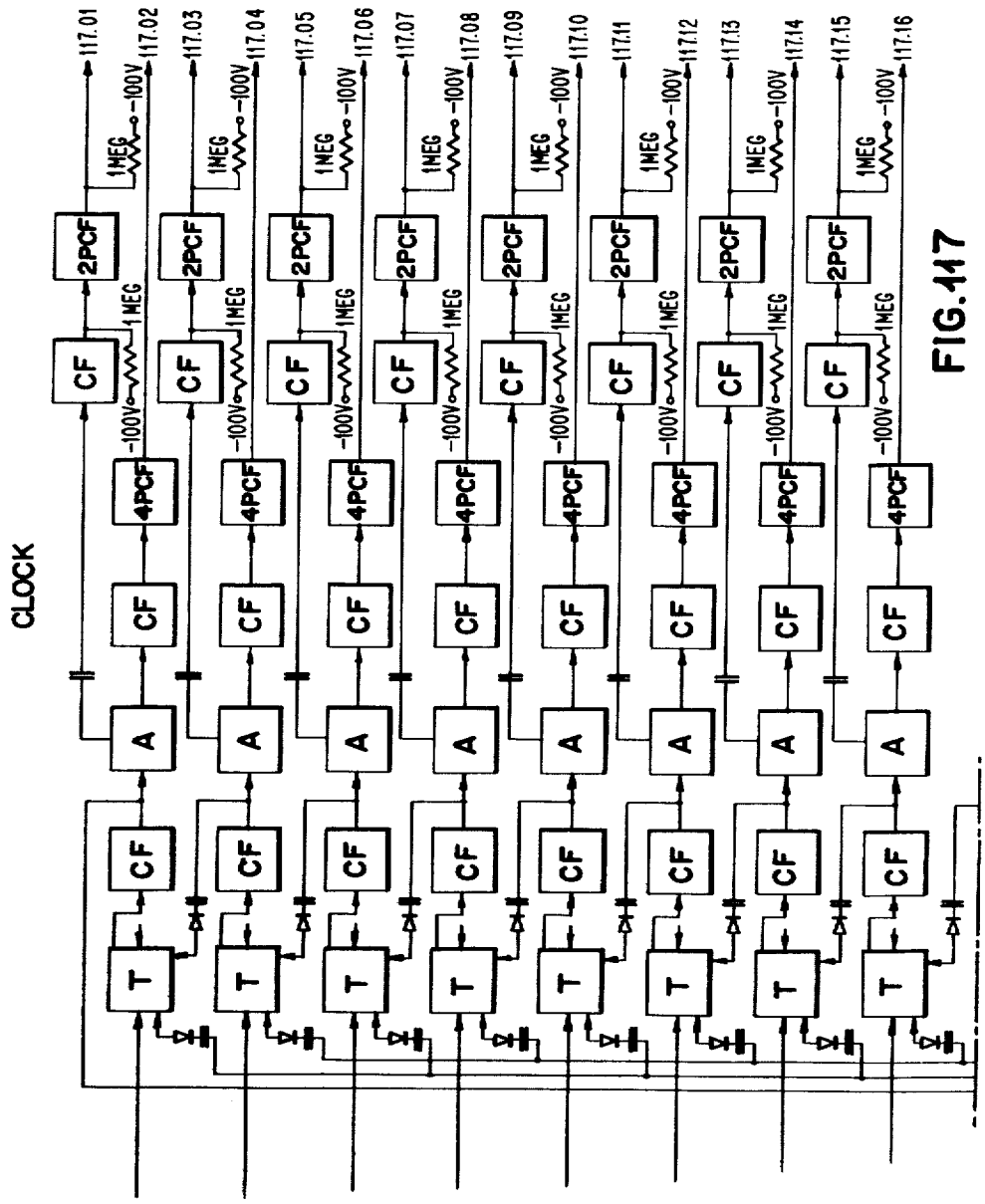

CLOCK
117.01
117.02
117.03
117.04
117.05
117.06
117.07
117.08
117.09
117.10
117.11
117.12
117.13
117.14
117.15
117.16
1MEG
-100V
2PCF
4PCF
CF
A
T

FIG.117

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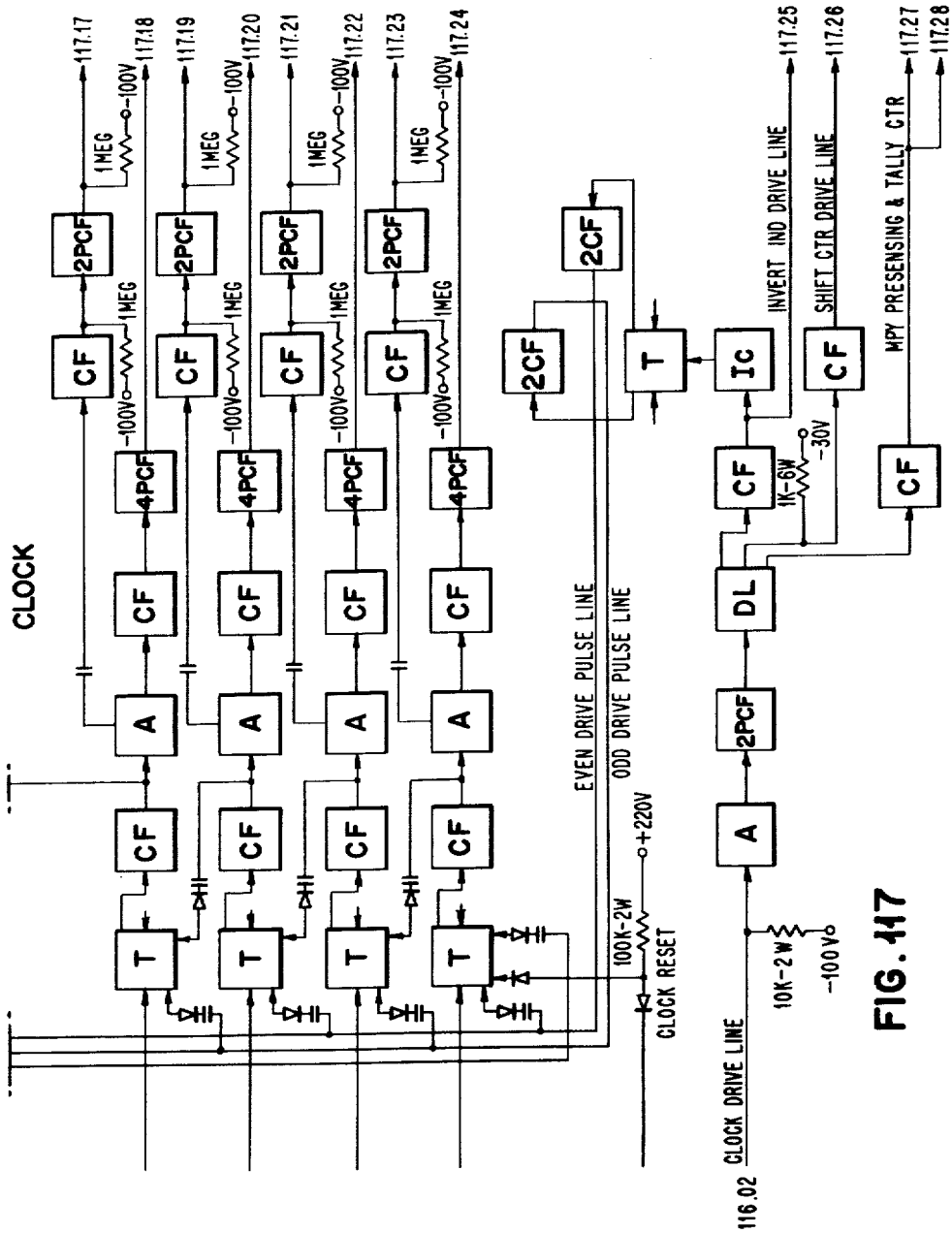
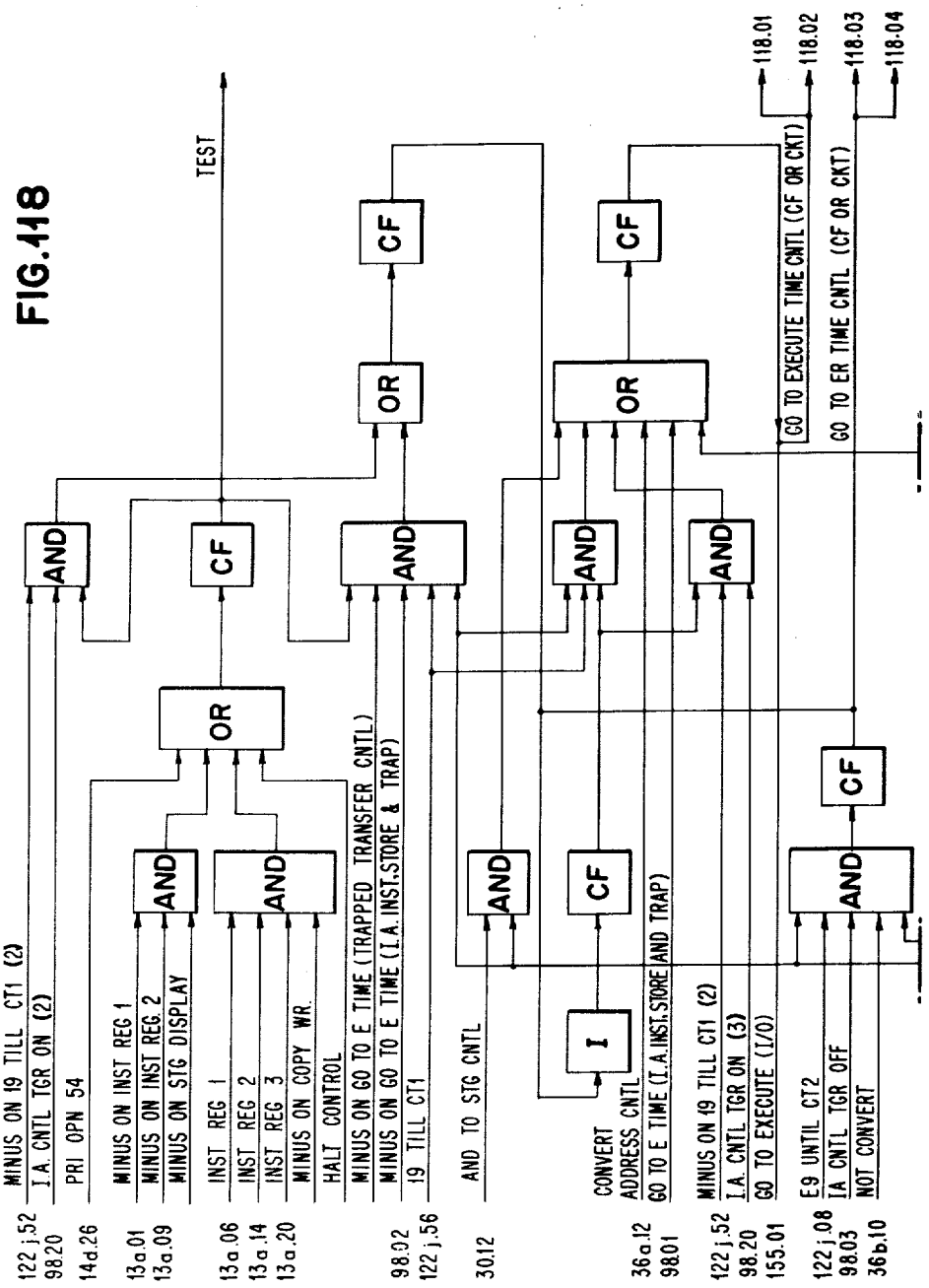


FIG. 117

CYCLE TIMER CONTROL

FIG.418



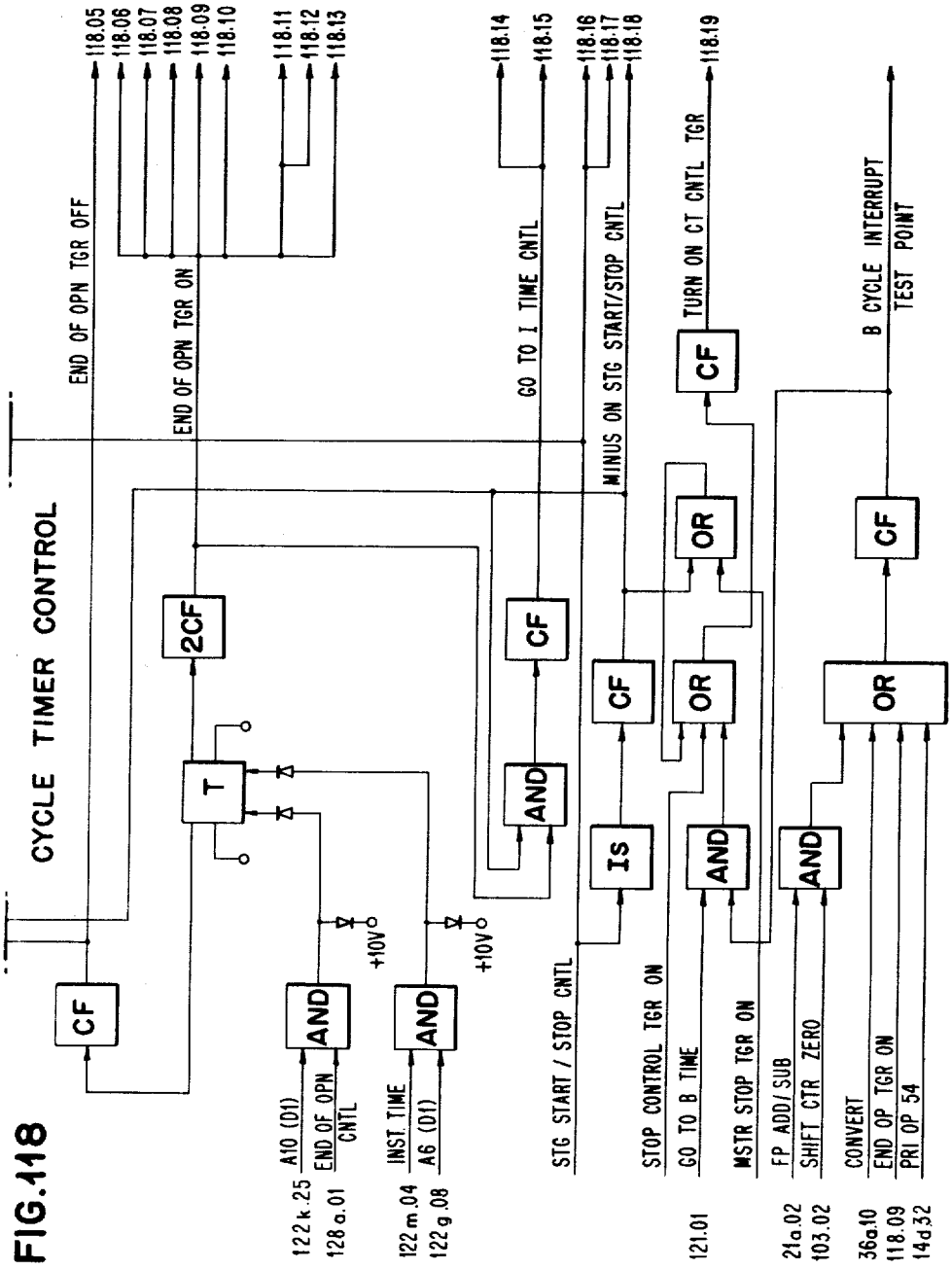

CYCLE TIMER CONTROL
END OF OPN TGR OFF
END OF OPN TGR ON
GO TO I TIME CNTL
MINUS ON STG START/STOP CNTL
TURN ON CT CNTL TGR
B CYCLE INTERRUPT
TEST POINT
118.05
118.06
118.07
118.08
118.09
118.10
118.11
118.12
118.13
118.14
118.15
118.16
118.17
118.18
118.19
CF
2CF
T
AND
Is
OR
+10V
A10 (D1)
END OF OPN CNTL
122 k.25
128 a.01
INST. TIME
A6 (D1)
122 m.04
122 g.08
STG START / STOP CNTL
STOP CONTROL TGR ON
GO TO B TIME
MSTR STOP TGR ON
121.01
FP ADD/SUB
SHIFT CTR ZERO
21a.02
103.02
CONVERT
END OP TGR ON
PRI OP 54
36a.10
118.09
14d.32

FIG.118

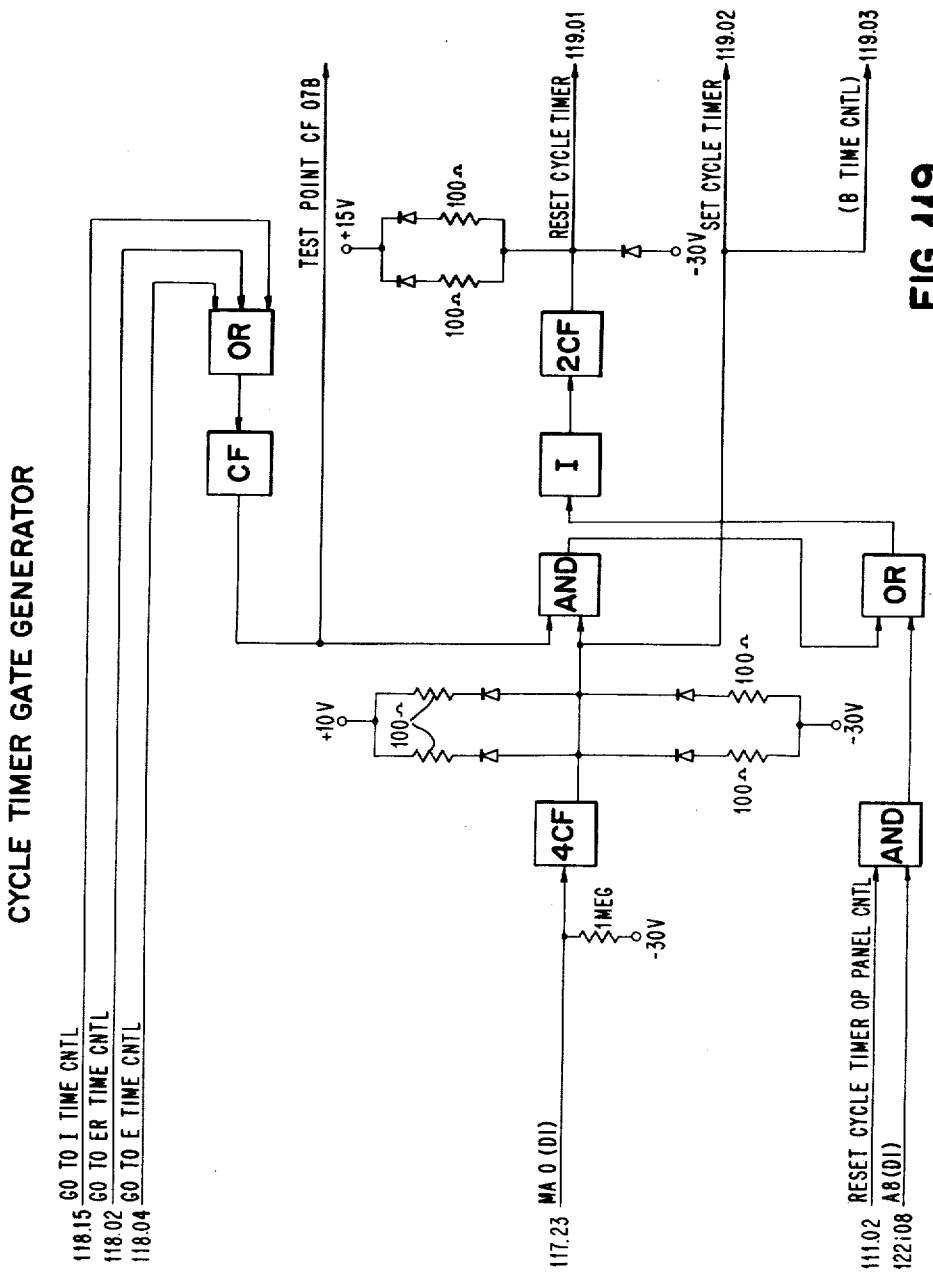

CYCLE TIMER GATE GENERATOR
118.15 GO TO I TIME CNTL
118.02 GO TO ER TIME CNTL
118.04 GO TO E TIME CNTL
OR
CF
TEST POINT CF 07B
+15V
100Ω
100Ω
RESET CYCLE TIMER 119.01
-30V
SET CYCLE TIMER 119.02
(B TIME CNTL) 119.03
2CF
I
AND
OR
+10V
100Ω
100Ω
100Ω
-30V
4CF
1MEG
-30V
AND
MA 0 (01) 117.23
RESET CYCLE TIMER OP PANEL CNTL 111.02
AB (01) 122.08

FIG. 119

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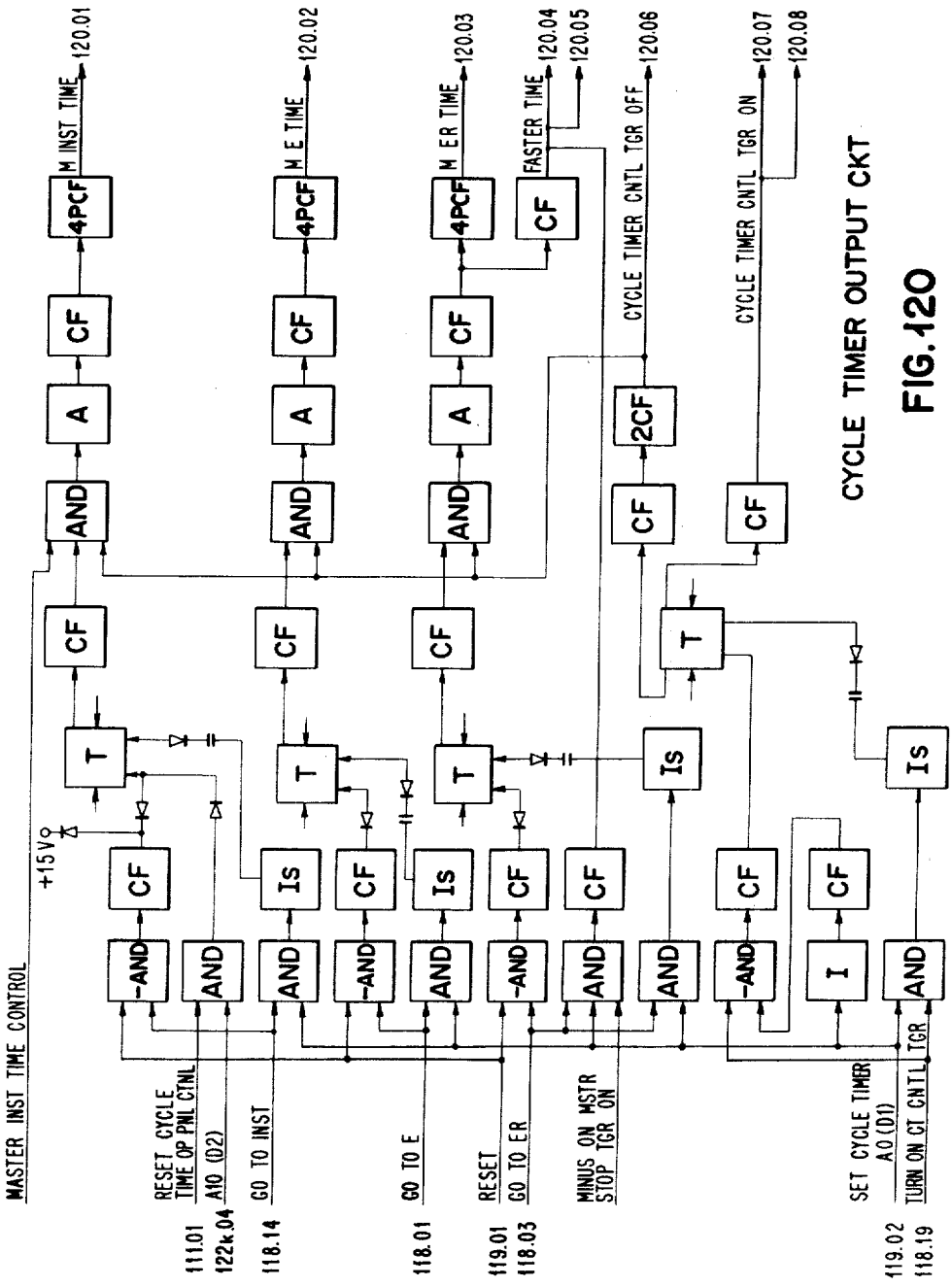
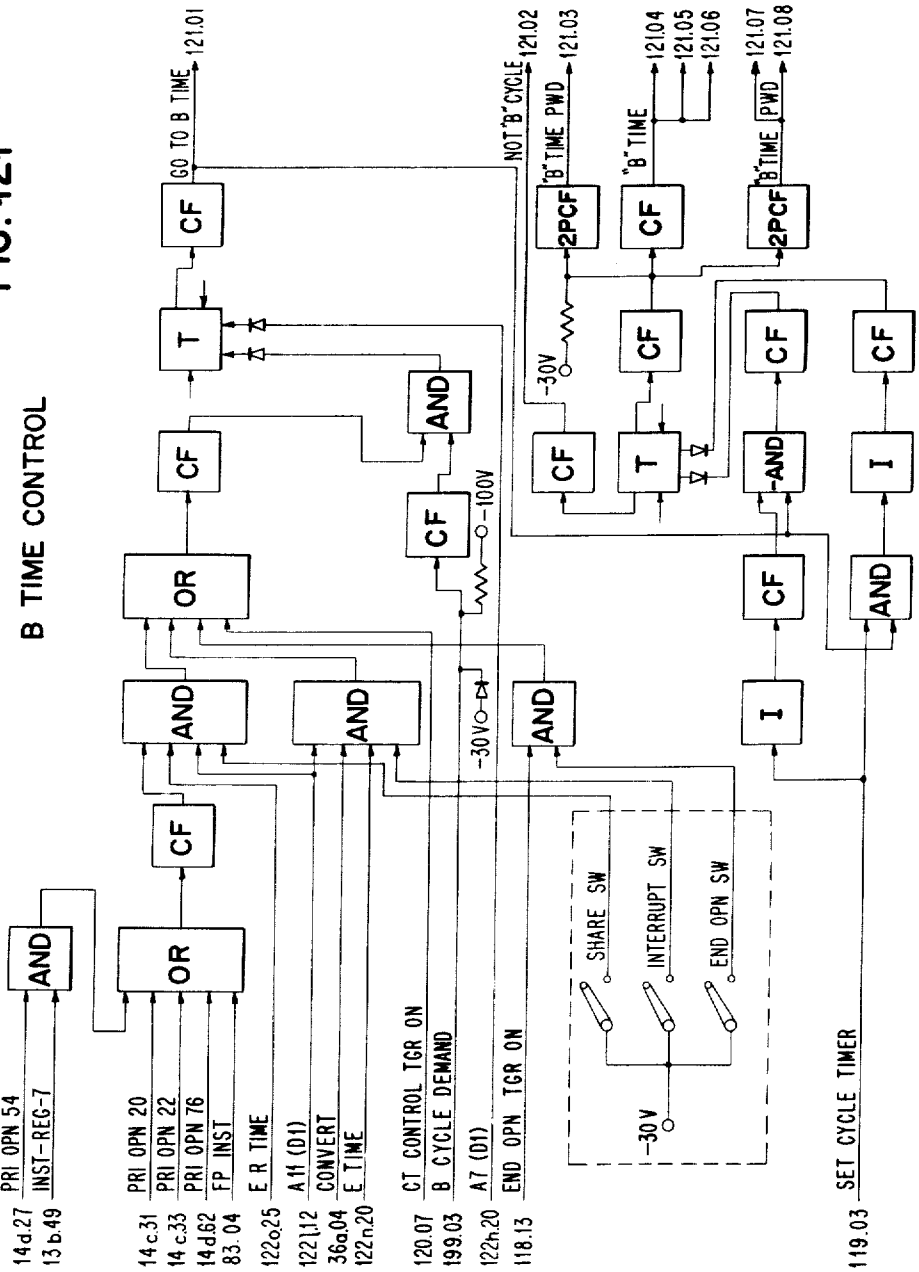


FIG. 120

FIG. 121

B TIME CONTROL



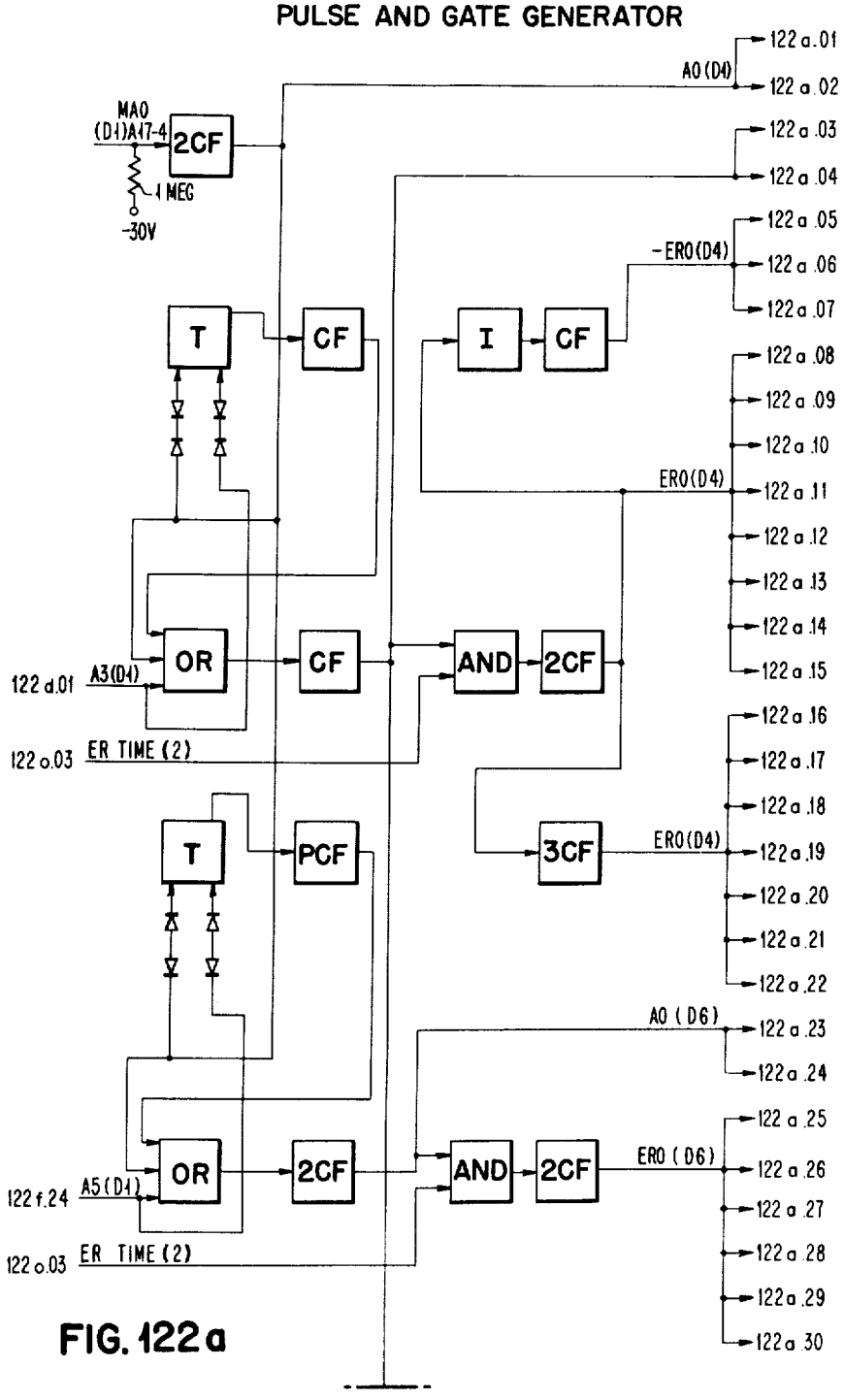

PULSE AND GATE GENERATOR
MA0 (D1)A17-4
2CF
1 MEG
-30V
T
CF
I
CF
OR
CF
AND
2CF
3CF
PCF
122 d.01 A3(D4)
122 o.03 ER TIME (2)
122 f.24 A5(D4)
122 o.03 ER TIME (2)
A0(D4)
-ER0(D4)
ER0(D4)
ER0(D4)
A0 (D6)
ER0 (D6)
122 a.01
122 a.02
122 a.03
122 a.04
122 a.05
122 a.06
122 a.07
122 a.08
122 a.09
122 a.10
122 a.11
122 a.12
122 a.13
122 a.14
122 a.15
122 a.16
122 a.17
122 a.18
122 a.19
122 a.20
122 a.21
122 a.22
122 a.23
122 a.24
122 a.25
122 a.26
122 a.27
122 a.28
122 a.29
122 a.30

FIG. 122a

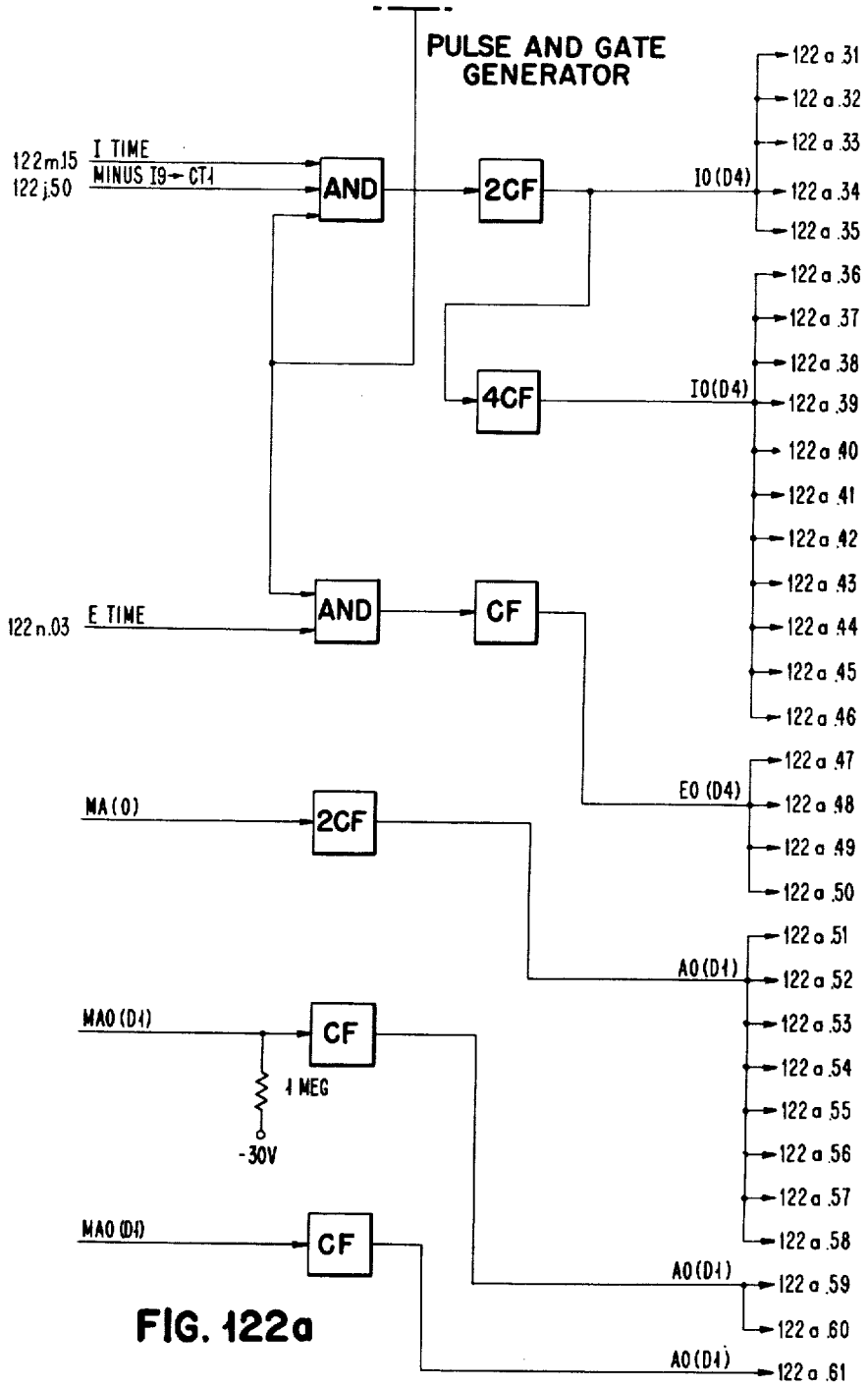

PULSE AND GATE GENERATOR
122m.15 I TIME
122j.50 MINUS I9→CT1
AND
2CF
IO(D4)
122a.31
122a.32
122a.33
122a.34
122a.35
4CF
IO(D4)
122a.36
122a.37
122a.38
122a.39
122a.40
122a.41
122a.42
122a.43
122a.44
122a.45
122a.46
122n.03 E TIME
AND
CF
EO(D4)
122a.47
122a.48
122a.49
122a.50
MA(0)
2CF
AO(D1)
122a.51
122a.52
122a.53
122a.54
122a.55
122a.56
122a.57
122a.58
MAO(D1)
CF
1 MEG
-30V
MAO(D1)
CF
AO(D1)
122a.59
122a.60
AO(D1)
122a.61

FIG. 122a

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INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

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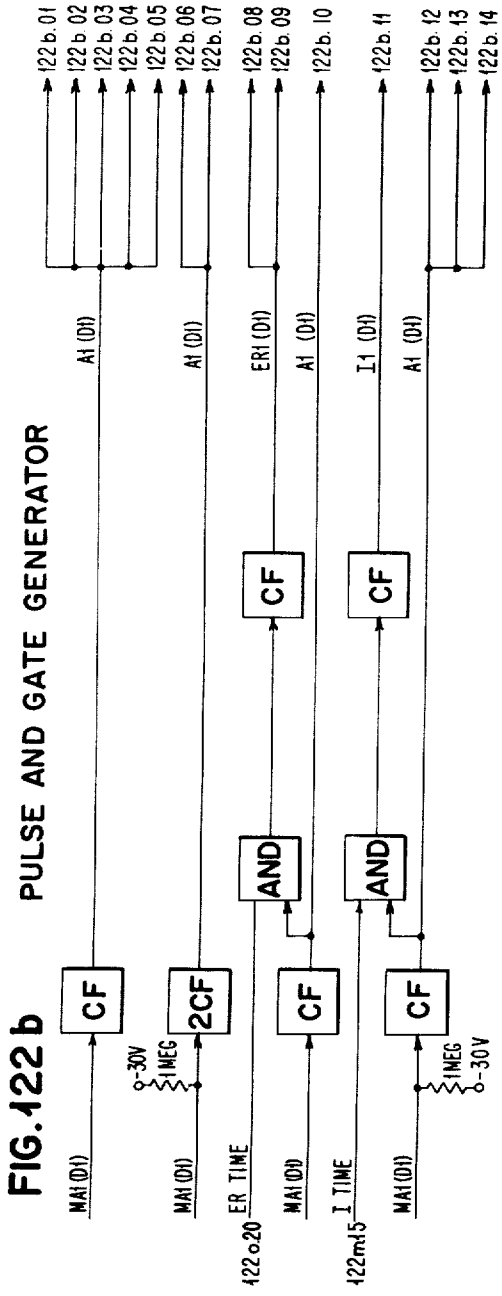

FIG. 122 b

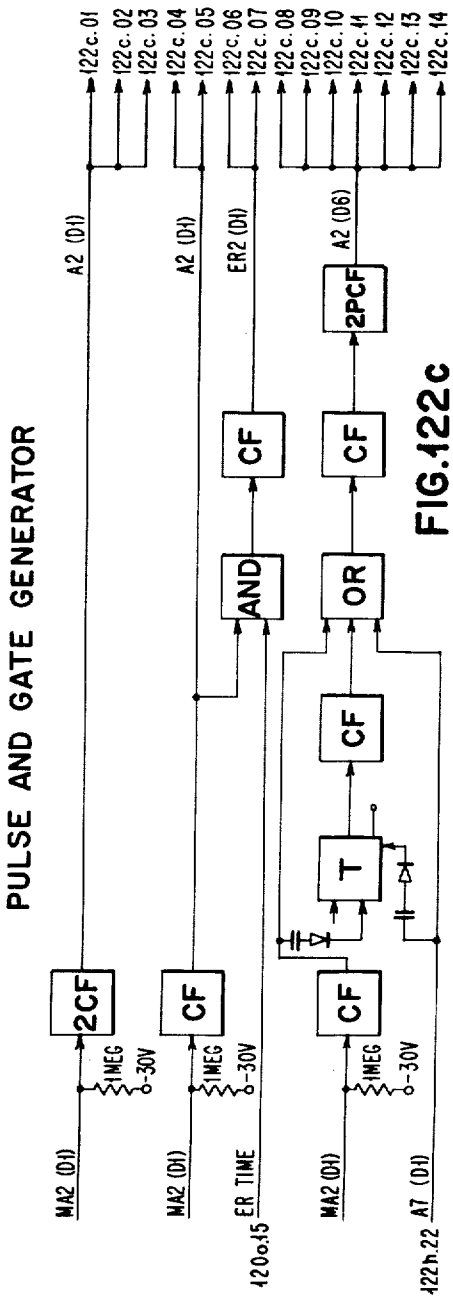

FIG. 122c

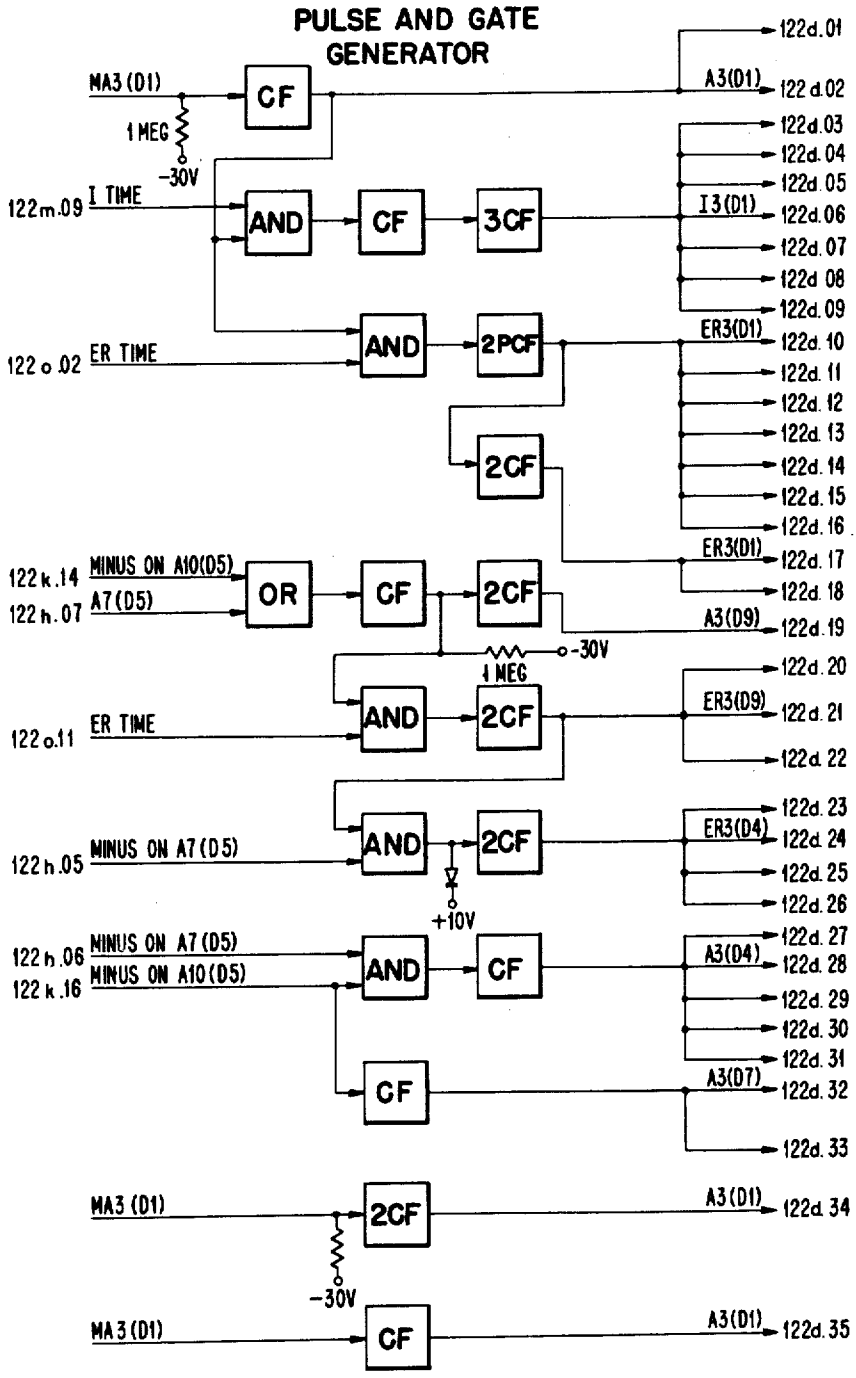
PULSE AND GATE GENERATOR
MA3 (D1)
CF
1 MEG
-30V
122m.09 I TIME
AND
CF
3CF
I3(D1)
122o.02 ER TIME
AND
2PCF
ER3(D1)
2CF
122k.14 MINUS ON A10(D5)
122h.07 A7(D5)
OR
CF
2CF
A3(D9)
-30V
1 MEG
AND
2CF
122o.11 ER TIME
ER3(D9)
122h.05 MINUS ON A7(D5)
AND
2CF
ER3(D4)
+10V
122h.06 MINUS ON A7(D5)
122k.16 MINUS ON A10(D5)
AND
CF
A3(D4)
CF
A3(D7)
MA3 (D1)
2CF
A3(D1)
-30V
MA3 (D1)
CF
A3(D1)
122d.01
122d.02
122d.03
122d.04
122d.05
122d.06
122d.07
122d.08
122d.09
122d.10
122d.11
122d.12
122d.13
122d.14
122d.15
122d.16
122d.17
122d.18
122d.19
122d.20
122d.21
122d.22
122d.23
122d.24
122d.25
122d.26
122d.27
122d.28
122d.29
122d.30
122d.31
122d.32
122d.33
122d.34
122d.35

FIG. 122d

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INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

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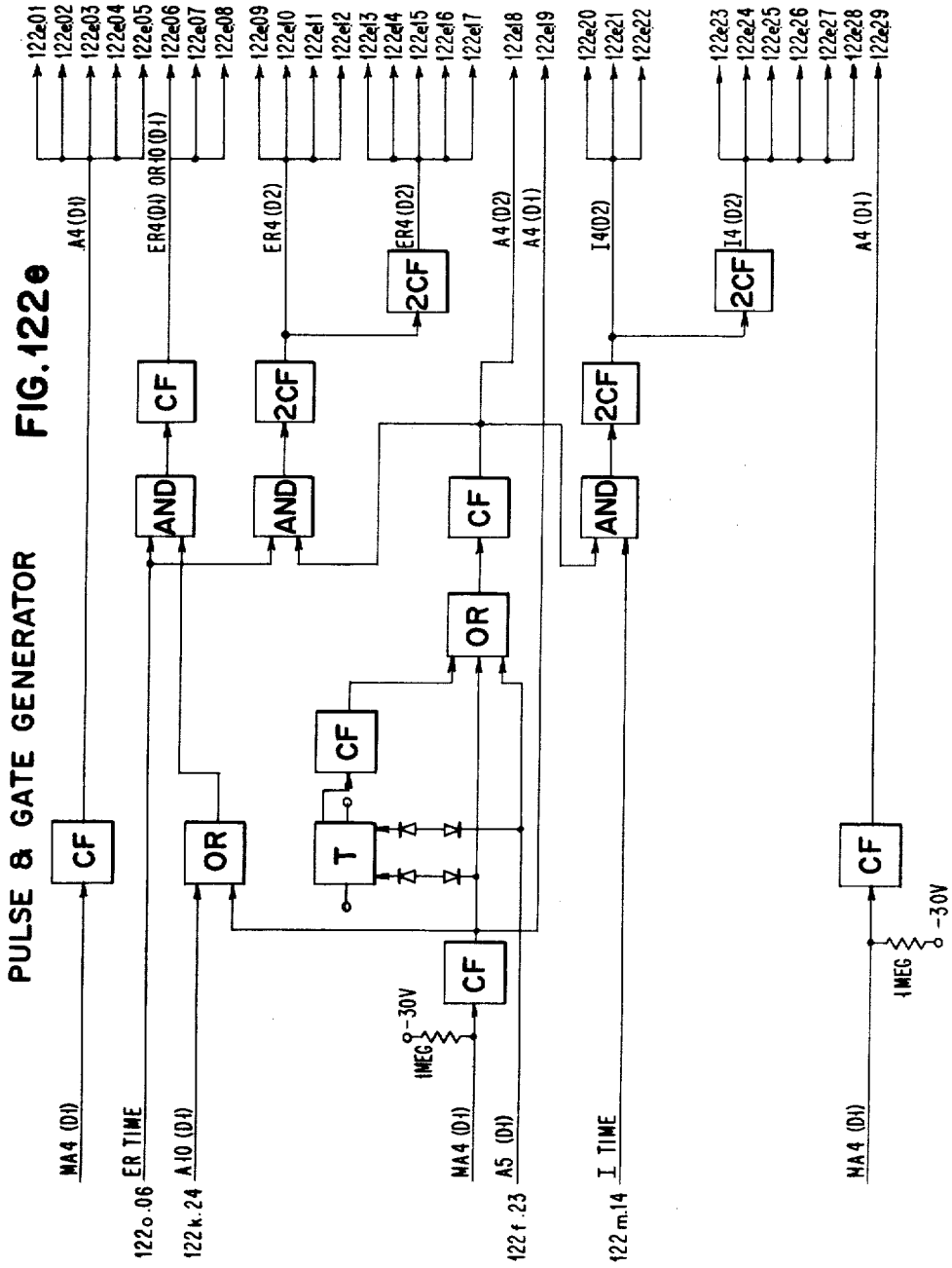


FIG. 122e

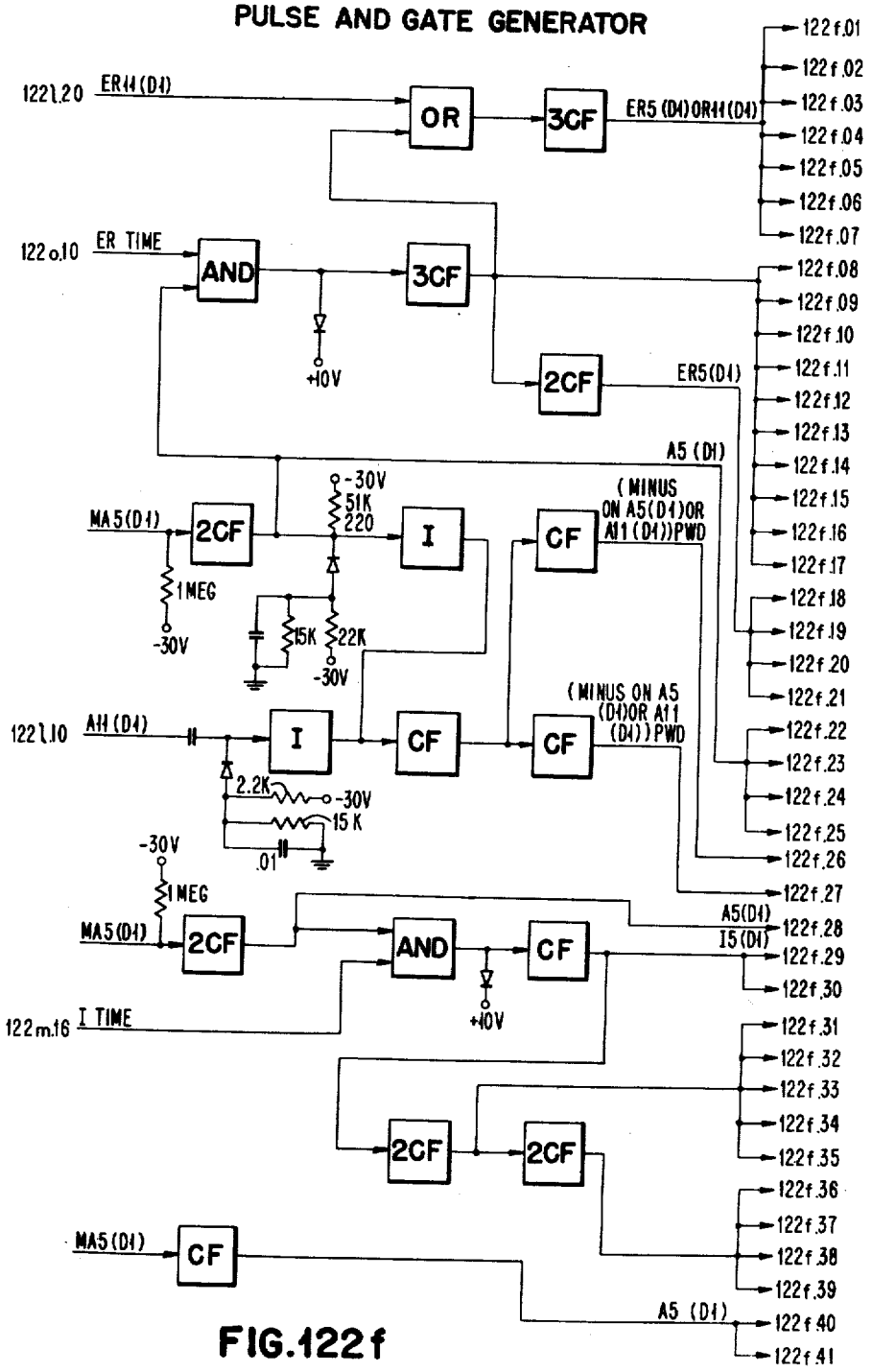

PULSE AND GATE GENERATOR
122l.20 ER4(D4)
OR
3CF
ER5(D4)OR4(D4)
122o.10 ER TIME
AND
3CF
+10V
2CF
ER5(D4)
A5 (D4)
MA5(D4)
2CF
-30V
51K
220
I
CF
(MINUS ON A5(D4)OR A11(D4))PWD
1MEG
-30V
15K
22K
-30V
122l.10 A4(D4)
I
CF
CF
(MINUS ON A5 (D4)OR A11 (D4))PWD
2.2K
-30V
15 K
.01
-30V
1MEG
MA5(D4)
2CF
AND
CF
A5(D4)
I5(D4)
+10V
122m.16 I TIME
2CF
2CF
MA5(D4)
CF
A5 (D4)
122f.01
122f.02
122f.03
122f.04
122f.05
122f.06
122f.07
122f.08
122f.09
122f.10
122f.11
122f.12
122f.13
122f.14
122f.15
122f.16
122f.17
122f.18
122f.19
122f.20
122f.21
122f.22
122f.23
122f.24
122f.25
122f.26
122f.27
122f.28
122f.29
122f.30
122f.31
122f.32
122f.33
122f.34
122f.35
122f.36
122f.37
122f.38
122f.39
122f.40
122f.41

FIG.122f

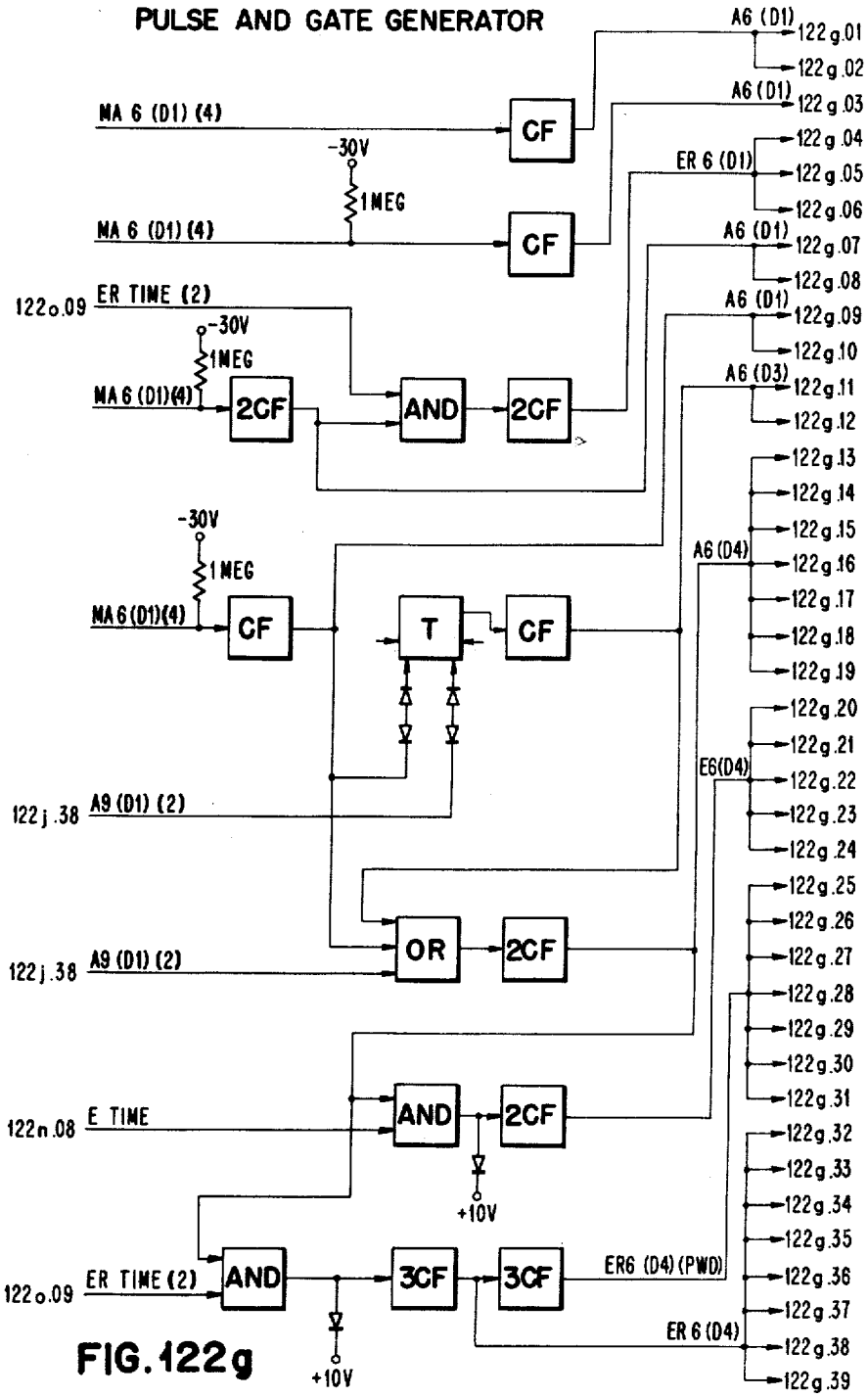

PULSE AND GATE GENERATOR
MA 6 (D1) (4)
CF
-30V
1MEG
MA 6 (D1) (4)
CF
A6 (D1)
122g.01
122g.02
A6 (D1)
122g.03
122g.04
ER 6 (D1)
122g.05
122g.06
A6 (D1)
122g.07
122g.08
122o.09 ER TIME (2)
-30V
1MEG
MA 6 (D1)(4)
2CF
AND
2CF
A6 (D1)
122g.09
122g.10
A6 (D3)
122g.11
122g.12
-30V
1MEG
MA 6 (D1)(4)
CF
T
CF
122g.13
122g.14
122g.15
A6 (D4)
122g.16
122g.17
122g.18
122g.19
122g.20
122g.21
E6(D4)
122g.22
122g.23
122g.24
122j.38 A9 (D1) (2)
122g.25
122g.26
122g.27
122g.28
122g.29
122g.30
122g.31
122j.38 A9 (D1) (2)
OR
2CF
122n.08 E TIME
AND
2CF
+10V
122g.32
122g.33
122g.34
122g.35
122g.36
122g.37
122g.38
122g.39
122o.09 ER TIME (2)
AND
3CF
3CF
ER6 (D4) (PWD)
ER 6 (D4)
+10V

FIG. 122g

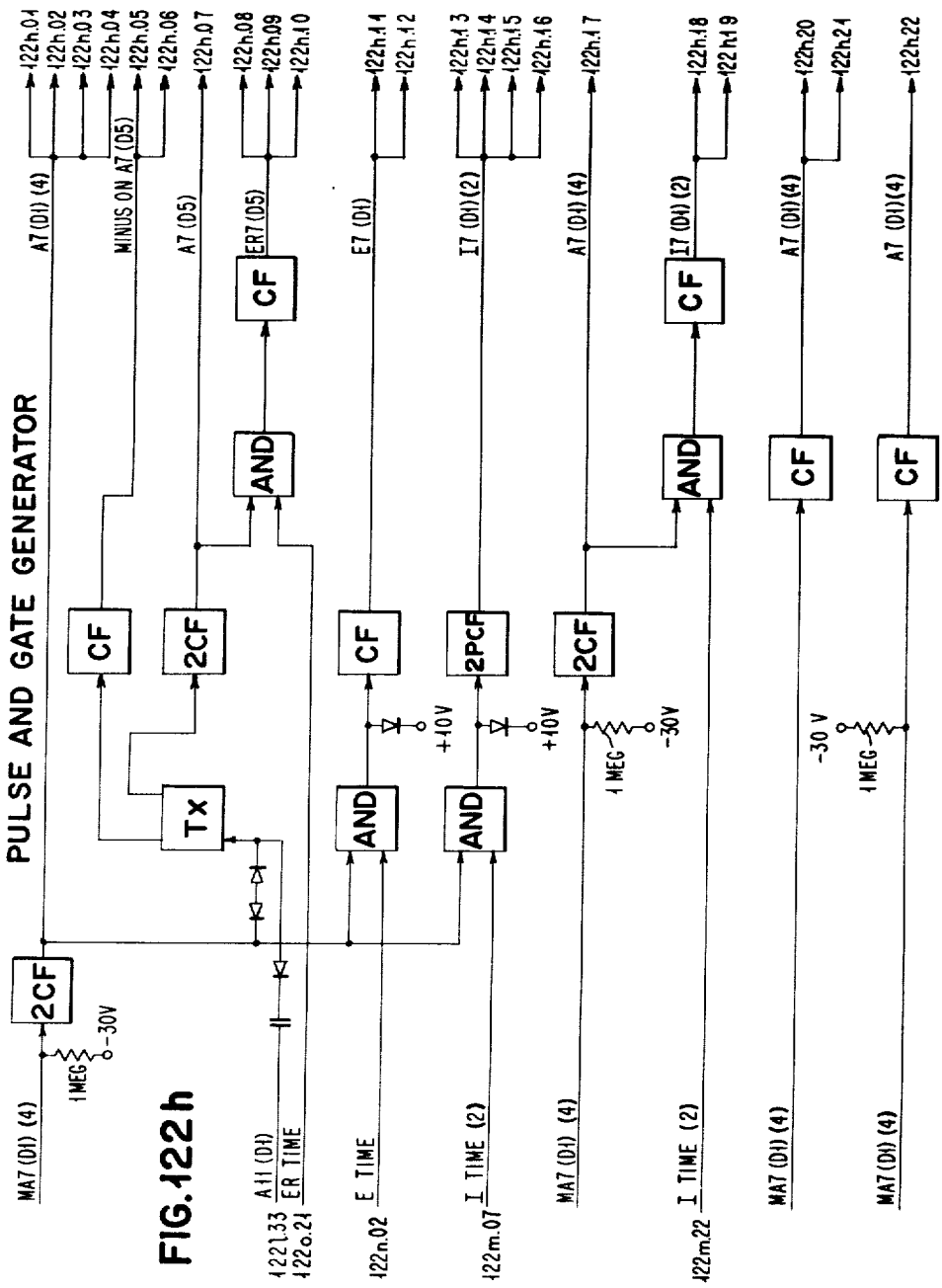
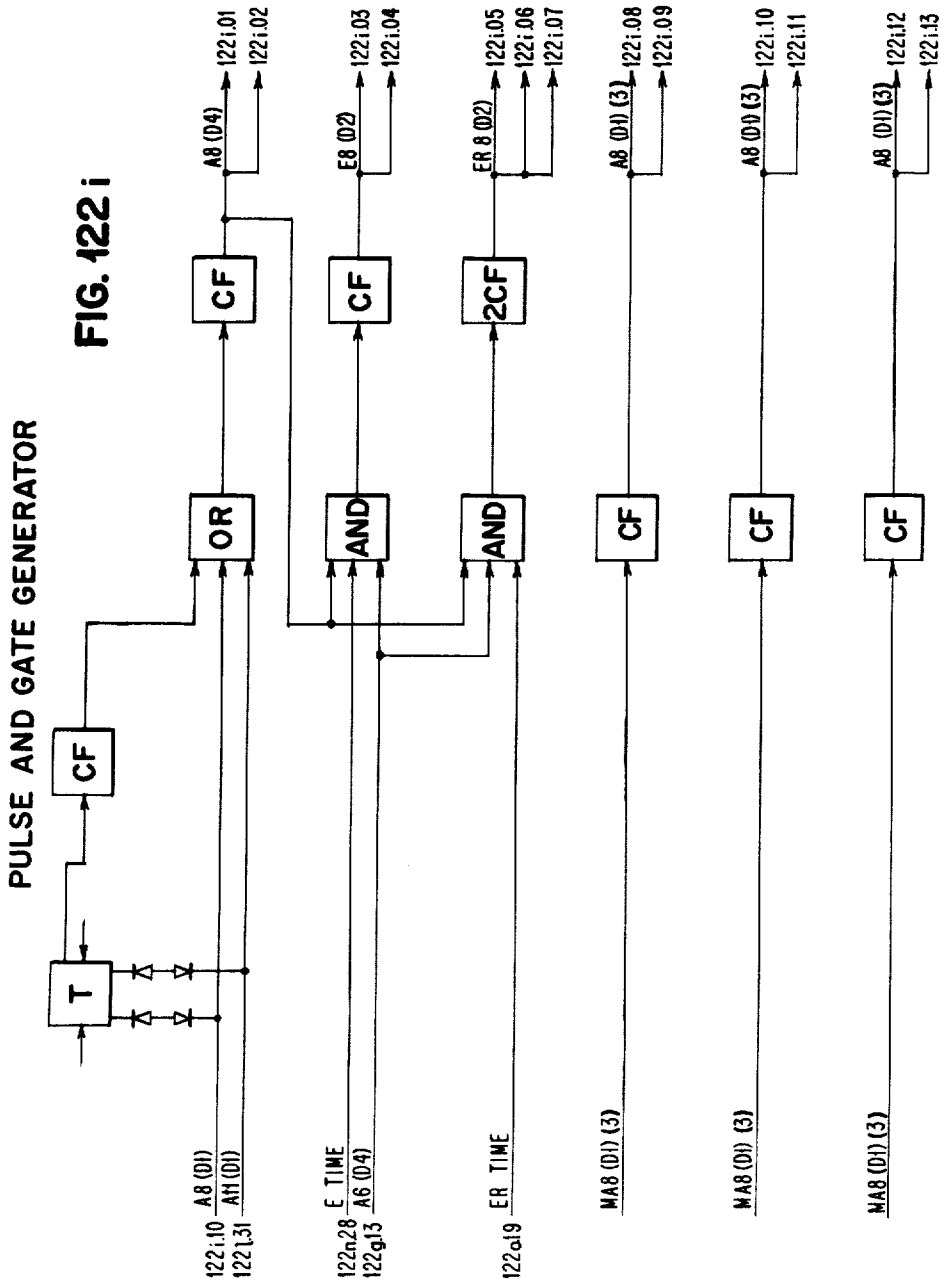

PULSE AND GATE GENERATOR
122n.01
122n.02
122n.03
122n.04
122n.05
122n.06
122n.07
122n.08
122n.09
122n.10
122n.11
122n.12
122n.13
122n.14
122n.15
122n.16
122n.17
122n.18
122n.19
122n.20
122n.21
122n.22
A7 (D1) (4)
MINUS ON A7 (D5)
A7 (D5)
ER7 (D5)
E7 (D1)
I7 (D1) (2)
A7 (D1) (4)
I7 (D1) (2)
A7 (D1) (4)
A7 (D1) (4)
CF
2CF
Tx
AND
2PCF
+10V
-30V
-30 V
1 MEG
MA7 (D1) (4)
A11 (D1)
122l.33
122o.24
ER TIME
E TIME
122n.02
I TIME (2)
122m.07
MA7 (D1) (4)
I TIME (2)
122m.22
MA7 (D1) (4)
MA7 (D1) (4)

FIG. 122h

FIG. 122 i


PULSE AND GATE GENERATOR
CF
T
OR
CF
A8 (04)
122i.01
122i.02
AND
CF
E8 (02)
122i.03
122i.04
AND
2CF
ER 8 (02)
122i.05
122i.06
122i.07
CF
A8 (01) (3)
122i.08
122i.09
CF
A8 (00) (3)
122i.10
122i.11
CF
A8 (01) (3)
122i.12
122i.13
122i.10 A8 (01)
122i.31 A11 (01)
122n.28 E TIME
122g.13 A6 (04)
122a.19 ER TIME
MA8 (01) (3)
MA8 (01) (3)
MA8 (01) (3)

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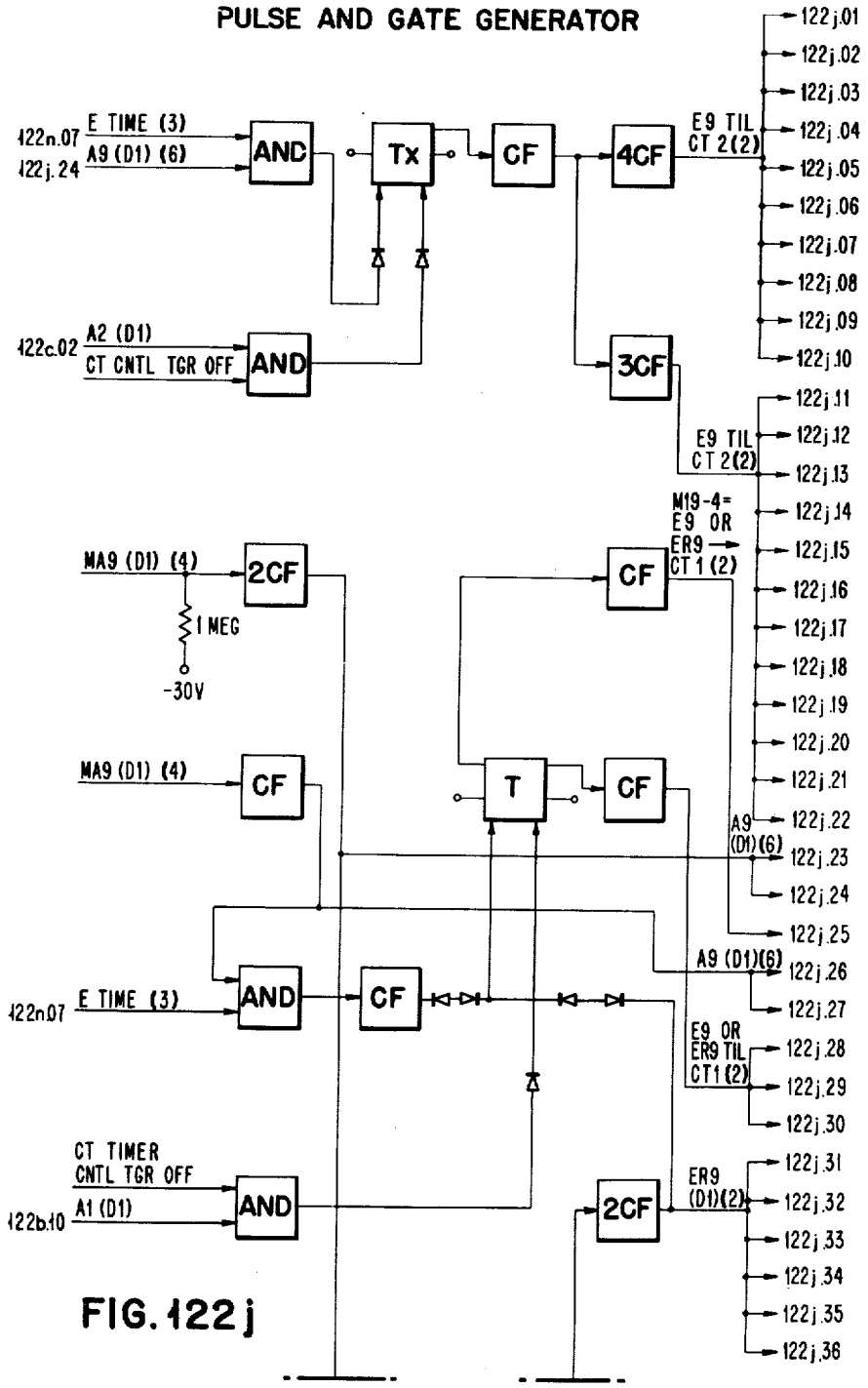

FIG. 122j

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INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

Filed Dec. 26, 1957 244 Sheets-Sheet 208

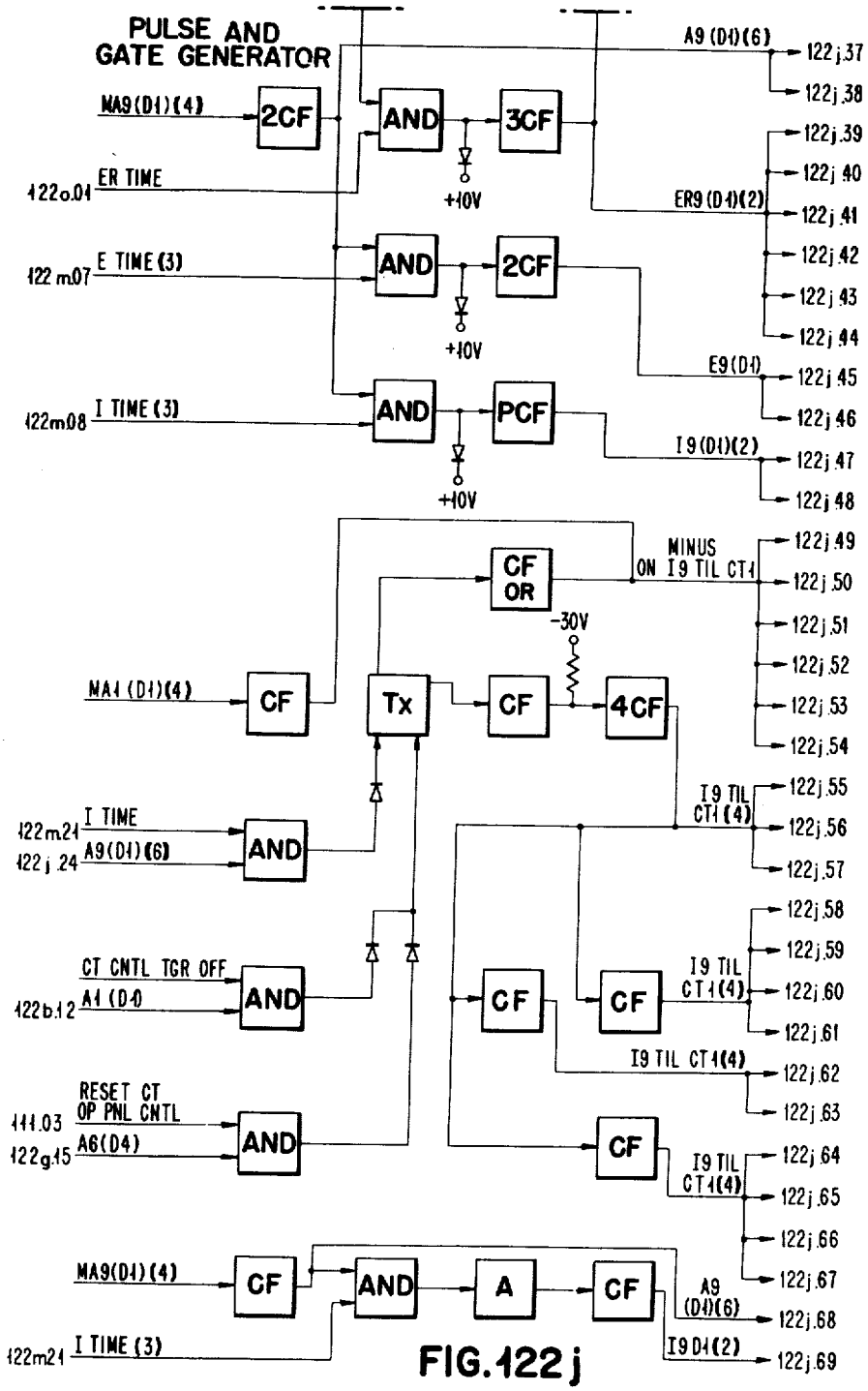

FIG. 122j

May 29, 1962 J. L. BROWN 3,036,773
INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE
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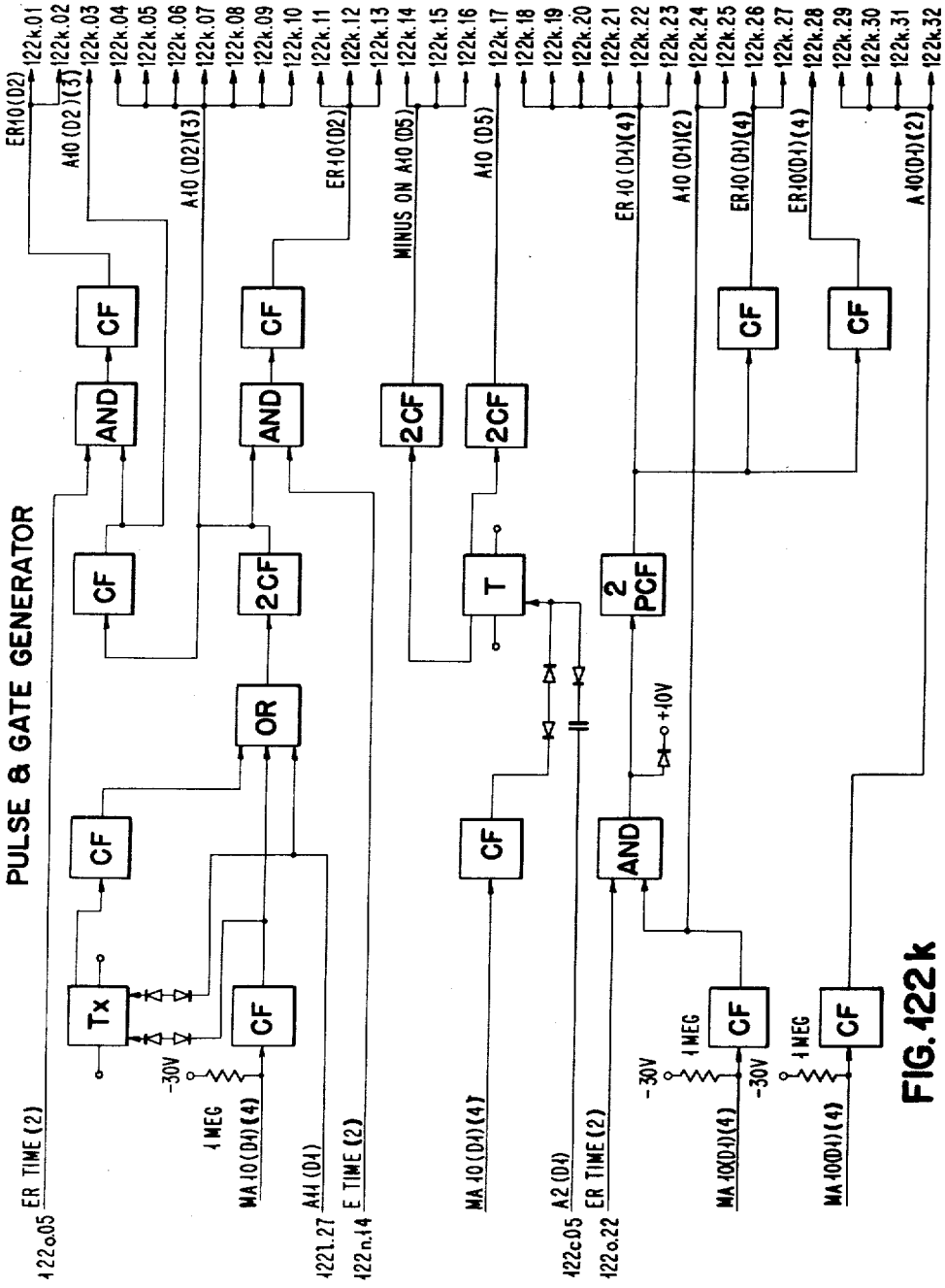

FIG. 422k

May 29, 1962 J. L. BROWN 3,036,773

INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

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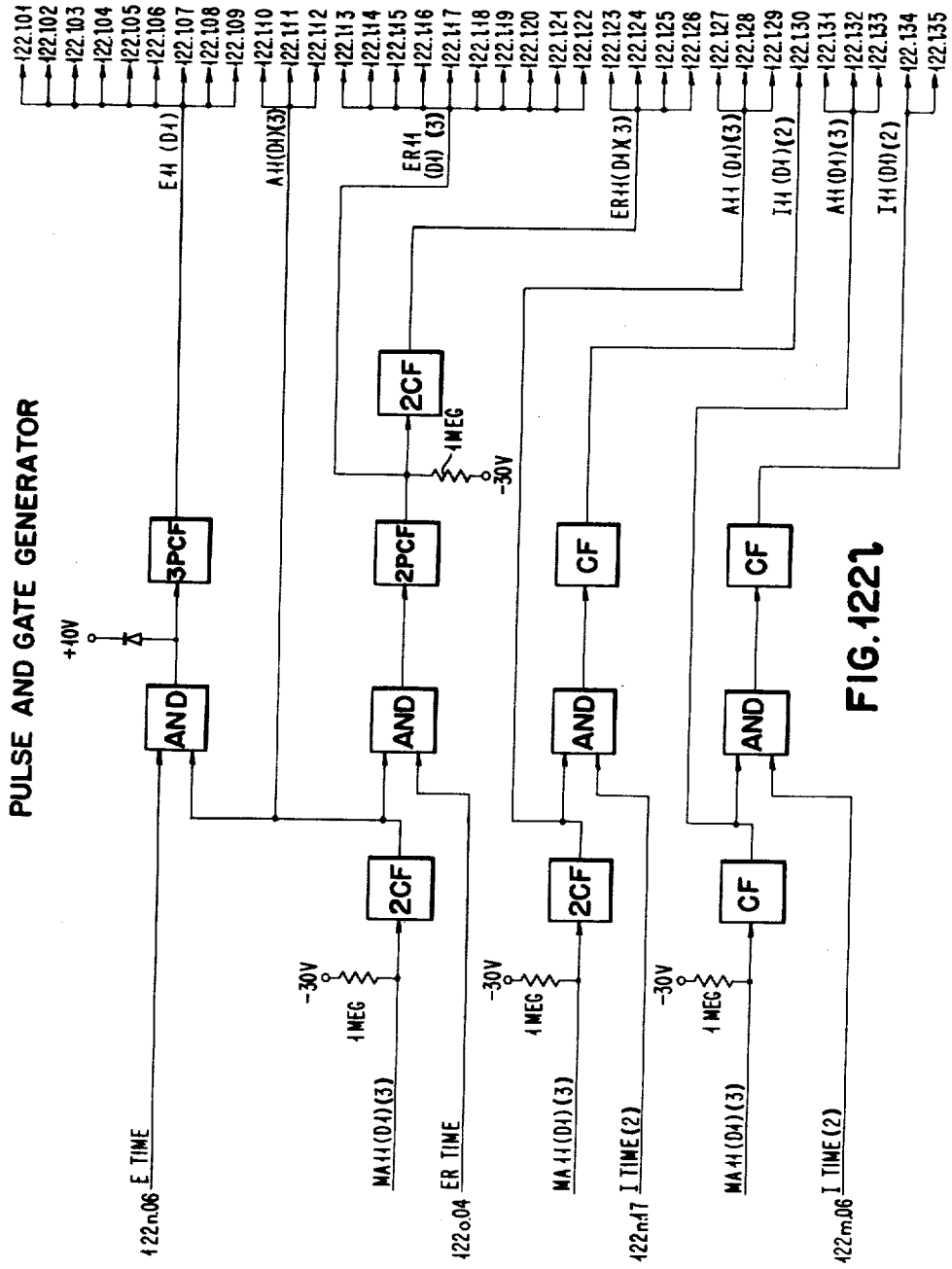

FIG. 1221

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INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

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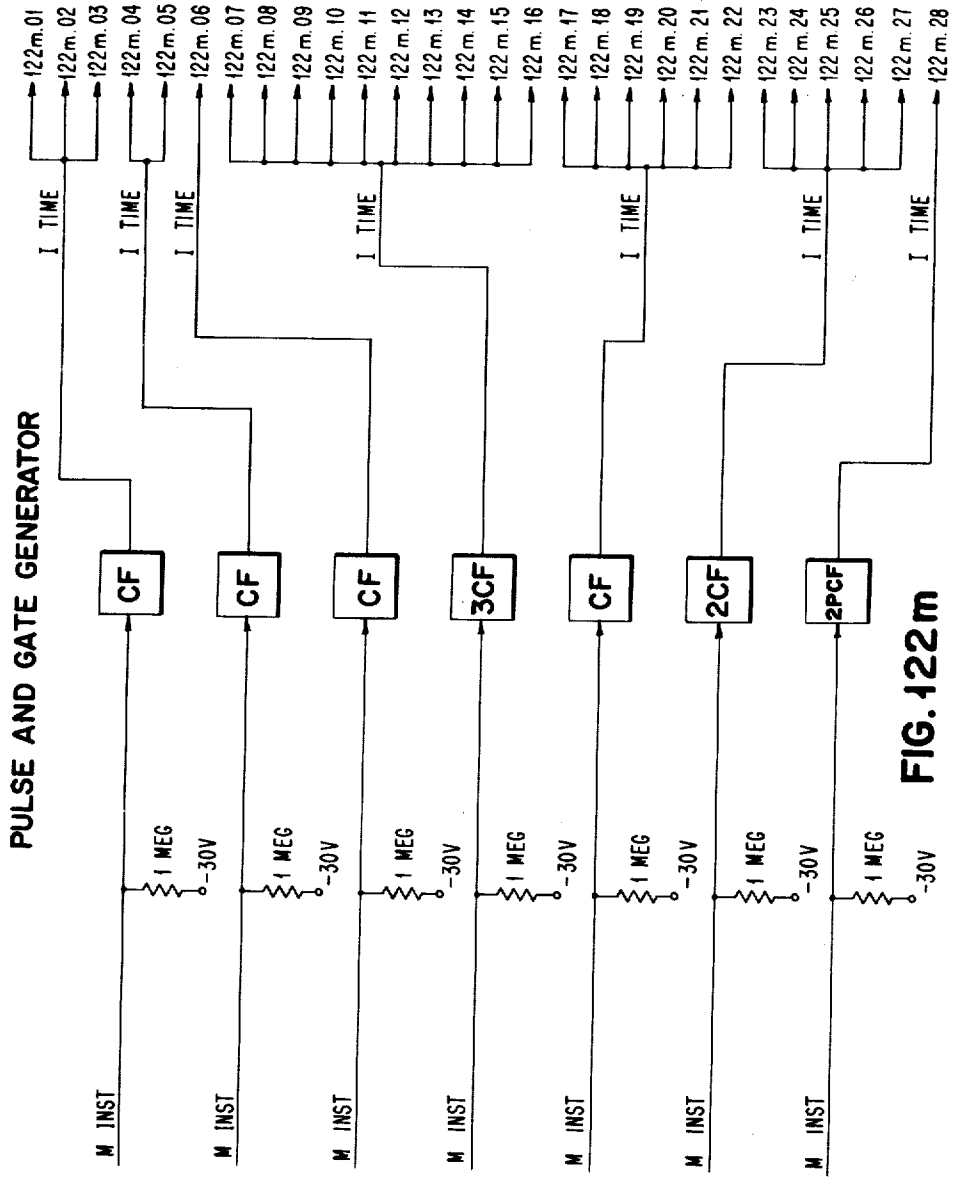


FIG. 122m

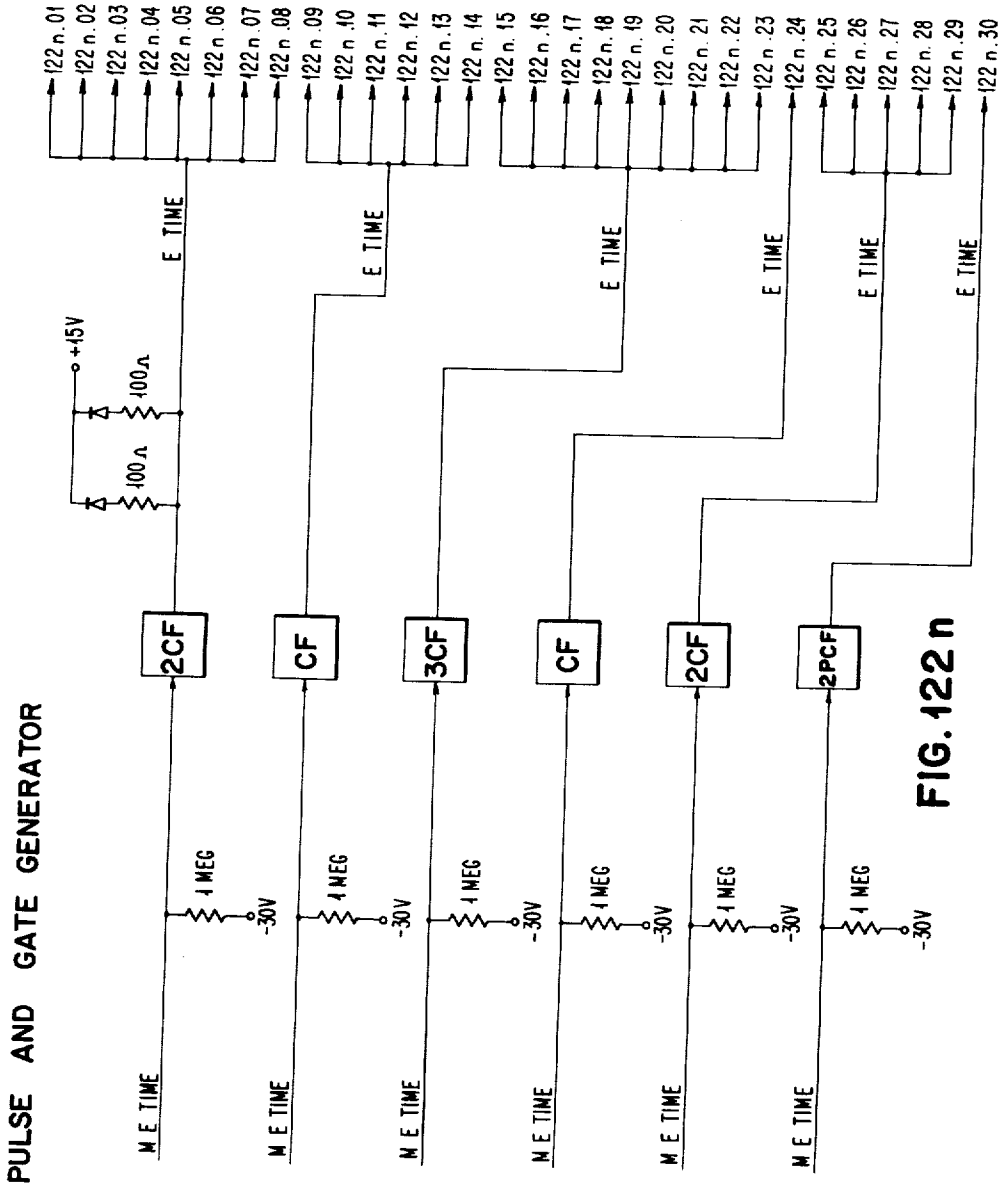
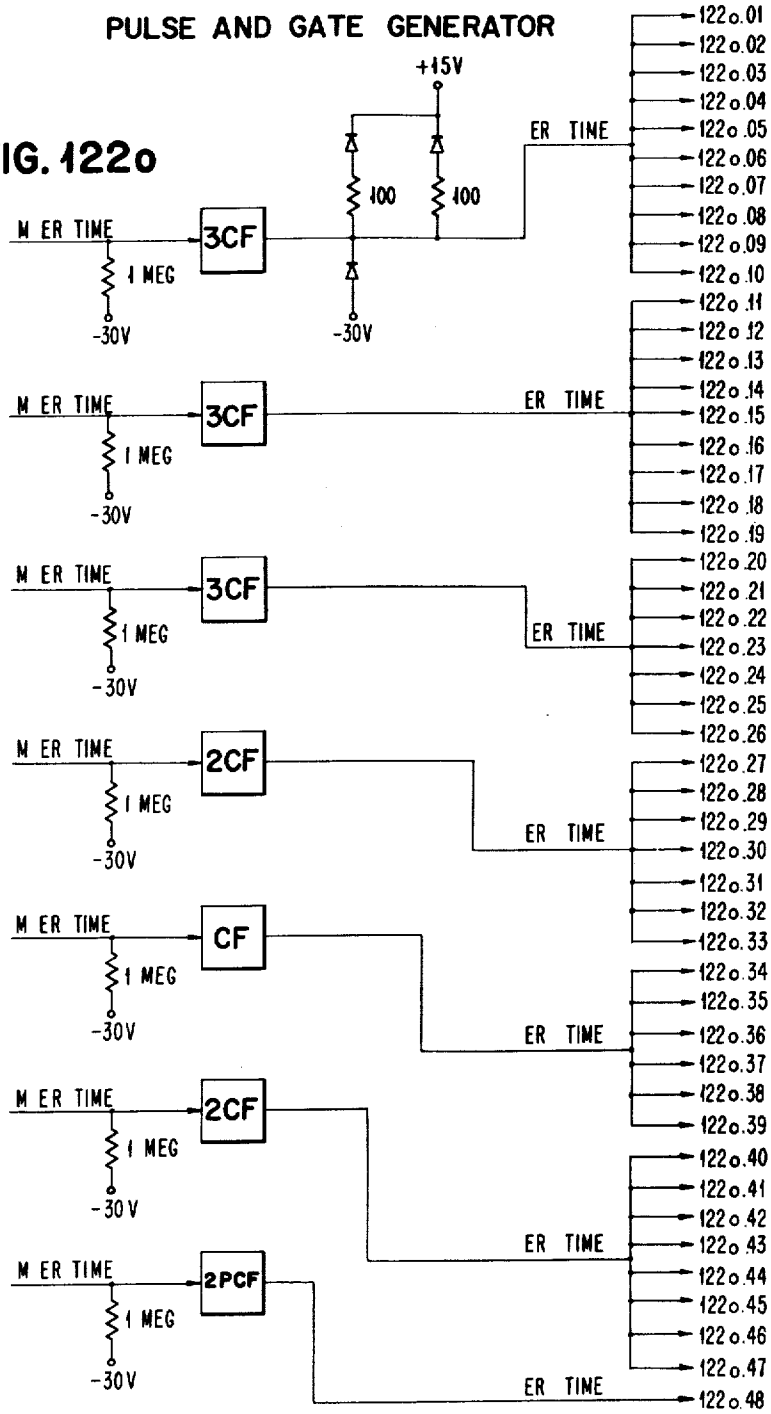

PULSE AND GATE GENERATOR
122 n.01
122 n.02
122 n.03
122 n.04
122 n.05
122 n.06
122 n.07
122 n.08
122 n.09
122 n.10
122 n.11
122 n.12
122 n.13
122 n.14
122 n.15
122 n.16
122 n.17
122 n.18
122 n.19
122 n.20
122 n.21
122 n.22
122 n.23
122 n.24
122 n.25
122 n.26
122 n.27
122 n.28
122 n.29
122 n.30
E TIME
+15V
100Ω
100Ω
2CF
CF
3CF
CF
2CF
2PCF
1 MEG
-30V
M E TIME

FIG. 122 n

FIG. 122o


PULSE AND GATE GENERATOR
+15V
100
100
M ER TIME
1 MEG
-30V
3CF
2CF
CF
2PCF
ER TIME
122o.01
122o.02
122o.03
122o.04
122o.05
122o.06
122o.07
122o.08
122o.09
122o.10
122o.11
122o.12
122o.13
122o.14
122o.15
122o.16
122o.17
122o.18
122o.19
122o.20
122o.21
122o.22
122o.23
122o.24
122o.25
122o.26
122o.27
122o.28
122o.29
122o.30
122o.31
122o.32
122o.33
122o.34
122o.35
122o.36
122o.37
122o.38
122o.39
122o.40
122o.41
122o.42
122o.43
122o.44
122o.45
122o.46
122o.47
122o.48

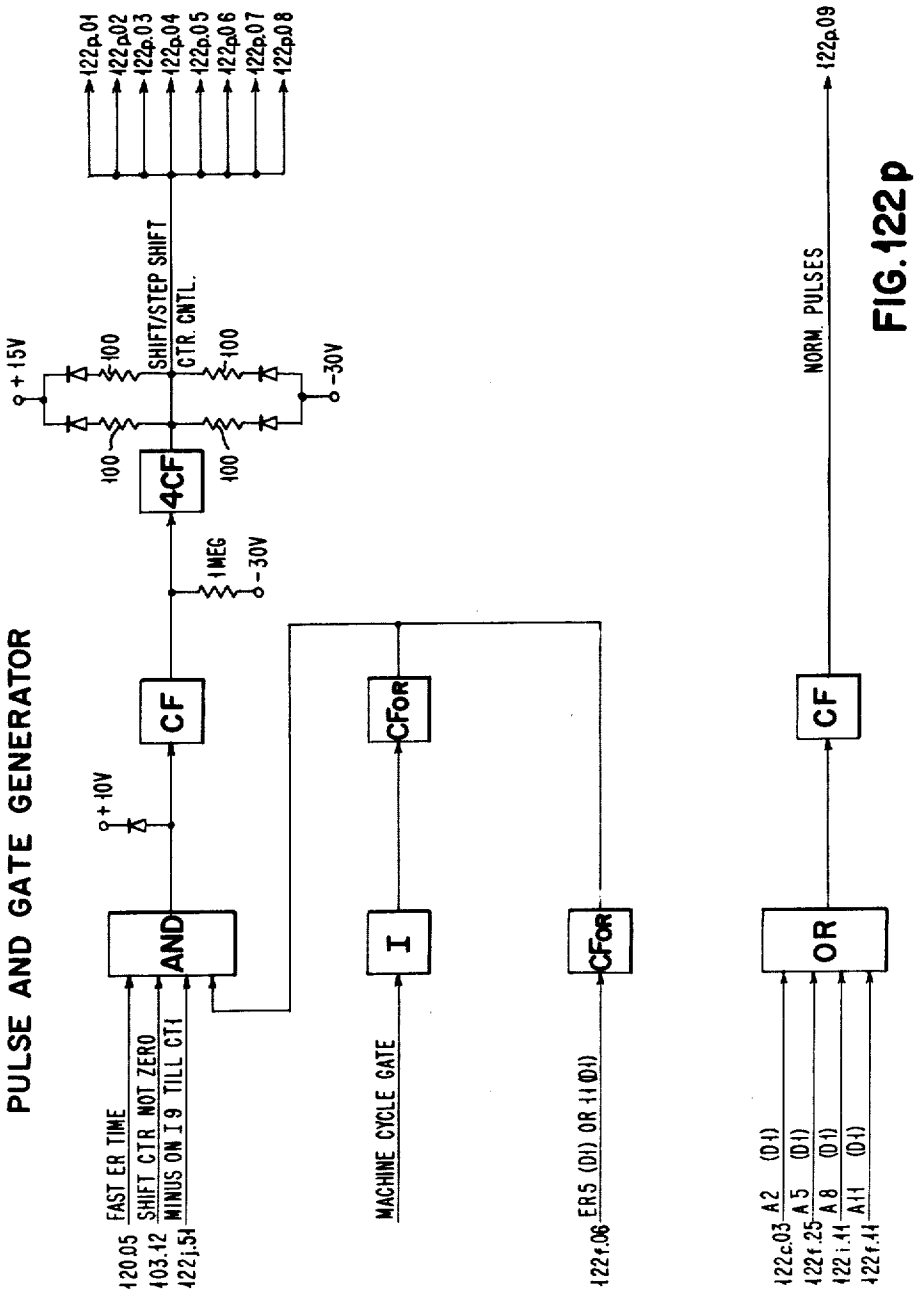

PULSE AND GATE GENERATOR
122p.01
122p.02
122p.03
122p.04
122p.05
122p.06
122p.07
122p.08
SHIFT/STEP SHIFT
CTR. CNTL.
+15V
100
100
-30V
100
100
4CF
1 MEG
-30V
+10V
CF
AND
CFOR
I
CFOR
OR
CF
122p.09
NORM. PULSES
120.05 FAST ER TIME
103.12 SHIFT CTR NOT ZERO
122j.54 MINUS ON I 9 TILL CT1
MACHINE CYCLE GATE
122f.06 ER5 (D1) OR 11 (D1)
122c.03 A2 (D1)
122f.25 A5 (D1)
122i.41 A8 (D1)
122f.44 A11 (D1)

FIG. 122p

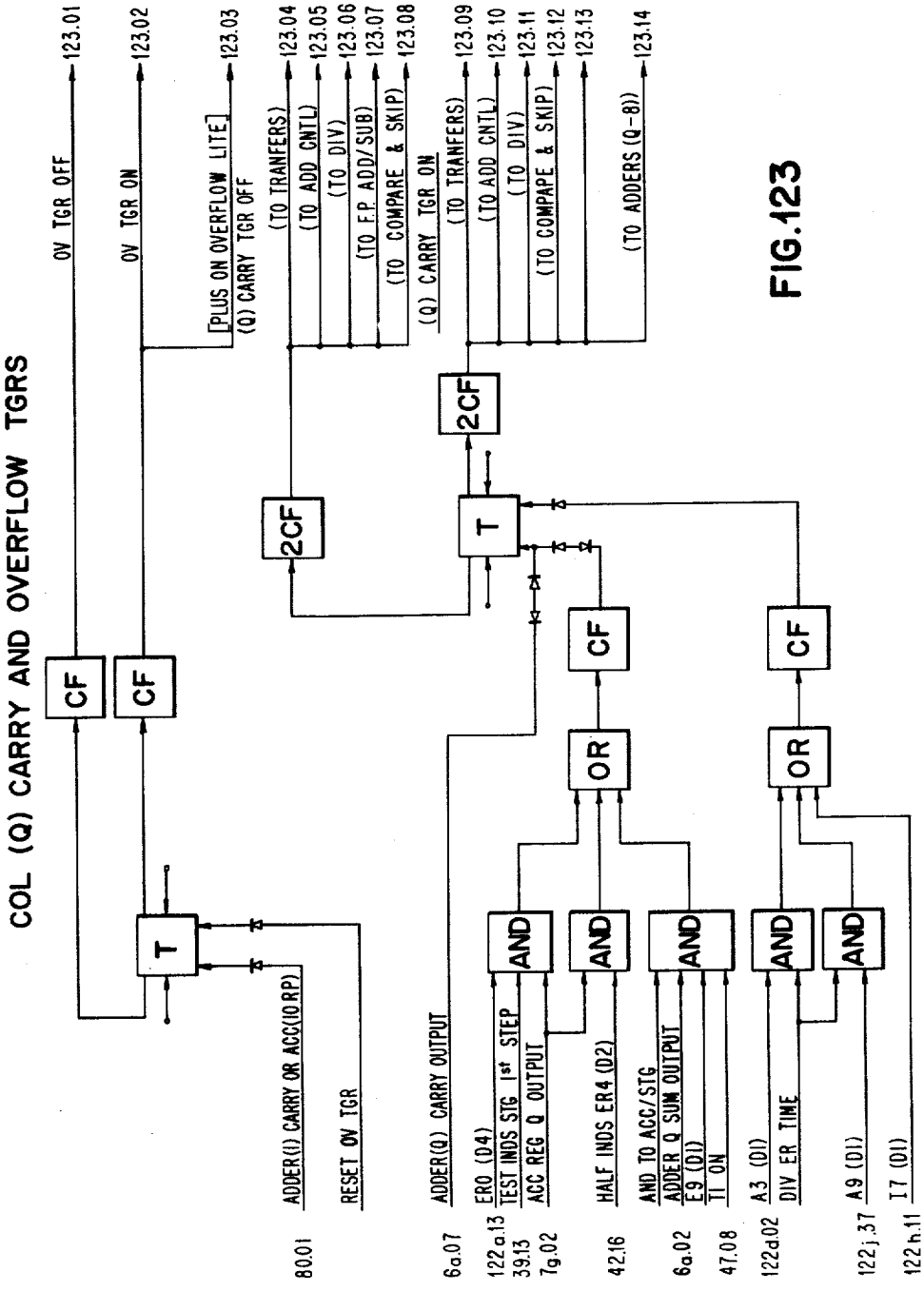

COL (Q) CARRY AND OVERFLOW TGRS
OV TGR OFF
123.01
OV TGR ON
123.02
PLUS ON OVERFLOW LITE
(Q) CARRY TGR OFF
123.03
(TO TRANFERS)
123.04
(TO ADD CNTL)
123.05
(TO DIV)
123.06
(TO F.P. ADD/SUB)
123.07
(TO COMPARE & SKIP)
123.08
(Q) CARRY TGR ON
(TO TRANFERS)
123.09
(TO ADD CNTL)
123.10
(TO DIV)
123.11
(TO COMPAPE & SKIP)
123.12
123.13
(TO ADDERS (Q-8))
123.14
CF
CF
2CF
2CF
T
T
OR
OR
CF
CF
AND
AND
AND
AND
AND
ADDER(I) CARRY OR ACC(10 RP)
80.01
RESET OV TGR
ADDER(Q) CARRY OUTPUT
6a.07
ERO (04)
122a.13
TEST INDS STG 1st STEP
39.13
ACC REG Q OUTPUT
7g.02
HALF INDS ER4 (02)
42.16
AND TO ACC/STG
ADDER Q SUM OUTPUT
6a.02
E9 (01)
TI ON
47.08
A3 (01)
DIV ER TIME
122d.02
A9 (01)
122j.37
I7 (01)
122h.11

FIG.123

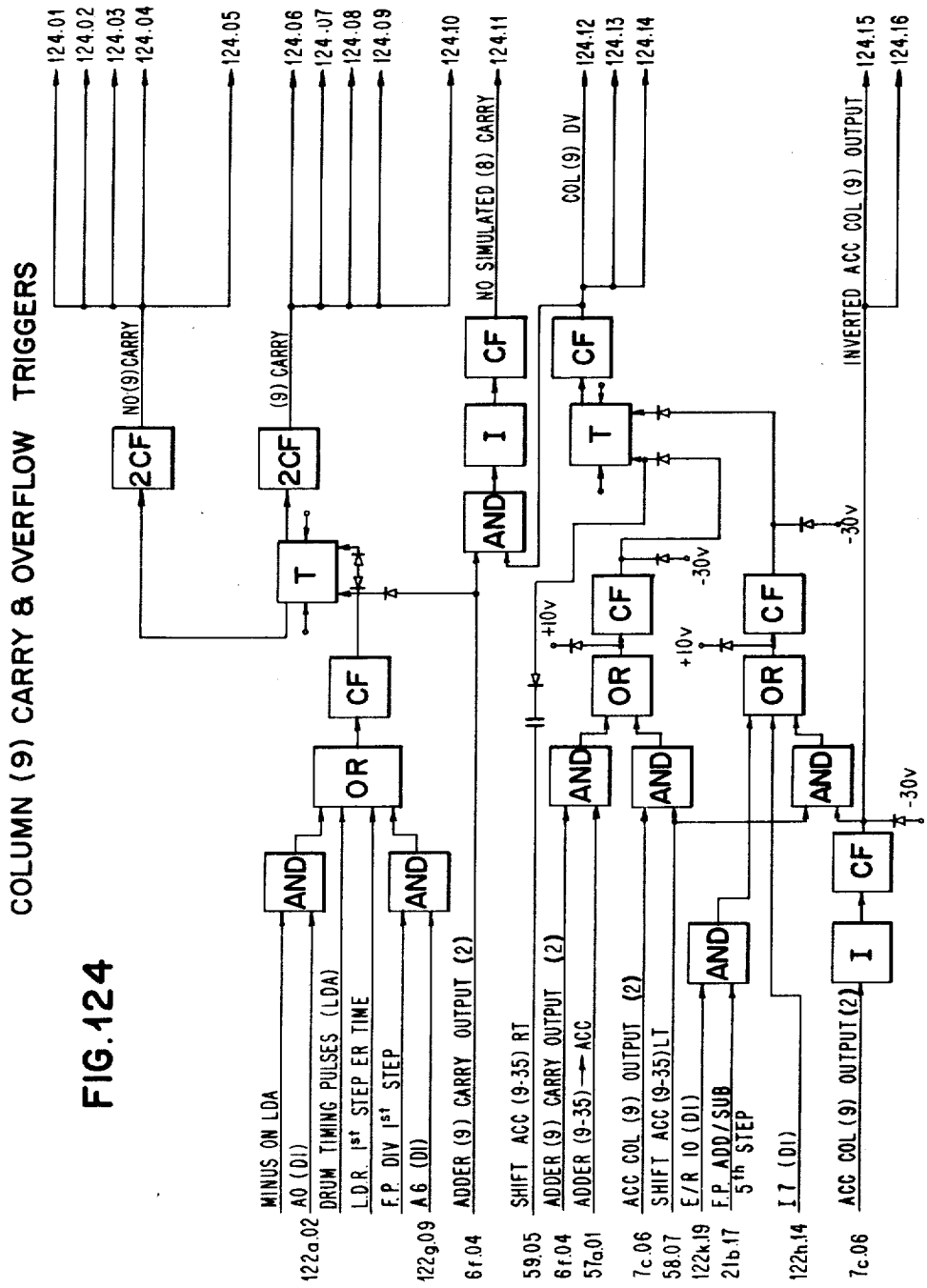

COLUMN (9) CARRY & OVERFLOW TRIGGERS
124.01
124.02
124.03
124.04
124.05
124.06
124.07
124.08
124.09
124.10
124.11
124.12
124.13
124.14
124.15
124.16
NO (9) CARRY
(9) CARRY
NO SIMULATED (8) CARRY
COL (9) DV
INVERTED ACC COL (9) OUTPUT
2CF
T
CF
I
AND
OR
+10v
-30v
MINUS ON LDA
122a.02 A0 (01)
DRUM TIMING PULSES (LDA)
L.D.R. 1st STEP ER TIME
F.P. DIV 1st STEP
122g.09 A6 (01)
6f.04 ADDER (9) CARRY OUTPUT (2)
59.05 SHIFT ACC (9-35) RT
6f.04 ADDER (9) CARRY OUTPUT (2)
57a.01 ADDER (9-35) → ACC
7c.06 ACC COL (9) OUTPUT (2)
58.07 SHIFT ACC (9-35) LT
122k.19 E/R 10 (01)
21b.17 F.P. ADD/SUB 5th STEP
122h.14 I 7 (01)
7c.06 ACC COL (9) OUTPUT (2)

FIG. 124

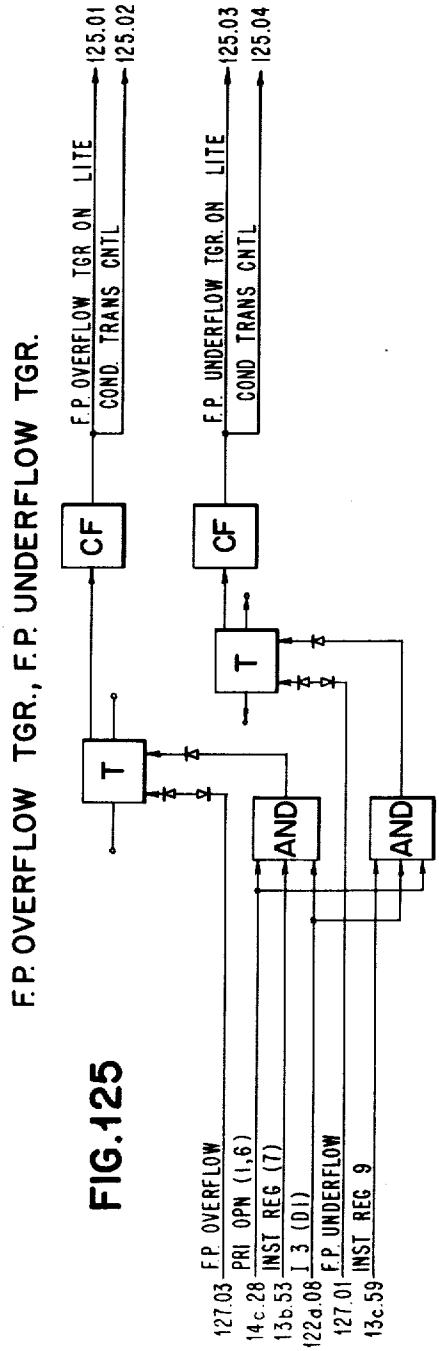


FIG.125

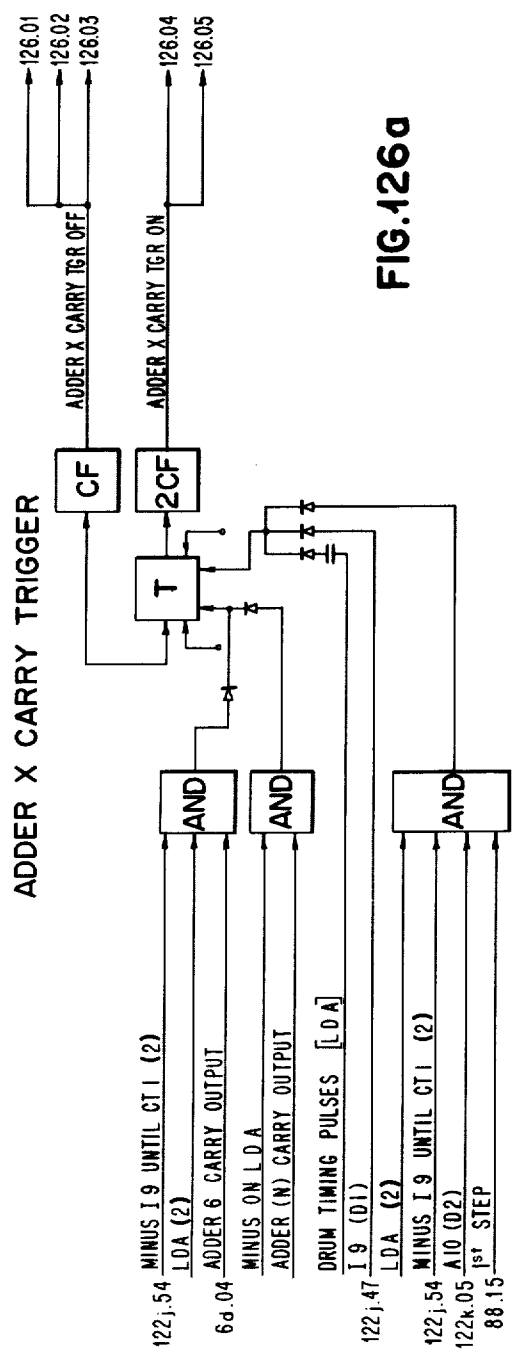


FIG.126a

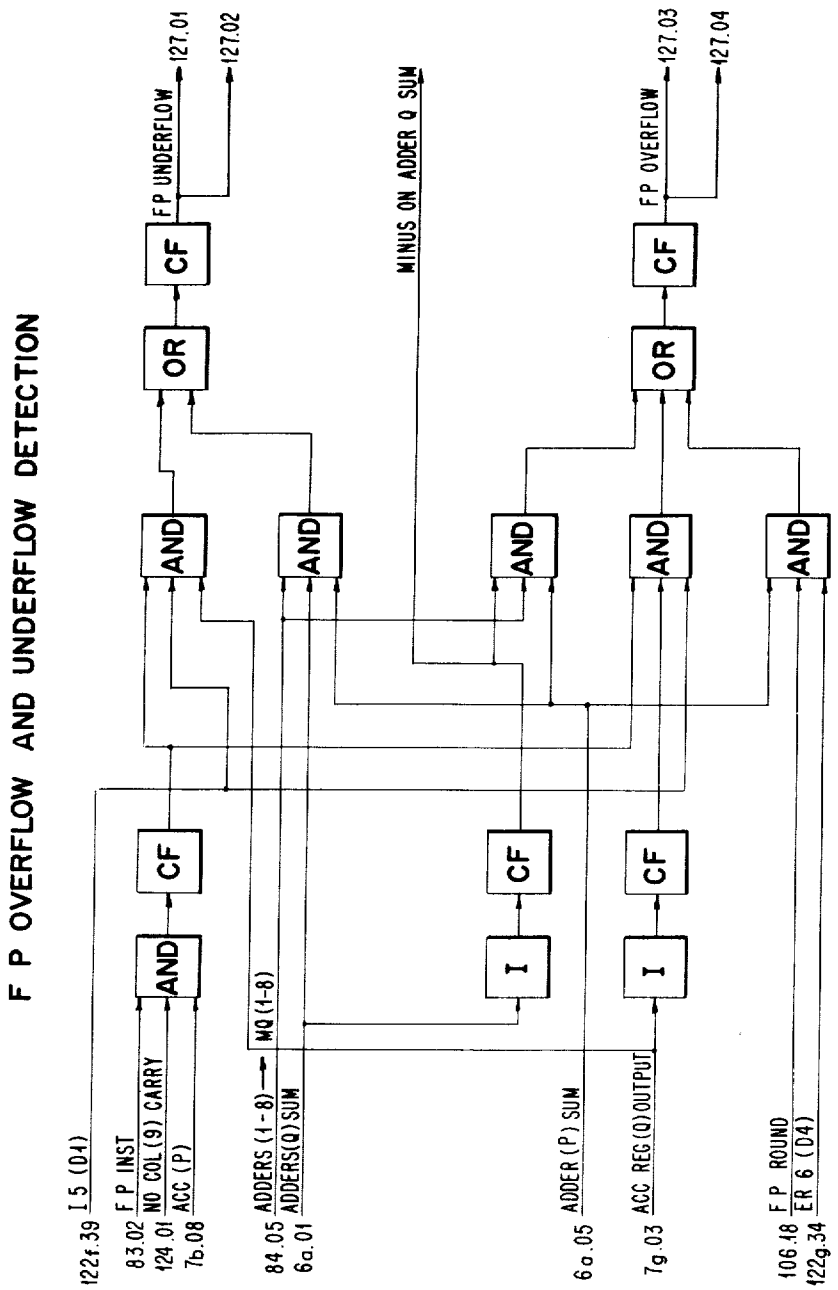
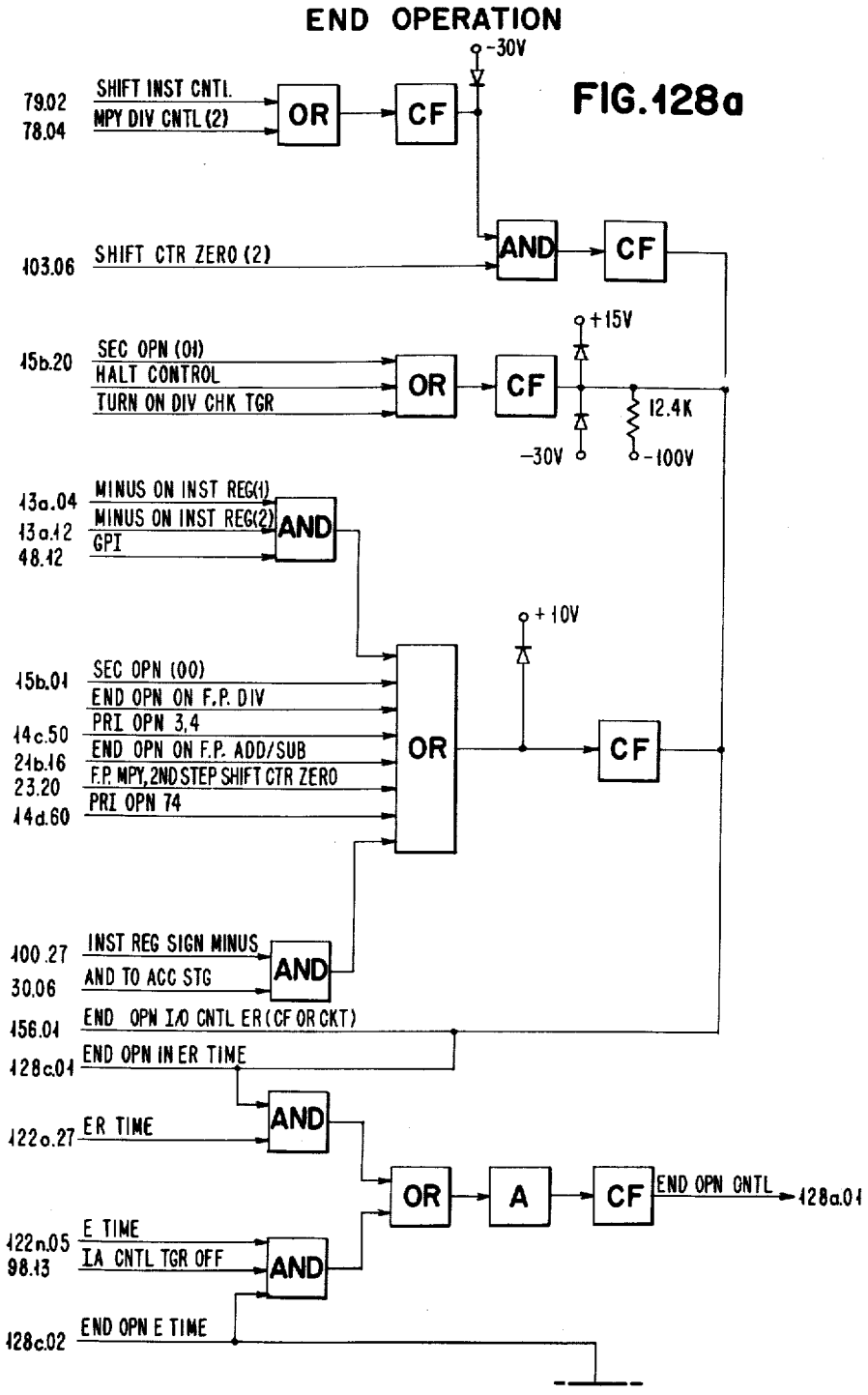

F P OVERFLOW AND UNDERFLOW DETECTION
122f.39 I 5 (04)
83.02 F P INST
124.01 NO COL (9) CARRY
7b.08 ACC (P)
84.05 ADDERS (1-8)
6a.01 ADDERS(Q) SUM
MQ (1-8)
MINUS ON ADDER Q SUM
6a.05 ADDER (P) SUM
7g.03 ACC REG (Q) OUTPUT
106.18 F P ROUND
122g.34 ER 6 (04)
AND
CF
I
OR
F P UNDERFLOW
127.01
127.02
F P OVERFLOW
127.03
127.04

FIG. 127

FIG. 128a


END OPERATION
-30V
79.02
78.04
SHIFT INST CNTL.
MPY DIV CNTL (2)
OR
CF
AND
CF
103.06
SHIFT CTR ZERO (2)
+15V
45b.20
SEC OPN (01)
HALT CONTROL
TURN ON DIV CHK TGR
OR
CF
12.4K
-30V
-100V
43a.04
43a.12
48.12
MINUS ON INST REG(1)
MINUS ON INST REG(2)
GPI
AND
+10V
45b.01
14c.50
24b.16
23.20
14d.60
SEC OPN (00)
END OPN ON F.P. DIV
PRI OPN 3,4
END OPN ON F.P. ADD/SUB
F.P. MPY, 2ND STEP SHIFT CTR ZERO
PRI OPN 74
OR
CF
100.27
30.06
INST REG SIGN MINUS
AND TO ACC STG
AND
156.04
END OPN I/O CNTL ER (CF OR CKT)
128c.04
END OPN IN ER TIME
122a.27
ER TIME
AND
OR
A
CF
END OPN CNTL
128a.04
122n.05
98.13
E TIME
IA CNTL TGR OFF
AND
128c.02
END OPN E TIME

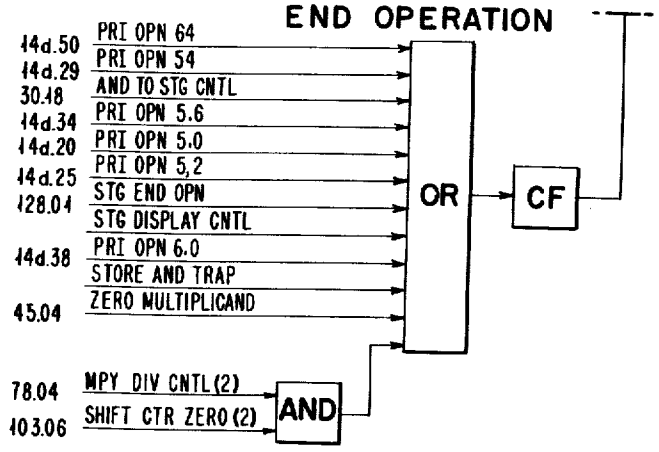


FIG. 128a

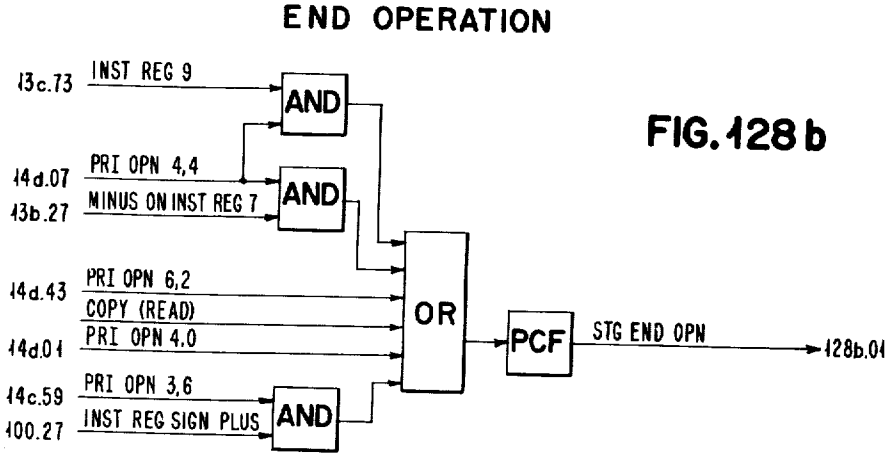


FIG. 128b

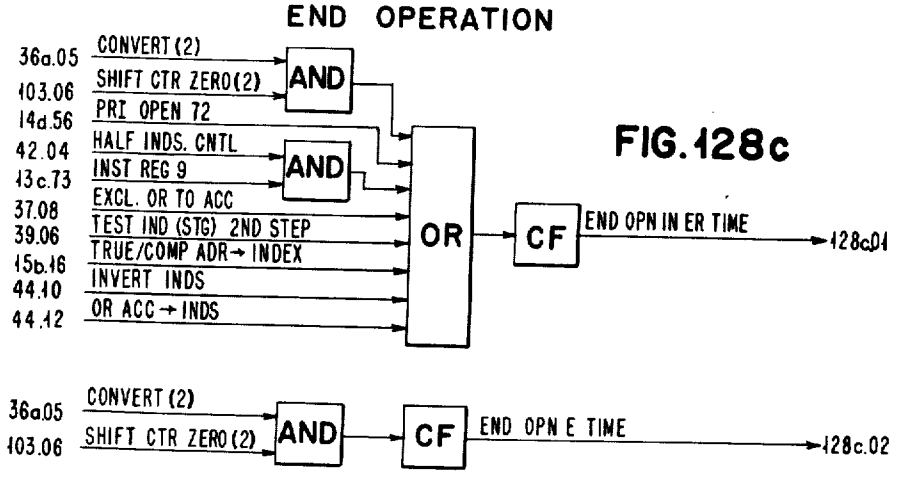


FIG. 128c

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FIG. 129a STORAGE ADDRESS REGISTER

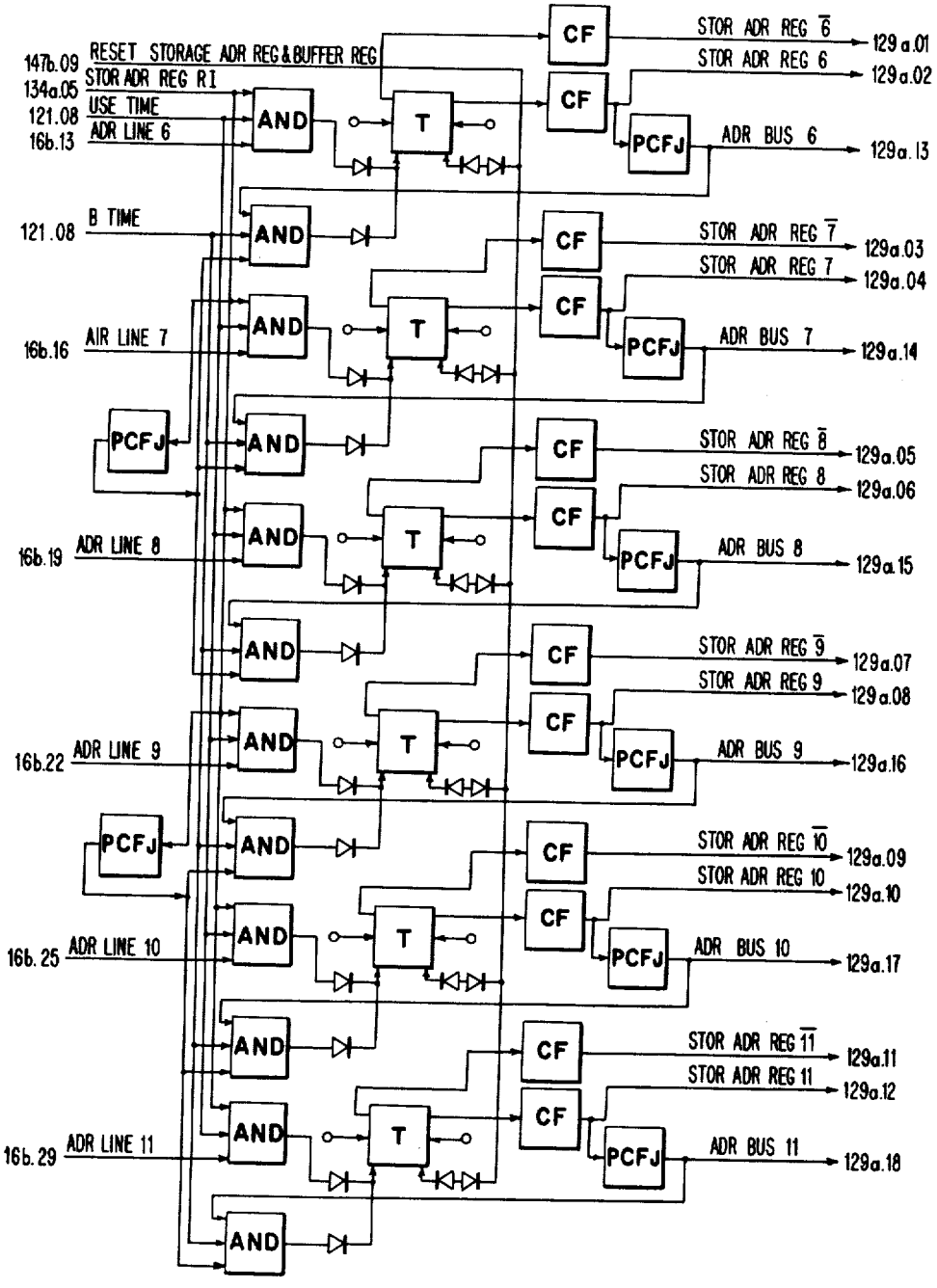

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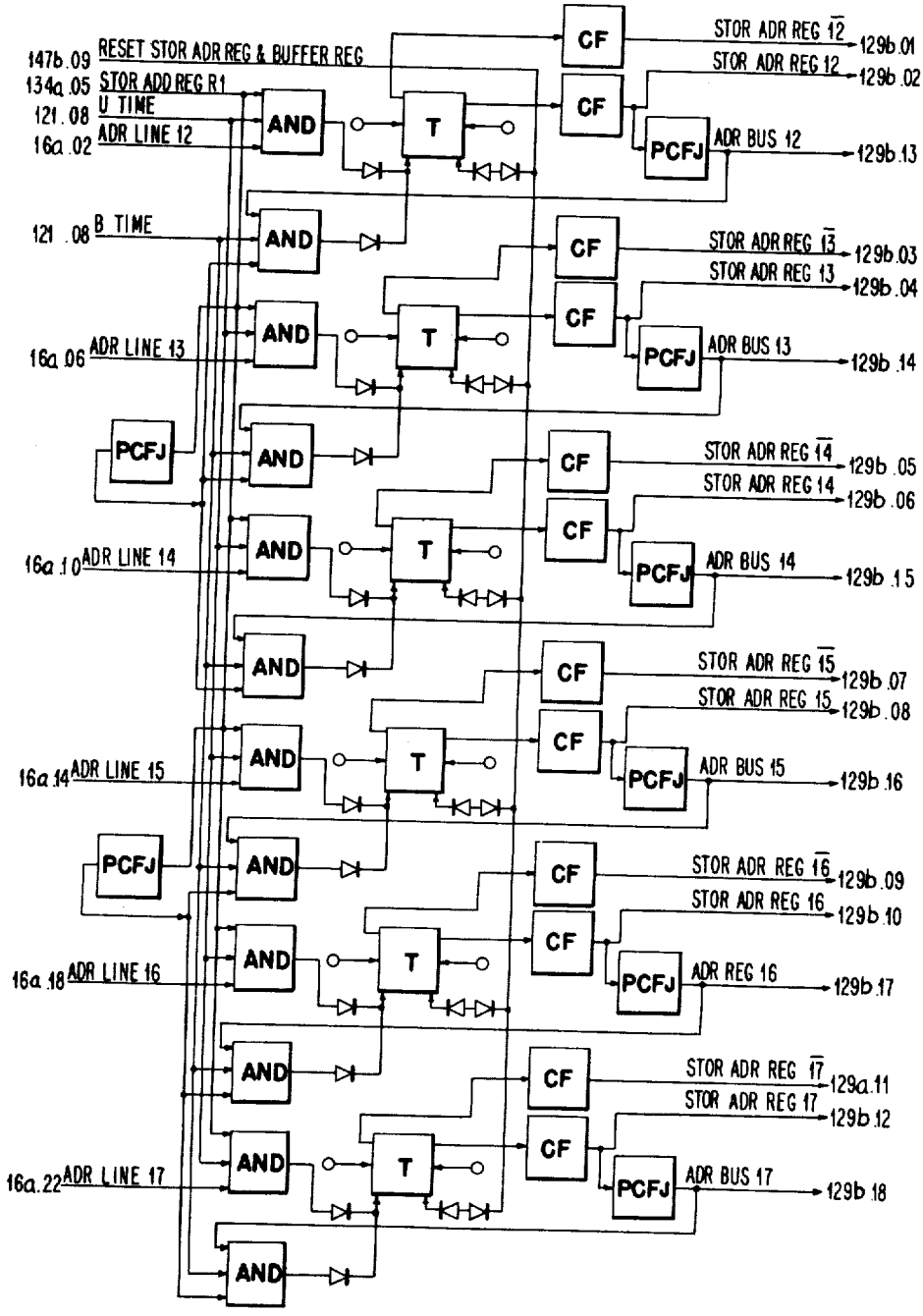
FIG. 129b



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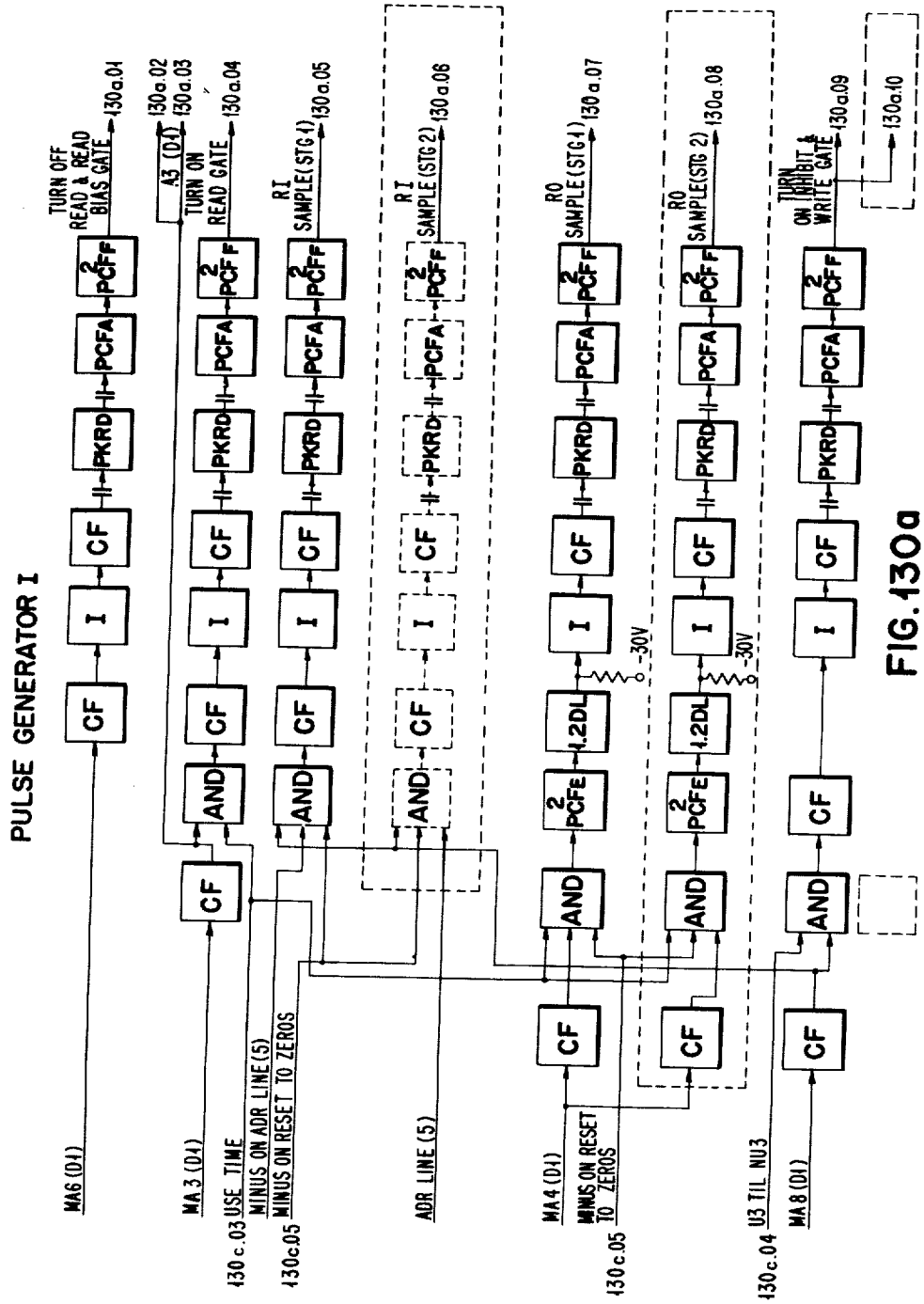

FIG. 130a

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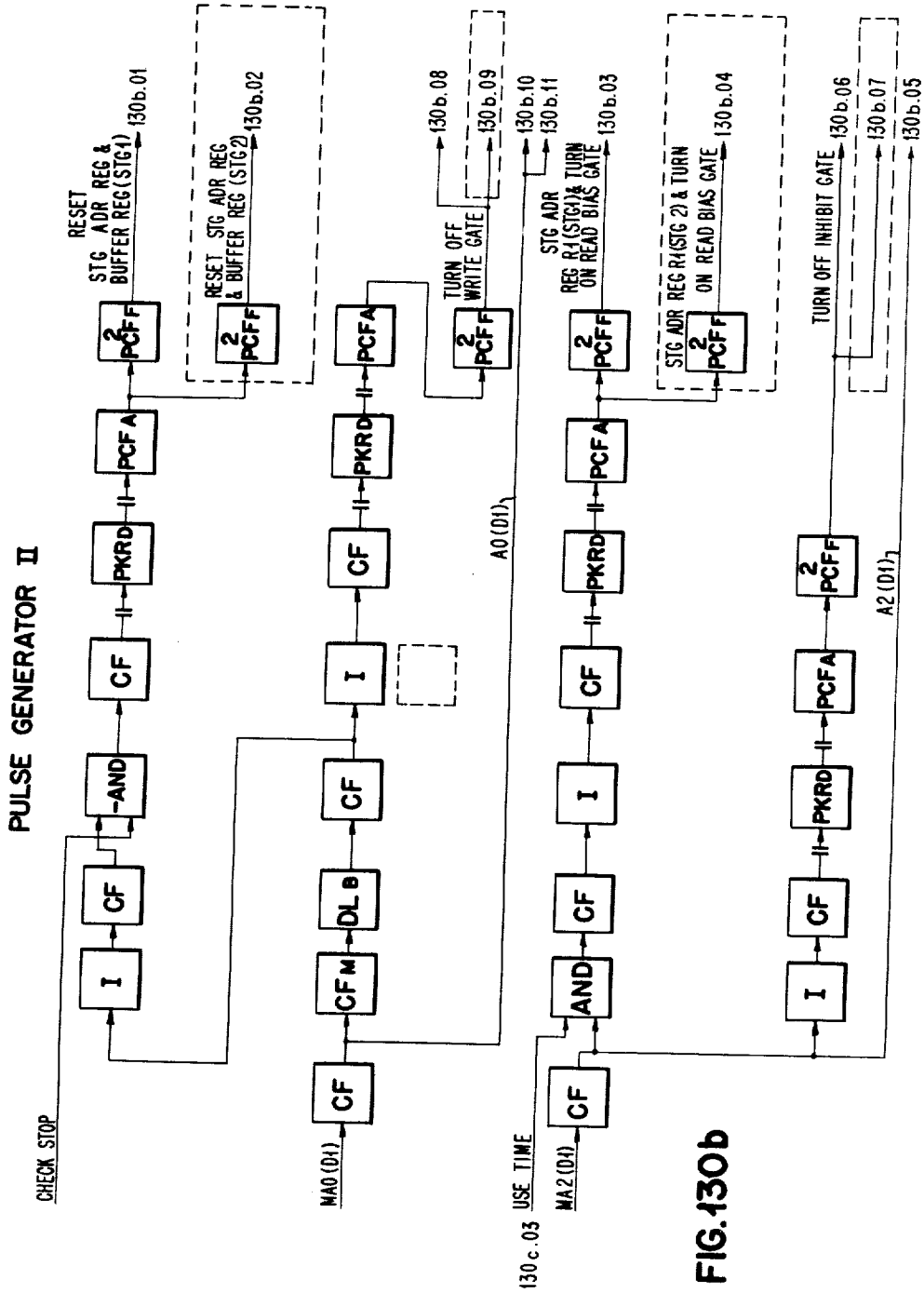

FIG. 130b

FIG. 131a

ADDRESS DECODER CIRCUIT

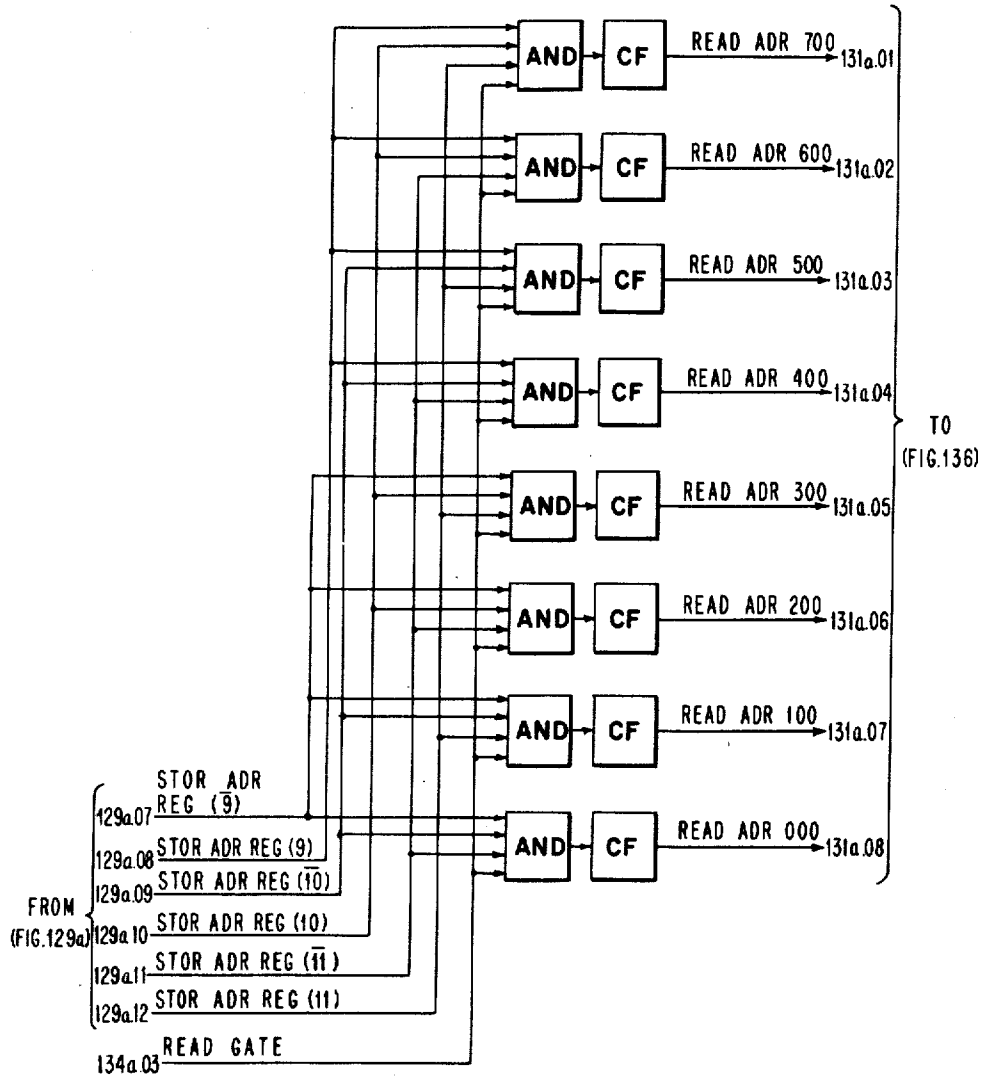

FIG. 131b

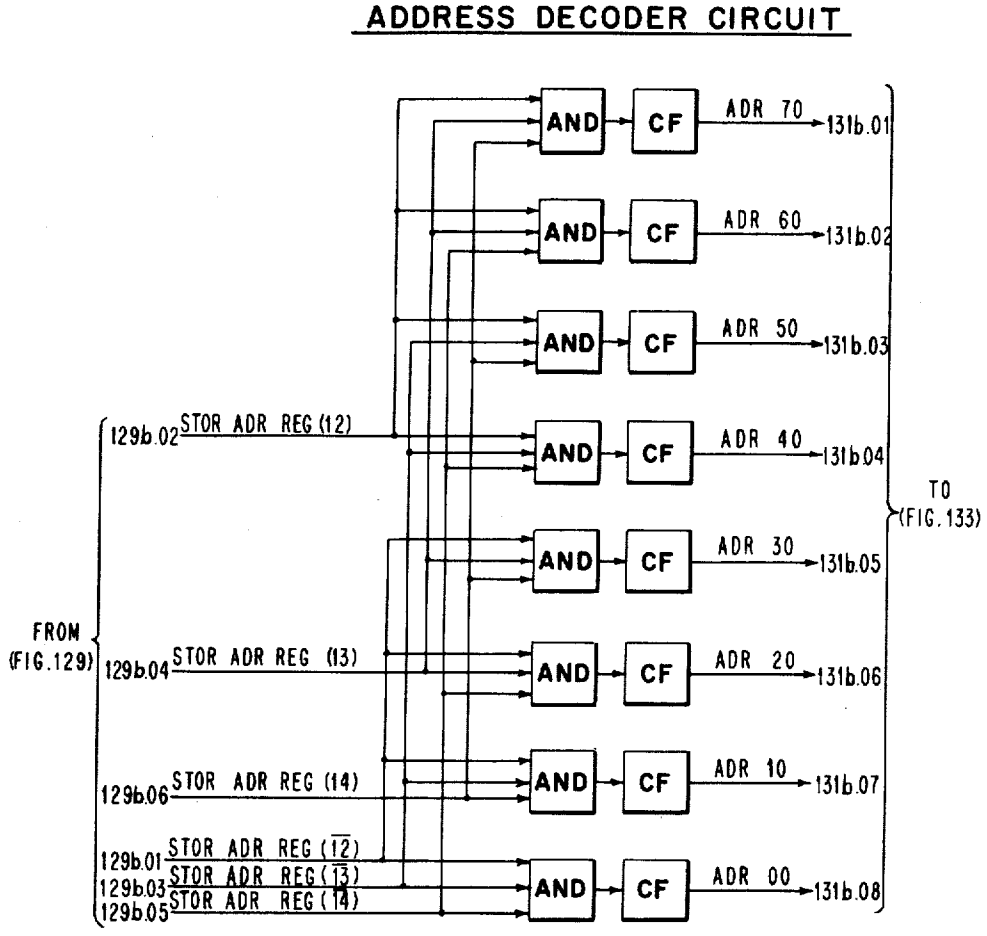
ADDRESS DECODER CIRCUIT
AND
CF
ADR 70
131b.01
ADR 60
131b.02
ADR 50
131b.03
ADR 40
131b.04
ADR 30
131b.05
ADR 20
131b.06
ADR 10
131b.07
ADR 00
131b.08
TO (FIG. 133)
FROM (FIG. 129)
129b.02 STOR ADR REG (12)
129b.04 STOR ADR REG (13)
129b.06 STOR ADR REG (14)
129b.01 STOR ADR REG (12)
129b.03 STOR ADR REG (13)
129b.05 STOR ADR REG (14)

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FIG. 132a

ADDRESS DECODER CIRCUIT

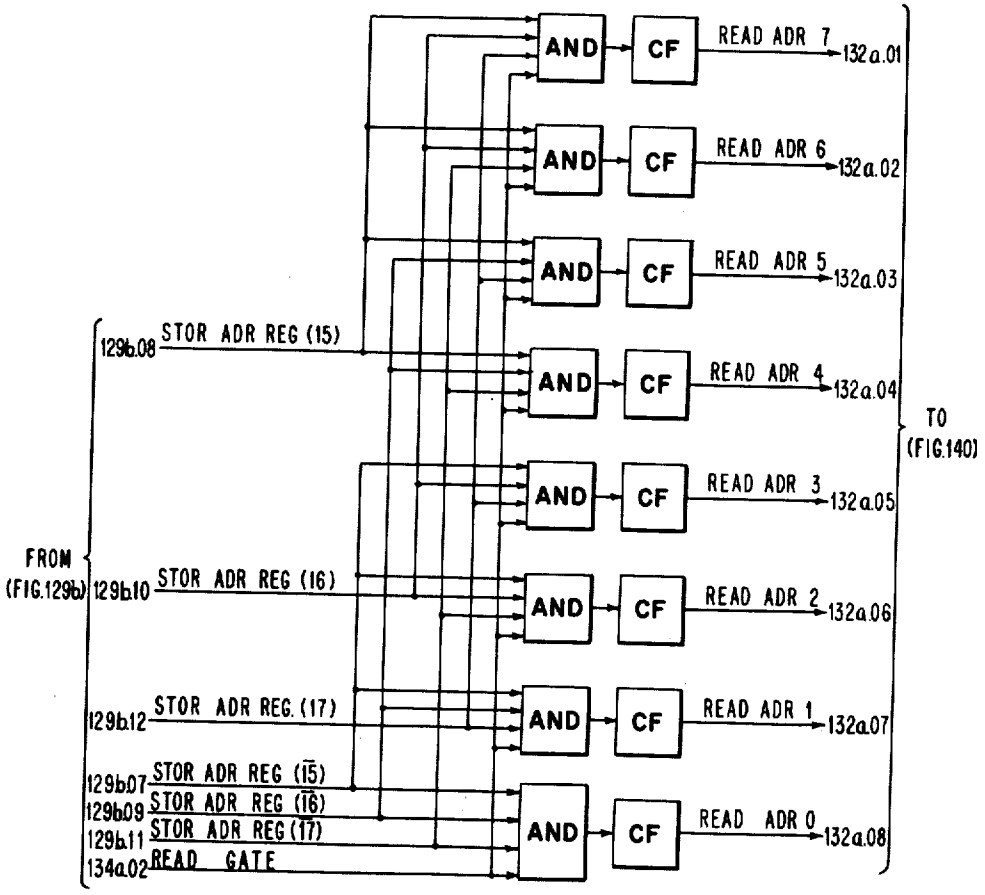
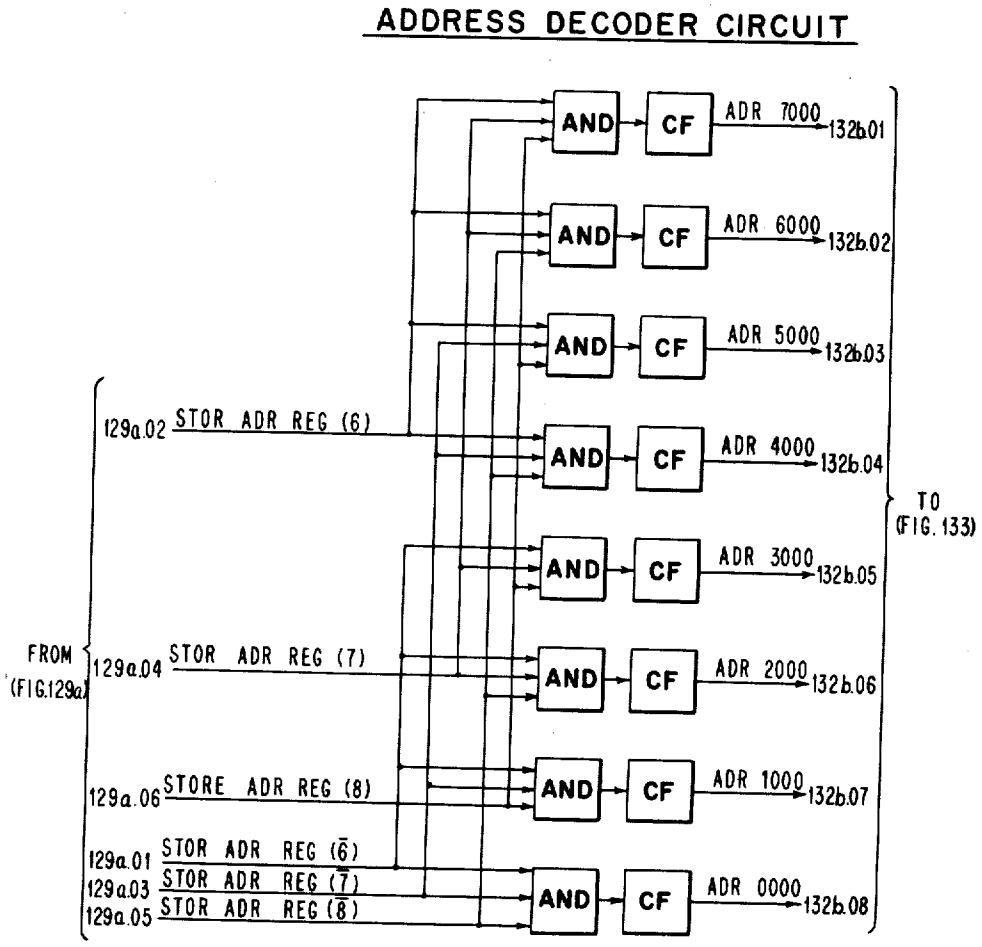


FIG. 132b


ADDRESS DECODER CIRCUIT
AND
CF
ADR 7000
132b.01
ADR 6000
132b.02
ADR 5000
132b.03
ADR 4000
132b.04
ADR 3000
132b.05
ADR 2000
132b.06
ADR 1000
132b.07
ADR 0000
132b.08
TO (FIG. 133)
FROM (FIG. 129a)
129a.02 STOR ADR REG (6)
129a.04 STOR ADR REG (7)
129a.06 STORE ADR REG (8)
129a.01 STOR ADR REG (6̄)
129a.03 STOR ADR REG (7̄)
129a.05 STOR ADR REG (8̄)

WRITE DRIVER SELECT CIRCUITS

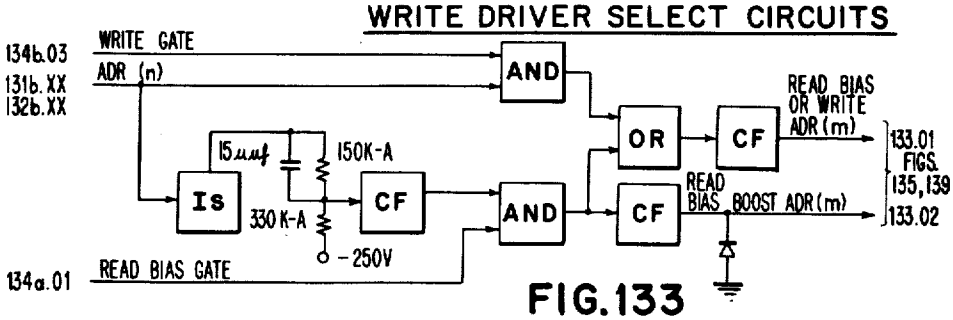


FIG.133

FIG.135 X MATRIX SWITCH WRITE DRIVER

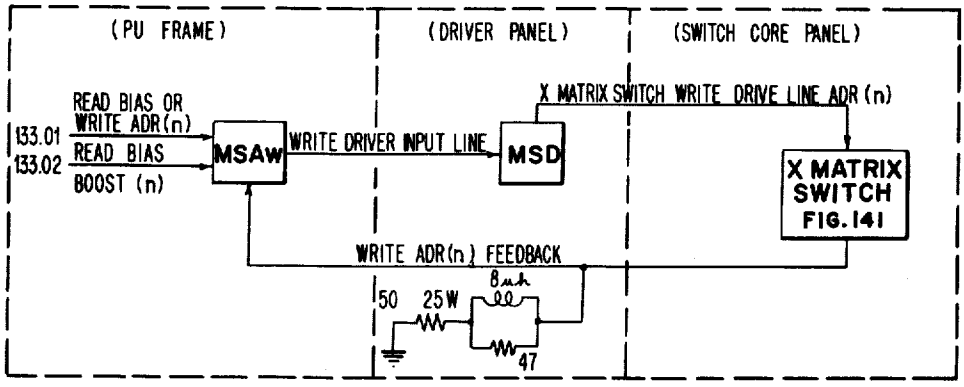
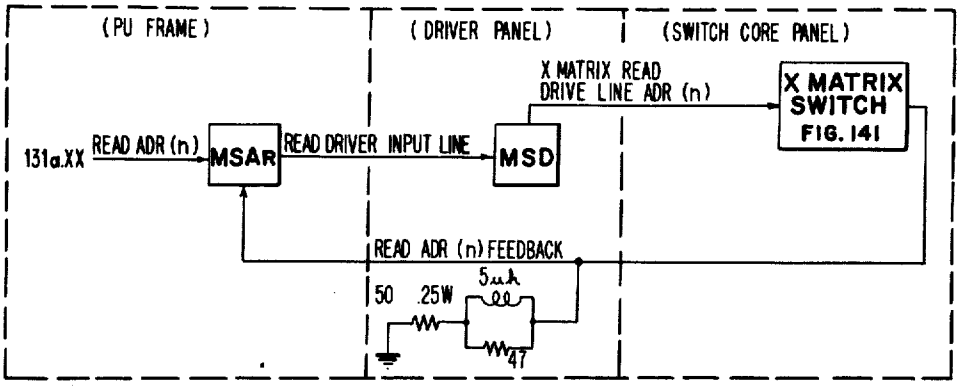


FIG.136 X MATRIX SWITCH READ DRIVER



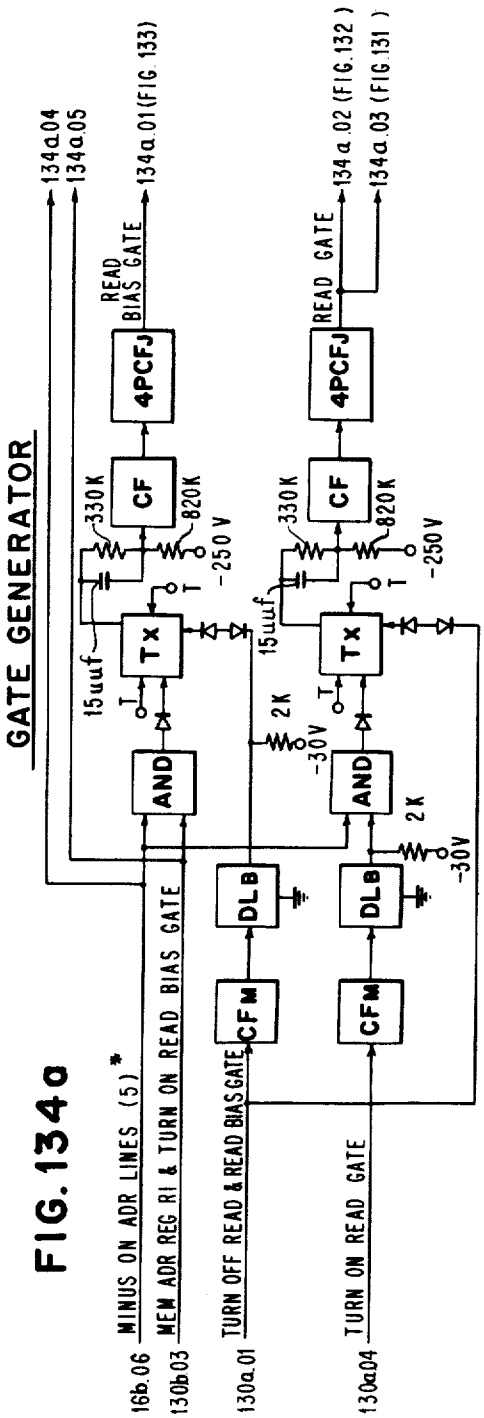


FIG. 134a

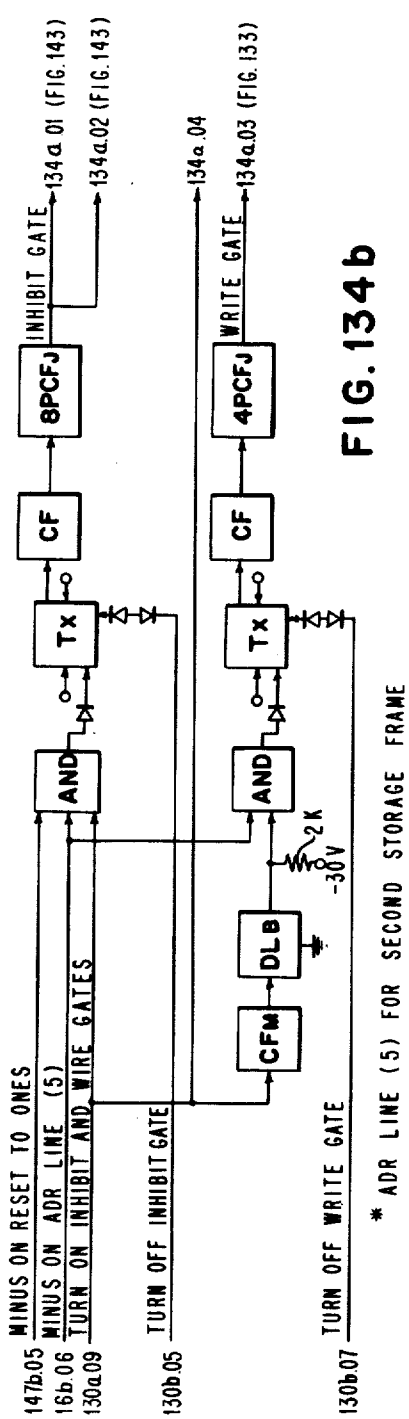


FIG. 134b

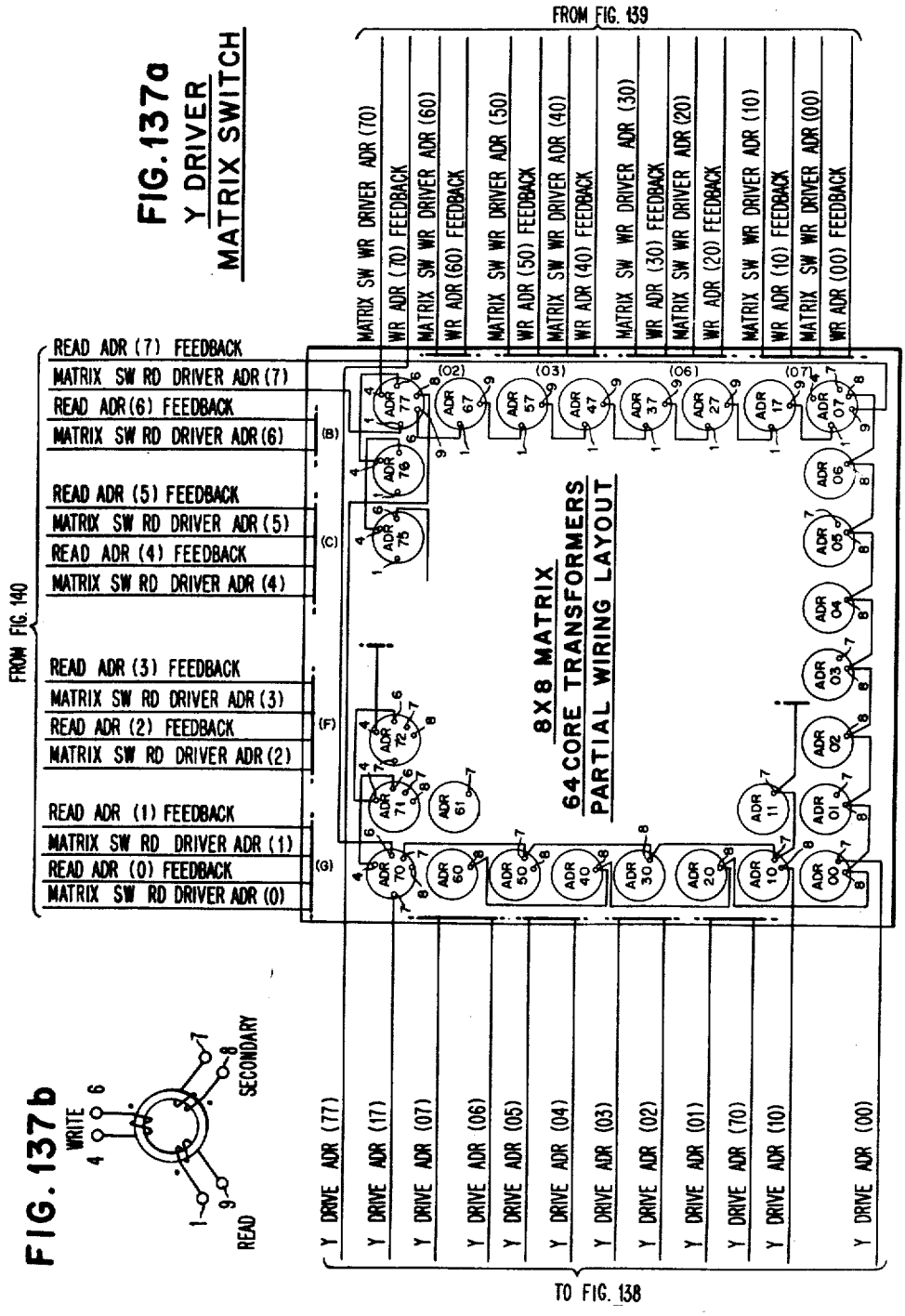


FIG. 137a
Y DRIVER
MATRIX SWITCH
FROM FIG. 139
MATRIX SW WR DRIVER ADR (70)
WR ADR (70) FEEDBACK
MATRIX SW WR DRIVER ADR (60)
WR ADR (60) FEEDBACK
MATRIX SW WR DRIVER ADR (50)
WR ADR (50) FEEDBACK
MATRIX SW WR DRIVER ADR (40)
WR ADR (40) FEEDBACK
MATRIX SW WR DRIVER ADR (30)
WR ADR (30) FEEDBACK
MATRIX SW WR DRIVER ADR (20)
WR ADR (20) FEEDBACK
MATRIX SW WR DRIVER ADR (10)
WR ADR (10) FEEDBACK
MATRIX SW WR DRIVER ADR (00)
WR ADR (00) FEEDBACK
FROM FIG. 140
READ ADR (7) FEEDBACK
MATRIX SW RD DRIVER ADR (7)
READ ADR (6) FEEDBACK
MATRIX SW RD DRIVER ADR (6)
READ ADR (5) FEEDBACK
MATRIX SW RD DRIVER ADR (5)
READ ADR (4) FEEDBACK
MATRIX SW RD DRIVER ADR (4)
READ ADR (3) FEEDBACK
MATRIX SW RD DRIVER ADR (3)
READ ADR (2) FEEDBACK
MATRIX SW RD DRIVER ADR (2)
READ ADR (1) FEEDBACK
MATRIX SW RD DRIVER ADR (1)
READ ADR (0) FEEDBACK
MATRIX SW RD DRIVER ADR (0)
(B)
(C)
(F)
(G)
8X8 MATRIX
64 CORE TRANSFORMERS
PARTIAL WIRING LAYOUT
(02)
(03)
(06)
(07)
FIG. 137b
WRITE
SECONDARY
READ
Y DRIVE ADR (77)
Y DRIVE ADR (17)
Y DRIVE ADR (07)
Y DRIVE ADR (06)
Y DRIVE ADR (05)
Y DRIVE ADR (04)
Y DRIVE ADR (03)
Y DRIVE ADR (02)
Y DRIVE ADR (01)
Y DRIVE ADR (70)
Y DRIVE ADR (10)
Y DRIVE ADR (00)
TO FIG. 138

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FIG.138b

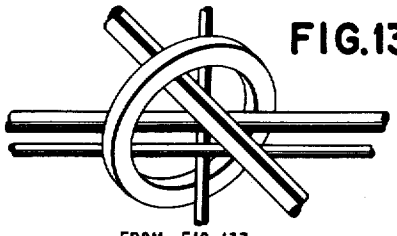


FIG.138a

CORE ARRAY

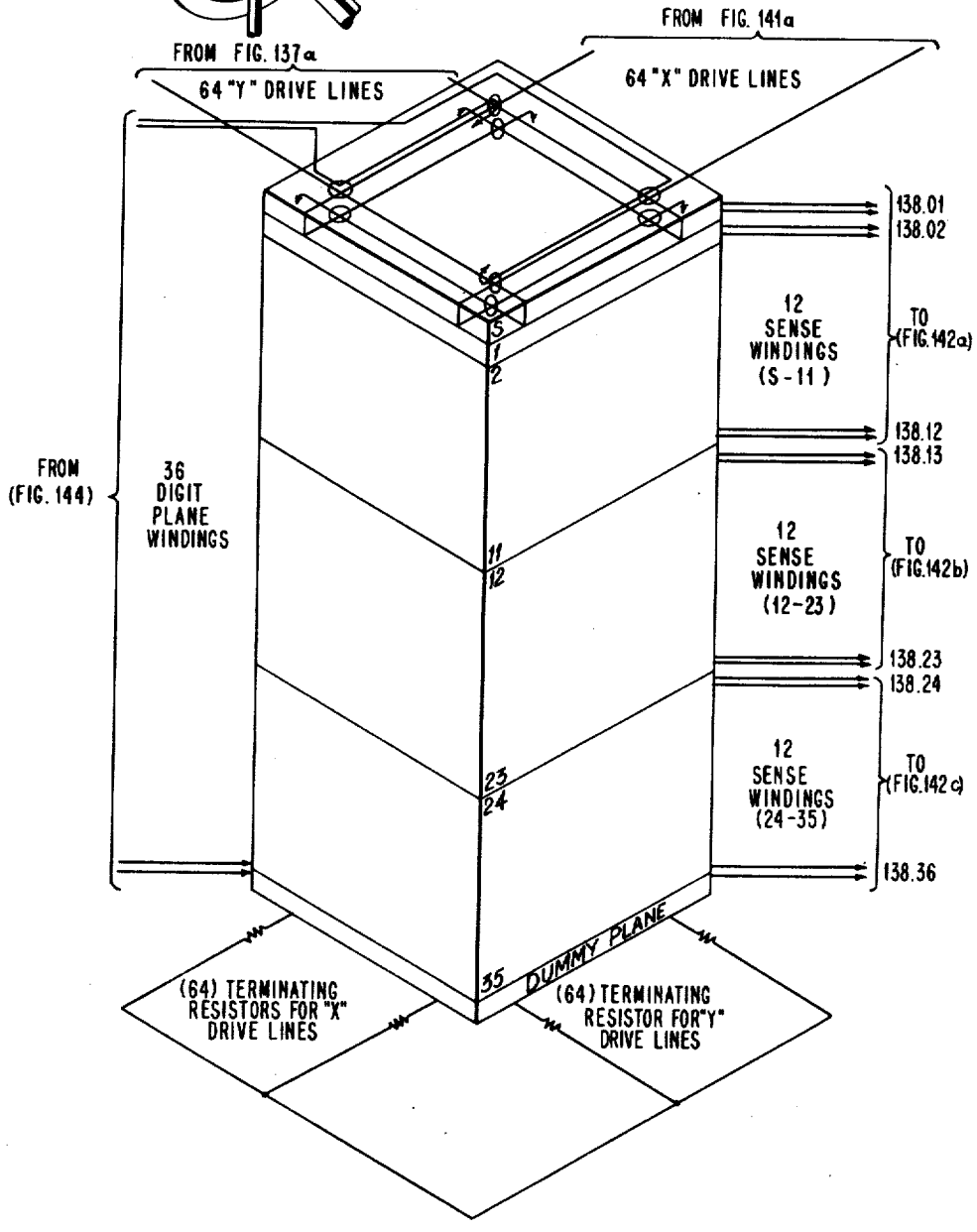


FIG. 139 Y MATRIX SWITCH WRITE DRIVER

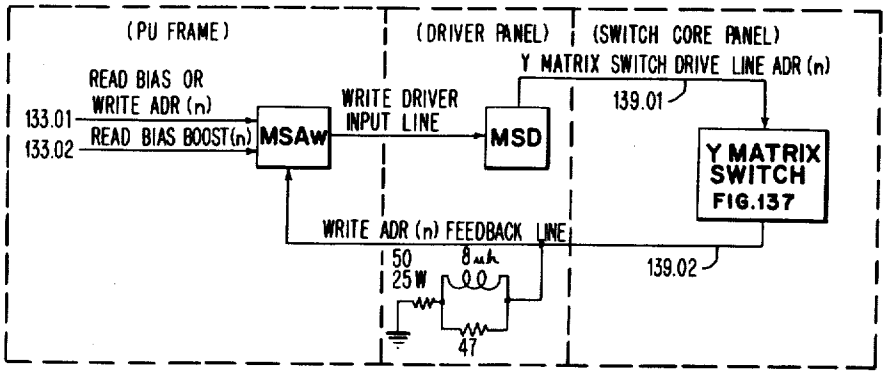


FIG. 140 Y MATRIX SWITCH READ DRIVER

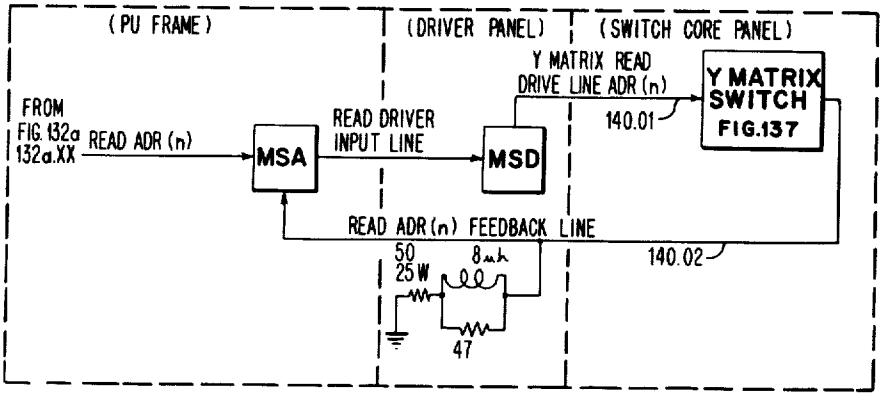
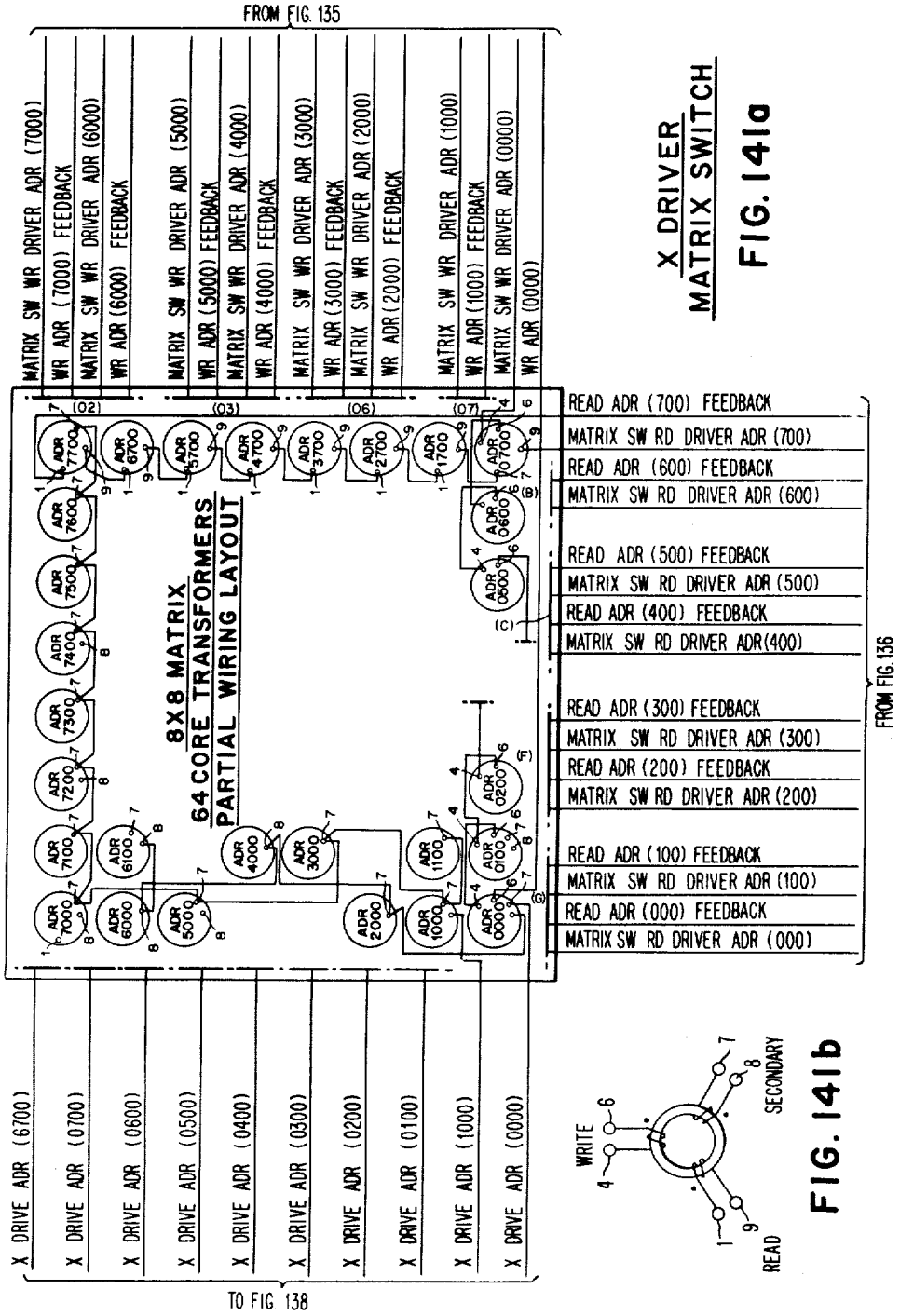


FIG. 143 DIGIT PLANE SELECT CIRCUITS


FROM FIG. 135
MATRIX SW WR DRIVER ADR (7000)
WR ADR (7000) FEEDBACK
MATRIX SW WR DRIVER ADR (6000)
WR ADR (6000) FEEDBACK
MATRIX SW WR DRIVER ADR (5000)
WR ADR (5000) FEEDBACK
MATRIX SW WR DRIVER ADR (4000)
WR ADR (4000) FEEDBACK
MATRIX SW WR DRIVER ADR (3000)
WR ADR (3000) FEEDBACK
MATRIX SW WR DRIVER ADR (2000)
WR ADR (2000) FEEDBACK
MATRIX SW WR DRIVER ADR (1000)
WR ADR (1000) FEEDBACK
MATRIX SW WR DRIVER ADR (0000)
WR ADR (0000)
X DRIVER MATRIX SWITCH
FIG. 141a
8X8 MATRIX
64 CORE TRANSFORMERS
PARTIAL WIRING LAYOUT
READ ADR (700) FEEDBACK
MATRIX SW RD DRIVER ADR (700)
READ ADR (600) FEEDBACK
MATRIX SW RD DRIVER ADR (600)
READ ADR (500) FEEDBACK
MATRIX SW RD DRIVER ADR (500)
READ ADR (400) FEEDBACK
MATRIX SW RD DRIVER ADR(400)
READ ADR (300) FEEDBACK
MATRIX SW RD DRIVER ADR (300)
READ ADR (200) FEEDBACK
MATRIX SW RD DRIVER ADR (200)
READ ADR (100) FEEDBACK
MATRIX SW RD DRIVER ADR (100)
READ ADR (000) FEEDBACK
MATRIX SW RD DRIVER ADR (000)
FROM FIG. 136
X DRIVE ADR (6700)
X DRIVE ADR (0700)
X DRIVE ADR (0600)
X DRIVE ADR (0500)
X DRIVE ADR (0400)
X DRIVE ADR (0300)
X DRIVE ADR (0200)
X DRIVE ADR (0100)
X DRIVE ADR (1000)
X DRIVE ADR (0000)
TO FIG. 138
WRITE
SECONDARY
READ
FIG. 141b

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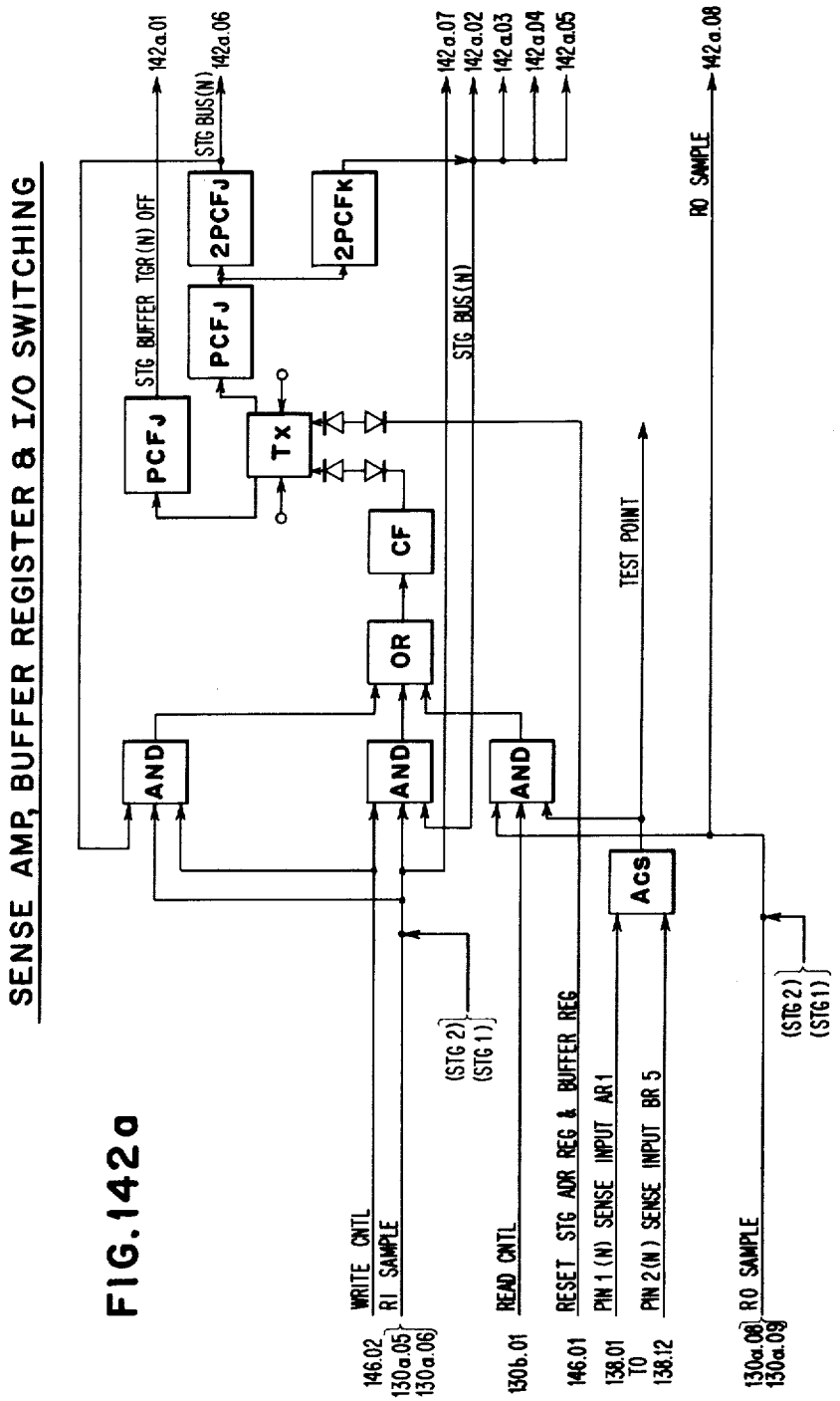

FIG. 142a

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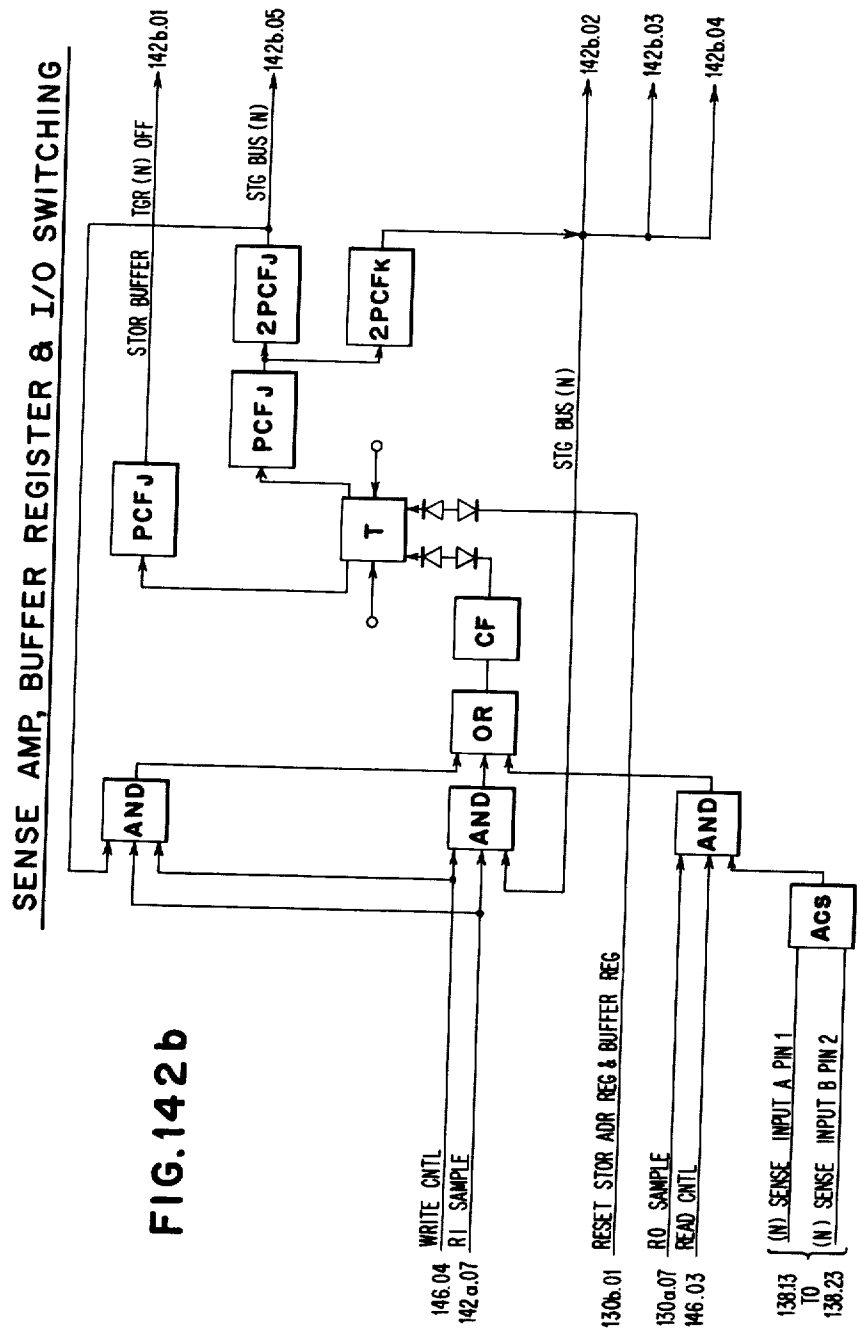


FIG. 142b

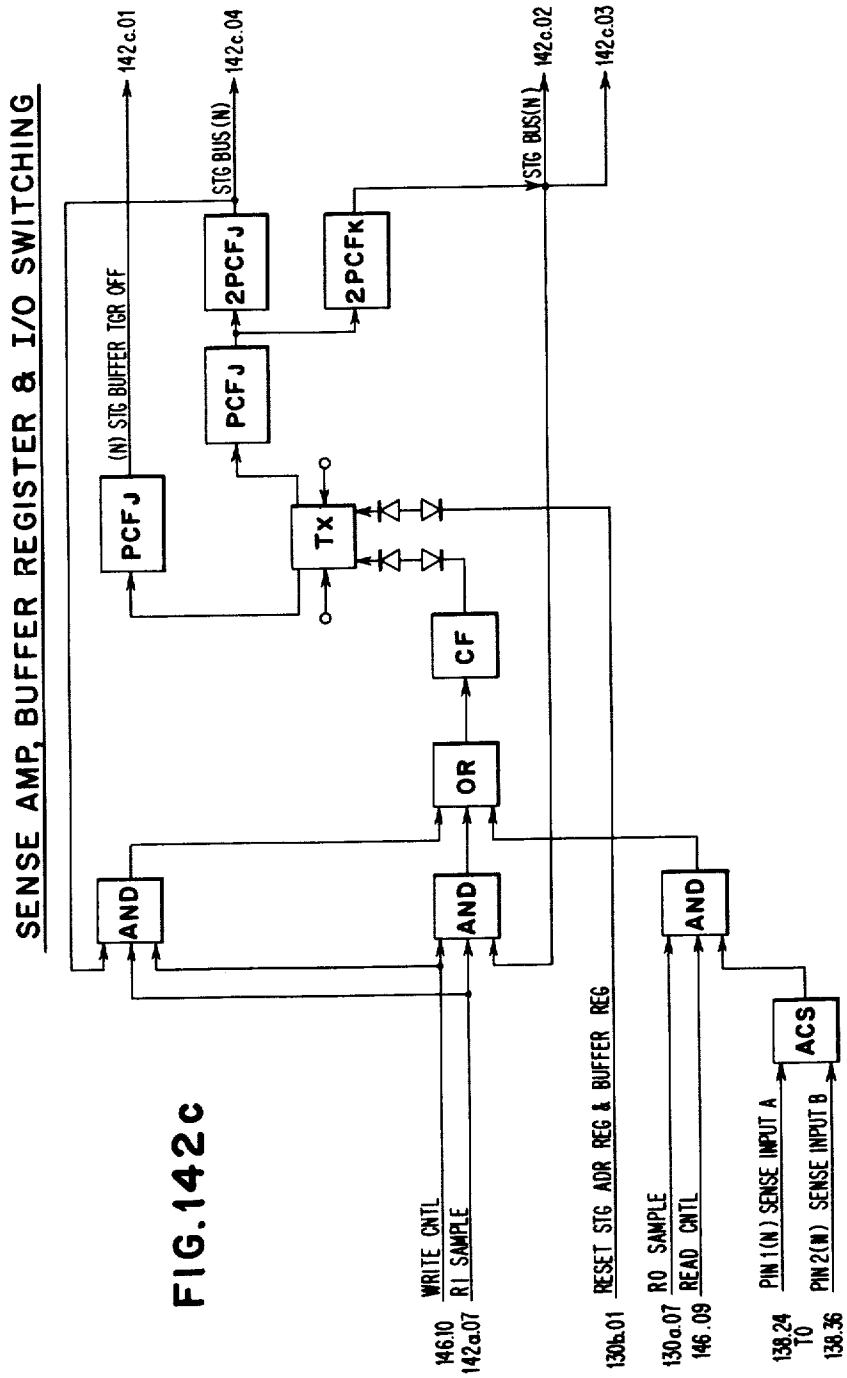

SENSE AMP, BUFFER REGISTER & I/O SWITCHING
142c.01
142c.04
142c.02
142c.03
STG BUS(N)
STG BUS(N')
(N) STG BUFFER TGR OFF
2PCFJ
2PCFK
PCFJ
PCFJ
TX
CF
OR
AND
AND
AND
ACS
WRITE CNTL
R1 SAMPLE
146.10
142a.07
RESET STG ADR REG & BUFFER REG
130b.01
R0 SAMPLE
READ CNTL
130a.07
146.09
PIN 1(N') SENSE INPUT A
PIN 2(N') SENSE INPUT B
138.24
TO
138.36

FIG. 142c

FIG.147c

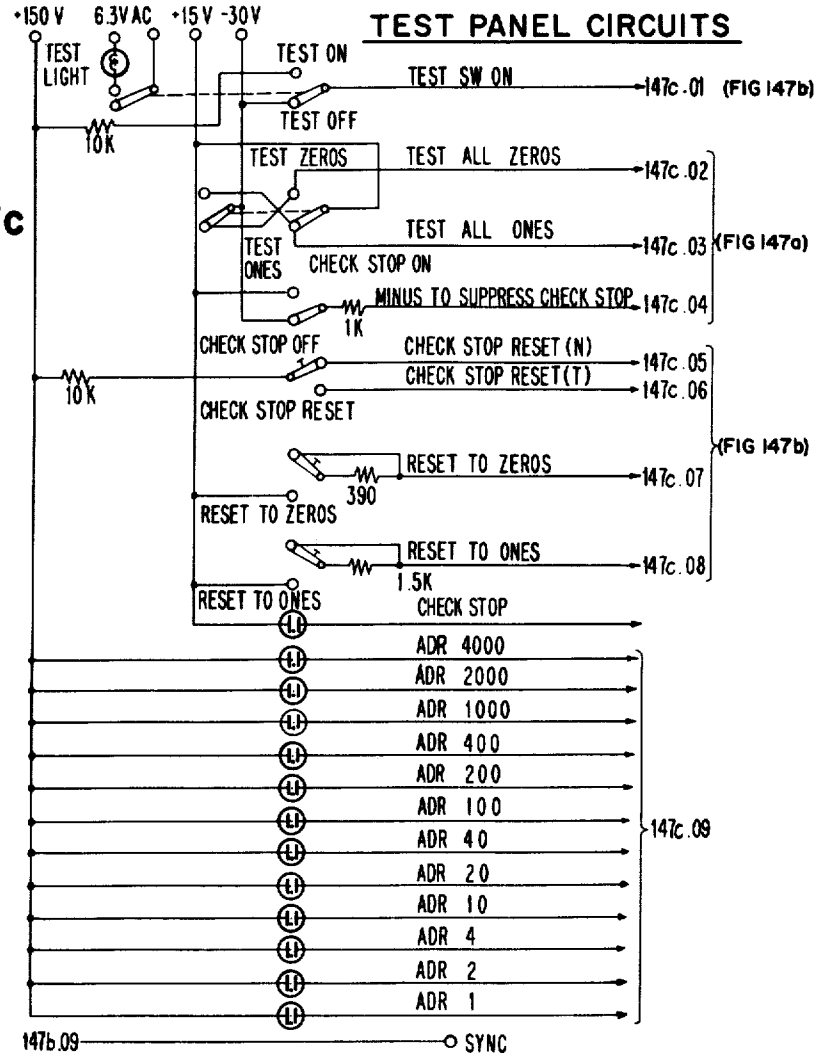


FIG.144 DIGIT PLANE DRIVER

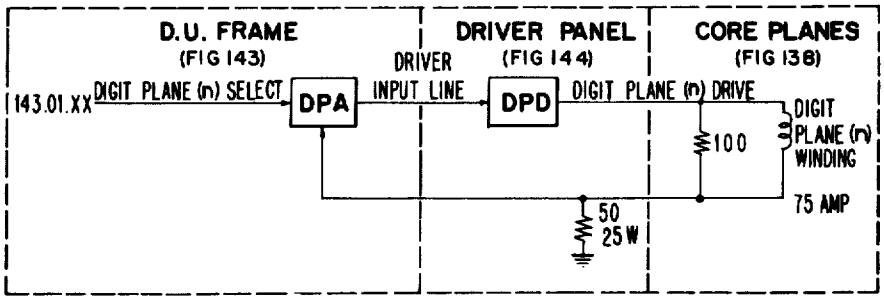


FIG. 145

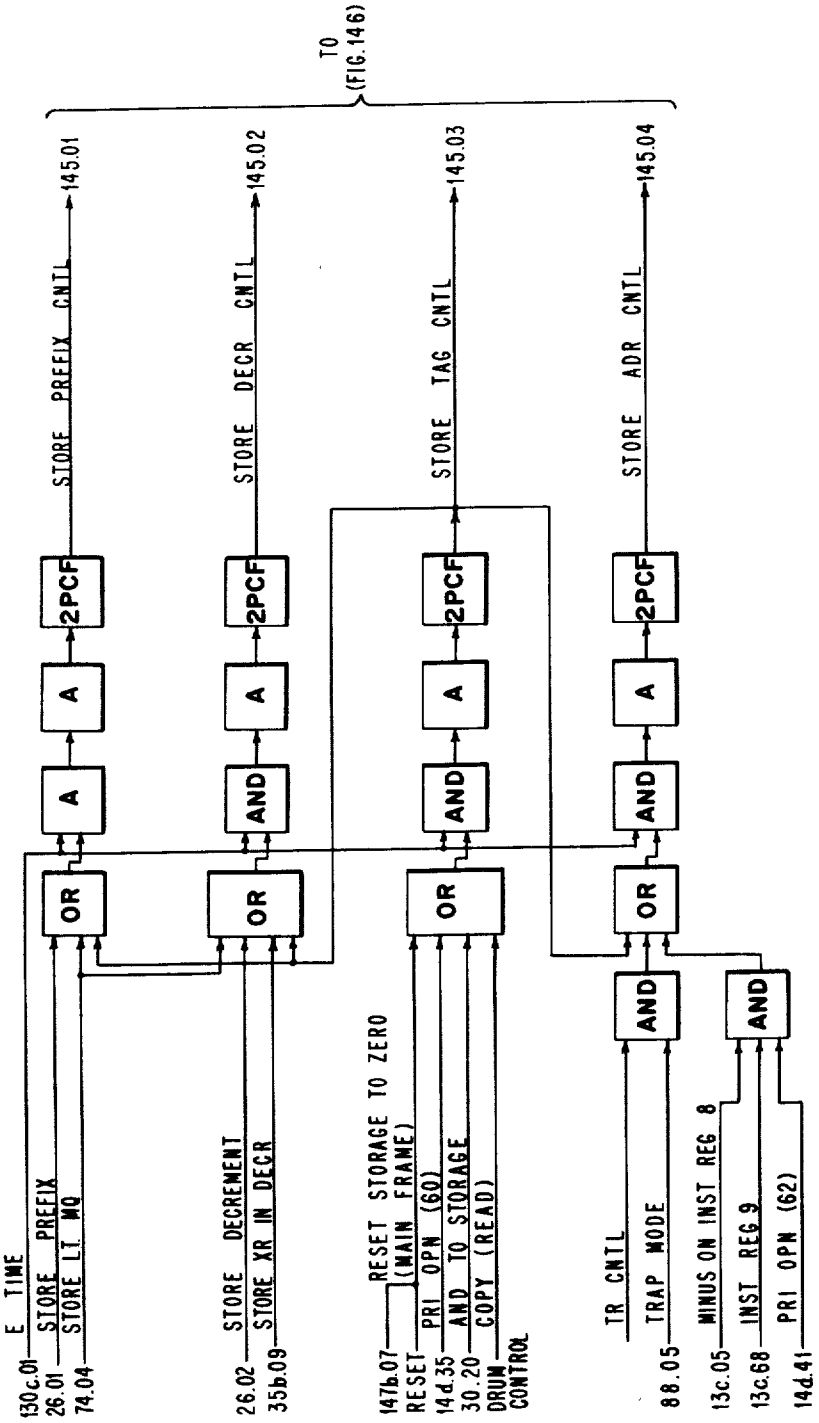

ADDRESS & OPERATION CONTROL
TO (FIG. 146)
STORE PREFIX CNTL
145.01
STORE DECR CNTL
145.02
STORE TAG CNTL
145.03
STORE ADR CNTL
145.04
2PCF
A
OR
AND
E TIME
130c.01
STORE PREFIX
26.01
STORE LT MQ
74.04
STORE DECREMENT
26.02
STORE XR IN DECR
35b.09
RESET STORAGE TO ZERO
147b.07
(MAIN FRAME)
RESET
PRI OPN (60)
14d.35
AND TO STORAGE
30.20
COPY (READ)
DRUM CONTROL
TR CNTL
TRAP MODE
88.05
MINUS ON INST REG 8
13c.05
INST REG 9
13c.68
PRI OPN (62)
14d.41

FIG. 146

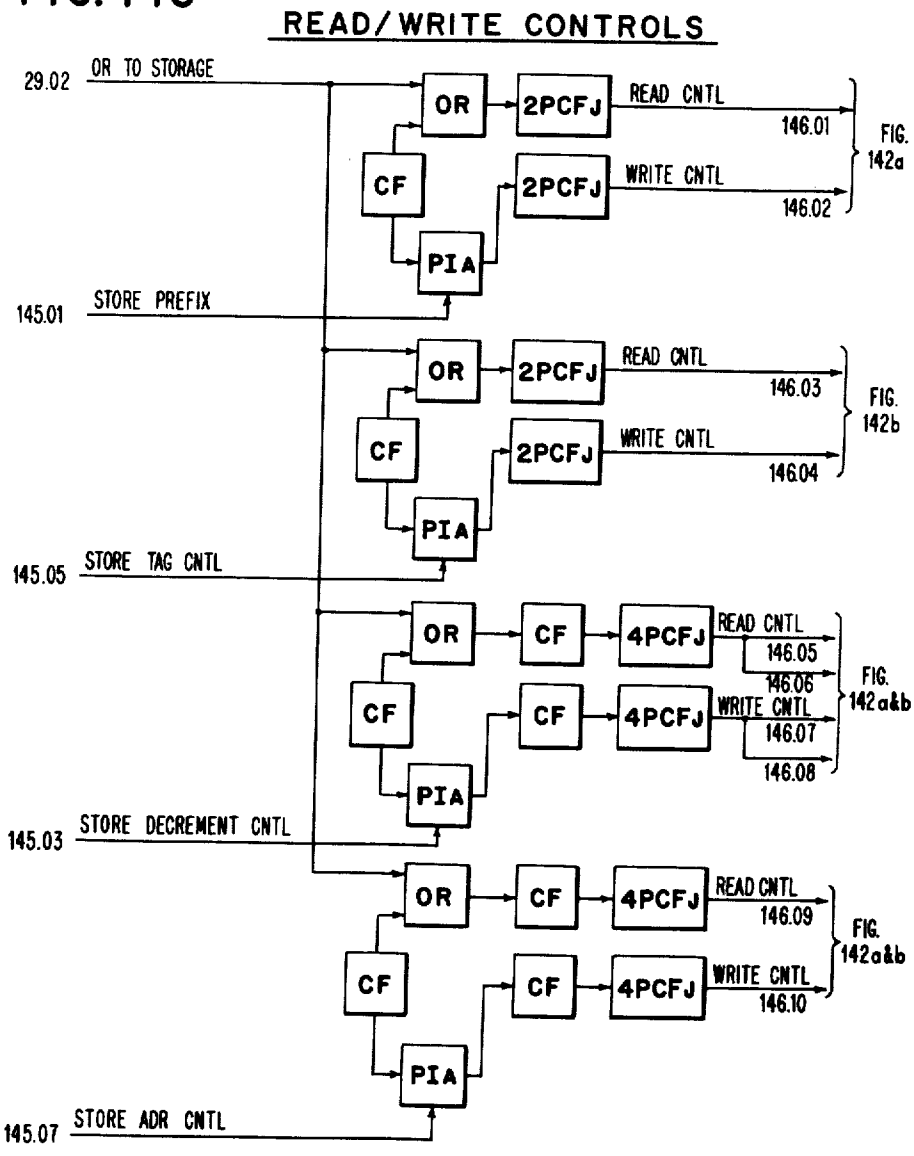
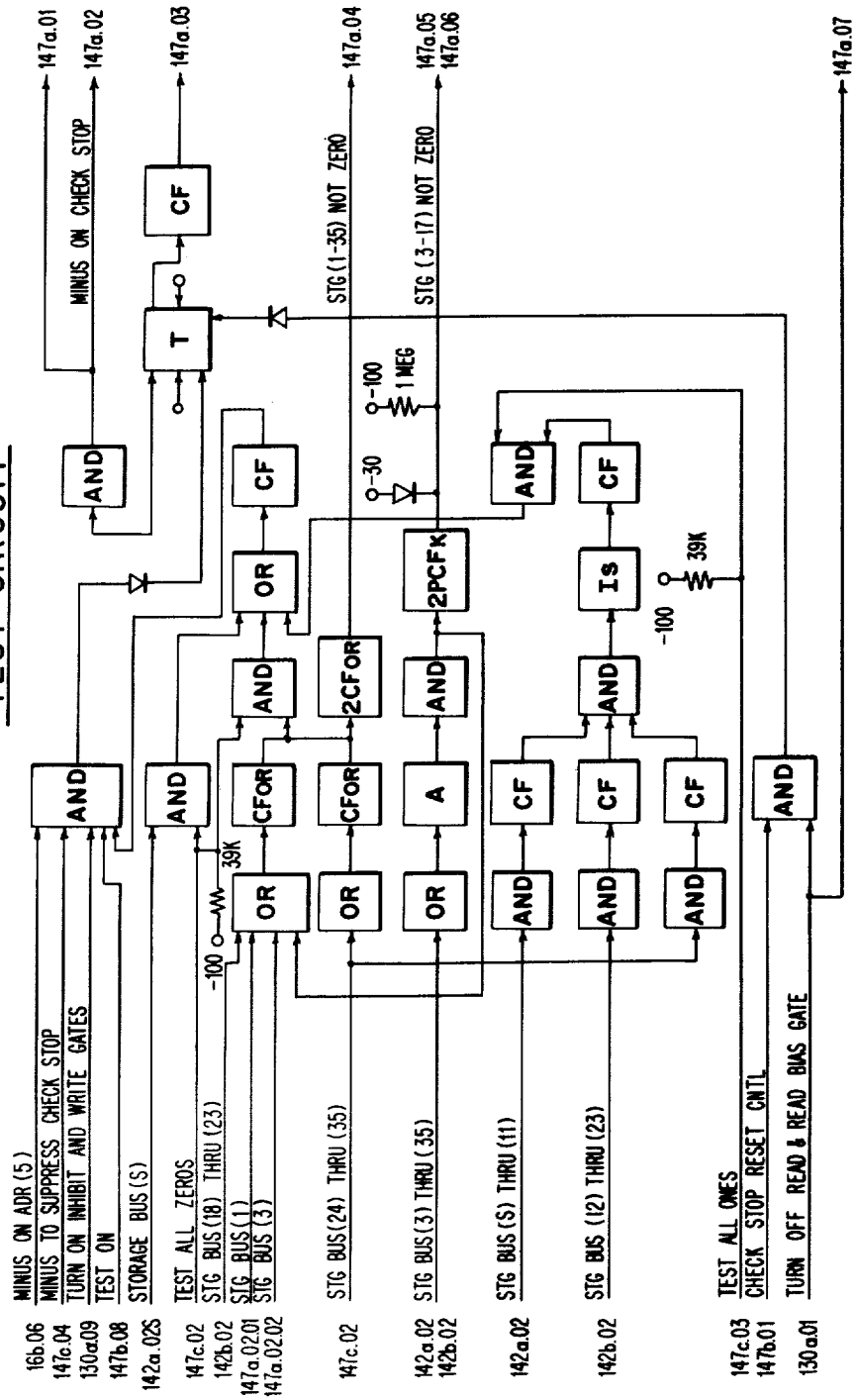

READ/WRITE CONTROLS
29.02
OR TO STORAGE
OR
2PCFJ
READ CNTL
146.01
FIG. 142a
CF
2PCFJ
WRITE CNTL
146.02
PIA
145.01
STORE PREFIX
OR
2PCFJ
READ CNTL
146.03
FIG. 142b
CF
2PCFJ
WRITE CNTL
146.04
PIA
145.05
STORE TAG CNTL
OR
CF
4PCFJ
READ CNTL
146.05
146.06
FIG. 142a&b
CF
CF
4PCFJ
WRITE CNTL
146.07
146.08
PIA
145.03
STORE DECREMENT CNTL
OR
CF
4PCFJ
READ CNTL
146.09
FIG. 142a&b
CF
CF
4PCFJ
WRITE CNTL
146.10
PIA
145.07
STORE ADR CNTL

FIG.147a

TEST CIRCUIT



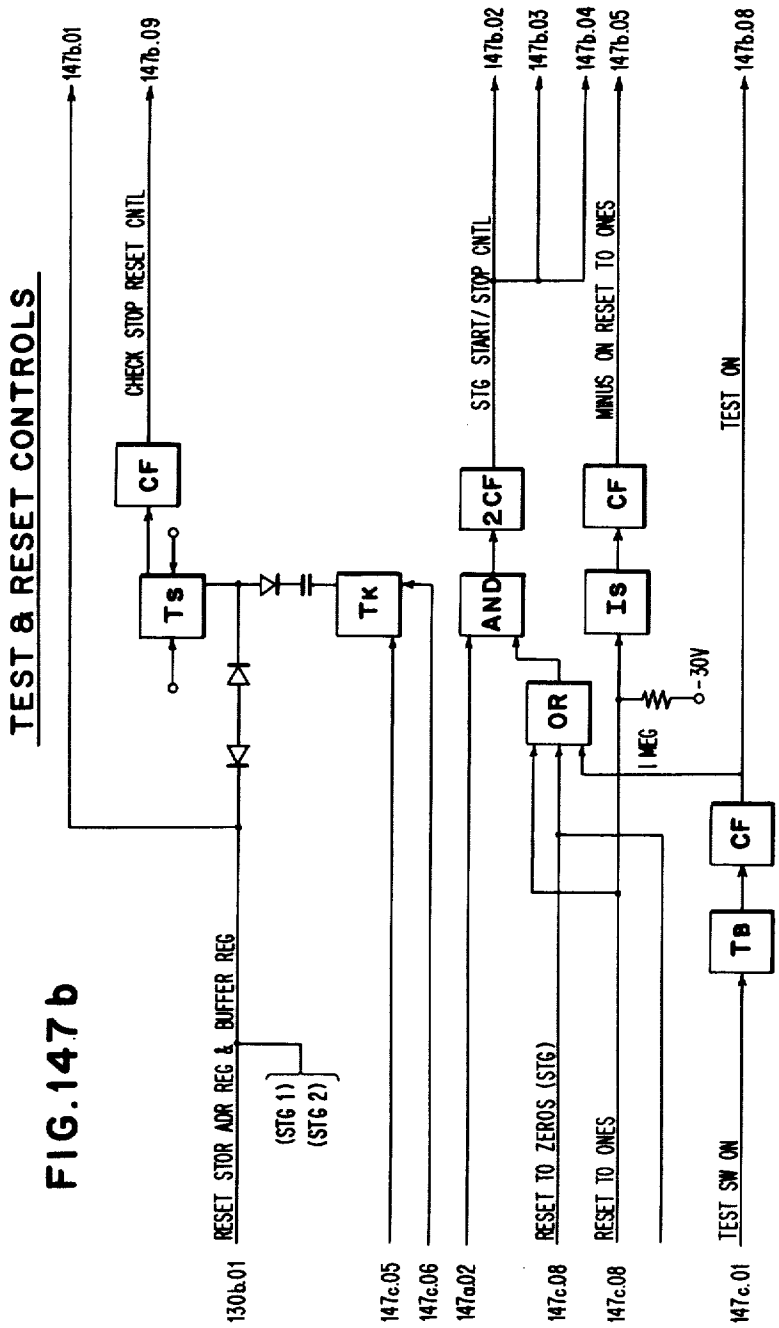

TEST & RESET CONTROLS
147b.01
147b.09
CHECK STOP RESET CNTL
CF
Ts
Tk
147b.02
147b.03
147b.04
147b.05
147b.08
STG START/STOP CNTL
2CF
AND
OR
CF
Is
MINUS ON RESET TO ONES
TEST ON
-30V
1 MEG
CF
TB
RESET STOR ADR REG & BUFFER REG
(STG 1)
(STG 2)
RESET TO ZEROS (STG)
RESET TO ONES
TEST SW ON
130b.01
147c.05
147c.06
147a.02
147c.08
147c.08
147c.01

FIG. 147b

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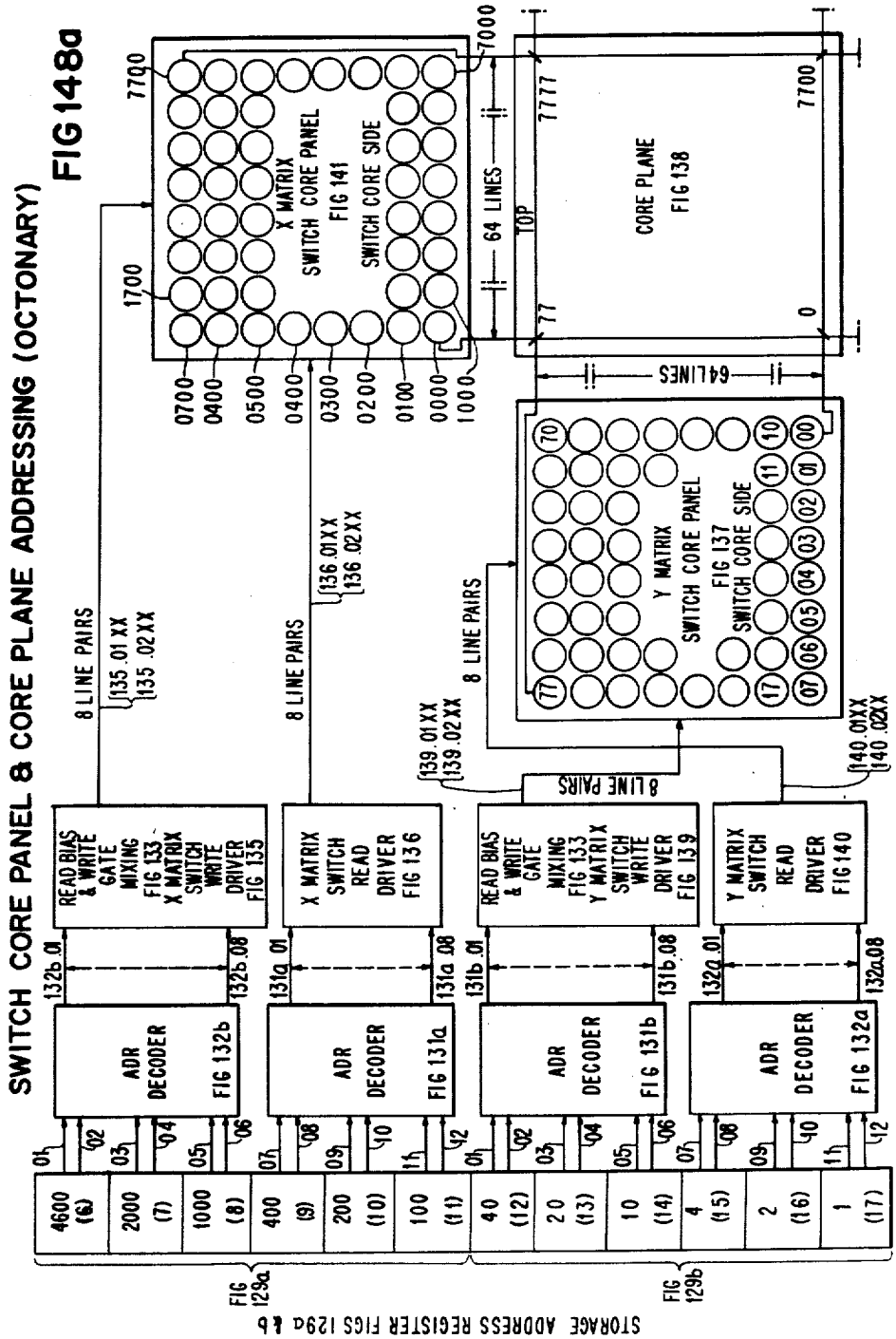
Filed Dec. 26, 1957 244 Sheets-Sheet 243

FIG 148a

SWITCH CORE PANEL & CORE PLANE ADDRESSING (OCTONARY)



May 29, 1962

J. L. BROWN

INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

3,036,773

Filed Dec. 26, 1957

244 Sheets-Sheet 244

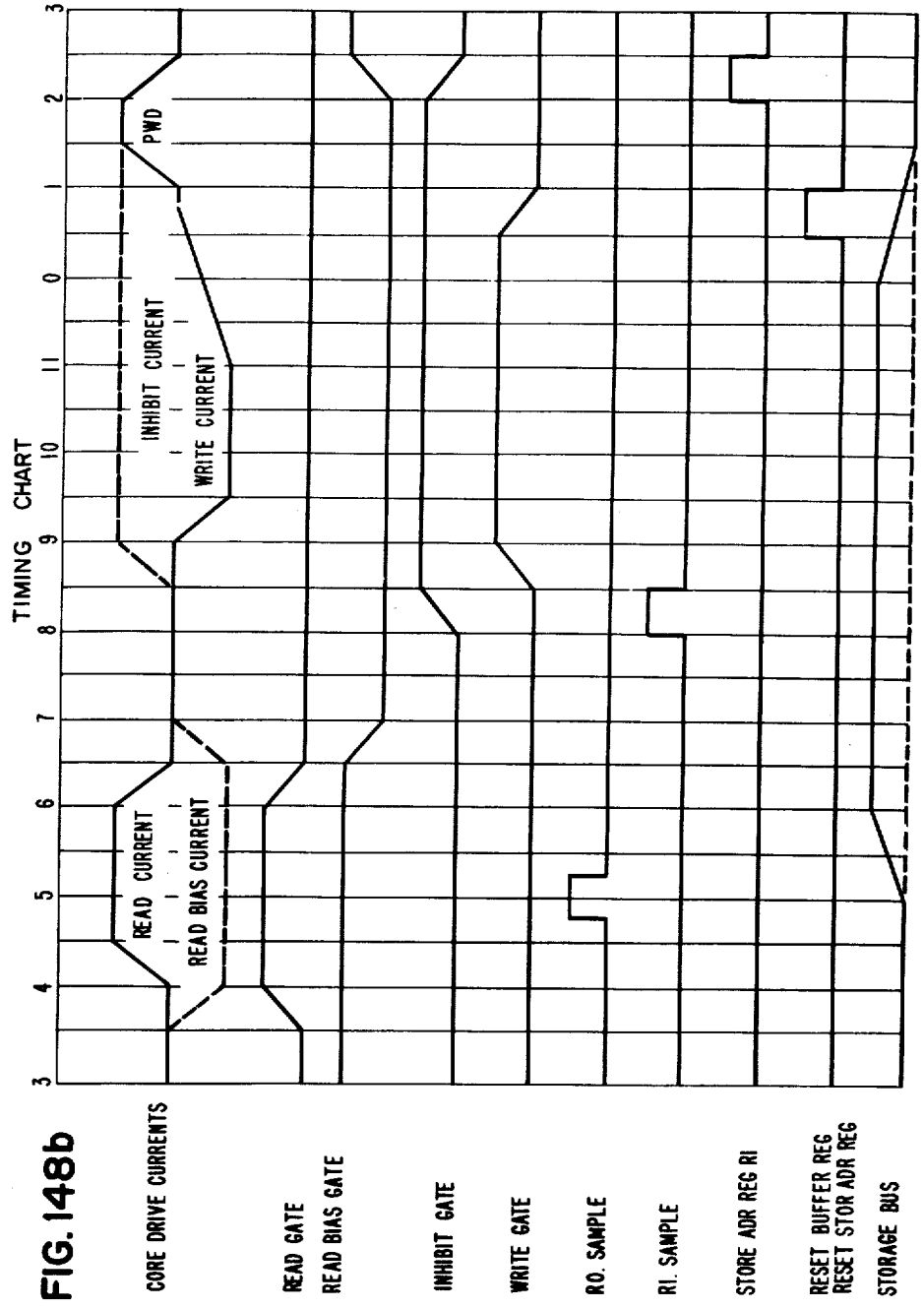


FIG. 148b

United States Patent Office 3,036,773 Patented May 29, 1962

3,036,773

INDIRECT ADDRESSING IN AN ELECTRONIC DATA PROCESSING MACHINE

Joseph L. Brown, Poughkeepsie, N.Y., assignor to International Business Machines Corporation, New York, N.Y., a corporation of New York

Filed Dec. 26, 1957, Ser. No. 705,445
9 Claims. (Cl. 235—157)

This invention relates to electronic data processing machines of the stored program type and more particularly ton an apparatus for modifying the address portion of an instruction word.

In electronic digital data processing machines, the instruction word includes a plurality of binary bits in which some of those bits are known as the operation part of the instruction and some others of these bits are known as the address part of the instruction. The operation part of the instruction word identifies some particular operation which the computer is to perform, and the address part of the instruction identifies the location in storage of the information upon which the specified operation is to be performed. In other instances, the address part of the instruction word identifies the address in storage of another instruction. It has been customary to store a plurality of instruction words in sequential addresses in storage and data words upon which operations are performed in other storage positions. The plurality of instruction words arranged in sequence is called a program and many of the programs are arranged to run in a loop fashion with some instructions being performed over and over in the same sequence with provision for variation being made when certain conditions occur which change the iterative process.

One way an instruction in a stored program may have its address modified by some predetermined amount is by indexing which is accomplished by a set of registers called Index registers. Each indexing instruction specifies an Indexing operation and a register in addition to an address and operation, and the number stored in the Index register is automatically added to the address of the instruction producing a sum which is the actual address used. To modify Instruction addresses, the instruction must specify the particular Index register which is to take part in the modifying operation and this is accomplished by an appropriate digit in the instruction word. The instruction is then executed as if its address field had contained the address minus the contents of the specified Index register. An instruction may refer to more than one Index register with the proper designation in the tag field and the use of a multiple tag results in the logical OR sum of the contents of the specified Index register being used to modify the address. In Direct addressing, an instruction word is decoded according to the operation portion and the address portion controls necessary apparatus to bring a word from Storage which is operated upon in a fashion as determined by the operation portion of the word. In Direct addressing with Indexing operations, the Operations part of the instruction is decoded and the address part of the instruction is delivered to a register where that address part of the instruction is modified by adding to or subtracting from it the contents of a specified one of several of the Index registers. The modified address now specifies the location in Storage

from which information is taken to be manipulated in accordance with the operation part of the instruction.

Just as Index registers are addressed with a tag, indirect addressing is specified by the presence of a code in the designated position of the instruction word. With such a predetermined code designation in the instruction an effective address may be computed in the usual way by subtracting the contents of an Index register if any are selected. The Calculator then examines the word whose location is specified by this effective address and senses the tags in the address part of this word to determine whether a second effective address is to be specified. If this last word is not indirectly addressed the instruction is then executed as if its address field had contained the second effective address.

Briefly stated, in accordance with the principles of this invention an indirected addressing instruction is brought from Storage and decoded and the address part of the instruction is delivered to a register where the address part may or may not be modified by adding to or subtracting from it the contents of predetermined ones of the Index Registers. The address (modified or not) now refers to a location in Storage from which the contents are extracted. These contents may be a data word or another indirectly addressed control word including an address which is entered into the register where it may be modified by indexing if desired. The result now specifies the location in Storage from which another word is taken for subsequent operations which may either be continued indirect addressing operations or data manipulations. The last word of the sequence of words is then operated upon according to the operation part of the initial indirect addressing word.

Indirect addressing is a flexible address modification means. For example, if ten instructions have addresses referring directly to the same data location, it is usually necessary to change the address portion of all ten instructions when the data location is changed. However, if the ten instructions had indirect addresses all referring to a single effective address (which specifices the data location), it would be necessary to change only the one effective address. Indirect addressing may be used in conjunction with standard indexing techniques. Indirect addressing may also be used as a relatively inexpensive substitute for standard indexing techniques by utilizing instructions which increment, or decrement, indirectly addressed effective addresses.

An object of the present invention is to provide an improved Address modification system for digital data processing machines.

It is another object of this invention to provide an improved address modification apparatus wherein the contents of a location in storage are not treated as data but the address of the contents of the location in storage specifies the location from which data or another address may be had for subsequent operations.

Another object is to provide apparatus having an object as described above including means for modifying each of the instruction words by the contents of a selected one of a group of Index registers.

Another object of this invention is to provide apparatus having an object as described above including means for selectively modifying each of the instruction words by the contents of at least two Index registers.

Another object of this invention is to provide improved

address modification apparatus wherein an instruction word is taken from storage at a location specified by an initial instruction word which may have its address portion modified a predetermined amount by an Index register, the latter referring to another instruction word which may have its address portion modified by the same or another Index register as determined by the instruction itself.

It is another object of this invention to provide apparatus for performing N order indirect addressing operations and $(N+1)$ order indexing operations selectively at the option of the programmer.

It is a still further object of this invention to provide apparatus for executing an indirect addressing instruction having instruction, address, and tag parts including a storage device and a computer for decoding operations and performing arithmetic operations including circuits responsive to the tag for delaying the decoding of the operation and for reading out the contents of the location in storage specified by the address as selectively modified by arithmetic operations.

Other objects of the invention will be pointed out in the following description and claims and illustrated in the accompanying drawings, which disclose, by way of example, the principle of the invention and the best mode, which has been contemplated of applying that principle.

In the drawings:

FIGURE 1 is an overall block diagram illustrating the general arrangement of interconnections of the major components comprising the Central Processing Unit.

FIGURES 2*a* through 2*ll* form the logical block diagram for the principal data portions of the Central Processing Unit and Magnetic Core Storage.

FIGURE 2*mm* illustrates how FIGURES 2*a* through 2*ll*, inclusive, may be placed to form a composite block diagram of the major data portions of the Central Processing System.

FIGURES 3*a* through 3*k* illustrate the Word Formats used in the Data Processing System.

FIGURE 4 is a Timing Chart of a Clear and Add Instruction with Indirect Addressing.

FIGURES 5*a* through 5*f* illustrate positions of the Storage Register and Storage Register Hold Circuits in logical block form.

FIGURES 6*a* through 6*n* illustrate the Adder and True Complement Controls in logical block form.

FIGURES 7*a* through 7*g* illustrate the Accumulator Registers in logical block form.

FIGURES 8*a* through 8*g* illustrate the Multiplier Quotient Register and its associated Hold Circuits in logical block form.

FIGURE 9 illustrates the Index Register in logical block form.

FIGURE 10 illustrates the Indicator Trigger Register in logical block form.

FIGURES 11*a*, 11*b* and 11*c* illustrate the Storage Bus Switching, columns S through 35, in logical block form.

FIGURE 12 illustrates the Operator's Panel Entry Keys (S through 35).

FIGURES 13*a*, 13*b*, 13*c* (2 sheets) and 13*d* (3 sheets) illustrate positions 1 through 17 of the Instruction Register (Primary Operation Part) in logical block form.

FIGURES 14*a* through 14*d* illustrate the Primary Operation Decoder in logical block form.

FIGURES 15*a* and 15*b* illustrate the Secondary Operation Decoder in logical block form.

FIGURES 16*a* (2 sheets) and 16*b* (2 sheets) illustrate the Address Register in logical block form.

FIGURE 17 (2 sheets) illustrates the Instruction Counter in logical block form.

FIGURE 18 illustrates the Add and Subtract Execution Control in logical block form.

FIGURE 19 illustrates Clear and Add/Subtract Execution Control in logical block form.

FIGURE 20 illustrates MPY/MPYR EXEC CNTLS (Multiply Execution Controls) in logical block form.

FIGURES 21*a* (2 sheets) and 21*b* (2 sheets) illustrate Floating Point Add/Subtract Execution Controls in logical block form.

FIGURE 22 illustrates Floating Point Trap Trigger in logical block form.

FIGURE 23 illustrates Foating Point Multiply Execution Controls in logical block form.

FIGURE 24 (2 sheets) illustrates Conditional Transfer Execution and Control in logical block form.

FIGURE 25 illustrates Conditional Transfer Controls for transfer on Low MQ in logical block form.

FIGURE 26 illustrates Store Execution Controls in logical block form.

FIGURE 27 illustrates Long Left, Logical Left Execution Control in logical block form.

FIGURE 28 illustrates Long Right, Logical Right Execution Control in logical block form.

FIGURE 29 illustrates OR to Storage Execution Control.

FIGURE 30 illustrates AND to Accumulator and to Storage Execution Control.

FIGURE 31 illustrates OR to Accumulator Execution Control.

FIGURE 32 illustrates Load Index Register Control.

FIGURE 33 illustrates Place Address in Index Register Control and Place Decrement in Index Register in logical block form.

FIGURE 34 illustrates Transfer with Index Raise Execution Control.

FIGURES 35*a* and 35*b* illustrate Indexing Execution Control in logical block form.

FIGURES 36*a* (2 sheets and 36*b* illustrate Convert Control in logical block form.

FIGURE 37 illustrates Exclusive OR to Accumulator in logical block form.

FIGURE 38 illustrates Exchange, Transfer Sign Control in logical block form.

FIGURE 39 illustrates Test Indicators (Storage) Half Test Indicators in logical block form.

FIGURE 40 illustrates Transfer-Indicators to (Accumulator) in logical block form.

FIGURE 41 illustrates Place Indicators in Accumulator and Reset Indicators from Accumulator in logical block form.

FIGURE 42 illustrates Half Indicator Register Controls in logical block form.

FIGURE 43 illustrates Multiply and Multiplier, Floating Point Multiply Trigger and Shift/Step controls in logical block form.

FIGURE 44 illustrates Place Accumulator in Indicators Load Indicators, Invert Indicators or Accumulator Indicators in logical block form.

FIGURE 45 illustrates Storage and Multiplicand Zero Test in logical block form.

FIGURE 46 illustrates Interrupt Control in logical block form.

FIGURE 47 illustrates Execution Control Trigger (T1).

FIGURE 48 illustrates Inverter Trigger T2.

FIGURE 49 illustrates Index Register (N) Hold Lines Adder to Index Register (N).

FIGURE 50 illustrates Adders to Index Register (N) Gating Line Control.

FIGURE 51 illustrates Index Register to Adders Gating Line.

FIGURE 52 illustrates Idex Register Mixing Unit in logical block form.

FIGURES 53*a* and 53*b* illustrate Storage Bus to Storage Register.

FIGURES 54*a* (2 sheets) and 54*b* (2 sheets) illustrate Storage Register (1–8) to Adder and Storage Register (9–35) to Adder.

FIGURES 55*a* (2 sheets), 55*b*, 55*c* (2 sheets) and 55*d*

illustrate True Accumulator (Q, P, 1–8) to Adders; True Accumulator (9–35) to Adders.

FIGURE 56 illustrates Carry to Adder (35) in logical block form.

FIGURES 57*a* and 57*b* (2 sheets) illustrate Adder (Q, P, 1–8) to Accumulator; Adder (9–35) to Accumulator in logical block form.

FIGURE 58 illustrates Shift Accumulator Register Left Control.

FIGURE 59 illustrates Shift Accumulator Register Right Control.

FIGURE 60 illustrates MQ positions S, 1 or 9 to Accumulator 35, 1 to Accumulator 35 Control in logical block form.

FIGURE 61 illustrates Plus to Accumulator Register position S control.

FIGURE 62 illustrates Minus to Accumulator Register S Control.

FIGURE 63 illustrates Storage Register S, 1 through 35 to MQ Register Controls in logical block form.

FIGURE 64 illustrates Shift MQ Right Controls in logical block form.

FIGURE 65 illustrates Shift MQ Left Controls in logical block form.

FIGURE 66 illustrates Clear MQ Register in logical block form.

FIGURE 67 illustrates Ring Shift MQ in logical block form.

FIGURE 68 illustrates 1 to MQ Register position 35 Control in logical block form.

FIGURE 69 illustrates I/O Bus, S through 35, to MQ Register Controls in logical block form.

FIGURE 70 illustrates Adders to Accumulator Controls in logical block form.

FIGURE 71 illustrates Minus to MQ position S controls in logical block form.

FIGURE 72*a* and 72*b* illustrate Accumulator to Storage Bus Controls.

FIGURE 73 illustrates operation Panel Keys to Storage Register Controls.

FIGURE 74 illustrates MQ Register S, 1 through 35 to Bus S, 1 through 35 and Storage MQ Register Store Control.

FIGURE 75 illustrates Address Switches to Storage Bus 3 through 17, 21 through 35 control.

FIGURE 76 illustrates Clear and Add AND Control.

FIGURE 77 illustrates Minus to Storage Register S Control in logical block form.

FIGURE 78 illustrates 35 to Shift Counter Control in logical block form.

FIGURE 79 illustrates Step Shift Counter Countrols in logical block form.

FIGURE 80 illustrates Adder (1) Carry or Accumulator (1 or P) to Overflow Trigger Controls.

FIGURE 81 illustrates Ones to Adders Q, P, 1 through 8 Controls in logical block form.

FIGURE 82 illustrates Carry to Adder Position 8 Controls in logical block form.

FIGURE 83 illustrates Floating Point Shift Control in logical block form.

FIGURE 84 illustrates Adders 1 through 8 to MQ 1 through 8 in logical block form.

FIGURE 85 illustrates Step Floating Point Tally Counter in logical block form.

FIGURES 86*a* and 86*b* illustrate Indexing Operation and Storage Register 18 through 35 to Adders P through 17.

FIGURES 87*a* and 87*b* illustrate Index Register to Adder Controls in logical block form.

FIGURE 88*a* illustrates Floating Point Tally Counter.

FIGURE 88*b* illustrates Trapping Control in logical block form.

FIGURES 89*a* and 89*b* illustrate Index Register Entry Control Carry One to Adder 16 and Carry One to Adder 17 Controls.

FIGURES 90*a* and 90*b* illustrate Indexing Controls.

FIGURES 91*a* and 91*b* illustrate Adder to Index Register.

FIGURE 92 illustrates Electronic Reset of Indicators.

FIGURE 93 illustrates Reset Indicators Controls in logical block form.

FIGURE 94 illustrates Set Indicators Controls in logical block form.

FIGURE 95*a* illustrates Invert Indicators Controls in logical block form.

FIGURE 95b illustrates Display Indicators.

FIGURE 96 illustrates Indicators to Storage Bus Controls in logical block form.

FIGURE 97 illustrates complement Indicators to Storage Register Controls in logical block form.

FIGURE 98 illustrates Indirect Addressing Controls in logical block form.

FIGURE 99 illustrates Instruction Register Pulse Generator in logical block form.

FIGURE 100 (2 sheets) illustrates Instruction Register Sign, Plus and Minus Controls in logical block form.

FIGURE 101 illustrates Shift Counter Plus Generator 1 in logical block form.

FIGURE 102 illustrates Shift Counter Pulse Generator 2 in logical block form.

FIGURE 103 illustrates Zero Address Controls.

FIGURE 104 illustrates Floating Point Entry to Shift Counter 10 throufh 17 Controls.

FIGURE 105 illustrates Subtract Control in logical block form.

FIGURE 106 illustrates Sense Unit Address in logical block form.

FIGURE 107 (2 sheets) illustrates Advance Instruction Counters in logical block form.

FIGURE 108 illustrates Reset Instruction Counter Address Switch to Instruction Counter Control in logical block form.

FIGURE 109 illustrates Instruction Counter Transfer Control in logical block form.

FIGURES 110*a* and *b* illustrate Address Switch Input Controls in logical block form.

FIGURE 111 illustrates Enter MQ Control in logical block form.

FIGURE 112 illustrates the Primary Drive Circuits.

FIGURE 113 illustrates a Sign Mixing Controls.

FIGURE 114 illustrates the Master Oscillator.

FIGURE 115 illustrates the Inverted Sync Generator.

FIGURE 116 illustrates the Inverted Clamp Generator and Clock Drive.

FIGURE 117 (2 sheets) illustrates the Clock.

FIGURE 118 (2 sheets) illustrates Cycle Timer Control.

FIGURE 119 illustrates Cycle Timer Gate Generator.

FIGURE 120 illustrates Cycle Timer Output Circuit.

FIGURE 121 illustrates B Time Control.

FIGURES 122*a* (2 sheets) to *p* illustrate Pulse and Gate Generator Controls.

FIGURE 123 illustrates Column Q Carry and Overflow Triggers.

FIGURE 124 illustrates Column 9 Carry and Overflow Triggers.

FIGURE 125 illustrates Floating Point Overflow Trigger and Floating Point Underflow Trigger.

FIGURE 126*a* indicates Adder X Carry Trigger.

FIGURE 126*b* illustrates Divide Check Trigger.

FIGURE 127 illustrates Floating Point Overflow and Underflow Detection.

FIGURES 128*a* (2 sheets), *b* and *c* illustrate End Operation Control.

FIGURE 129*a* and *b* illustrates the Storage Address Register.

FIGURES 130*a* and *b* illustrate the Pulse Generator I and II.

FIGURE 130*c* illustrates Timing Pulse Control Circuits.

FIGURES 131*a* and *b* illustrate the Address Decoder Circuit.

FIGURES 132*a* and *b* illustrate the Address Decoder Circuit.

FIGURE 133 illustrates Write Driver Select Circuits.

FIGURE 134*a* and *b* illustrate Gate Generator.

FIGURE 135 illustrates the X Matrix Switch Write Driver.

FIGURE 136 illustrates the X Matrix Switch Read Driver.

FIGURES 137*a* illustrates the Y Driver Matrix Switch Layout.

FIGURE 137*b* illustrates diagrammatically a Core with certain of its Control Windings.

FIGURE 138*a* illustrates diagrammatically the Core Array Layout.

FIGURE 138*b* illustrates in isometric, a Core with Windings.

FIGURE 139 illustrates the Y Matrix Switch Write Driver.

FIGURE 140 illustrates Y Matrix Switch Read Driver.

FIGURE 141*a* illustrates the X Driver Matrix Switch Layout.

FIGURE 141*b* illustrates diagrammatically a Core with certain of its Control Windings is in FIG. 137*b*.

FIGURES 142*a*, *b*, and *c* illustrate the Sense Amplifier, Buffer Register and I/O Switching.

FIGURE 143 illustrates the Digit Plane Select Circuits.

FIGURE 144 illustrates the Digit Plane Driver Circuits.

FIGURE 145 illustrates the Address and Operation Control.

FIGURE 146 illustrates the Read/Write Controls.

FIGURES 147*a*, *b*, and *c* illustrate Test Circuits, Test and Reset Controls and the Test Panel Circuits.

FIGURE 148*a* illustrates Switch Core Panel and Core Plane Addressing (Octonary).

FIGURE 148*b* is a timing chart illustrating the Timing of Magnetic Core Storage in sequence for one cycle from 3 time of a first cycle until 3 time of a second cycle.

The convention employed in numbering lines in the logical block diagrams is as follows: from left to right, the first numbers and the letter, if any, to the period or point is the figure number from which the line originated; the next two numbers to the second point refer to the "output" lines (generally numbered according to their positions on the sheet from top to bottom); and the last two numbers, when used, refer to the numerical position of the line with the word S, 1 through 35. Each input line in the block diagram bears the number derived from its point of origin. In the composite drawings, data flows generally into the block at the top and out of the block at the bottom, and control lines which cause the movement of data to enter the block from the left.

In FIGURE 1, there is shown a Central Processing Unit of a high speed Data Processing system which is controlled by an internally stored program with instructions of the single address type which direct the machine to execute instructions at the rate of about 20,000 per second. The funcions of transferring data in and out of the Central Processing Unit from Input-Output devices, Magnetic Core Storage, Magnetic Drum Storage, are controlled by the stored program as well. Internally, the Central Processing Unit operates in the binary number system, but the Input-Output number system may be those used in punched card systems, the decimal system, or the binary coded decimal (BCD) system to name a few. Many of the basic devices of the Central Processing Unit, shown generally in FIGURE 1, and more specifically in FIGURE 2, assume two stable states and are well suited to the binary system of notation where one specified state is indicative of a binary "one" and the other state is indicative of a binary "zero." The basic unit of information, the Word, consists of thirty-six binary digits and may be alphabetic, numeric, symbolic, an instruction, or any pattern of thirty-six bits desired by the programmer for any reason. The thirty-six positions of the word are shown schematically in FIGURE 3 where S refers to the sign position, **1** refers to bit position **1**, **2** refers to bit position **2** and so forth. Only when a word is interpreted as numerical data does position S have any algebraic significance. Then, with position S containing a "zero" the word is signified as positive and with position S containing a "one" the word is signified as negative. When a logical operation is performed upon a word, the word is interpreted as a thirty-six bit signless number.

Individual location in Magnetic Core Storage, Magnetic Drum Unit and individual units such as Magnetic Tape Units and all other Input-Output Units are identified by systems of numerical addresses, as described more fully in copending application, Serial No. 705,447, filed December 26, 1957. By means of a number contained in the Address part of the Instruction, it is possible to refer to the information contained in any location in Magnetic Core Storage or any Input-Output Unit of the system.

In FIGURE 1, the Central Processing Unit has data portions which comprise a thirty-six order Storage Register **1.01** comprising thirty-five orders and a sign order, a thirty-six order Adder **1.03** plus one overflow order, an Accumulator Regiser **1.05** of thirty-five orders plus two overflow orders P and Q and a sign order S, a Multiplier Quotient Register **1.07** comprising thirty-five orders and a sign order, three Index Registers **1.09** A, B and C of fifteen orders and their associated Index Register controls, an Indicator Trigger Register **1.12** of thirty-six orders **0** through **35**, Storage Bus Switching **1.14** of thirty-six orders connected to a Storage Bus **1.16** of thirty-six orders, the latter being connected to Magnetic Core Storage, and Operator's Entry Keys **1.18** of thirty-six orders. Associated with the data portion previously described is an Instruction Register **1.20** of eighteen positions S, **1** through **17**, an Address Register **1.22**, and in Instruction Counter **1.24** with related Storage Address Controls **1.26**. Information may be placed in Core Storage from either the Accumulator Register **1.05**, the Multiplier Quotient Register **1.07**, or the Indicator Register **1.12**. It is a function of the Sstorage Bus Switches **1.14** to switch the contents of the Accumulator Register, the MQ Register, or the Indicator Register onto the Storage Busses **1.16** in accordance with the execution of certain instructions which require that information be located in Storage.

The Central Processing Unit and Core Storage of the present invention may be employed in a data processing system whihc includes Data Synchronizers, Tape Control Units, Tape Drive Units, Printers, Perforating machines and Readers. The Data Synchronizers are used to control the flow of information from the input-output devices such as Tape Control Units, Tape Drive Units and Readers to Core Storage and to control the flow of information from Core Storage to the Tape Units, Printers, and Perforating machines. The Tape Control Unit controls all operations to be executed by the Tape Drive Units and assembles and disassembles **36** bit words as required in the transmission of data through the system.

A detailed description of general operations of a computer of this class may be performed in response to well-known instructions is found in copending applicatiou Computer for **701**, Serial No. 419,642, Haddad et al., filed March 30, 1954. Certain arithmetic, logical, and other operations may be performed by the device of the present invention in response to instructions tabulated immediately below in accordance with the principles set forth in Manual of Operations, Electronic Data Processing Machines, Type 704, Form No. 24–6661, copyright 1954, 1955, and printed in the U.S.A. by International Business Machines Corporation, the assignee of this application. The operation codes specify the particular operation to be performed and are tabulated in numeric form below. However, each numeric code must be translated into machine language which is in the binary code. For example, 0361 (octal) is expressed as 000011110001.

Title	Operation Code
Add and Carry Logical Word	ACL+0361
Add	ADD+0400
Add Magnitude	ADM+0401
Accumulator Left Shift	ALS+0767
AND to Accumulator	ANA−0320
AND to Storage	ANS+0320
Accumulator Right Shift	ARS+0771
Backspace Tape	BST+0764
Clear and Add Logical Word	CAL−0500
Compare Accumulator with Storage	CAS+0340
Change Sign	CHS+0760 . . . 0002
Clear and Add	CLA+0500
Clear Magnitude	CLM+0760 . . . 0000
Clear and Subtract	CLS+0502
Complement Magnitude	COM+0760 . . . 0006
Divide Check Test	DCT+0760 . . . 0012
Divide or Halt	DVH+0220
Divide or Proceed	DVP+0221
Enter Trapping Mode	ETM+0760 . . . 0007
Floating Add	FAD+0300
Floating Divide or Halt	FDH+0240
Floating Divide or Proceed	FDP+0241
Floating Multiply	FMP+0260
Floating Subtract	FSB+0302
Halt and Proceed	HPR+0420
Halt and Transfer	HTR+0000
Low Order Bit Test	LBT+0760 . . . 0001
Locate Drum Address	LDA+0460
Load MQ	LDQ+0560
Logical Left	LGL−0763
Long Left Shift	LLS+0763
Long Right Shift	LRS+0765
Leave Trapping Mode	LTM−0760 . . . 0007
Load Index from Address	LXA+0534
Load Index from Decrement	LXD−0534
Multiply and Round	MPR−0200
Multiply	MPY+0200
Minus Sense	MSE+0760
No Operation	NOP+0761
OR to Accumulator	ORA−0501
OR to Storage	ORS−0602
Place Address in Index	PAX+0734
P-Bit Test	PBT−0760 . . . 0001
Place Decrement in Index	PDX−0734
Plus Sense	PSE+0760
Place Index in Decrement	PXD−0754
Read Select	RDS+0762
Rewind	REW+0772
Round	RND+0760 . . . 0010
Rotate MQ Left	RQL−0773
Subtract Magnitude	SBM−0400
Store Left Half MQ	SLQ−0620
Store Logical Word	SLW+0602
Set Sign Minus	SSM−0760 . . . 0003
Set Sign Plus	SSP+0760 . . . 0003
Store Address	STA+0621
Store Decrement	STD+0622
Store	STO+0601
Store Prefix	STP+0630
Store MQ	STQ−0600
Subtract	SUB+0420
Store Index in Decrement	SXD−0634
Transfer on Index	TIX+2000
Transfer on Low MQ	TLQ+0040
Transfer on Minus	TMI−0120
Transfer on No Overflow	TNO−0140
Transfer on No Index	TNX−2000
Transfer on No Zero	TNZ−0100
Transfer on Overflow	TOV+0140
Transfer on Plus	TPL+0120
Transfer on MQ Plus	TQP+0162
Transfer	TRA+0020
Transfer and Set Index	TSX+0074
Trap Transfer	TTR+0021
Transfer on Index High	TXH+3000
Transfer with Index Incremented	TXI+1000
Transfer on Index Low or Equal	TXL−3000
Transfer on Zero	TZE+0100
Unnormalized Floating Add	UFA−0300
Unnormalized Floating Multiply	UFM−0260
Unnormalized Floating Subtract	UFS−0302
Write End of File	WEF+0770
Write Select	WRS+0766

Still other instructions not described in this application cause operations to be performed in accordance with the principles described in copending applications, Serial No. 705,477, filed Dec. 26, 1957; Serial No. 705,446, filed Dec. 26, 1957; Serial No. 705,444, filed Dec. 26, 1957; and Serial No. 705,442, filed Dec. 26, 1957.

In FIGURE 4, there is illustrated the general timing relationship of machine operations performed in accordance with the principles of this invention. At this time, reference to the figure serves only to show generally the sequence of operations in order that a better understanding of the structure may be had while reading the description of the system to follow, after which the operations are described in detail.

The term "data" is used to describe transmission of information which is not destined for interpretation as an instruction or command even though ultimately it may, in some other program routine, be interpreted as an instruction or command or part of either subject to modification by the machine or the program or a combination thereof.

In FIGURE 2, data portions of the Central Processing Unit of FIGURE 1 are shown in FIGURES 2*a* through 2*gg* which comprise the Storage Register, FIGURES 2*b* through 2*d* (FIGURES 5*a*–5*f*); the Adder, FIGURES 2*j* through 2*u* (FIGURES 6*a*–6*m*); the Accumulator Register, FIGURES 2*x* through 2*cc* (FIGURES 7*a*–7*g*); the Multiplier Quotient Register, FIGURES 2*dd* through 2*gg* (FIGURES 8*a*–8*g*); the Index Registers, FIGURES 2*f* and 2*g* (FIGURE 9); the Indicator Register, FIGURE 2*a* (FIGURE 10); Storage Bus Switching, FIGURES 2*w* through 2*y* (FIGURE 11); the Storage Bus, FIGURES 2*w* through 2*y*; and the Operator's Entry Keys, FIGURE 2*e* (FIGURE 12). Associated with the data portion previously described is the Instruction Register, FIGURE 2*h* (FIGURE 13), the Primary and Secondary Operation Decoders, FIGURES 14 and 15, and the Address Register, FIGURE 2*i* (FIGURE 16), and the Instruction Counter, FIGURE 2*v*. Magnetic Core Storage as a unit is shown in FIGURES 2*hh* through 2*ll* and Storage Address Controls are shown in FIGURES 2*hh* through 2*kk*.

Arithmetic Control

The Arithmetic Control section of the CPU is to determine what operation must be performed for executing each instruction and to sequence these operations. In order to perform this function, there are Execution Controls illustrated in FIGURES 18 through 51 for each arithmetic instruction. Arithmetic Control Mixing Circuits or Command Circuits are illustrated in FIGURES 52 through 98 which take the information from the Execution controls and provide gates and pulses to perform each operation required.

Program Circuits

The information received from Core Storage by the Central Processing Unit is initially placed in the Storage Register, FIGURES 2*b* through 2*d*, from the Sense Amplifier Buffer and I/O Switching of FIGURE 2*ll* prior to being operated on by the Program and Arithmetic circuits. The registers and counters used to receive and decode the instructions consist of the Instruction Register, FIGURE 13, the Instruction Counter, FIGURE 17, the Primary Operation Decoder, FIGURE 14, the Secondary Operation Decoder, FIGURE 15, and related control circuits, FIGURES 99–111. The Storage Address Register, FIGURES 129*a* and *b*, controls the addressing of the Core Storage Unit and is located in the unit it controls, that is, Magnetic Core Storage **1.12**, illustrated functionally in FIGURES 2*hh*–2*ii*. Each of the registers and counters is described individually with reference to its function in the overall flow of information and both general and specific timings are set forth later in connection with the receiving and decoding of instructions.

The input information to the execution controls is primarily the output of the Instruction Register, FIGURE 13, which is routed through the Primary Operation Decoder, FIGURE 14 and the Secondary Operation Decoder, FIGURE 15. The decoder output is often mixed with an indication of one of the following conditions to provide conditional operation: (1) whether an overflow has occurred in the Accumulator, (2) whether the carry output from column Q of the Adder is present, (3) whether the carry output from column 6 of the Adder is present, (4) whether the contents of the sign position of the Accumulator Register, the Storage Register or the Quotient Register is negative, or (5) whether the Shift Counter is at "0" or not. (The Shift Counter, as described later, is used to count E/R (Execute-Route)

cycles for a Multiply or a Divide instruction and is also used to count the number of shifts in a Shifting instruction.) The command circuits are provided with pulses or gates which circuits become the output command lines or control lines when they are conditioned by the outputs of the execution controls.

The Storage Register, FIGURES 2*b–d*, has inputs **12.01.01** through **12.01.36** to each of its positions S, **1** through **35** from respectives ones of positions S, **1** through **35** of the Entry Keys, FIGURE 2*e*. The Storage Register also has inputs **11***b*.**03** and **11***c*.**03** to positions **1** through **35** from corresponding outputs of positions **1** through **35** of Storage Bus Switching, FIGURES 2*w–y*. Another set of inputs **10.01**S through **10.01.35** is provided to the Storage Register positions S, **1** through **35** from the outputs of the Indicator Register, FIGURE 2*a*, positions O, **1** through **35**. Outputs **5***a*.**04**; **5***b*.**06**; **5***c*.**04**; and **5***f*.**05** are provided from Storage Register, positions S, **1** through **35** to the input of positions O, **1** through **35** of the Indicator Register. Outputs **5***b*.**04** are provided from the Storage Register positions **1**, **2**, **8** and **9** to Indexing Controls," FIGURE 90. Outputs **5***b*.**07** from Storage Register positions **3** through **11** are provided to positions **1** through **9** of the Instruction Register, FIGURE 2*h*, with additional lines **5***b*.**07.01** and **5***b*.**07.02** from positions **1** and **2** to the Instruction Register Pulse Generator, FIGURE 99. Furthermore, an additional pair of outputs **5***b*.**07** from Storage Register positions **1** and **2** are sent to the inputs **5***b*.**07.01** and **5***b*.**07.02** of the Instruction Register positions **8** and **9**. Outputs **5***a*.**02**S; **5***b*.**03**; **5***c*.**08**; and **5***f*.**08** from Storage Register positions S and **1** through **35** are provided to respective positions S, **1** through **35** of the MQ Register, FIGURES 2*dd–gg*. Outputs **5***b*.**05** from positions **12** and **13** of the Storage Register, FIGURE 2*c* are provided to "Indirect Addressing Controls," FIGURE 98. Outputs **5***b*.**02**; **5***c*.**07**; **5***f*.**07** are provided from positions **1** through **35** of the Storage Register to respective inputs **1** through **35** of the Adder Register. Outputs **5***a*.**01** and **5***b*.**01** from positions S, **1** through **5** of the Storage Register, FIGURES 2*b–2d* are provided to the inputs of positions **30** through **35**. FIGURE 2*gg* of the MQ Register. Outputs **5***c*.**02**; **5***c*.**09**; **5***f*.**06** from positions **19** through **35** of the Storage Register are provided to the inputs of positions **1** through **17** of the Adder. Output **5***c*.**01** for S position **18** of the Storage Register is provided to "Ones to Adder," FIGURE 81. Outputs **5***c*.**06** are provided from positions **18** through **20** of the Storage Register, FIGURE 2*d*, to "Index Register Hold Lines and Adder Control," FIGURE 49. Outputs **5***f*.**01**; **5***f*.**03** are provided from positions **24** through **26** of the Storage Register, FIGURE 2*d* to "Channel Select," FIGURE 153. Outputs **5***f*.**04** from Storage Register positions **24** through **26**, FIGURE 2*d*, are provided to the Data Synchronizer Instruction Decoder, FIGURE 160 and outputs **5***f*.**02.24–26** are provided from positions **24** through **26** of the Storage Register to "Sense Unit Address Control," FIGURE 106. Outputs **5***c*.**05.18–20** are taken from positions **18** through **20** of the Storage Register and are sent to "Index Registers to Address Gating Line," FIGURE 51.

The Adder Register has positions Q, P and **1** through **35** as previously described and inputs **81.01** through **81.10** are provided to positions Q, P, **1** through **8** from "Ones to Adder Control," FIGURE 81. Inputs **7***g*.**01**; **7***b*.**02**; **7***c*.**02**; **7***d*.**02** are provided to positions Q, P and **1** through **35** of the Adder Register from positions Q, P and **1** through **35** outputs of the Accumulator Register, FIGURES 2*x–cc*. Inputs are provided to positions **3** through **17** of the Adder Register, FIGURE 2*k–2q*, from positions **3** through **17** of the Index Register Mixing, FIGURE 2*f*. Inputs are provided to Adder positions **6** through **17** from Drum Control of Drum Unit **1.14**. Inputs **7***c*.**03–34**; **7***d*.**03.35** are provided to positions **12** through **17** of the Adder, FIGURES 2*k–2q*, from positions **30** through **35**, FIGURE 4*cc*, of the Accumulator Register, and inputs **8***a*.**06**; **8***b*.**06**; **8***c*.**03** are provided to positions **12** through **17** of the Adder from positions **1** through **5**, FIGURE 2*dd*, of the MQ Register. Outputs are provided from the Adder as inputs to positions Q, P and **1** through **35** of the Accumulator Register. Outputs **6***b*.**02**; **6***c*.**01**; **6***d*.**02**; **6***e*.**02** are provided from the Adder positions **1** through **8** to the input of positions **1** through **8** of the MQ Register. Outputs are provided from the Adder positions **3** through **17** to the inputs of each of the Index Registers A, B and C, FIGURE 9. Outputs are provided from the Adder positions **3** through **17** to the inputs of the Address Register, FIGURE 2*i*.

An output is provided from each lower order Adder position, FIGURES 2*i–u*, to the input of each higher order position as illustrated. For example, the carry output **6***h*.**03**, FIGURE 2*u*, of position **34** of the Adder is connected to the input of position **33** of the Adder, the carry output of position **33** of the Adder is connected to the input of position **32** of the Adder, and in like manner similar carry lines are connected through position Q.

Output lines are provided from positions **3** through **17** of the Address Register, FIGURE 2*i* (FIGURES 16*a* and 16*b*) as inputs to positions **3** through **17** of the Storage Bus Switches.

Inputs are provided to the Storage Bus Switching, FIGURES 2*w–y* positions S, **1** through **35** from the output of the MQ Register positions S, **1** through **35** and inputs are provided to Storage Bus Switching positions S, **1** through **35** from the outputs of the Indicator Register. An input **71.01**S, FIGURE 2*w*, is provided to positions S of Storage Bus Switching from the output of position P, FIGURE 2*aa*, of the Accumulator Register. Inputs are provided to the Storage Bus Switching positions **1** through **35** from positions **1** through **35** of the Accumulator Register and there is a connection **7***b*.**01**P between the output of position P, FIGURE 2*aa*, of the Accumulator Register to the input of the S position, FIGURE 2*w* of the Storage Bus Switching.

An output **11***a*.**04**S is provided from position S, FIGURE 2*w*, of Storage Bus Switching to "Minus on Storage Register," FIGURE 77. Outputs **11***a*.**02**; **11***b*.**04**; **11***c*.**04** are provided from the Storage Bus Switching positions S, **1** through **35** to Memory Buffer Register, FIGURE 142. Outputs **11***a*.**03**; **11***b*.**01**; **11***c*.**01** are provided from Storage Bus Switching positions S, **1** through **5**, FIGURES 2*w–2x* to position P, **1** through **5**, FIGURES 2*j–2l*, of the Accumulator Register. Positions P, **1** through **35** of the Accumulator Register have outputs from each lower order position connected to the next adjacent higher order position terminating at the input of position P for the purpose of shifting left. There are outputs from positions Q, P, **1** through **34** of the Adder to the inputs of the next adjacent lower order position terminating with the output position **34** entering as an input of position **35** for shifting right. Position Q of the Accumulator Register has an output **7***g*.**02**Q to the Carry Overflow Trigger, FIGURE 123, and another output **7***g*.**03**Q to **2**, Floating Point Overflow/Underflow Detection, FIGURE 127. An output line **7***b*.**07**P is provided from position P of the Accumulator Register to Test Sense Input (not shown in the drawings) and another output **7***b*.**08**P to Floating Point Overflow/Underflow Detection Controls, position **1** of the Accumulator Register has an output **7***b*.**01.01** to Adder **1** Carry to Accumulator Overflow Trigger, FIGURE 80. Outputs are provided from the Accumulator Register positions P, **1** through **35** to the input of Storage Bus Switching positions S, **1** through **35** as previously described. Position **9** of the Accumulator Register has two output lines **7***c*.**06.08** and **7***c*.**07.09** to Column **9** Carry and Overflow Trigger, FIGURE 124, and to Floating Point Add/Subtract Execution Controls, FIGURES 21*a* and 21*b*. An output **7***d*.**08.35** from position **35**, FIGURE 2*cc*, of the Accumulator Register is connected to the input of position S, FIGURE 2*dd*, of the Multiplier Quotient Register, and another output **7***d*.**07.35** is connected to position **1** of the MQ, FIGURE 2*dd*.

Position S, FIGURE 2*dd*, of the MQ Register has an output line **8***a*.**06**S to "Adder and True Complement Controls," FIGURE 6*k*, an output **8***a*.**05**S to "Floating Point Shift Control," FIGURE 83, and another output **8***a*.**01**.S to "Sign Mixing," FIGURE 113. Position **1** of the MQ Register, FIGURE 2*dd*, has an output **8***b*.**03**.**01** to "Floating Point Shift Control," FIGURE 83, has an output **8***b*.**02**.**01** to "Multiply Execution Control," FIGURE 20, and an output **8***b*.**01**.**01** to "Sense Unit Address, FIGURE 106; Position **8**, FIGURE 2*ee*, of the MQ Register has an output **8***d*.**01**.**08** to "Floating Point Shift Control," FIGURE 83. Position **9**, FIGURE 2*ff*, has an output **8***e*.**02**.**09** to the "Floating Point Shift Control," FIGURE 83, and an output **8***e*.**01**.**09** that goes to "Floating Point Round," FIGURE 106. Outputs **8***e*.**06**.**34** and **8***f*.**03**.**35** are provided from position **34** and position **35** to "Multiply Floating Point Trigger Shift Step," FIGURE 43. Output lines are provided from positions S, **1** through **35** for entry of the Drum **1.10** in FIGURE 1. The output of each lower order position of the MQ Register is connected as an input to the next higher order position, for example, the output **8***f*.**01**.**35** of Position **35**, FIGURE 2*gg*, is connected to the input of position **34** and so forth in like manner until the final connection is made between the output of position **1** and the input of position S, FIGURE 2*dd*, of the MQ Register for left shifting. Furthermore, outputs are provided from each higher order position of the MQ Register to each adjacent lower order position beginning with the output **8***a*.**04**S of position S to the input of position **1** and ending in like manner with connections from the final one of the outputs **8***e*.**03**.**34** to the input of position **35**. A single input **68**.**01**, FIGURE 2*gg*, is supplied to position **35** of the MQ Register from "One to MQ" Register, FIGURE 68.

Output lines are provided from positions **3** through **17** of the Address Register, FIGURE 2*i*, to positions **3** through **17** of the Instruction Counter, FIGURE 2*v*, and outputs are provided from positions **3** through **17** of the Instruction Counter as inputs to positions **3** through **17** of the Address Register. Inputs are provided from Address Register, FIGURE 2*i*, positions **10** through **17** to the Instruction Register positions **10** through **17**. An input is provided to position S of the Storage Register from **3**.**10**.**01** Primary Operation Decoder, FIGURES 14*a* through 14*d*.

Control of Data Flow

With reference to the Central Processing Unit, FIGURES 2*a–gg*, the flow of data is controlled in the following manner: Operator's Entry Keys S, **1** through **35**, FIGURE 2*e*, via cable **12**.**01**, then in parallel by the individual wires of the cables **12**.**01**.S, **12**.**01**.**01**, etc. to the Storage Register positions S, **1** through **35**, FIGURE 2*b–d*, to "Operator Panel Keys to Storage Register Control," FIGURE 73, which controls entry into positions S, **1** through **35** of the Storage Register, FIGURES 2*b–d*, or instead under control of "Complement Indicators to Storage Register," FIGURE 97; the Indicator Register S, **1** through **35** are fed from the outputs of the Storage Register positions S, **1** through **35** via a cable under control of the "Reset Indicators," FIGURE 93 (see also FIG. 2*a*), "Set Indicators," FIGURE 94, or "Invert Indicators," FIGURE 95, controls. "Electronic Reset of Indicators Control" is also provided in FIGURES 92 (see line **92.01**) and 2*a*.

Data may also be transferred from positions **1** through **35** of the Storage Bus Switching, FIGURES 2*w–y*, via a cable to respective inputs of the Storage Register, FIGURES 2*b–d*, under control of "Storage Bus to Storage Register Control," FIGURE 53. Data is transferred via cable from positions S, **1** through **35** of the Storage Register, FIGURES 2*b–d*, to positions S, **1** through **35** of the MQ Register, FIGURES 2*dd–gg*, under control of "Storage Register to MQ Register Controls," FIGURE 63. Outputs from positions S, **1** through **35** of the Storage Register, FIGURES 2*b–d*, are connected to positions P, **1** through **35** of the Adder Register, FIGURES 2*j–u*, for entry of data in response to operation of Storage Register to Adder Control, FIGURE 54. Data are also transferred between positions **18** through **35** only of the Storage Register, FIGURES 2*c* and *d*, to positions P through **17** of the Adder under control of "Storage Register (**18—35**) to Adder (P–**17**) Control," FIGURE 86*a*. Six positions of data (**1–5**) contained in positions S, **1** through **35** of the Storage Register, FIGURES 2*b–d*, may be entered into positions **30** through **35** of the MQ Register, FIGURE 2*gg*, by means of "Convert Controls," FIGURE 36. The negative of the contents of selected ones of the orders of the Index Register, FIGURES 2*f* and *g*, are provided to positions **3** through **17** of the Adder by means of "Index Register to Adders Gating Line," FIGURE 51. True outputs of positions Q, P, **1** through **35** of the Accumulator Register, FIGURES 2*z–cc*, are transferred to positions Q, P, **1** through **35** of the Adders by means of the "True Accumulator to Adders Control," FIGURES 55*a* and *b*. The complement of the Accumulator positions Q, P, and **1** through **35** are provided to positions Q, P, **1** through **35** of the Adder under control of "Complement Accumulator to Adder," FIGURES 55*c* and *d*. Carry output of position P, of the Adder is provided to the input of position **35** of the Adder by means of "Carry to Adder" **35**, FIGURE 56. The contents of positions **3** through **17** of the Adders are supplied to selected ones of the Index Registers, FIGURES 2*f* and *g*, in response to operation of "Adders to Index Register Gating Line," FIGURE 50. The contents of Adder positions **3** through **17** are transferred to the Address Register, FIGURE 2*i*, in response to operation of "Address Switch Input Controls," FIGURE 110. The contents of positions **1** through **8** of the Adders are transferred to positions **1** through **8** of the MQ Register, FIGURES 2*dd*, 2*ee*, in response to operation of the Adders **1–8** to MQ**1–8** Controls, FIGURE 84. The Contents of the Accumulator positions **30** through **35**, FIGURE 2*cc*, are transferred to the Adder positions **12** through **17**, FIGURES 2*o–2q*, in response to operation of "Convert Controls," FIGURES 36*a* and *b*. The contents of positions S, **1** through **5** of the Storage Bus FIGURE 2*u*, are entered in positions P, **1** through **5** of the Accumulator, FIGURES 2*aa–2bb*, in response of operation of Convert Controls, FIGURES 36*a* and *b*, which contents of Storage Bus Switching may be from Accumulator Register, the MQ Register or the Indicator Register as specified by the controls of Storage Bus Switching. Storage Bus Switching, FIGURES 2*w–y*, is not a storage device in the sense that a register is and it merely transfers information from the Accumulator Register, the MQ Register and the Indicator Register to the Storage Busses. The contents of the Address Register, positions **3** through **17**, FIGURE 2*i*, may be placed in positions **3** through **17** of positions **21** through **35** of Storage Bus Switching, FIGURES *w–y*, in response to operation of "Address Switches to Storage Bus **3—17** and **21—35**" of FIGURE 75. The contents of the MQ Register may be transferred to the Storage Busses via Storage Bus Switching by means of "MQ Registers S, **1—35** to Storage Bus S, **1—35** Control," FIGURE 74. The contents of the Accumulator may be placed on the Storage Busses via Storage Bus Switching by means of "Accumulator to Storage Bus," FIGURE 72. The Instruction Register, FIGURE 2*h*, is controlled by means of Shift Counter Pulse Generator **1** or Shift Counter Pulse Generator **2**, FIGURES 101 and 102. Data on the Storage Bus may be entered into the MQ by means of "I/O Bus S, **1—35** to MQ Register Control," FIGURE 69. A word from the Drum, FIGURE 1, **14** may be entered into the MQ Register positions S, **1** through **35** by way of the I/O Bus in response to operation of "I/O Bus, S, **1—35** to MQ Register S, **1—35**," FIGURE 69. The contents of the Address Register, FIGURE 2*i*, may be placed in the Address

Register by means of the "Control Address Switch Input," FIGURE 110.

Control Flow

There are two general types of control words, namely an Instruction and a Command, both having an operation part and an address part. For the purposes of explanation an Instruction is defined as a configuration of thirty-six bits which is decoded by the decoder of the Central Processing Unit for the purpose of controlling an operation to be performed by the Central Processing Unit. This operation, if it be an Instruction for an Input-Output type of operation, is transmitted to a Data Synchronizer channel. The second type of control word is known as a Command, and is similar to an Instruction except it enteds Transmission Registers of the Data Synchronizer Channel through which it acts like an Instruction and Controls that kind of an operation dealing with the transmission of data between a Data Synchronizer Channel and Core Storage. Commands are decoded by the Transmission Register in a DSC. The difference between the two is that Instructions enter and are decoded by the Central Processing Unit whereas Commands enter and are decoded by the Data Synchronizer Channel.

For a better understanding of the operation of the system, control is divided into two sub-control levels, namely, initial control and operation control. Initial control means those control functions necessary to initiate an Input-Output operation and originates in the Central Processing Unit while operational control comprises those control functions necessary to maintain operation once started and to insure a proper completion. For example, during a system operation a Central Processing Unit instruction is needed to initiate any tape operation. Once started, initial control is then passed to the Data Synchronizer concerned, then to the Tape Control Unit, and finally to the Tape Drive Unit selected. Once each unit has satisfied its initial requirement, the control is then held by the units necessary to complete the operation desired. It is seen here, that except for initial operation, the Central Processing Unit is needed in the tape operation for one purpose only, which is to provide the Data Synchronizer Channel access to Core Storage, when such access is needed. For any one tape system (Tape Control Unit and connected Tape Drive Units), this will occur no more frequently than once every 400 microseconds. The Central Processing Unit is otherwise free during this time to pursue its other activities while operational control rests with the Data Synchronizer, the Tape Control Unit and the Tape Drive Unit.

The major function of the operational control is to determine when the other units involved will perform their specific functions to accomplish the given over-all operation. The function of the control logic circuits between the Data Synchronizer Unit and the Central Processing Unit is to determine when the Central Processing Unit will provide the Data Synchronizer needs access to Core Storage, to store or obtain a word. The function of the control logic circuits between the Tape Control Unit and the Data Synchronizer unit is multiple: (*a*) It indicates to the Data Synchronizer Unit when the Tape Control Unit has a word ready or needs a word, (*b*) it indicates when an operation is completed and whether completed by the Data Synchronizer or the Tape Control Unit, and (*c*) it also indicates the occurrence of special conditions, such as an error. The function of the control logic circuits between the Tape Drive Unit and the Tape Control Unit is to indicate to the Tape Control Unit when the Tape Drive Unit is ready to perform an operation, when it is performing an operation, and when it has completed an operation. In each of the operational control functions, a complete interlock between all units involved is maintained until the operation is complete.

Machine Timing

The fundamental machine cycle of the Central Processing Unit (CPU) is 12 microseconds. One cycle is the duration of Core Storage access time which is the time required by the Central Processing Unit to transmit to or receive a word of information from Core Storage. The time required to transmit information between the Core Storage and any of the Input-Output units via one of the Data Synchronizers is given later when the timing relationship of the Input-Output devices in relation to the basic machine cycles are discussed. The fundamental machine cycles may be Instruction (I) cycles, Execution (E) cycles, Execute-Route (E/R) cycles and B cycles, each of 12 microseconds duration. I cycles are required to make references to Memory to obtain Instructions and to distinguish instruction words from data words. Execution (E) cycles are required for the Central Processing Unit and the Data Synchronizer Unit to make reference to Memory in order to bring data from Core Storage into the units or to enter words into Storage. E/R cycles are required by the CPU for operations without references to Memory. B cycles are references to Core Storage by the Data Synchronizer channel and differ from E cycles only in the manner in which they arise and the fact that the Central Processing Unit may not make reference to Core Storage during this time. There are particular cycles where references are made to Core Storage for the Central Processing Unit's purpose, but Control Word data is also stored in the Data Synchronizer Channel. Simply stated, the CPU and DSC do have access to memory at the same time for certain instructions during I and E times but, of course, the only time that this is true is when the same information can be used or if it is common to both units.

The timing circuits comprise an Oscillator, FIGURE 114, which oscillates at a frequency of 1 megacycle and provides signals to an Inverted Sync Generator, FIGURE 115. The Inverted Sync Generator provides inverted sync pulses on one output and pulses on another output to the Inverted Clamp Generator and Clock Drive, FIGURE 116, the latter having 2 outputs, an inverted clamp line and a drive line to the Clock, FIGURE 117. The Clock provides the 12 master timing pulses, labelled Master **A0** through Master **A11** under control of the 1 megacycle oscillator by using a ring of 12 triggers fed by the oscillator in a manner well known in the art. The signals on the Inverted Clamp Line from FIGURE 116 and the Inverted Sync Line, FIGURE 115, are special signals required by the Microsecond Delay and Storage Units in the Storage Register, Accumulator Register and MQ Register. The Inverted Synchronizing pulse on line **115.01** is a positive pulse having a duration of approximately 0.3 of a microsecond and the clamp pulse on line **116.01** is a negative pulse having duration of approximately .02 microsecond. Both pulses are repeated at the megacycle rate of the Oscillator, FIGURE 114, and are in phase with each other which is necessary for proper operation of the Microsecond Delay Units as described hereafter. A Cycle Timer Control, FIGURE 118, utilizes inputs from various command controls and operation controls for providing outputs to a Cycle Timer Gate Generator, FIGURE 119, and to Cycle Timer Output Circuits, FIGURE 120. The Cycle Timer Output Circuits provide outputs **120.01**; **120.02** and **120.03** indicative of the type of cycle that the machine is to operate in, that is, whether the cycle shall be an instruction (I) cycle, Execution (E) cycle or Execute-Route (E/R) cycle and one and only one of the outputs indicative of I, E, or E/R time is up at any time. Each output stays up for a minimum duration of one 12 microsecond clock cycle. The Cycle Timer Control, FIGURE 118, provides instruction signals to the Cycle Timer Output Circuits, FIGURE 120, labeled Go to E Time, **118.01**, Go to E/R Time **118.03**, and Go to I Time **118.14**. Other inputs are provided to the Cycle Timer Gate Generator, FIGURE 119, having outputs Reset Cycle Timer **119.01**, Set Cycle Timer

119.02, and B Time Control circuits 119.03. The B Time Control, FIGURE 121, has inputs from the Primary Operation Decoder, Instruction Register and certain other control and timing units for generating outputs concerning B time. A Pulse and Gate Generator, FIGURE 122, generates output signals in response to master timing pulses, type of cycle, and instruction controls.

When the Input-Output units are not being used the Cycle Timer Control follows this sequence: During the last machine cycle pertaining to a previous instruction, a signal is sent to the Cycle Timer Control, FIGURE 118, indicating that the previous operation is complete and that the Central Processing Unit is to proceed to I time for the purpose of interrogating Core Storage for the next instruction according to usual stored program techniques. When this has been accomplished, at Lead-In Instruction time (around I0 time in I time) the new instruction is decoded. Immediately following the decoding of this instruction, its type of instruction is known as well as whether or not another reference to Core Storage is required. For instance, if the instruction is Add this requires another reference to Core Storage to bring in the data to be added. Therefore, the Central Processing Unit is so controlled that its next machine cycle is an E cycle which provides a reference to Core Storage. In case of a store instruction, the same would apply, except that this time the references to Memory would cause information to be moved from a register in the Central Processing Unit to Core Storage. During execution of some instructions, references to Memory may not be required as in the case of multiply, which does not require more than the initial reference to memory to get the multiplicand after which a series of E/R cycles are required in order to actually carry out the iterative addition and shifting by the Central Processing Unit in order to perform the multiplication. Only the initial reference to Storage is required.

In addition to the three basic cycles I, E and E/R there is the B (Buffer) cycle referred to previously which results from the inter-action between a Data Synchronizer Channel and the CPU requiring a reference to Storage. B cycles do not provide data simultaneously to the DSU and CPU but frequently data is sent to a DSC simultaneously with control information being sent to the CPU and vice versa.

Instruction Counter

The Instruction Counter, FIGURE 2*v*, determines the address in Core Storage involved during an Instruction cycle. In the normal progress of the program, sequential addresses in storage are interrogated during successive I times because the Instruction Counter normally receives a pulse at the end of each operation to step it up 1 so that a succeeding higher numbered address is referred to on the next Instruction cycle. The orders of the Counter are labelled 3 through 17 in order to agree with the corresponding orders of the Address Register, FIGURE 2*i*. The loading of the instruction counter occurs at the beginning of each Instruction cycle as will later be described and determines the address of the word comprising the next Instruction except in those I times following a Halt, a successful Transfer or Branch and in certain operations such as Skip which advances the Instruction Counter more than one to cause skipping of instructions.

Instruction Register

The Instruction Register, FIGURE 2*h*, stores and operates on the information normally received from Magnetic Core Storage as a result of an Instruction cycle until the instruction is completely executed when it is reset during the early part of the next instruction cycle prior to receiving a new instruction. At every I8 time of the Instruction cycle, a one microsecond pulse (abbreviated D1) (see FIG. 2*h*), causes positions S, 1—9 of the Instruction Register to be reset to 0 and at the same time positions 10 through 17, and the Shift Counter of the Indicator Register, are reset to 1. The layout of the Instruction Register is as follows: Sign in position S; primary operation, positions 1 through 5; secondary operation, positions 6 through 9; and advance or shift counter data, positions 10 through 17. The information read from the Storage Register, FIGURES 2*b–d*, into the Instruction Register includes the sign, the primary operation part, and the secondary operation part of the Control Word, while positions 10 through 17 of the Instruction Register receive information from the Address Register, FIGURE 2*i*.

On a type A instruction (those that contain a prefix), bits 1 and 2 of the Storage Register are read into positions 8 and 9 of the Instruction Register. All B type instructions (those that do not contain a prefix) read positions 3 through 11 of the Storage Register into positions 1 through 9 of the Instruction Register. During the Instruction cycle, the sign bit in the Storage Register is transferred into the S position of the Instruction Register, where it has no algebraic significance but is used only to expand the capacity of the register, and, thus, make it possible to decode more instructions.

Primary Operation Decoder

Orders 1—5 of the Instruction Register, FIGURE 13, store the primary operation part of the instruction to be performed. The double outputs of each of these orders are analyzed in the Primary Operation Decoder, FIGURE 14, which resolves the five conjugate pairs of signals into one signal on one of 32 possible decoder output lines. Since only 32 outputs are available from the Primary Operation Decoder and 189 computer operations must be provided for, it is necessary to further employ the output of the Primary Operation Decoder by combining it with bits stored in other orders of the Instruction Register to expand the number of instructions over that offered by the Primary Operation Decoder.

Secondary Operation Decoder

A sense type instruction has its primary code stored in the primary operation part of the Instruction Register while the type of Sense is stored in the secondary operation part. For example, in Read Select 0762, the 7 and the 6 are represented by bits in orders 1 through 5 of the Instruction Register while the 2 is indicated by a binary bit in column 8. Whenever an instruction with a primary operation code 7, 6 is decoded the secondary operation part of the instruction is sampled into the Secondary Operation Decoder, FIGURE 15, to bring up a secondary operation output of (0, 2). On the non-indexable instruction, column 8 and 9 of the decoder contain the prefix which was transferred from columns 1 and 2 of the Storage Register. Like the primary part of the Instruction Register, the secondary part is rest at I8 (D1) and read at I9 time.

Address Part of the Instruction Register (Shift Counter)

The 8 positions of the address part, FIGURE 2*i*, of the Instruction Register form a count-down counter of eight triggers which has a capacity of 255 places. This counter is reset to 1 every I8 (D3) and on a Shift Instruction the number of places to be shifted is placed in the Shift Counter by turning "Off" the appropriate triggers at I12 time. The shift counter is impulsed every microsecond under a machine cycle gate and as the counter goes to 0, it signals the end of the shifting operation. Similarly, shifting during Multiply, Divide and Floating Point operations are controlled by the Shift Counter.

When using a Sense of an Input-Output Unit Instruction, the Address part of the instruction is read into the Shift Counter at I12 time through the address Switch Controls and the output of the Shift Counter during this type of an Instruction are fed to the Class and Unit Select Matrices, FIGURES 149, 150, which in turn feed the Class and Unit selectors, FIGURES 151–160. It is

pointed out that Shift Counter is reset with all triggers "On" and that zeros are then set into the counter since to set it to its proper setting the counter is of the count-down type and the normal reset and set of the counter would cause an erroneous carry.

Address Switches

The Address Switches, FIGURE 110, sample either the Instruction Counter outputs or Adder outputs of positions 3 through 17. In order to store the Index Register in the decrement portion of the Storage Register or to display the effective address, it is necessary to route the Adder outputs 3 through 17 through the Address Switches to the Storage Bus Switches, FIGURES 2*w–y*.

Sign Mixing Circuits

The Sign Mixer Circuits, FIGURE 113, combine all the outputs from the sign bits of the Storage Register, FIGURES 2*b–d*, the Accumulator Register, FIGURES 2*z*–22, and the MQ Register, FIGURE 2*dd–gg* to provide signals indicating that the signs are alike or unlike, and also provide signals from the Instruction Register, FIGURE 2*h*, indicating when the Address counter reaches the desired count during a Multiply or Divide operation.

Summary of Timing Considerations

Every I time the information from Storage is operated on as an Instruction and the location interrogated during the Instruction cycle is selected by the Instruction Counter, FIGURE 2*v*. When the End Operation Trigger comes on near the end of last cycle of the previous operation the contents of the Instruction Counter are gated through to the Address Register, FIGURE 2*i*, at I0(D1) time. The contents of the Address Register at this time indicate the location in Storage that is to be interrogated for a new Instruction. At I2(D1) time, the contents of the Address Register are delivered to the Storage Address Register, FIGURE 2*hh* (FIGURE 129), of the Core Storage Unit.

When the Storage Address Register has received the address and instruction, it controls the interrogation of the specified location and at I4¾ (D½) time places the contents on the Storage Bus I5 to CT 0.5 of next cycle. At I7 (D1) the information on the Storage Busses is referred into Storage Register, FIGURES 2*b, c, d*. In preparation for the decoding of this Instruction, the Instruction Register is reset at I8 time. If there is a bit in Storage Register positions 1 or 2 then data from positions 1 and 2 are placed in the Instruction Register positions 8 and 9 at I9 (D1). However, if no bit is present in Storage Register positions 1 or 2, then the bits in Storage Register orders 3 through 11 are set into the Instruction Register at positions 1 through 9, I9 (D1) time. Regardless of the condition of orders 1 and 2, the content of the sign (S) position of the Storage Register is sent into the Instruction Register S position at I9 (D1). The instruction code is received by the Instruction Register at I9 time and is decoded by the Primary Operation Decoder, FIGURE 14, from I9.5 until the succeeding I8 time. The output of the Primary Operation decoder prescribes commands for various arithmetic and logical operations and because of the large number of types of Instructions and the limited capacity of the Primary Operation Decoder, it is necessary to use also outputs 6 through 9 of Instruction Registers along with the outputs of the Primary Operation Decoder for decoding purposes.

The number stored in the Instruction Counter, FIGURE 2*v*, is advanced by 1 at I11 (D1) to effect the interrogation of the next sequential Core Storage address during the succeeding I cycle. This is the normal advance and the advance is only suppressed in special cases as stated above. By this time the program circuits have caused the decoding of the Instruction which controls the types of cycles to follow I time and the Instruction Counter is set for the next sequential address.

When the instruction has been completed, a command line End of Operation control, FIGURE 128, is brought up to turn ON the End Operations Trigger, FIGURE 118, at 10 time of the last cycle of the operation which signals the Cycle Timer to proceed to I time and bring out the next instruction.

Overflow and Carry Triggers and Controls

In FIGURE 123 there is shown two triggers, one for storing the fact that an Overflow has occurred and the other for storing the fact that a Carry out of column Q of the Adder has occurred. A pair of triggers are used in FIGURES 124, one for indicating the presence or absence of a carry into position 9 of Adder and another trigger for indicating the carry out of column 9. In FIGURE 125, there is shown a pair of triggers, one for indicating Floating Point Overflow and the other for indicating Floating Point Underflow. There is shown a trigger in FIGURE 126 which has an input from a predetermined Adder depending upon the size of Core Storage that is used in the system. In this instance, there is a Carry output from Adder 6 to this trigger. Although Locate Drum Address, LDA, is not used in the explanation of this embodiment of this invention and is not explained in detail, the fact that Locate Drum Address is not used is pertinent to the extent that the associated controls are down.

In connection with Floating Point Overflow and Underflow detection circuits of FIGURE 127 provide outputs indicative of Floating Point Overflow and Minus on Adder Q sum. In FIGURES 128*a, b* and *c*, there is shown the control circuits for End Operation, Storage End Operation in ER time and End Operation in E time.

Word Format

FIGURE 3*a* shows the layout of a type A instruction. These instructions use positions S, "1," and "2" for an operation code and are characterized by having a "1" in positions 1 and/or 2. All other instructions contain zeros in both positions "1" and "2." Instructions Transfer on Index TIX, Transfer on No Index TNX, Transfer on Index High TXH, Transfer with Index Incremented TXI, and Transfer on Index Low or Equal TXL use positions 3 through 17 as a decrement part, positions 18 through 20 as an index tag, and bits 21 through 35 as an address part. The index tag selects the Index Register, FIGURES 2*f* and 2*g*, to be modified and tested by the instruction. The decrement contains the modifications or test amount and the address specifies the storage location of the next instruction if the test condition is met. Another of these instructions uses only S, 1 and 2 and bits 3 through 35 have no effect on the execution of the instruction.

The format of a type B instruction is shown in FIGURE 3*b*, the shaded part representing the field not used by all type B instructions. These instructions are characterized by having an operation part in S, 1 through 11 (1 and 2 contains 0's), an index tag in 18 through 20 and an address part in 21 through 35 for Shift Instructions. Positions 12 and 13 are used as an indirect address tag by all type B Instructions except non-indexable, shift, input-output, variable multiple and variable divide instructions. Position 14 and 15 are not used by type B instructions.

FIGURE 3*c* shows the format of the type C instructions. Type C instructions use S, 1 through 9, as an operation part (1 and 2 contains 0's), 10 through 17 as a count, 18 through 20 as an index tag and 21 through 35 as an address part. Three of these instructions, Variable Length Multiply (VLM), Variable Length Divide or Halt (VDH) and Variable Length Divide or Proceed (VDP) are indexable and use the index tag for address modification. Convert by Replacement from Accumulator (CVR), Convert by Replacement from MQ (CRQ), and Convert by Addition from MQ (CAQ), are not in-

dexable and use position **20** of the index tag to indicate that the base address of a count cycle is to replace the contents of index register A. The number of convert cycles, the number of bits in the multiplier, or the number of bits to develop in the quotient is specified by the count. While the count field has a capacity of 255, a count larger than 47 may cause indirect addressing to take effect on VLM, VDH, VDP but not on Convert Instructions since such a count places bits in positions **12** and **13**. Bits through **21** and **35** specify the storage location of the operand or the base address of the first convert cycle.

FIGURE 3*d* shows the format of type D instruction. Type D instructions operate in conjunction with columns **0** through **17** or **18** through **35** of the Indicator Register, FIGURE 2*a*. The **18** bit mask used in Sense Indicator instructions is contained in the positions **18** through **35** of the instruction. Positions S, **1** through **11** contain the operation part with **1** and **2** containing zeros. Position S is used to denote whether the columns left (**0** through **17**) or columns right (**18** through **35**) positions of the Indicator Register are used in the instruction. If S contains a "1," the left positions are used, and if S contains a "0," the right positions are used.

In FIGURE 3*e*, the format of type E instructions is shown. These are defined by plus or minus 0760 in positions S, **1** through **11**, do not contain an adress part, and use positions **24** through **35** as part of the operation code. Address modification through an index register is specified by positions **18** through **20**, is not prohibited but may cause the operation to be changed.

Data Synchronizer operation makes use of three word formats as shown in FIGURES 3*f* and 3*g* and 3*h*. Word formats of FIGURES 3*f* and 3*g* illustrate an instruction word (Control Word) sent to DSC from storage and FIGURE 3*h* illustrates a word sent from a DSC to storage. The normal DSC control word specifies the number of words to be transmitted (Word Count) in positions **3** through **17** and specifies the initial storage location in positions **21** through **35** to which data is to be sent or taken from. DSC control is specified by positions S, **1**, **2** and **19** and the use of these positions for DSC control are described in detail hereafter. The special DSC control word in FIGURE 3*g* is a word which modifies the sequential location of other control words for the Data synchronizer as described later. Positions S and **1** contains 0's, position **2** must contain a 1 and position **19** contains a zero. Positions **21** through **35** give the location of the next control word to be used by the DSC.

FIGURE 3*h* shows the format of an instruction word when a store DSC instruction is executed. The storage location from which the next control word is taken is specified in positions **3** through **17** (location). The storage address of the next word of data is specified in positions **21** through **35** (Address).

FIGURE 3*i* illustrates the layout of a Floating Point instruction. The magnitude of the binary fraction is given by positions **9** through **35** and the sign of the binary fraction is given in position S. The binary characteristic of the fraction (binary exponent +128) is stored in positions **1** through **8**.

In FIGURE 3*j*, a Fixed Point instruction is illustrated. In fixed-point arithmetic, the 36 bit word in storage is interpreted as containing a sign in S and a 35 bit magnitude in poistions **1** through **35**. In logical operations, the word is treated as a 36 bit unsigned quantity.

In FIGURE 3*k*, a six character binary coded data (BCD) word format is indicated. It will be discussed in some detail later.

The Central Processing Unit distinguishes between instructions and data information by the type of cycle selected. Words read out of memory during an instruction cycle are channeled to the Instruction Register where the stored manifestations of the bits comprise a representation of the instruction. Information read from memory during an execute cycle is always handled as numeric data.

Automatic Address Modification

When an iterative program operates on different items of data during each step of the iteration, it is necessary to change the addresses of instructions which further refer to this data before each iteration. Without the use of automatic address modification, instructions which change the addresses of other instructions may constitute a large number of instructions in a given program. When the address of the instruction is brought to the Storage Address Register, it passes first through the Adders and Address Switches. If indexing (address modification) is desired the 2's complement of the amount in one of a chosen of the Index Registers is brought into the Adders at the same time in positions **3—17**. The result of this adder operation is that the Address Switches receive the difference between the address and the contents of the selected Index Register and this difference is known as effective address. The execution of the instruction proceeds in the usual manner using the effective address. Each index register serves as an accumulator register so that its contents can be increased and decreased by the execution of certain indexing instructions. The Index Register can receive information from either the decrement portion or the address portion of the instructions, from the Accumulator or from the Instruction Counter and it can send information to Adders for address modification, to the Accumulator or to Storage. Selection of an Index Register is made by bits in Storage Register locations **18**, **19** and **20**. Further address modifications may be had by providing bits in positions **12** and **13** in the Storage Register. By means of controls, FIGURE 98, the contents of the Storage location referred to are not added, but instead the address found at this Storage location specifies the location from which data are to be added to the Accumulator. Both of these addresses may be indexed by the same or different Index Registers, each word containing its own tag in positions **18**, **19** and **20**. Indirect addressing may be used with all indexable transfer instructions and with all other indexable instructions which make a reference to Storage.

Magnetic Core Storage Organization

Referring now, in general, to FIGURES 2*hh* through 11 and specifically to FIGURES 129 through 147, the Data Processing System employs a three dimensional Magnetic Core Storage Device and associated storage controls. Outputs from the Address Register, FIGURE 2*i*, and DSU Address Switches, FIGURE 2*ww*, are provided as inputs to a Storage Address Register shown in FIGURE 2*hh*, the specific logical contents of which are shown in FIGURE 129. Certain timing pulses are provided to a Pulse Generator shown generally in FIGURE 2*jj* and specifically in FIGURES 130*a*, *b* and *c* which provides output signals to the Memory Address Register, FIGURE 2*hh*. The Memory Address Register provides outputs to an X Address Decoder, FIGURES 131*a* and 132*b*, and to Y Address Decorder, FIGURES 132*a* and 131*b*. Both the X and Y Address Decoders have outputs to respective ones of a pair of Read Bias and Write Gate Mixing Circuits, FIGURE 133. Timing pulses are provided from a Read-Write Gate generator, FIGURES 134*a* and *b*, to the Gate Mixing Circuits; to the X and Y Address Decoders, FIGURES 131*a* and 132*b* and 132*a* and 131*b*, respectively; and to the Read Bias and Write Gate Mixing controls, FIGURE 133. Output lines 133.01 and 133.02 are provided from Read Bias and Write Gate Mixing circuits to the inputs of an X Matrix Switch Write Driver, FIGURE 135. Outputs **131A.01–08** are provided from the X Address Decoder to an X Matrix Switch Read Driver, FIGURE 136, and outputs **131*b*.0.–08** are provided from FIG. 131*b* to Read Bias and Write Gate Mixing Circuits, FIGURE 133. Connections are made according to FIGURE 135 between Gate Mixing, FIG-

URE 133, and an X Driver Matrix Switch, FIGURE 141*a*. The **64** output lines of this X Driver Matrix Switch are provided as inputs to the Core Array, FIGURE 138*a*, each output drives one of **64**X drive lines in the array as indicated in FIG. 138*a* when that driver line has been addressed. Outputs are provided from a Read Bias and Write Gate Mixing, FIGURE 133, to the Y Matrix Switch Write Driver, FIGURE 139, and outputs are provided from the Y Address Decoder to the Y Matrix Switch Read Driver, FIGURE 140. Connections are made according to FIGURE 133 between the Address Decoder, FIGURE 131*a*, and a Y Matrix Switch, FIGURE 139. Outputs **132A.01–08** are provided as inputs to the Y Matrix Switch Read Driver, FIGURE 140, and connections are made according to FIGURE 140 to the Y Driver Matrix Switch, FIGURE 137*a*. Sixty-four Y Drive lines of Y Matrix Driver Switch, FIGURE 137*a*, are provided to the Core Array, FIGURE 138. Thirty-six digit windings shown in FIGURE 138 are provided to inhibit the writing of a "1" in a selected core as will be described in detail later.

Communications with Core Storage from either the Central Processing Unit or Input-Output devices are made through a Sense Amplifier Buffer and Input-Output Switching Register, FIGURES 2–11 (FIGURE 142). Outputs **142A.03**; **142A.04**; **142A.05**; **142B.03**; **142B.04**; **142C.03** and provided to Storage Bus Switching, FIGURES 2*w–y* (FIGURES 11*b, c, d*) and 36 output lines **142.01** are provided as inputs to a Digit Plane Select Circuits FIGURE 143. Thirty-six outputs of the Digit Plane Select Circuits are provided to a Digit Plane Driver Unit, FIGURE 144; the latter having 36 digit plane drive outputs which are connected to the Core Array, FIGURE 138, as previously described. With the energization of a selected X and Y line, outputs from cores at the selected address are present at the Sense windings of the Core Array to the input of the Sense Amplifier Buffer and I/O Switching, FIGURE 142. Control lines are provided to the Sense Amplifier Buffer and I/O Switching, FIGURE 142, by way of an Address and Operations Control, FIGURE 145 and, in turn, by way of Read-Write Control, FIGURE 146. (Adders and operations control are part of CPU) (Inputs to the Adders and Operations Control are from the Central Processing Unit and are shown specifically in FIGURE 145.) Inputs are provided to the Test Circuits shown generally as FIGURES 147*a, b* and *c* from the Sense Amplifier Buffer and I/O Switching Register and from the Pulse Generator, FIGURES 130*a* and *b*. An understanding of the Test Circuits is not necessary for an understanding of the invention. Accordingly, no specific details are mentioned except in those instances where a control line is operated as an incident to the operation of Core Storage.

In FIGURE 138, there is shown a diagrammatical view of a Core Array in which cores are arranged in square arrays such that each core is situated at the junction of two mutually perpendicular single turn windings that are called the X and Y windings. If I is the minimum current necessary to change a core from the "zero" state to the "one" state then if current

$$\frac{I}{2}$$

is supplied to the single X and a single Y winding, the only core which can change state is the one at the intersection of these two windings. Four windings actually pass through each core and are called the X, Y Digit and Sense Windings as shown in FIGURE 138*b*. The planes are stacked vertically to form a three dimensional array of 36 planes, each X or Y winding being connected in series with the corresponding X or Y winding in the planes above or below it. Currents of

$$\frac{I}{2}$$

are applied to one X and one Y winding and a vertical line of cores is selected at the intersection of the planes at which the X and Y windings lie. The Digit and Sense windings, however, are not connected between the various planes. The process of reading information from the selected vertical line of cores leaves that line of cores of 36 positions in "zero" state and, therefore, to prevent the loss of the information read out it becomes necessary to write "ones" in those cores which has previously contained "ones." This process is accomplished producing magnetizing currents for writing "ones" in the entire line of cores, but whenever a "zero" should appear, an inhibit signal is returned to the plane associated with that digit from the digit winding to cancel a portion of the magnetizing effect which suppresses the writing of a "one" in that plane. More specifically, during the Write cycle the Core Plane Address to be written first receives a Read pulse which changes the full address of 36 positions to "zero." The Sense winding output is supressed at the output of the Sense Amplifier which prevents setting the Storage Buffer triggers to the contents of the Address which has been read from. At Write time the Read in sample together with the Storage Bus outputs either turns on the Buffer Triggers for those outputs containing a "one" or leaves it off as in the case of reading a "zero." After the Buffer Triggers have been set, the Write current is sent to all 36 cores of the Address to be written tending to cause all "ones" to be read into that Address. Where "zero" is to be written into a particular core the writing of the "one" is suppressed by the Storage Buffer Lines **142*a*.01S** through **142*a*.01.11**; **142*b*.01.12**; **142*b*.01.23**; **142*c*.01.24**; **142*c*.01.35** which go to the Digit Plane Select circuits of FIGURE 143 to bring up the Digit Plane Select lines **143.01S** through **143.01.35** to inhibit "ones" from being written into respective planes associated with each Digit Plane Select winding. Since a Write operation is always preceded immediately by a Read operation during any selection of a Memory Address, the selected core is always in a "zero" state when writing starts. To write a "zero" into a core the X and Y windings are each pulsed simultaneously with current of

$$+\frac{I}{2}$$

and the Digit Plane winding receives an inhibit pulse of

$$-\frac{I}{2}$$

which results in a net of

$$+\frac{I}{2}$$

to the core which is insufficient to switch the core from "zero" to the "one" state.

Read and Write Operation

A Store Instruction is one that writes the contents or partial contents of a Central Processing Unit Register at an address in Core Storage specified by the Store Instruction. This is commonly referred to as Writing. Other instructions cause the contents of some Addresses in Core Storage to be read out and sent to the CPU for the purpose of adding, subtracting and so forth, depending upon the instruction, and this is referred to as Reading. For example, the instruction Store +0601 with an Address of 0700 (octal) is assumed to be located at Address 0777 (octal) in Core Storage. The Instruction Counter in the Central Processing Unit, FIGURE 2*v*, normally tells the machine where to go in Core Storage during an Instruction cycle and get the next instruction and in this example, contains the Address 0777 (octal) in the positions indicated below:

Instruction Counter Position	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
Contents	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Until I6 time the output of the Instruction Counter feeds the Address Register, FIGURE 2*i*, in the Central Processing Unit and the contents thereof are transferred into the Address Register at **10** (D1) time. At **12** time, the contents of the Address Register positions (FIGURE 2*i*) **6** through **17** or the contents of the DSU location Register are transferred to the Storage Address Register, FIGURE 2*hh*, located in Magnetic Core Storage. Each position of the Storage Address Register, FIGURE 129, has three outputs, making the total of thirty-six and is divided into four major divisions as shown schematically in FIGURE 148*a*: the group of bit positions **6**, **7** and **8** comprises the Thousands position; **9**, **10** and **11** comprise the Hundreds; the group of bit positions **12**, **13** and **14** comprise the Tens; and the group of bit positions **15**, **16** and **17** comprise the Units. Each of these four groups has six outputs **129***a*.**01**–**129***a*.**12** and **129***b*.**01**–**129***b*.**12**, labeled **6**, $\overline{6}$, **7**, $\overline{7}$ and so forth. The Address Decoder, FIGURE 132*b*, decodes positions **6**, **7**, and **8**; Address Decoder, FIGURE 131*a*, decodes positions **9**, **10** and **11**; Address Decoder, FIGURE 131*b*, decodes positions **12**, **13** and **14**; and Address Decoder, FIGURE 132*a*, decodes positions **15**, **16** and **17**. The address contained in the Storage Address Register and placed in the Address Decoders is 0777 (octal) and accordingly, in FIGURE 132*a*, Storage Address Register **15** line **129***b*.**08** is up; Storage Address Register **16** line **129***b*.**10** is up; Storage Address Register **17** line **129***b*.**12** is up; Storage Address Register $\overline{15}$ line **129***b*.**07** is down; Storage Address Register $\overline{16}$ line **129**.**09** is down; Storage Address Register $\overline{17}$ line **129***b*.**11** is down; and when the Read Gate line **134***a*.**02** comes up; Read Address **7** line **132***a*.**01** is up since all inputs to its AND circuit are up. In FIGURE 131*b*, Storage Address Register **12** line **129***b*.**02** is up; Storage Address Register **13** line **129***b*.**02** is up; Storage Address Register **14** line **129***b*.**04** is up; Storage Address Register $\overline{12}$ line **129***b*.**01** is down; Storage Address Register $\overline{13}$ line **129***b*.**03** is down; Storage Address Register $\overline{14}$ line **120***b*.**05** is down. Address **70** line **131***b*.**01** is up since all the inputs are up to its AND circuit. In FIGURE 131*a*, Storage Address Register $\overline{9}$ line **129***a*.**07** is down; Storage Address Register **9** line **129***a*.**08** is up; Storage Address Register $\overline{10}$ line **129***a*.**09** is down; Storage Address Register **10** line **129***a*.**10** is up; Storage Address Register $\overline{11}$ line **129***a*.**11** is down; and Storage Address Register **11** line **129***a*.**12** is up. When the Read Gate line **134***a*.**03** comes up, an output is provided on Read Address **700** line **131***a*.**01**, since all the inputs to its AND circuit are up. In FIGURE 132*b*, the Storage Address Register **6** line **129***a*.**02** is down; the Storage Address Register **7** line **129***a*.**04** is down; the Storage Address Register **8** line **129***a*.**06** is down; Storage Address Register $\overline{6}$ line **129***a*.**01** is up; Storage Address Register $\overline{7}$ line **129***a*.**03** is up; Storage Address Register $\overline{8}$ line **129***a*.**05** is up. Accordingly, an output is provided on an Address 000 line **132***b*.**08** since all of the inputs to its AND circuit are up. The outputs from the Tens and Thousands Decoders, FIGURES 131*b* and 132*b*, respectively, are available as soon as the Storage Address Register is read into at I2 (D1). However, the Units and Hundreds Decoders await a Read Gate pulse on lines **134***a*.**02** and **134***a*.**03** from the Read and Write Gate Generator before their outputs are up. This allows time to set up the biasing of the Switch Cores before the Selected Switch Cores are actually transferred. The outputs **131***b*.**01** and **132***b*.**08** for the Tens and Thousands Address Decoders are sent to Read Bias and Write Gate Mixing circuits, FIGURE 133, and here their outputs are logically inverted for providing from each of these circuits seven lines which are up and one which is down. The seven lines that are up from the Read Bias and Write Gate Mixing circuits for the Thousands Address Decoder are sent to the X Switch Core Matrix, FIGURE 135, and the seven lines which are up from the Mixing circuits from the Tens Decoder are sent to the Y Switch Core Matrix, FIGURE 139. As shown in Timing Chart, FIGURE 148*b*, both Switch Core Matrices are biased and a Read Gate Line comes up at approximately I3.5 time which allows the Units and Hundreds Address Decoders, FIGURES 132*a* and 131*a*, to select the correct Switch Core in both the X and Y Matrix.

With reference to FIGURE 138, the Read-Out of a 36 bit word from the 36 sense windings to the Buffer Register, FIGURE 142, is accomplished by the use of Switch Cores shown in FIGURES 137 and 141. Since each of the 36 Core Planes in the Core Storage Unit is a 64 x 64 Array the Two Switch Core Matrix Panels are used to provide 64 X Drive lines and 64 Y Drive lines as shown in FIGURE 138, at the top of the figure. FIGURE 137*a* shows an 8 x 8 Switch Core Matrix having 64 Y Drive Address lines which go to the Core Array shown in FIGURE 138. The cores shown diagrammatically in FIGURE 137*a* are each identified by an Address shown thereon and are illustrated in detail in FIGURE 137*b*. The Switching Cores have a substantially rectangular hysteresis loop with a Read winding having terminals identified by the numbers **1** and **9**, a Write winding having terminals identified as **4** and **6** and a Secondary winding having terminals **7** and **8** with the polarities as indicated by the dots shown in the figure. When the Write winding is energized, the switch core remains magnetized in the state representative of "zero"; and when current is provided to the Read winding, the switch core is magnetized in the opposite sense indicative of a "one." A switch core is said to switch when current is provided in the Read winding sufficient to cause a residual magnetism to change from "zero" to "one." Likewise, sufficient current in the Write winding switches the core from "one" to "zero." A magnetizing force applied through the Write winding has very little effect on the core already magnetized in that direction and a magnetizing force applied to the Read winding has little effect on a core already magnetized in that direction. The Write winding provides the biasing force which, when used simultaneously with a magnetizing force applied on the Read winding, prevents the core from switching due to cancellation of the flux.

The line pairs coming from the Y Matrix Switch Read, FIGURE 140, are related to the Units position, of the Address as previously mentioned, FIGURE 148*a*, so that the lines associated with the Units position Address are up and the other seven pairs of lines associated with the Non-Selected Units Address are down. For example, the Read Address **7** line **132***a*.**01** is up providing an input to the Matrix Switch Read Amplifier of FIGURE 140 bringing up the Read Driver input line to the Matrix Switch Driver, which provides current through the line **140.01**. In FIGURE 137*a*, the Matrix Switch Read Driver Address (**7**) line **140.01** is up which provides current through the series Read coils of the Switch Cores terminals **1** and **9** of Address Cores **77**, **67** and so forth through terminals **1** and **9** of Address (**07**) Switch Core and from the **9** terminal back to the Read Address **7** Feedback line **140.02**. The Read Address Feedback line is returned to the Y Matrix Switch Read Driver of FIGURE 140. In this regard, it is pointed out that current flows from a negative D.C. potential at the cathode to plate of the Matrix Switch Driver through the Read windings in series and through the Feedback line to the cathode of the Matrix Switch Read Amplifier and to ground through the lines **140.03**, shown in FIGURE 140. Since the cathods of the Matrix Switch Driver is at a negative potential of 130 volts essentially positive B+ is provided to the Matrix Switch Driver. Thus, the Read windings of the Switching Cores Address **77**, **67**, **57**, **47**, **37**, and **27**, **17** and **7** are carrying magnetizing current sufficient to cause a residual magnetism to change the state of from "zero" to "one."

Referring now to FIGURE 131*b*, the Tens Address Decoder, Address line **131***b*.**01** for Address **70** is up to the Write Driver Select circuits, FIGURE 133, but the Write Gate line **134***b*.**03** is not up until about **I9** time. However, the Address **70** line is up and inverted to an AND circuit at the more negative level. Even though the Read Bias Gate line **134***a*.**01** is up there is no output from the AND circuit since the inverted Address **70** line is down.

With reference to the Address Decoder, FIGURE 131*b*, it will be noted that although the **131***b*.**01** line is up that the other seven lines **131***b*.**02** through **131***b*.**08** are down. Accordingly, in the Write Driver Select circuits of FIGURE 133, the output of the Write Driver Select circuits for the Address **70** is down, but the outputs of the Write Driver Select circuits for the Addresses **60, 50, 40, 30, 20, 10** and **0** are down. Therefore, with reference again to FIGURE 133, the Address lines **131***b*.**02–08** being down provides outputs which are up from the inverters and the Read Bias Gate line **134***a*.**01** is up at **I2** near the beginning of the cycle providing outputs on lines **133.01** and **133.02** for Matrix Switch Write Driver lines for the Addresses **60, 50, 40, 30, 20, 10** and **0** as shown in FIGURE 137*a*. In FIGURE 137*a*, it will be noted that the Matrix Switch Write Driver Address line **70** is connected to the 4 terminal of the Address **77** core and that the 4 and the 6 terminals are those terminals for the Write coils which are connected in series from the Address **77** core through the Address **70** core. The 6 terminal of the last mentioned core is connected to the Write Address **70** Feedback line as shown. As previously mentioned, the Matrix Switch Write Driver Address **70** line is down and accordingly, current is not provided to the Write coils of the series-connected Switching Coils of Addresses **77—70**. However, current is supplied to the Write coils of the other rows of Address Switching cores by way of the Matrix Switch Write Drive Address **60, 50, 40, 30, 20, 10** and **0** lines as mentioned previously with regard to the Write Driver Select circuits of FIGURE 133. In summation, the Address Switching cores **77, 67, 57, 47, 37, 27, 17** and **07** have their Read coils energized; the Switching Cores Address **67, 57, 47, 37, 27, 17** and **07** also have their Write coils energized; the net effect on the last mentioned cores is that they are not switched, but the Address Core **77** is switched since it has only read current supplied. The Switching Cores **66–60**; **56–50**; **46–40**; **36–30**; **26–20**; **16–10**; and **6–0** receive current through their Write Coils which tends to switch the core from a "one" to a "zero." However, since the last mentioned cores are already at that state the magnetizing force is ineffective to change that state. The Switching Core Addresses **76, 75, 74, 73, 72, 71** and **70** have neither the Read nor the Write coils energized so that no change of state takes place. The Switch Core Address **77** has only the Read coil energized as previously described and is switched from "zero" to "one." This change of state from a "zero" to a "one" in effect induces a voltage in the secondary winding which is felt on the Y Drive Address **7** line which goes to Core Plane, FIGURE 138, and provides

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Similarly, the Hundreds Address is decoded, FIGURE 131*a*, and provides an input on line **131***a*.**01** to the X Matrix Switch Read Driver, FIGURE 136, to bring up the Read Address **700** Matrix Driver. The Thousands Address Decoder of FIGURE 132*b* inverts the selected output **132***b*.**08** in FIGURE 133 to provide one pair of output lines associated with the Address **0000** which is down and seven pairs associated with Addresses **7000—1000** which are up to the X Matrix Switch Core panel, FIGURE 141. Specifically, Matrix Switch Write Driver Addresses **7000, 6000, 5000, 4000, 3000, 2000** and **1000** are up whereas the Matrix Switch Write Driver Address **0** is down and the Switch Core Address **0700** is the only core which can change from the "zero" to the "one" state. This change is felt on the X Drive Address **0700** line which provides

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to the Selected X Drive line. Thirty-six cores are acted upon since each X or Y winding is connected in series with the corresponding X or Y windings in the planes above or below it. A Sense winding is threaded through all the cores in each plane so that in FIGURE 138 there are two terminals for the Sense winding for each plane and there are two terminals provided to the Sense Amplifier Buffer Register, FIGURES 142*a*, *b* and *c*. More specifically, two terminals from each of the thirty-six planes are applied to the input of the primary of the transformer, as shown in FIGURE 62, U.S. patent application Serial Number 592,545, filed July 6, 1956, title: Data Coordinator. For each plane having a "1" an output is provided from the Sense Amplifier to the AND circuit having two other inputs Read Control **146.03** and Read-Out Sample **130***a*.**07**. For a "1," an output is provided through the OR circuit and Cathode Follower to turn on the Buffer Register Trigger. When a "0" is being read, there is no output from the Sense Amplifier and accordingly, the trigger remains in a state indicative of a "zero." Since the Read-Out is destructive and the location (**0777**) specified by the Address now contains "zero," it is required that the word written out into the Buffer Register be read back into the Address specified, (**0777**).

It will now be described how "ones" are written in those cores of Address **0777** which had previously contained "ones" and which are now contained in the Storage Buffer Register, FIGURE 2*ll* (FIGURES 142*a*, *b*, *c*). This operation is accomplished by setting up circuits for writing "ones" in the entire line of cores, but in those positions in which a "zero" should appear, an inhibit signal is returned to those planes associated with the "zero" digits by way of the individually associated Digit Plane windings, which causes suppression of the writing of "ones" in those planes. The timing of the Inhibit Gate is shown in the Timing Chart, FIGURE 148*b*. After the Read-Out operation, the X and Y Switching Cores corresponding to the Address from which the information was read are in the "one" state. That is, they have been switched to provide an output in the Secondary which drives the cores in the Selected vertical line, FIGURE 138, from the "one" to the "zero" state to provide an output from the Sense windings indicative of the values contained in the selected thirty-six cores. To write the information contained in the Buffer Register back into the Core Array, advantage is taken of the fact that the Switch Cores for the Address Read-Out are now in the "one" state. During Write time all inputs to the Read Windings, FIGURES 136 and 140, of the Switch Core Matrices (FIGURES 137 and 141), are suppressed by a Read Gate lines **134***a*.**02** and **134***a*.**03** (FIGURES 132*a* and 131*a*). This is to say that the Read Gate provided on the line **134***a*.**02** to the Address Decoder circuit in FIGURE 132*a* and the Read Gate provided on the line **134***a*.**03** to the Address Decoder circuit in FIGURE 131*a* are down. Accordingly, there will be no output from either the Address Decoder, FIGURE 131*a*, or the Address Decoder, FIGURE 132*a*. The outputs of the Thousands Address Decoder, FIGURE 132*b*, and the Tens Address Decoder, FIGURE 131*b*, are not inverted. With reference to FIGURE 133, for example, the Read Bias Gate on line **134***a*.**01** is down which prohibits the passage of the inverted output from the Address line, but the Write Gate on the lines **134***b*.**03** is up which brings up the selected one of the Read Bias or Write Address lines which output is provided to the X Matrix Switch Write Driver Address (**0000**) lines of FIGURES 135 and 141. Similarly, the output of the Tens Address Decoder, FIGURE 131*b*, is passed through Read Bias and Write Gate Mixing, FIGURE 133, and is provided as an input to the Y Matrix Switch Write Driver Address (**70**)

line of FIGURES 139*a* and 137*a*. With reference now to the Y Driver Matrix Switch, FIGURE 137*a*, it will be noted that the inputs from Y Matrix Switch Read Driver, FIGURE 140, are all down and that the only input to the Y Driver Matrix Switch is on the Matrix Switch Write Driver Address **70** from FIGURE 139. Recalling now that the Address (**77**) Switch Core was the only one which was changed from the "zero" to the "one" state, it is apparent that the application of current to the Write coil causes the Address Switch core **77** to switch from the "one" to the "zero" state. However, other Switch cores are not affected in this manner since they are already in the "zero" state and the magnetizing force applied is therefore ineffectual to cause a significant voltage in the Sense Output winding or Secondary Output winding. These, of course, are the cores having Addresses **76, 75, 74, 73, 72, 71** and **70**. Accordingly, an output is provided on the Y Drive Address **77** line of FIGURE 137*a* to FIGURE 138. Similarly, with reference to the X Driver Matrix Switch, FIGURE 141*a*, the inputs from the X Matrix Switch Read Driver, FIGURE 136, are down and the only input from X Matrix Switch Write Driver, FIGURE 135, is provided on the Matrix Switch Write Driver Address (**0000**). It is pointed out that this provides the Write current to the Write coil of Switching Core Address **0700** which is the only core in the X Driver Matrix Switch Array which has been changed from the status of "zero" to "one." Therefore, this core when provided with a Write current in the absence of the Read current switches from "one" to "zero" and the voltage induced in the Secondary winding is provided on the X Drive Address line **0700** to the Core Array of FIGURE 138. Since a current of

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is provided to a selected one of the Y drive lines and a current of

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is provided to selected one of the X Drive lines shown in FIGURE 138 each of the thirty-six cores in the vertical line selected would normally be switched from the "zero" to the "one" state. However, through the use of the thirty-six digit plane windings, selected ones of the cores which were normally in the "zero" state prior to reading out will be preserved in the "zero" state in the following manner:

With reference to the Sense Amplifier Buffer Register and I/O Switching, FIGURES 142*a*, *b* and *c*, it will be noted that there is provided a line **142***a*.**01**, **142***b*.**01** and **142***c*.**01** which is Storage Bus Trigger (N) Off. Accordingly, when each Trigger in the Buffer Register is in the "Off" condition as indicated by conduction of the right-hand side of the Trigger, the left-hand side is "Off" with the plate at its higher positive potential which is interpreted on the output lines Storage Buffer Trigger (N) Off as the "Off" condition, and these outputs are provided from the Buffer Register to the Digit Plane Selector circuits, FIGURE 143. The inhibit Gate comes up at **18.5** and for each of the thirty-six positions containing a "zero" in the Buffer Register an output is provided from the Digit Plane Select circuits on selected ones of the lines **143.01**.S through **043.01.35**. The outputs are provided to the Digit Plane Driver in the manner shown in FIGURE 144 for driving the Digit Plane windings shown in FIGURE 138 for those of thirty-six positions containing "zeros." The current provided to the Digit winding is sufficient to cancel the total effect of the current provided to the Y and X Drive lines since

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is provided to each of the X and Y Drive lines (which is the current required to switch the core) and the current provided to the Digit Plane winding is sufficient to overcome at least a portion of this current thereby prohibiting the switching of the core from the "zero" to the "one" state on Writing operation. When a word is to be written into Core Storage in response to a Store instruction, the operation proceeds almost as previously described with respect to a Read instruction. However, before a Write pulse can be generated from the Switch Cores, the Switch Cores associated with the selected address must be placed in a Write status and this can be done by causing the proper Switch Cores to first provide a Read current. Therefore, for a Write cycle the Core Plane Address to be written first receives a Read pulse which causes the contents at the Address specified to be all "zeroes" in all 36 positions. Output signals will be present on those Sense Windings having a core change from the "one" to the "zero" state but these are suppressed at the output of the Sense Amplifier since the Read-Out Sample line **130***a*.**07** is down. At this time the selected Switching Cores of the X Matrix Switch and the Y Matrix Switch have been switched from the "zero" to the "one" for providing outputs to the Selected vertical line of cores causing them to change from a "one" to a "zero." Information is present on the lines **142***a*.**02**, **142***b*.**02** and **142***c*.**02** from the Storage Bus or in the alternate is present on the DSU Storage Bus **142***a*.**06**, **142***b*.**05**, **142***b*.**04**. When the Read-In Sample signal is provided on the line **130***a*.**05** together with the Write Control signal on **164.02** the trigger is turned on for those positions having "ones" present at the inputs (that is, having the input lines up).

After the Buffer trigger has been set, the Write current is sent to all thirty-six cores of the Address to be written which causes all "ones" to attempt to read into that Address. Where "zero" is to be written into a particular core the writing of a "one" is suppressed by the Storage Buffer Trigger Off line **142***a*.**01**, **142***b*.**01** or **142***c*.**01** in the manner previously described. The Buffer Register triggers are reset by way of the lines **130***b*.**01**, Reset Storage Address Register and Buffer Register between **0.5** and **1.0** time.

Component Circuits

A detailed description of the principles of operation of a Magnetic Core Storage device may be had in U.S. patent application, Serial Number 592,545, filed July 6, 1956, and referred to previously. A detailed description of a Central Processing Unit of the parallel binary type is described in Computer for **701**, copending application Serial No. 419,642, Philip E. Fox, filed March 30, 1954, and includes basic instructions and typical circuits for causing their performance. Especially applicable are FIGURES 1*b*, 1*d*, 1*f* and 1*g*, which correspond generally to devices employed in the present invention. Other operations, particularly those utilizing Input-Output units such as magnetic tapes are disclosed in the copending application, Serial No. 401,648, Bartelt et al., filed December 31, 1953, and in the copending application, Serial No. 401,502, of Bartelt et al., filed December 31, 1953. Further description may be had with reference to similar arithmetic elements in "IBM" Type 701 Computer, by H. D. Ross, Proceedings of the I.R.E., vol. 41, pages 1287–1294, October 1953.

The Storage Register, Accumulator Register, and Multiplier Quotient Register are composed of microsecond delay units which are storage units having the particular capacity of being able to accept information and transmit information at the same time. These units are described in detail in U.S. Patent Re. 23,699. The Adder and True Complement controls comprise thirty-five full Adders and two half Adders of the type explained in detail with reference to FIGURES 7*b* and 7*c* of application, Serial Number 419,642 referred to previously. The

True complement controls are those circuits that control the input to the Adders and consist of switching circuits and inverters. The switches control the time of entry of a word into the Adder and also determine whether the digits pass through the Inverter or not. Thus, a word entered into the Adders may be either true or complement. The Indicator register is composed of triggers of the bistable multivibrator type which remain in one or the other of two stable states until forced by external signals to assume the other state. The trigger is said to be "On" when its left side is conducting, and therefore its left side is called the "On Side" and the right side is the "Off Side." In this instance, a trigger is said to be storing a "1" when On and a "0" when "Off." In this embodiment of the invention, circuits are arranged to operate at voltage levels at a −30 volts and a +10 volts. When a line is referred to as being in the "Down" condition, it is to be assumed that the line is at a −30 volts, and conversely when a line is said to be in the "Up" condition it is to be assumed that he line is at a +10 volts potential.

Circuits employed in the practice of this invention have been designed to function in a one microsecond period which has been the usual period employed in similar machines by the assignee of this application since the Type 701 Computer was introduced. Computer type circuits are used throughout the patent applications to which reference is made and a detailed explanation of the circuits themselves and of the modifications thereof are not considered necessary because of the present state of the art. Throughout the description of operation no reference is made to passive elements such as to cathode followers, level setters and the like. It is obvious that the characteristics of these elements vary and are largely determined not only by the component load but also by the length of conductors coupling one circuit to another.

Indirect Addressing

To illustrate the invention by example, a Clear and Add Indirect Addressing Instruction is used as shown in FIGURE 4. The Clear and Add (CLA+**0500**) instruction is a type B instruction illustrated in FIGURE 3*b* and has an operations part in positions S through **11** with "zeros" in positions **1** and **2**, a tag in positions **18**, **19** and **20**, binary "ones" in positions **12** and **13** to indicate indirect addressing and an address to which reference is made in Storage in positions **21** through **35**. The CLA instruction is brought from the Storage Busses to the Storage Register by the Minus to Suppress Storage Bus to Storage Register line (always up in this instance of application) and the I7 (D1) line in FIGURE 53*a*. Storage Register positions **3** through **11** are placed in positions **1** through **9** of the Primary Operations part of the Instruction Register, FIGURE 13*a*, by the lines **99.05** and **99.06**. In FIGURE 13*a*, Instruction Register **1** lines **13***a*.**05** through **13***a*.**08** are up, Minus on Instruction Register **2** lines **13***a*.**09** through **13***a*.**12**, Instruction Registers **3** lines **13***a*.**19** through **13***a*.**21** are up, Minus on Instruction Register line **13***a*.**22** is up, Minus on Instruction Register **5** line **13***a*.**25** is up. In FIGURE 3*b*, Minus on Instruction Register **6** lines **13***b*.**01** through **13***b*.**13** are up, and Minus on Instruction Register **7** lines **13***b*.**25** through **13***b*.**37** are up. In FIGURE 13*c*, Minus on Instruction Register **8** lines **13***c*.**01** through **13***c*.**19** are up and Minus on Instruction Register **9** lines **13***c*.**37** through **13***c*.**53** are up. Thus, in the Primary Operation Decoders, FIGURE 14*b*, the lines **1**, $\bar{2}$, $\bar{3}$, $\bar{4}$, and $\bar{5}$ are up providing an output (**5**, **0**) indicative of the tens and hundreds positions of the operation code. Accordingly, in FIGURE 14*d* outputs are provided on lines **14***d*.**16** through **14***d*.**22**. In FIGURE 100, the trigger is "Off" and the lines **100.01** through **100.41** are up indicating Instruction Register Sign Plus.

In FIGURE 90*a*, Indexing Controls, the lines Storage Register **1** and **2** are down since the instruction contain zeros in these two positions. Storage Register **8** and **9** lines are down as well, so the output of the inverter is up. Therefore, from I9 until CT1 the Indexable Instruction lines **90***a*.**01** through **90***a*.**03** are up to Carry One to Adders **17**, FIGURE 89*b*, Index Register Entry Control, FIGURE 89*a*, and Indirect Addressing Control, FIGURE 98. When the Indirect Addressing Control Trigger comes "On" at **I10**, it holds up the Indexable Instruction line for so long as the Indirect Addressing Control Trigger is "On" even though the status of the Storage Register lines **1**, **2**, and **8** and **9** may change. The line **90***a*.**03** goes to Indirect Addressing Controls, FIGURE 98, where it is combined with Storage Register **12** line, Storage Register **13** line (bits in **12** and **13** identify an indirect addressing word), and Minus on Floating Point Trap or Interrupt to bring up the outputs of the AND circuit. Instruction Register **1** line **13***a*.**08**, and Minus on Instruction Register **2** line **13***a*.**10** are up and at **A10** (D2) the line **122***k*.**07** turns "On" the Indirect Addressing Trigger. The Indexable Instruction line **90***a*.**03**, Storage Register **12** and **13** line **5***b*.**05**, Minus on Floating Point Trap or Interrupt line **22.01**, Instruction Register **1** line **13***a*.**08**, and Minus on Instruction Register **2** line **13***a*.**10** combine to provide an output Go to E Time (IA Instruction Store and Trap) line **98.01** and the line **98.02**, Minus on Go to E Time, goes down. The line **98.01** Go to E Time goes to Cycle Timer Control, FIGURE 118, where it brings up the Go to Execute Time Control lines **118.01** and **118.02**. The line **98.18** goes to Indexing Operation in Storage Register **18** through **35** to Adders P through **17**, FIGURE 86*a*, to bring up the lines **86***a*.**01** through **86***a*.**12**. The line **98.17** goes to Address Switch Input Controls, FIGURE 110, to provide an output on the Adder to Address Switch Control line **110.04** to gate the address into the Storage Address Register, FIGURE 129. In Index Register to Adder Controls, FIGURE 87*a*, the Indexable Instruction line **98.02** is up to bring up the lines **87***a*.**01** through **87***a*.**09** which go to the Adder positions **3** through **17** to gate the output to the Index Register Mixing, FIGURE 52.

Index Register A has an octal address of 1 which appears in positions **18**, **19**, and **20** as 001. Index Register B has an octal address of 2 and a bit configuration in positions **18** through **20** of 010. Index Register C has an octal address of 4 and a bit configuration in positions **18** through **20** of 100. Assume in this instance that Index Register A is addressed, then there will be "zeros" in Storage Register positions **18** and **19** and a "1" in Storage Register position **20**. Accordingly, in Index Register to Adders Gating, FIGURE 51, the line Minus on Master Stop Trigger "On" is always up for the purposes of illustration of this invention. The Storage Register **20** line is up to provide an output on the Index Register A to Adders lines **51.01** and **51.02**. The Index Register A column N output lines **9.01.03** through **9.01.07** are gated through to bring down the complement index column N output lines **52.01** through **52.09**. The line **98.20** goes to Cycle Timer Control, FIGURE 118, to take a second Execute cycle.

It is pointed out that in the CLA instruction the operation is decoded at I9 since Clear and Add does not interfere with the Indirect Addressing operation. However, if the Indirect Addressing and Control Trigger Off line **98.14** is down decoding via the Primary Operation Decoder, FIGURES 14*a* and *b*, is prevented in the cases of codes (5, 4), (3, 2), (4, 8), (4, 4), (6, 2), (6, 0) and (6, 4) because in these instances the decoding of the tens and hundreds position the operation code would cause operations which are not compatible with the Indirect Addressing operation. Accordingly, in the Timing Chart it is shown in the example given so far, the operation is decoded in FIGURE 14 as usual, but in other of the instructions to which the foregoing operation code may apply the decoding operation is prevented from being decoded until the Indirect Address Control trigger is

turned "Off" at which time the operation is decoded as E1 time as shown in the Timing Chart.

During the Execute cycle following the Instruction cycle, the word brought from the location in Storage specified by the Address portion of the CLA Instruction is modified by the Indexing Operation if the Instruction so directs. This word may or may not provide reference to another location in Storage which specifies the location from which data are to be taken by having "ones" in positions **12** and **13** of the word.

Assume for the moment that the word taken from Storage during the first Execute cycle is not of the Indirect Addressing type. If this is so, then this word is operated upon during the second E cycle in the manner prescribed by the operations part of the CLA Instruction. With reference to the Timing Chart of FIGURE 4 and more particularly to Indirect Addressing Controls of FIGURE **98**, the Cycle Timer Control Trigger Off line **120.06** comes up at CT1 when the Carry Timer goes down. The line E9 until CT1 **122***j***.19** is up 1 microsecond after the Cycle Timer Trigger is turned "Off," and at **A1** (D1) a pulse comes in on line **122***b***.03** to turn "Off" the Indirect Addressing trigger. In FIGURE 4, the Operation decoded in the Timing diagram has a data portion which indicates that the operation is decoded during the I cycle, the first Execute cycle, and the last Execute cycle for the CLA Instruction. However, for those instructions previously mentioned that would interfere with Indirect Addressing operation the operation is decoded from E1 through the second E cycle to perform the operations upon the data word brought from Storage. In FIGURE 128*a*, End Operation Control, the Primary Operation (**5, 0**) line is up, E time is up, and IA Control Trigger Off line gives an output End Operation Control on the line **128***a***.01** which goes to the Cycle Timer Control, FIGURE 118, where at **A10** (D2) the End Operation Trigger is turned "On" to bring up the output lines **118.06** through **118.13**.

Assuming that the word taken from Storage during the first Execute cycle is in the Indirect Addressing format having a "1" in position **12** and a "1" in position **13**, then the Storage Register **12** line **15***b***.05.12** and the Storage Register **13** line **15***b***.05.13** shall be up in FIGURE 98 and the Indirect Addressing trigger may stay on for so long as there is a "1" in Storage Register position **12**, and a "1" in position **13**. Since both SR**12** and **13** lines are up, the output of AND circuit **98.34** is up, but the output of the inverter **98.36** is down which prevents the Minus on E9 or ER9 until CT1 line from bringing up the output of the AND circuit **98.38** when the E and ER cycle trigger of FIGURE 122*j* is "Off." The trigger may be turned "Off" by the Cycle Timer Control Trigger "Off" line **120.06**, E9 until CT2 line, and the **A1** (D1) line **122***b***.03**. However, the Cycle Timer Control trigger is held "On" by repeated execution cycles and the Indirect Addressing Control trigger remains "On." Assuming that the word brought from Storage during the first Execute cycle has a "1" in Storage Address Register position **12** and a "1" in Storage Address Register position **13**, then the lines **15***b***.05.12** and **15***b***.05.13** are up. Accordingly the output of the AND circuit **98.34** is up, the output of the Inverter **98.36** is down so the Minus on E9 or ER9 until CT1 cannot provide an output of the AND circuit **98.38**. However, once a word is brought in from storage in which positions **12** and **13** are not both "ones" then the output of the AND circuit **98.34** is down, the output of the Inverter **98.36** is up, and when Minus on E9 or ER9 until CT1 comes up a positive output is provided from the AND circuit. This output is inverted and the negative shift cuts off the Indirect Addressing Control trigger. Therefore, the circuit just described permits N order Indirect Addressing Operations to be performed under control of Indicator bits **12** and **13** in the Indirectly Addressing word. N+1 order Indexing Operations follow and are controlled by the tag field indicators in the Indirectly Addressing word. Simply stated, the Indirect Addressing Control trigger of FIGURE 98 may be held on for repeated Execute cycles during which cycles, words are taken from Storage, each of which has an address which may be modified by the Index Registers to provide an address in Storage from which the next word may be taken.

Definitions of Symbols

$A^{I\,MEG}$, A_C, A, AND are AND circuits; A_S is a Slow Amplifier; —AND and —A are OR circuits; A_D is a Drum Amplifier; A_{CS} is a Sense Amplifier; and ATA is a Read Preamplifier.

CF is a cathode follower; CF (infinite), CF^R_{OR}, CF_{OR} (infinite), CF_{OR} are cathode follower OR circuits; CF_T is a tapped cathode follower; CF_{ER} is a cathode follower used for the electronic reset of triggers; CF_M, $CF_{OR}(R)$ are cathode follower OR circuits having the cathode clamped so as not to go below ground; CF_T is a cathode follower with tapped load for reduced output; CG_M is a Clamp Generator; and CPA is a Clamp Power Amplifier.

D is a Microsecond Delay Unit; DG is a Diode Gate; DL is a Delay Line, DPQ is a Digit Plane Amplifier; DPD is a Digit Plane Driver; and DL_B is Delay Line. GA and GAF are Grounded Grid Amplifiers.

K and K_{PP} are Cathode Followers; K_{RA} and KR_A are Reset Cathode Followers; K_O is a Power Cathode Follower OR; K_C is Power Cathode Follower with very small load resistor suitable for low duty cycle use; K_O is cathode follower OR; K_j is a Power Cathode Follower; and K_{JO} is a Power Cathode Follower OR.

MV is a Multivibrator; MSAW is a Matrix Switch Amplifier, Write; MSAR is a Matrix Switch Amplifier, Read; and MSD is a Matrix Switch Driver.

O, $O_{I\,meg}$ and OR are OR circuits; O_C is a Cascaded OR circuit; —OR is an AND; and OSC is a Master Oscillator. R is a Relay Driver (essentially an inverter with a relay coil as a plate load).

SS_F is a Single Shot (fast recovery); ST is a Switch Timer; SS_E is a Single Shot (fast recovery); SS_H is a Single Shot (holdover); SS_D is a Single Shot (short duration); SR is a Switch Read; SG is a Sync Generator; SC is a Sync Clipper; and SPA is a Sync Power Amplifier. T is a High Speed Trigger; T_{WR} is a Write Trigger; T_{KX} is a Key Trigger with reset (X denotes reset); T_K is a Key Trigger; T_T, T_U, T_V, T_W, T_y, T_{XA} and T_{XB} are Triggers where the subscripts denote different resets; TH is a Thyratron; T_A is a Trigger with particular output dividers; T_S is a Slow Trigger; T_{AXA}, T_{AXB}, T_{AZ}, T_{AW}, T_W, and T_C are Slow Triggers having various output dividers; T_{KA} is a Key Trigger and T_B is a Schmitt Trigger.

WD is a Write Driver, ${}_xT_{KA}$ and ${}_xT$ are Key Triggers reset off; ${}_xT_D$ is a Key Trigger with a large crossover capacitance; and $_{XTAL}$ is a crystal.

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to a preferred embodiment, it will be understood that various omissions and substitutions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art without departing from the spirit of the invention. It is the intention therefore, to be limited only as indicated by the following claims.

What is claimed is:

1. In an electronic data processing machine for executing an indirect addressing operation in response to the contents of a location allotted to a tag portion in manifestations representative of an instruction word which also includes operation and address portions, apparatus comprising in combination; an addressable storage device including read-in means for storing a program of manifestations representative of data words and instruction words at selectable addresses therein, and read-out means for reading out said manifestations representative of instruction and data words therefrom; control means oper-

ative to treat said read out manifestations as representative of a selected one of said instruction and data words; means for interpreting instruction manifestations received from said storage device; an instruction counter; means normally operable for stepping said counter; means controlled by said counter for normally controlling said read-out means for sequentially selecting said numbered addresses and read out manifestations from said storage device; means for initially causing said control means to treat said manifestations as an instruction word; means for transferring the contents of the tag location and the operations portion of said instruction word to said means for interpreting instruction manifestations, and the address portion in said instruction word to said read-out means; means for initiating another read-out from storage at the location specified by aforesaid address portion of information treatable by said control means as another address portion when said tag is present and treatable as data manifestations when said tag is absent.

2. In an electronic data processing machine including means effective to execute an indirect addressing operation in response to a particular portion of instruction word manifestations which includes a first address portion, a tag and an operation portion, apparatus comprising in combination; an addressable storage device storing data manifestations and a program of instruction manifestations at selectable addresses therein and read-out means for reading out instruction manifestations and data manifestations, an instruction register, an instruction counter, means for normally advancing said counter, means controlled by said counter for normally selecting addresses in said storage device, means for controlling said read-out means for transferring manifestations of an indirect addressing instruction including a first address portion and a tag and operations portion from said storage device to said instruction register, means responsive to said first address portion in said instruction register for causing said read-out means to read out another address portion from the location specified by said first address portion of said indirect addressing instruction, and means to control said read-out means to obtain data manifestations from the location specified by said other address portion to be operated upon in accordance with said tag and operations portions of said indirect addressing instruction manifestations.

3. A claim, in accordance with claim 2, wherein means are included for modifying said first address portion of said indirect addressing instruction word manifestations by a predetermined amount so that said other address portion is obtained from a different location in said storage device.

4. In a data processing system, adapted for operation with manifestations representative of instruction words, each containing an address portion and an operation portion including a tag, and including: a storage device, for storing said instruction word manifestations and a plurality of manifestations representative of words in addressable locations and adapted to read in and read out said instruction manifestations and data word manifestations in response to read-in and read-out signals, and a data processing unit having an arithmetic section for processing data manifestations and an interpretation section for controlling the execution of the given operation in response to interpretation of said operation portion, and addressing means for providing read-in and read-out signals to said storage device in response to said address portions, means for entering the operation portion and the address portion of instruction word manifestations, read out of said storage device, into said interpretation section and addressing means, respectively, means controlling said addressing means for providing read-out signals to said storage device to read out manifestations representative of a selected one of said instructions, means controlled by said interpretation section, in accordance with said tag, for controlling said addressing means to provide read-out signals to read out a first word, including another address manifestation portion, from the location in said storage specified by said address portion of said instruction manifestations, said means controlled by said interpretation section, subsequently providing read-out signals to said storage device to read out manifestations, now specified by said other address manifestation portion of said first word manifestations in said addressing means, and means operable in response to said interpretation section for controlling operation in accordance with said operation portion, upon said second word in said arithmetic section.

5. A claim, in accordance with claim 4, wherein additional means are provided for storing a modifying address portion and for selectively applying said modifying address portion to said address portion of said instruction word manifestations, in response to said operation portion of said instruction word manifestations.

6. A data processing system adapted for operating with manifestations representative of instruction words containing address portions and operation portions and a tag, comprising, in combination; a storage device for sorting information including instruction words and data manifestations, an instruction register, means for storing instruction word manifestations and data manifestations in said storage device at selectable addresses, addressing means controlled by said instruction register to control the read out of information from said storage device, arithmetic means, means for extracting manifestations representative of a particular instruction word from said storage device and placing said operation part and tag, of said instruction word manifestations, in said instruction register, and said address part, in said addressing means, means controlled by said tag effective to control a read out of another address portion from said storage device into said addressing means according to the address portion of said particular instruction word manifestations, and means controlling read out from said storage device into said arithmetic means of data manifestations at the location specified by said other address portion, said instruction register controlling said arithmetic means in response to said operation manifestation of said particular instruction word manifestations.

7. In an electronic data processing machine adapted for operation with manifestations representative of instruction words having operation, tag and address portions, apparatus comprising, in combination; an addressable storage device storing data manifestations and a variety of instruction word manifestations at selectable addresses therein and having read-in and read-out means for reading in and reading out selected instruction word manifestations and data manifestations, arithmetic means, including an instruction register settable to address, tag and operation portions of said instruction word manifestations for controlling said read-in and read-out means and said arithmetic means, means controlling said read-out means for extracting instruction word manifestations having a tag, specifying an indirect addressing operation, from said storage device and placing the same in said instruction register, means effective in response to the tag and operation portions in said instruction register, for controlling said read-out means to extract an address portion from said storage device at the location specified by the address portion of said indirect addressing instruction manifestations, and means responsive to said extracted address portion for controlling said read-out means for reading data manifestations into said arithmetic apparatus from said storage device.

8. In a machine, for processing data manifestations, controlled by manifestations representative of instructions each comprising an operations portion, an address portion and a control portion; memory means having addressable locations for storing as states, manifestations representative of data and instructions; program means for sequentially selecting instruction manifestations; routing means for controlling the execution in turn of said

selected instruction manifestations; computation means for performing operations indicated by the operation portions of said selected instruction manifestations, upon manifestations at locations in the memory means, initially indicated by the address portions of said selected instructions manifestations; first control means associated with said routine means for sensing the control portion of said instruction manifestations and indicating either one of two conditions, second control means associated with said routing means and operative, when a first, of said two conditions, is sensed by said first control means to cause said computation means to perform data operations upon said initially indicated manifestations, third control means associated with said routing means and operative, when a second, of said two conditions, is sensed by said first control means to prevent said computation means from performing data operations upon said initially indicated manifestations, and fourth control means associated with said routing means and operative, when said second condition is sensed, for causing said manifestations at locations in the memory means initially indicated by said address portions to be treated as a second address, said computation means thereafter performing operations indicated by the operation portion of said selected instruction manifestation upon data manifestations, at said second address locations in the memory.

9. In a data processing machine; means for sequencing the machine through a program of operations, each operation being specified by manifestations representative of an instruction comprising an operation part, an address part and a tag; means for sensing the absence or presence of the tag; first means for causing processing of data manifestations at a location indicated by the address part in accordance with the operations part, when said sensing means indicate absence of the tag; and second means for causing processing in accordance with the operations part, of data manifestations, at another address, found at a location indicated by the address part when said sensing means indicate the presence of the tag.

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UNITED STATES PATENT OFFICE

Certificate

Patent No. 3,036,773 Patented May 29, 1962

Joseph L. Brown

Application having been made jointly by Joseph L. Brown, the inventor named in the patent above identified; International Business Machines Corporation, New York, New York, a corporation of New York, the assignee; John E. Griffith, Tatomuck Road, Pound Ridge, New York; and Elaine M. Boehm, Middlebush Road, Wappingers, New York, for the issuance of a certificate under the provisions of Title 35, Section 256 of the United States Code, adding the names of the said John E. Griffith and the said Elaine M. Boehm to the patent as joint inventors, and a showing and proof of facts satisfying the requirements of the said section having been submitted, it is this 11th day of December 1962, certified that the names of the said John E. Griffith and the said Elaine M. Boehm are hereby added to the said patent as joint inventors with the said Joseph L. Brown.

[SEAL]

EDWIN L. REYNOLDS,
First Assistant Commissioner of Patents.

UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,036,773

May 29, 1962

Joseph L. Brown

It is hereby certified that error appears in the above numbered patent requiring correction and that the said Letters Patent should read as corrected below.

Column 1, line 12, for "ton" read -- to --; column 2, line 17, for "indirected" read -- indirect --; column 4, line 34, after "(2 sheets" insert a closing parenthesis; line 42, strike out "to"; column 5, line 46, for "Add AND" read -- Add/AND --; column 6, line 22, for "Plus" read -- Pulse --; line 28, for "throufh" read -- through --; line 34, for "counters" read -- counter --; column 7, line 25, for "is" read -- as --; column 8, line 24, for "Regiser" read -- Register --; line 36, for "in" read -- an --; column 11, line 72, for "7c.03-34" read -- 7c.03.30-34 --; column 13, line 9, after "Unit" insert a closing quotation mark; column 15, line 15, for "enteds" read -- enters --; line 26, for "operation" read -- operational --; column 19, line 20, for "FIGURE" read -- FIGURES --; line 31, after "of", first occurrence, insert -- the --; column 24, line 74, for "Position" read -- Positions --; column 26, line 69, for "ods" read -- ode --; column 29, line 68, after "of" insert -- the --; column 30, line 30, for "on", second occurrence read -- ON --; column 31, line 20, for "he" read -- the --; line 58, for "Registers" read -- Register --; column 32, line 1, quotations marks should be inserted around the word "zeros"; column 33, line 44, for "on" read -- ON --; column 36, line 23, for "sorting" read -- storing --.

Signed and sealed this 24th day of September 1963.

(SEAL)
Attest:

ERNEST W. SWIDER
Attesting Officer

DAVID L. LADD
Commissioner of Patents