

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
4 June 2009 (04.06.2009)

PCT

(10) International Publication Number
WO 2009/069366 A1

(51) International Patent Classification:
H04N 5/213 (2006.01)

(21) International Application Number:
PCT/JP2008/066801

(22) International Filing Date:
10 September 2008 (10.09.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2007-311651 30 November 2007 (30.11.2007) JP

(71) Applicant (for all designated States except US):
KABUSHIKI KAISHA TOSHIBA [JP/JP]; 1-1, Shibaura
1-chome, Minato-ku, Tokyo 1058001 (JP).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **HONDA, Yuichi**
[JP/JP].

(74) Agents: **SUZUYE, Takehiko** et al.; c/o **SUZUYE**
& **SUZUYE**, 1-12-9, Toranomon, Minato-ku, Tokyo
1050001 (JP).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

(54) Title: NOISE REDUCING CIRCUIT, NOISE REDUCING METHOD, AND VIDEO APPARATUS

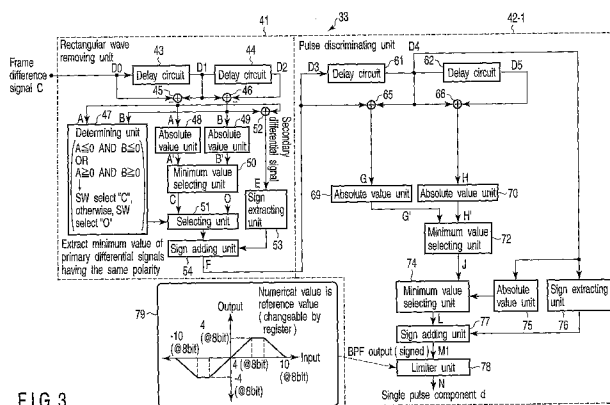


FIG. 3

(57) Abstract: A noise reducing circuit includes a frame memory configured to frame-delay a video signal, a first arithmetic unit configured to subtract the frame-delayed video signal given by the frame memory from the video signal to output a first frame difference signal, a first rectangular wave removing unit configured to remove a rectangular wave component from the first frame difference signal to generate a second frame difference signal, a first pulse discriminating unit configured to receive the second frame difference signal, remove a continuous pulse component from the second frame difference signal, and output a single pulse component, and a second arithmetic unit configured to subtract the single pulse component from the video signal.

D E S C R I P T I O N

NOISE REDUCING CIRCUIT, NOISE
REDUCING METHOD, AND VIDEO APPARATUS

5

Technical Field

The present invention relates to a noise reducing circuit, a noise reducing method, and a video apparatus which remove a rectangular wave component and a continuous pulse component from a noise component to output a single pulse component.

10

Background Art

In recent years, in an impulse noise removing apparatus, a large number of schemes which reduce impulse noise error detection in a moving image are known.

15

Patent Document 1 discloses a technique which can determine the presence/absence of a single impulse noise component having a large change in luminance and included in a video signal.

20

[Patent Document 1] Jpn. Pat. Appln. KOKAI
Publication No. 5-145802

However, in the conventional technique of Patent Document 1, a continuous pulse noise or a single impulse noise mixed in a rectangular wave cannot be always correctly separated and detected.

25

Disclosure of Invention

The present invention has as its object to provide

a noise reducing circuit, a noise reducing method, and a video apparatus which remove a rectangular wave from a noise signal to reliably detect and remove a single pulse.

5 An embodiment to solve the problem is a noise reducing circuit including: a frame memory (31) configured to frame-delay a video signal (a); a first arithmetic unit (32) configured to subtract the frame-delayed video signal (b) given by the frame memory from
10 the video signal to output a first frame difference signal (c); a first rectangular wave removing unit (33: 41) configured to remove a rectangular wave component from the first frame difference signal (c) to generate a second frame difference signal (D3); a first pulse
15 discriminating unit (33: 42) configured to receive the second frame difference signal, remove a continuous pulse component from the second frame difference signal, and output a single pulse component (d); and a
20 second arithmetic unit (36) configured to subtract the single pulse component (d) from the video signal (a).

Brief Description of Drawings

FIG. 1 is a block diagram showing an example of a configuration of a noise reducing circuit according to an embodiment of the present invention.

25 FIG. 2 is a timing chart showing an example of an operation of the noise reducing circuit according to an embodiment of the present invention.

FIG. 3 is a block diagram showing an example of a configuration of a single pulse detecting unit which is a main configuration of the noise reducing circuit according to an embodiment of the present invention.

5 FIG. 4 is a timing chart showing an example of an operation of a single pulse detecting unit which is a main configuration of a noise reducing circuit according to an embodiment of the present invention.

10 FIG. 5 is a flow chart showing an example of a rectangular wave removing process of a single pulse detecting unit which is a main configuration of a noise reducing circuit according to an embodiment of the present invention.

15 FIG. 6 is a flow chart showing an example of a separating process of continuous pulse signals and a single pulse signal of a single pulse detecting unit which is a main configuration of a noise reducing circuit according to an embodiment of the present invention.

20 FIG. 7 is a graph showing an example of input/output characteristics of a single pulse detecting unit which is a main configuration of the noise reducing circuit according to an embodiment of the present invention.

25 FIG. 8 is a block diagram showing an example of a configuration of a single pulse detecting unit which is a main configuration of a noise reducing circuit

according to an embodiment of the present invention.

FIG. 9 is a timing chart showing an example of an operation of a single pulse detecting unit which is a main configuration of a noise reducing circuit

5 according to an embodiment of the present invention.

FIG. 10 is a flow chart showing an example of a detecting process for continuous pulse signals and a single pulse signal in a single pulse detecting unit which is a main configuration of a noise reducing circuit according to an embodiment of the present invention.

FIG. 11 is a block diagram showing an example of a configuration of a single pulse detecting unit which is a main configuration of a noise reducing circuit according to an embodiment of the present invention.

FIG. 12 is a flow chart showing an example given when an operation of a single pulse detecting unit which is a main configuration of a noise reducing circuit according to an embodiment of the present invention is realized by a computer program.

FIG. 13 is a block diagram showing an example of another configuration of a noise reducing circuit according to an embodiment of the present invention.

FIG. 14 is a timing chart showing an example of an operation of a noise reducing circuit according to an embodiment of the present invention.

FIG. 15 is a block diagram showing an example of a

configuration of a video apparatus to which a noise reducing circuit according to an embodiment of the present invention is applied.

Best Mode for Carrying Out the Invention

5 Embodiments of the present invention will be described below in detail with reference to the accompanying drawings.

FIG. 1 is a block diagram showing an example of a configuration of a noise reducing circuit according to an embodiment of the present invention. FIG. 2 is a
10 timing chart showing an example of an operation of a noise reducing circuit according to an embodiment of the present invention. A configuration and an operation of a noise reducing circuit 21 will be
15 described with reference to FIGS. 1 and 2.

The noise reducing circuit 21 includes a frame memory 31, an arithmetic unit 32, a first single pulse detecting unit 33, a second single pulse detecting unit 34, an arithmetic unit 35, and an arithmetic unit 36.

20 The frame memory 31 stores a video signal of 1 frame and outputs a video signal before 1 frame (frame delay signal) b. The arithmetic unit 32 calculates a frame difference signal c between a video signal a and the video signal b. The first single pulse detecting
25 unit 33 extracts a single pulse included in the frame difference signal c as a single pulse component d.

The second single pulse detecting unit 34 detects

a size of a single pulse included in the video signal a, and generates an output f expressing, for example, a 0 to 1 time coefficient depending on an amplitude of the detected pulse. The arithmetic unit 35 multiplies an amplitude of a pulse of the single pulse component output d by the coefficient determined by the output f to generate a single pulse component d' obtained by changing the amplitude of the pulse of the single pulse component d. The arithmetic unit 36 outputs an output signal e obtained by subtracting the single pulse component d' from the video signal a.

In the video signal a shown in FIG. 2, pulse signals v2, v3, and v4 are superposed on a rectangular signal v1, and a rectangular signal v5 is present. The pulse signal mentioned here is turned on or off in units of pixels, and the rectangular signal is a signal in which a plurality of continuous pixels are turned on.

In the video signal a, the rectangular signals v1 and v5 are signals expressing a video but noise. The single pulse signal v2 in which only one pixel is turned on is noise, and a signal to be processed by the noise reducing circuit 21. The continuous pulse signals v3 and v4 in which a plurality of pixels are repeatedly turned on or off may be noise or video signals.

In a noise reducing circuit according to the

embodiment described below has a β mode in which only a single pulse is detected and an α mode in which a single pulse and continuous pulses are detected.

[First Embodiment]

5 The first single pulse detecting unit 33 which is a main part of a noise reducing circuit according to an embodiment of the present invention will be described below in detail with reference to drawings.

10 FIG. 3 is a circuit diagram showing a configuration of the first single pulse detecting unit 33. The first single pulse detecting unit 33 shown in FIG. 3 is a β mode configuration which detects a single pulse signal. FIG. 4 is a timing chart showing an example of an operation of the first single pulse
15 detecting unit 33.

 The first single pulse detecting unit 33 includes a rectangular wave removing unit 41 and a pulse discriminating unit 42-1. The rectangular wave removing unit 41 removes a rectangular wave signal from
20 the frame difference signal c. The pulse discriminating unit 42-1 discriminates continuous pulses and a single pulse from an output signal from the rectangular wave removing unit 41 to extract only the single pulse.

25 [Rectangular Wave Removing Unit]

 An operation of the rectangular wave removing unit 41 will be described below with reference to FIGS. 3

and 4.

In the rectangular wave removing unit 41, a frame difference signal c (D0) is supplied to a delay circuit 43. The delay circuit 43 outputs a delay signal D1.

5 The delay signal D1 is supplied to a delay circuit 44. In the delay circuit 44, a further delayed delay signal D2 is output.

The delay circuit 43 and 44 mentioned here are memories operating in units of pixels. Therefore, the
10 delay signal D1 is a signal delayed by one pixel with respect to the frame difference signal c. The delay signal D2 is a signal delayed by 2 pixels with respect to the frame difference signal c.

It must be noticed that the delay circuit 43 and
15 44 may be memories operating in several units of pixels. Therefore, the delay signal D1 may be a signal delayed by a first pixel number with respect to the frame difference signal c. The delay signal D2 may be a signal delayed by a second pixel number with respect
20 to the frame difference signal c.

An adder 45 subtracts the frame difference signal c from the delay signal D1 to generate an output A. An adder 46 subtracts the delay signal D2 from the delay signal D1 to generate an output B.

25 The output A and the output B are difference signals between two signals with reference to the delay signal D1. However, in this specification, the

difference signals are called differential signals.
More specifically, the differential signals are
difference signals between the two signals. A
secondary differential signal is a difference signal of
5 two differential signal.

In this case, it must be noticed that the
difference is calculated with reference to the delay
signal D1 by the output A and the output B. Because
this will allow the determination of polarities of the
10 output A and the output B.

The output A is input to an absolute value unit
48. The absolute value unit 48 generates an absolute
value signal A' obtained by converting a negative
signal of the output A into a positive signal. The
15 output B is input to an absolute value unit 49. The
absolute value unit 49 generates an absolute value
signal B' obtained by converting a negative signal of
the output B into a positive signal. A minimum value
selecting unit 50 selects a smaller one of the absolute
20 value signal A' and the absolute value signal B' to
output the signal as a signal C.

On the other hand, the output A and the output B
are input to a determining unit 47. In this case, the
determining unit 47 examines the polarities of the
25 signals. The determining unit 47 outputs a signal
representing whether the polarities of the output A and
the output B are equal to or different from each other

to a selecting unit 51. More specifically, when the signals A and B satisfy $A \leq 0$ and $B \leq 0$, or when $A \geq 0$ and $B \geq 0$ are determined, the determining unit 47 outputs a signal representing that the polarities of both the signals are equal to each other to the selecting unit 51. When the signals A and B satisfy $A \leq 0$ and $B > 0$, or when $A \geq 0$ and $B < 0$ are determined, the determining unit 47 outputs a signal representing that the polarities of both the signals are different from each other to the selecting unit 51.

When the signal from the determining unit 47 represents "polarities are equal to each other", the selecting unit 51 selects an output C from the minimum value selecting unit 50. The selecting unit 51 selects a signal having a value = 0 when the signal from the determining unit 47 represents that "polarities are different from each other". The selecting unit 51 outputs the selected signal to a sign adding unit 54.

With the operations of the determining unit 47 and the selecting unit 51, a rectangular wave signal corresponding to a rectangular signal V5 is removed. More specifically, parts corresponding to both the end parts of the rectangular wave signals present in the output A and the output B are not output because the parts have different polarities, and a signal having a value of 0 is output in place of the parts.

On the other hand, the output A and the output B

are added to each other in an adder 52. Since the operation corresponds to an operation of subtracting the inverted output B from the output A, it can be interpreted that the adder 52 generates a secondary differential signal E. The secondary differential signal E serving as an output from the adder 52 is supplied to a sign extracting unit 53 to extract sign information. For example, the sign is "+" when the secondary differential signal is positive, the sign is "-" when the secondary differential signal is negative. Extracted sign information is sent to the sign adding unit 54.

The sign adding unit 54 adds the extracted sign information to the output from the selecting unit 51. The signal selected by the selecting unit 51 is converted into an absolute value by the absolute value units 48 and 49. Therefore, the sign adding unit 54 adds a sign to convert the signal into a signal having an original sign. A signed output signal F (video signal D3) of the sign adding unit 54 is supplied to the pulse discriminating unit 42-1 serving as a latter part.

An outline of a general operation of the rectangular wave removal described above will be described below with reference to the flow chart. FIG. 5 is a flow chart showing an example of a rectangular wave removing process of a single pulse

detecting unit which is a main configuration of a noise reducing circuit according to an embodiment of the present invention.

5 In step S11, the rectangular wave removing unit 41 generates the first delay signal D1 obtained by delaying the frame difference signal c by a predetermined first pixel. The second delay signal D2 obtained by delaying the frame difference signal c by a second pixel is generated. In step S12, the
10 rectangular wave removing unit 41 outputs two differential values by using the frame difference signal c, the first delay signal D1, and the second delay signal D2. In step S13, the polarities of the two differential values are detected. In step S14, it
15 is determined whether the polarities of the two differential values are equal to each other.

When Yes in step S14, that is, when the polarities of both the differential values are equal to each other, the rectangular wave removing unit 41 determines
20 that the frame difference signal c given for the first time is not a rectangular wave in step S15 to shift to the latter part. When No in step S14, that is, when the polarities of both the differential values are different from each other, the rectangular wave
25 removing unit 41 determines that the frame difference signal c given for the first time is a rectangular wave in step S16 to remove a rectangular wave component.

In this manner, in the first single pulse detecting unit 33, removal of a rectangular wave which is a hindrance when a single pulse is detected is executed to make it possible to improve accuracy of detection of a single pulse in the latter part.

The steps in the flow chart in FIG. 5 can be replaced by circuit blocks, respectively. Therefore, all the steps in the flow chart can be redefined as blocks. More specifically, a general operation of the rectangular wave removing unit 41 of the first single pulse detecting unit 33 is not limited to the concrete embodiment of the rectangular wave removing unit 41 in FIG. 3. As the general operation, only the operation described above may be performed.

[Pulse Discriminating Unit]

An operation of the pulse discriminating unit 42-1 will be described below with reference to FIGS. 3 and 4.

The pulse discriminating unit 42-1 includes a delay circuit 61, a delay circuit 62, an adder 65, and an adder 66.

The delay circuit 61 generates a delay signal D4 obtained by delaying a signal F (to be referred to as a "video signal D3" hereinafter) output from the rectangular wave removing unit 41. The delay circuit 62 outputs a delay signal D5 obtained by delaying the delay signal D4 output from the delay circuit 61. The

adder 65 adds the video signal D3 and the delay signal D4 to each other to generate an output G. The adder 66 adds the delay signal D4 and the delay signal D5 to each other to generate an output H.

5 The output G is input to an absolute value unit 69. The absolute value unit 69 generates an absolute value signal G' obtained by converting a negative signal of the output G into a positive signal. The output H is input to an absolute value unit 70. The
10 absolute value unit 70 generates an absolute value signal H' obtained by converting a negative signal of the output H into a positive signal. The minimum value selecting unit 72 selects a smaller one of the absolute value signal G' and the absolute value signal H' to
15 output the selected signal as a signal J. As shown in FIG. 4, with the above processes, as the signal J, only the single pulse signal and the first and last pulse signals of the continuous pulse signals are extracted.

 On the other hand, the delay signal D4 output from
20 the delay circuit 61 is input to an absolute value unit 75 and a sign extracting unit 76. The absolute value unit 75 generates an absolute value signal D4' obtained by converting a negative signal of the delay signal D4 into a positive signal. A minimum value selecting unit
25 74 selects a smaller one of the signal J and the absolute value signal D4' to generate an output signal L.

The sign extracting unit 76 extracts sign information of the delay signal D4. For example, a sign is "+" when the delay signal D4 is positive, and a sign is "-" when the delay signal D4 is negative. The
5 extracted sign information is sent to a sign adding unit 77. The sign adding unit 77 adds the extracted sign information to the output signal L to generate an output signal M1 having an original sign. In this case, as the output signal M1, not only a single pulse
10 signal, but also the first and last pulse signals of continuous pulse signals are extracted. However, since almost pulse trains are removed in the continuous pulse signals, even though the first and last pulse signals of the continuous pulse signals are removed from the
15 original video signal, an actual video image is hardly adversely affected.

The output signal M1 is further supplied to a limiter unit 78. In the limiter unit 78, an amplitude value of the output signal M1 is limited within a
20 predetermined range as shown by a graph 79 in FIG. 3, and a signal is output as a more appropriate output signal N (single pulse component d in FIG. 1).

The limiter unit 78 is a converting circuit which converts an input signal by using the characteristics
25 shown by the graph 79. In the graph 79, the abscissa expresses an input value, and the ordinate expresses an output value. According to the characteristics, when

the input value falls within the range of -4 to +4, the input is output without being changed. When the input value falls out of the range, the output value is limited to a predetermined value. Furthermore, when
5 the input value is large, the output value is set to be smaller than the predetermined value or set to be 0.

In this manner, the output value is limited because handling in the subsequent signal processing circuit is considered. The signal having the
10 predetermined value or more is removed to be prevented from being handled as noise because the signal may be a video signal rather than noise.

An outline of a general operation of the pulse discriminating process described above will be
15 described below with reference to a flow chart. FIG. 6 is a flow chart showing an example of a pulse discriminating process of a single pulse detecting unit which is a main configuration of a noise reducing circuit according to an embodiment of the present
20 invention.

In step S21, the first delay signal D4 obtained by delaying the video signal D3 by a predetermined first pixel is generated, and the second delay signal D5
obtained by delaying the video signal D3 by a second
25 pixel is generated. In step S22, the pulse discriminating unit 42-1 adds the video signal D3 and the first delay signal D4 to each other and adds the

first delay signal D4 and the second delay signal D5 to each other. In step S23, the pulse discriminating unit 42-1 calculates a minimum value (J) of absolute values of the additional results and compares the minimum value (J) with the absolute value of the first delay signal D4 to select a minimum one.

As a result, in step S24, continuous pulse signals of the frame difference signal c are canceled out and removed. In step S25, a single pulse signal M1 is extracted.

The steps in the flow chart in FIG. 6 can be replaced with circuit blocks, respectively. Therefore, all the steps in the flow chart can be redefined as blocks. More specifically, a general operation of the pulse discriminating unit 42-1 of the first single pulse detecting unit 33 is not limited to the concrete embodiment of the pulse discriminating unit 42-1 in FIG. 3. As the general operation, only the operation described above may be performed.

The second single pulse detecting unit 34 will be described below. As described above, the second single pulse detecting unit 34 detects a size of a single pulse included in a video signal a, and generates an output f expressing, for example, a 0 to 1 time coefficient depending on an amplitude of the detected pulse. The second single pulse detecting unit 34 has the same configuration as that of the first single

pulse detecting unit 33 except for the configuration of the limiter unit 78. Therefore, the same reference numerals as in the first single pulse detecting unit 33 denote the same parts in the second single pulse
5 detecting unit 34, detailed explanation of the second single pulse detecting unit 34 will not be repeated here.

FIG. 7 is a diagram showing input/output characteristics of the limiter unit 78 of the second
10 single pulse detecting unit 34. In the graph shown in FIG. 7, an x-axis direction expresses a size of an input signal, and a y-axis direction expresses a size of an output signal. According to the characteristics, a positive value (coefficient value) is output
15 independently of the polarity of the input value. When the input value falls within the range of -4 to +4, the coefficient value is a constant value. When the input value falls out of the range, the coefficient value is set to be smaller than a predetermined value or set to
20 0.

In this manner, the limiter unit of the first single pulse detecting unit 33 and the limiter unit of the second single pulse detecting unit 34 are different from each other in input/output characteristic. For
25 this reason, the second single pulse detecting unit 34 can output a signal representing a ratio of subtraction of a noise component detected from the frame difference

signal from the present signal by the second single pulse detecting unit 34.

[Second Embodiment]

A noise reducing circuit 21 according to a second
5 embodiment of the present invention will be described
below. The noise reducing circuit 21 according to the
second embodiment is configured to remove a single
pulse and continuous pulses. In the second embodiment,
configurations of single pulse detecting units 33 and
10 34 are different from those of the first embodiment.
Therefore, the same reference numerals as in the first
embodiment denote the same parts in the second
embodiment, and a detailed description thereof will not
be repeated here.

15 FIG. 8 is a block diagram showing an example of a
configuration of the first single pulse detecting unit
33 which is a main configuration of the noise reducing
circuit according to the second embodiment of the
present invention. FIG. 9 is a timing chart showing an
20 example of an operation of the first single pulse
detecting unit 33 according to an embodiment of the
present invention. The configuration and the operation
of the first single pulse detecting unit 33 will be
described below with reference to FIGS. 8 and 9.

25 [Rectangular Wave Removing Unit]

Since the configuration of the rectangular wave
removing unit 41 of the first single pulse detecting

unit 33 shown in FIG. 8 is the same configuration of the first embodiment, a description thereof will not be repeated here.

[Pulse Discriminating Unit]

5 A pulse discriminating unit 42-2 shown in FIG. 8 extracts a region of a single pulse signal and a region of continuous pulse signals.

 The pulse discriminating unit 42-2 includes a delay circuit 61, a delay circuit 62, an attenuating unit 63, an adder 65, an attenuating unit 68, and an adder 66.

 The delay circuit 61 delays a video signal D3. The delay circuit 62 delays a delay signal D4 output from the delay circuit 61. The attenuating unit 63 receives the video signal D3 to attenuate the video signal D3 to 1/2. The adder 65 adds the attenuated video signal D3 and the delay signal D4 to each other to generate an output G. The attenuating unit 68 receives a delay signal D5 output from the delay circuit 62 to attenuate the delay signal D5 to 1/2. The adder 66 adds the delay signal D4 and the attenuated delay signal D5 to each other to generate an output H.

 An output G is input to the absolute value unit 69. The absolute value unit 69 generates an absolute value signal G' obtained by converting a negative signal of the output G into a positive signal. The

output H is input to the absolute value unit 70. The absolute value unit 70 generates an absolute value signal H' obtained by converting a negative signal of the output H into a positive signal. A maximum value selecting unit 71 selects a larger one of the absolute value signal G' and the absolute value signal H' to output the selected signal as a signal I. As shown in FIG. 9, with the above processes, as the signal I, only the single pulse signal and the continuous pulse signals are extracted.

On the other hand, the delay signal D4 output from the delay circuit 61 is input to an absolute value unit 75 and a sign extracting unit 76. The absolute value unit 75 generates an absolute value signal D4' obtained by converting a negative signal of the delay signal D4 into a positive signal. A minimum value selecting unit 74 selects a smaller one of the signal I and the absolute value signal D4' to generate an output signal L.

The sign extracting unit 76 extracts sign information of the delay signal D4. For example, a sign is "+" when the delay signal D4 is positive, and a sign is "-" when the delay signal D4 is negative. The extracted sign information is sent to a sign adding unit 77. The sign adding unit 77 adds the extracted sign information to the output signal L to generate an output signal M2 having an original sign. As a result,

as shown in FIG. 9, as an output signal M2, not only a single pulse signal but also continuous pulse signals are extracted.

5 The output signal M2 is further supplied to a limiter unit 78. In the limiter unit 78, an amplitude value of the output signal M2 is limited within a predetermined range as shown by a graph 79 in FIG. 8, and a signal is output as a more appropriate output signal N (single pulse component d in FIG. 1).

10 An outline of a general operation of the pulse discriminating process described above will be described below with reference to a flow chart. FIG. 10 is a flow chart showing an example of a pulse discriminating process of a single pulse detecting unit which is a main configuration of a noise reducing
15 circuit according to an embodiment of the present invention.

In step S31, the pulse discriminating unit 42-2 generates a first delay signal D4 obtained by delaying
20 the video signal D3 by a predetermined first pixel and generates the second delay signal D5 obtained by delaying the video signal D3 by a second pixel. In step S32, the pulse discriminating unit 42-2 makes the video signal D3 and the delay signal D5 1/2 to add the
25 delay signal D4 to each of the 1/2 video signal D3 and the 1/2 delay signal D5.

In step S33, the pulse discriminating unit 42-2

calculates a maximum value (I) of absolute values of additional results and selects a minimum one of the maximum value (I) and the first delay signal D4. As a result, in step S34, the pulse discriminating unit 42-2 can generate a signal M2 including a "region of a single pulse signal" and a "region of continuous pulse signals".

The steps in the flow chart in FIG. 10 can be replaced with circuit blocks, respectively. Therefore, all the steps in the flow chart can be redefined as blocks. More specifically, a general operation of the pulse discriminating unit 42-2 of the first single pulse detecting unit 33 is not limited to the concrete embodiment of the pulse discriminating unit 42-2 in FIG. 8. As the general operation, only the operation described above may be performed.

[Third Embodiment]

A noise reducing circuit 21 according to a third embodiment of the present invention will be described below. The noise reducing circuit 21 according to the third embodiment is configured to select a mode (β mode) in which a single pulse is removed and a mode (α mode) in which a single pulse and continuous pulses are removed. In the third embodiment, the configurations of the single pulse detecting units 33 and 34 are different from those of the first embodiment. Therefore, the same reference numerals as in the first

embodiment denote the same parts in the third embodiment, and a detailed description thereof will not be repeated here.

FIG. 11 is a block diagram showing an example of a configuration of the first single pulse detecting unit 33 which is a main configuration of the noise reducing circuit according to the third embodiment of the present invention. The configuration and the operation of the first single pulse detecting unit 33 will be described below with reference to FIGS. 11, 4, and 9.

[Rectangular Wave Removing Unit]

Since the configuration of the rectangular wave removing unit 41 of the first single pulse detecting unit 33 shown in FIG. 11 is the same configuration of the first embodiment, a description thereof will not be repeated here.

[Pulse Discriminating Unit]

A pulse discriminating unit 42-3 shown in FIG. 11 is configured to switch the configuration of the pulse discriminating unit 42-1 in FIG. 3 and the configuration of the pulse discriminating unit 42-2 in FIG. 8 by a selector unit 64, a selector unit 67, and a selecting unit 73. In this case, any one of the α mode and the β mode can be switched by an external operation performed by a user. With this configuration, by selection signals α and β , two functions including a "function of detecting a single pulse" or a "function

of detecting a single pulse and continuous pulses" can be arbitrarily switched.

More specifically, when a first detection mode setting is α , an output G is a signal obtained by adding $D3 \times 1/2$ to $D4$, and an output H is a signal obtained by adding $D4$ to $D5 \times 1/2$. Of values obtained by converting the output G and the output H into absolute values, the maximum value is output as a signal I, and the minimum value is output as a signal J.

On the other hand, when a first detection mode setting is β , an output G is a signal obtained by adding $D3$ and $D4$ to each other, and an output H is a signal obtained by adding $D4$ and $D5$ to each other. Of values obtained by converting the output G and the output H into absolute values, the maximum value is output as a signal I, and the minimum value is output as a signal J.

When a second detection mode setting is α , the signal I of the maximum value is selected and output as a signal K.

When the second detection mode setting is β , the signal J of the minimum value is selected, and a value obtained by converting $D4$ into an absolute value is compared with the signal K to output a smaller one as a signal L. An output M ($M1$, $M2$) obtained by adding a sign of $D4$ to the signal L is corrected in an output

signal level by an input/output converting process of the limiter unit 78.

As described above, with the configuration of the pulse discriminating unit 42-3 shown in FIG. 11, two functions including a function of detecting a single pulse depending on the selection signals α and β and a function of detecting a single pulse and continuous pulses can be arbitrarily switched.

An outline of a general operation of the single pulse detecting process described above will be described below with reference to a flow chart. FIG. 12 is a flow chart showing an example of a rectangular wave removing process and a pulse discriminating process of a single pulse detecting unit which is a main configuration of a noise reducing circuit according to an embodiment of the present invention.

In steps S101 and S102, a loop Y coordinate and a loop X coordinate are defined. In this case, a Y coordinate and the X coordinate correspond to a screen of a video image. Therefore, in a high-definition image, coordinates are defined as 1920 × 1080 at a maximum by using pixels as units.

A rectangular wave removing process is executed first. In step S103, pixel data of an alignment IN defined by coordinates is stored as an alignment Xp of a buffer. Furthermore, in step S104, end portions of a

screen, i.e., portions given by $X < 0$ and $X > X_MAX$ are terminated. In step S105, differences A and B between delay signals shown in FIG. 4 and a secondary differential signal E are calculated. In steps S106 and S107, a polarity is determined, and a signal is output to a latter part without being specially processed depending on the polarity, or the signal is set to 0 to perform a rectangular wave excluding process.

10 A pulse discriminating process is executed. In step S108, pixel data of an alignment F defined by coordinates is stored as an alignment Xq of the buffer to perform a delay process and an arithmetic process. In steps S109 and S110, depending on the detection mode setting by α or β , a maximum value or a minimum value of the absolute values of the delay signals is calculated. In step S111, a minimum value L is calculated. A sign is rationalized in step S112, and the limiter process is performed in step S113.

20 In steps S114 and S115, these processes are performed with respect to the loop X coordinate and the loop Y coordinate. More specifically, these processes are executed to all pixel data.

25 The steps in the flow chart in FIG. 12 can be replaced by circuit blocks, respectively. Therefore, all the steps in the flow chart can be redefined as blocks. More specifically, in a general operation of

the first single pulse detecting unit 33, without the concrete circuit as shown in FIG. 11, the single pulse or the "region of the single pulse signal and the region of the continuous pulse signals" M2 can be
5 detected by performing the same processes as described above by a computer program and a computer.

[Fourth Embodiment]

A noise reducing circuit 21' according to a fourth embodiment of the present invention will be described
10 below. In the noise reducing circuit 21' according to the fourth embodiment, a video signal of a current frame from which a single pulse is removed is output, and a video signal of a delay frame from which a single pulse is removed is output.

15 FIG. 13 is a block diagram showing a configuration of a noise reducing circuit 21' of the fourth embodiment according to an embodiment of the present invention. FIG. 14 is a timing chart showing an example of an operation of the noise reducing circuit
20 21' according to an embodiment of the present invention. A configuration and operation of the noise reducing circuit 21' will be described below with reference to FIGS. 13 and 14.

The noise reducing circuit 21' includes a frame
25 memory 31, a single pulse detecting unit 142, a single pulse detecting unit 143, a single pulse detecting unit 144, and an adder 141 which adds one terminals of these

units. Further more, the noise reducing circuit 21' includes a multiplier 145 to which outputs of the single pulse detecting unit 143 and the single pulse detecting unit 142 are connected, a multiplier 146 to which the single pulse detecting unit 143 and the single pulse detecting unit 144 are connected, an adder 147, and an adder 148.

In this case, the noise reducing circuit 21' shown in FIG. 13 includes the configuration of the noise reducing circuit 21 shown in FIG. 1. The single pulse detecting unit 143 and the single pulse detecting unit 144 correspond to the first single pulse detecting unit 33 and the second single pulse detecting unit 34 in FIG. 1, respectively, and the multiplier 146 and the adder 148 correspond to the multiplier 35 and the adder 36 in FIG. 1, respectively.

On the other hand, the single pulse detecting unit 142, the multiplier 145, and the adder 147 perform operations equivalent to that of the first single pulse detecting unit 33 in FIG. 1. However, since the single pulse detecting unit 142 receives only a delay frame signal from the frame memory 31, a noise-removed frame signal before one frame is obtained as an output from the adder 147.

When, for example, an IP converting circuit (not shown) is arranged in the latter part, the frame signal before one frame can be used in the IP converting

circuit.

With the above configuration, a noise reducing process of a video signal in, for example, an image processing apparatus or the like can be performed by using the single pulse detecting unit 142 or the like.

[Video Apparatus using Noise Reducing Circuit according to Embodiment of the Present Invention]

An example of a video apparatus 10 using the noise reducing circuit 21 described above will be described below with reference to a drawing. FIG. 15 is a block diagram showing an example of a configuration of a video apparatus to which a noise reducing circuit according to an embodiment of the present invention is applied.

The video apparatus 10 includes a digital tuner 13 which receives signals from an antenna 11 and an antenna 12, analog tuner 14, an MPEG-2 decoder 15 connected to the digital tuner 13, an A/D converter 16 connected to the analog tuner 14, and an A/D converter 17 connected to an external connector. Furthermore, the video apparatus 10 has a signal select 18 to which these components are connected and a signal processing unit 19 connected to the signal select 18.

The signal processing unit 19 mentioned here is the video apparatus 10 including the noise reducing circuit 21 described above, a scaling unit serving as the latter part of the noise reducing circuit 21, a

video processing unit 23 serving as the latter part of the scaling unit, a driver 24 serving as the latter part of the video processing unit 23, and a display unit 20 which receives a video signal from the driver 24 to perform display.

An MPEG-2 transport stream signal demodulated by the digital tuner 13 connected to the antenna 11 is subjected to a decoding process by the MPEG-2 decoder 15 and then input to the signal select 18. Similarly, a video signal demodulated by the analog TV tuner 14 connected to the antenna 12 is converted from an analog signal into a digital signal by the A/D converter 16 and then input to the signal select 18.

A video signal from an external video apparatus such as a VTR or a DVD player is converted from an analog signal into a digital signal by the A/D converter 17 and then input to the signal select 18.

The signal select 18 selects an input video signal by a selecting operation by a user to output the video signal to the signal processing unit 19.

The video signal input to the signal processing unit 19 passes through the noise reducing circuit 21 described above, a scaling process unit 22 which adjusts the number of pixels to the number of pixels of a display unit 20 with respect to the input video signal, and a video processing unit 23 which performs a contour correcting process or the like and is supplied

to the display unit 20 through the driver 24 to display a video image.

Even in the video apparatus 10, in the noise reducing circuit 21 described above, by using a single pulse component reliably detected by removing a rectangular wave component from a noise component, noise of a single pulse component can be reliably removed from a video signal or the like. In this manner, since especially outstanding single pulse component noise on a video screen can be effectively removed, a vivid image display can be achieved.

According to the various embodiments described above, a person skilled in the art can realize the present invention. However, furthermore, the person skilled in the art can easily conceive various modifications of these embodiments, and can apply the present invention to various embodiments without inventive ability. Therefore, the present invention covers wide ranges consistent with the disclosed principle and the novel characteristics, and is not limited to the embodiments described above.

Industrial Applicability

The present invention can be widely used in industries which manufacture a noise reducing circuit, a noise reducing method, and a video apparatus which removes a rectangular wave from a noise signal to reliably detect and remove a single pulse.

C L A I M S

1. A noise reducing circuit comprising:

a frame memory configured to frame-delay a video signal;

5 a first arithmetic unit configured to subtract the frame-delayed video signal given by the frame memory from the video signal to output a first frame difference signal;

10 a first rectangular wave removing unit configured to remove a rectangular wave component from the first frame difference signal to generate a second frame difference signal;

15 a first pulse discriminating unit configured to receive the second frame difference signal, remove a continuous pulse component from the second frame difference signal, and output a single pulse component; and

a second arithmetic unit configured to subtract the single pulse component from the video signal.

20 2. The noise reducing circuit according to claim 1, further comprising:

a second rectangular wave removing unit configured to receive the video signal to remove a rectangular wave component;

25 a second pulse discriminating unit configured to receive the video signal from which a rectangular wave component is removed by the second rectangular wave

removing unit, remove a continuous pulse component from the video signal to calculate a single pulse component, and output a coefficient signal obtained by converting the single pulse component; and

5 a multiplying unit configured to multiply the single pulse component output from the first pulse discriminating unit by the coefficient signal output from the second pulse discriminating unit to output a multiplication result.

10 3. The noise reducing circuit according to claim 1, wherein

 the first rectangular wave removing unit calculates a first delay video signal obtained by delaying the first frame difference signal by a first pixel number and a second delay video signal obtained by delaying the first frame difference signal by a second pixel number, forms a first differential signal from the first frame difference signal and the first delay video signal, forms a second differential signal from the first delay video signal and the second delay video signal to calculate polarities of the first and second differential signals, causes a smaller one of absolute value signals of the first and second differential signals to pass when the polarities are equal to each other, and causes a signal having a value of 0 to pass when the polarities are different from each other to remove the rectangular wave component

15

20

25

from the first frame difference signal.

4. The noise reducing circuit according to claim 1, wherein

5 the first pulse discriminating unit calculates a first delay video signal obtained by delaying the second frame difference signal by a first pixel number and a second delay video signal obtained by delaying the second frame difference signal by a second pixel number, adds the second frame difference signal to the first delay video signal, adds the second delay video
10 signal to the first delay video signal, selects a smaller one of absolute value signals of the added signals to cancel out a continuous pulse component in the second frame difference signal, and causes the single pulse component to remain.
15

5. The noise reducing circuit according to claim 1, wherein

the first pulse identifying unit calculates a first delay video signal obtained by delaying the second frame difference signal by a first pixel number
20 and a second delay video signal obtained by delaying the second frame difference signal by a second pixel number, calculates two signals obtained by adding the first delay video signal to results obtained by multiplying the second frame difference signal and the
25 second delay video signal by $1/2$, compares a large one of the absolute value signals of signals which are the

additional results with an absolute value of the first
delay video signal to output a small signal, and
extracts a signal value of a region of a single pulse
component in the second frame difference signal and a
5 signal value of a region of a continuous pulse
component in the second frame difference signal.

6. The noise reducing circuit according to
claim 1, wherein

the first pulse discriminating unit, when a first
10 selection signal is received, calculates a first delay
video signal obtained by delaying the second frame
difference signal by a first pixel number and a second
delay video signal obtained by delaying the second
frame difference signal by a second pixel number, adds
15 the second frame difference signal to the first delay
video signal, adds the second delay video signal to the
first delay video signal, selects a smaller one of
absolute value signals of the added signals to cancel
out a continuous pulse component in the second frame
20 difference signal, and causes a single pulse component
to remain,

when a second selection signal is received,
calculates a first delay video signal obtained by
delaying the second frame difference signal by the
25 first pixel number and a second delay video signal
obtained by delaying the second frame difference signal
by the second pixel number, calculates two signals

obtained by adding the first delay video signal to
results obtained by multiplying the second frame
difference signal and the second delay video signal by
1/2, compares a larger one of the absolute value
5 signals of signals which are the additional results
with an absolute value of the first delay video signal
to output a small signal, and extracts a signal value
of a region of a single pulse component in the second
frame difference signal and a signal value of a region
10 of a continuous pulse component in the second frame
difference signal.

7. The noise reducing circuit according to
claim 1, wherein

the first pulse discriminating unit further
15 includes a limiter unit which limits an amplitude value
of a single pulse component to be output and supplies
the single pulse component to the second arithmetic
unit.

8. A video apparatus comprising:
20 a tuner unit configured to receive a broadcasting
signal to output a video signal;
a decoder unit configured to decode the video
signal from the tuner unit;
a frame memory configured to frame-delay the video
25 signal decoded by the decoding unit;
a first arithmetic unit configured to subtract the
frame-delayed video signal given by the frame memory

from the video signal to output a frame difference signal;

5 a rectangular wave removing unit configured to remove a rectangular wave component from the frame difference signal;

a pulse discriminating unit configured to receive the frame difference signal from which the rectangular wave component is removed by the rectangular wave removing unit and remove a continuous pulse component from the frame difference signal to output a single pulse component;

10

a second arithmetic unit configured to subtract the single pulse component from the video signal; and

a display unit configured to display a video image on a screen depending on the video signal obtained by subtracting the single pulse component from the video signal.

15

9. A noise reducing method comprising:

frame-delaying a video signal;

20 outputting a first frame difference signal obtained by subtracting the frame-delayed video signal from the video signal;

removing a rectangular wave component from the first frame difference signal and generating a second frame difference signal;

25

receiving the second frame difference signal and removing a continuous pulse component from the second

frame difference signal to output a single pulse component; and

subtracting the single pulse component from the video signal.

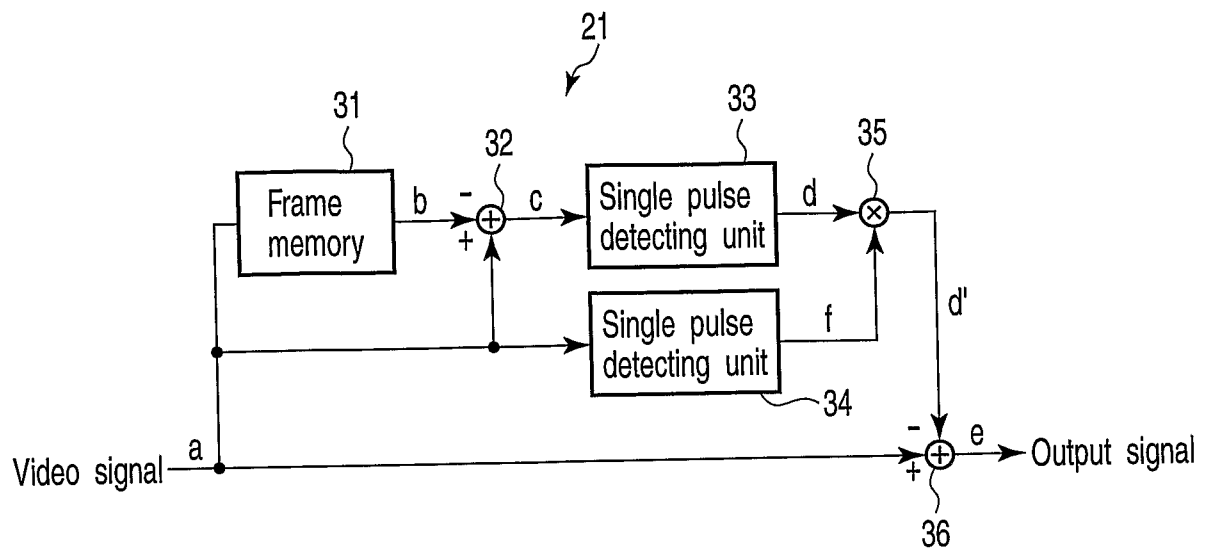


FIG. 1

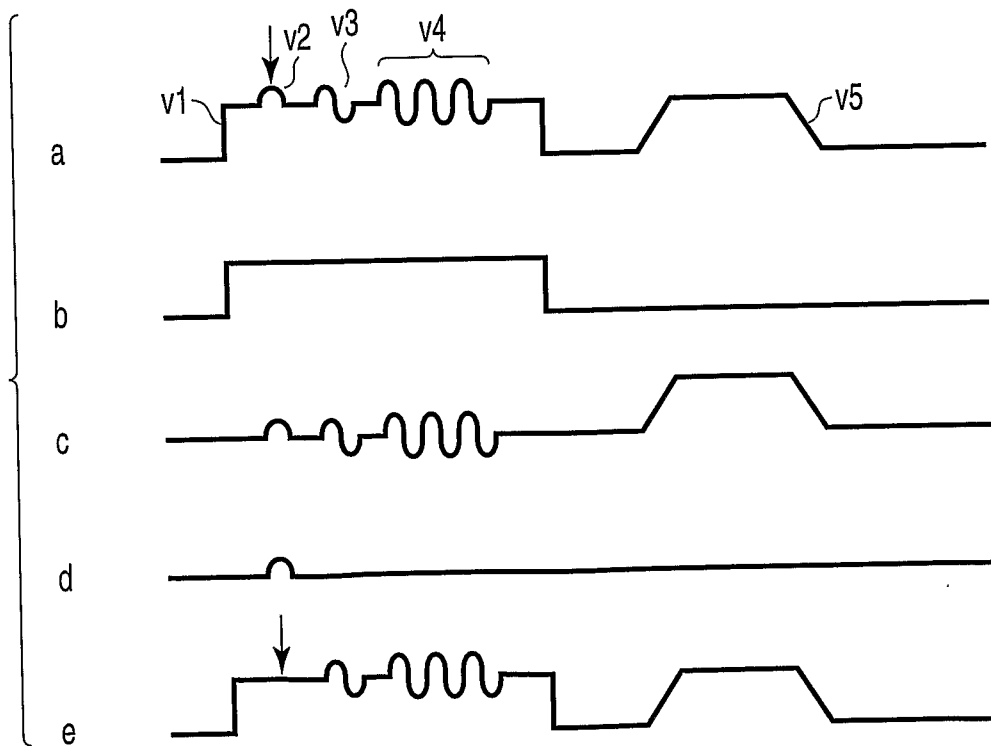
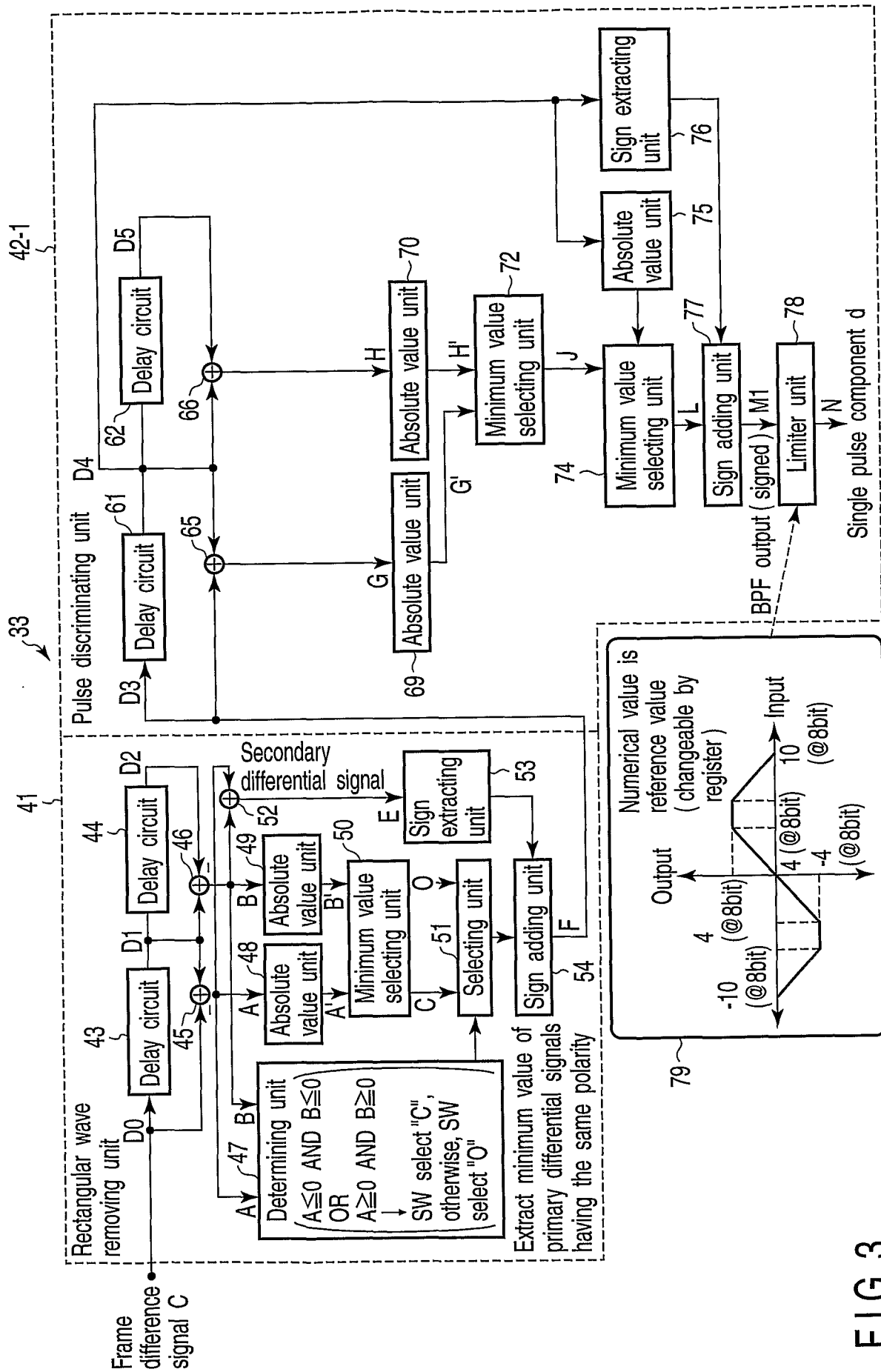


FIG. 2



3/14

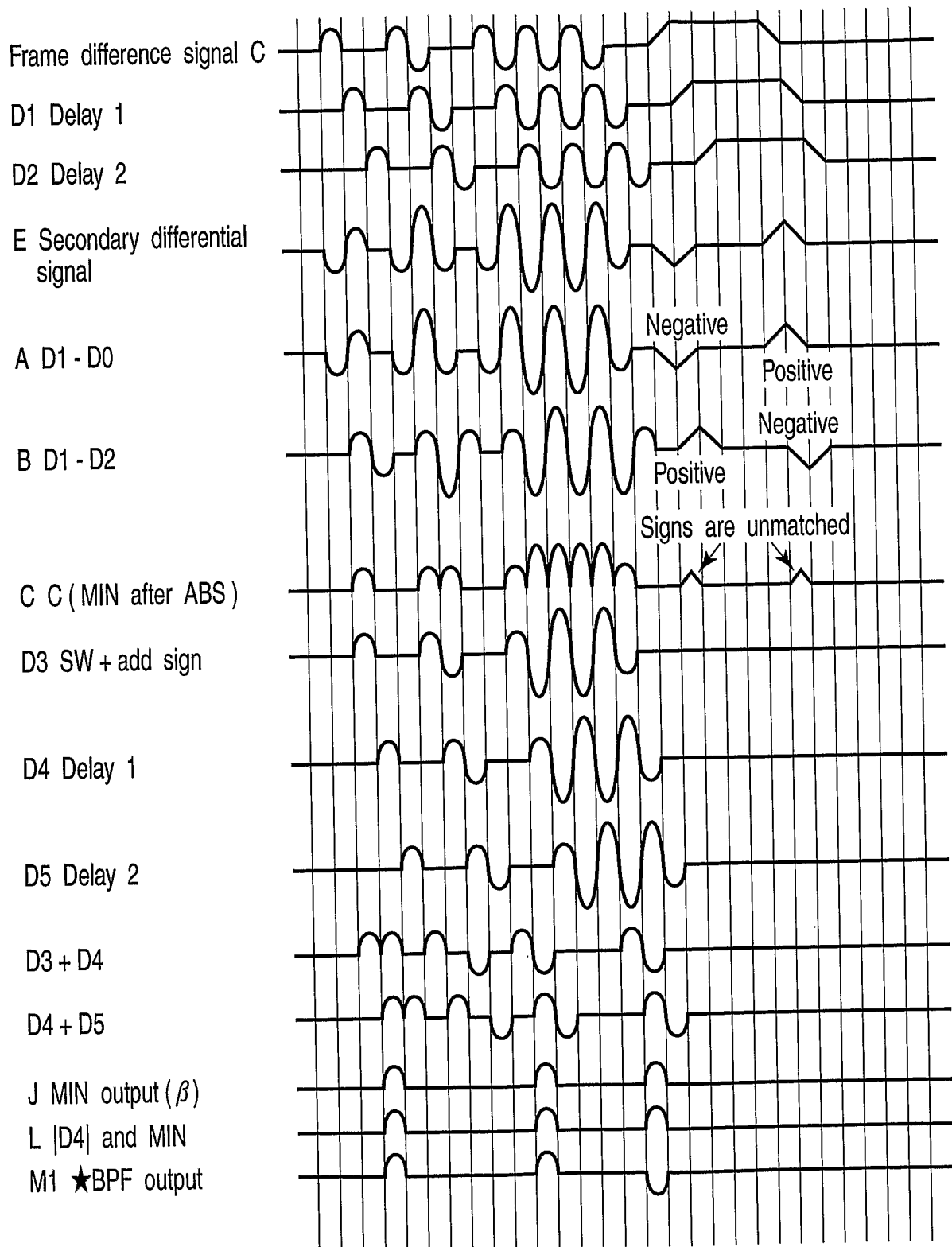


FIG. 4

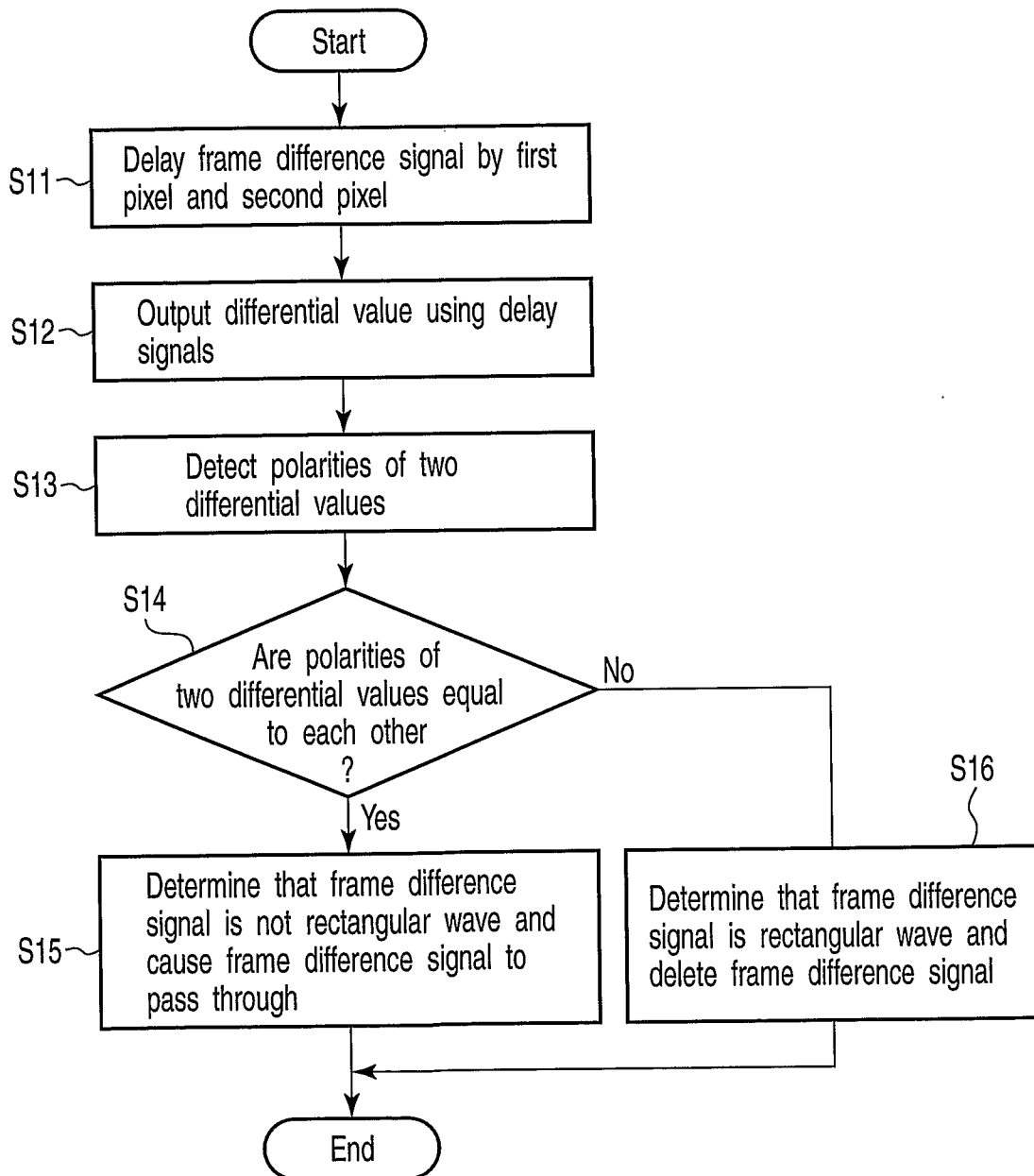


FIG. 5

5/14

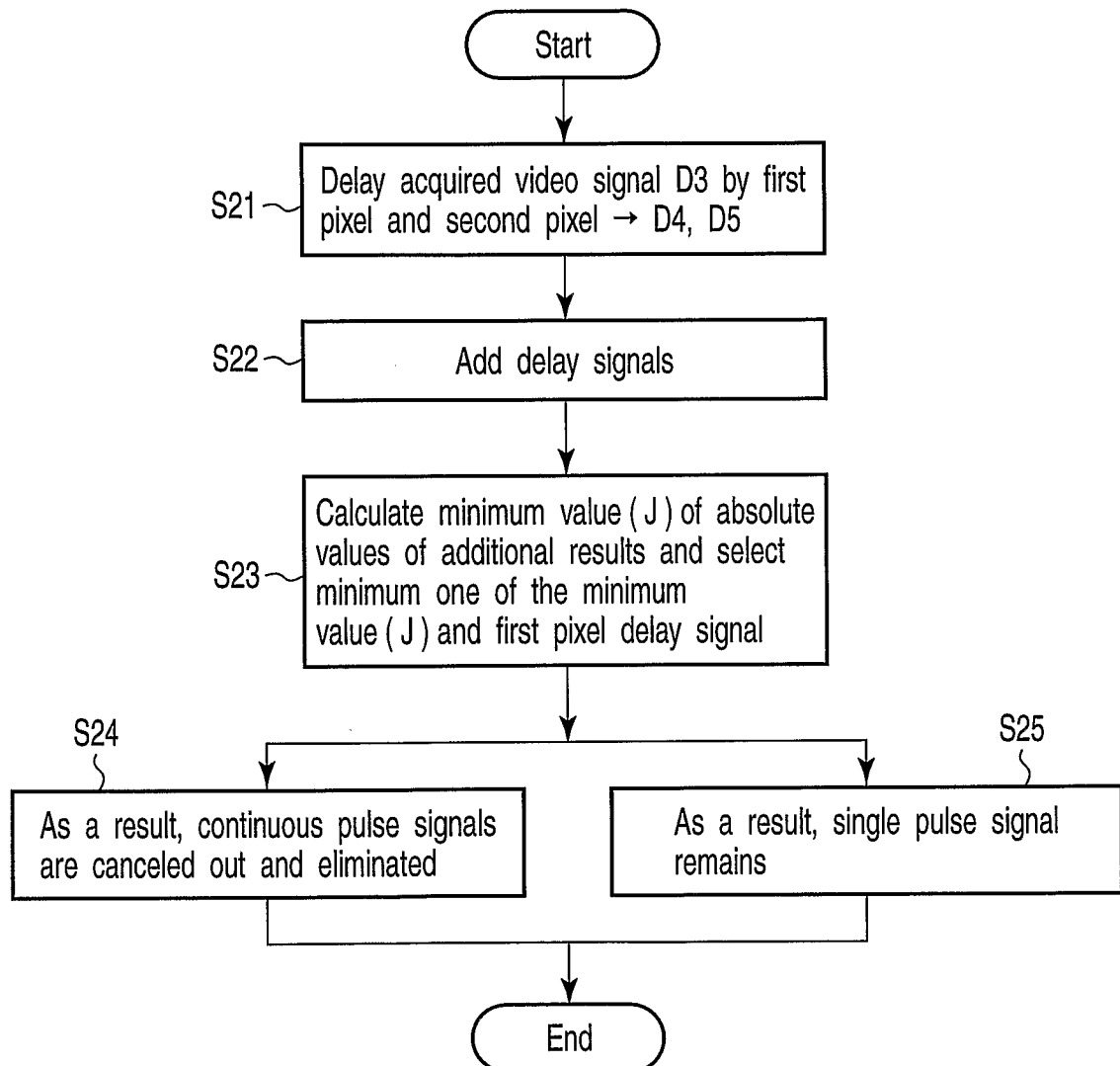


FIG. 6

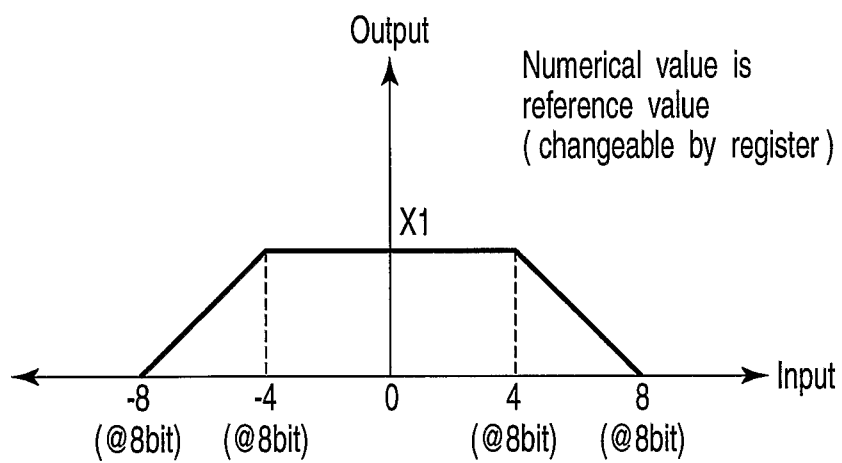


FIG. 7

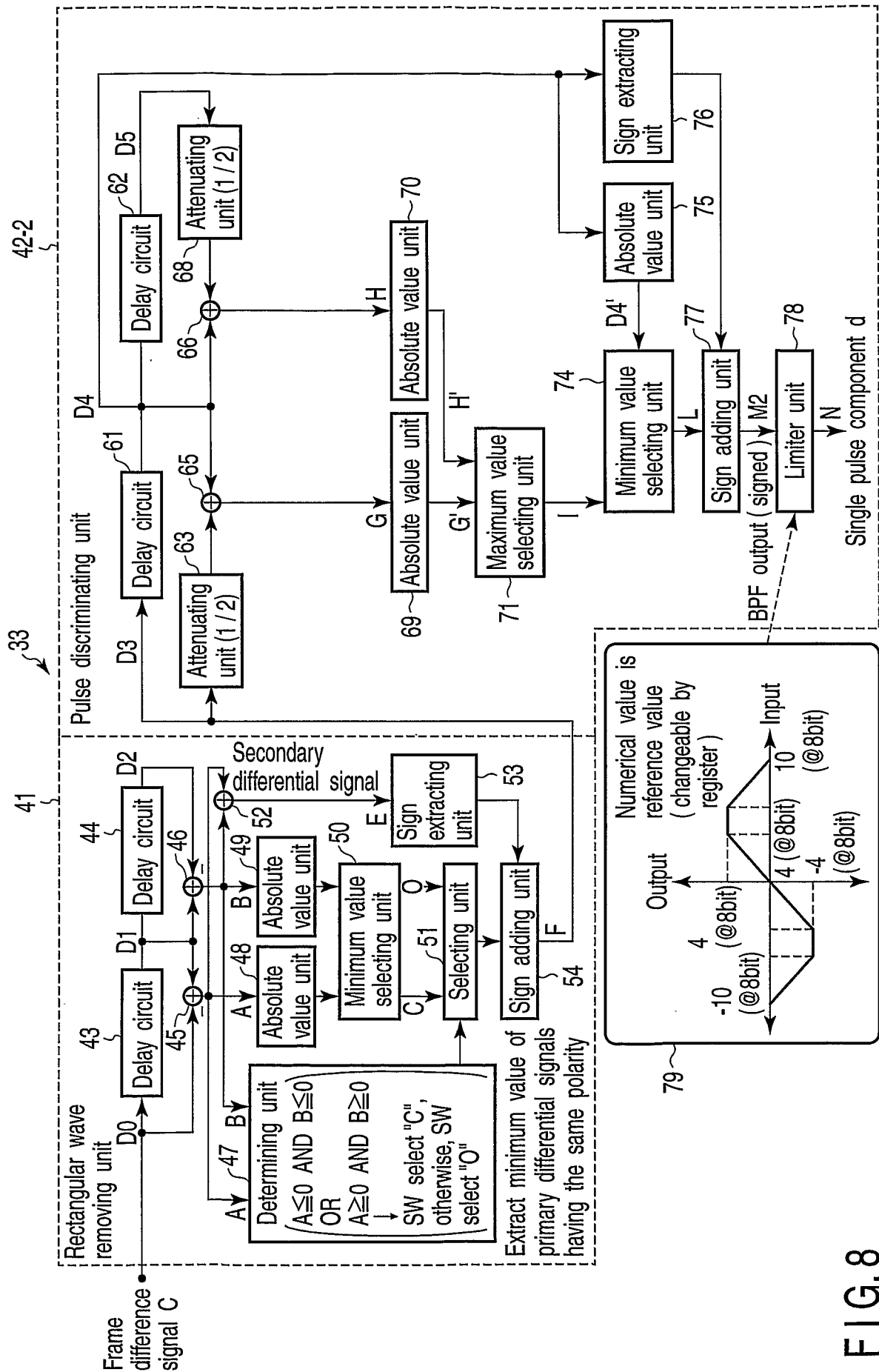


FIG. 8

8/14

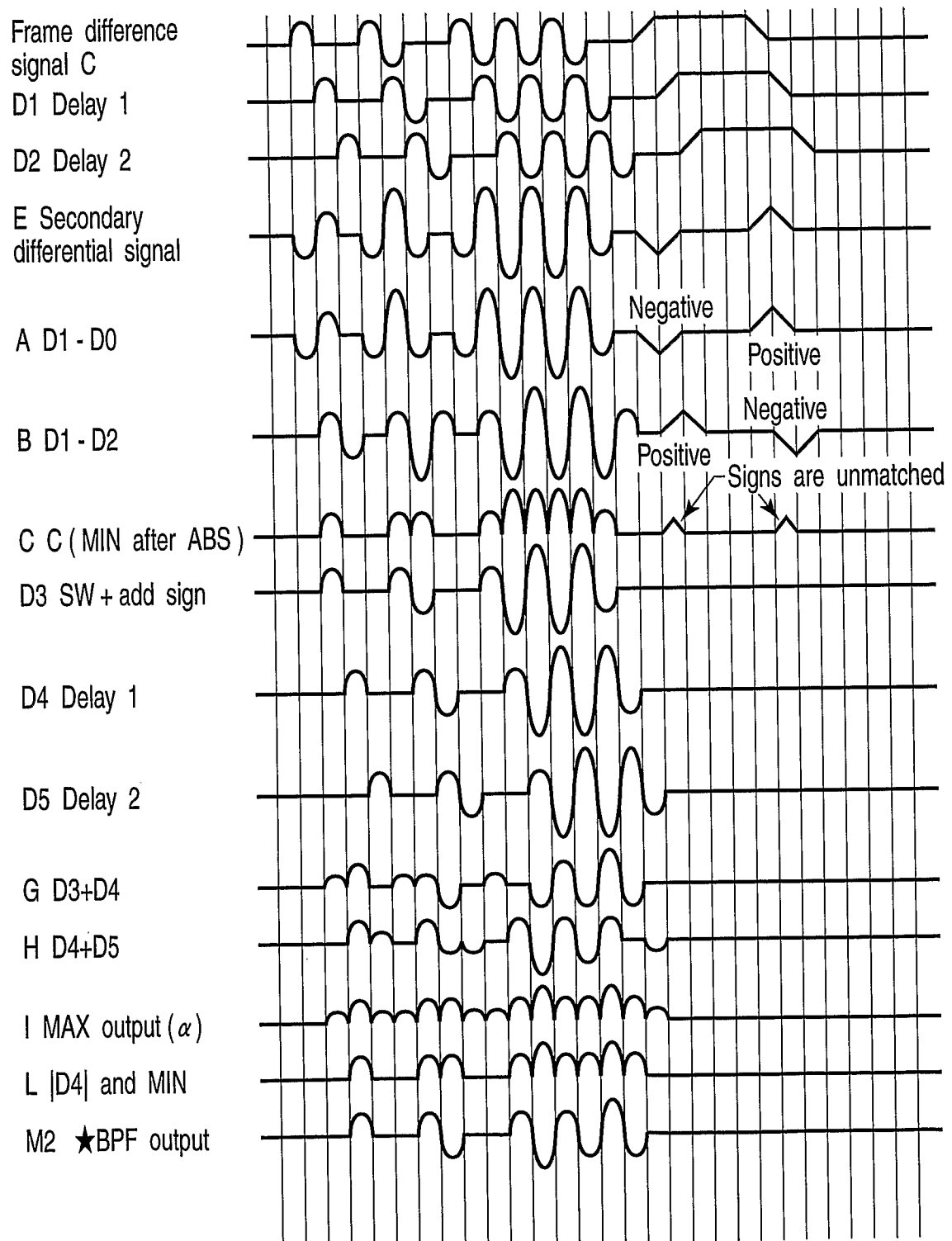


FIG. 9

9/14

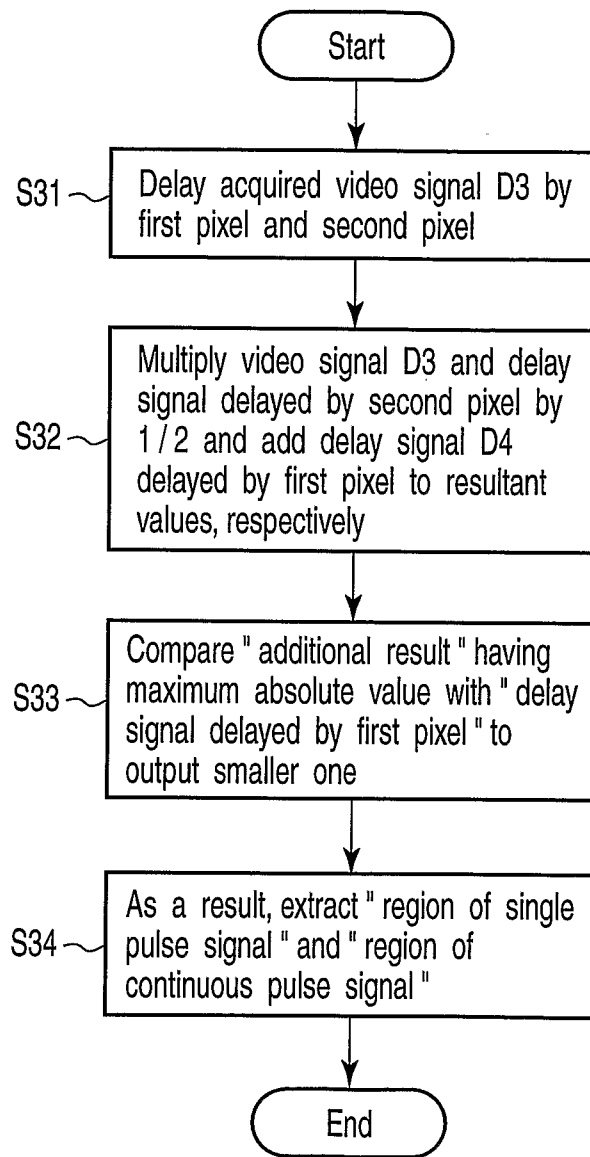
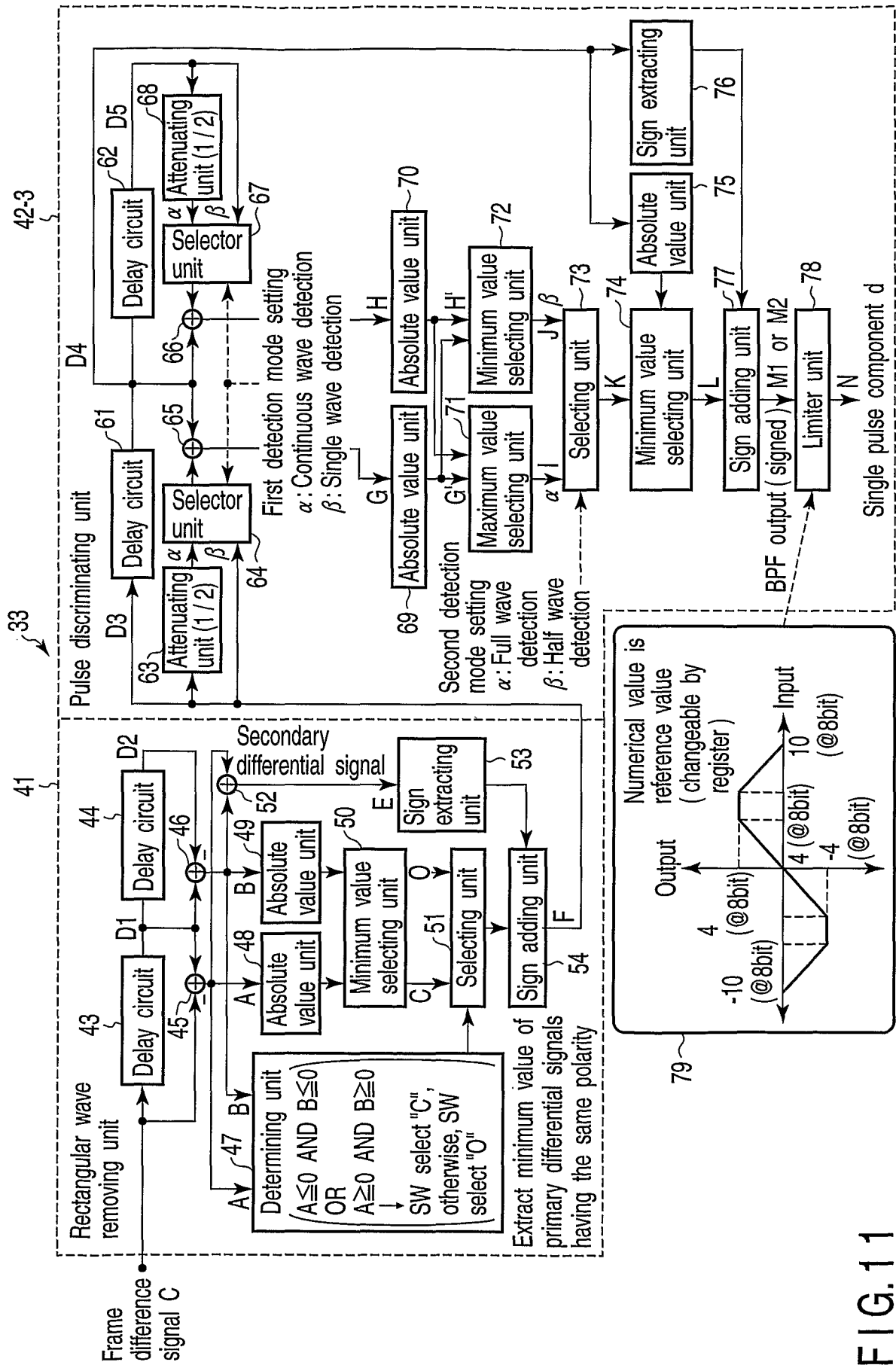


FIG. 10



11/14

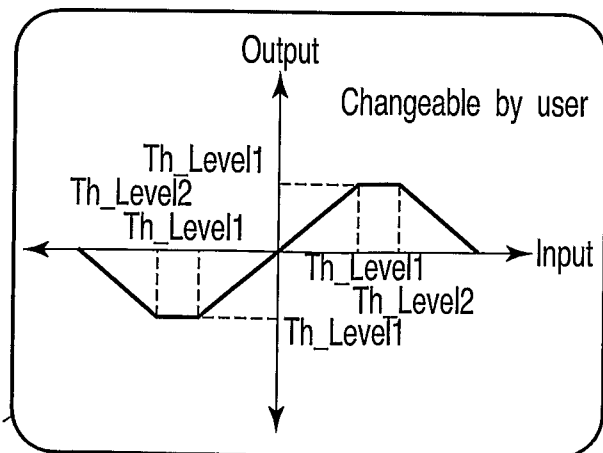
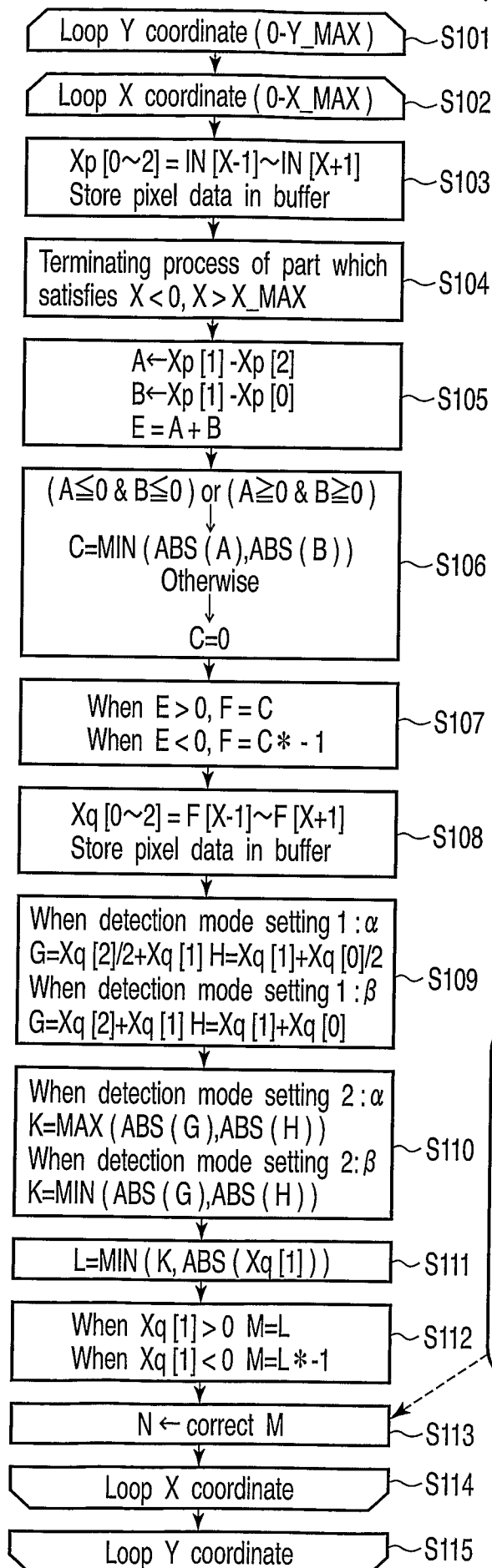
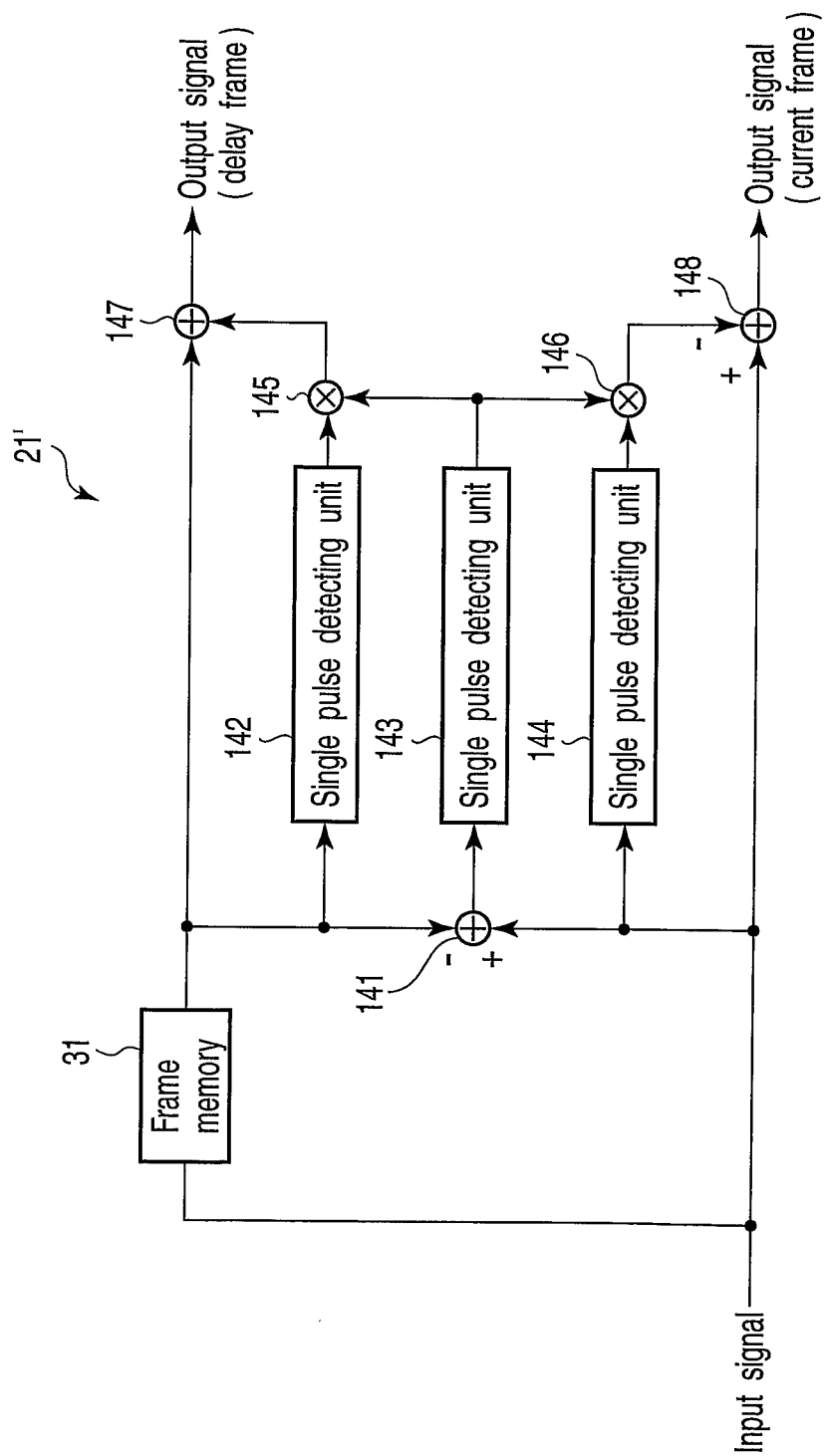


FIG. 12



13/14

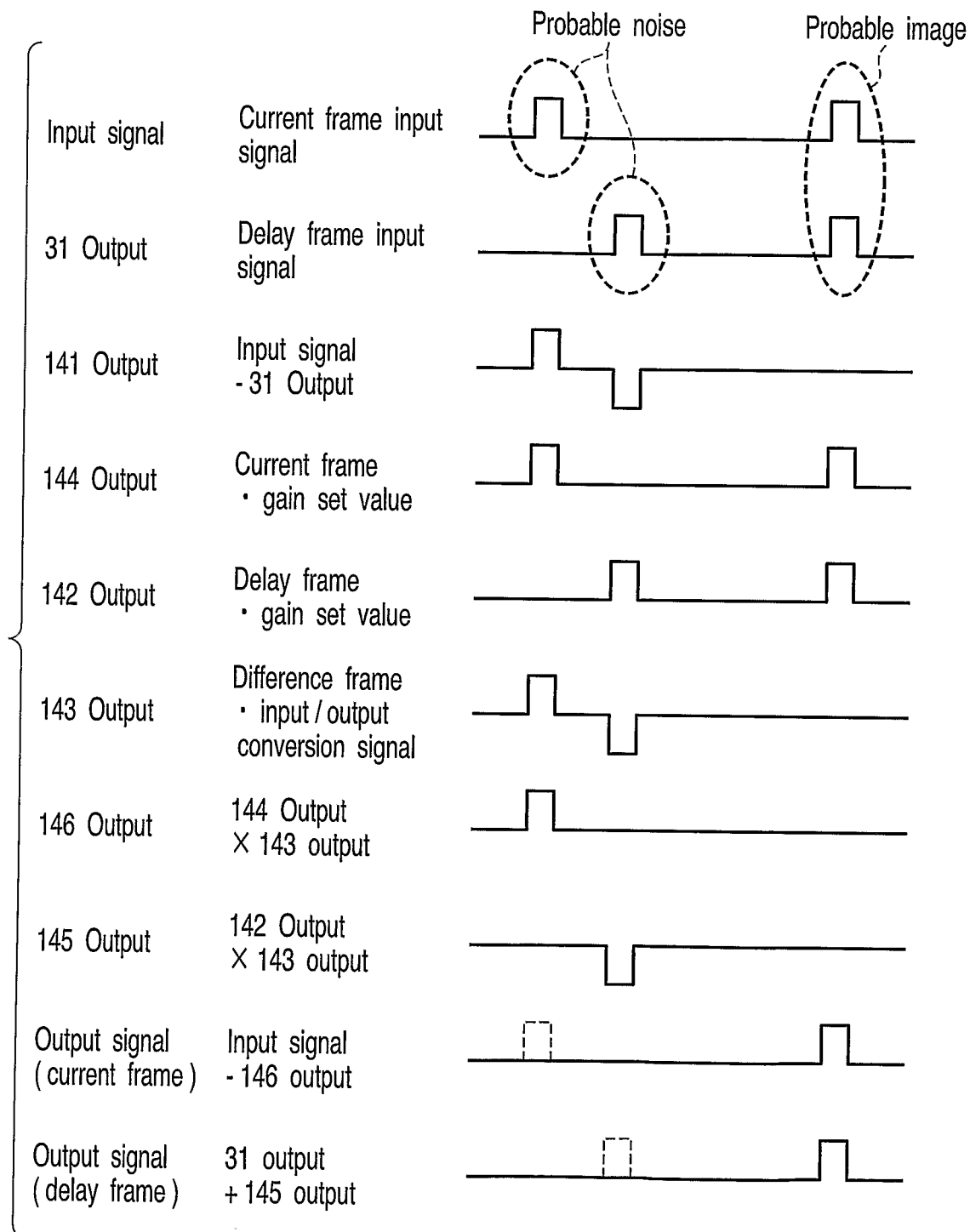


FIG. 14

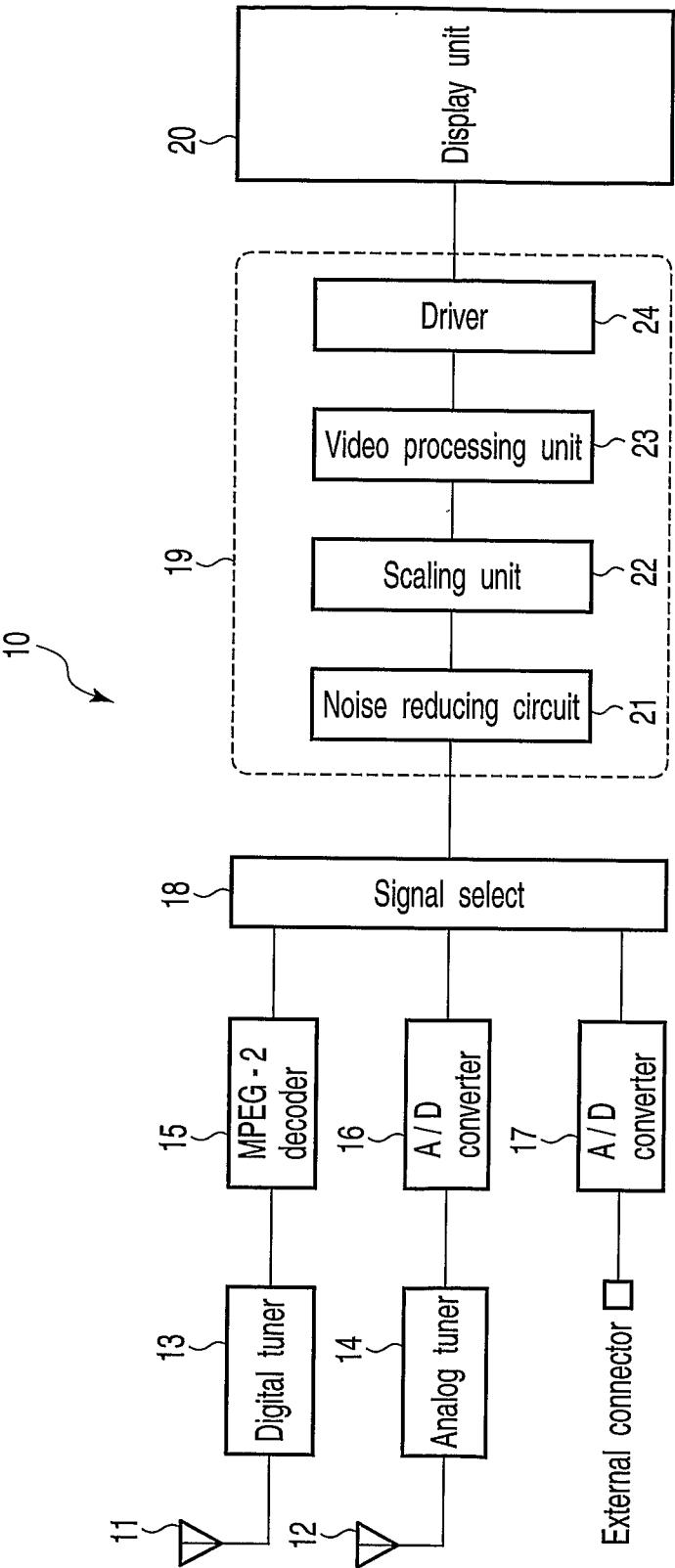


FIG.15

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2008/066801

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H04N5/213 (2006.01) i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H04N5/213

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2008
Registered utility model specifications of Japan 1996-2008
Published registered utility model applications of Japan 1994-2008

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 7-274045 A (Clarion Co., Ltd.) 1995.10.20, Figs 1,3,9,12 (No Family)	1-9
A	JP 4-20182 A (Sony Corporation) 1992.01.23, page 2,3 (No Family)	1-9



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

21.10.2008

Date of mailing of the international search report

04.11.2008

Name and mailing address of the ISA/JP

Japan Patent Office

3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan

Authorized officer

Naoki SATO

Telephone No. +81-3-3581-1101 Ext. 3581

5P 9562