May 6, 1969 J. O. McCALDIN ET AL 3,442,721

SEMICONDUCTING DEVICE

Original Filed Oct. 26, 1964

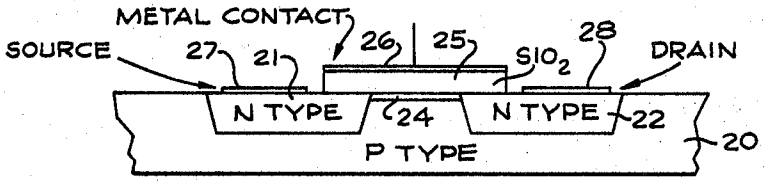


FIG. 1

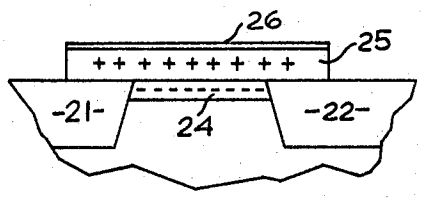


FIG. 2

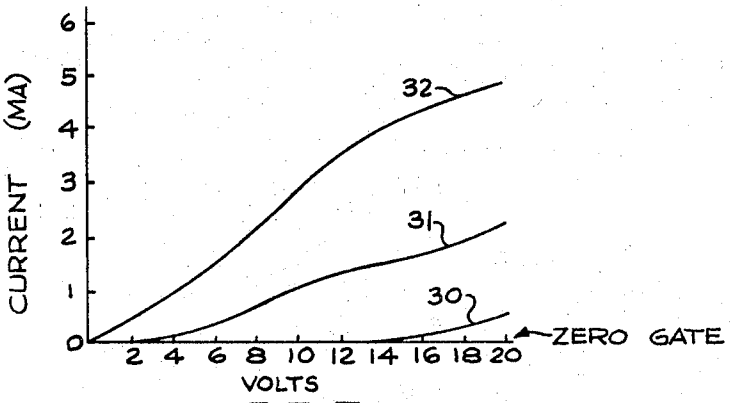


FIG. 3

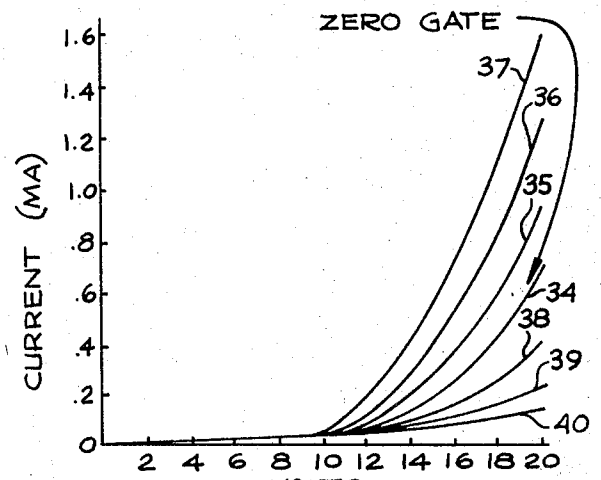


FIG. 4

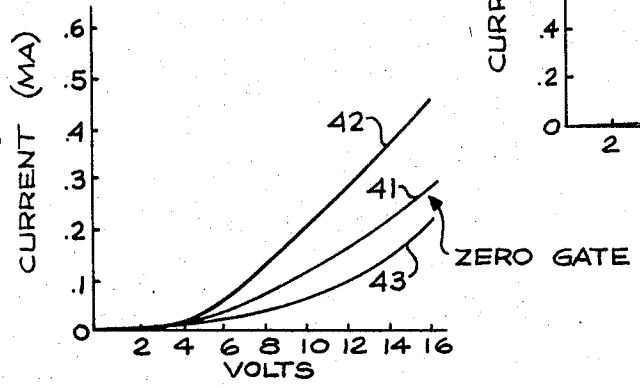


FIG. 5

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SEMICONDUCTING DEVICE

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Original application Oct. 26, 1964. Ser. No. 406,449, now Patent No. 3,328,210, dated June 27, 1967. Divided and this application July 18, 1966, Ser. No. 574,855
Int. Cl. H01l 3/12, 7/54, 11/00
U.S. Cl. 148—33 2 Claims

ABSTRACT OF THE DISCLOSURE

This invention relates to a product having a thin film of dielectric material such as silicon oxide overlying a substrate of semiconducting material where the dielectric layer contains ions implanted by bombardment. These ions induce a space charge in the underlying semiconductor and induce conduction electrons in the crystal to congregate near the dielectric layer and form a space charge.

This is a division of application Ser. No. 406,449, filed Oct. 26, 1964, now U.S. Patent No. 3,328,210.

The present invention is directed to semiconductor devices having implanted ions in an insulated layer.

One aspect of the present invention relates to semiconductor devices which have had insulation surface layers on a body of semiconducting material treated to control or alter the properties of the layer as well as the material adjacent to such a treated layer, which treatment results in the distribution of a permanently induced space charge in the treated layer.

In accordance with the broad aspects of the present invention an insulating surface layer on a semiconductor body is bombarded with ions of a predetermined space charge inducing type, thereby creating a permanent unneutralized charge in the surface layer and a corresponding charge of opposite polarity in the semiconductor body adjacent the insulating surface. The insulation layer is bombarded for a time sufficient to provide a concentration of space charge inducing ions sufficient to control or alter the conductivity characteristics of the volume of underlying semiconductor immediately adjacent to the insulating layer.

A particularly preferred feature of the present invention giving superior results is the formation of semiconductor devices by the bombardment of the heated silicon oxide surface of a semiconductor by donor type alkali metal ions selected from the group consisting of sodium, potassium, rubidium and cesium. The ions implanted in the oxide coating give rise to no change in the conductivity characteristics of the oxide insulation but their presence is evidenced rather by charge effects associated with the implanted ions which are reflected by changes in the conductivity characteristics of the underlying material, e.g., silicon.

In the present invention space charge inducing ions are divided into two categories, i.e., ions of electropositive elements and ions of electronegative elements, which are ionizable in apparatus operable at reasonable temperatures, i.e., less than about 300° C. for Penning type ion sources. However, for other source types, e.g., contact ionizers, appropriately higher temperatures may be used. Examples of the electropositive elements are alkaline earth metals, such as barium and strontium, and the alkali metal ions enumerated above, while examples of the electronegative elements are the halogens, such as iodine, bromine, chlorine and fluorine.

The insulating layer, while preferably the oxide of a semiconductor material such as silicon or germanium,

may be any insulation over or adjacent to a material, semiconductor or metal, the electrical characteristics of which it is desired to alter or control.

In accordance with the principal object of the present invention devices are formed having an insulating layer over a substrate body in which controlled or altered electrical characteristics of the substrate are affected by ions injected into the insulator of the space charge inducing ions.

Another object of the present invention is to provide a device which has selectively altered electrical characteristics in that portion of substrate material adjacent to a surface insulator.

A further object of the present invention is to provide a semiconductor device having a surface insulation layer bombarded with ions in order to induce a change in the electrical characteristics of an underlying semiconductor body.

These and other objects of the present invention will become more apparent from the following detailed description of various embodiments of the present invention taken together with the drawings, hereby made a part thereof, in which:

FIG. 1 is a sectional representation of a device utilizing the method and composition of the present invention;

FIG. 2 is a pictorial representation of a portion of FIG. 1 showing the space charge generated by the method of the present invention;

FIG. 3 is a graph showing the characteristics of an unbombarded field effect transistor; and

FIGS. 4 and 5 are graphs showing the characteristics of field effect transistor structures fabricated in accordance with the present invention.

The present invention will be described with respect to an insulated gate field effect transistor structure, the characteristics and operation of which are well known (see "The Feld Effect Transistor—A Review," J.T. Wallmark, R.C.A. Review 24: 641 (1963)) and which are schematically shown in FIG. 1. Referring now to FIG. 1, a transistor structure which may be fabricated in accordance with the method of the present invention is illustrated. The structure comprises a p-type semiconductor **20**, e.g., silicon, with a pair of spaced regions **21** and **22** having a conductivity type different than the bulk of semiconductor **20**. The spaced regions **21** and **22** may be formed by standard diffusion techniques well known in the art or by ion bombardment as described in the copending application of James O. McCaldin, entitled "Method of Treating Semiconductor Bodies," Ser. No. 308,617, filed Sept. 9, 1963, the disclosure of which is incorporated herein by reference. The spaced regions **21** and **22** are separated by a channel **24** of semiconductor material **20** having a length, i.e., the distance between the adjacent regions **21** and **22**, which may be of any desired magnitude.

A dielectric coating **25**, e.g., SiO_2 of the order of a hundred or thousand angstroms thick, is grown or deposited by standard techniques over the channel **24** and portions of the adjacent regions **21** and **22**. Appropriate thin metallic contacts **26**, **27** and **28** are provided to the dielectric coating and each area **21** and **22**, respectively.

The present invention is directed to a method and resulting product in which the space charge is controlled to an initial predetermined extent by generating a permanently induced space charge in the channel **24** of semiconductor **20**. This is accomplished by implanting in the dielectric layer **25** ions which induce a space charge in the underlying semiconductor. This arrangement is illustrated in FIG. 2. The dielectric layer **25** contains, as described hereinafter, implanted ions indicated in FIG. 2 as plus symbols. These ions, when implanted in a thin film of dielectric **25** such as silicon oxide, do not generally

become neutralized. Instead their presence in the dielectric **25** induces a space charge (—) in the channel **24** of the underlying semiconductor crystal **20**. In this manner a permanent n-type space charge is induced thereby facilitating electron flow between areas **21** and **22**. As a result a larger biasing voltage would be required to prevent electron flow. The opposite result may be attained by implanting negative ions in the dielectric **25** and thereby inducing a permanent positive space charge in the channel **24**. In such an arrangement a permanent built-in biasing effect is produced which would prevent electron flow unless an appropriately large driving signal was applied.

The process for obtaining the above described device is exemplified by the following steps. A silicon crystal having an initial uniform p-type resistivity of about 0.1 ohm-cm. and boron concentration of about 4×10^{17}cm.$^{-3}$ was exposed to an oxidation atmosphere of steam, at about 1200° C. for three hours, to produce an oxide layer having a thickness of about 12,000 A. Appropriate windows or opening are made in the oxide using conventional photo-resist techniques followed by phosphorous deposition at 1200° C. using a conventional carrier gas system. The phosphorous glass formed is removed by a 25 sec. etching step using an etch consisting of 15 parts HF, 10 parts HNO_3 and 300 parts water. The phosphorous is then diffused deeper into the silicon crystal by heating at about 1200° C. for 12½ hours. The oxide is then completely removed.

The surface of crystal **20** is then completely reoxidized by exposure to dry oxygen at about 1200° C. for three hours to grow a new oxide layer of about 4000 A. thickness on the entire crystal surface. This oxide is then bombarded with cesium ions of 10 kev. energy for 20 minutes with a beam about 3 ma. while maintaining the specimen at from 200 to about 500° C., preferably about 500° C.

Standard photoresist techniques are then utilized to selectively remove portions of the bombarded silicon oxide so that adjacent areas **21** and **22**, spaced about five mils apart in this example, are connected with an overlapping oxide layer **25** in which cesium ions have been injected. A metal contact **26** is then deposited on the surface of oxide layer **25** and appropriate electrical connections made with the source and drain.

This process was followed in the following examples for the specific conditions outlined.

EXAMPLE I

A single crystal silicon sample with 110 orientation having a p-type bulk dopant concentration of about 4×10^{17}cm.$^{-3}$ boron was treated by the above described method until completion of the reoxidizing step. The specimen was heated to and maintained at about 500° C. and bombarded with cesium ions of 10 kev. energy for 20 minutes. The ion beam current average was about 2.9 ma. Standard photoresist techniques were utilized to selectively remove portions of the oxide so that over the channel **24** the bombarded oxide remained as shown in FIG. 2. In this manner a field effect transistor structure consisting of two spaced n-type regions **21** and **22** separated by a p-type region having a channel length of about 5 mils was fabricated. The bombarded oxide coating also covered adjacent portions of the n-type regions. Electrical contacts were applied to the n-type regions, by methods well known in the art, and an aluminum metal gate contact was applied by standard procedures to the oxide surface between the two n-type regions.

EXAMPLE II

The procedure of Example I was repeated for a specimen having an initial p-type bulk dopant concentration of about 4×10^{17} cm.$^{-3}$, except that the reoxidizing step was performed for two hours at 1197° C. to obtain an oxide coating 2700 A. thick. The oxide surface was bombarded with cesium ions while the specimen was maintained at 460° C. The ion energy was 10 kev., the bombardment time 30 minutes and the average beam current about 1.7 ma. The remaining steps were the same as Example I.

EXAMPLE III

The procedure of Example I was repeated for a specimen having the same characteristics except that the oxide thickness after the reoxidizing step was 900 A. thick, and the bombarding time with cesium was 25 minutes with an average beam current of about 2 ma.

EXAMPLE IV

The procedure of Example I was repeated for a specimen having the same characteristics except that the channel length was 10 mils, the oxide thickness after the reoxidizing step was about 1000 A. and sodium ion bombardment was used. The specimen was maintained at 400° C. while the surface was bombarded with 9 kev. sodium ions for 10 minutes where the average beam current was about 4×10^{-7} amps.

Each specimen described in the above examples of the process of the present invention had electrical characteristics significantly different than those of the same structure but without ion injection. Thus, a sample was prepared by the above procedures except that no ion bombardment of the oxide was undertaken. The electrical characteristics of such a device are shown in FIG. 3. The voltage-current relationship shown is between the source and drain while the curves **30**, **31** and **32** shown the change from zero gate voltage for applied gate voltages of +22.5, +45 and +67.5 volts, respectively. It is clear that for zero gate voltage there is no conductance for the range of 0 to 20 volts.

The structures made in accordance with the process of the present invention, however, show significantly changed voltage-current-gate voltage relationship. For example, FIG. 4 shows the characteristics of the device described in Example II above. It is apparent from FIG. 4 that with zero gate voltage, curve **34**, that significant conductance is present at voltage values greater than about 10 volts. The effect of various positive and negative gate voltage is also shown. Thus, curves **35**, **36** and **37** show the increased conductance resulting from applied gate positive polarity voltages of 5, 10 and 15 volts, respectively. Curves **38**, **39** and **40** show the decreased conductance resulting from applied gate negative polarity voltage of 5, 10 and 15 volts, respectively. A comparison of FIGS. 3 and 4 establishes that the introduction of cesium ions into the oxide layer of a field effect transistor can permanently increase channel conductance.

FIG. 5 shows the characteristics of the device described in Example IV above. It is apparent from FIG. 5 that sodium ions introduced into the oxide layer also materially change the electrical characteristics. Thus, curve **41**, **42** and **43** are for zero gate voltage, positive 50 volts, and negative 50 volts, respectively. It is also apparent from the above that the effect on the electrical characteristics of the underlying semiconductor is a function of the bombardment time, beam current, oxide thickness and channel length, since the device of FIG. 5 (Example IV) had twice the initial channel length, a significantly reduced bombardment time and beam current, but a reduced oxide thickness. However, since none of these parameters are critical to device operability, selective variations may be made to obtain the desired characteristics. As is well-known, however, sodium is more mobile in SiO_2 type materials than larger ions like cesium. Therefore, diffusion of the sodium is more likely with consequent modification of the electrical characteristics.

While the above examples are described with respect to silicon, other semiconductor materials may be utilized as is well-known in the art. Further, either negative or positive ions may be introduced in the semiconductor material which may be of any preselected conductivity type. In addition, the insulating surface layer need not be an oxide nor an oxide of the underlying semiconductor

since other insulating oxides (including metal oxides), ceramics and glasses or other dielectrics may be used.

The process of the present invention has been described as particularly adapted for use in modifying the electrical characteristics of a field effect transistor. However, other applications include hot electron devices employing an oxide layer as an insulator between two other layers, e.g., a pair of metal layers or metal layer and a vacuum layer, in a sandwich construction. In such a device the electrostatic potential across the sandwich is an important parameter which may be controlled and modified by introducing charges by the process of the present invention.

Although particular embodiments of the present invention have been described herein, various modifications may be made without departing from the spirit and scope of the invention.

We claim:

1. A product comprising a substrate and a dielectric layer on the surface of said substrate, said dielectric layer

containing a preselected concentration of space charge inducing ions, said concentration being sufficient to induce a space charge in said material.

2. The product of claim 1 wherein said ion is at least one selected from the class consisting of Na, K, Rb and Cs.

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U.S. Cl. X.R.

117—201, 223, 225; 148—33.3, 33.4; 161—412; 317—235