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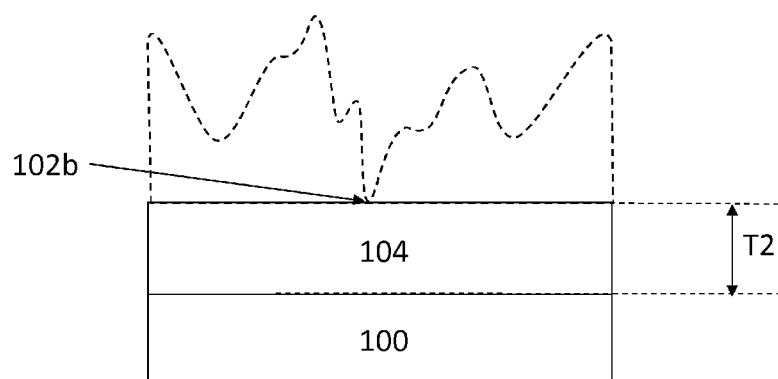


FIG.3

(57) Abstract: The present invention discloses a method for providing a tungsten layer on a substrate surface (101) and thereafter covering the as-formed tungsten layer (103) with a planarized material (107) having an etch rate similar to the etch rate of tungsten (103); and thereafter etching the planarized material (107) and top part of the as-formed tungsten layer (103) until all the planarized material (107) is removed.



METHOD FOR PROVIDING A TUNGSTEN LAYER**Field of the disclosure**

[001] The present disclosure relates to a method for providing a tungsten layer. The present disclosure relates to a method for etching an as-formed tungsten layer.

State of the art

[002] Over the past decades, aggressive and continuous transistor scaling according to Moore's law has provided ever increasing device performance and density. For advanced (sub-)5nm nodes, to keep the growth pace, several options can be considered in terms of material choices, device architectures and circuits design.

[003] The use of tungsten (W) layers is an integral part of currently available semiconductor integration processes. Because of the low resistivity, thermal stability of tungsten and its behaviour with regard to diffusion mechanisms (for example compared to copper), tungsten is standardly used for example as fill-metal of replacement gate in the gate stack of semiconductor devices with a gate-last scheme or as part of the top gate electrode in transistors with gate-first scheme. Tungsten is also often used as bottom or top electrode for different semiconductor device applications such as logic and memory. Furthermore tungsten is also often used as fill-material for contacts in back-end-of-line (BEOL).

[004] One of the challenges however for tungsten layer deposition concerns the control of the surface roughness of tungsten when (partially) etching-back this material, for example in a gate-first module.

[005] Tungsten (W) is standardly used as a gate stack fill-metal but because of its fairly large W grains size, its partial etch-back by a wet [e.g. ammonium hydroxide-hydrogen peroxide mixture (APM)] or dry [e.g., a F-based (such as SF₆ or NF₃) plasma] process results in a W layer with a quite rough surface, worst if a thicker amount of W material needs to be etched-back. If implementing such processes in the gate-first module of a vertical device integration flow, this will bring issues in terms of the control of the gate electrode thickness, also impacting the subsequent isolation (its thickness and roughness control) between the gate and top electrodes.

[006] US application US2012/0164832 discloses a method for depositing a tungsten film having a low resistivity, low roughness and high reflectivity. The method comprises depositing a layer of tungsten having a thickness T1 by using chemical vapour deposition (CVD) and thereafter removing top portion of the deposited tungsten layer to form a tungsten bulk layer having

thickness T_d , T_d being less than T_1 . The top portion is between 5% and 25% of the thickness T_1 . For example a remote NF_3 plasma may be used to remove the top portion.

[007] A disadvantage of the disclosed method is that the reactivity of the NF_3 plasma cannot be controlled towards different layers and as a consequence the method is only applicable for the deposition of tungsten layers on blanket wafers and is not applicable on patterned structures. Moreover the etch process as disclosed in US2012/0164832 needs to be controlled such that the bottom of the space in between the grains is not touched and as a consequence roughness is not increased again. Therefore the method is limited to the removal of only a top portion in between 5% and 25% of the as-deposited W thickness T_1 , which limits the method to a limited amount of thicknesses.

[008] There is a need for new methods of providing a tungsten layer in a controlled way wherein a tungsten layer of any desired thickness may be formed or more specifically an as-formed tungsten layer may be etched to any desired thickness. Furthermore there is a need for a method of providing a tungsten layer which is applicable for a wide range of applications not only on blanket wafers but also including methods for providing a tungsten layer on a patterned structure.

Summary of the disclosure

[009] It is an object of particular embodiments of the present invention to provide a method for providing a tungsten layer having a desired thickness and having a low roughness surface profile.

[0010] It is an object of particular embodiments of the present invention to etch back an initial tungsten layer to a final tungsten layer such that the final roughness of the final tungsten layer is lower than the initial roughness of the initial tungsten layer.

[0011] It is an object of particular embodiments of the present invention to etch back an initial tungsten layer to a final tungsten layer such that the thickness of the final tungsten layer may be more than 25% lower than the thickness of the initial tungsten layer.

[0012] The above objectives are accomplished by the method according to embodiments of the present invention.

[0013] Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from the dependent claims may be combined with features of the independent claims and with features of other independent claims as appropriate and not merely as explicitly set out in the claims.

[0014] A first aspect relates to a method for providing a tungsten layer, the method comprising providing a substrate (100) having a substrate surface (101); providing a tungsten layer (103) on the substrate surface (101); covering the tungsten layer (103) with a planarized material (107) having an etch rate similar to the etch rate of tungsten (103); etching the planarized material (107) and top part of the tungsten layer (103) until all the planarized material (107) is removed.

[0015] According to embodiments of the invention the etch rate of the planarized material (107) differs not more than 25% from the etch rate of tungsten (103). More preferably the etch rate of the planarized material is not more than 10%, even more preferably not more than 5% from the etch rate of tungsten.

[0016] According to embodiments of the invention the etch rate of the planarized material (107) is equal to the etch rate of tungsten (103).

[0017] According to embodiments of the invention the planarized material (107) comprises a self planarizing material. The self-planarizing material may comprise a spin-coating material such as for example SOC or SOG.

[0018] According to embodiments of the invention removing the planarized material (107) and top part of the tungsten layer (103) comprises etching with an F-based etch chemistry.

[0019] According to embodiments of the invention etching the planarized material (107) and top part of the tungsten layer (103) further comprises after etching removing etch residues.

[0020] According to embodiments of the invention the method further comprising before etching the planarized material (107) and top part of the tungsten layer (103): removing top part of the planarized material (107) without removing the tungsten layer (103).

[0021] According to embodiments of the invention removing top part of the planarized material (107) comprises removing the planarized material (107) until reaching the tungsten layer (103) top surface.

[0022] According to embodiments of the invention removing top part of the planarized material (107) comprises etching with a O₂-plasma based chemistry.

[0023] According to embodiments of the invention the tungsten layer (107) has an initial surface roughness before etching the planarized material (107) and top part of the tungsten layer (103) and wherein the tungsten layer (107) has a final surface roughness after etching the planarized material (107) wherein the final surface roughness is lower than the initial surface roughness.

[0024] According to embodiments of the invention the final surface roughness is at least 30% lower than the initial surface roughness.

[0025] According to embodiments of the invention the tungsten layer (103) has an initial thickness and wherein removing top part of the tungsten layer (103) comprises removing more than 50% of the initial thickness.

[0026] According to embodiments of the invention the substrate comprises a blanket wafer or wherein the substrate comprises a patterned structure. The patterned structure may comprise a vertical nanostructure.

Brief description of the drawings

[0027] Figure 1 to 3 schematically show different steps for forming a tungsten layer according to embodiments of the present invention, wherein the substrate is not patterned.

[0028] Figure 4A-4C schematically shows providing a tungsten layer according to embodiments of the present invention.

[0029] Figure 5 to 7 schematically show different steps for forming a tungsten layer according to embodiments of the present invention, wherein the substrate comprises a patterned structure.

[0030] Figure 8 schematically shows different steps for providing a tungsten layer according to embodiments of the present invention.

[0031] Figure 9 shows a scanning electron microscopy (SEM) image after CMP of an as-deposited tungsten layer according to embodiments of the present invention.

[0032] Figure 10 shows a scanning electron microscopy (SEM) image after removing top portion of the tungsten layer after bulk deposition of the tungsten layer according to embodiments of the present invention.

[0033] Figure 11 shows a scanning electron microscopy (SEM) image after performing the method for forming a tungsten layer according to embodiments of the present invention.

[0034] All the figures are schematic, not necessarily to scale, and generally only show parts which are necessary to elucidate the embodiments of the present invention, wherein other parts may be omitted or merely suggested.

[0035] Any reference signs in the claims shall not be construed as limiting the scope.

[0036] In the different drawings, the same reference signs refer to the same or analogous elements.

Detailed description of the disclosure

[0037] The disclosure will be further elucidated by means of the following detailed description of several embodiments of the disclosure and the appended figures.

[0038] In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the disclosure and how it may be practiced in particular embodiments. However, it will be understood that the present disclosure may be practiced without these specific details. In other instances, well-known methods, procedures and techniques have not been described in detail, so as not to obscure the present disclosure. While the present disclosure will be described with respect to particular embodiments and with reference to certain drawings, the disclosure is not limited hereto. The drawings included and described herein are schematic and are not limiting the scope of the disclosure. It is also noted that in the drawings, the size of some elements may be exaggerated and, therefore, not drawn to scale for illustrative purposes.

[0039] The term “comprising”, used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps. It needs to be interpreted as specifying the presence of the stated features, integers, steps or components as referred to, but does not preclude the presence or addition of one or more other features, integers, steps or components, or groups thereof. Thus, the scope of the expression “a device comprising means A and B” should not be limited to devices consisting only of components A and B.

[0040] “Horizontal” refers to a general direction along or parallel to a primary surface of a substrate, and “vertical” is a direction generally orthogonal thereto. “Horizontal” and “vertical” are used as generally perpendicular directions relative to each other independent of the orientation of the substrate in the three-dimensional space.

[0041] In the following, certain embodiments will be described with reference to a silicon (Si) substrate, but it should be understood that they apply equally well to other semiconductor substrates. In embodiments, the “substrate” may include a semiconductor substrate such as e.g. a silicon, a germanium (Ge), or a silicon germanium (SiGe) substrate, a gallium arsenide (GaAs), a gallium arsenide phosphide (GaAsP), an indium phosphide (InP),. The “substrate” may include for example, an insulating layer such as a SiO₂ or a Si₃N₄ layer in addition to a semiconductor substrate portion. Thus, the term substrate also includes silicon-on-glass, silicon-on-sapphire substrates. The term “substrate” is thus used to define generally the elements for layers that underlie a layer or portions of interest. Also, the “substrate” may be any other base on which a layer is formed, for example a glass or metal layer. Accordingly a substrate may be a wafer such as a blanket wafer or may be a layer applied to another base material, e.g. an epitaxial layer grown onto a lower layer.

[0042] Figure 1 to 3 shows the process according to certain embodiments of the invention. The process or manufacturing method starts with providing a substrate 100, the substrate 100 having a substrate surface 101 as shown in FIG 1. On the substrate surface 101 a tungsten layer 103 is provided.

[0043] According to embodiments the substrate may be a blanket substrate (which means it does not comprise any patterned structures, otherwise said the substrate is unpatterned) or the substrate may comprise a patterned structure. A blanket substrate may also be referred to as a blanket wafer, which means the wafer or substrate comprise blanket layers or films over the entire substrate. FIG 1 to 3 refer to embodiments wherein the substrate is unpatterned. FIG 5 to 7 refer to embodiments wherein the substrate comprises a patterned structure.

[0044] Providing the tungsten layer 103 on the substrate surface 101 may be done according to different embodiments which will now be described in more detail.

[0045] Whenever there is referred to the final tungsten layer, this refers to the final layer which is formed after performing all the process steps according to embodiments of the invention.

[0046] Whenever there is referred to the as-deposited or as-formed or initial tungsten or initially formed layer, this refers to the tungsten layer before performing the step of covering the tungsten layer with a planarized material.

[0047] According to embodiments providing the tungsten layer 103 (i.e. the initial tungsten layer) may involve different process steps.

[0048] According to embodiments providing the tungsten layer may involve bulk deposition of a tungsten layer 103a (as shown in FIG. 4A) using techniques known for a person skilled in the art such as chemical vapor deposition (CVD), physical vapor deposition (PVD) or atomic layer deposition (ALD) or a combination of these techniques.

[0049] According to embodiments after bulk deposition of the tungsten layer 103a top portion of the tungsten layer may be removed (FIG. 4C) thereby forming a tungsten layer 103c having a smaller thickness than the bulk deposited tungsten layer 103a. Removing of a top portion of the tungsten layer may involve etching back the bulk deposited tungsten layer 103a. The etch step may comprise for example etching with a fluorine-based plasma such as for example SF_6 , NF_3 . SF_6 has a faster etch-rate than NF_3 which may be advantageous if a larger top portion of the tungsten layer needs to be removed.

[0050] Optionally before etching back top portion of the tungsten layer a chemical-mechanical polishing (CMP) step (FIG.4B) may be performed as a first planarizing step of the bulk deposited tungsten layer 103a. As such a planarized tungsten layer 103b is formed. Although the profile of

the tungsten layer after CMP may be reasonable (i.e. having a low roughness), further etch-back of the tungsten layer is needed especially for a substrate comprising a patterned structure.

[0051] As tungsten has a fairly large grain size (grain size can be even more than 100nm), after providing the tungsten layer, the as-formed tungsten layer surface 102 comprises a grain structure profile. The grain structure profile comprises peaks and valleys, wherein the peaks comprise a highest peak 102a defining the largest thickness T_1 of the as-formed tungsten layer 103 and a lowest peak 102b defining the smallest thickness T_2 of the as-formed tungsten layer 103. Thickness of the tungsten layer is defined starting from the substrate surface 101 as shown schematically in FIG.1. The smallest thickness T_2 of the as-formed tungsten layer 103 defines the targeted thickness for the final tungsten layer using the method according to embodiments of the invention. The thickness of the as-formed tungsten layer which is also referred to as the initial thickness T_a may be defined by the average thickness of the surface profile as shown in FIG. 1.

[0052] It is an object of the invention to form a (final) tungsten layer which has a roughness (also known as surface roughness) which is smaller than the roughness of the initial tungsten layer. The roughness of a layer, more specifically of a tungsten layer, may be measured by defining the profile roughness parameters. This may be done using for example atomic force microscopy (AFM) or other surface metrology techniques known for a person skilled in the art. R_a and RMS may for example be defined. R_a is the arithmetic average of the absolute values of the profile height deviations from the mean line. It measures thus the average value of a set of individual measurements of the surface profile peaks and valleys. RMS is the root mean square average of the profile height deviations from the mean line. It measures thus the root mean square average value of a set of individual measurements of the surface profile peaks and valleys. Other possible metrology techniques which may be used to determine the roughness profile of the tungsten layer are secondary electron microscopy (SEM) or transmission electron microscopy (TEM) which both have the advantage that the roughness profile or roughness difference between the as-deposited tungsten layer and the final tungsten layer after performing the method according to embodiments of the present invention may be determined quickly by just scanning the surface profile without the need for determining the RMS-values.

[0053] The decrease in roughness for the (final) tungsten layer after performing the method according to embodiments of the present invention may be already visible with standard microscopy techniques such as for example SEM/TEM. With the method for providing a tungsten layer according to embodiments of the present invention the RMS values of the tungsten layer may be decreased from an RMS value of the as-deposited tungsten layer being in the high 2

digits number (at least more than 10nm, even more than 20nm) to a (final) RMS value of the final tungsten layer which is an order of magnitude lower compared to the RMS value of the as-deposited tungsten layer. The RMS value of the final tungsten layer may become below 20nm, even below 10nm or even below 1nm.

[0054] It is a further object of the invention to form a tungsten layer having any desired final thickness. The final thickness is defined by T_2 of the as-formed tungsten layer, the smallest thickness (i.e. of the smallest valley). The final thickness T_2 is thus smaller than the thickness T_a of the as-formed tungsten layer. The desired final thickness may depend on the application (for example logic, memory)

[0055] After providing the tungsten layer 103, the as-formed tungsten layer 103 is covered with a planarized material 107 having a similar etch-rate as the etch-rate of tungsten as shown in FIG.2. With similar etch rate is meant that the etch rate of the planarized material using the same etch chemistry is differing not more than 25% from the etch rate of tungsten, even more preferably not more than 10%, even more preferably not more than 5%. Otherwise said the etch rate of the planarized material may be up to 25% higher or lower than the etch rate of tungsten. Even more preferably the etch rate of the planarized material may be up to 10% higher or lower than the etch rate of tungsten. Even more preferably the etch rate of the planarized material may be up to 5% higher or lower than the etch rate of tungsten. Preferably the etch rate of the planarized material is equal or at most 10% lower than the etch rate of tungsten.

[0056] The ideal situation is to provide a planarized material 107 which does not differ in etch rate from tungsten, otherwise said the etch rate of the planarized material 107 and the etch rate of tungsten (for equivalent etch chemistry) is substantially the same. It is an advantage of having the same etch rate that the roughness of the final etch layer 104 can be further reduced compared to etch rates which differ slightly. The higher the etch rate difference between the two materials (i.e the planarized material 107 and tungsten 103), the higher the roughness of the etched final tungsten layer will become. Therefore the etch rate of the planarized material 107 has to be chosen carefully and needs to be within an margin difference of at most 25% compared to the etch rate of tungsten.

[0057] For example for embodiments wherein the planarized material comprises a spin-coating material such as SOC, the following exemplary experimental etch rates were obtained. The experiments were first performed on blanket wafers and thereafter further optimization was done on patterned structures. For tungsten an etch rate of 122nm/min was obtained using SOC chemistry. The SOC layer is etched by looking at the EP trace and in 60 seconds (EP+EO) 100nm of SOC was consumed.

[0058] A planarized material 107 is a material for which the top surface is substantially planar and thus without a surface profile. The material may be planarized by deposition. For example atomic layer deposition (ALD) is known to be able to deposit layers with high uniformity. The material may also be planarized by first depositing the material and thereafter performing a planarizing step such as for example chemical mechanical polishing (CMP).

[0059] According to embodiments the planarized material 107 may be a self-planarizing material. In this case the planarizing step of the material is not needed, but by deposition a planarized material is formed. An example of such self-planarizing material 107 is a spin-coating material such as for example spin-on-glass (SOG) or spin-on-carbon (SOC).

[0060] The thickness of the planarized material 107 may be selected based on the techniques available. For example a spin-coating material can be formed with a thickness of about 30 nm. By repeating the spin-coating step a planarized material having a larger thickness may be provided.

[0061] By covering the tungsten layer 103 with the planarized material 107 all the peaks and valleys are covered and filled with the planarized material 107 as is shown in FIG. 2.

[0062] After covering the tungsten layer 103 with the planarized material 107 a removal step is performed wherein both the planarized material 107 and top part of the tungsten layer 103 are removed until all the planarized material 107 is removed. As shown in FIG. 3, a final tungsten layer 104 is formed which has a substantial planar surface profile. This means the roughness of the final tungsten layer 104 is smaller than the roughness of the initially formed tungsten layer 103. More specifically the roughness of the final tungsten layer 104 is at least 30%, even at least 50%, even at least 60% smaller than the roughness of the initially formed tungsten layer 103. Moreover the thickness of the final tungsten layer 104 is smaller than the thickness of the initially formed tungsten layer 103. More specifically more than 5% of the initial thickness T_a , even more than 25% of the initial thickness T_a may be removed, even more than 50% of the initial thickness T_a may be removed.

[0063] As the planarized material 107 is covering and filling the peaks and valleys of the as-formed tungsten layer 103, the planarized material 107 will typically be removed until the deepest valley 102b of the surface profile of the tungsten layer 103 is reached. In FIG. 3 this is schematically shown by also showing in a striped line the initial surface profile of the tungsten layer 103 which was present before the step of removing top part of the tungsten layer 103 and the planarized material 107, but which is not present anymore after the step of removing top part of the tungsten layer 103 and the planarized material 107.

[0064] According to embodiments, removing top part of the tungsten layer 103 and the material 107 may comprise one etching step, more specifically etching both materials (together) with an F-based etch chemistry such as SF_6 , NF_3 . The specific etch parameters such as for example the etching time may be optimized depending on the amount of tungsten and of the planarized material that needs to be removed.

[0065] Removing top part of the tungsten layer 103 and the planarized material 107 may further comprise a cleaning step or stripping to remove any residues or by-products left from the etching step. Also residues of the planarized material 107 which may be left can be removed so that after the step of removing top part of the tungsten layer 103 and the planarized material 107 all the planarized material 107 is removed and only tungsten 103 remains present.

[0066] It is an advantage of the method according to embodiments of the invention that a tungsten layer may be provided having a smooth substrate surface, or at least a smoother substrate surface even after etching back part of the tungsten layer.

[0067] It is an advantage of the method according to embodiments of the invention that a tungsten layer may be provided having a RSM value close to zero (in the order of few angstroms).

[0068] It is an advantage of the method according to embodiments of the invention that a tungsten layer may be provided having any desired thickness. More specifically also very thin tungsten layers may be provided, i.e. having a thickness below 5 nm (using ALD). Depending on the desired resistivity of the tungsten layer, one can provide larger thicknesses.

[0069] It is an advantage of the method according to embodiments of the invention that any desired thickness of an initial tungsten layer may be removed without increasing the roughness value of the final tungsten layer after removal of the desired thickness.

[0070] It is an advantage of the method according to embodiments of the invention that any desired thickness of an initial tungsten layer may be removed and the roughness value of the final tungsten layer after removal of the desired thickness has decreased compared to the roughness value of the as-deposited tungsten layer.

[0071] According to embodiments of the invention before removing both the planarized material 107 and top part of the tungsten layer 103 optionally a top part of the provided planarized material 107 may be etched back, without affecting the tungsten layer 103. This has the advantage that rather thick layers may be provided for the planarized material 107 and part of the planarized material 107 may be removed using a faster removal method. The planarized material is thus etched back until the point where the planarized material is essentially filling the valleys in between the peaks of the tungsten layer 103. According to embodiments part of the planarized material 107 is removed using an O_2 -based plasma. The etch parameters for this

removal step should be chosen such that the tungsten layer 103 is not removed. The specific etch parameters such as for example the etching time may be optimized depending on the thickness of the planarized material and the amount of material that needs to be removed.

[0072] According to embodiments the substrate may comprise a patterned structure. FIG 5 to 7 refer to embodiments for a method of providing a tungsten layer wherein the substrate comprises a patterned structure. The description of the different steps for the method of providing a tungsten layer according to embodiments of the present invention are analogue to the description as given for FIG. 1 to 3 (blanket wafer) except that the substrate comprise a patterned structure such as for example vertical nanostructures 105. The tungsten layer 103, 104 is thus formed in between the vertical nanostructures 105.

[0073] Experimental Results.

[0074] A possible application of a method for providing a tungsten layer according to embodiments of the present invention may be tungsten deposition as a metal gate for vertical field effect transistor devices (VFETs). VFETs are devices in which the current is flowing in a direction perpendicular to the substrate surface. A VFET comprises thus a vertical pillar extending outwardly from a horizontal substrate surface, the vertical pillar comprising a channel region and the VFET further more comprising a source region at one side of the channel region (for example at a bottom portion of the pillar) and a drain region at the opposite side of the channel region (for example at a top portion of the pillar). VFETs have the advantage that the channel length is not defined by lithography, but rather by the methods used for manufacturing

[0075] According to embodiments of the present invention include the substrate comprises a base substrate and a vertical pillar extending away from the substrate surface.

[0076] An etch challenge faced in integration concerns the control of the surface roughness of tungsten (W) when (partially) etching-back this material, namely within the gate-first module. W is standardly used as the gate stack fill-metal but because of its fairly large W grains size, its partial etch-back by a wet [e.g. ammonium hydroxide-hydrogen peroxide mixture (APM)] or dry [e.g., a F-based (such as SF₆ or NF₃) plasma] process results in a W layer with a quite rough surface, worst if a thicker amount of W material needs to be etched-back. If implementing such processes in the gate-first module of a vertical flow, this will of course bring issues in terms of the control of the gate electrode thickness, also impacting the subsequent isolation (its thickness and roughness control) between the gate and top electrodes. To attenuate such issues and obtain a smoother W surface after metal etch-back, a method for providing a tungsten layer according to embodiments of the present invention is proposed which for example may comprise the following steps:

[0077] 1) after an optional W CMP (FIG. 8a), a first W etch-back step (done using a F-based plasma) leads to a rough W surface in-between pillars (FIG. 8b). The thinnest local thickness of the W layer obtained is the targeted final W thickness on the wafer.

[0078] 2) a spin-on-carbon (SOC) material is coated on the wafer. This material was chosen based on the fact that it has a similar etch-rate (ER) to that of W for the selected F-based chemistry.

[0079] 3) an O₂-based plasma is used to etch-back SOC until the point where SOC is essentially filling the valleys in-between the W peaks on the W layer which is present on the wafer, surrounding the NW pillars. The NW pillars are Si pillars comprising a gate stack liner, i.e. a gate dielectric layer (for example a high-k dielectric layer) and a gate metal layer for example TiN conformally formed on the Si pillar.

[0080] 4) W and SOC are etched-back simultaneously and with similar ER, resulting in a final W layer on the wafer with a much smoother surface as compared to that obtained after the simple dry-etch in step 1 (FIG. 8c).

[0081] From this point on, the rest of the process for gate electrode definition continues, namely with complete (dry-wet etch) removal of the effective work-function (EWF)-metal from the exposed, top part of the vertical NW pillars, followed by a 248nm lithography and etch steps to remove the gate metals from the areas on the wafer uncovered by resist, thus finishing the gate electrode formation module.

[0082] FIG. 9 to FIG. 11 show SEM images which were experimentally measured after different steps of the method for forming a tungsten layer. FIG. 9 shows the SEM profile after an initial (optional) CMP of the as-deposited tungsten layer as also shown schematically in FIG. 8a. The substrate comprises vertical pillars 105. The pitch size between the vertical pillars is about 300nm and the grain size 106 of the planarized tungsten is clearly visible. The grain size is about 150nm. FIG. 10 shows the SEM image after the first etch-back step of tungsten resulting a rough surface profile 102 as also shown schematically in FIG. 8b. FIG. 10 shows thus the initial tungsten layer 103. FIG. 11 shows the SEM image after performing the method for forming a tungsten layer, i.e. after simultaneous etch-back of the W and SOC layer. As can be visually seen the surface profile 102 of the final tungsten layer 104 has become substantially flat and the roughness is decreased drastically.

[0083] After performing the different steps of the method according to embodiments of the invention, further process steps may be performed. For example for gate electrode definition for VFET, such as complete (dry-wet etch) removal of the effective work-function (EWF)-metal from the exposed, top part of the vertical NW pillars, followed by a 248nm lithography and etch

steps to remove the gate metals from the areas on the wafer uncovered by resist, thus finishing the gate electrode formation module.

CLAIMS

1. A method for forming a tungsten layer, the method comprising:
 - providing a substrate (100) having a substrate surface (101);
 - providing a tungsten layer (103) on the substrate surface (101);
 - covering the tungsten layer (103) with a planarized material (107) having an etch rate similar to the etch rate of tungsten (103);
 - etching the planarized material (107) and top part of the tungsten layer (103) until all the planarized material (107) is removed.
2. Method for forming a tungsten layer according to claim 1 wherein the etch rate of the planarized material (107) differs not more than 25% from the etch rate of tungsten (103).
3. Method for forming a tungsten layer according to claim 2 wherein the etch rate of the planarized material (107) is equal to the etch rate of tungsten (103).
4. A method for forming a tungsten layer according to any of the preceding claims, the planarized material (107) comprising a self planarizing material.
5. A method for forming a tungsten layer according to any of the preceding claims, wherein the self-planarizing material comprises a spin-coating material.
6. Method for forming a tungsten layer according to any of the preceding claims wherein removing the planarized material (107) and top part of the tungsten layer (103) comprises etching with an F-based etch chemistry.
7. Method for forming a tungsten layer according to claim 6 wherein etching the planarized material (107) and top part of the tungsten layer (103) further comprises after etching removing etch residues.
8. A method for forming a tungsten layer according to any of the preceding claims, the method further comprising before etching the planarized material (107) and top part of the tungsten layer (103): removing top part of the planarized material (107) without removing the tungsten layer (103).

9. A method for forming a tungsten layer according to claim 8 wherein removing top part of the planarized material (107) comprises removing the planarized material (107) until reaching the tungsten layer (103) top surface.
10. A method for forming a tungsten layer according to claim 8 or 9 wherein removing top part of the planarized material (107) comprises etching with a O₂-plasma based chemistry.
11. A method for forming a tungsten layer according to any of the preceding claims wherein the tungsten layer (107) has an initial surface roughness before etching the planarized material (107) and top part of the tungsten layer (103) and wherein the tungsten layer (107) has a final surface roughness after etching the planarized material (107) wherein the final surface roughness is lower than the initial surface roughness.
12. A method for forming a tungsten layer according to claim 11 wherein the final surface roughness is at least 30% lower than the initial surface roughness.
13. A method for forming a tungsten layer according to any of preceding claims wherein the tungsten layer (103) has an initial thickness and wherein removing top part of the tungsten layer (103) comprises removing more than 50% of the initial thickness.
14. A method for forming a tungsten layer according to any of the preceding claims wherein the substrate comprises a blanket wafer or wherein the substrate comprises a patterned structure.
15. A method for forming a tungsten layer according to claim 14 wherein the patterned structure comprises a vertical nanostructure.

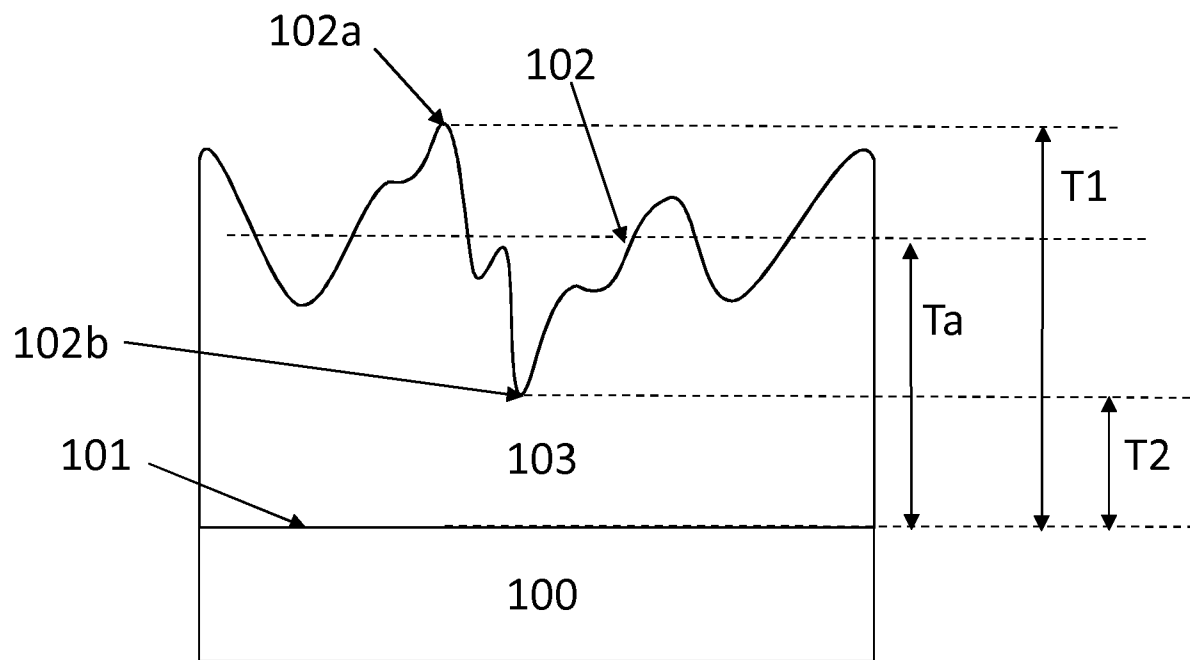


FIG.1

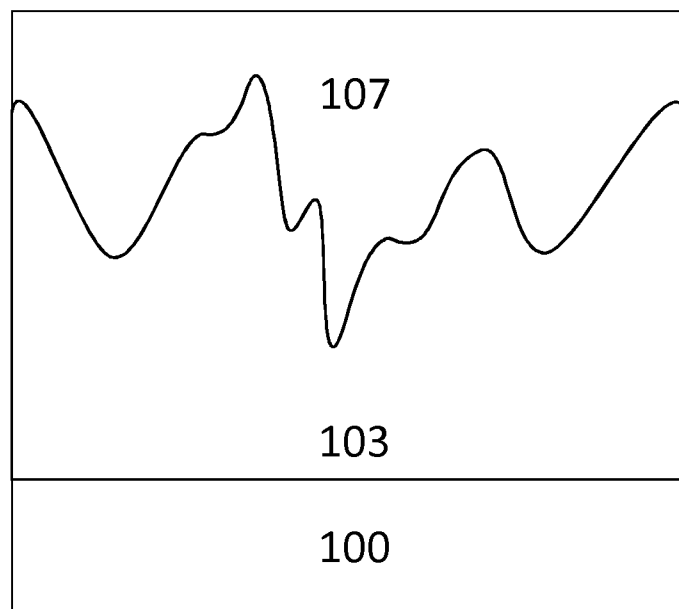


FIG.2

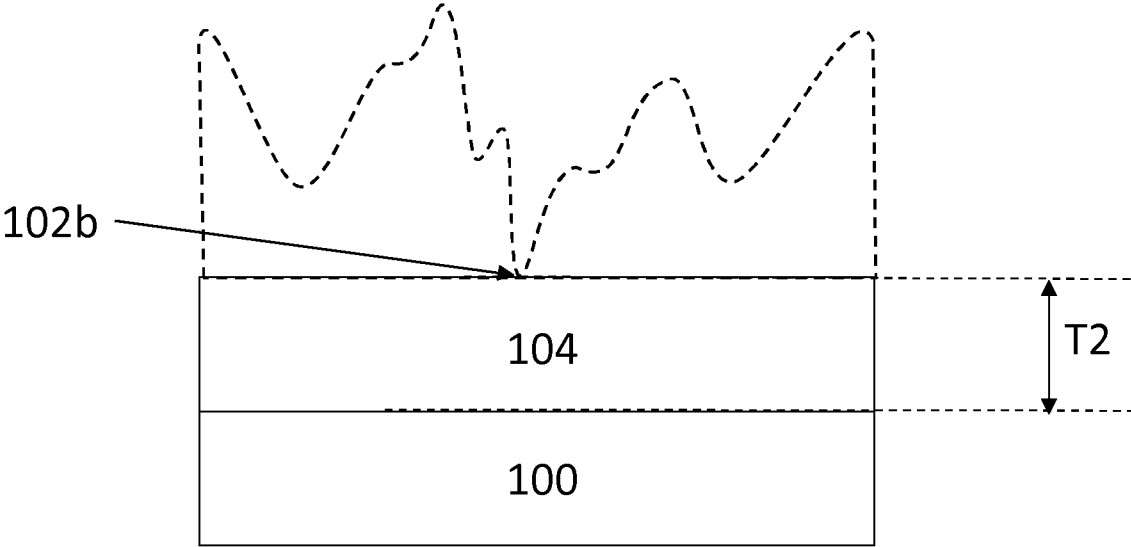


FIG.3

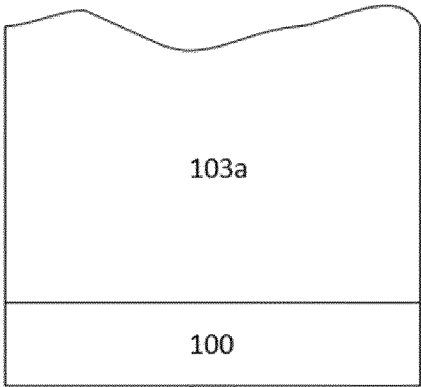


FIG.4A

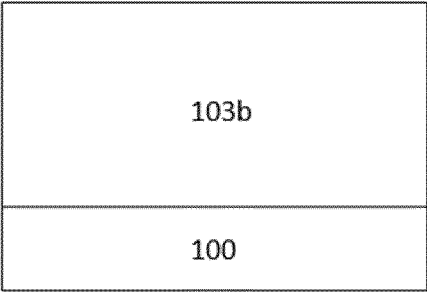


FIG.4B

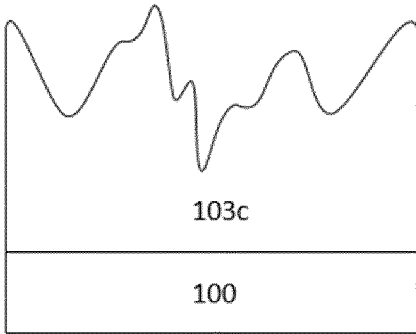


FIG.4C

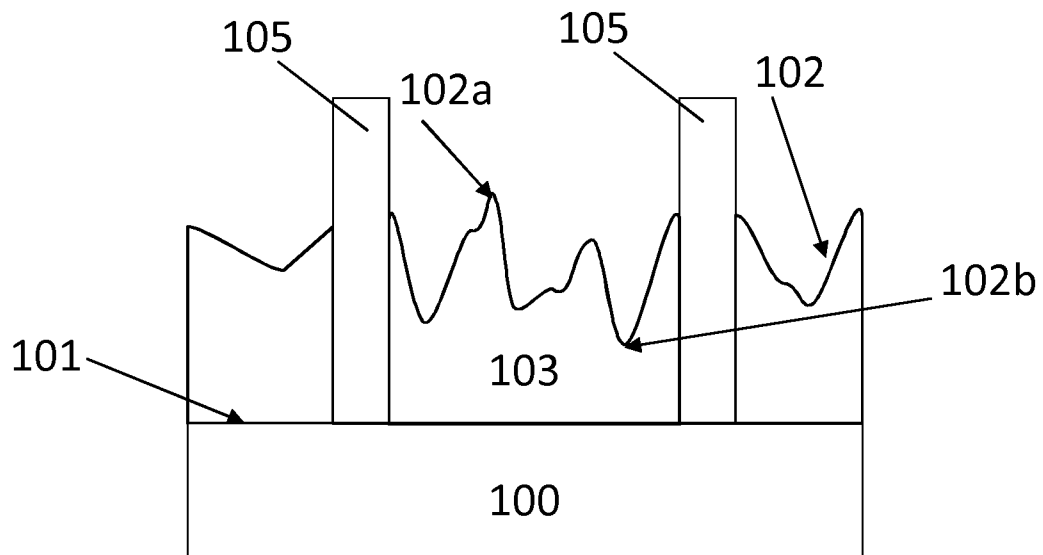


FIG.5

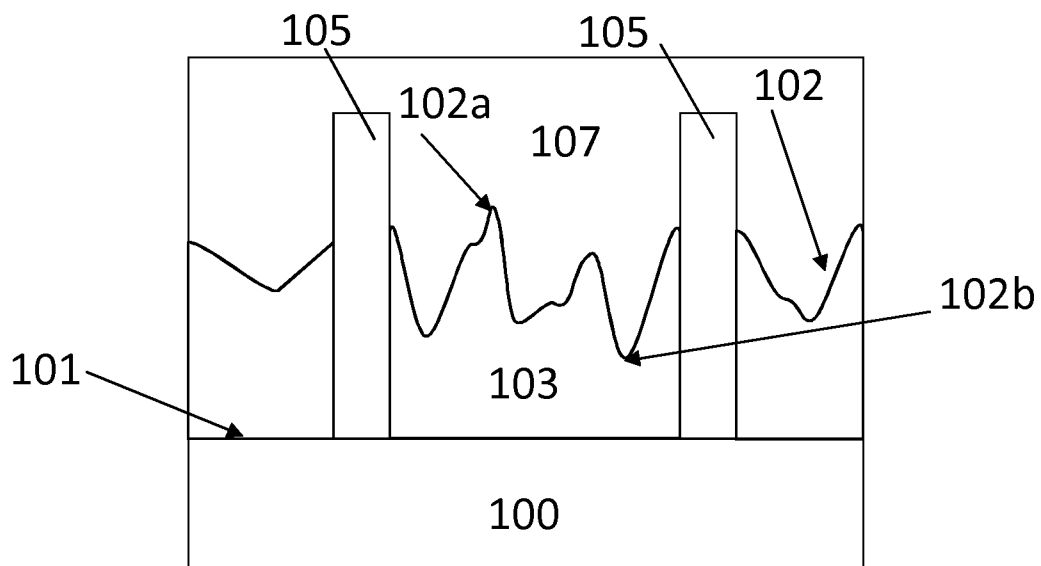


FIG.6

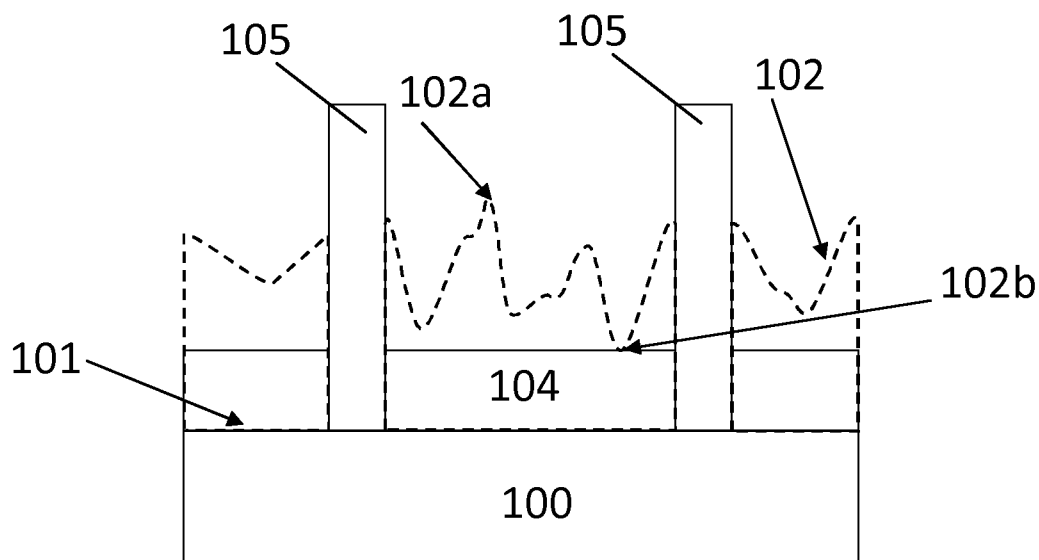


FIG. 7

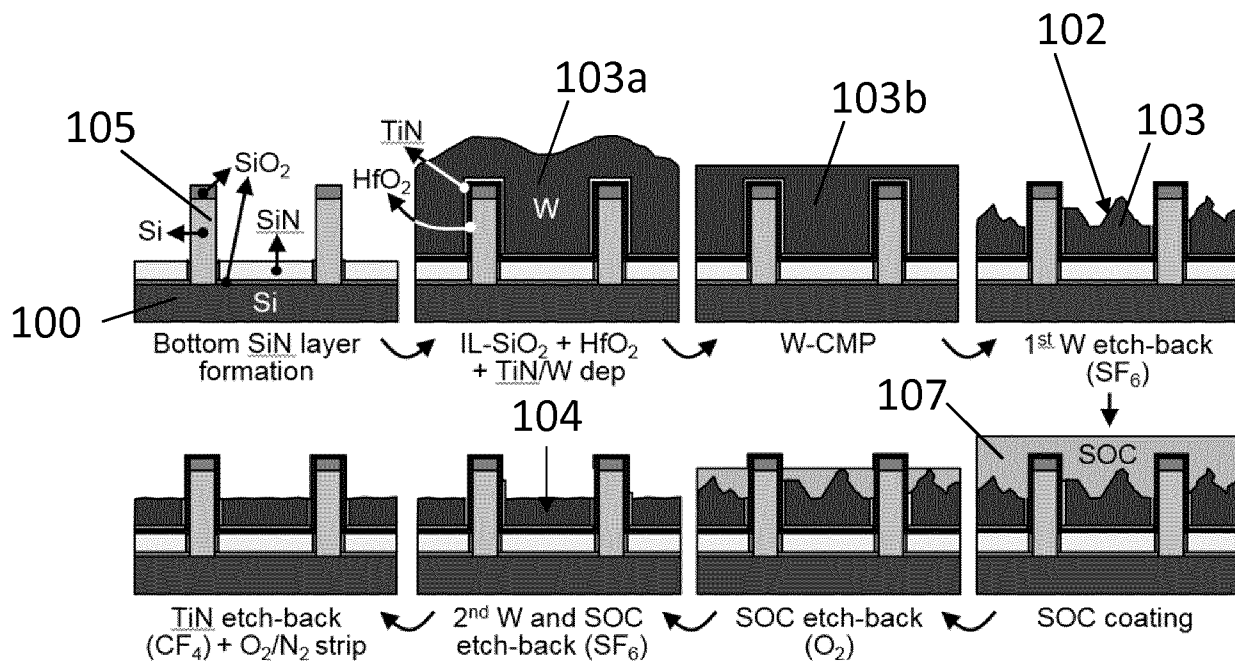


FIG. 8

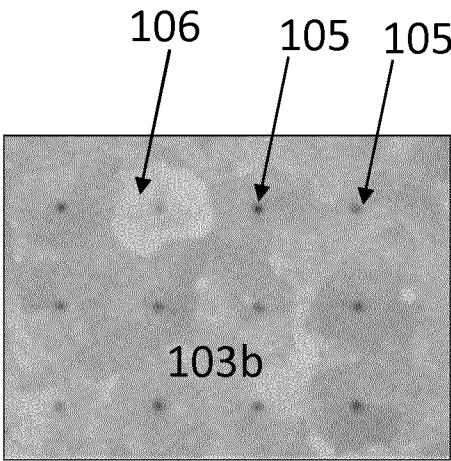


FIG.9

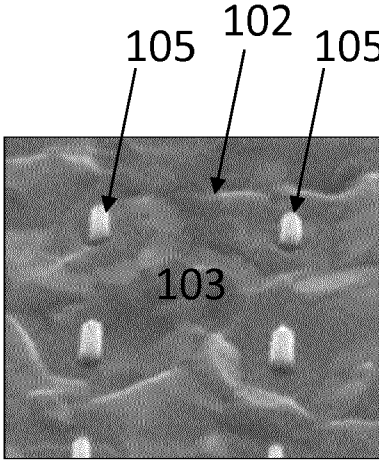


FIG.10

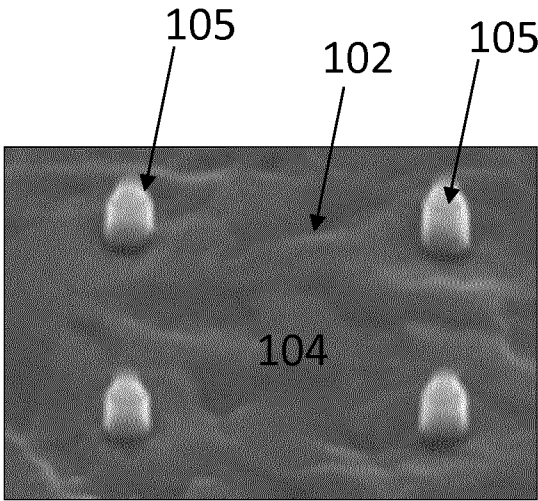


FIG.11

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2017/054490

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L21/321 H01L29/06
 ADD. H01L21/3213 H01L21/311

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	"GRAVURE IONIQUE REACTIVE DU TUNGSTENE POUR L'INTERCONNECTION", VIDE, LES COUCHES MINCES, SOCIETE FRANCAISE DU VIDE. PARIS, FR, vol. 44, no. 247, 1 May 1989 (1989-05-01), pages 297-309, XP000048737, ISSN: 0223-4335 pages 297-299; figures 1-4,6 -----	1-15
X	US 6 355 553 B1 (SHINOHARA KEIJI [JP]) 12 March 2002 (2002-03-12) column 2, line 58 - column 3, line 31 column 4, line 36 - column 5, line 64; figure 2 column 5, line 65 - column 6, line 49; figure 3 column 8, line 34 - column 9, line 36; figure 5 ----- -/--	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search

11 May 2017

Date of mailing of the international search report

19/05/2017

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Szarowski, Anne

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/054490

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	US 5 063 175 A (BROADBENT ELIOT K [US]) 5 November 1991 (1991-11-05) column 7, lines 47-60; figure 3c -----	1-15
A	JP H05 198817 A (SHARP KK) 6 August 1993 (1993-08-06) paragraphs [0027] - [0033]; figures 1,2 -----	15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2017/054490

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