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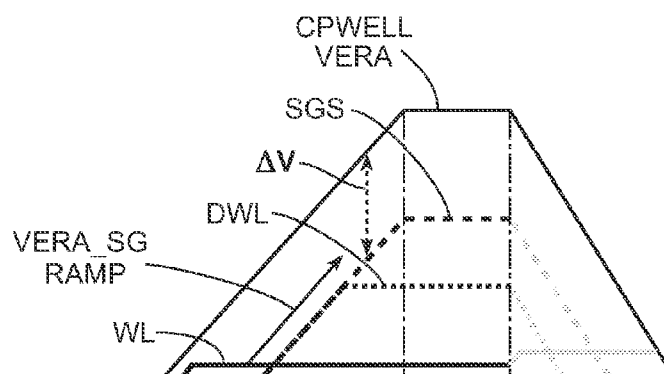


FIG. 23

(57) **Abstract:** In 3D NAND type memory structures, such as of the BiCS type, the NAND strings have a channel that runs vertically up from the substrate between the memory cells and select gates. In an erase process, holes travel up from the well down at the sub-
strate up towards the bit line in order to reach the cells to be erased. In such a process, the voltage applied to source side select gates should be low enough for the holes to pass through these gates and up the column, but not so low as to result in device breakdown as the erase voltage is applied to the well. Techniques are presented to do this by controlling the source side select gate voltages so that the difference from the well voltage is kept largely constant during the erase process by use of a fixed offset during ramping and at the final level for the erase process.



5 **DIGITALLY CONTROLLED SOURCE SIDE SELECT GATE OFFSET
IN 3D NAND MEMORY ERASE**

BACKGROUND

10 **[0001]** This application relates to the operation of re-programmable non-volatile memory systems such as semiconductor flash memory that record data using charge stored in charge storage elements of memory cells.

[0002] Solid-state memory capable of nonvolatile storage of charge, particularly in the form of EEPROM and flash EEPROM packaged as a small form factor card, has
15 recently become the storage of choice in a variety of mobile and handheld devices, notably information appliances and consumer electronics products. Unlike RAM (random access memory) that is also solid-state memory, flash memory is non-volatile, and retains its stored data even after power is turned off. Also, unlike ROM (read only memory), flash memory is rewritable similar to a disk storage device. In
20 spite of the higher cost, flash memory is increasingly being used in mass storage applications.

[0003] Flash EEPROM is similar to EEPROM (electrically erasable and programmable read-only memory) in that it is a non-volatile memory that can be erased and have new data written or “programmed” into their memory cells. Both
25 utilize a floating (unconnected) conductive gate, in a field effect transistor structure, positioned over a channel region in a semiconductor substrate, between source and drain regions. A control gate is then provided over the floating gate. The threshold voltage characteristic of the transistor is controlled by the amount of charge that is retained on the floating gate. That is, for a given level of charge on the floating gate,
30 there is a corresponding voltage (threshold) that must be applied to the control gate before the transistor is turned “on” to permit conduction between its source and drain regions. Flash memory such as Flash EEPROM allows entire blocks of memory cells to be erased at the same time.

[0004] The floating gate can hold a range of charges and therefore can be
35 programmed to any threshold voltage level within a threshold voltage window. The size of the threshold voltage window is delimited by the minimum and maximum

- 5 threshold levels of the device, which in turn correspond to the range of the charges that can be programmed onto the floating gate. The threshold window generally depends on the memory device's characteristics, operating conditions and history. Each distinct, resolvable threshold voltage level range within the window may, in principle, be used to designate a definite memory state of the cell.
- 10 [0005] In order to improve read and program performance, multiple charge storage elements or memory transistors in an array are read or programmed in parallel. Thus, a "page" of memory elements are read or programmed together. In existing memory architectures, a row typically contains several interleaved pages or it may constitute one page. All memory elements of a page are read or programmed together.
- 15 [0006] Nonvolatile memory devices are also manufactured from memory cells with a dielectric layer for storing charge. Instead of the conductive floating gate elements described earlier, a dielectric layer is used. An ONO dielectric layer extends across the channel between source and drain diffusions. The charge for one data bit is localized in the dielectric layer adjacent to the drain, and the charge for the other data
- 20 bit is localized in the dielectric layer adjacent to the source. For example, a nonvolatile memory cell may have a trapping dielectric sandwiched between two silicon dioxide layers. Multi-state data storage is implemented by separately reading the binary states of the spatially separated charge storage regions within the dielectric.

SUMMARY

- 25 [0007] A monolithic three-dimensional non-volatile semiconductor memory device includes a well structure formed in a silicon substrate, one or more strings each formed along a common channel structure above the well structure, and driver circuitry. The strings are each formed along a common channel structure above the well structure and run in a vertical direction relative to the substrate, each of the
- 30 strings having a plurality of memory cells connected in series between the well structure and a corresponding bit line respectively through source side and drain side select gates. The memory cells each have a charge storage medium and are arranged in multiple physical levels above the silicon substrate. The driver circuitry is connected to receive a clock signal and is connectable to apply voltage levels to the
- 35 well structure and control gates of the memory cells, the source side select gates, and

5 drain side select gates. When performing an erase operation on the strings, the driver circuitry applies to the well structure a first staircase waveform that begins with an initial level and increases in voltage with each of a first number of cycles of the clock signal. After a delay of a second number of clock cycles subsequent to beginning to
10 apply the first staircase waveform to the well structure, the driver circuitry applies the first staircase waveform beginning with the initial level to the control gates of the source side select gates for the remainder of the first number of clock cycles.

[0008] A method is presented of performing erase operation on a monolithic three-dimensional non-volatile semiconductor memory device. The memory device includes a well structure formed in a silicon substrate and one or more strings each
15 formed along a common channel structure above the well structure and running in a vertical direction relative to the substrate, each of the strings having a plurality of memory cells connected in series between the well structure and a corresponding bit line respectively through source side and drain side select gates, where the memory cells each have a charge storage medium and are arranged in multiple physical levels
20 above the silicon substrate. The method includes: applying to the well structure a first staircase waveform that begins with an initial level and increases in voltage with each of a first number of cycles of the clock signal; and, after a delay of a second number of clock cycles subsequent to beginning to apply the first staircase waveform to the well structure, applying the first staircase waveform beginning with the initial
25 level to the control gates of the source side select gates for the remainder of the first number of clock cycles.

[0009] Various aspects, advantages, features and embodiments are included in the following description of exemplary examples thereof, which description should be taken in conjunction with the accompanying drawings. All patents, patent
30 applications, articles, other publications, documents and things referenced herein are hereby incorporated herein by this reference in their entirety for all purposes. To the extent of any inconsistency or conflict in the definition or use of terms between any of the incorporated publications, documents or things and the present application, those of the present application shall prevail.

35 BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 illustrates schematically the main hardware components of a memory

5 system suitable for implementing various aspects described in the following.

[0011] **FIG. 2** illustrates schematically a non-volatile memory cell.

[0012] **FIG. 3** illustrates the relation between the source-drain current I_D and the control gate voltage V_{CG} for four different charges Q_1 - Q_4 that the floating gate may be selectively storing at any one time at fixed drain voltage.

10 [0013] **FIG. 4** illustrates schematically a string of memory cells organized into a NAND string.

[0014] **FIG. 5** illustrates an example of a NAND array 210 of memory cells, constituted from NAND strings 50 such as that shown in **FIG. 4**.

15 [0015] **FIG. 6** illustrates a page of memory cells, organized in the NAND configuration, being sensed or programmed in parallel.

[0016] **FIGs. 7A-7C** illustrate an example of programming a population of memory cells.

[0017] **FIG. 8** shows an example of a physical structure of a 3-D NAND string.

20 [0018] **FIGs. 9-12** look at a particular monolithic three dimensional (3D) memory array of the NAND type (more specifically of the “BiCS” type).

[0019] **FIG. 13** illustrates the erase process for a programmable threshold transistor.

[0020] **FIGs. 14A and 14B** respectively illustrate erase enable and erase inhibit case.

[0021] **FIGs. 14C and 14D** illustrate erase in 2D versus 3D memory structures.

[0022] **FIGs. 15A and 15B** illustrate the direct bias erase inhibit technique.

25 [0023] **FIGs. 16A and 16B** illustrate a coupling erase inhibit technique.

[0024] **FIG. 17** is a schematic representation of word/select line to word/select line variation in coupling ratios in a vertical NAND arrangement.

[0025] **FIGs. 18A and 18B** illustrate one approach to using capacitive coupling for erase inhibit.

5 [0026] FIGs. 19A-C illustrate an exemplary embodiment for using capacitive coupling for erase inhibit.

[0027] FIG. 20 schematically illustrates the erase process in a 2D floating gate NAND memory structure.

10 [0028] FIG. 21 schematically illustrates the erase process in a vertical NAND string arrangement.

[0029] FIG. 22 illustrates applying a high voltage for the source side select gates with a fixed delta during the ramping and final level of an erase as applied to the well.

[0030] FIG. 23 shows the well voltage, select gate voltage, and the voltage applied to word lines selected for erase and for the dummy word lines not selected for erase.

15 [0031] FIG. 24 looks at the well and source side select gate voltage waveform in more detail.

[0032] FIG. 25 is a block diagram for an example of some of the circuitry involved in an exemplary embodiment.

[0033] FIG. 26 looks at one variation on the waveforms of FIG. 24.

20 DETAILED DESCRIPTION

MEMORY SYSTEM

[0034] FIG. 1 illustrates schematically the main hardware components of a memory system suitable for implementing the following. The memory system 90 typically operates with a host 80 through a host interface. The memory system may be in the form of a removable memory such as a memory card, or may be in the form of an embedded memory system. The memory system 90 includes a memory 102 whose operations are controlled by a controller 100. The memory 102 comprises one or more array of non-volatile memory cells distributed over one or more integrated circuit chip. The controller 100 may include interface circuits 110, a processor 120, ROM (read-only-memory) 122, RAM (random access memory) 130, programmable nonvolatile memory 124, and additional components. The controller is typically formed as an ASIC (application specific integrated circuit) and the components

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5 included in such an ASIC generally depend on the particular application.

[0035] With respect to the memory section 102, semiconductor memory devices include volatile memory devices, such as dynamic random access memory (“DRAM”) or static random access memory (“SRAM”) devices, non-volatile memory devices, such as resistive random access memory (“ReRAM”), electrically erasable
10 programmable read only memory (“EEPROM”), flash memory (which can also be considered a subset of EEPROM), ferroelectric random access memory (“FRAM”), and magnetoresistive random access memory (“MRAM”), and other semiconductor elements capable of storing information. Each type of memory device may have different configurations. For example, flash memory devices may be configured in a
15 NAND or a NOR configuration.

[0036] The memory devices can be formed from passive and/or active elements, in any combinations. By way of non-limiting example, passive semiconductor memory elements include ReRAM device elements, which in some embodiments include a resistivity switching storage element, such as an anti-fuse, phase change material, etc.,
20 and optionally a steering element, such as a diode, *etc.* Further by way of non-limiting example, active semiconductor memory elements include EEPROM and flash memory device elements, which in some embodiments include elements containing a charge storage region, such as a floating gate, conductive nanoparticles, or a charge storage dielectric material.

25 [0037] Multiple memory elements may be configured so that they are connected in series or so that each element is individually accessible. By way of non-limiting example, flash memory devices in a NAND configuration (NAND memory) typically contain memory elements connected in series. A NAND memory array may be configured so that the array is composed of multiple strings of memory in which a
30 string is composed of multiple memory elements sharing a single bit line and accessed as a group. Alternatively, memory elements may be configured so that each element is individually accessible, *e.g.*, a NOR memory array. NAND and NOR memory configurations are exemplary, and memory elements may be otherwise configured.

[0038] The semiconductor memory elements located within and/or over a substrate
35 may be arranged in two or three dimensions, such as a two dimensional memory

5 structure or a three dimensional memory structure.

[0039] In a two dimensional memory structure, the semiconductor memory elements are arranged in a single plane or a single memory device level. Typically, in a two dimensional memory structure, memory elements are arranged in a plane (*e.g.*, in an x-z direction plane) which extends substantially parallel to a major surface of a substrate that supports the memory elements. The substrate may be a wafer over or in which the layer of the memory elements are formed or it may be a carrier substrate which is attached to the memory elements after they are formed. As a non-limiting example, the substrate may include a semiconductor such as silicon.

[0040] The memory elements may be arranged in the single memory device level in an ordered array, such as in a plurality of rows and/or columns. However, the memory elements may be arrayed in non-regular or non-orthogonal configurations. The memory elements may each have two or more electrodes or contact lines, such as bit lines and word lines.

[0041] A three dimensional memory array is arranged so that memory elements occupy multiple planes or multiple memory device levels, thereby forming a structure in three dimensions (*i.e.*, in the x, y and z directions, where the y direction is substantially perpendicular and the x and z directions are substantially parallel to the major surface of the substrate).

[0042] As a non-limiting example, a three dimensional memory structure may be vertically arranged as a stack of multiple two dimensional memory device levels. As another non-limiting example, a three dimensional memory array may be arranged as multiple vertical columns (*e.g.*, columns extending substantially perpendicular to the major surface of the substrate, *i.e.*, in the y direction) with each column having multiple memory elements in each column. The columns may be arranged in a two dimensional configuration, *e.g.*, in an x-z plane, resulting in a three dimensional arrangement of memory elements with elements on multiple vertically stacked memory planes. Other configurations of memory elements in three dimensions can also constitute a three dimensional memory array.

[0043] By way of non-limiting example, in a three dimensional NAND memory array, the memory elements may be coupled together to form a NAND string within a

5 single horizontal (*e.g.*, x-z) memory device levels. Alternatively, the memory elements may be coupled together to form a vertical NAND string that traverses across multiple horizontal memory device levels. Other three dimensional configurations can be envisioned wherein some NAND strings contain memory elements in a single memory level while other strings contain memory elements
10 which span through multiple memory levels. Three dimensional memory arrays may also be designed in a NOR configuration and in a ReRAM configuration.

[0044] Typically, in a monolithic three dimensional memory array, one or more memory device levels are formed above a *single* substrate. Optionally, the monolithic three dimensional memory array may also have one or more memory layers at least
15 partially within the single substrate. As a non-limiting example, the substrate may include a semiconductor such as silicon. In a monolithic three dimensional array, the layers constituting each memory device level of the array are typically formed on the layers of the underlying memory device levels of the array. However, layers of adjacent memory device levels of a monolithic three dimensional memory array may
20 be shared or have intervening layers between memory device levels.

[0045] Then again, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device having multiple layers of memory. For example, non-monolithic stacked memories can be constructed by forming memory levels on separate substrates and then stacking the memory levels
25 atop each other. The substrates may be thinned or removed from the memory device levels before stacking, but as the memory device levels are initially formed over separate substrates, the resulting memory arrays are not monolithic three dimensional memory arrays. Further, multiple two dimensional memory arrays or three dimensional memory arrays (monolithic or non-monolithic) may be formed on
30 separate chips and then packaged together to form a stacked-chip memory device.

[0046] Associated circuitry is typically required for operation of the memory elements and for communication with the memory elements. As non-limiting examples, memory devices may have circuitry used for controlling and driving memory elements to accomplish functions such as programming and reading. This
35 associated circuitry may be on the same substrate as the memory elements and/or on a separate substrate. For example, a controller for memory read-write operations may

- 5 be located on a separate controller chip and/or on the same substrate as the memory elements.

[0047] It will be recognized that the following is not limited to the two dimensional and three dimensional exemplary structures described but cover all relevant memory structures within the spirit and scope as described herein

10 Physical Memory Structure

[0048] FIG. 2 illustrates schematically a non-volatile memory cell. The memory cell 10 can be implemented by a field-effect transistor having a charge storage unit 20, such as a floating gate or a charge trapping (dielectric) layer. The memory cell 10 also includes a source 14, a drain 16, and a control gate 30.

- 15 [0049] There are many commercially successful non-volatile solid-state memory devices being used today. These memory devices may employ different types of memory cells, each type having one or more charge storage element.

[0050] Typical non-volatile memory cells include EEPROM and flash EEPROM. Also, examples of memory devices utilizing dielectric storage elements.

- 20 [0051] In practice, the memory state of a cell is usually read by sensing the conduction current across the source and drain electrodes of the cell when a reference voltage is applied to the control gate. Thus, for each given charge on the floating gate of a cell, a corresponding conduction current with respect to a fixed reference control gate voltage may be detected. Similarly, the range of charge programmable onto the
25 floating gate defines a corresponding threshold voltage window or a corresponding conduction current window.

- [0052] Alternatively, instead of detecting the conduction current among a partitioned current window, it is possible to set the threshold voltage for a given memory state under test at the control gate and detect if the conduction current is lower or higher
30 than a threshold current (cell-read reference current). In one implementation the detection of the conduction current relative to a threshold current is accomplished by examining the rate the conduction current is discharging through the capacitance of the bit line.

5 [0053] FIG. 3 illustrates the relation between the source-drain current I_D and the control gate voltage V_{CG} for four different charges Q1-Q4 that the floating gate may be selectively storing at any one time. With fixed drain voltage bias, the four solid I_D versus V_{CG} curves represent four of seven possible charge levels that can be programmed on a floating gate of a memory cell, respectively corresponding to four possible memory states. As an example, the threshold voltage window of a population of cells may range from 0.5V to 3.5V. Seven possible programmed memory states “0”, “1”, “2”, “3”, “4”, “5”, “6”, and an erased state (not shown) may be demarcated by partitioning the threshold window into regions in intervals of 0.5V each. For example, if a reference current, I_{REF} of 2 μ A is used as shown, then the cell programmed with Q1 may be considered to be in a memory state “1” since its curve intersects with I_{REF} in the region of the threshold window demarcated by $V_{CG} = 0.5V$ and 1.0V. Similarly, Q4 is in a memory state “5”.

[0054] As can be seen from the description above, the more states a memory cell is made to store, the more finely divided is its threshold window. For example, a memory device may have memory cells having a threshold window that ranges from -1.5V to 5V. This provides a maximum width of 6.5V. If the memory cell is to store 16 states, each state may occupy from 200mV to 300mV in the threshold window. This will require higher precision in programming and reading operations in order to be able to achieve the required resolution.

25 NAND Structure

[0055] FIG. 4 illustrates schematically a string of memory cells organized into a NAND string. A NAND string 50 comprises a series of memory transistors M1, M2, ... Mn (e.g., n= 4, 8, 16 or higher) daisy-chained by their sources and drains. A pair of select transistors S1, S2 controls the memory transistor chain's connection to the external world via the NAND string's source terminal 54 and drain terminal 56 respectively. In a memory array, when the source select transistor S1 is turned on, the source terminal is coupled to a source line (see FIG. 5). Similarly, when the drain select transistor S2 is turned on, the drain terminal of the NAND string is coupled to a bit line of the memory array. Each memory transistor 10 in the chain acts as a memory cell. It has a charge storage element 20 to store a given amount of charge so as to represent an intended memory state. A control gate 30 of each memory

5 transistor allows control over read and write operations. As will be seen in **FIG. 5**, the control gates 30 of corresponding memory transistors of a row of NAND string are all connected to the same word line. Similarly, a control gate 32 of each of the select transistors S1, S2 provides control access to the NAND string via its source terminal 54 and drain terminal 56 respectively. Likewise, the control gates 32 of
10 corresponding select transistors of a row of NAND string are all connected to the same select line.

[0056] When an addressed memory transistor 10 within a NAND string is read or is verified during programming, its control gate 30 is supplied with an appropriate voltage. At the same time, the rest of the non-addressed memory transistors in the
15 NAND string 50 are fully turned on by application of sufficient voltage on their control gates. In this way, a conductive path is effectively created from the source of the individual memory transistor to the source terminal 54 of the NAND string and likewise for the drain of the individual memory transistor to the drain terminal 56 of the cell.

20 [0057] **FIG. 5** illustrates an example of a NAND array 210 of memory cells, constituted from NAND strings 50 such as that shown in **FIG. 4**. Along each column of NAND strings, a bit line such as bit line 36 is coupled to the drain terminal 56 of each NAND string. Along each bank of NAND strings, a source line such as source line 34 is coupled to the source terminals 54 of each NAND string. Also the control
25 gates along a row of memory cells in a bank of NAND strings are connected to a word line such as word line 42. The control gates along a row of select transistors in a bank of NAND strings are connected to a select line such as select line 44. An entire row of memory cells in a bank of NAND strings can be addressed by appropriate voltages on the word lines and select lines of the bank of NAND strings.

30 [0058] **FIG. 6** illustrates a page of memory cells, organized in the NAND configuration, being sensed or programmed in parallel. **FIG. 6** essentially shows a bank of NAND strings 50 in the memory array 210 of **FIG. 5**, where the detail of each NAND string is shown explicitly as in **FIG. 4**. A physical page, such as the page 60, is a group of memory cells enabled to be sensed or programmed in parallel.
35 This is accomplished by a corresponding page of sense amplifiers 212. The sensed results are latched in a corresponding set of latches 214. Each sense amplifier can be

5 coupled to a NAND string via a bit line. The page is enabled by the control gates of the cells of the page connected in common to a word line 42 and each cell accessible by a sense amplifier accessible via a bit line 36. As an example, when respectively sensing or programming the page of cells 60, a sensing voltage or a programming voltage is respectively applied to the common word line WL3 together with
10 appropriate voltages on the bit lines.

Physical Organization of the Memory

[0059] One difference between flash memory and other of types of memory is that a cell is programmed from the erased state. That is, the floating gate is first emptied of charge. Programming then adds a desired amount of charge back to the floating gate.
15 It does not support removing a portion of the charge from the floating gate to go from a more programmed state to a lesser one. This means that updated data cannot overwrite existing data and is written to a previous unwritten location.

[0060] Furthermore erasing is to empty all the charges from the floating gate and generally takes appreciable time. For that reason, it will be cumbersome and very
20 slow to erase cell by cell or even page by page. In practice, the array of memory cells is divided into a large number of blocks of memory cells. As is common for flash EEPROM systems, the block is the unit of erase. That is, each block contains the minimum number of memory cells that are erased together. While aggregating a large number of cells in a block to be erased in parallel will improve erase performance, a
25 large size block also entails dealing with a larger number of update and obsolete data.

[0061] Each block is typically divided into a number of physical pages. A logical page is a unit of programming or reading that contains a number of bits equal to the number of cells in a physical page. In a memory that stores one bit per cell, one physical page stores one logical page of data. In memories that store two bits per cell,
30 a physical page stores two logical pages. The number of logical pages stored in a physical page thus reflects the number of bits stored per cell. In one embodiment, the individual pages may be divided into segments and the segments may contain the fewest number of cells that are written at one time as a basic programming operation. One or more logical pages of data are typically stored in one row of memory cells. A
35 page can store one or more sectors. A sector includes user data and overhead data.

5 All-bit, Full-Sequence MLC Programming

[0062] FIG. 7A – 7C illustrate an example of programming a population of 4-state memory cells. FIG. 7A illustrates the population of memory cells programmable into four distinct distributions of threshold voltages respectively representing memory states “0”, “1”, “2” and “3”. FIG. 7B illustrates the initial distribution of “erased” threshold voltages for an erased memory. FIG. 6C illustrates an example of the memory after many of the memory cells have been programmed. Essentially, a cell initially has an “erased” threshold voltage and programming will move it to a higher value into one of the three zones demarcated by verify levels vV_1 , vV_2 and vV_3 . In this way, each memory cell can be programmed to one of the three programmed states “1”, “2” and “3” or remain un-programmed in the “erased” state. As the memory gets more programming, the initial distribution of the “erased” state as shown in FIG. 7B will become narrower and the erased state is represented by the “0” state.

[0063] A 2-bit code having a lower bit and an upper bit can be used to represent each of the four memory states. For example, the “0”, “1”, “2” and “3” states are respectively represented by “11”, “01”, “00” and “10”. The 2-bit data may be read from the memory by sensing in “full-sequence” mode where the two bits are sensed together by sensing relative to the read demarcation threshold values rV_1 , rV_2 and rV_3 in three sub-passes respectively.

3-D NAND structures

[0064] An alternative arrangement to a conventional two-dimensional (2-D) NAND array is a three-dimensional (3-D) array. In contrast to 2-D NAND arrays, which are formed along a planar surface of a semiconductor wafer, 3-D arrays extend up from the wafer surface and generally include stacks, or columns, of memory cells extending upwards. Various 3-D arrangements are possible. In one arrangement a NAND string is formed vertically with one end (e.g. source) at the wafer surface and the other end (e.g. drain) on top. In another arrangement a NAND string is formed in a U-shape so that both ends of the NAND string are accessible on top, thus facilitating connections between such strings.

[0065] FIG. 8 shows a first example of a NAND string 701 that extends in a vertical direction, i.e. extending in the z-direction, perpendicular to the x-y plane of the

5 substrate. Memory cells are formed where a vertical bit line (local bit line) 703 passes through a word line (e.g. WL0, WL1, etc.). A charge trapping layer between the local bit line and the word line stores charge, which affects the threshold voltage of the transistor formed by the word line (gate) coupled to the vertical bit line (channel) that it encircles. Such memory cells may be formed by forming stacks of word lines and
10 then etching memory holes where memory cells are to be formed. Memory holes are then lined with a charge trapping layer and filled with a suitable local bit line/channel material (with suitable dielectric layers for isolation).

[0066] As with planar NAND strings, select gates 705, 707, are located at either end of the string to allow the NAND string to be selectively connected to, or isolated
15 from, external elements 709, 711. Such external elements are generally conductive lines such as common source lines or bit lines that serve large numbers of NAND strings. Vertical NAND strings may be operated in a similar manner to planar NAND strings and both SLC and MLC operation is possible. While **FIG. 8** shows an example of a NAND string that has 32 cells (0-31) connected in series, the number of
20 cells in a NAND string may be any suitable number. Not all cells are shown for clarity. It will be understood that additional cells are formed where word lines 3-29 (not shown) intersect the local vertical bit line.

[0067] A 3D NAND array can, loosely speaking, be formed tilting up the respective structures 50 and 210 of **FIGs. 5** and **6** to be perpendicular to the x-y plane. In this
25 example, each y-z plane corresponds to the page structure of **FIG. 6**, with m such plane at differing x locations. The (global) bit lines, BL1-m, each run across the top to an associated sense amp SA1-m. The word lines, WL1-n, and source and select lines SSL1-n and DSL1-n, then run in x direction, with the NAND string connected at bottom to a common source line CSL.

30 [0068] **FIGs. 9-12** look at a particular monolithic three dimensional (3D) memory array of the NAND type (more specifically of the “BiCS” type), where one or more memory device levels are formed above a single substrate, in more detail. **FIG. 9** is an oblique projection of part of such a structure, showing a portion corresponding to two of the page structures in **FIG. 5**, where, depending on the embodiment, each of
35 these could correspond to a separate block or be different “fingers” of the same block. Here, instead to the NAND strings lying in a common y-z plane, they are squashed

5 together in the y direction, so that the NAND strings are somewhat staggered in the x direction. On the top, the NAND strings are connected along global bit lines (BL) spanning multiple such sub-divisions of the array that run in the x direction. Here, global common source lines (SL) also run across multiple such structures in the x direction and are connect to the sources at the bottoms of the NAND string, which are
10 connected by a local interconnect (LI) that serves as the local common source line of the individual finger. Depending on the embodiment, the global source lines can span the whole, or just a portion, of the array structure. Rather than use the local interconnect (LI), variations can include the NAND string being formed in a U type structure, where part of the string itself runs back up.

15 [0069] To the right of **FIG. 9** is a representation of the elements of one of the vertical NAND strings from the structure to the left. Multiple memory cells are connected through a drain select gate SGD to the associated bit line BL at the top and connected through the associated source select gate SDS to the associated local source line LI to a global source line SL. It is often useful to have a select gate with a greater length
20 than that of memory cells, where this can alternately be achieved by having several select gates in series (as described in US patent application number 13/925,662, filed on June 24, 2013), making for more uniform processing of layers. Additionally, the select gates are programmable to have their threshold levels adjusted. This exemplary embodiment also includes several dummy cells at the ends that are not used to store
25 user data, as their proximity to the select gates makes them more prone to disturbs.

[0070] **FIG. 10** shows a top view of the structure for two blocks in the exemplary embodiment. Two blocks (BLK0 above, BLK1 below) are shown, each having four fingers that run left to right. The word lines and select gate lines of each level also run left to right, with the word lines of the different fingers of the same block being
30 commonly connected at a “terrace” and then on to receive their various voltage level through the word line select gates at WLTr. The word lines of a given layer in a block can also be commonly connected on the far side from the terrace. The selected gate lines can be individual for each level, rather common, allowing the fingers to be individually selected. The bit lines are shown running up and down the page and
35 connect on to the sense amp circuits, where, depending on the embodiment, each sense amp can correspond to a single bit line or be multiplexed to several bit lines.

5 [0071] FIG. 11 shows a side view of one block, again with four fingers. In this exemplary embodiment, the select gates SGD and SGS at either end of the NAND strings are formed of four layers, with the word lines WL in-between, all formed over a CPWELL. A given finger is selected by setting its select gates to a level VSG and the word lines are biased according to the operation, such as a read voltage (VCGRV)
10 for the selected word lines and the read-pass voltage (VREAD) for the non-selected word lines. The non-selected fingers can then be cut off by setting their select gates accordingly.

[0072] FIG. 12 illustrates some detail of an individual cell. A dielectric core runs in the vertical direction and is surrounded by a channel silicon layer, that is in turn
15 surrounded a tunnel dielectric (TNL) and then the charge trapping dielectric layer (CTL). The gate of the cell is here formed of tungsten with which is surrounded by a metal barrier and is separated from the charge trapping layer by blocking (BLK) oxide and a high K layer.

Erase of Programmable Transistors

20 [0073] The goal of erase is to clean the electrons collected in the charge-trapping layer. By raising the channel to a high voltage, and applying a low voltage to the gate, an electric field is created. The electrons are pushed out of the charge trapping layer back into the polysilicon. This is illustrated schematically in FIG. 13, where example values of 0.5V and 20V are respectively applied to the gate and channel of
25 the transistor.

[0074] There are circumstances when it may be wanted to erase some, but not all, of the cells or other programmable transistors on the shared polysilicon that is raised to a high voltage in the erase process. For example, the BiCS structure described above uses programmable select gates and, when erasing the data cells of a block, it may not
30 be wanted to erase any select gates or dummy word lines (i.e., word lines, typically end word lines or sets of word lines not storing user data) of the block. FIGS. 14A and 14B illustrate the two cases with some example voltages. FIG. 14A shows an erase enable case, where by applying a low voltage to the gate, a strong electric field is created and the electrons in the charge trapping layer are pushed back into the
35 polysilicon. FIG. 14B looks at the erase inhibit case: By applying a high voltage to

5 the gate, either no electric field or a very weak electric field is created and the electric field is not strong enough to push the electrons out of the charge trapping layer, thus the cell remains the same.

[0075] The erase process for a 3D/BiCS-type memory is different than for 2D NAND types of memory, as illustrated respectively in **FIGs. 14D** and **14C**. In the 3D/BiCS,
10 there is no body so that a channel must be passed through and the channel is made up of holes.

[0076] In order to inhibit erase of a programmable transistor, whether a memory cell or select gate, a high voltage is applied to the corresponding control line (word line or select gate line). This can be done by either a direct bias or coupling. **FIGs. 15A** and
15 **15B** illustrate the direct bias case. As shown schematically in **FIG. 15A**, a word line 503 is connected to an input line through decoding circuitry represented by the transistor 505. The word line is capacitively coupled to the well structure. To set the erase inhibit voltage (15V in this example) on the word line, the voltage is applied on the input line and a relatively high pass voltage VERAH is applied to the gate of the
20 decoding transistor 503 to fully pass the voltage from the input line to the word line. With the word line (or select line) so biased, when the CP well voltage is set to the erase voltage VERA (=23V in this example). **FIG. 15B** illustrates the various waveforms.

[0077] **FIGs. 15A** and **15B** illustrate the coupling case. **FIG. 15A** again shows a
25 word line 503 connected to an input line through decoding circuitry represented by the transistor 505. The word line is capacitively coupled to the well structure. The transistor 505 shares decoding with other word lines and select lines of the NAND string or block so that the gate of 505 and the other lines that share decoding need to be set high enough to pass the low voltage (such as 0-3V) on the selected IN lines.
30 Here 5V is applied to the gate of the block select (BLKSEL) transistor. The IN line is again at a higher voltage (here $V=15$), but once the voltage on the word line is greater than BLKSET less the threshold voltage of 505, $WL > 5V - V_t$, the block select transistor will cut off, leaving the word line (or select line) to float. Due to the capacitive coupling to the well, as the word line is floating, as CPWELL rises it will
35 also couple up the word line or select line to be erase inhibited.

5 **[0078]** The direct bias arrangement has the advantage that the word line voltage is set accurately as directly biased, but has the drawbacks that the select transistor gate needs to be brought to a high voltage level that induces high stress levels and consumes power. The coupling arrangement causes less stress and consumes less power, but is less accurate as the final voltage depends on coupling ratio between
10 CPWELL and the control line; and if the word/select line level is not accurate the transistor may be erased or suffer dielectric breakdown.

[0079] This word line to word line variation in coupling ratios can be particularly pronounced in the vertical NAND arrangement of 3D/BiCS type memories, as is illustrated schematically with respect to **FIG. 17**. Due to memory hole width
15 variation, the capacitance can change between word/select lines at the top, where the coupling ratio may be something like 75%, and word/select lines at the bottom, where the coupling ratios may be something like 50-60%. The bottom lines can have very low coupling ratios making it difficult for them to couple up to desired erase inhibit level. This situation is thus particularly acute in the case where the data word lines
20 are to be erased, but the select gates, dummy word lines, or both are not to be erased, as these are the top-most and bottom-most lines. (These sorts of variations between top and bottom word lines can also affect read and program operations, as is discussed further in US patent application numbers 14/328,018; 14/486,152; and 14/508,352.)

TIME DOMAIN RAMP RATE CONTROL FOR ERASE INHIBIT

25 **[0080]** As noted above, vertically arranged NAND memories, such as of the BiCS type, there is a big difference in the capacitance between the word/select lines at the top and at the bottom. Also, the lines at the bottom may have a low coupling ratio, making the word line voltage level during coupling erase difficult to make accurate and to bring to a high voltage level. This section looks at techniques for dealing with
30 issue.

[0081] Considering coupling erase further, and referring to the arrangement of **FIG. 18A** which again shows a word line 503 capacitively coupled to the well and connected through a block decoding switch 505 to the input line 501, one approach illustrated with respect to **FIG. 18B** is to keep IN at VSS as CPWELL rises to above a
35 level V_{detect} . When $\text{CPWELL} > V_{\text{detect}}$, a Flag will go high. When

- 5 CPWELL > Vdetect, IN will rise to a voltage higher than BLKSEL, cutting off the transistor on that side as $(\text{BLKSEL} - \text{IN}) < V_t$, where V_t is the threshold voltage of the block select transistor 505. The word line will charge up to $\text{BLKSEL} - V_t$ initially, then WL will be coupled up by CPWELL to its final level, where the amount the word line is coupled up by is determined by coupling ratio.
- 10 **[0082]** This arrangement has some limitations. A first is that the Vdetect level must be greater than $(\text{BLKSEL} - V_t)$. If not, then when the word line charges up to $(\text{BLKSEL} - V_t)$, it will be higher than CPWELL; and if $\text{WL} > \text{CPWELL}$, the channel cannot pass the holes. Also, the erased word line voltage can be 0V, and the neighbor cannot be too high due to dielectric breakdown. Another limitation of this
- 15 arrangement is that it also has a direct dependence on V_t , so that depending on the process corner of the specific device, the V_t will change and this will have a direct effect on the final level. Additionally, due to first limitation, the final level of the word line may not be high enough.

- [0083]** To improve upon this situation, this section introduces a method for coupling
- 20 erase that uses a time delay to create a voltage difference (Δ) between the VERA level on the well and the word/select line voltage. It also utilizes a ramp rate control so the input signal will ramp at same rate as VERA. More specifically, for the transistors to be erase inhibited, the raising of the IN level is delayed until CPWELL reaches a certain Δ , after which IN rises at same rate as CPWELL. The
- 25 word/select line will be directly biased until IN reaches $\text{BLKSEL} - V_t$, after which WL is coupled up to its final level as determined by the coupling ratio.

- [0084] FIG. 19A** shows the word lines and select lines as would attach to a NAND string, where only end most drain and source select lines (SGD, SGS) and a pair of intervening word lines are shown. These lines are all capacitively coupled to the well
- 30 and are connected to their corresponding IN line through the block select transistors, such as IN line 901 being connected through switch 903 for SGD line 905. (Under arrangements with multiple source and/or drain select gates, more than one transistor may an IN line and maybe also switch.) The decoding circuit 907 is connected to the gates of the block select transistors and the IN levels, as well as the well voltage, are
- 35 provided by drivers 909. In this example, the select gates are to be erase inhibited and the intervening word lines to be erased. Consequently, the word lines have their

- 5 corresponding IN lines set at a low, erase enable voltage, where this level is low enough to fully pass to the word lines.

[0085] **FIG. 19B** illustrates the delaying the IN value relative to erase voltage VERA that is being applied to the well. After a time delay, IN ramps up and as long as it is below BLKSEL-V_t, it will set the level on the corresponding word or select gate line.
 10 Once at BLKSEL-V_t, the switch turns off and the line is then pulled up as illustrated by the dashed line to a level of:

$$V = (VERA - (BLKSEL - V_t) - \Delta) * Cr + BLKSEL - V_t$$

$$= (VERA - \Delta) * Cr + (1 - Cr) * (BLKSEL - V_t),$$

where Cr is coupling ratio. In **FIG. 19B**, the dashed line showing the coupling up
 15 shows the situation for different delays, but for the same coupling ratio. Consequently, lines with different coupling ratios can use different delays to get to the same level. In the **FIG. 19B**, the value of IN is not shown once it reaches BLKSEL-V_t, as the switch turns off at this point, but it can continue on to BLKSEL as a convenient value or some lower level that, as it needs to be at least BLKSEL-V_t for
 20 all of the switches, that is offset to some lower level such as BLKSEL- ½V_t.

[0086] Returning to **FIG. 19A**, the example is used where the two shown word lines are to be erased while inhibiting the two shown select gates. In the BiCS example, as discussed above with respect to **FIG. 17**, the bottom of the NAND string typically has a lower coupling ratio than at the top; and as the select gates are at the ends of the
 25 NAND string, the difference in coupling ratios between the source and drain side select gates can be pronounced. Consequently, IN1 at the drain side has a longer delay than the IN0 at the source. This is illustrated at **FIG. 19C**.

[0087] In the example of **FIGs. 19A-C**, the word lines were selected to be erased while the select gates were erase inhibited, but various combinations of select gates
 30 and word lines (both those holding data and dummy word lines) can be chosen. In terms of the amount of delay for the different word lines and select lines, these need not be set individually, but in adjacent groups: For example, all of the source side select lines can use the same delay, and all of the drain side select lines can use a common (but different than on the source side) delay; and if it is desired to erase
 35 inhibit word lines, the delays of all the word lines of a zone of adjacent word lines can have a common value. Alternately, the delays can be set individually if a particularly

5 accurate coupling erase is desired, but at the cost being able to generate the appropriate values for each word/select line. The various delay values can be determined based upon device characterizations.

[0088] Under this arrangement, there is not the sort of limitation discussed above with respect to **FIG. 18B** that V_{detect} needs to be greater than $(\text{BLKSEL}-V_t)$. There is no
10 restriction for the delta, so it can be adjusted to provide the final level needed. Also, the word and select line levels will be below CPWELL level, so that the channel maintains its conductivity for the whole string.

[0089] Additionally, the corner for the block select transistors' threshold voltage has a reduced effect on the file level as it is multiplied by $(1-C_r)$, as seen in the equation
15 above. Since the coupling ratio (C_r) is normally relatively high, the V_t value has a small effect on final level. A further advantage relative to the arrangement of **FIG. 18B** is that as no circuitry is need to detect the well level in order to determine when to raise I_N , the area requirement is reduced.

Digital Controlled High Voltage Source Side Select Gate Offset in Erase

20 [0090] This section looks further at the erase process in vertically arranged NAND memories, such as of the BiCS type, further. In particular, it considers the voltage control of the source side select gates during an erase operation.

[0091] Considering the erase process further, for comparison, **FIG. 20** schematically illustrates the erase process in a 2D floating gate NAND memory structure. A pair
25 memory cells are illustrated between a source side select gate (SGS) and a drain side select gate (SGD), with the n-type source-drain regions between the transistors and the bit line (BL) and source line (CELSRC) respectively connected at the drain and source ends of the string. The CP-well connects at the p region and spreads under the memory cells, so that the select gate voltage has no influence on an erase operation,
30 represented as the arrows.

[0092] In the vertical NAND string arrangement, as in BiCS, the situation is not so simple, as is represented in **FIG. 21**. Here, the channel runs vertically between the memory cells and select gates, with holes travelling up from the CP-well down at the substrate up towards the bit line BL in order to reach the cells to be erased. (**FIG. 21**

5 illustrates an example using multiple select gates in series, as described above for the BiCS structure, where some or all of these can be commonly controlled.) In order to raise the channel voltage, the holes have to pass through the area controlled by source side select gates SGS, so that SGS voltage must be lowered to a certain level lest SGS should prevent the holes to pass. (Loosely speaking, the select gate is function as if it
10 were a PMOS relative to the holes.) However, the bottom SGS would break down if SGS voltage is too low. Consequently, the voltage applied to the select gate needs to be low enough for the holes to pass through the gates and up the column, but not so low as to result in device breakdown as the erase voltage VERA is applied to the well. This section presents techniques to do this by controlling the SGS voltages so that
15 there difference from the CP-well voltage VERA is kept constant, or are at least within an acceptable range, during the erase process.

[0093] More specifically, the exemplary embodiment generates a high voltage (VERA_SG) for the source side select gates with a fixed delta during the ramping and final level of VERA as applied to the well. This illustrated in **FIG. 22**, which shows
20 the fixed $\Delta V = (VERA - VERA_SG)$ during ramping and at the final level for the erase process. **FIG. 23** shows these two voltages along with the voltage applied to word lines selected for erase and for the dummy word lines (or other word lines) not selected for erase. The dummy (or other) word lines not to be erased can either be driven directly or left to float and be pulled up, such as is described above in the preceding
25 section. This allows the holes to pass up the column without overly stressing the devices at each step.

[0094] The exemplary embodiments control the high voltage VERA (to the well) and VERA_SG (to the source side select gates) ramping and offset through digital DAC (converting to digital time domain). The ramping offset can be same or different from
30 final voltage offset. The digital control allows for the offset to be translated directly to the count. By converting the fixed $\Delta V (VERA - VERA_SG)$ from the analog high voltage domain to digital time domain, the step ramping can be set to match the strength of the charge pump circuitry supplying these voltages, independently of PVT, providing a more accurate ΔV that can be controlled during ramping and regulation.

35 [0095] **FIG. 24** looks at the VERA and VERA_SG voltage waveform in more detail. In this example, the levels start at an on-chip supply level of 2.4V and increases by a

5 step size of 0.4V. BINVERA_INT shows the count for VERA waveform, which increases by one step at each count until the full VERA level is reached. BINVERASG_INT shows the count for VERA_SG waveform, which after a delay increases by one step at each count until the full VERA_SG level is reached. At bottom is the delay of, in this example, 5 count (DAC) to provide the delta offset
 10 control during ramping. By delaying by, in this example, 5 counts, a fixed delta_V (VERA – VERASG) is realized during ramping. Depending on the case, this offset can be same or different from final delta offset. Above the counts is shown enable signals for the charge pump providing these levels. Initially, when the pump enabled by VMASIST is stronger and the counting is faster in this example. After the initial
 15 ramp up, the circuitry switches to less strong pumping circuitry enabled by VMASIST2/3 and the DAC counting is slowed.

[0096] FIG. 25 is a block diagram for an example of some of the circuitry involved. The charge pump UMSYS PUMP 2501 provides a level VERAH when FLG is asserted, which is then dropped by the diode 2503 to provide the VERA level. The
 20 regulator circuit VERA LIMITER 2505 receives the count BIVERA_INT and the VERA level to provide the FLG signal to the pump. The pump VMSYS PUMP 2507 can assist in providing VERA based on the signals FLG and VMASIST to help provide VERA through switch 2509 controlled by VMASIST. A select gate step down regulator 2511 is connected to receive VERA and provide VERA_SG, where
 25 the regulator VSG LIMITER 2513 receives the count BINVSG_INT. In the examples described here, only a single VERA_SG is generated, but the concept readily extends to multiple such signals with differing offsets and delays.

[0097] The control circuitry, such as can implemented by synthetic logic, includes a counter and comparison circuit 2519 that provides the BINVSG_INT clock to the
 30 regulator VSG LIMITER 2513 based on inputs such as an enable signal from the logic block 2517, the erase clock from block 2515, and the BINVERSG input. The control circuitry 2517 includes counter and comparison function and also provides the delay count for VERA_SG relative to VERA by way of the VMASIST signal, the VERA count BINVERA_INT, and a counter enable signal for block 2519 that are
 35 generated from inputs for an enable signal, a signal to specify the delta or delay, and the BINVERA input. The erase clock is provided from the block 2515 based on

5 control signals including the VMASSIST signal and a pump clock signal.

[0098] Under the arrangement described here, VERA_SG for the source select gates is generated from VERA by using the step down regulator 2511 to track VERA_SG with VERA. The control blocks provide the signals for the VERA / VERA_SG ramp control, where VERA and VERA_SG can have similar limiter designs (respectively
10 2505 and 2523). The digital ramp control through DAC counting is here implemented as the two DAC counters and comparators (2517, 2519), with one for each limiter. The control blocks can generate the clock signals described with respect to **FIG. 24**, where the offset clock counting for VMASSIST can be matched to pump strength. The internal pump ramp rate should be faster or equal to CLOCK_VERA for the
15 DAC counter and comparators. The VMASSIST detection can be done though the logic, where the VMASSIST signal is generated by the COUNTER/COMP block at 2517.

[0099] **FIG. 26** looks at one variation on the waveforms of **FIG. 24** to illustrate how to adapt the voltages to different requirements. In this example, the erase voltage is
20 initial taken to a first level VERA, then raised in a series of (here, two) steps. The select gate voltage tracks as before, with the 5 count delay corresponding to 2V delta.

Conclusion

[0100] The foregoing detailed description has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the above to
25 the precise form disclosed. Many modifications and variations are possible in light of the above teaching. The described embodiments were chosen in order to explain the principles involved and its practical application, to thereby enable others to best utilize the various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope be defined by the claims
30 appended hereto.

5 IT IS CLAIMED:

1. A monolithic three-dimensional non-volatile semiconductor memory device, comprising:

a well structure formed in a silicon substrate;

one or more strings each formed along a common channel structure above the well structure and running in a vertical direction relative to the substrate, each of the strings having a plurality of memory cells connected in series between the well structure and a corresponding bit line respectively through source side and drain side select gates, where the memory cells each have a charge storage medium and are arranged in multiple physical levels above the silicon substrate; and

driver circuitry connected to receive a clock signal and connectable to apply voltage levels to the well structure and control gates of the memory cells, the source side select gates, and drain side select gates,

wherein, when performing an erase operation on the strings, the driver circuitry applies to the well structure a first staircase waveform that begins with an initial level and increases in voltage with each of a first number of cycles of the clock signal and, after a delay of a second number of clock cycles subsequent to beginning to apply the first staircase waveform to the well structure, applies the first staircase waveform beginning with the initial level to the control gates of the source side select gates for the remainder of the first number of clock cycles.

25

2. The monolithic three-dimensional non-volatile semiconductor memory device of claim 1, further comprising:

a plurality of word lines along which the control gates of memory cells are connected and whereby the driver circuitry is connectable thereto, wherein the word lines run in horizontal relative to the substrate;

30

one or more drain select lines along which the control gates of the source side select gates are connected and whereby the driver circuitry is connectable thereto, wherein the drain select lines run in horizontal relative to the substrate; and

one or more source select lines along which the control gates of the source side select gates are connected and by which the first staircase waveform is applied to the control gates of source side select gates, wherein in the source and drain select lines run in horizontal relative to the substrate.

35

5

3. The monolithic three-dimensional non-volatile semiconductor memory device of claim 2, wherein, when performing the erase operation on the strings, the driver circuitry sets the word lines corresponding to memory cells selected for erase to a low voltage level.

10

4. The monolithic three-dimensional non-volatile semiconductor memory device of claim 3, wherein the low voltage level is ground.

5. The monolithic three-dimensional non-volatile semiconductor memory device of claim 3, wherein the plurality of word lines includes one or more dummy word lines not used for the storage of user data adjacent to one or both of the source side and drain side select lines, wherein when performing the erase operation on the strings, the dummy word lines are set to float.

6. The monolithic three-dimensional non-volatile semiconductor memory device of claim 1, wherein the strings include one or both of multiple source side select gates connected in series and multiple drain side select gates connected in series.

7. The monolithic three-dimensional non-volatile semiconductor memory device of claim 1, further comprising:
a clock connected to the driver circuitry to provide the clock signal thereto.

8. The monolithic three-dimensional non-volatile semiconductor memory device of claim 1, wherein the frequency of the clock signal decreases after a third number of cycles subsequent to beginning to apply the first staircase waveform to the well structure.

9. A method of performing erase operation on a monolithic three-dimensional non-volatile semiconductor memory device, where the memory device includes a well structure formed in a silicon substrate and one or more strings each formed along a common channel structure above the well structure and running in a vertical direction relative to the substrate, each of the strings having a plurality of memory cells connected in series between the well structure and a corresponding bit line

5 respectively through source side and drain side select gates, where the memory cells each have a charge storage medium and are arranged in multiple physical levels above the silicon substrate, the method comprising:

 applying to the well structure a first staircase waveform that begins with an initial level and increases in voltage with each of a first number of cycles of the clock
10 signal; and

 after a delay of a second number of clock cycles subsequent to beginning to apply the first staircase waveform to the well structure, applying the first staircase waveform beginning with the initial level to the control gates of the source side select gates for the remainder of the first number of clock cycles.

15

 10. The method of claim 9, further comprising:

 setting word lines corresponding to memory cells selected for erase to a low voltage level, wherein the word lines run in horizontal relative to the substrate.

20 11. The method of claim 10, wherein the low voltage level is ground.

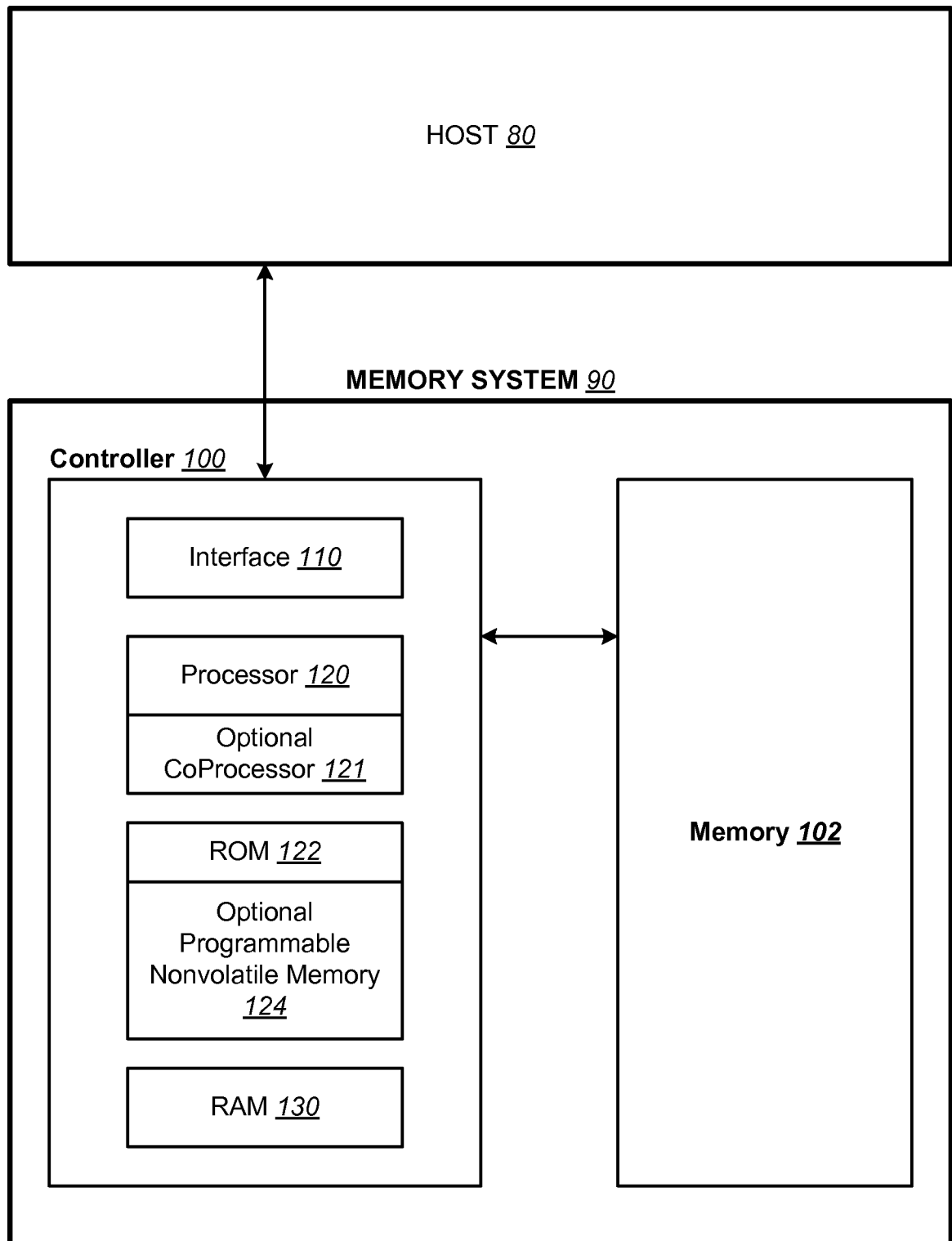
 12. The method of claim 10, wherein the monolithic three-dimensional non-volatile semiconductor memory device includes one or more dummy word lines not used for the storage of user data adjacent to one or both of the source side and drain
25 side select lines, wherein when performing the erase operation on the strings, the dummy word lines are set to float.

 13. The method of claim 9, wherein the stings include one or both of multiple source side select gates connected in series and multiple drain side select gates
30 connected in series.

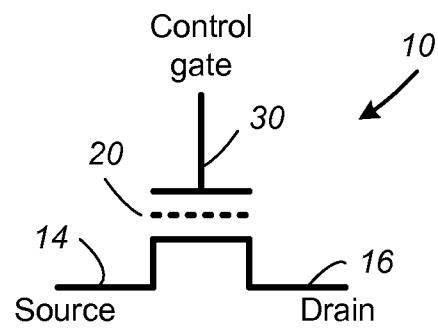
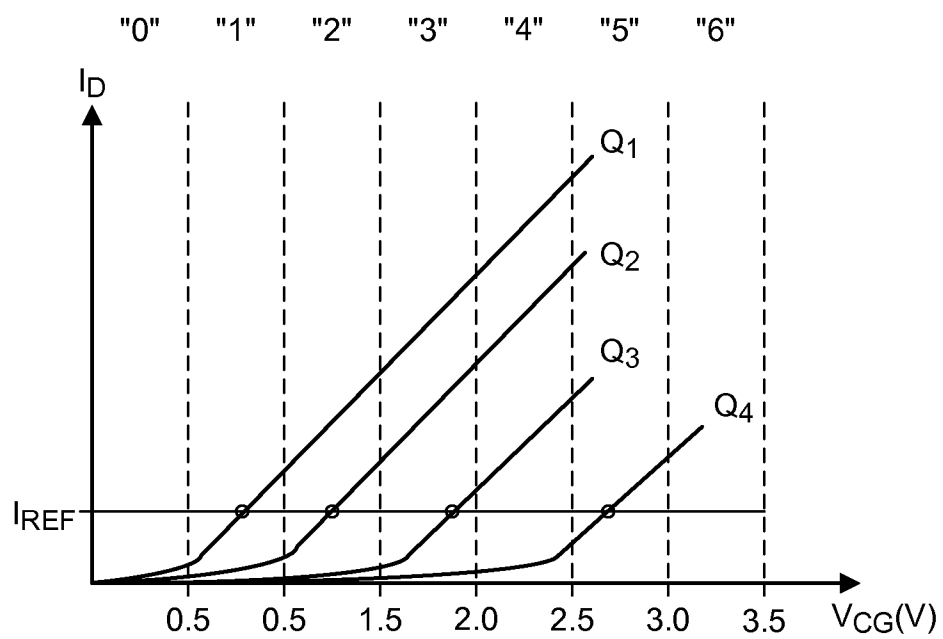
 14. The method of claim 9, wherein the frequency of the clock signal decreases after a third number of cycles subsequent to beginning to apply the first staircase waveform to the well structure.

35

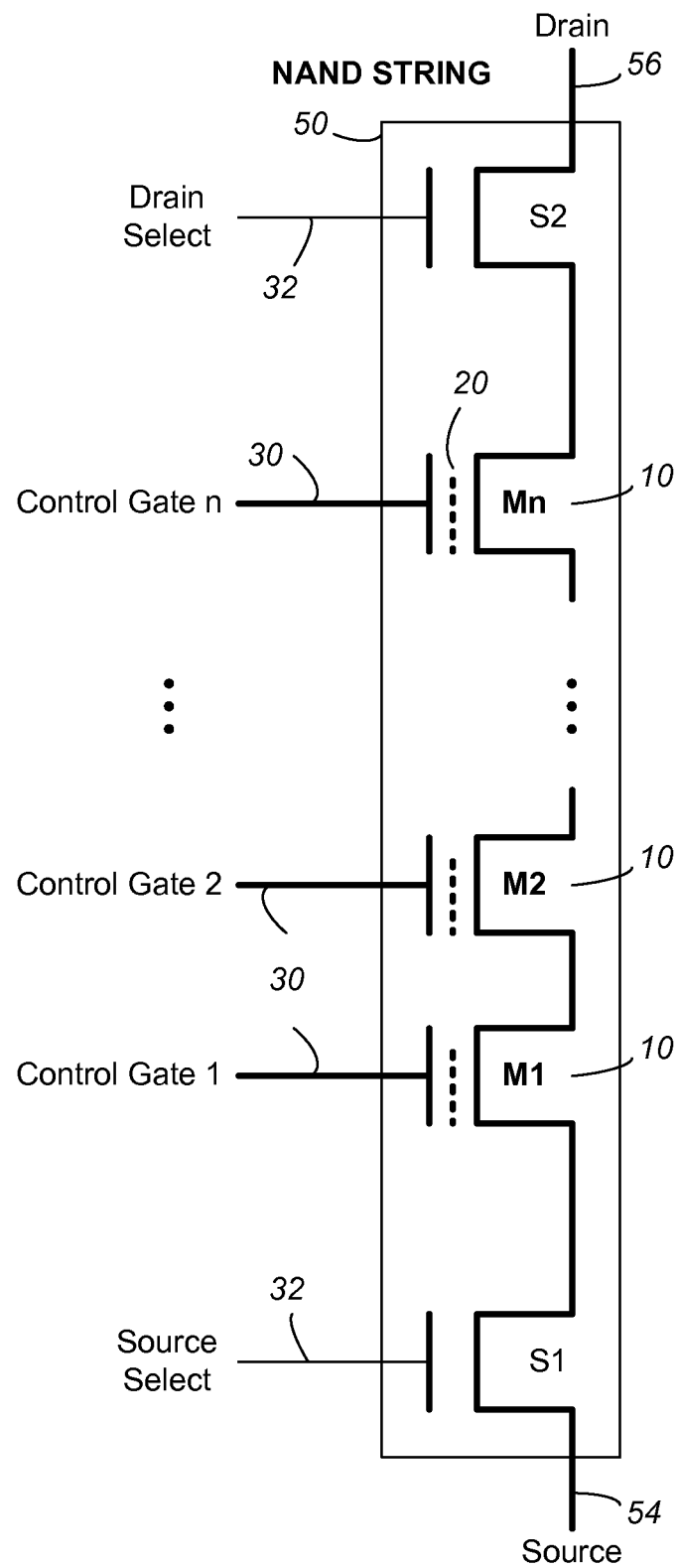
1 / 21

**FIG. 1**

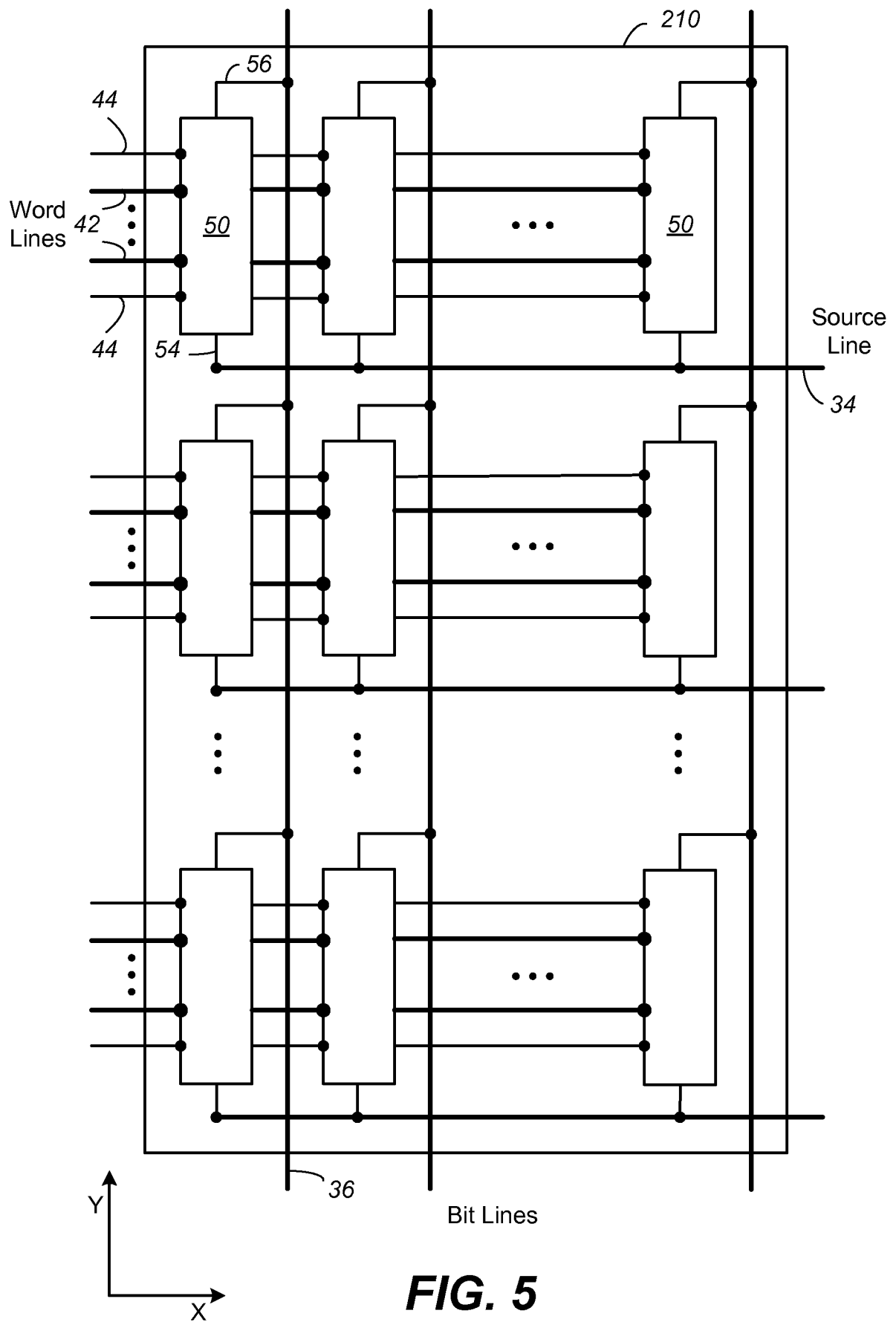
2 / 21

**FIG. 2****FIG. 3**

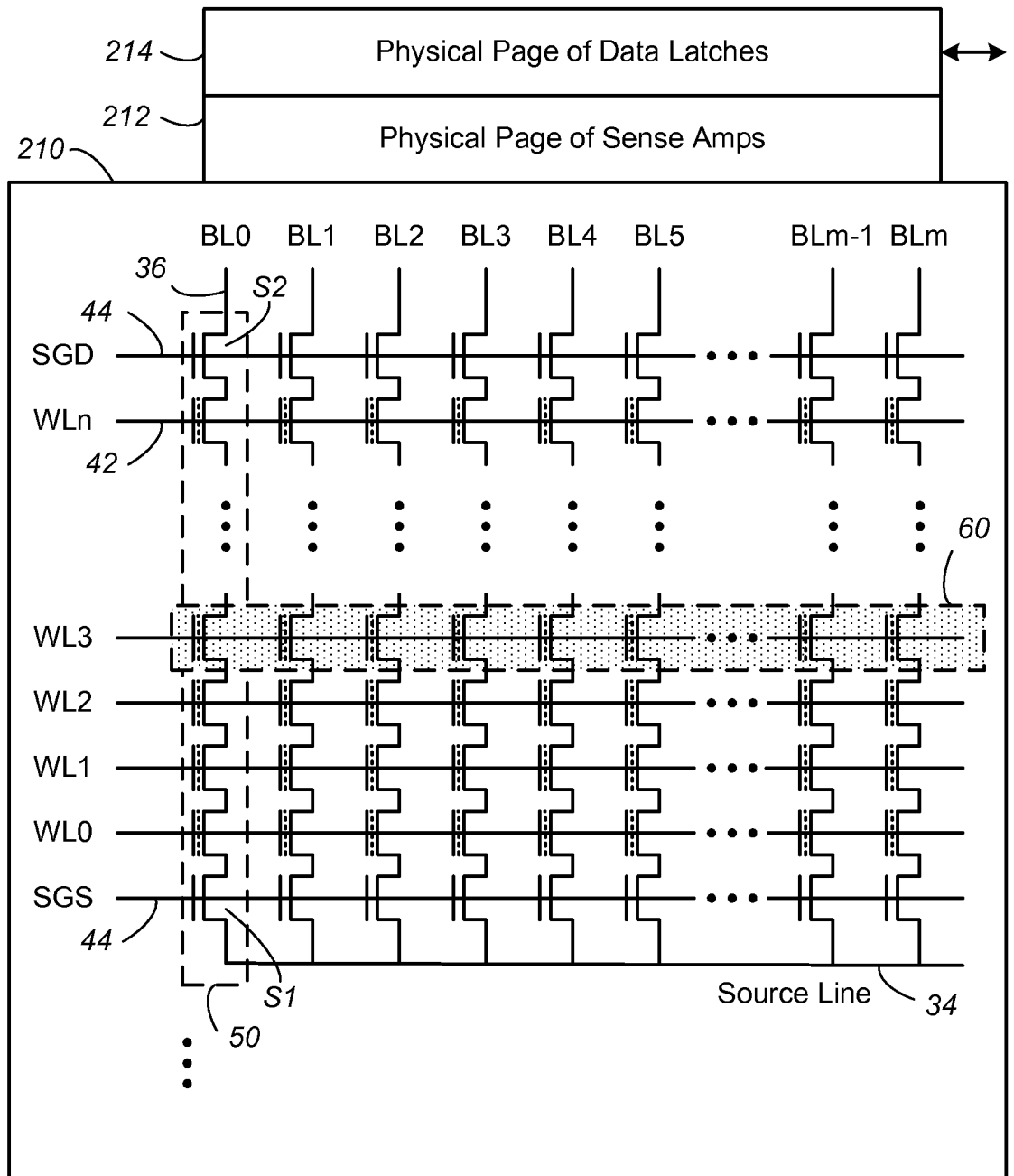
3 / 21

**FIG. 4**

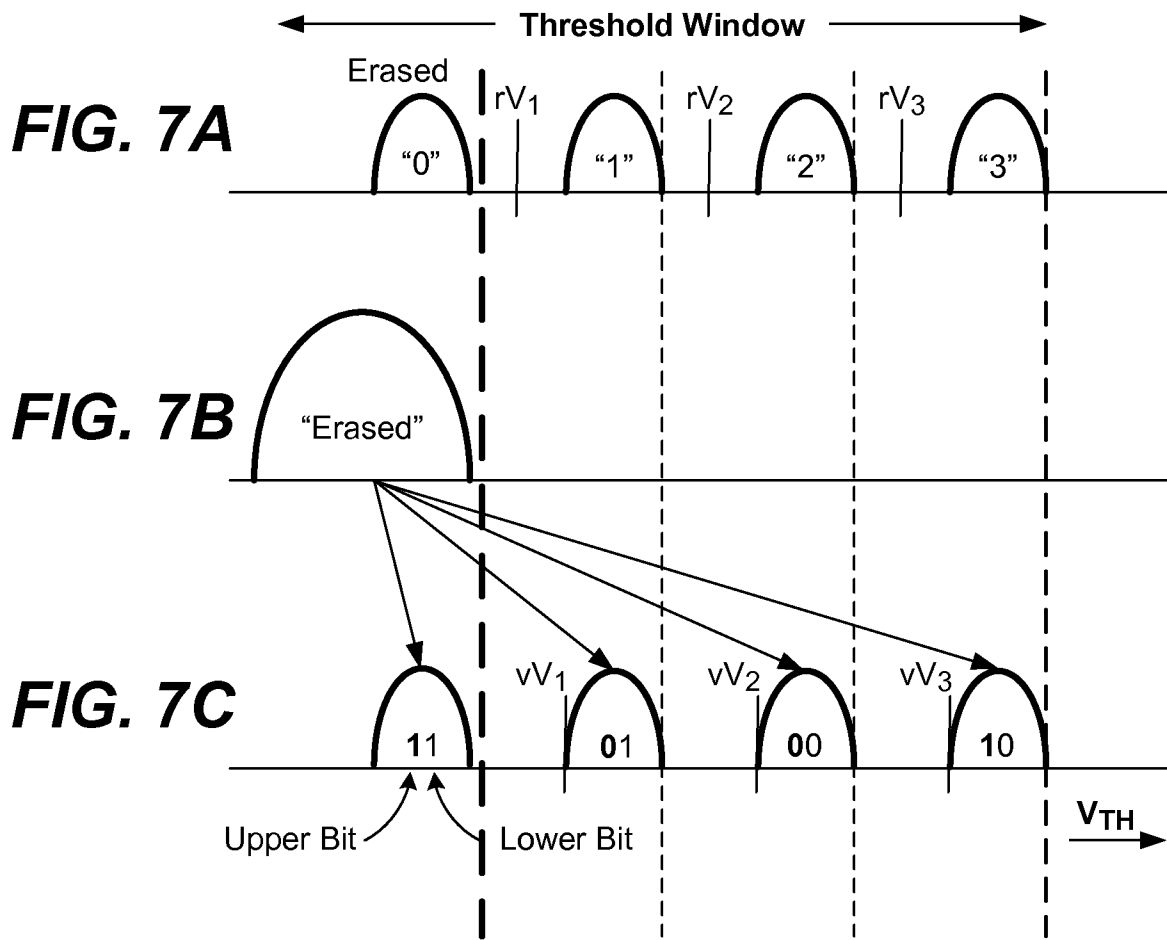
4 / 21

**FIG. 5**

5 / 21

**FIG. 6**

6 / 21



Programming into four states represented by a 2-bit code

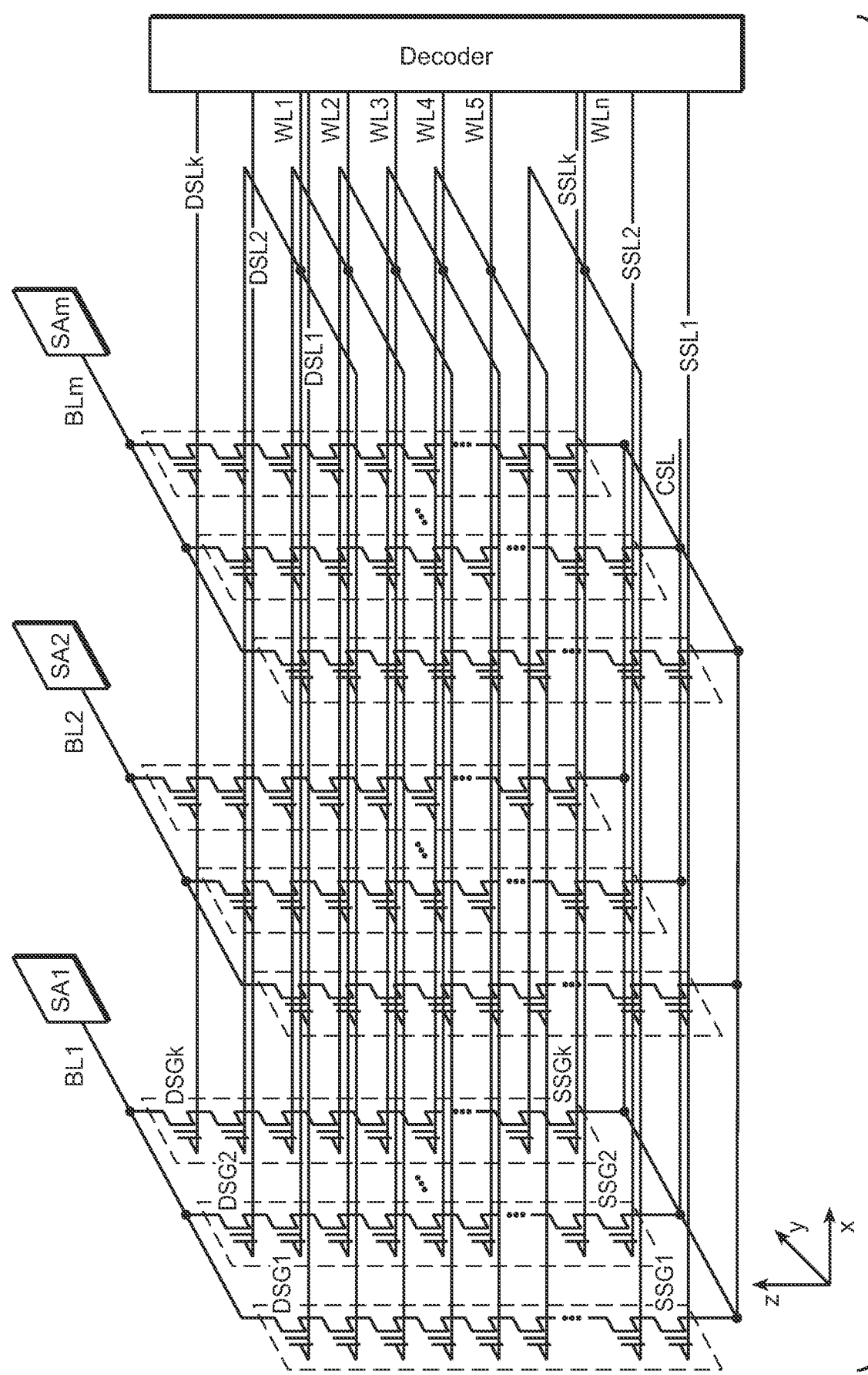


FIG. 8

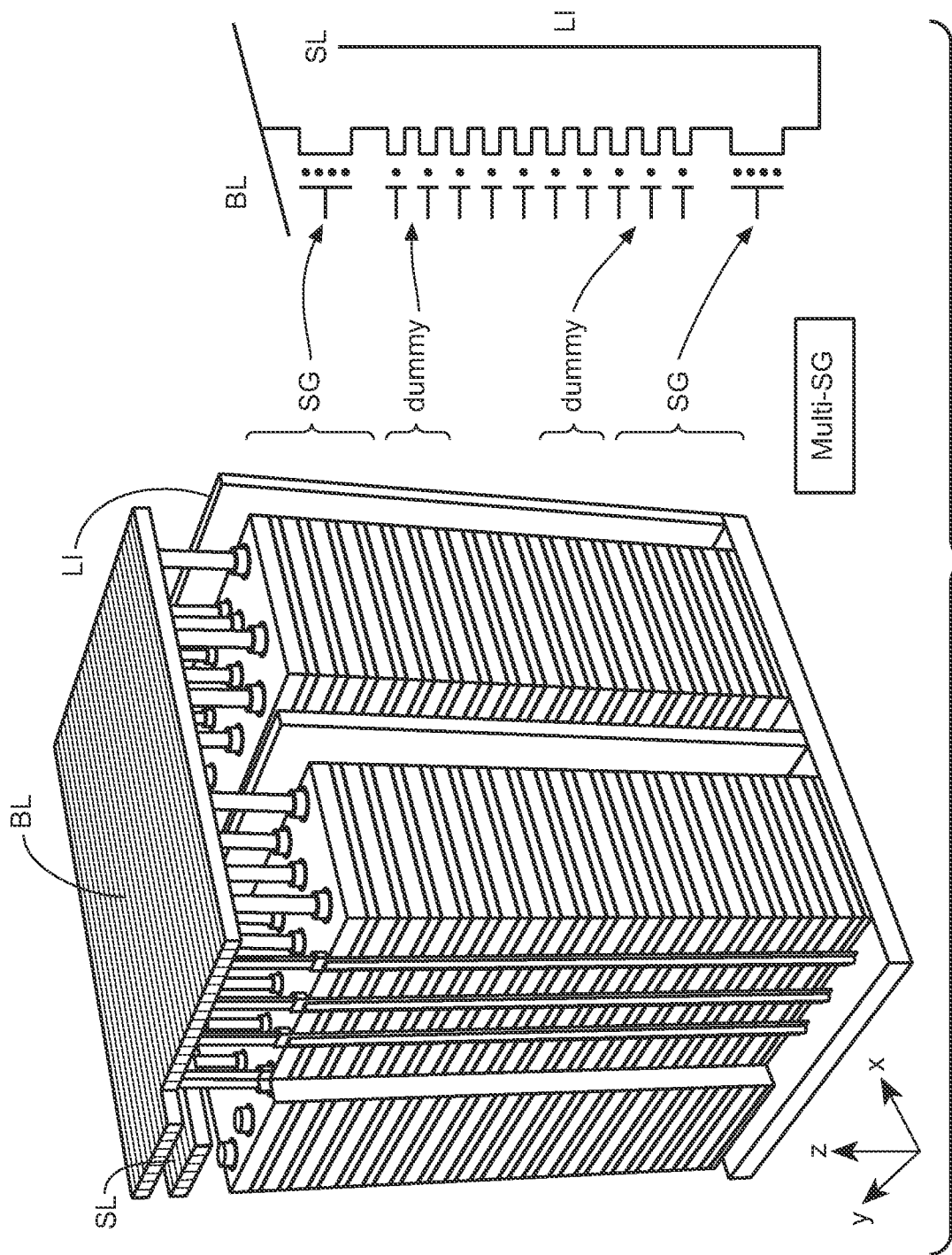


FIG. 9

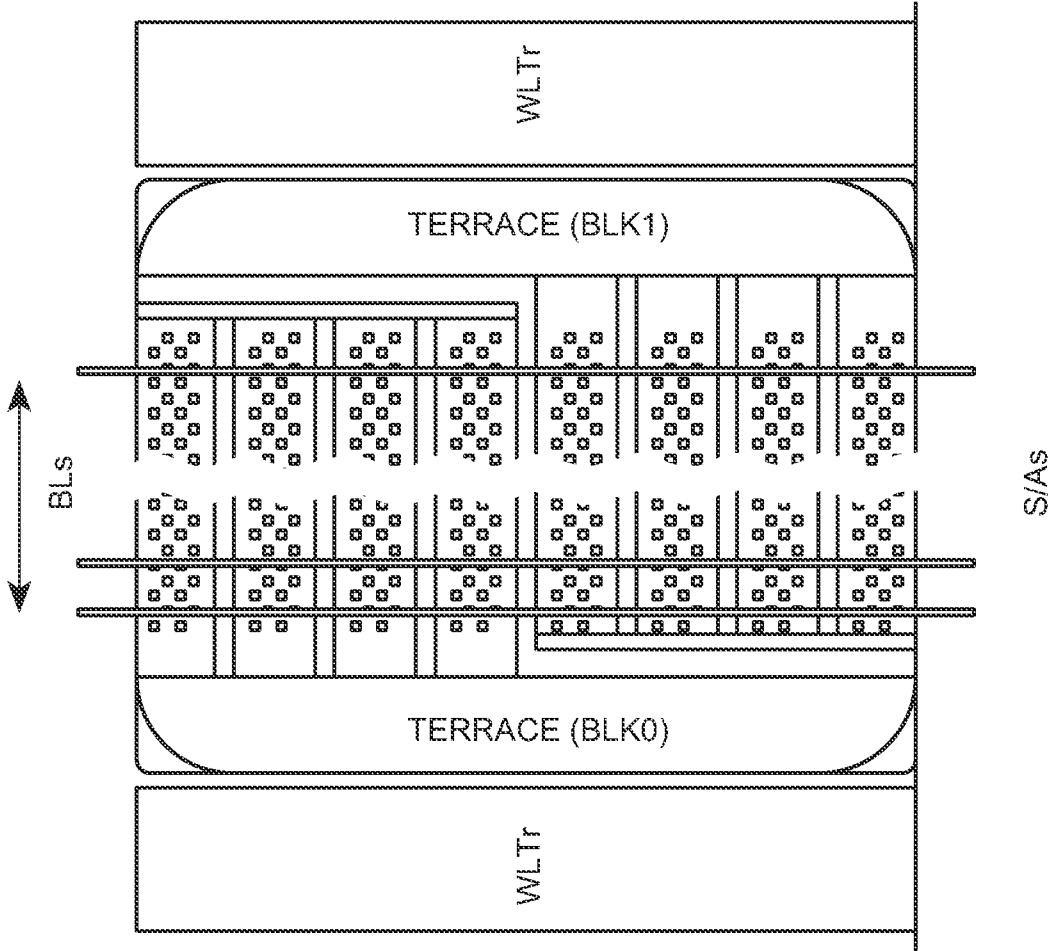


FIG. 10

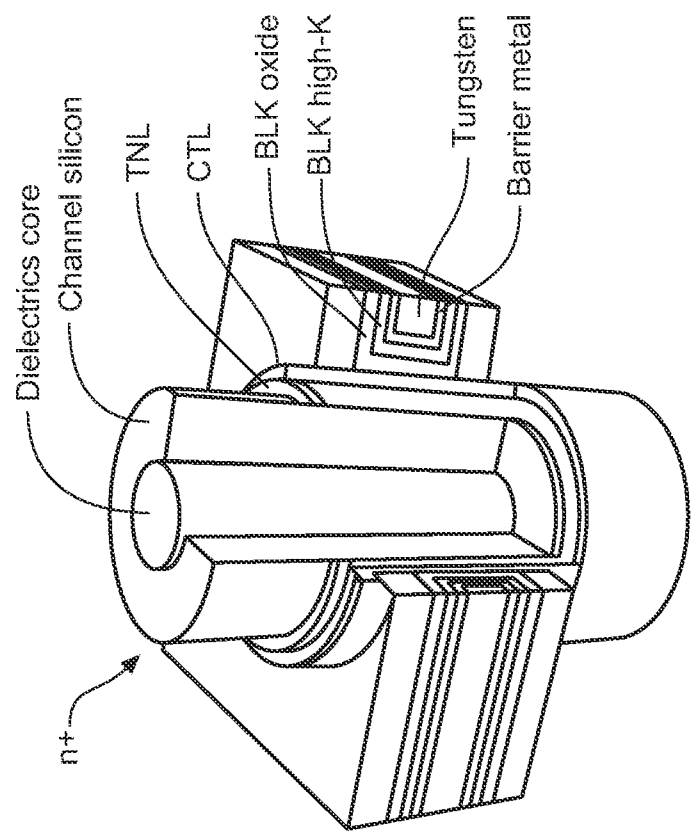


FIG. 12

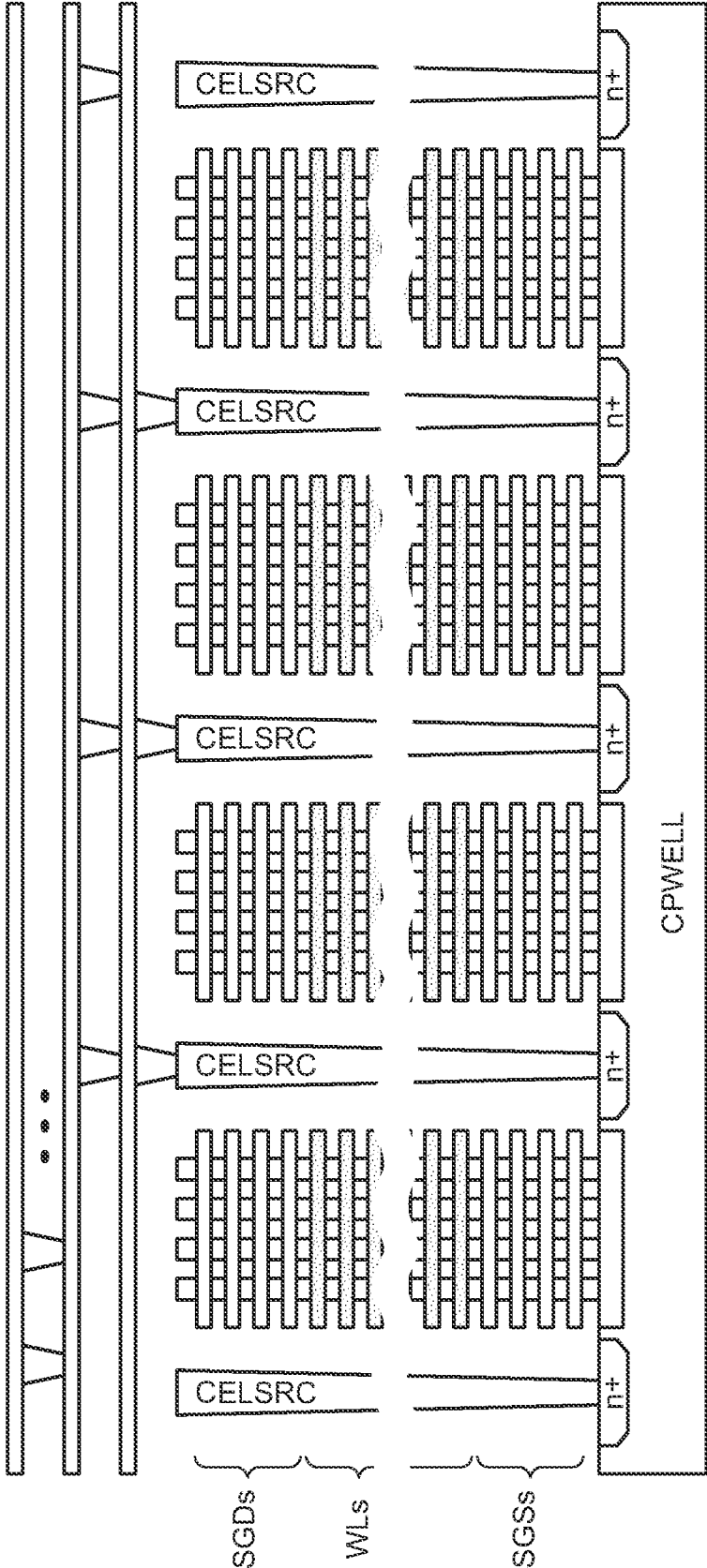


FIG. 11

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FIG. 13

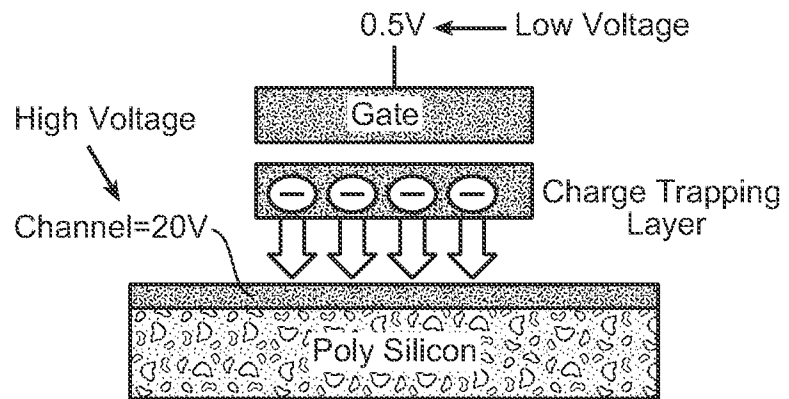


FIG. 14A

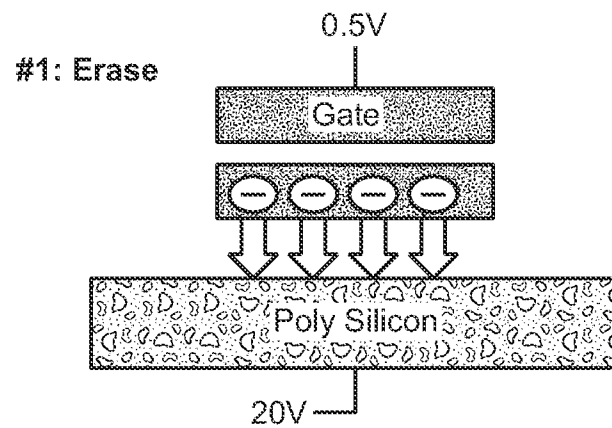
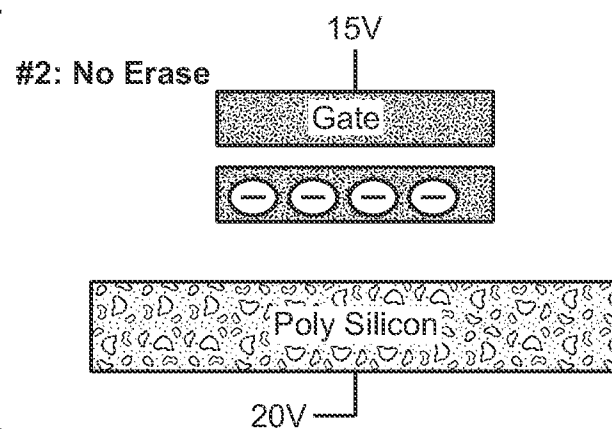


FIG. 14B



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FIG. 14C

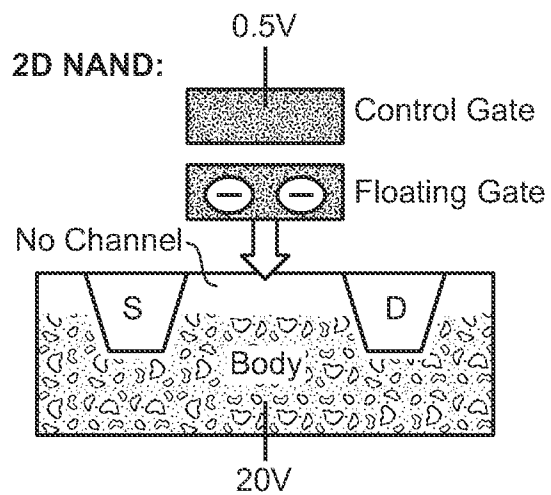
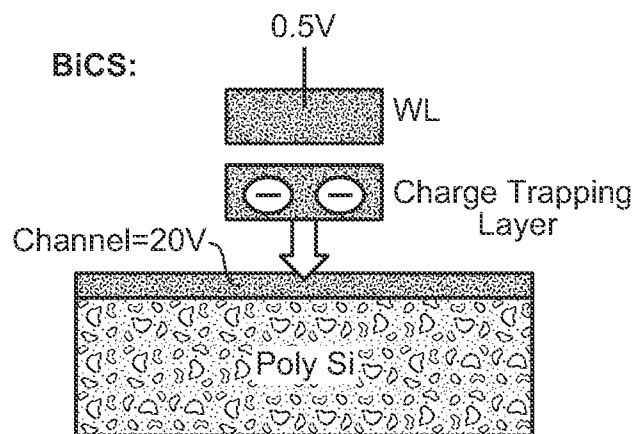
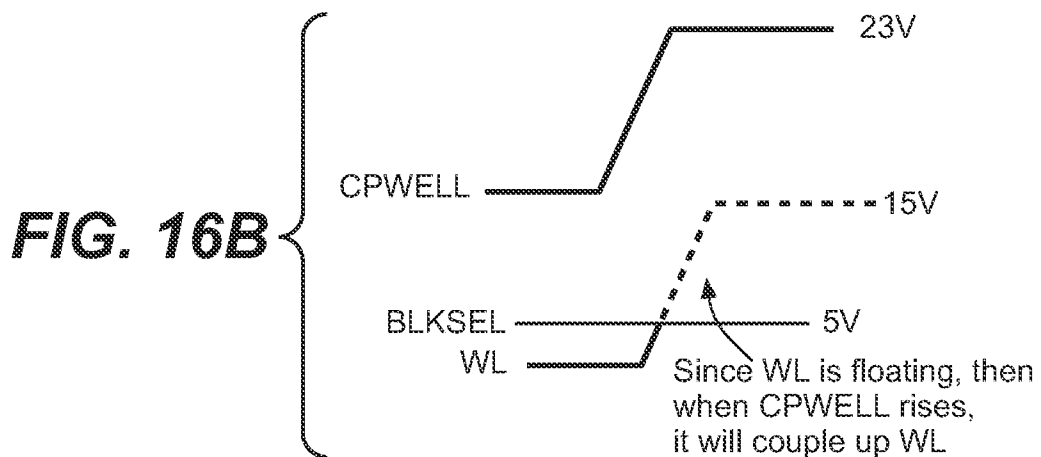
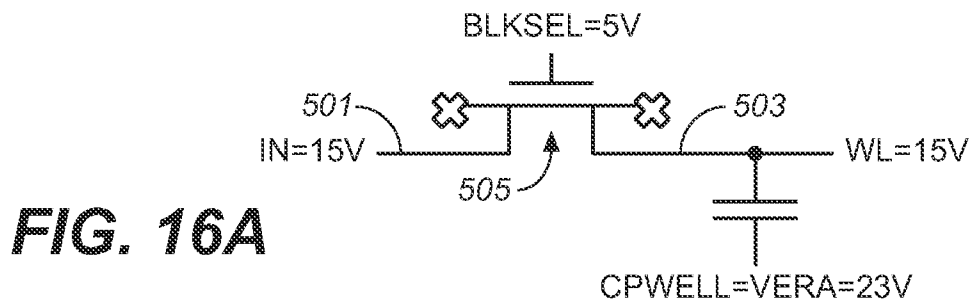
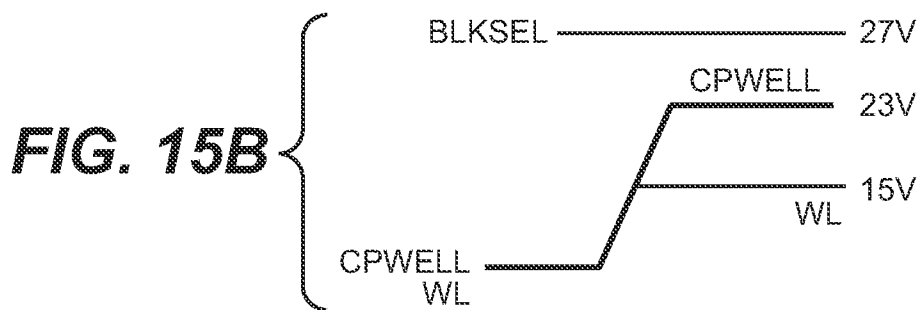
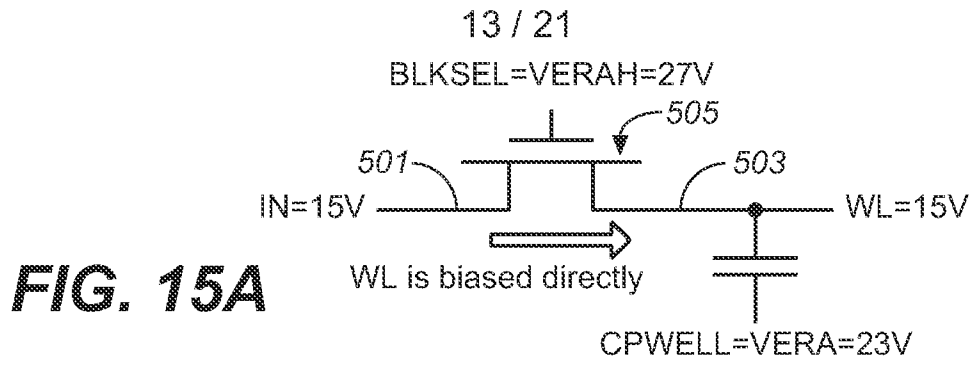


FIG. 14D





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Memory Hole

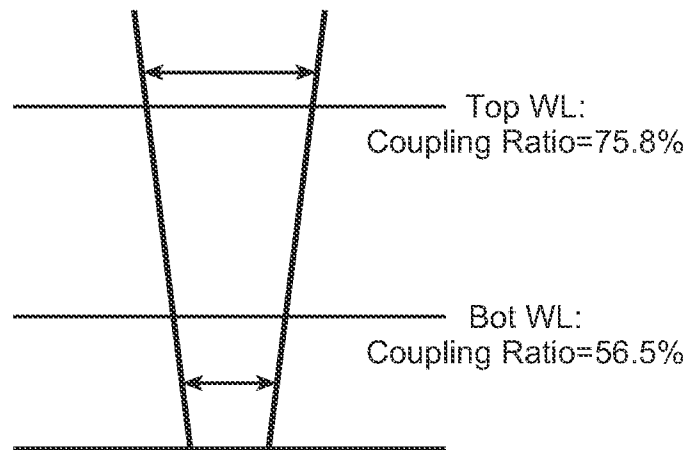


FIG. 17

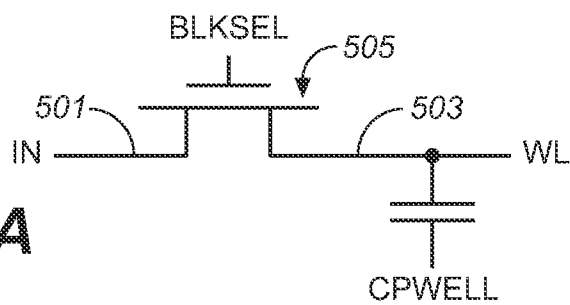


FIG. 18A

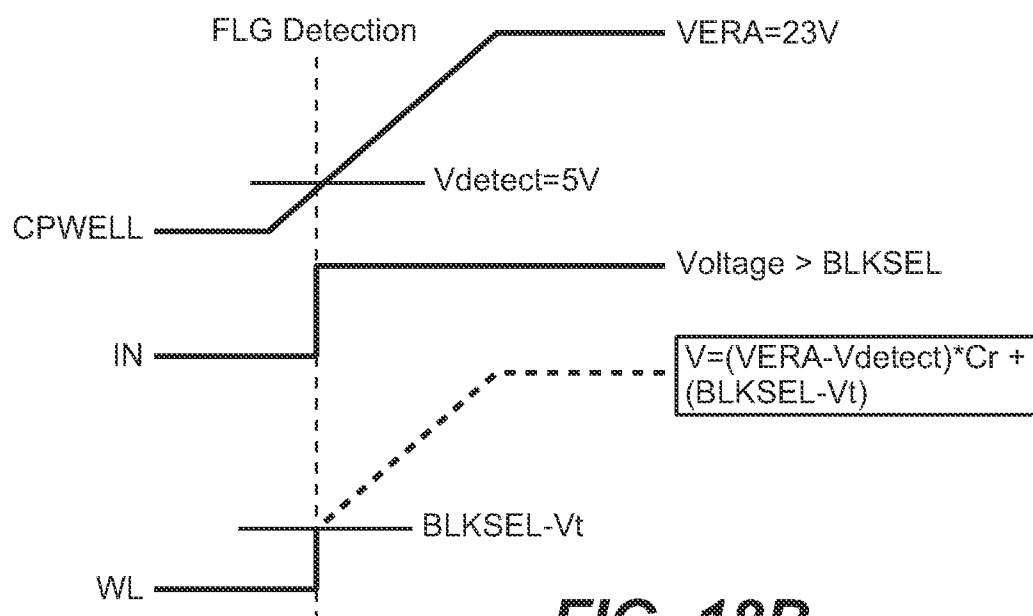
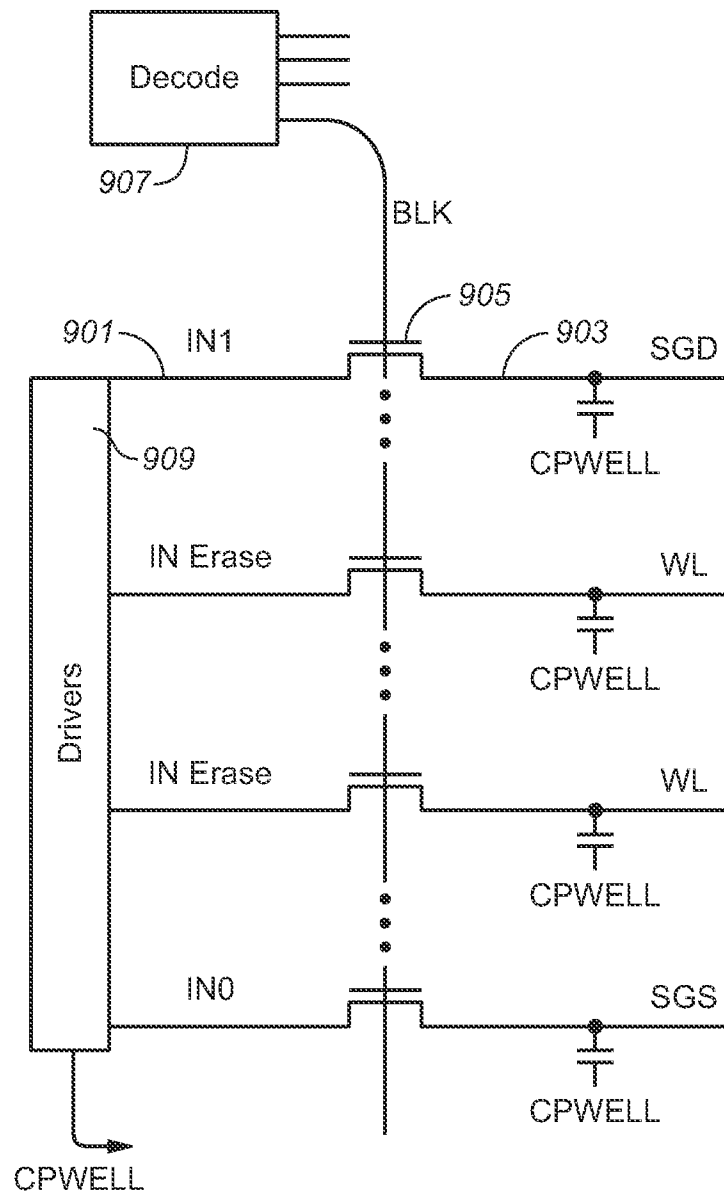


FIG. 18B

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**FIG. 19A**

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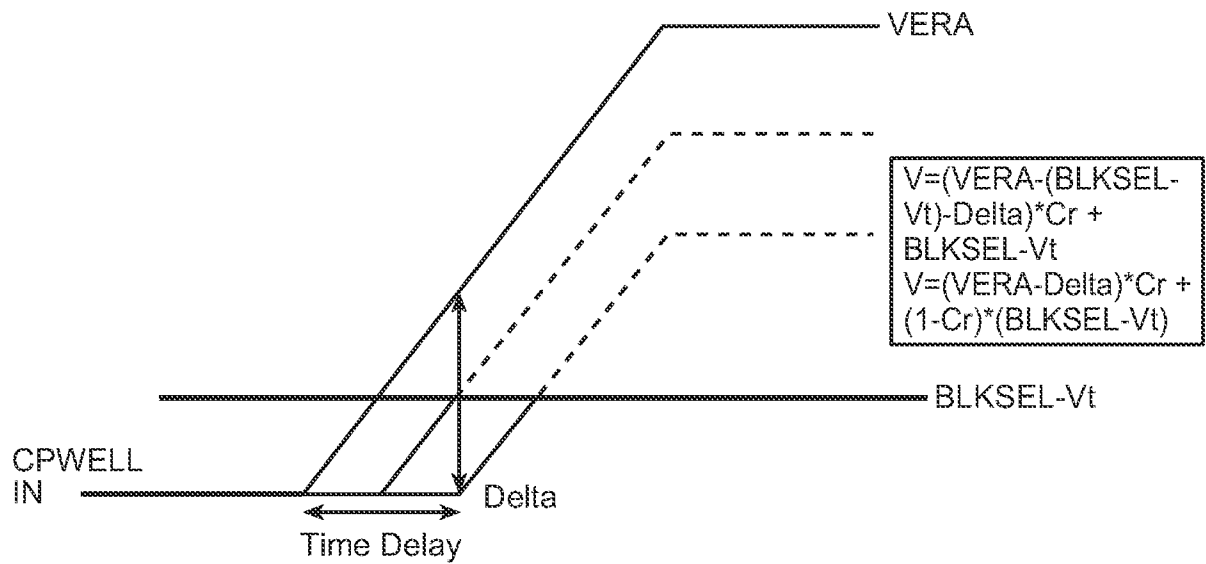


FIG. 19B

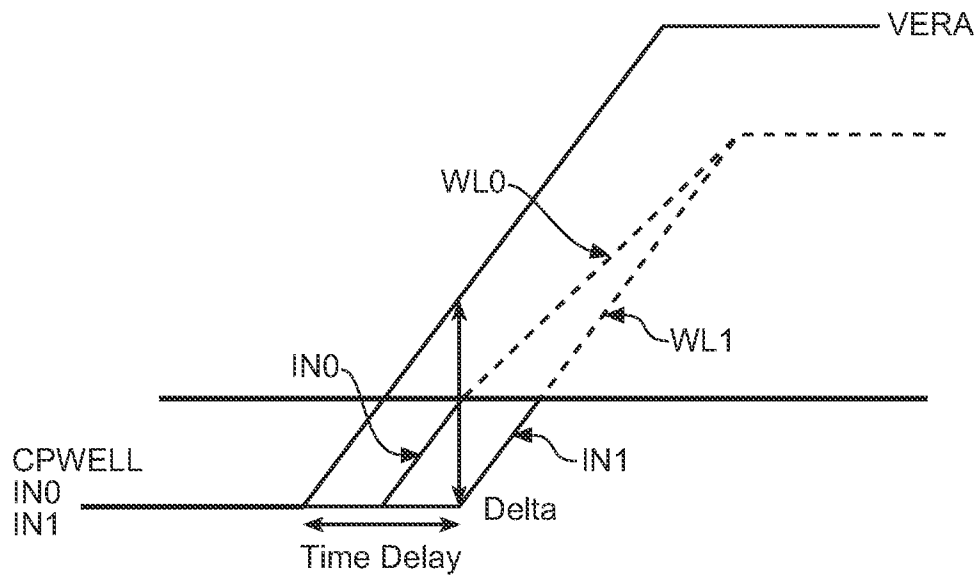


FIG. 19C

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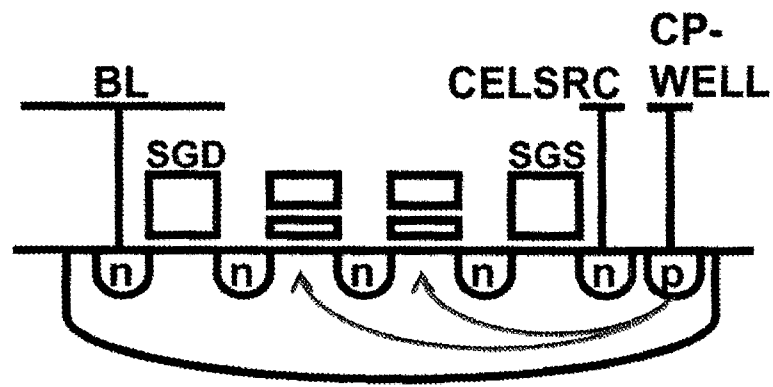


FIG. 20

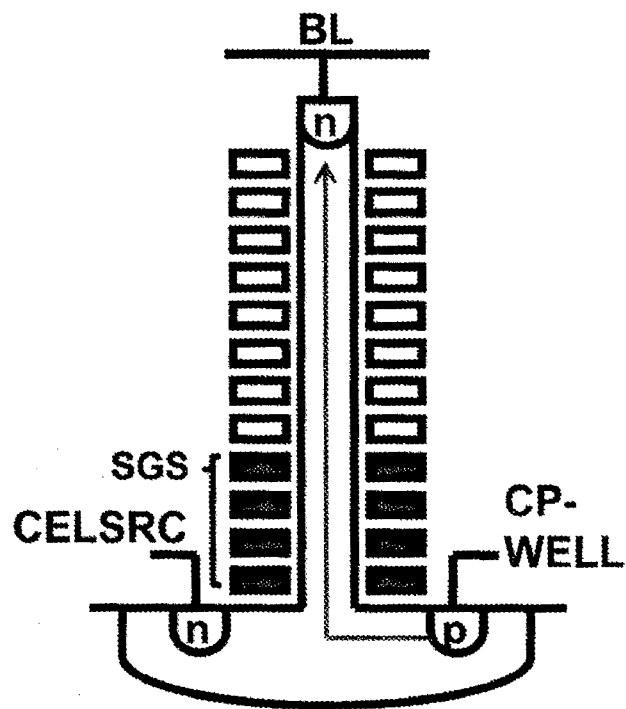


FIG. 21

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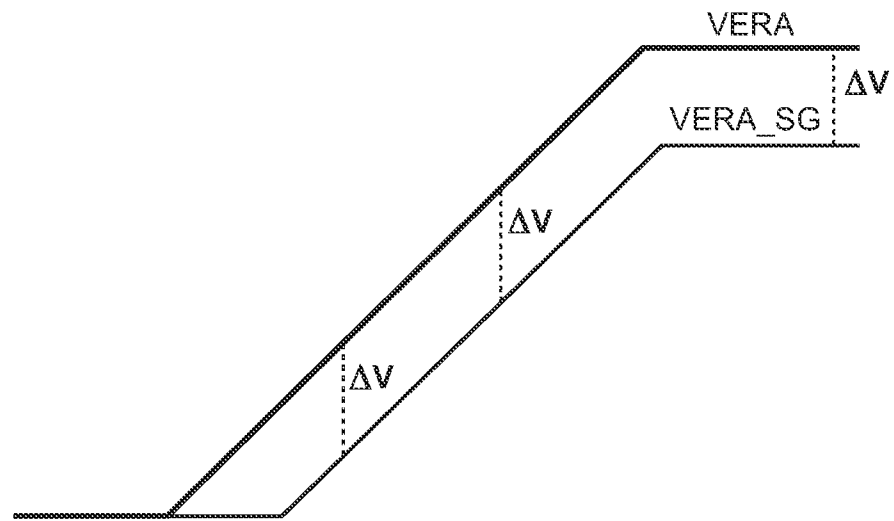


FIG. 22

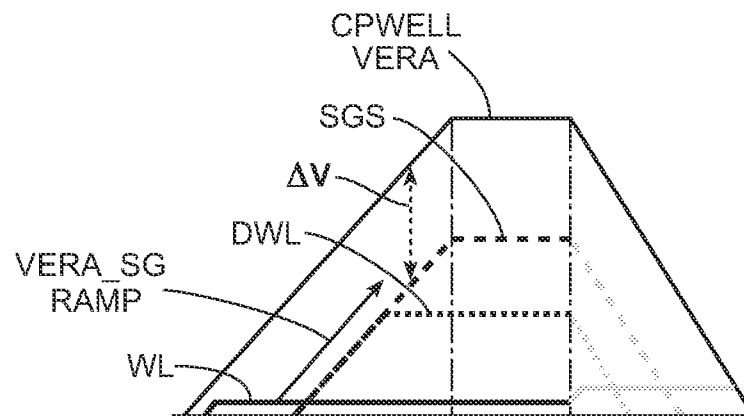
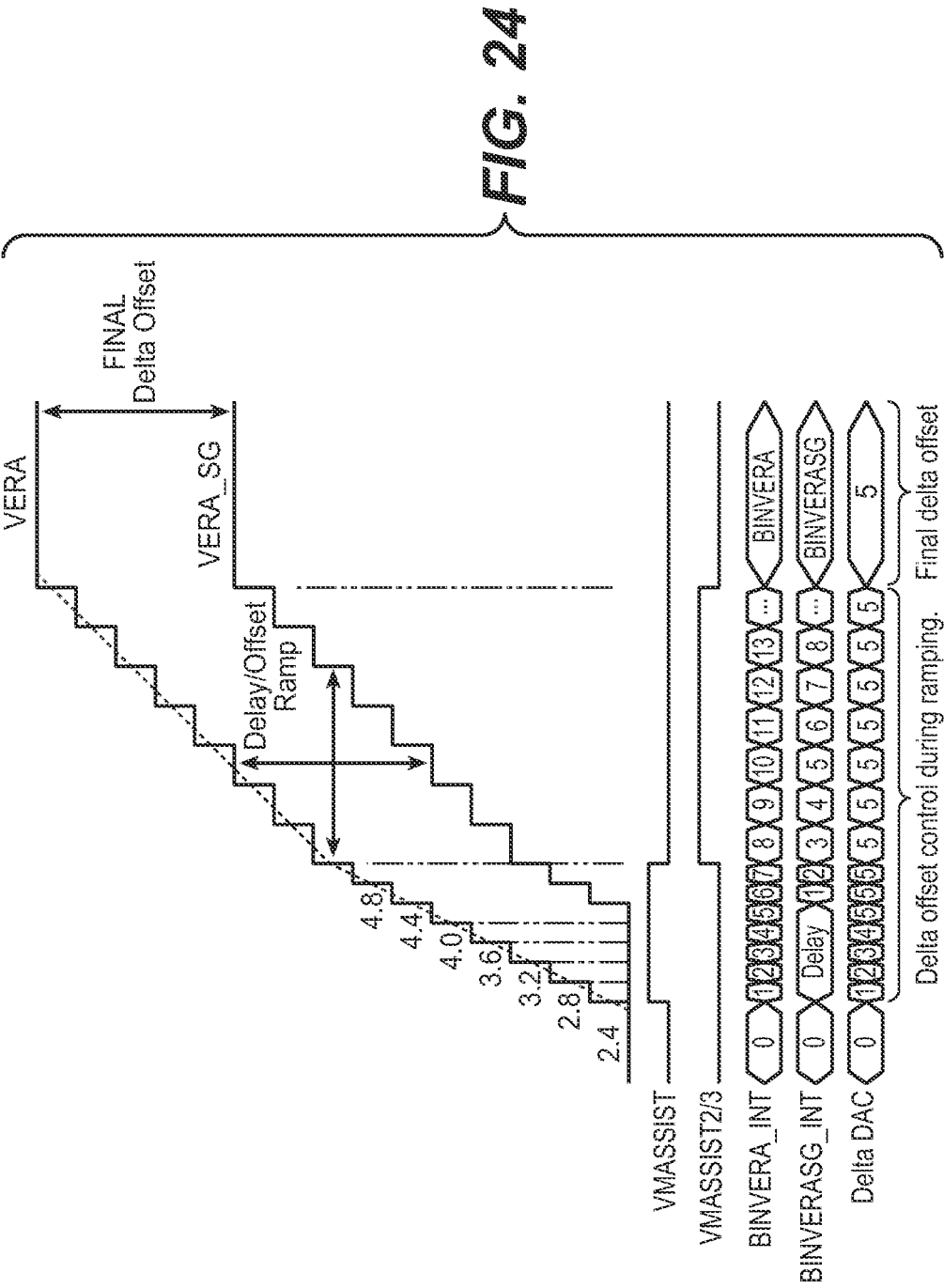
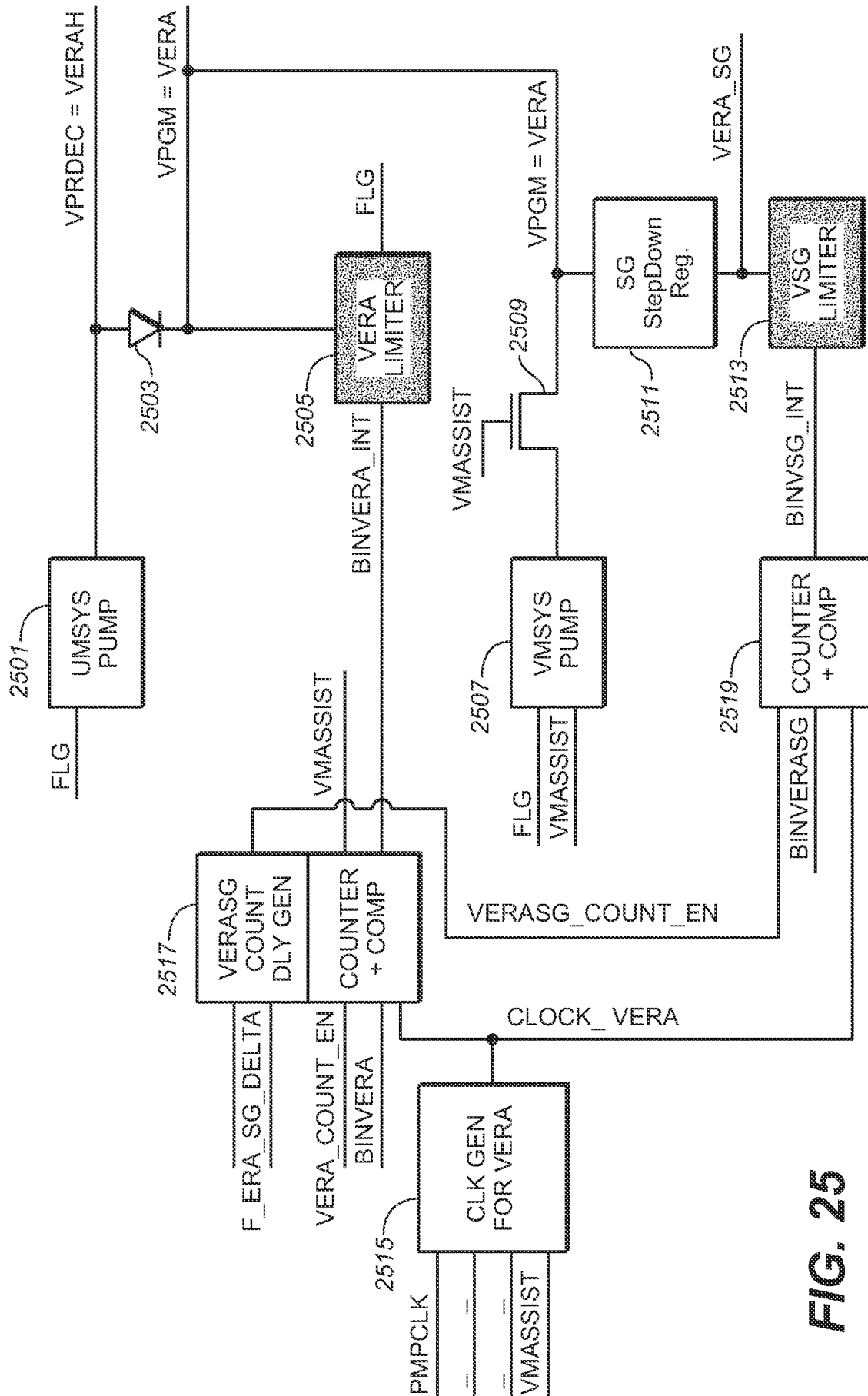
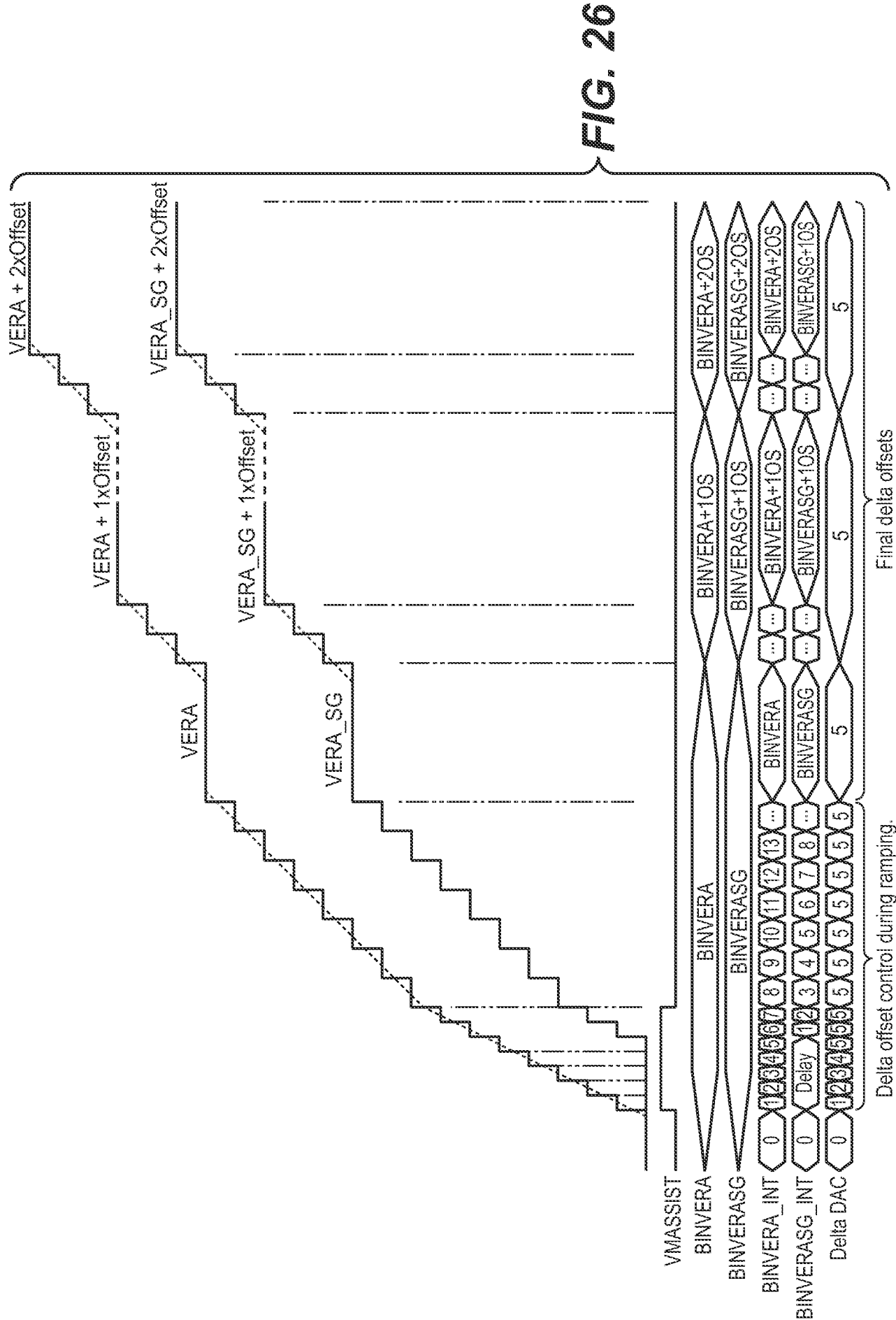


FIG. 23







INTERNATIONAL SEARCH REPORT

International application No

PCT/US2015/061149

A. CLASSIFICATION OF SUBJECT MATTER

INV. G11C16/16 G11C16/32
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2012/120740 A1 (SHIM SUNIL [KR] ET AL) 17 May 2012 (2012-05-17) paragraph [0083] - paragraph [0103]; figures 4,5,7 paragraph [0181] - paragraph [0192]; figure 15	1-14
A	----- US 2011/188321 A1 (KITO MASARU [JP] ET AL) 4 August 2011 (2011-08-04) paragraph [0079] - paragraph [0096]; figures 1A-1D -----	1-14



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"E" earlier application or patent but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search

14 January 2016

Date of mailing of the international search report

22/01/2016

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Authorized officer

Knack, Steffen

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2015/061149

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		US 2012120740 A1	17-05-2012

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		JP 2011159362 A	18-08-2011
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