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(54) Title: MULTIPLE SINGLE LAYER MONOLITHIC PASSIVE INTEGRATED CIRCUITS AND METHOD

(57) Abstract

Integrated circuits and the method of making same are disclosed which are suitable for use in integrated circuits such as amplifiers, filters and oscillators. Each integrated circuit includes using a main dielectric body that has a thin conductive layer (12) on opposite faces, using conventional etching process to etch out selected spaces or gaps (15, 16) in the layers according to a preselected pattern and cutting through the body to form oblong shaped bodies that form the integrated circuit. These circuits have conductive plates and spaces between plates on both sides with opposite plates providing capacitors connected mechanically and electrically and square shaped sections connected between plates of selected conductive materials which function as resistors and inductors.
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MULTIPLE SINGLE LAYER MONOLITHIC PASSIVE INTEGRATED CIRCUITS AND METHOD

Technical Field

This invention relates to integrated circuits and more particularly to passive integrated circuits particularly suited for RF and microwave use and the method of making same.

Background Art

In the past passive integrated circuits particularly suitable for radio frequency RF and microwave use have included capacitors, inductors, resistors and a combination of each. Such integrated circuits with capacitors have problems of circuit parasitics and a relatively high effective series resistance that places a limit on the Q of the circuit and have had problems of reaching high frequencies as on the order of 6-8GHz.

Integrated circuits having capacitors and heretofore known as multiple layer ceramic chip caps have opposed, interleaved, parallel plates with a layer of ceramic between the plates serving as a dielectric. Capacitors known as a single layer have a ceramic body with a conductive layer on the top face and a conductive layer on the bottom face.

Yamagiwa et al. U.S. Patent No. 4,306,274 and DeVoe et al. U.S. Patent No. 5,367,430 are examples of prior art monolithic passive capacitors but have a different structure and a different method of making from that of the present invention.

Disclosure of the Invention

A multiple single layer monolithic passive integrated circuits and method of making same disclosed includes the steps of providing a main dielectric body
with thin flat conductive layers on opposite faces, etching spaces in the layers along preselected spaced lines to form a plurality of plates with spaces between plates and cutting through the body along preselected lines to provide a plurality of identical integrated circuits. Each circuit has a selected plate height and width and a selected gap or spacing between the plates. Resistors and inductors in the form of squared wave shaped strips connected between the plates are provided in a further embodiment.

Brief Description of the Drawings
Details of this invention are described in connection with the accompanying drawings which like parts bear similar reference numerals in which:

Figure 1 is a top plan view of a main dielectric body after the etching has been accomplished to in a preselected pattern remove a portion of the top and bottom layers from the main body.

Figure 2 is an enlarged top plan view of a portion within the circle shown in Figure 1.

Figure 3 is an enlarged top plan view of one of the circuits that is cut from Figure 2 embodying features of the present invention.

Figure 4 is a side elevation view of the circuits shown in Figure 3 with the opposite side being an identical mirror image.

Figure 5 is an enlarged bottom plan view of the circuit shown in Figure 3.

Figure 6 is an enlarged bottom plan view of a portion of the body within the circle of Figure 2 showing the opposite bottom face.

Figure 7 is a schematic diagram of the circuit shown in Figures 3, 4 and 5.

Figure 8 is a top plan view similar to Figure 3 of another embodiment of a circuit embodying features of
the present invention.

Figure 9 is a side elevation view of the circuit of Figure 8.

Figure 10 is a bottom plan view of the circuit of Figure 8.

Figure 11 is a schematic diagram of the circuit shown in Figures 8-10.

Figure 12 is a top plan view similar to Figure 3 of another embodiment of a circuit embodying features of the present invention.

Figure 13 is a side elevation view of the circuit of Figure 12.

Figure 14 is a bottom plan view of the circuit of Figure 12.

Figure 15 is a schematic diagram of the circuit of Figures 12-14.

Figure 16 is a top plan view of yet another embodiment of circuit similar to Figure 3 embodying features of the present invention.

Figure 17 is a side elevation view of the circuit of Figure 16.

Figure 18 is a bottom plan view of the circuit of Figure 16.

Figure 19 is a schematic diagram of the circuit of Figures 16-18.

Figure 20 is a top plan view of yet another embodiment of a circuit embodying features of the present invention.

Figure 21 is a side elevation view of the circuit shown in Figure 20.

Figure 22 is a bottom plan view of the circuit shown in Figure 20.

Figure 23 is a schematic diagram of the circuit of Figures 20-22.
Detailed Description

Referring now to Figure 1 there is shown a flat surfaced, main dielectric body 11 of a rectangular shape having a selected height, width and thickness dimensions. Body 11 preferably is a ceramic body. Initially, the dielectric body 11 is plated on the flat top and bottom surfaces so as to have a thin, conductive top layer 12 and a thin, conductive bottom layer 13 that covers almost the entire surface area of the top and bottom surfaces of body 11.

A conventional thin film process presently used for making integrated circuits is used to form the pattern of interspersed conductive elements and non-conductive gaps described hereinafter. In this process a photoresist material is applied to the conductive top layer 12 and a photoresist material is applied to the conductive bottom layer 13. The top layer 12 is exposed using a pattern or art work of a selected configuration. The bottom layer 13 is exposed using a pattern or art work of a selected configuration. An etching process is applied to the top and bottom layers which is used to remove portions of the conductive layer. In the top layer 12 seen in Figure 2 there is shown etched out vertical strips or gaps 15, 16 and 17 along parallel, spaced vertical lines of a preselected spacing and along parallel, spaced horizontal lines 18 at equal spacing. A pattern of etched out vertical gaps 15, 16 and 17 along parallel spaced vertical lines is repeated laterally of the dielectric body from left to right to the right side edge of top layer 12.

In the bottom layer 13 shown in Figure 6 there is provided etched out vertical gaps 21 and 22 along preselected parallel spaced vertical lines and a plurality of equally spaced etched out horizontal gaps 23. Vertical gap 17 is located directly opposite vertical gap 22. Horizontal gap 18 is located directly
opposite horizontal gap 23.

Cuts are then made through the body using a single saw blade. Beginning at the upper left hand corner the top layer 12 as shown in Figure 2 the first vertical cut by the blade would be along left side edge 25 of the top layer 12 and along the first etched gap 17 proceeding from left to right. The horizontal cut would be along the top edge 26 of the top layer 12 and along the uppermost etched gap 18. With reference to Figure 6 this vertical cut would be along the right side edge 27 of the bottom layer 13 and along the first etched gap 22 proceeding from left to right. The above described first horizontal cut would be along the top edge 28 of the bottom layer and along the uppermost etched gap 23.

These vertical cuts are repeated through each successive etched gaps 17 and 22 proceeding from left to right in Figure 2 and the horizontal cuts are repeated through successive etched gaps 18 and 23 from top to bottom.

Referring now to Figures 3-5 each integrated circuit 29 resulting from the above described process is identical. A typical dimension is 30 mil. by 60 mil. Each circuit 29 is in the form of an oblong block having a plate A provided by a portion of the above described top layer 12 of a selected height designated h and width designated w on the top face of an oblong body 11. A plate B of a selected height and selected width is separated from plate A by a strip or gap 15 and a plate C of a selected height and width is separated from plate B by gap 16. Similarly, a plate D is provided by a portion of the above described bottom layer 13 of a selected height and selected width is on the bottom face of body 11 and a plate E of a selected height and selected width is separated from plate D by gap 21. Plates A, B and C are opposite plate D to form capacitors C1, C2 and C3, respectively, and plate C is opposite plate E to form
capacitor C4. The schematic diagram of circuit 29 is shown in Figure 7. Circuit 29 is essentially a "T" circuit which includes capacitors C1 and C2 in series with one another in a top leg and capacitor C3 and capacitor C4 in series with one another in a bottom leg. One end of the other leg is connected to a common junction between capacitors C1 and C2 and plate D. Plate C is common to capacitors C3 and C4 at a terminal.

The variables for the above described integrated circuit capacitors and method of making are:
1. to change the thickness of the substrate, 2. change the dielectric constant of the body, 3. change the width of the plate, and 4. change the height of the plate. The capacitors are then mechanically joined by how the cut pattern is selected and electrically joined by selecting the width of the pattern of the layers.

Referring now to Figures 8-11 there is shown another embodiment of an integrated circuit 30 in the form of an oblong block having conductive plates K, L, M and N, on the top face of an oblong body 11 and conductive plates N, O and P on the bottom face of body 11. There is a gap 31 between plates K and L and a gap 32 between plates L and M. There is a gap 33 between plates N and O and a gap 34 between plates O and P. Plate M is opposite plate B to form capacitor C1', plate L is opposite plate P to form capacitor C2', plate P is opposite plate K to form capacitor C3', plate K is opposite plate O to form capacitor C4' and plate K is opposite plate N to form capacitor C5'. The schematic diagram for circuit 28 is shown in Figure 11 has capacitors C1', C3' and C5' connected in what is commonly referred to as a "pie" network in that they are connected in a closed loop with a series capacitor C2' and a series capacitor C4' connected at the ends of the "pie" network.

A terminal is shown at plate K.

Referring now to Figures 12-14 there is shown
another embodiment of an integrated circuit 37 having top
plates Q, R and S on the top face of an oblong body 11
and bottom plates T, U and V on the bottom face of an
oblong body 11. There is a gap 38 between plates Q and R
and a gap 39 between plates R and S. There is a gap 41
between plates T and U and a gap 42 between plates U and
V. These plates are of an equal dimension. Plate Q is
opposite plate T, plate R opposite plate U and plate S
opposite plate V. The schematic diagram of circuit 37
shown in Figure 15 has three parallel mechanically
connected capacitors that are not electrically connected
to one another.

Referring now to Figures 16-19 there is shown
another embodiment of integrated circuit 47 having a
single top plate S on the top face of an oblong body 11
and three bottom plates T, U and V on the bottom surface
of an oblong body 11. There is a gap 48 between plates X
and Y and a gap 49 between plates Y and Z. Plate W is
opposite plate X to form capacitor, plate W is opposite
plate Y to form capacitor C10 and plate W is opposite
plate Z to form capacitor C11. The schematic diagram for
circuit 47 shows three capacitors connected in parallel
as is shown in Figure 19.

Referring now to Figures 20-23 there is shown
another embodiment of an integrated circuit 57 having
both capacitors and impedances. Circuit 57 has
conductive top plates 61, 62 and 63 on the top surface of
oblong body 11 and conductive plates 64 and 65 on the
bottom face of oblong body 11. There is a space or gap
67 between plates 61 and 62 and a gap 68 between plates
64 and 65 with an open area 69 to the right of bottom
plate 65. Plate 63 is opposite plate 64 to form
capacitor C12 and plate 62 is opposite plate 65 to form
capacitor C13. In addition, there is provided an
impedance element X1 connected between plates 61 and 62
and an impedance element X2 connected between plates 62
and 63. The schematic diagram for circuit 57 is shown in Figure 23 as having a capacitor C12 connected to impedance X1 and capacitor C13 connected between impedances X1 and X2. These impedances may be a resistor by using a high resistance metal such as tantalum nitride (TaN) and an inductor could be formed by using the same shape as the resistor but a low resistance metal such as the same base metal as plate 61. These impedances X1 and X2 are formed by depositing a thin, flat layer of metal in a particular pattern as shown. The shape of the impedances shown are a straight, horizontal section, a raised section that extends up, horizontally and down, and a second straight horizontal section similar to a square wave. It is understood other shapes may be used.

The above described circuits are suited for RF and microwave use and are useful as a filter, amplifier, oscillator and the like. The advantages over the prior art are summarized as:

1. Tighter tolerance ±.05
2. Lower effective series resistance ESR
3. Multiple parts monolithically joined into one part
4. Higher operating frequencies of 6-8GHz as to 4GHz of prior art
5. Reduction of parasitic stray capacitance
6. Reduction in cost of about 6-8 to one per unit

Although the present invention has been described with a certain degree of particularity, it is understood that the present disclosure has been made by way of example and that changes in details of structure may be made without departing from the spirit thereof.
WHAT IS CLAIMED IS:

1. A method of making an integrated circuit comprising the steps of:
   providing a main dielectric body of a selected shape and height and width dimension with first and second thin flat conductive layers on opposite faces of said body,
   removing portions of said layers along a preselected pattern to form a plurality of opposed first and second plates and gaps between adjacent plates, and cutting through said body along preselected lines to form a plurality of identical integrated circuits.

2. A method as set forth in claim 1 including the steps of forming three of said first plates that are opposite one of said second plates to provide first, second and third circuit elements, one of said first plates opposite another of said second plates to provide a fourth circuit element and form a T schematic diagram having two legs with two circuit elements in series with one another in each of said legs.

3. A method as set forth in claim 1 including the step of forming one of said first plates opposite one of said second plates to form a first circuit element, forming a second of said first plates opposite one said second plate to form a second circuit element and forming a third of said first plates opposite three of said second plates to form third and fourth circuit elements connected in a pie network with said second and fourth circuit elements connected at ends of said pie network.

4. A method as set forth in claim 1 including the step of forming three of said first plates opposite
three of said second plates corresponding in size to said first plates to form three circuit elements and provide a schematic diagram of three elements arranged parallel to one another and not electrically connected to one another.

5. A method as set forth in claim 1 including the step of forming one of said first plates opposite three of said second plates to form three circuit elements connected in parallel to one another.

6. A method as set forth in claim 1 including the step of forming three of said first plates opposite two of said second plates to provide first and second circuit elements, forming a first reactive element between two of said first and second plates and forming a second reactive element connected between said second and third of said plates to form a schematic diagram having one side of the first and second circuit elements connected to one side of said first reactive elements and one side of second circuit element connected between said first and second reactive elements.

7. A method as set forth in claim 1 including the step of adding at least one layer of a selected shape between adjacent of said plates to form an impedance connected between said adjacent plates.

8. A method as set forth in claim 1 wherein said removing is by etching along selected spaced, parallel, horizontal lines and along selected spaced vertical lines and said cutting is along selected of said horizontal and vertical lines.

9. A method of making multiple single layer passive integrated circuits comprising the steps of:
providing a main ceramic body of a selected oblong shape and having selected height and selected width dimensions,

etching strips of said layers along a preselected pattern of spaced parallel horizontal lines and spaced parallel vertical lines to form a plurality of opposed first and second plates, and

cutting through said body with a saw blade along selected of said horizontal and vertical lines to form a plurality of identical circuits including a plurality of capacitors.

10. An integrated circuit having pre-selected multiple integrated circuits comprising:

a dielectric body having a selected shape, length, and width,

a plurality of thin, conductive first plates on a first face of said body, each said first plates being of a selected width and a selected height with a gap of a selected width between adjacent of each of said first plates,

a plurality of thin, conductive second plates on an opposite second face of said body, each said second plate being of a selected width and a selected length with a gap of a selected width between adjacent each of said second plates, each oppositely disposed of said first and second plates forming a circuit element with said circuit elements being mechanically joined by said body, at least one of said first and second plates being opposite more than one of the other of said first and second plates to provide a common plate to at least two opposite plates.

11. A circuit as set forth in claim 10 wherein said body is ceramic.
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12. A circuit as set forth in claim 10 wherein each of said circuit elements are a capacitor.

13. A circuit as set forth in claim 12 wherein one of said first and second plates are opposite three of the other of said first and second plates to form three circuit elements.

14. A circuit as set forth in claim 10 wherein three of said first plates are opposite one of said second plates to provide three circuit elements, one of said first plates is opposite another of said second plates to provide a fourth circuit element and form a T schematic diagram and having two legs with two circuit elements in series with one another in each of said legs.

15. A circuit as set forth in claim 10 wherein one of said first plates is opposite to one of said second plates to form a first circuit element, a second of said first plates is opposite one second plate to form a second circuit element and a third of said plates are opposite three of said second plates to form third, fourth and fifth circuit elements connected in a pie network with said second and fourth circuit elements connected at the ends of said pie network.

16. A circuit as set forth in claim 10 wherein each of said first plates is opposite one of said second plates to provide a schematic diagram of three parallel capacitors that are not connected to one another.

17. A circuit as set forth in claim 10 wherein one of said first and second plates is opposite three of the other of said first and second plates to provide three capacitors electrically connected in parallel with one another.
18. A circuit as set forth in claim 10 wherein three of said first plates are opposite two of said second plates to provide first and second circuit elements, a first reactive element connected between two of said first and second plates and a second reactive element connected between the second and third of said plates to form a schematic diagram having one side of the first circuit element connected to one side of the first reactive element and one side of the second circuit element connected between said first and second reactive elements.

19. A circuit as set forth in claim 18 wherein said reactive element is in the shape of a square wave having a straight horizontal section, a raised section that extends up, horizontally and down and a straight horizontal section.

20. A circuit as set forth in claim 19 wherein said reactive element is a resistor.

21. A circuit as set forth in claim 19 wherein said reactive element is an inductor.

22. A multiple single layer passive integrated circuit comprising:
   a ceramic body having a selected shape, length and width,
   a plurality of thin, conductive first plates on a first face of said body, each of said first plates being of a selected width and a selected height with a gap of a preselected width between adjacent of said first plates,
   a plurality of thin, conductive second plates on an opposite face of said body, said second plate being of a selected width and a selected length
with a gap of a selected width between adjacent of each of said plates,

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each oppositely disposed of said first and second plates forming a capacitor, each of said first plates is opposite one of a second of said second plates to provide a schematic diagram of three parallel plates that are not connected to one another.
FIG. 6

FIG. 7
A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : Please See Extra Sheet.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO APS, STN
search terms: integrated circuits, etching, sawing, thin films, capacitors, resistors, inductors

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y</td>
<td>US 4,356,530 A (SATO ET AL.) 26 OCTOBER 1982 (26.10.82); see Figure 13B.</td>
<td>1-22</td>
</tr>
<tr>
<td>Y</td>
<td>US 4,312,026 A (IWAYA ET AL.) 19 JANUARY 1982 (19.01.82) ; see Figure 13B.</td>
<td>1-22</td>
</tr>
<tr>
<td>Y</td>
<td>US 3,431,473 A (CORMIER ET AL.) 04 MARCH 1969 (04.03.69) ; see Figure 3.</td>
<td>1-22</td>
</tr>
</tbody>
</table>

Further documents are listed in the continuation of Box C. See patent family annex.

| * Special categories of cited documents: |
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Date of the actual completion of the international search
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Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (6):
H01G 4/005, 4/012, 4/008, 4/228, 4/06, 4/38, 7/00; H05K 3/02, 1/00, 1/03, 1/18, 1/16, 7/02; B05D 5/12

US CL: