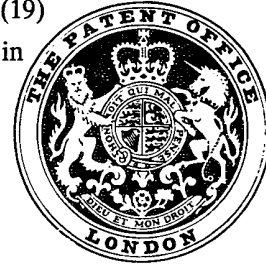


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(54) IMPROVED CONTROL ARRANGEMENTS FOR ELECTRONIC APPARATUS INCLUDING PLURAL CIRCUIT MEANS

(71) We, CASIO COMPUTER COMPANY LIMITED, a Japanese corporation, of 6-1, 2-chome, Nishishinjuku, Shinjuku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

The present invention relates to control arrangements used for switching modes of operation of an electronic apparatus including plural circuit means driven by different power systems.

A small electronic computer providing also a time counting function (referred to as a calculator with clock) using a single display for both the functions, for example, has been used in practice. Continuous drive of the display device consuming relatively large power is undesirable from a viewpoint of power saving. A countermeasure taken for this is that power is constantly supplied to the time counting circuits while power is supplied to the computing and display circuits only when a computing function is to be performed or the time counted is to be displayed.

This kind of calculator uses various modes of operation; a computing mode or an OFF mode, a set mode for setting time, etc. When a change is made from one mode of operation to another mode, it is desirable that the date contents thus far stored or displayed is cleared to be set at an initial value. For example, the apparatus may be set to the set mode to set a desired time and then switched to the computing mode. In this case if it is assumed that the computer circuits are not set at the initial condition, if a function key is erroneously actuated, before the computer circuits are initialized, the calculator calculates the contents displayed on the basis of the instruction produced by the key actuation. Failing to take notice of this error, an operator may enter new data into the calculator and operates the corresponding func-

tion key. The result is that the calculator employs operate the newly entered data as a part only of the operand, even though it was entered as the whole of the operand to be operated upon. The result of the calculation is erroneous. It is for this reason that the operator must set the calculator circuitry to its initial condition by an appropriate key actuation before its operation, each time that the mode of operation is changed. This is troublesome in calculator operation.

Therefore, it is desirable to automatically reset the respective circuits of the computing block to an initial condition whenever a mode change is made. It is usual for the initial value setting circuit to comprise a CR circuit including resistance and capacitance, and a wave-shaping circuit. In mode changing the resetting operation does not take place synchronously with the operation of the constantly operating time counting circuit, since the time constant, being dependent on the CR values, is asynchronous with the timing of the internal operation of the time counting circuits. It is impossible, therefore, to perform a correct transfer of data between the two circuit blocks.

Accordingly, an object of the present invention is to provide electronic apparatus including a plurality of circuit means in which an output signal of a mode switch for selecting various modes of operation is transmitted as an initializing signal to a second circuit means through a control circuit of a first circuit means which is constantly operating, said control circuit providing an output signal synchronously with the operation of the first circuit means whereby, when the mode switch is actuated to produce a mode change, the second circuit means is initialized in synchronism with the operation of the first circuit means.

According to the present invention there is provided electronic apparatus including plural circuit means and comprising: mode

selecting means for selecting one of a plurality of modes of operation; a first power source; first circuit means arranged to be continuously fed with power from said first power source; a second power source; second circuit means which operates only in response to the supply thereto of power from the second power source; synchronous control means for producing an initializing signal at a time determined by said first circuit means when said mode selecting means is actuated to select a new mode in which said second circuit means is operative, said second circuit means including initial condition setting means arranged to respond to said initializing signal from said synchronous control means and to set at least one element of said second circuit means to a predetermined condition.

In a preferred embodiment of electronic apparatus according to the invention the first circuit means continuously fed with power includes the synchronous control means for producing said initializing signal. To the synchronous control means there are connected fixed contacts of a switch, constituting the mode selecting means, which contacts are spaced from one another by a distance greater than the width of a movable switch contact. Thus when switching is effected between the modes, other than when switching into the "OFF (TIME)" mode, or when the operation initiating key is actuated in the "OFF(TIME)" mode, the synchronous control means supplies an initializing signal to the second circuit means. As a result the second circuit means is initialized, for example, to erase any data stored therein. A troublesome key actuation for initializing the apparatus after each mode change is thus obviated and erroneous operation is eliminated.

Furthermore, since the initializing operation produced in mode switching is in synchronism with the operation of the first circuit means, the first and second circuit means are both synchronized with each other in operation, ensuring correct data transfer therebetween.

Other objects and features of the present invention will be apparent from the following description in connection with the accompanying drawings, in which:-

Figure 1 shows a block diagram of a calculator with clock which is an embodiment of the present invention;

Figure 2 shows a circuit diagram of major circuit portions of the Figure 1 circuit;

Figure 3 schematically shows a mode selector used in the Figure 1 circuit; and

Figure 4 is a set of timing diagrams useful in illustrating the operation of the Figure 2 circuit.

Reference will first be made to Figure 1 illustrating an entire circuit of a calculator

with clock. In the figure, reference numeral 1 designates an operation block and numeral 2 a time counting block. The operation block 1 operates upon receipt of power from a power source 3 controlled by a power-on signal issued from the time counting block as described later. An input unit 4 comprises a mode selector 41 which also is operable as a power switch, and a key input section including a group of operation keys 42a including functional keys, ten digit keys and a time key 42b. The input unit 4 produces mode select information and key input information to be directed to a control section 5 including a ROM, for example. Upon receipt of the input information, the control section 5 produces numerical data, control signals for the operation block 1, and other control signals for the time counting block 2. The numerical data produced are loaded into a memory 6. Reference numeral 7 denotes an arithmetic unit which operates under the control of the control section 5 to execute a calculation by using the numerical data stored in the memory 6, and loads the result of the calculation into the memory 6. Finally, the data thus loaded again into the memory 6 are read out therefrom to be applied to a display section 8. Reference numeral 9 designates a timing signal generator for synchronizing the operation of the respective circuit portions of the operation block 1.

The time counting block 2 is operated by power from a power source 10 which constantly supplies power independently of setting of the mode selector 41. A time counting section is designated by reference numeral 11. Time setting information is transferred when required from the memory 6 of the operation block 1 to the time counting section 11. In normal operation, the time counting section 11 time-counts each one second or one minute through the addition of "1". For simplicity, the addition of "1" will be referred to as "+1" operation. The "+1" operation is controlled by a control section 12. As shown, a transfer control signal T is applied from the control section 5 of the operation block 1 to the control section 12 of the time counting block 2. The transfer control signal T is used to control transfer of the time information from the memory 6 to the time counting section 11. A synchronous control circuit designated by reference numeral 13 receives output signals from the mode selector 41 and from the time key 42b of the input unit 4. When a predetermined logical condition holds between the signals supplied from the mode selector 41, the time key 42b and the control section 12, the synchronous control circuit 13 turns on the power source 3 and issues an initializing signal. The initializing signal is applied to control section 5 and to the timing signal generator 9. A timing signal generator 14 generates timing signals

for synchronizing the operations of the respective circuit portions of the time counting block 2. Inputs of the timing signal generators 14 and 9 are connected to a reference timing signal generator 15 including by a crystal resonator, for example and, arranged to count cycles of a signal generated from the reference clock generator to produce various timing signals.

Turning now to Figure 2, there is shown a circuit diagram of major circuits used in performing the invention. In this figure, reference numeral 110 designates a time counting register of which the output returns to its own input through a gate circuit 111 controlled by the control section 12 to circulate there-through, and also goes to an adder 112. The adder 112 executes the "+1" operation in response to a "+1" instruction outputted from the control section 12 every one second or one minute and feeds the result of the addition to the time counting register 110 via the gate circuit 111.

Outputs from contacts 411 and 412 of a "SET" mode (mode specified when time is to be set) and a "COMP" mode (mode specified when computing circuitry 1 is to be operated) of the mode selector 41, are applied through an OR circuit 130 to a synchronizing flip-flop 131 operating in synchronism with a word clock signal  $\phi_w$  (the word clock signal  $\phi_w$  means a clock pulse produced each time the respective registers perform one cycle). Another "OFF(TIME)" mode (mode specified when the computing circuitry 1 is not to be used) produces at a contact 410 an output which is applied to an AND gate 132 together with the output of the time key 42b. The output of the AND circuit 132 is applied to the synchronizing circuit 131, through the OR circuit 130. A movable contact 413 connected with a battery 30 is moved to make contact with the respective contacts 410 and 412 to produce the required outputs. The output of the synchronizing circuit 131 is applied as a power-on instruction to the operation block 1. Specifically, the output of flip-flop 131 is applied to an electronic switching circuit 31, and also to a delay circuit 133 with a given time delay and to an AND circuit 134. The output of the delay circuit 133 is applied to the AND circuit 134 through an inverter 135. The delay circuit 133, the AND circuit 134 and the inverter 135 constitute a called one-shot circuit in which the AND circuit 134 produces one-shot pulse with a duration corresponding to the time delay of the delay circuit 133. The one-shot pulse is applied as an initialization signal to the operation block 1. In the power source 3 of the operation block 1, a battery 30 outputs various voltages through the switching circuit 31. The electronic switching circuit 31 connected to a DC-DC converter 32 is conductive when it receives

the power-on signal from the synchronizing circuit 131, to produce various voltages to the operation block 1. Reference numeral 60 denotes an input/output register of which the output is inputted again to its input via a gate circuit 61 controlled by a gate control signal fed from the control section 5, and is also applied to a driver 80 including a parallel-series converter and a segment decoder. The output of the input/output register 60 is applied to the gate circuit 111 of the time counting block 2 to permit data to be transferred to the time counting register 110. The gate circuit 61 receives input data fed from other registers in the memory 6, numerical codes fed from the operation unit 7 or the control section 5 and the output signal from the time counting register 110. The driver 80 properly processes the output signal of the input/output register 60 which is in turn applied to the display device 81 where the contents of the input/output register 60 are made visible.

The mode selector 41 will be further described with reference to Figure 3. The mode selector 41 is of the so called non-shorting structure. The movable contact 413 slides over an electrode 413a to selectively connect this electrode with the fixed contacts 410, 411 and 412 for the respective modes. For this reason, the width of the movable contact 413 is slightly narrower than those of the fixed contacts 410, 411 and 412. The intervals between adjacent contacts 410, 411 and 412 are each wider than the width of the movable contact 413. With this arrangement, when the movable contact 413 moves along the fixed contacts 410, 411 and 412, there is a state that the contact 413 does not contact any one of the fixed contacts 410 to 412 and any one of these fixed contacts produces no output signal.

The explanation to follow is the operation of the embodiment thus far mentioned of the present invention. Referring now to Figures 4(A) to 4(E), there are shown a set of timing diagrams of the operation. Assume now that the movable contact 413 of the mode selector 41 is at first in contact with the fixed contact 410 for the "OFF(TIME)" mode and is then shifted to the "SET" mode. In the "OFF(TIME)" mode, the time counting block 2 operates but the operation block 1 is in an inoperative condition (power-off condition). When the movable contact 413 is moved from the fixed contact 410 to make contact with the fixed contact 411 (SET mode), the contact 411 provides an output signal which in turn is applied to through the OR circuit 130 the synchronizing circuit 131 to develop an output synchronous with the clock signal, through the OR circuit 130. The synchronizing circuit 130 synchronizes an input signal received at any time within a word to yield an output signal at time  $t_1$  as

shown in time  $t_1$ , which is then applied to the electronic switching circuit 31 of the operation block 1. The switching circuit 31 then connects the battery 30 to the DC-DC converter 32 so that the power source 3 provides a voltage with a rise time  $t_a$  from time  $t_1$  to  $t_2$ , as shown in Figure 4(D). The output of the synchronizing circuit 131 is also applied to the delay circuit 133. Upon receipt of the output signal, the delay circuit 133 produces an output signal at  $t_3$  after a given delay time  $t_a$ , as shown in Figure 4(B). The output of the delay circuit 133 is applied through an inverter 135 to the AND circuit 134, together with the output of the synchronous circuit 131. The AND circuit 134 thus produces a one-shot pulse with a width  $t_a$  equal to the delay time, as shown in Figure 4(C). The output of the AND circuit 134 is applied as the initializing signal to the respective circuits of the operation block 1. Any data stored in the computing circuits or operation block 1 is completely cleared after the time period  $t_b$  (between time  $t_2$  and  $t_3$ ) shown in Figure 4(D). As shown, the time period  $T_b$  follows the rise time  $t_a$  and the output voltage of the power source 3 has a constant value during this period of time  $t_b$ . At time  $t_3$ , at the end of interval  $t_a$ , the operation block has been initialized and is ready for operation. The output signal of the AND circuit 134 is synchronous with a word unit of the time counting block 2. For this reason, when the operation block 1 enters an operation mode, the start point of the output signal is in synchronism with the start point of the unit. Therefore, the register 110 of the time counting block 2 operates fully in synchronism with the input/output register 60 of the operation block 1.

Let us consider now the case where the mode selector 41 is switched from the "SET" mode to the "COMP" mode. Assume now that data used in the "SET" mode remains in the input/output register 60. To produce the mode change the movable contact 413 is slid from the fixed contact 411 to the fixed contact 412. In so sliding, the movable contact passes through a state in which it is in contact with neither of the fixed contacts 411 or 412. At this time, the OR gate 130 produces no output. Accordingly, the synchronous circuit 131 detects the "OFF" condition and so causes the power source to be temporarily in an "OFF" condition. Immediately after this, the movable contact slides into contact with the fixed contact 412 so that the OR circuit 130 again produces again an output signal and the synchronizing circuit 131 is synchronized by the clock signal  $\phi_w$  to produce the power-on instruction. Further, the AND circuit 134 produces the initializing signal. As a consequence, the contents of the input/output register 60 is cleared and the operation block 1 again starts to operate in

synchronisms with the time counting block 2, to be ready for the execution of various operations.

The next case to be discussed is when the mode selector 41 is switched from the "SET" or "COMP" mode to the "OFF (TIME)" mode. In this case, the output of the OR circuit 130 ceases at time  $t_4$  in Figure 4. Therefore, the switch circuit 31 becomes non-conductive and the output of the DC-DC converter 32 of the power source 3 falls with a slight delay. This stops the operation of the operation block 1, and also the display at the display section at time  $t_5$ . When in this condition, actuation of the time key 42b enables the AND circuit 132 of which the output is applied to the synchronizing circuit 131 through the OR circuit 130, with the result that the operation block 1 is ready for operation because of its power-on, as in the previous case. At this time, the operation block 1 is set to its initial condition, synchronously with the time counting block 2, as in the case of the above-mentioned mode switching, and the control section 5 detects the condition that the power source is turned on, and detects that the present mode is "OFF (TIME)" and that the time key 42b is operated. The control section 5, then issues an instruction to input the contents of the time counting register 110 into the gate circuit 61, with the result that the contents of the time counting register 110 is transferred to the input/output register, through the gate circuit 61. The contents of the input/output register 60 is transferred through the drive circuit 80 to the display device 81 to be displayed. When subsequently, the actuation of the time key 42b is released so that the operation block 1 becomes in inoperative condition and the display goes out, as in the mode selection of "OFF (TIME)" by the mode selector 41. When the mode selector is in the "SET" mode, actuation of the time key 42b instructs to transfer the contents of the input/output register 60 into the time counting register 110 when the mode selector 41 is in "SET" mode. More specifically, the mode selector 41 is set for the "SET" mode and the operation key 42a is actuated to enter a desired time in the time counting register 110. The time key 42b is then actuated, and as a result the control section 5 issues to the control section 12 an instruction to transfer data from the input/output register 60 into the time counting register 110. Upon receipt of this signal and the signal inputted directly from the time key 42b, the control section 12 controls the gate circuit 111 so that the contents of the input/output register 60 is loaded into the time counting register 110 through the gate circuit 111.

In the above-mentioned embodiment, the switch shown in Figure 3 is used for the mode

selector 41. Note, however, that the essential requirements for the mode selector 41 is that the respective fixed contacts are disposed with intervals each wider than the width of the electrode of the movable contact, and that there must be a state that, when the movable contact shifts from one to another fixed contact, it necessarily contacts none of the fixed contacts.

The present invention thus far referred to relates to its application for a calculator with clock; however, the present invention is applicable widely for those including a normally operable circuit means, circuit means for which the power is turned on only when required, and a mode selector for mode selection.

#### WHAT WE CLAIM IS:-

1. Electronic apparatus including plural circuit means and comprising: mode selecting means for selecting one of a plurality of modes of operation; a first power source; first circuit means arranged to be continuously fed with power from said first power source; a second power source; second circuit means which operates only in response to the supply thereto of power from the second power source; synchronous control means for producing an initializing signal at a time determined by said first circuit means when said mode selecting means is actuated to select a new mode in which said second circuit means is operative, said second circuit means including initial condition setting means arranged to respond to said initializing signal from said synchronous control means and to set at least one element of said second circuit means to a predetermined condition.

2. Electronic apparatus according to claim 1, in which said synchronous control means produces a power-on signal controlling said second power source as well as said initializing signal.

3. Electronic apparatus according to claim 2, in which said second power source comprises connectable by way of an electronic switch to a battery, a DC-DC converter, and said power-on signal is applied to said electronic switch.

4. Electronic apparatus according to claim 1, 2 or 3, in which said initializing signal has a pulse width wider than the sum of the rise time of said second power source voltage and the time required for said initializing.

5. Electronic apparatus according to any one of claims 1 to 4, and further comprising input means which is available for both said first and second circuit means and includes at least mode selecting means and data input means.

6. Electronic apparatus according to claim 5, in which said input means includes at least switches for mode selection, and keys for data input and an operation-initiating key

provided on a key board.

7. Electronic apparatus according to claim 6, in which power is constantly supplied to the mode selection switch.

8. Electronic apparatus according to claim 6, in which said mode selection switch is of the non-shortcircuiting type and has fixed contacts spaced apart by intervals each wider than the width of a movable contact cooperating therewith, and said synchronous control means is arranged to produce the initializing signal and the power-on signal whenever the movable contact of said mode selection signal does not contact any one of the fixed contacts.

9. Electronic apparatus according to claim 6, in which said mode selection switch is arranged to select one of a plurality of operational modes including "POWER-OFF" mode for said second circuit means.

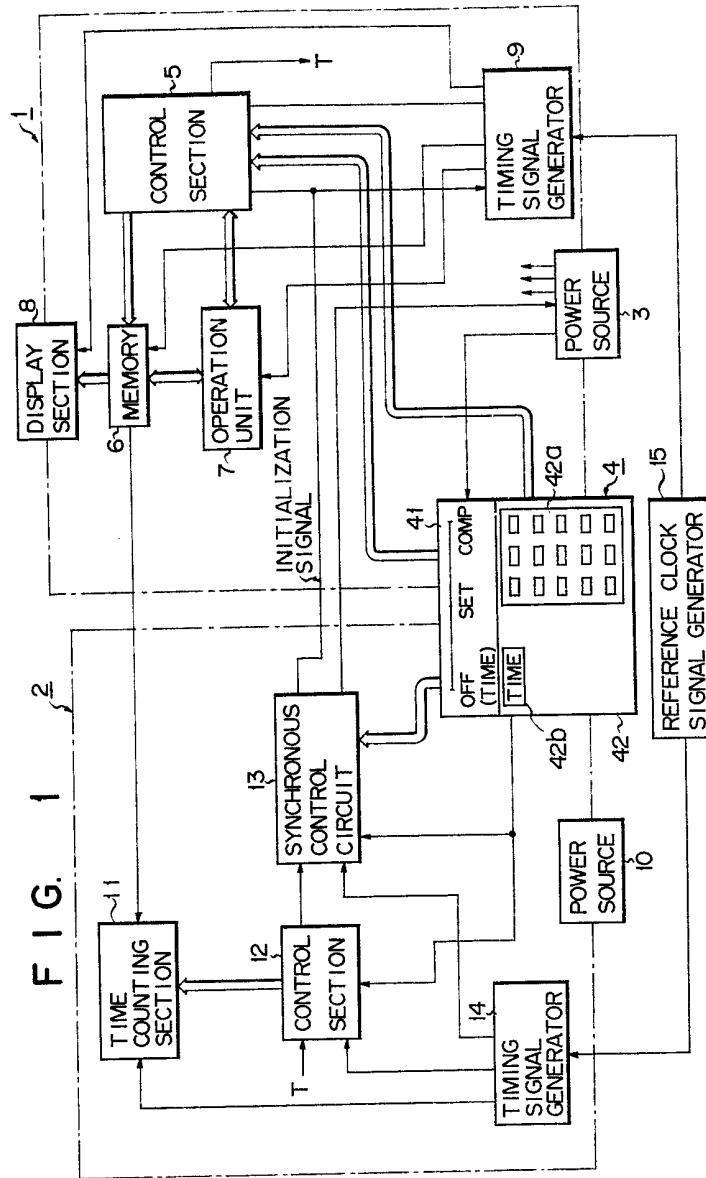
10. Electronic apparatus according to claim 9, in which said synchronous control means includes means for detecting the logical product of an operational signal fed from said operation-initiating key provided on said key board and a signal representing that said "POWER-OFF" mode is specified.

11. Electronic apparatus according to claim 1, in which said first circuit means includes a controller, a time counter, a timing signal generator, and said synchronous control means and constitutes a time counting block which operates receiving constantly power from said first power source, and said second circuit means includes a timing signal generator, a controller, an operation section, and a memory, and constitutes an operation block which is selectively provided with power from said second power source.

12. Electronic apparatus in accordance with claim 1 and substantially as hereinbefore described with reference to the accompanying drawings.

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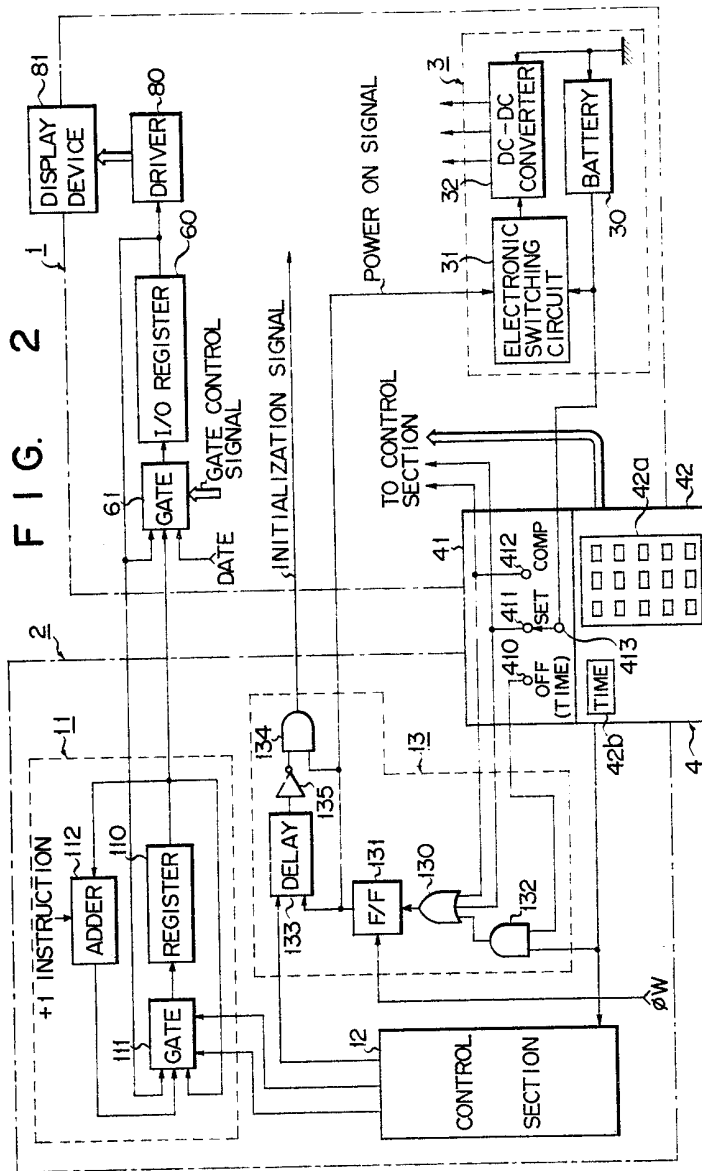


FIG. 3

