(12) UK Patent Application (19) GB (11) 2 062 320 A

(21) Application No 8035098
(22) Date of filing 31 Oct 1980
(30) Priority data
(31) 54/140442
(32) 1 Nov 1979
(33) Japan (JP)
(43) Application published
20 May 1981
(51) INT CL³
G08B 7/00
(52) Domestic classification
G4H 13D 14A 14B 14D
14G 1A 60 RBE RCE RCT
(56) Documents cited
None
(58) Field of search
G4H
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(54) **Paging Receiver with Display**

(57) A paging receiver comprises first means for receiving and demodulating a carrier wave modulated with a paging signal code, and a plurality of information key codes corresponding to a plurality of words, respectively; second means for decoding said information key codes when its own paging signal code is detected; third means for storing in advance a plurality of words corresponding to said information key codes, respectively; and means for reading out and displaying the words corresponding to the decoded information key codes.

Fig.3.

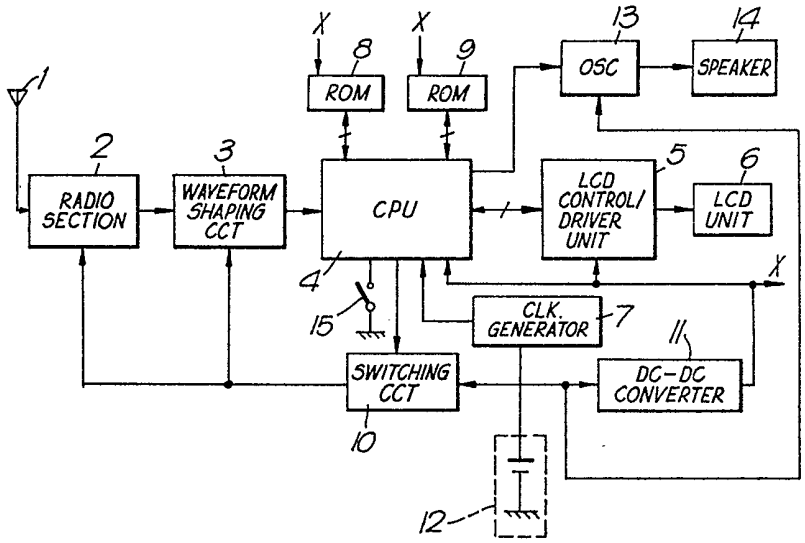


Fig. 1.

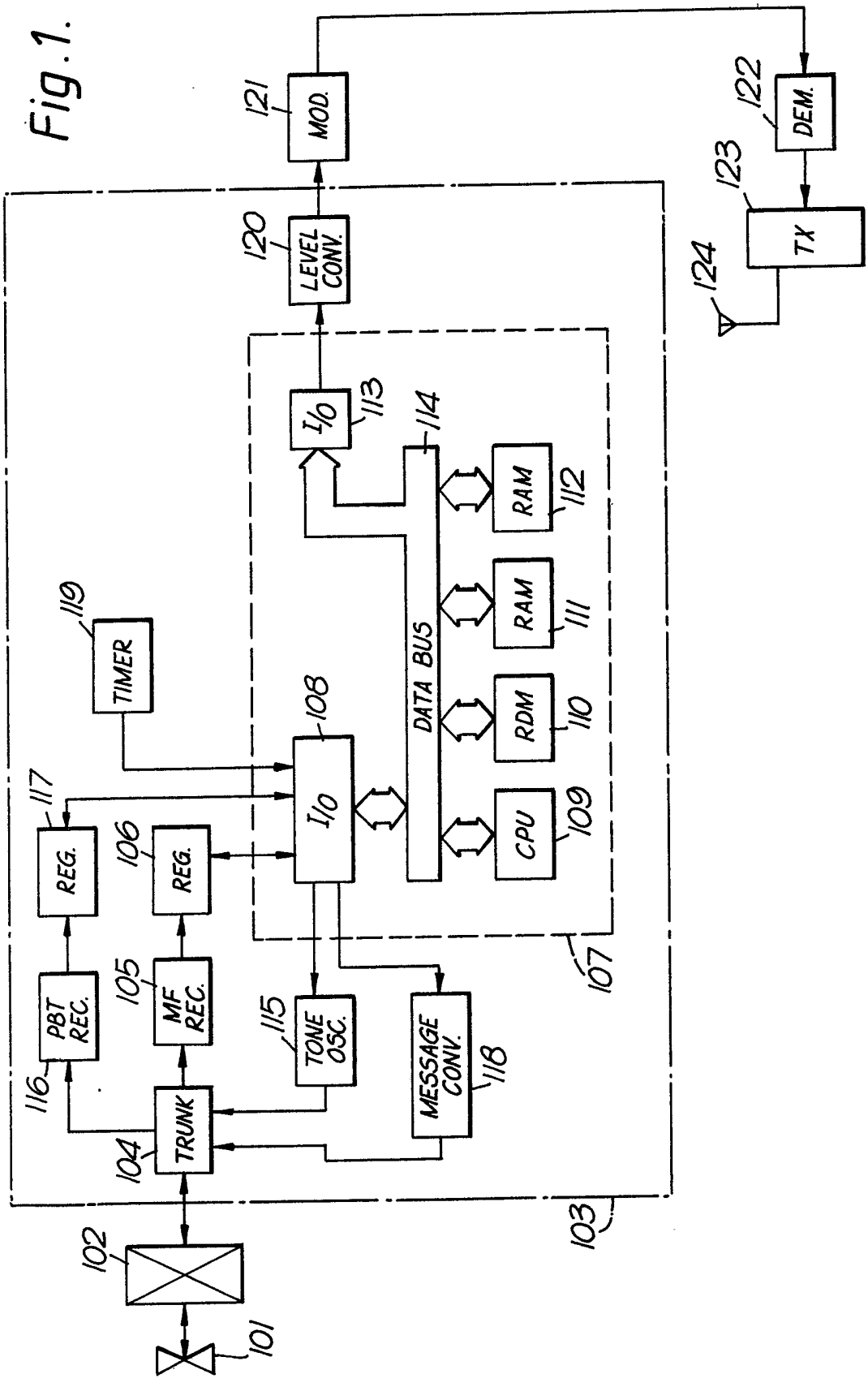

101
102
103
104
TRUNK
105
MF REC.
106
REG.
107
108
I/O
109
CPU
110
RDM
111
RAM
112
RAM
113
I/O
114
DATA BUS
115
TONE OSC.
116
PBT REC.
117
REG.
118
MESSAGE CONV.
119
TIMER
120
LEVEL CONV.
121
MOD.
122
DEM.
123
TX
124

Fig. 2A.

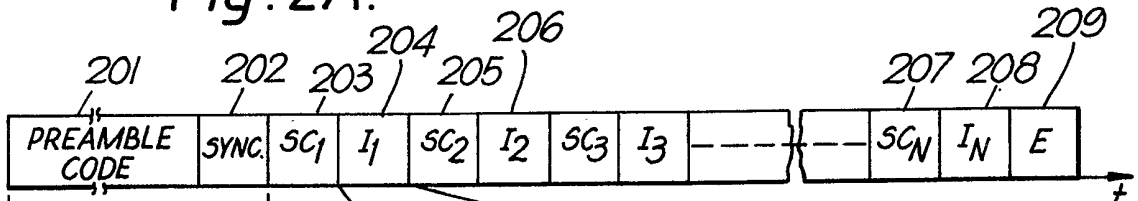
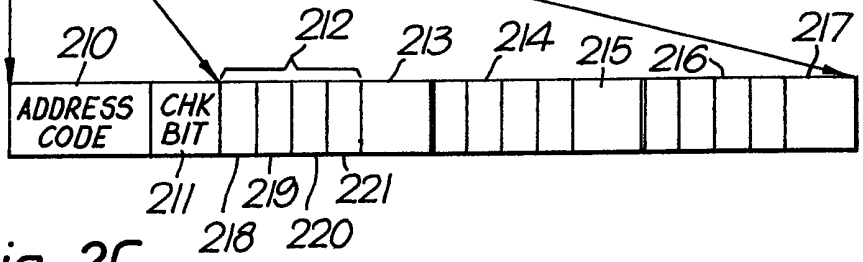


Fig. 2B.



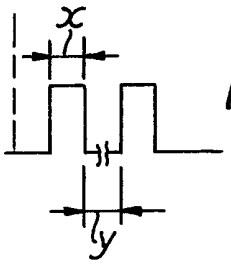


Fig. 2C.

Fig. 3.

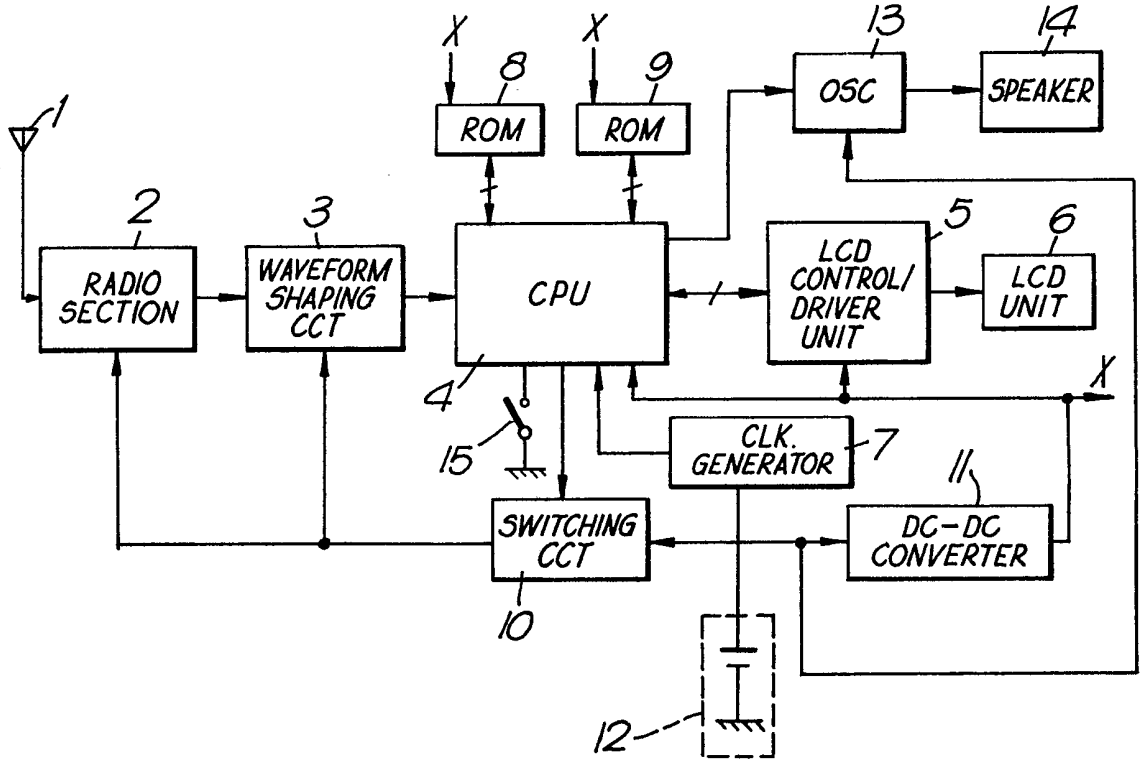
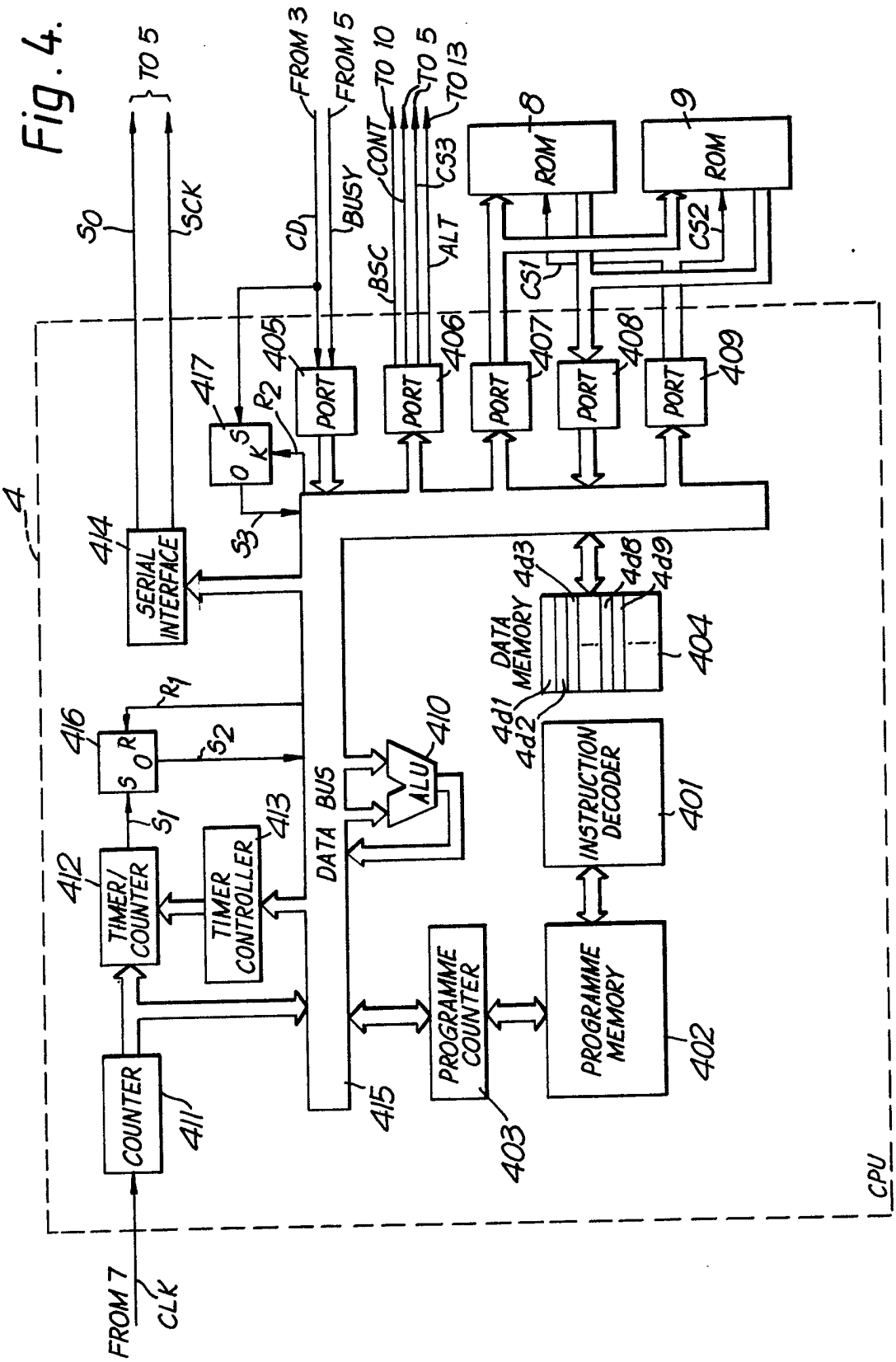


Fig. 4.


4
CPU
FROM 7
CLK
COUNTER
411
TIMER/ COUNTER
412
TIMER CONTROLLER
413
DATA BUS
415
PROGRAMME COUNTER
403
PROGRAMME MEMORY
402
INSTRUCTION DECODER
401
ALU
410
DATA MEMORY
404
4d1
4d2
4d3
4d8
4d9
SERIAL INTERFACE
414
S0
SCK
TO 5
S1
S2
S3
R1
R2
416
417
FROM 3
FROM 5
TO 10
TO 5
TO 13
CD
BUSY
CONT
CS3
BSC
ALT
CS1
CS2
PORT
405
406
407
408
409
ROM
8
9

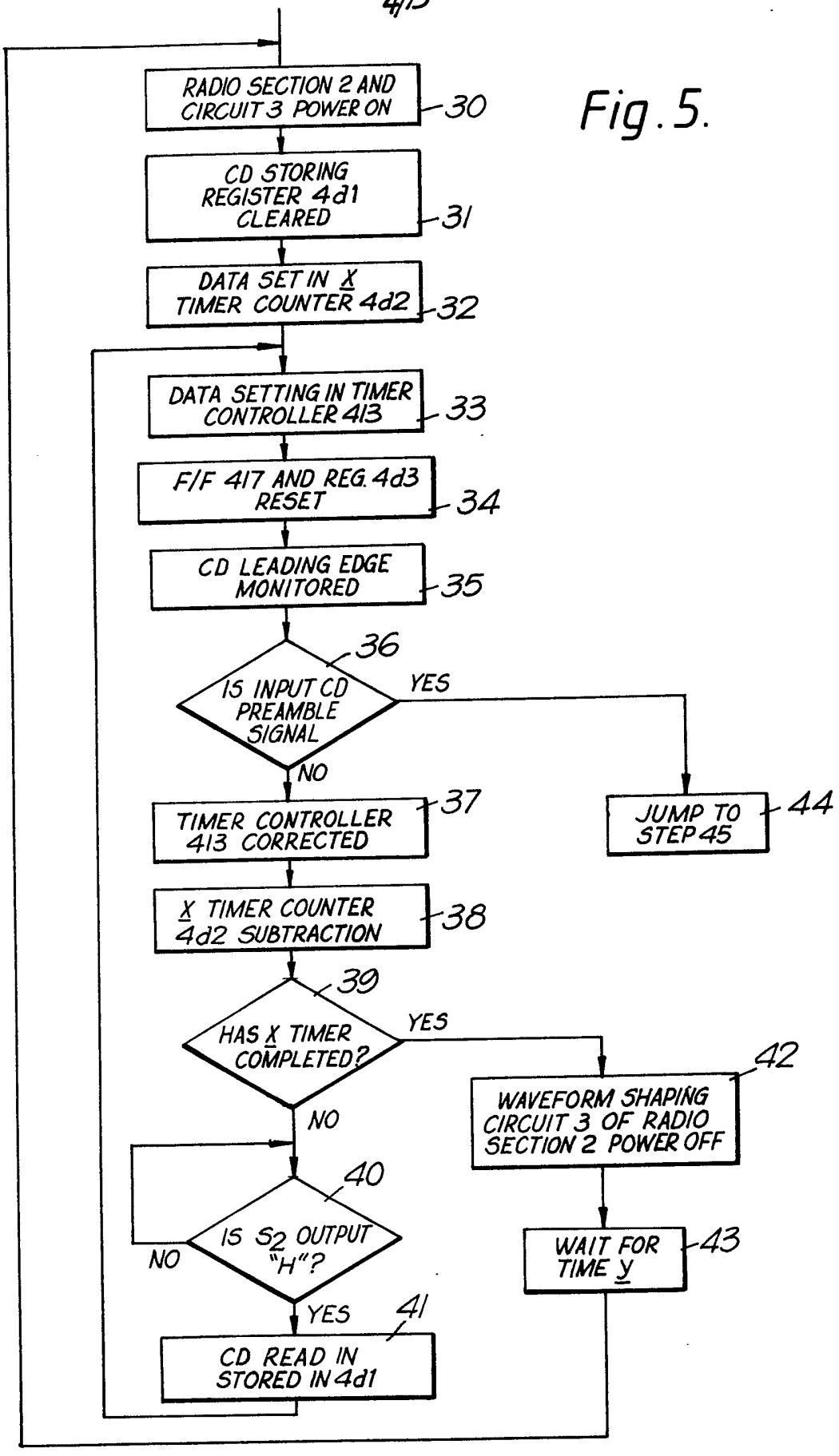

RADIO SECTION 2 AND CIRCUIT 3 POWER ON
30
CD STORING REGISTER 4d1 CLEARED
31
DATA SET IN X TIMER COUNTER 4d2
32
DATA SETTING IN TIMER CONTROLLER 413
33
F/F 417 AND REG. 4d3 RESET
34
CD LEADING EDGE MONITORED
35
36
IS INPUT CD PREAMBLE SIGNAL
YES
NO
TIMER CONTROLLER 413 CORRECTED
37
JUMP TO STEP 45
44
X TIMER COUNTER 4d2 SUBTRACTION
38
39
HAS X TIMER COMPLETED?
YES
NO
42
WAVEFORM SHAPING CIRCUIT 3 OF RADIO SECTION 2 POWER OFF
40
IS S2 OUTPUT "H"?
NO
YES
WAIT FOR TIME Y
43
41
CD READ IN STORED IN 4d1

Fig. 5.

Fig.6.

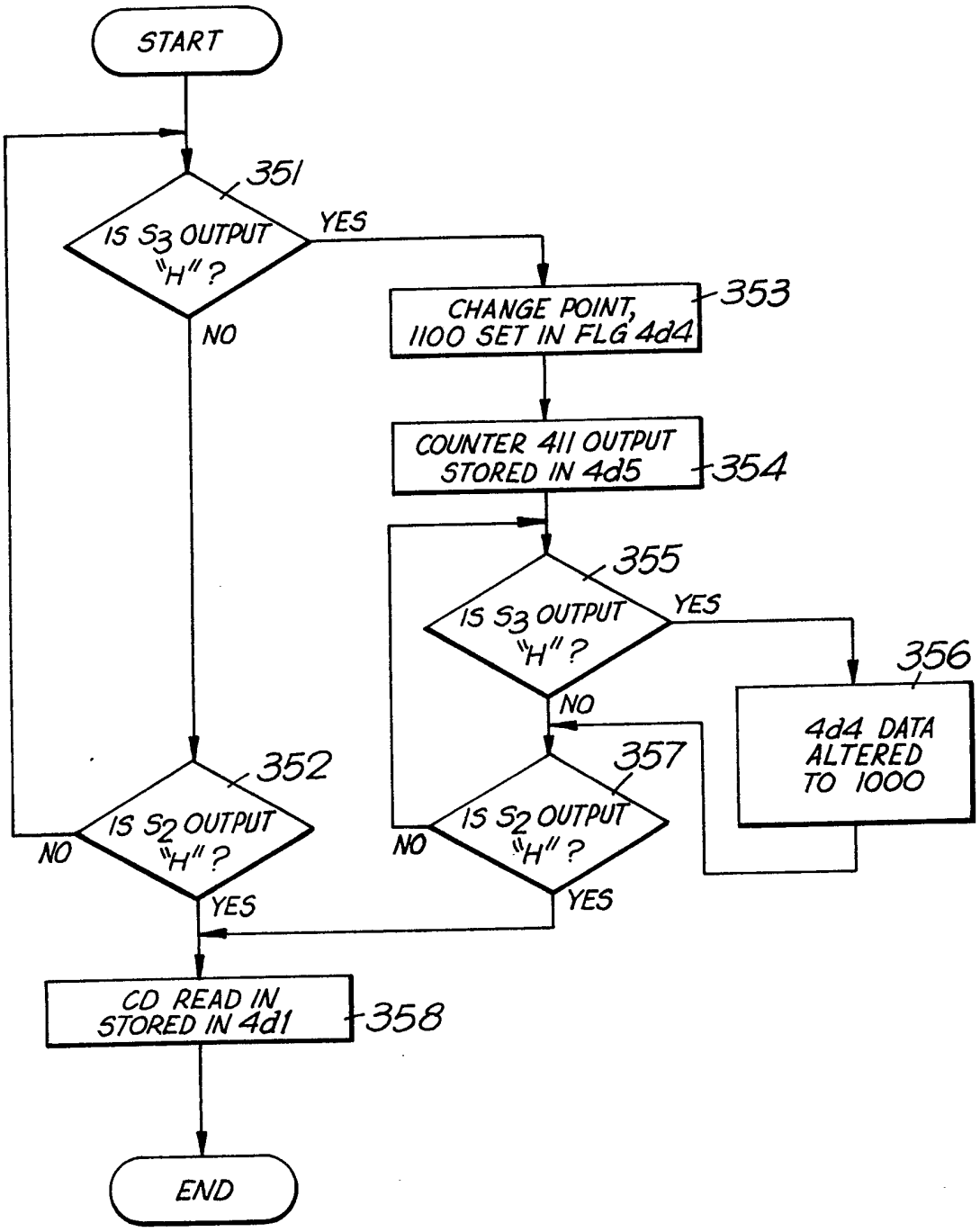

START
351
IS S_3 OUTPUT "H"?
YES
NO
353
CHANGE POINT, 1100 SET IN FLG 4d4
354
COUNTER 411 OUTPUT STORED IN 4d5
355
IS S_3 OUTPUT "H"?
YES
NO
356
4d4 DATA ALTERED TO 1000
357
IS S_2 OUTPUT "H"?
NO
YES
352
IS S_2 OUTPUT "H"?
NO
YES
358
CD READ IN STORED IN 4d1
END

Fig. 7.

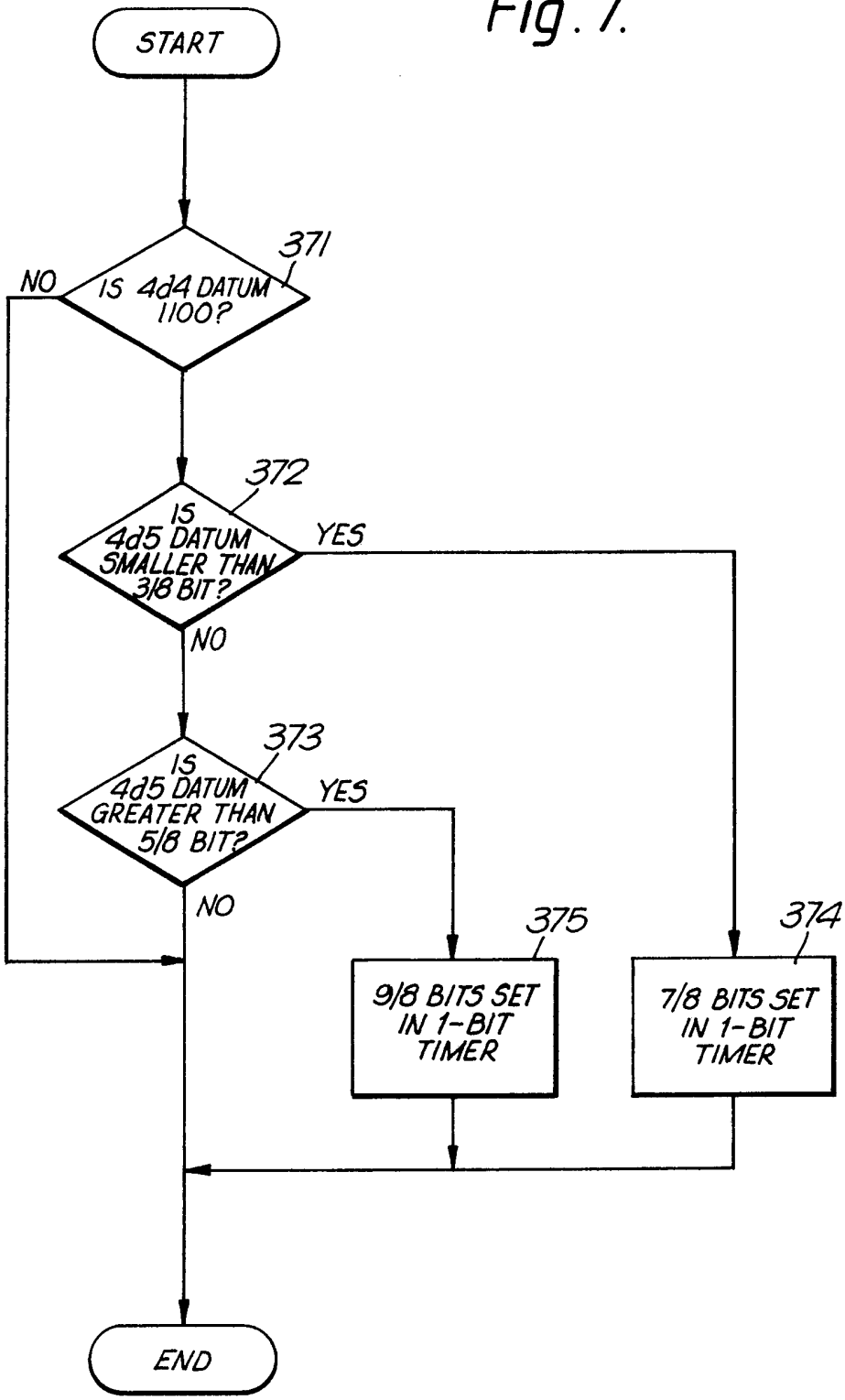
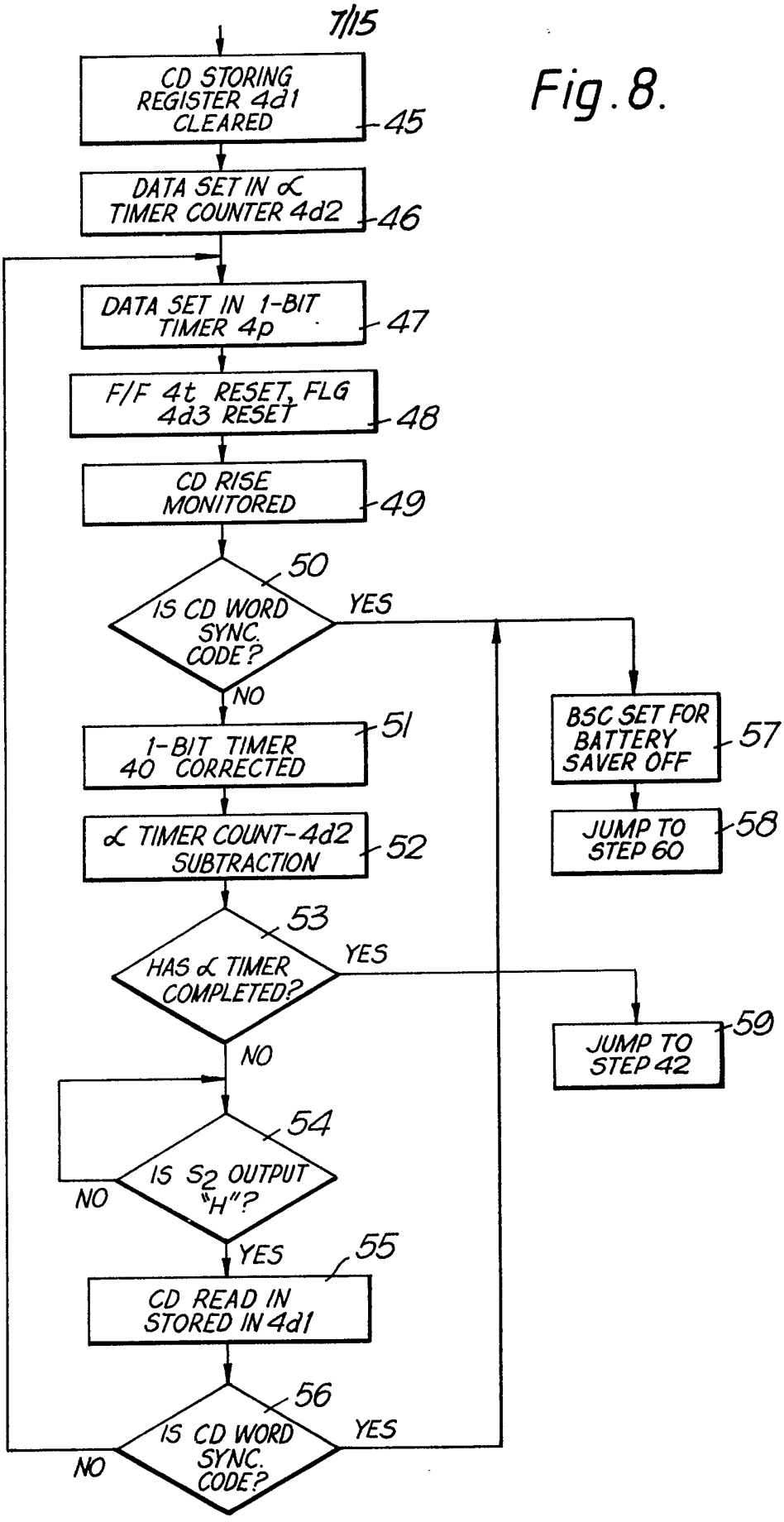

START
371
IS 4d4 DATUM 1100?
NO
372
IS 4d5 DATUM SMALLER THAN 3/8 BIT?
YES
NO
373
IS 4d5 DATUM GREATER THAN 5/8 BIT?
YES
NO
375
9/8 BITS SET IN 1-BIT TIMER
374
7/8 BITS SET IN 1-BIT TIMER
END

Fig. 8.


CD STORING REGISTER 4d1 CLEARED
45
DATA SET IN α TIMER COUNTER 4d2
46
DATA SET IN 1-BIT TIMER 4p
47
F/F 4t RESET, FLG 4d3 RESET
48
CD RISE MONITORED
49
50
IS CD WORD SYNC. CODE?
YES
NO
1-BIT TIMER 40 CORRECTED
51
α TIMER COUNT-4d2 SUBTRACTION
52
53
HAS α TIMER COMPLETED?
YES
NO
54
IS S2 OUTPUT "H"?
NO
YES
CD READ IN STORED IN 4d1
55
56
IS CD WORD SYNC. CODE?
YES
NO
BSC SET FOR BATTERY SAVER OFF
57
JUMP TO STEP 60
58
JUMP TO STEP 42
59

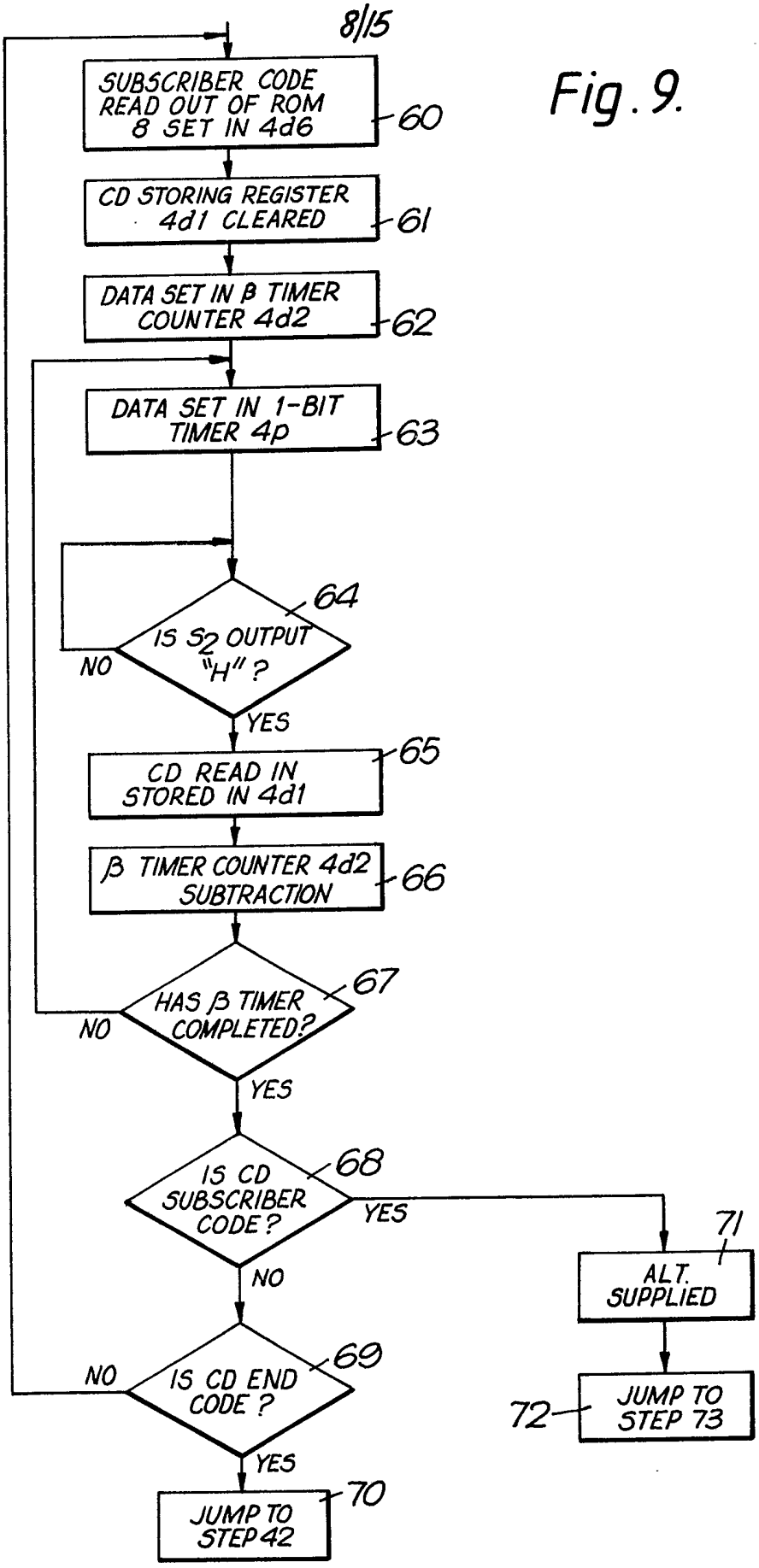

SUBSCRIBER CODE READ OUT OF ROM 8 SET IN 4d6
60
CD STORING REGISTER 4d1 CLEARED
61
DATA SET IN β TIMER COUNTER 4d2
62
DATA SET IN 1-BIT TIMER 4p
63
64
IS S2 OUTPUT "H"?
NO
YES
CD READ IN STORED IN 4d1
65
β TIMER COUNTER 4d2 SUBTRACTION
66
HAS β TIMER COMPLETED?
67
NO
YES
IS CD SUBSCRIBER CODE?
68
YES
NO
71
ALT. SUPPLIED
72
JUMP TO STEP 73
IS CD END CODE?
69
NO
YES
JUMP TO STEP 42
70

Fig. 9.

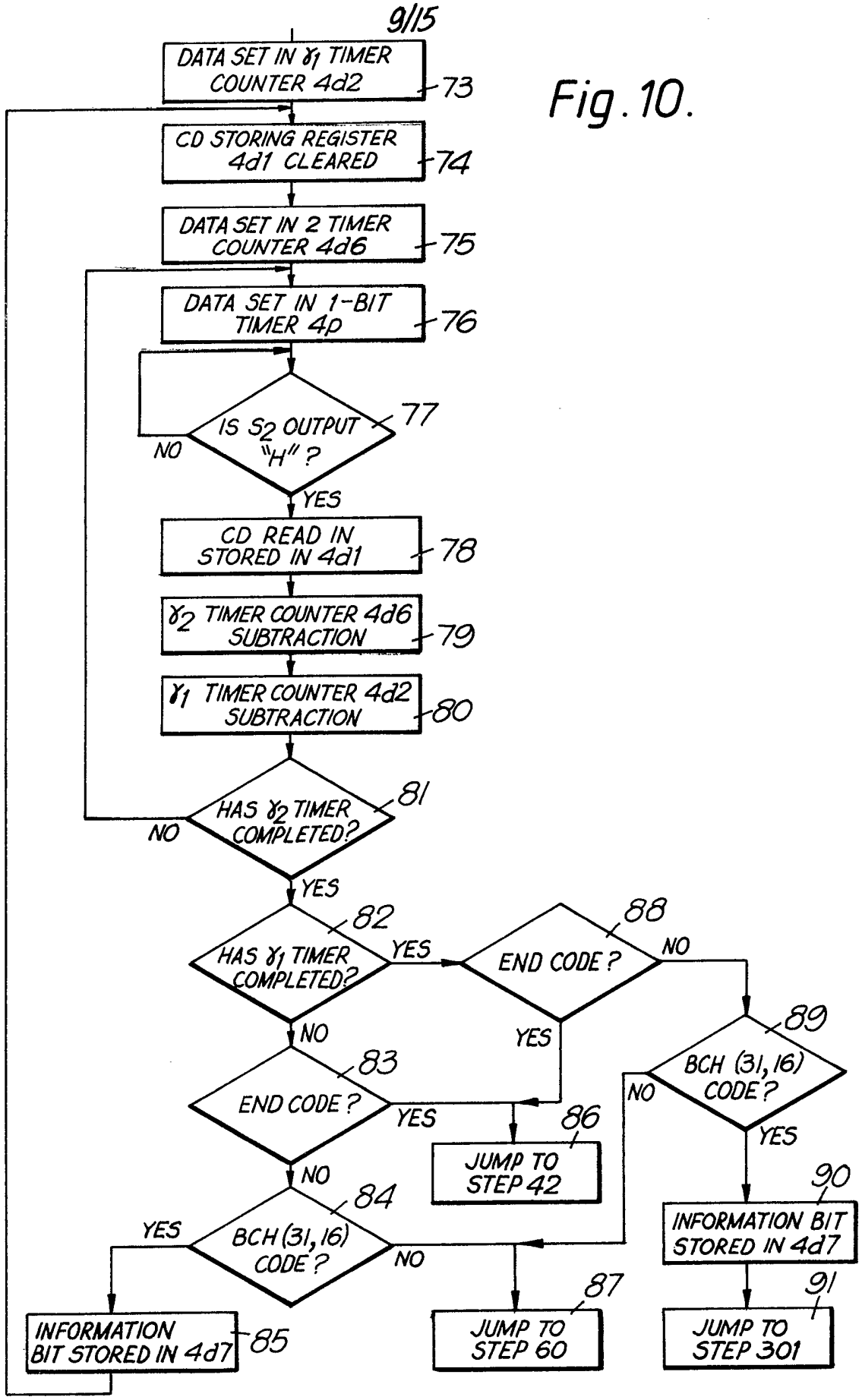

DATA SET IN γ1 TIMER COUNTER 4d2
73
CD STORING REGISTER 4d1 CLEARED
74
DATA SET IN 2 TIMER COUNTER 4d6
75
DATA SET IN 1-BIT TIMER 4p
76
IS S2 OUTPUT "H"?
77
NO
YES
CD READ IN STORED IN 4d1
78
γ2 TIMER COUNTER 4d6 SUBTRACTION
79
γ1 TIMER COUNTER 4d2 SUBTRACTION
80
HAS γ2 TIMER COMPLETED?
81
NO
YES
HAS γ1 TIMER COMPLETED?
82
YES
END CODE?
88
NO
YES
NO
END CODE?
83
YES
JUMP TO STEP 42
86
NO
BCH (31, 16) CODE?
89
NO
YES
BCH (31, 16) CODE?
84
YES
NO
INFORMATION BIT STORED IN 4d7
90
INFORMATION BIT STORED IN 4d7
85
JUMP TO STEP 60
87
JUMP TO STEP 301
91

Fig. 10.

Fig. 11.

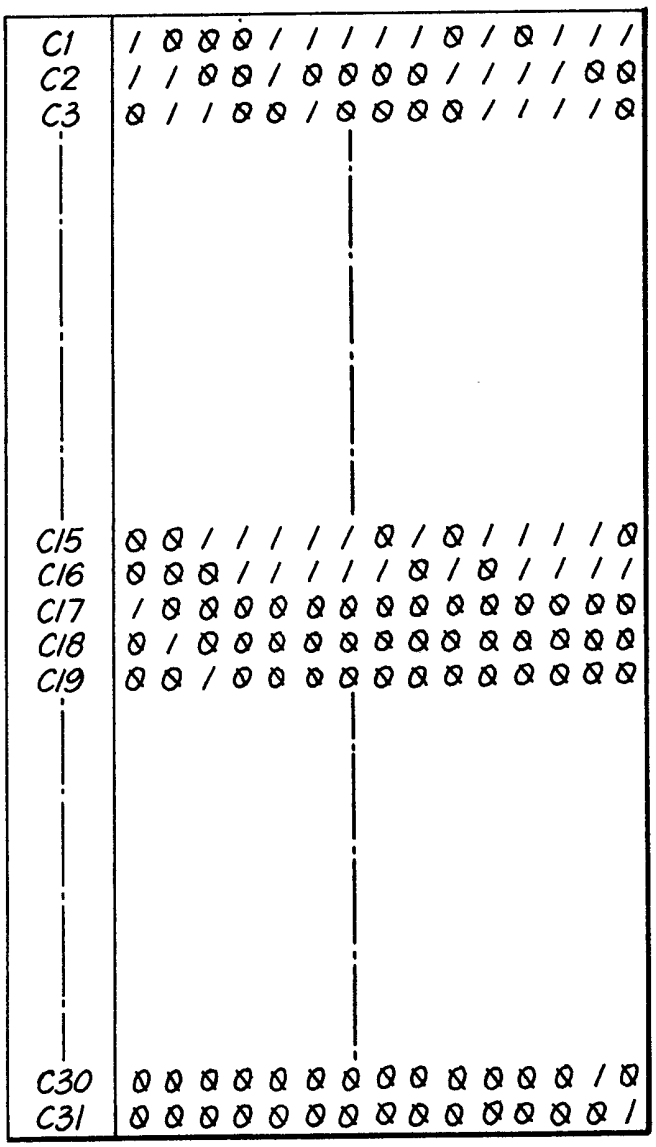


Fig. 12.

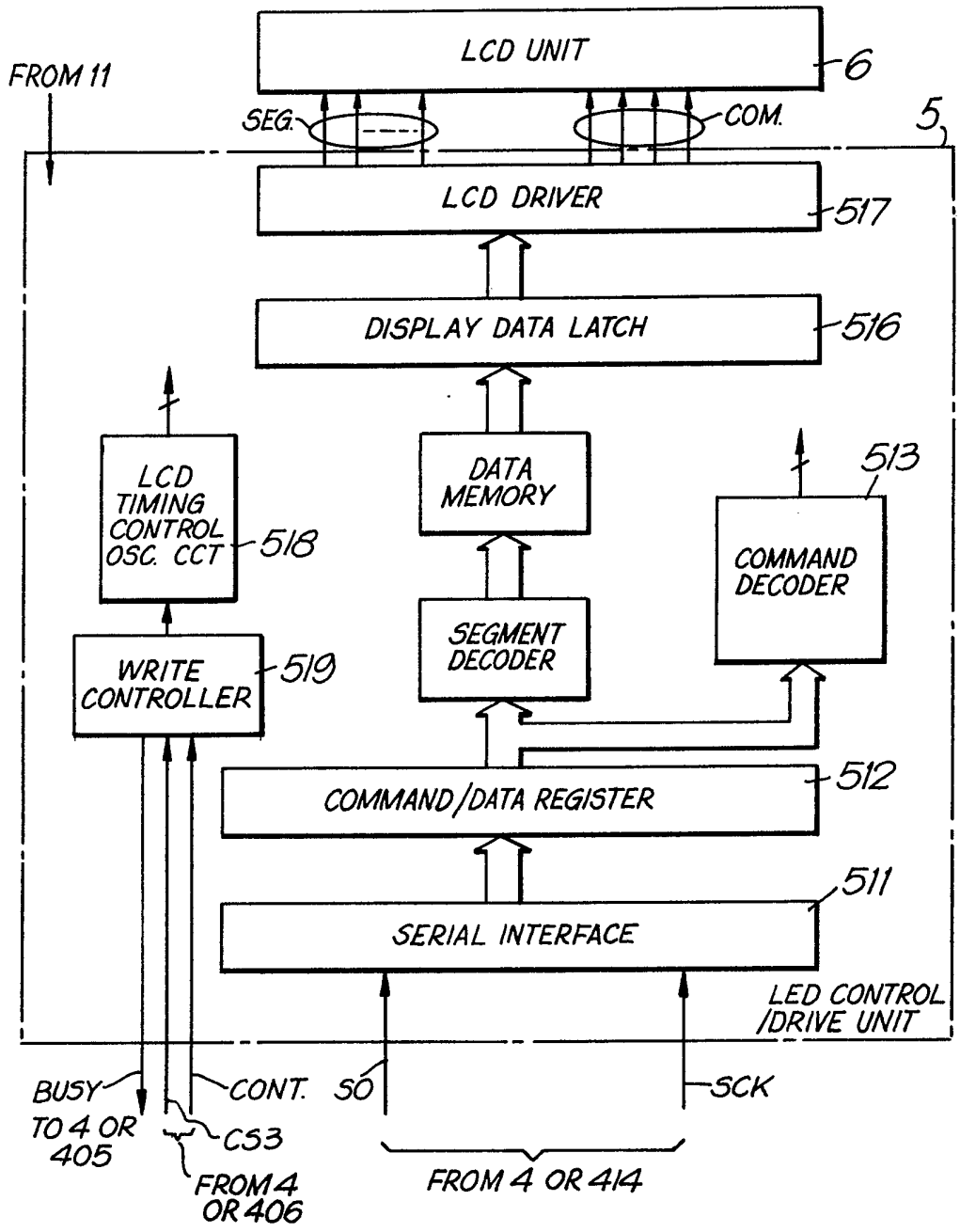

LCD UNIT
6
FROM 11
SEG.
COM.
5
LCD DRIVER
517
DISPLAY DATA LATCH
516
LCD TIMING CONTROL OSC. CCT
518
DATA MEMORY
513
COMMAND DECODER
SEGMENT DECODER
WRITE CONTROLLER
519
COMMAND/DATA REGISTER
512
511
SERIAL INTERFACE
LED CONTROL /DRIVE UNIT
BUSY
TO 4 OR 405
CONT.
CS3
FROM 4 OR 406
SO
SCK
FROM 4 OR 414

Fig.13A.

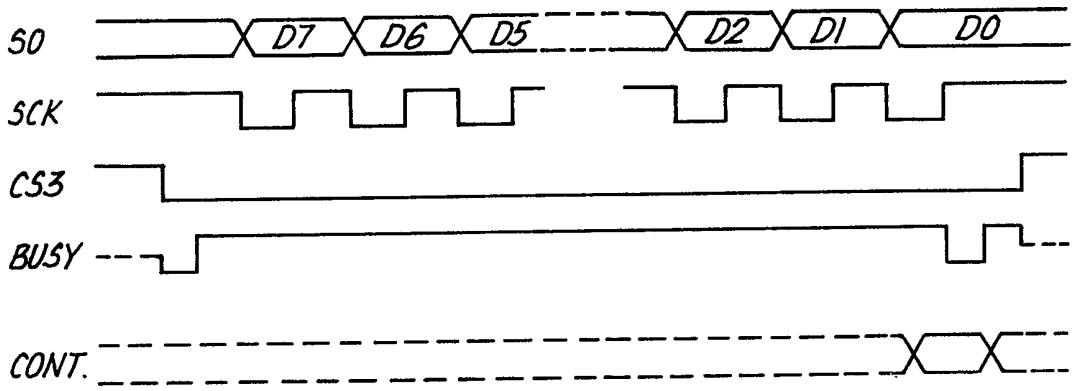


Fig.13B.

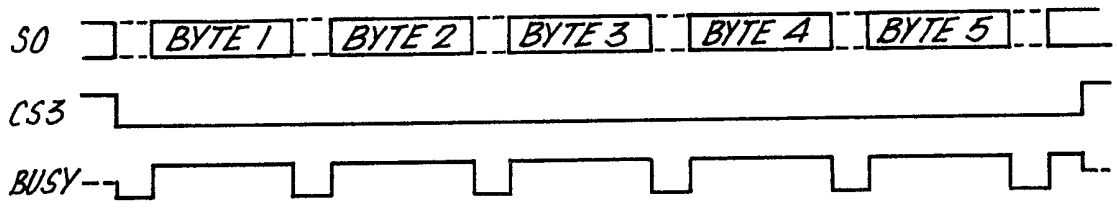


Fig. 14.

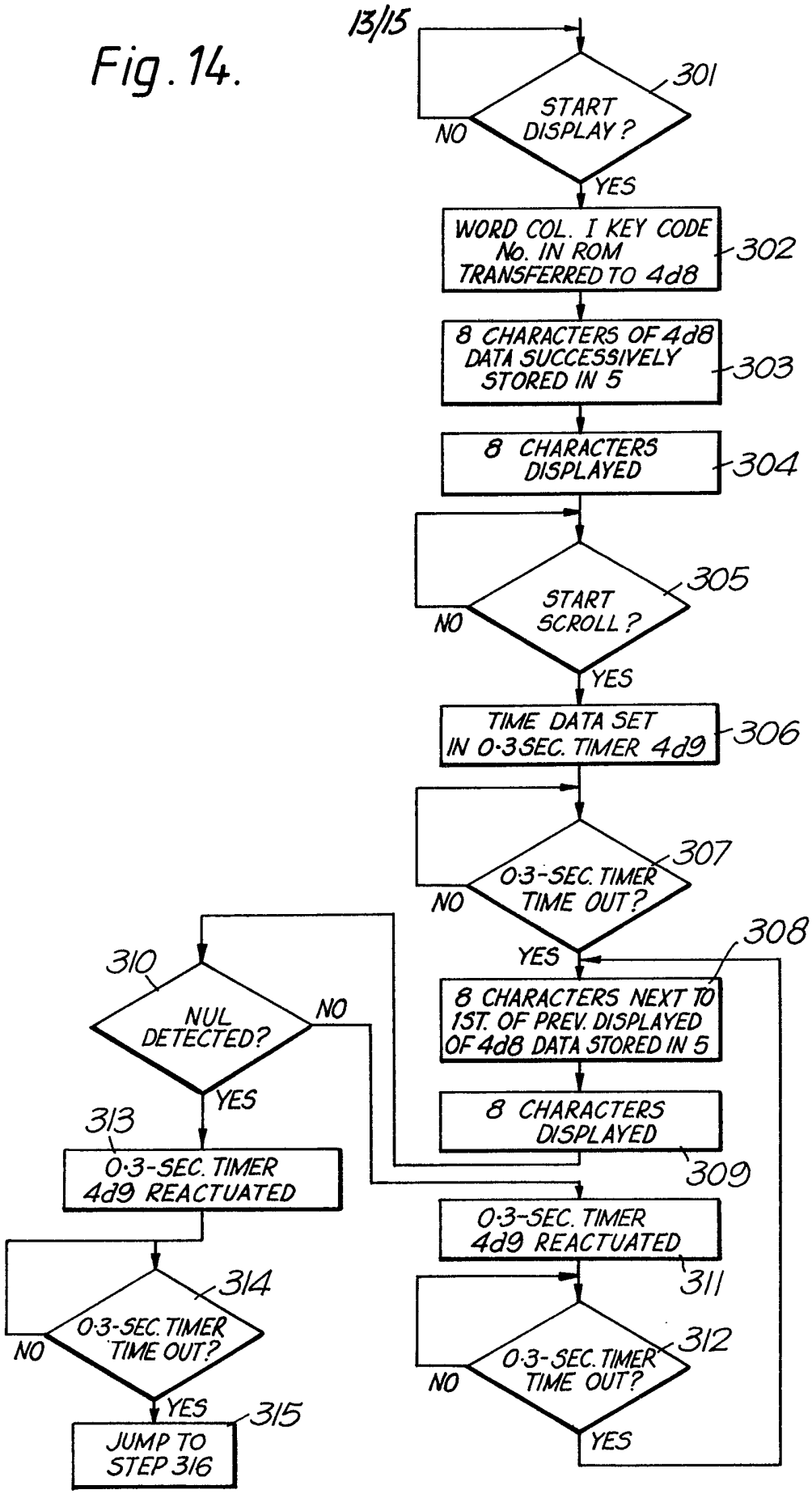

START DISPLAY ?
301
NO
YES
WORD COL. I KEY CODE No. IN ROM TRANSFERRED TO 4d8
302
8 CHARACTERS OF 4d8 DATA SUCCESSIVELY STORED IN 5
303
8 CHARACTERS DISPLAYED
304
START SCROLL ?
305
NO
YES
TIME DATA SET IN 0·3SEC. TIMER 4d9
306
0·3-SEC. TIMER TIME OUT?
307
NO
YES
308
8 CHARACTERS NEXT TO 1ST. OF PREV. DISPLAYED OF 4d8 DATA STORED IN 5
8 CHARACTERS DISPLAYED
309
0·3-SEC. TIMER 4d9 REACTUATED
311
0·3-SEC. TIMER TIME OUT?
312
NO
YES
NUL DETECTED?
310
NO
YES
0·3-SEC. TIMER 4d9 REACTUATED
313
0·3-SEC. TIMER TIME OUT?
314
NO
YES
JUMP TO STEP 316
315

Fig. 15.

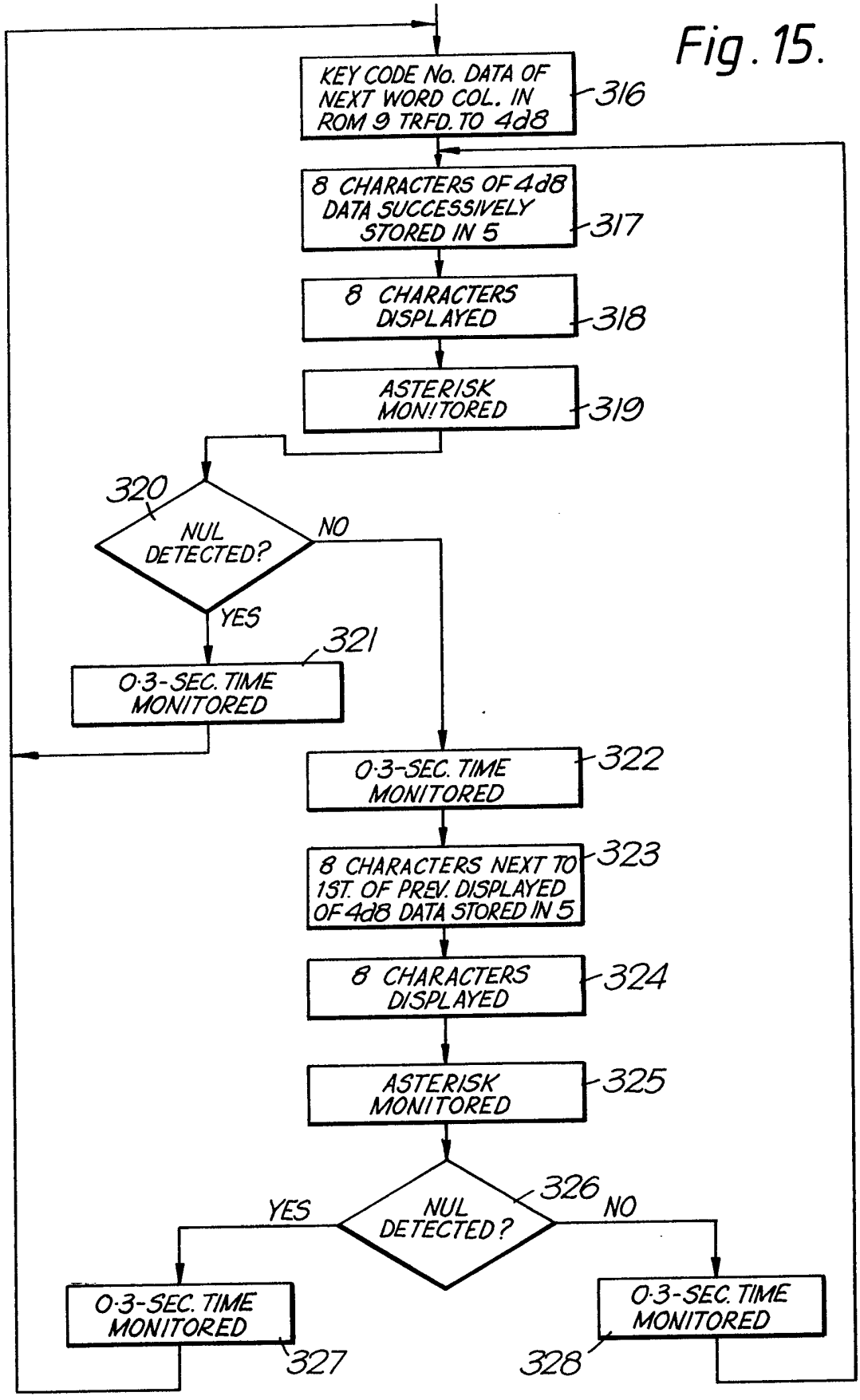

KEY CODE No. DATA OF NEXT WORD COL. IN ROM 9 TRFD. TO 4d8
316
8 CHARACTERS OF 4d8 DATA SUCCESSIVELY STORED IN 5
317
8 CHARACTERS DISPLAYED
318
ASTERISK MONITORED
319
320
NUL DETECTED?
NO
YES
321
0·3-SEC. TIME MONITORED
0·3-SEC. TIME MONITORED
322
8 CHARACTERS NEXT TO 1ST. OF PREV. DISPLAYED OF 4d8 DATA STORED IN 5
323
8 CHARACTERS DISPLAYED
324
ASTERISK MONITORED
325
NUL DETECTED?
326
YES
NO
0·3-SEC. TIME MONITORED
327
0·3-SEC. TIME MONITORED
328

Fig. 16.

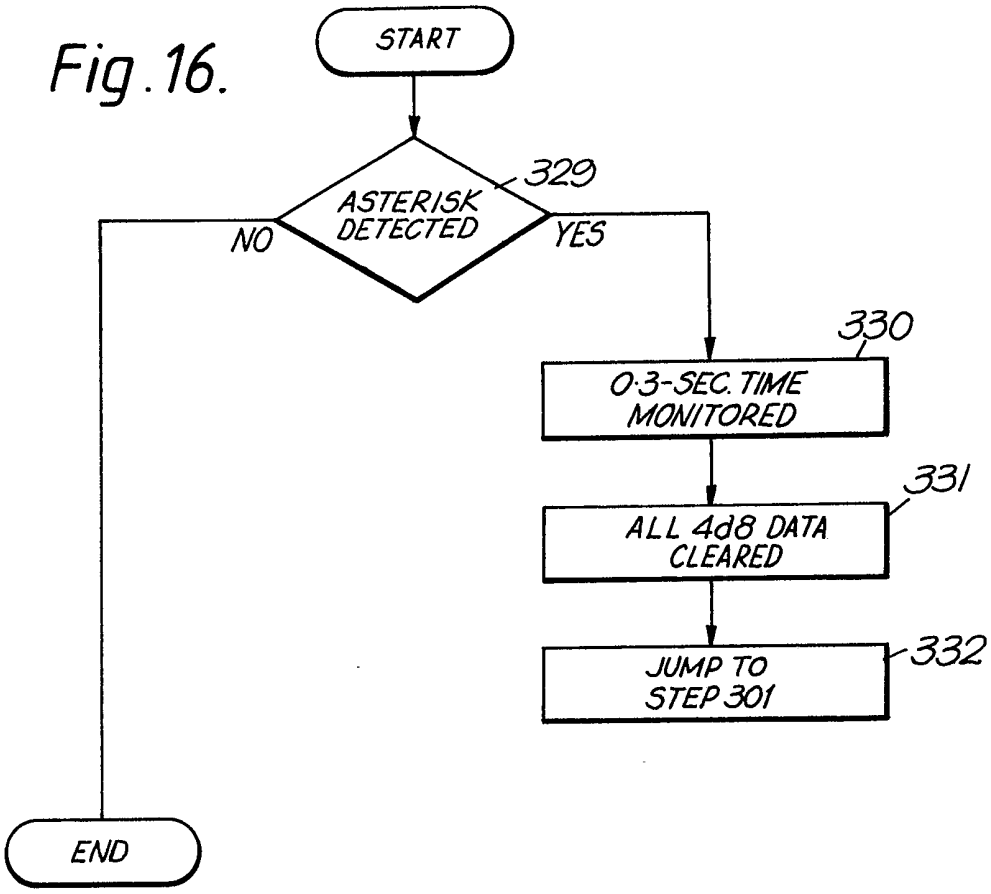
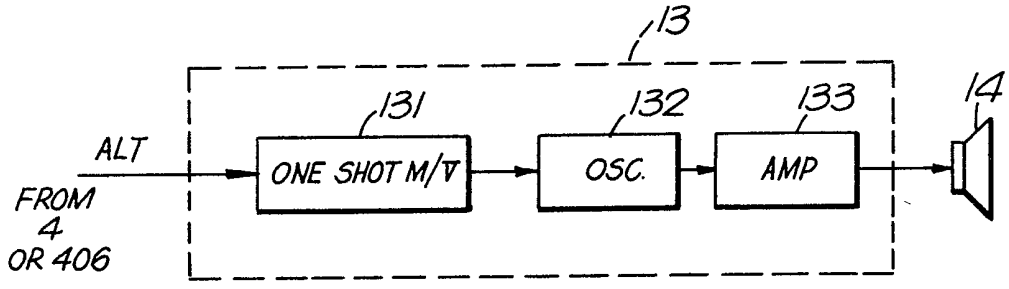

START
ASTERISK DETECTED
329
NO
YES
330
0·3-SEC. TIME MONITORED
331
ALL 4d8 DATA CLEARED
JUMP TO STEP 301
332
END

Fig. 17.


13
131
132
133
14
ALT
FROM 4 OR 406
ONE SHOT M/V
OSC.
AMP

SPECIFICATION

Paging Receiver with Display

The present invention relates to paging receivers with display function.

In such radio paging receivers of prior art, calling signals usually consist of a paging signal for identification of the called receiver and information signals such as speech messages. However, since such receivers use speech messages and accordingly a round of calling signals takes from 15 to 20 seconds, they have a disadvantage of having to limit the number of subscribers per channel to around 1,500. Moreover, because any such receiver involves a difference in bandwidth between its circuit for selecting a paging signal, such as a tone signal, and its voice amplifier for speech messages, such messages can hardly, if at all, reach a called person in a weak electric field zone even though the receiver detects, and draws his attention to, a paging signal. Furthermore, to obtain a great enough audio output to overrride the noise level in the environment of its use, any such receiver requires a highly power audio amplifier for speech messages, resulting in a shorter battery life.

Meanwhile, some of such receivers have a single-digit numeral display but they require the user to remember what he is supposed to do in response to the displayed numeral, and he may sometimes be unable to remember it and therefore to take the required action. As the address is indicated in a single digit, moreover, the amount of information is too strictly limited for the receiver to handle so complex information as speech messages.

An object of the present invention therefore is to provide a battery saving, highly sensitive paging receiver with display, taking little occupied calling time and yet capable of receiving diverse information.

According to the present invention, there is provided a paging receiver comprising: first means for receiving and demodulating a carrier wave modulated with a paging signal code, and a plurality of information key codes corresponding to a plurality of words, respectively; second means for decoding the demodulated information key codes when its own paging signal code is detected; third means for storing in advance a plurality of words corresponding to said information key codes, respectively; fourth means for reading out of said third means words corresponding to the decoded information key codes; and fifth means for displaying the read-out words.

Other advantages and features of the present invention will be more apparent from the detailed description hereunder taken in conjunction with the accompanying drawings, wherein

Figure 1 is a schematic diagram illustrating a base station for use in the invention;
Figures 2A and 2B are diagrams showing transmission signal composition;
Figure 2C is a timing chart of battery saving operation;
Figure 3 is a schematic diagram illustrating a receiver for use in the invention;
Figure 4 shows a block diagram of the central processor unit;
Figure 5 is a flow chart showing a preamble code detecting procedure;
Figure 6 is a flow chart showing a data leading edge monitoring procedure;
Figure 7 is a flow chart showing the single bit correcting procedure;
Figure 8 is a flow chart showing a word synchronization code detecting procedure;
Figure 9 is a flow chart showing a subscriber (or paging) code detecting procedure;
Figure 10 is a flow chart showing an information code detecting procedure;
Figure 11 shows a parity check matrix;
Figure 12 illustrates the composition of a liquid crystal device (LCD) control/drive unit;
Figures 13A and 13B are timing charts showing data transfers of serial interface;
Figures 14, 15 and 16 are flow charts showing an LCD display operating procedure, and
Figure 17 illustrates a block diagram of an oscillator circuit.

In the base station illustrated in Figure 1, when the subscriber calling enters into his push-button telephone set 101 the address number of the paging receiver to be called, a common telephone exchange network 102 transfers this address number in the form of MF (multi-frequency) signal to a paging terminal 103, wherein an MF receiver 105 receives the transferred MF signal through a trunk 104, detects the address number and supplies to a register 106. The address number in the register 106 is checked, by way of an input/output port (I/O port) 108 a data bus 114 in a central controller 107, with a subscriber address number data file in a random access memory (RAM) 111. If the number is found registered therein, the I/O port 108 actuates a tone oscillator 115 and sends a valid tone to the push-button telephone set 101.

Upon receipt of this valid tone, the caller enters first an asterisk (*), then, referring to an index, an appropriate key code number which will be explained in greater detail hereunder, and finally another asterisk. Thus, if the key code number is 020301010103, the entry will be *020301010103*.

A push-button tone receiver 116 in the paging terminal 103 receives the entered signal through the network 102 and the trunk 104, decodes it into a BCD signal and feeds it to a register 117, which, upon detecting the second asterisk, drives a central processing unit (CPU, for example, 8080 marked by Intel) 109 by way of the I/O port 108. The CPU 109 reads out a key code number stored in the register 117 and further reads out key code number data and message data for the caller's confirmation service, registered in a key code number data file and a word data file in the RAM 111,

respectively. Also, the CPU 109 sends these read-out data to a message converter 118 through the i/O port 108. The message converter 118 converts these read-out data into a voice message and supplies the voice message to the push-button telephone set 101. The confirmation message may be, for instance, "Is your message so-and-so (words corresponding to 020301010103)? If it is, hang up after pushing the asterisk button."

When the caller, after confirming his message, pushes in an asterisk through his push-button telephone set 101, the asterisk is again entered into a register 117 through the trunk 104 and a push-button tone receiver 116. Upon detecting the third asterisk, the register 117 ceases to receive key code numbers, and gives a signal indicating this cease to the central controller 107 by way of the I/O port 108.

In response to this signal, the central controller 107 first enters a paging receiver address number in the register 106 via the I/O port 108, encodes it into a BCH (31, 16) code (this BCH code will hereinafter be referred to as the subscriber code) and stores the code in a RAM 112. Then, a key code number is entered from the register 117 by way of the I/O port 108, and every four digits, from the most significant digit on, of the key code number are grouped into a unit. Thus in the aforementioned case of 020301010103, the first unit will be 0203; the second 0101; and the third, 0103. These units are stored in the BCH code (31, 16) form as a signal code of three consecutive words (hereinafter referred to as information code) at an address immediately following the aforementioned subscriber code in the RAM 112. In this manner, input signals from the caller are successively stored in the calling signal area of the RAM 112.

A timer 119 gives an output timing signal to the I/O port 108 at one-minute intervals. Upon detecting this output timing signal, the central controller 107 reads out first a preamble code and synchronization code in a ROM 110, then successively the subscriber code and information code in the calling signal area of the RAM 112 and, after having read out the codes in the calling signal area of the RAM 112, and end code in the ROM 110, and supplies these codes, serially in the reading-out order, to a level converter circuit 120 by way of an I/O port 113. The level converter circuit 120 converts these signals to a level suitable for a data MODEM, and feeds them to a modulator 121, which sends them out on the line as FSK signals. The FSK signals are demodulated into baseband signals by a demodulator 122 in the transmitting base station and fed to a transmitter 123, which modulates a carrier wave with these baseband signals and sends them out through an antenna 124.

The signal code format for use in the present invention, as illustrated in Figure 2A, consists of a preamble code 201, word synchronization code 202, subscriber or paging codes 203, 205 and 207, information codes 204, 206 and 208, and an end code 209. The preamble code 201 is in a pattern "1010 ... " for bit synchronization, and the word synchronization code 202 has a unique pattern for word synchronization. The subscriber code 203, as shown in Figure 2B, is a single 31-bit word consisting of a 16-bit address code 210 and 15 check bits 211. In the information code 204, 206 or 208 consisting of three words, the key code numbers are assigned, for each unit, to 212, 214 and 216 in that order, to which check bits 213, 215 and 217 are added respectively. Herein, 218, 219, 220 and 221 are key code numbers of the first unit, expressed in BCD code.

Figure 2C illustrates the cycle of the battery saving operation of the receiver of Figure 3 for use in the present invention.

In the receiver illustrated in Figure 3, a CPU 4 so controls an electronic switching circuit 10 as to supply power to a radio section 2 and a waveform shaping circuit 3 for a fixed duration of *x* shown in Figure 2C. In this while, the radio section 2, after amplifying radio signals received through an antenna 1, demodulates them into baseband signals. The demodulated signals are converted into rectangular signals by the waveform shaping cicuit 3 and entered into the CPU 4, which receives the input signals in synchronization with a read-in timing pulse in the manner described below, and monitors the emergence of the preamble code 201 (Figure 2A). If no preamble signal is detected within the prescribed period of time, the CPU 4 so controls the electronic switching circuit 10 as to cut off power supply to the radio section 2 and the waveform shaping circuit 3 for a fixed duration of *y* shown in Figure 2C. This battery saving operation is repeated.

Secondly, when the preamble code 201 is detected, the CPU 4 releases its battery saving operation and shifts to detection of the word synchronization code 202 and the subscriber code of its own receiver. Upon detection of a subscriber code identical with a code written into a Programable Read-Only-Memory (PROM) 8, the CPU 4 feeds an alert actuating signal to an oscillator 13, and reads out of a PROM 9 the words which are stored at an address corresponding to a key code number designated by the following information code. Also, the words is expressed in an eight-bit ASCII code.

Thirdly, the CPU 4 temporarily stores in its internal RAM the ASCII code read out of the PROM 9, reads it out by operating a switch 15 and transfers it to a display control/drive unit 5, to which a display control signal is also given.

Fourthly, after detecting the preamble code 201, the CPU 4 resumes its battery saving operation upon detection of the end code 209. The display control/drive unit 5 internally processes the ASCII code entered (i.e. decodes it with a segment decoder and stores it in a data memory, whose output is connected to an LCD driver) and, in response to the display control signal from the CPU 4, drives each segment of an LCD unit 6 to have its displaying function performed.

Meanwhile the oscillator 13, in response to the alert actuating signal entered, starts low frequency oscillation and amplifies the level of this oscillation to drive a speaker 14, which converts the input signals into sounds. A clock oscillator 7 generates a source clock for the CPU 4 and control/drive unit 5. The output of a battery 12 is boosted in voltage by a DC—DC converter 11 and supplied to the circuits 4, 5, 8, 9 and 13.

In the CPU 4 of Figure 4 (for instance a μPD 7502 unit manufactured by NEC), reference numeral 401 represents an instruction decoder, which is a central component to control each block for deciphering codes to be executed and executing the instructions thereby expressed. A Read-Only-Memory (ROM) 402 is a program memory in which are stored groups of instructions to be executed, and reference numeral 403 represents a program counter (PC) for addressing the programs written into the ROM 402. Normally, every time an instruction is executed, the count of the PC 403 is automatically incremented according to the number of bytes of the instruction, and is cleared by a jump instruction or a subroutine instruction.

Reference numeral 405 represents an input port for entering rectangular signals CD from the waveform shaping circuit 3; 406, an output port for supplying the control signal BSC to the electronic switching circuit 10 and the alert actuating signal ALT to the oscillator 13; 407, an output port for supplying an addressing signal for reading out of the ROMs 8 and 9; 408, an input port for entering the addressed contents of the ROMs 8 and 9; 409, an output port for supplying a chip select signal CS1 to set the ROM 8 in action and another chip select signal CS2 to set the ROM 9 in action; 410, an arithmetic and logic unit (ALU) for storing the results of operation and exchanging data with memory I/O ports and registers; 411, a counter circuit; 412, a timer/counter which is a comparator/equality unit; 413, a timer control circuit for setting the timer cycle; 414, a serial interface for supplying an output signal SO to transfer serial data to the display control/drive unit 5 and a synchronizing signal SCK to enable the LCD control/drive unit 5 to read serial data in; 415, an internal data bus by way of which data are transmitted and received between blocks; and 416 and 417, S—R type flipflops.

This CPU 4 functions in the following manner. The instruction decoder 401 performs various processes by reading in data stored in the program memory 402 as addressed by the program counter 403 and decoding the data so read. For instance, it reads in signals CD by way of the I/O port 405, and alters the data contents of the data memory 404 or the timer controller 413 by way of the data bus 415. The output signal (source clock signal) CLK of the oscillator 7 is connected to the clock input of the counter 411, which counts up in accordance with the input clock and whose output is led to the timer/counter 412. The timer/counter 412 compares the output of the counter 411 and data set in the timer control 413 and, when it founds them identical sends a detection signal S_1 to a flipflop 416 to set it, whose output signal S_2 is connected to the internal data bus and can be detected by executing a specific instruction. Similarly, the flipflop 417 detects the leading edge of the rectangular signals or pulses CD from the circuit 3, thereby providing a signals S_3. Upon detection of the signals S_2 and S_3, reset signals R_1 and R_2 are supplied from the instruction decoder 401, and the flipflops 416 and 417 are thereby reset.

Next, the battery saving operation and receiving operation will be described in detail with reference to the flow charts of Figures 5 to 10.

First, at step 30, the CPU 4 starts its operation to receive radio signals by supplying power to the radio section 2 and waveform shaping circuit 3 by way of the electronic switching circuit 10 in response to the control signal BSC. Next, at step 31, a register 4d1 of the data memory 404, in which rectangular signals CD from the waveform shaping circuit 3 are stored (The CPU 4 reads in rectangular signals CD bit by bit and stores the data read in on a bit-by-bit basis. Therefore in this data memory region are stored required bits of the latest rectangular signals CD), is cleared. Then, at step 32, data corresponding to a time *x*, required for detecting the preamble, are set in a counter 4d2 of the data memory 404 to monitor the time *x*. Monitoring of this time *x*, as step 38 shows, is accomplished by subtracting 1 from the data in said *x* counter in the data memory 404 at fixed intervals and checking whether or not the data have become zero or smaller. At step 33, to synchronize a read-in timing pulse with the rectangular signals CD, reference data are set in the timer controller 413. These data can be obtained in a unitary manner to make the cycle of each bit of the signal code strings to be received coincide with that of the read-in timing pulse.

Step 34, which is pretreatment for monitoring the leading edges of rectangular signals CD at the following step 35, resets the flipflop 417 which is set by the leading of a rectangular signal CD and clears a register 4d3 in the memory 404 which is used for monitoring the leading edges of rectangular signals CD.

At step 35, as will be described in greater detail hereunder, the leading edge of a rectangular signal CD is detected by way of the flipflop 417, and the output datum of the counter 411 at that time (the length of time required for a rectangular signal CD to rise, as measured from a read-in timing pulse) is stored in a part of the data memory 404 to register information needed for correcting the timer cycle at step 37. Completion of the timer operation set at step 33 is monitored through the output S_2 of the flipflop 416; upon completion of the timer operation, a rectangular signal CD is read in through the I/O port 405, and the datum is stored, shifted by one bit, by way of the internal data bus 415, in a storage area 4d1 of the memory 404 initially cleared at step 31.

At step 36, it is determined whether or not the content of the memory area 4d1 coincides with the preamble code 201 (the reference preamble code is registered in the program memory 402 in advance). If coincidence is confirmed , the process moves on to step 44 and enters the reception flow from the word synchronization code 202 on. Conversely, if no coincidence is observed, the process goes on to step 37 to continue detection of the preamble code 201. At step 37, to correct any advance or delay of the read-in timing pulse in accordance with the information collected at step 35, cycle adjustment for one bit is achieved by setting in the timer controller 413 the data set at step 33 and appropriately corrected. Further details will be given hereunder. At step 38, 1 is subtracted from the *x* counter for determining the preamble code detection time set at step 32. Then at step 39, whether or not the *x* counter has finished counting is checked; if it has, the process moves on to step 42 to immediately cut off power supply to the radio section 2 and waveform shaping circuit 3 by means of a control signal BSC, and at step 43 the system stands by (in a battery saving operation) for a duration of *y*. After the time *y* has elapsed, the process returns to step 30 to repeat the aforementioned preamble code detecting operation. On the other hand, at step 39, if the *x* counter has not finished counting yet, the process goes on to step 40, at which the output S_2 of the flipflop 40 is monitored. If the output S_2 is "H (high level)", the process goes on to step 41, at which the signal CD is read in the register 4d1 through the I/O port 465 and the process goes on to step 33.

Next, the procedure required for bit synchronization, or step 35, and the "timer controller 413 correction" of step 37, both referred to in Figure 5, will be described in further detail with reference to the flow charts of Figures 6 and 7.

Figure 6 is a flow chart for explaining the procedure for "monitoring of data leading edges". At step 351 is monitored the leading edge of a rectangular signal CD. The leading edge of a rectangular signal CD sets the flipflop 417, and S_3 gives an "H" output, which is monitored at step 351. If the S_3 output is not "H", the process moves onto step 352, and judgment is made as to whether or not the S_2 output is high, i.e. whether or not the single-bit timer has completed operation. If the S_2 output is not high, the process jumps back to step 351, and the foregoing procedure is repeated until the single-bit timer completes operation.

Meanwhile, if the S_2 output is judged to be "H" at step 352, the process goes on to step 358, at which, as at step 41, a rectangular signal CD is read in and stored in a rectangular signal storing register 4d1 to complete the procedure.

If the S_3 output is judged to be "H" at step 351, the process moves ahead to step 353, at which data "1100" are set in a flag storing register 4d4. Then at step 354, the output of the counter 411 at this time is stored in a register 4d5 by way of the internal data bus 415. Next at step 355, it is again checked whether or not the S_3 output is "H". If the S_3 output is found "H", the process goes on the step 356, at which the data set in the flag storing register 4d4 at step 353 are turned "1000" to make it known that two or more data leading edges have taken place in a bit, followed by a jump to step 357. If the S_3 output is not found "H", the process moves on to step 357 to judge whether or not the single-bit timer has completed its operation and, if it has not, returns to step 355 or, if it has, jumps to step 358. This operation charted in Figure 6 enables the leading edge timing of input rectangular signals to be known from the data contents of the register 4d5 and the number of leading edges of input rectangular signals in a single-bit cycle to be known in the range of 0, 1 or more than 1.

Figure 7 is a flow chart of the procedure for "correcting the single-bit timer" to adjust the phase of the read-in timing pulse on the basis of information obtained by the procedure for "monitoring of data leading edges" charted in Figure 6. At step 371, it is judged whether or not the data contents of the flag register 4d4 are "1100", i.e. whether or not only one rectangular signal leading edge has taken place in said procedure for "monitoring of data leading edges". If the answer is "No", the timer controller 413 is not corrected and the procedure is completed here. In other words, the phase of the read-in timing pulse is kept as it is. If, conversely, the answer is "Yes", the process moves on to steps 372 and 373 to judge, with reference to the rectangular signal leading edge timing data in the register 4d5, whether the read-in timing pulse is in or out of phase and, if out, whether forward or backward. If it is found forward, the phase of the read-in timing pulse is delayed by 1/8 bit at step 373 by setting data corresponding to 9/8 bits in the timer control circuit 413. If, on the contrary, it is found backward, the phase of the read-in timing pulse is advanced by 1/8 bit at step 374 by setting data corresponding to 7/8 bit in the timer control circuit 413. If the pulse is found in phase, the timer control circuit 413 is not corrected and therefore the phase of the read-in timing pulse is kept as it is. The range in which the read-in timing pulse is judged to be synchronized is where the rectangular signal leading edge timing data in the register 4d5 correspond to anywhere between 3/8 bit and 5/8 bit (the median being 4/8 bit).

Figure 8 is a flow chart for explaining the procedure for detection of the word synchronization code 202. This procedure is roughly similar to detection of the preamble code 201, charted in Figure 5, and differs from it in that data corresponding to a word synchronization code 202 detecting time α are set at step 46 and that the word synchronization code 202 is detected at steps 50 and 56. All other steps from 47 to 55 respectively correspond to steps 33 to 41 of Figure 5. Detection of word synchronization by the two steps, 50 and 56, is to check rectangular signals CD, bit by bit, whether or not any one of them is the word synchronization code 202. Thereby is achieved the detection of the

word synchronization code 202, which has a unique pattern differing from the I/O pattern of the preamble code 201. (The reference word synchronization code 202 is registered in the program memory 402 in advance). Upon detection of the word synchronization code 202, the battery saver control signal BSC is set to "Battery Saver OFF" and latched at step 57. Next at step 58, the process jumps to detection of the subscriber code 203.

Figure 9 is a flow chart for explaining the procedure for detection of the subscriber code 203. At step 60, the chip selector control signal CS1 of the ROM 8 is made high (usually in a waiting state, both CS1 and CS2 are made low and no contents of the ROM are read out), and the subscriber code written at a predetermined address in the ROM 8 is read out and set in a register 4d6. Next at step 61, as at step 31, the storing register 4d1 is cleared, and at step 62 data for a time β corresponding to 31 bits of the subscriber code 203 are set in the register 4d2. At step 63, to synchronize rectangular signals CD following the read-in timing pulse of the timer controller 413 corrected at step 51 immediately preceding the detection of the word synchronization code 202, data are set in the timer controller 413. At step 64 is conformed a single-bit time out, and at step 65 the rectangular signal CD at this time is read in and stored in the register 4d1. Then at step 66, one bit is subtracted from the counter 4d2 set at step 62. At step 67 is confirmed a 31-bit time out, and at step 68 it is determined whether or not the 31-bit rectangular signals stored in the register 4d1 coincide with the subscriber code set in the register 4d6. If the difference is two bits or greater, the subscriber code is judged not to have been received yet, and the process moves ahead to step 69, at which is monitored the end code 209 registered in advance in the program memory 402. If the received signal is not the end code 209, the process returns to step 60 and newly goes on to waiting for the next rectangular signal CD, or if it is the end code 209, the process jumps to step 42 to return to the battery saving state. If the difference is one bit, like in the case of complete coincidence, the received signal is judged to be the subscriber code, and the process moves ahead to step 71, at which the alert actuating signal ALT is issued to the oscillator circuit 13, and further to step 72 for progress to detection of the information code.

Figure 10 is a flow chart for explaining the procedure for detection of the information code. At step 73, data for a time γ_1 corresponding to three words or (31×3=) 93 bits of the information code are set in a counter 4d2. At step 74, like at step 31, the rectangular signal storing register 4d1 is cleared. At step 75 are stored in another counter 4d6 data for a time γ_2 corresponding to 31 bits equivalent to one word. Procedures taken at steps 76 through 79 are the same as those at steps 63 through 66 described above. At step 80, one bit is subtracted from a counter 4d2. Then at step 81 is checked a 31-bit time out; if the time out is confirmed, a 93-bit time out is checked at step 82, and if this time out is not confirmed, the process moves ahead to step 83. At step 83 is checked whether or not the 31-bit rectangular signal in the register 4d1 is the end code 209, and if it is found the end code 209, the process jumps to step 42 or, if it is not the end code 209, moves on to the step 84 to check whether or not it is a BCH (31, 16) code. If it is a BCH (31, 16) code, the information bit is stored in a register 4d7, followed by a jump to step 74. If it is not, a jump to step 60 takes place, resulting in a state of waiting for the subscriber code. Meanwhile, if the γ_1 timer takes a time out at step 82, the same procedures are followed at steps 88 and 89 as at steps 83 and 84, respectively. If, at step 89, the third word also is found a BCH (31, 16) code, its information bit is stored following those of the first and second words already stored at step 85, and the process goes ahead to step 91.

Here at steps 84 and 89 are accomplished single-error corrections, details on which will be given below. The parity check matrix given in Figure 11 is stored in the program memory 404. Supposing the input data $I=a_1a_2a_3 \ldots a_{31}$, a representing each bit of the data is either 1 or 0. These data and said parity check matrix are subjected to matricial operation, or the logical product of each a_n and the corresponding C_n is calculated, and modulo 2-added for each element:

$$S=a_1C_1 \oplus a_2C_2 \oplus \ldots a_{31}$$

The resultant matrix S is made the syncrome matrix. If this syndrome matrix S is 0, there is no error in error in its data. If S is not 0, it is checked with the parity check matrix C, and if $C_n=S$, the corresponding datum a_n is wrong. If a_n is given as 1, it is corrected to 0, and vice versa. The absence of C_n corresponding to S indicates the presence of an incorrectible error in the data. Error correction is achieved in this procedure. The foregoing procedures are logical operations and therefore programmable. The principle of error correction in this manner is disclosed in Shu-lin, "An Introduction to Error Correcting Codes", 1970, Prentice-Hall Inc., among others. If, as a result of such error correction, the first bit is found erroneous, its content is rewritten and stored in a data memory 4d7. Hitherto has been described how signal code strings are received.

Next will be explained the relationship between key code numbers and words. The key code numbers altogether consist of 12 digits, every two of which make up a word column. Thus the whole word group comprises six word columns. The relationship of correspondence between the key code number constituting each word column and words is determined in advance. Since each word column number herein consists of two digits, 100 words are assigned to each word column. For instance, key code numbers and words are determined as tabulated below for word column I represented by the first

two digits, word column II represented by the second two digits, word column III, word column IV and so forth.

Key code number	*Word column I*	*Word column II*	*Word column III*	*Word column IV*	*Word column V*	*Word column VI*
00	Telephone	in	home	on	AM	1
01	Go	to	office	at	PM	2
02	Come	on	factory	until	right	3
03	Contact	back	here			4
04	Stay	.	.	.	.	now
05	Wait	.	.	.	.	.
06	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.

When words corresponding to any of these key code numbers are written into the ROM 9, addresses in the ROM 9 are made to correspond to the foregoing table. Words corresponding to the addresses are written in, each character in an 8-bit ASCII code, with the final characters of word columns I through V being followed by NUL as end symbol and that of word column VI by an asterisk as end symbol.

In display control/drive unit 5 (for example, μPD7225G unit marked by NEC), reference numeral 511 represents a serial interface, comprising an eight-bit serial register and a three-bit SCK counter. The serial counter takes in one bit of signals so at the leading edge of each clock SCK fed from the serial interference 414 (See Figure 4), and at the same time the SCK counter counts up by +1 at a time. When the counter has counted up eight, entry of any more signal SO is prohibited, and the contents of the serial register are supplied to a command/data register 512, which latches data transferred from the serial register. After the data are latched, the command/data register 512, following command/data designation given by a signal CONT fed from the port 406 (see Figure 4), supplies the latched data to a command decoder 513 if command is designated, or to a segment decoder 514 if data is designated. The signal CONT designates command at "High" and data at "Low". The command decoder 513 takes in and decodes data entered from the command/data register 512, and controls the display control/drive unit 5. The segment decoder 514 is a decoder for 14-segment type LCD, whose input data and display pattern comprise the eight-bit ASCII code. Reference numeral 515 represents a data memory for storing display data. The μPD7225G unit at this stage has a capacity of 32×4 bits, requires a 4×4-bit address per character, and accordingly has a capacity of eight characters. Reference numeral 516 represents a display data latch, which stores driving data for an LED driver 517, composed of 32×4 bits having addresses in a relationship of one-to-one correspondence with the data memory 515. At the leading edge of signal CS_3 fed from the port 406 (See Figure 4), the whole contents of the data memory 515 are transferred to the display data latch 516 to renew the indication of the LCD 6. Display data written into the display data latch 516 are successively selected under the control of a timing control and OSC circuit 518 and supplied as output after being converted into segment drive signals.

The LED driver 517, consisting of a segment driver and a common driver, generates segment drive signals and common drive signals in response to control signals from the timing control and OSC circuit 518. The common drive signals, designated for time division, successively drives the common electrodes of the LCD. In this embodiment, four-way time division is used. The timing control and OSC circuit 518 generates and supplies to the driver 517 and LCD driving voltage. The OSC circuit also generates the system clock. SEG represents 32 drive output signals; and COM, four common drive output signals.

Hereunder will be described in detail how serial data SO are shifted from the CPU 4 (Figure 4) to the display control/drive unit 5 with reference to time charts of Figures 13A and 13B.

The serial data SO, synchronized with the serial clock SCK, are entered in eight-bit units (or one byte) at the leading points of the most significant bit (MSB). As turning CS_3 low results in a low level also for BUSY, when the BUSY signal comes up high after the completion of internal processing (clearing the SCK counter and data pointer), the transfer of the first bit (MSB) is begun in synchronization with SCK. In response to the leading edge of SCK, the serial data are transferred bit by bit to the serial register in the serial interface 511, and entry of eight serial clocks results in a transfer of all the eight-bit data to the serial register. At the leading edge of the eighth serial clock, BUSY turns low to take in the condition of CONT, and the command/data designation is achieved for the eight-bit data. After that, the contents of the serial register are taken into the command/data register 512.

When two or more bytes of the serial data are to be consecutively entered, CS_3 is kept low until the entry of all the bytes is completed as shown in Figure 13B. Upon completion of the entry of each

byte BUSY turns low, and when a serial datum is taken from the serial register into the command/data register 512 BUSY turns high, so that entry of the next serial dataum is made possible.

By raising CS_3 after the entry of all the serial data is completed, the contents of the data memory 515 are transferred to the display data latch 516.

The display action will be described in detail hereunder with reference to the flow chart of Figure 14. At step 301, whether or not display is started is judged according to the state of the display start switch 15 (See Figure 3), and if the switch 15 is turned ON, the process moves ahead to step 302. At step 302, eight bits following the MSB are read out of the register 4d7 in the data memory 404, CS_2 is turned ON. A word (sequence of characters) corresponding to the address of the key code number of word column I in the ROM 9 (Figure 3) and expressed in an ASCII code is read out and stored in a register 4d8. At step 303, data (for the first eight characters) stored in the register 4d8 are fed to the diplay control/drive unit 5, and they are displayed at step 304. At step 305, information on the turning-ON of the switch 15 to start scroll display is monitored, and if it is ON, the process goes ahead to step 306, where a time of 0.3 second is set in a timer 4d9, followed by monitoring of a time out at step 307. Upon time out taken in 0.3 second, the process moves on to step 308, at which the display control/drive unit 5 is reset, the display is turned off, and data in the register 4d8 for the first eight characters are again fed to the display control/drive unit 5 to be displayed, with the first character of the previously displayed being cleared and each of the following characters being shifted in address by one character equivalent toward the top position. Upon detection of NUL end symbol of word column I at step 310, the process goes ahead to step 313 and 314, and after displaying for 0.3 second as at steps 306 and 307, further ahead to step 316 for a jump to the key code display flow for for word group 2. If no NU1 symbol is detected, the process returns to step 308 after display for 0.3 second at steps 311 and 312.

Figure 15 is a flow chart for explaining the displaying of word groups 2 through 6. At step 316, the immediately following eight bits in the register 4d7 are read out, and a word (a sequence of characters) corresponding to the key code number of the following word group is read out of the ROM 9 and stored at the addeess following the previous sequence of words in the register 4d8. At step 317, the first character in the register 4d8 is cleared, and the following characters are shifted in address by one character equivalent each toward the top position. Then the first eight characters are stored in the LED control/drive unit 5 and displayed at step 318. At 319 is monitored an asterisk, that is, the end symbol of word column VI. If no asterisk is detected, the process moves ahead to step 320 to monitor end symbol NUL of the next word column. If NUL is detected, the process returns to step 316 after displaying for 0.3 second at step 321. If NUL is not detected, the process goes ahead to step 322 and, after displaying for 0.3 second, further ahead to step 323, at which the first character in the register 4d8 is cleared and the following characters are shifted in address by one character equivalent each toward the top position. Then the first eight characters are stored in the LED control/drive unit 5, and displayed at step 325. At 325 is monitored an asterisk, and if no asterisk is detected, the process moves on to step 326 to monitor NUL. If NUL is detected, the process returns to step 316 after displaying for 0.3 second at step 327. If NUL is not detected, the process returns to step 317 after displaying for 0.3 second at step 328. At these steps 321, 322, 327 and 328, similar procedures to those at step 306 and 307 are taken.

Figure 16 is a detailed flow chart of steps 319 and 325. At step 329, an asterisk is monitored, and if no asterisk is detected, the process ends this procedure. If an asterisk is detected, eight characters are displayed for 0.3 second at step 330 (in similar procedures to those at steps 306 and 307), and all the data in the register 4d8 are cleared, followed by a jump to step 301.

Figure 17 is a block diagram of the oscillator circuit 13. In response to an alert actuation signal ALT, a one-shot multi-vibrator 131 is actuated to operate for a certain period of time, and its output signal actuates an oscillator 132, whose output is amplified by an amplifier 133 to drive the speaker 14.

In the above described process, upon detection by this receiver of a key code number "020301010103" sent by said caller, an alert tone is issued for a certain period time from the speaker 14 and, because the following relations of correspondence hold,

02→Word column I,	number 02→COME
03→Word column II,	number 03→BACK
01→Word column III,	number 01→OFFICE
01→Word column IV,	number 01→AT
01→Word column V,	number 01→PM
03→Word column VI,	number 03→4

"COME" is indicated on the LCD display when the display switch 15 of the receiver is pushed once, another push of the display switch resulting in scroll display of "COME BACK OFFICE AT PM 4*".

Incidentally, the ROMs 8 and 9 can be integrated into a single ROM if the subscriber code storing section, key code number corresponding word (character sequence) storing section and addresses are separated from each other.

Although a word is used in the foregoing description to correspond to a key code number, a sentence can correspond to a key code number by using a blank character symbol (ASCII) for word connection.

As hitherto stated, the present invention makes possible combination of not just characters but also words, transmission of sufficient information for routine communication, repeated confirmation of information and moreover more efficient utilization of channels than voice transmission.

Claims

1. A paging receiver comprising: first means for receiving and demodulating a carrier wave modulated with a paging signal code, and a plurality of information key codes corresponding to a plurality of words, respectively; second means for decoding said information key codes when its own paging signal code is detected; third means for storing in advance a plurality of words corresponding to said information key codes, respectively; fourth means for reading out of said third means words corresponding to the decoded information key codes; and fifth means for displaying the read-out words.

2. A paging receiver claimed in Claim 1, comprising sixth means for providing an alert tone when its own paging signal code is detected.

3. A paging receiver as claimed in claim 1 substantially as described herein with reference to Figure 3 and to any one of Figures 2C and Figures 4—17 of the accompanying drawings.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1981. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.