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(54) **VACUUM JACKETED ELECTRODE FOR PHASE CHANGE MEMORY ELEMENT**

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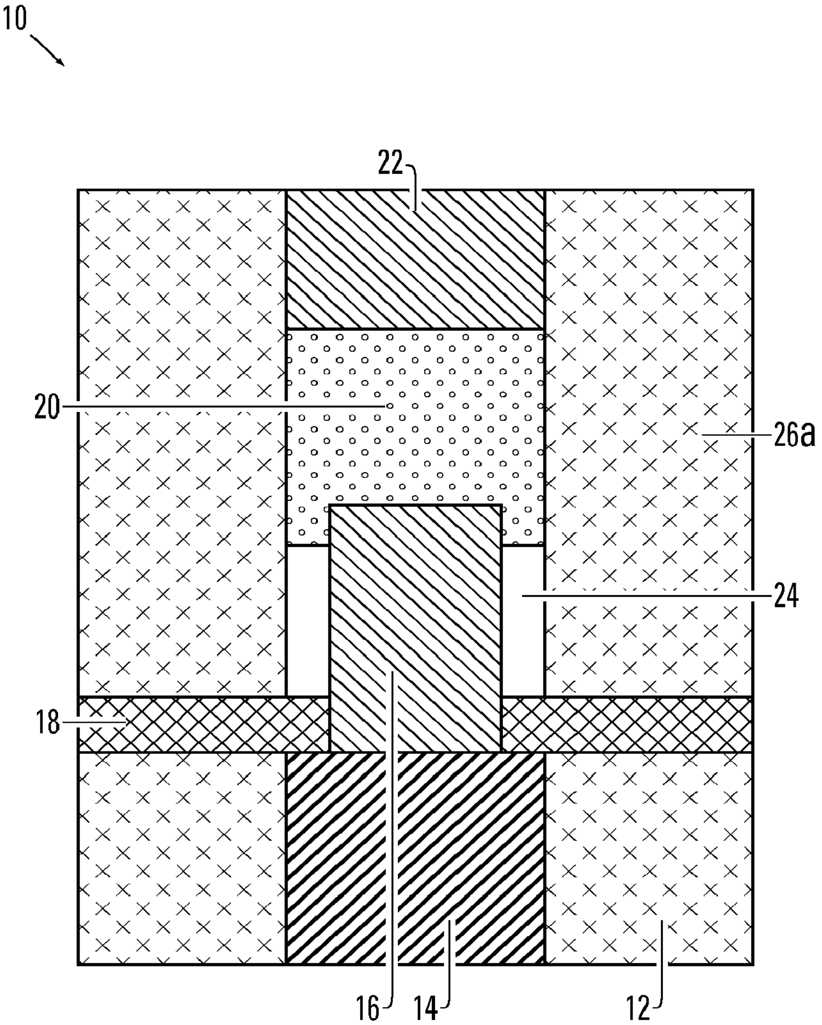
(57) **ABSTRACT**

A memory device having a vacuum jacket around the first electrode element for improved thermal isolation. The memory unit includes a first electrode element; a phase change memory element in contact with the first electrode element; a dielectric fill layer surrounding the phase change memory element and the first electrode element, wherein the dielectric layer is spaced from the first electrode element to define a chamber between the first electrode element and the dielectric fill layer; and wherein the phase change memory layer is sealed to the dielectric fill layer to define a thermal isolation jacket around the first electrode element.



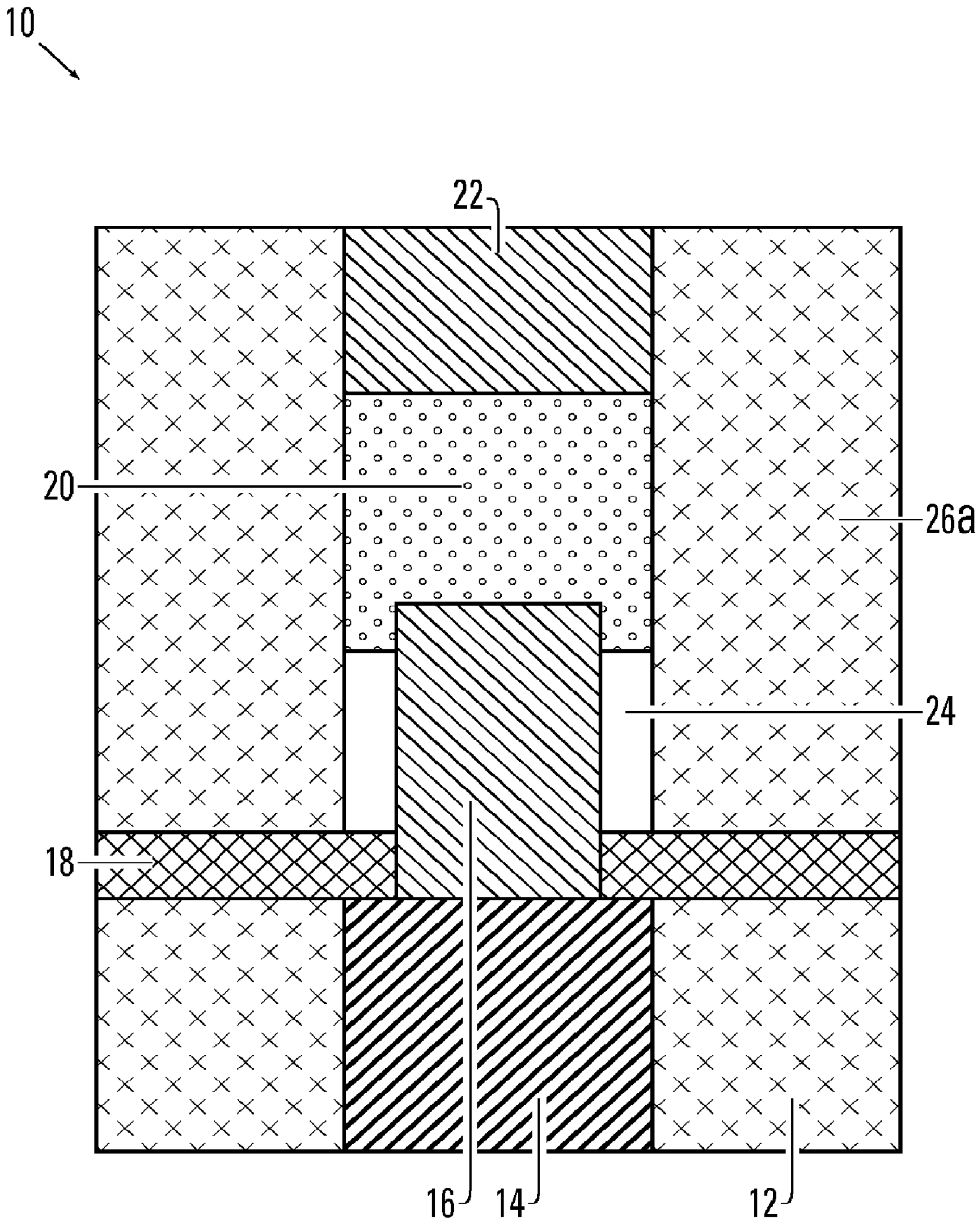


FIG. 1

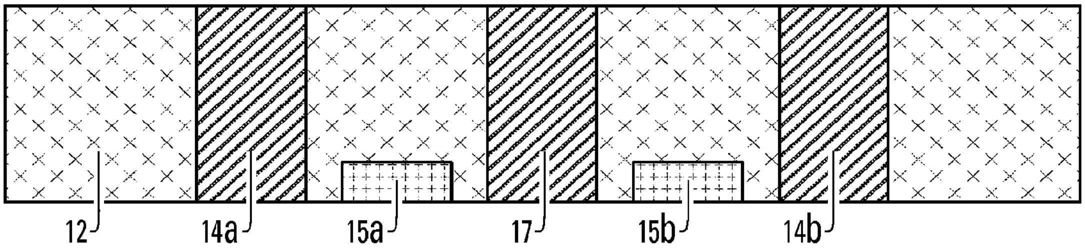


FIG. 2A

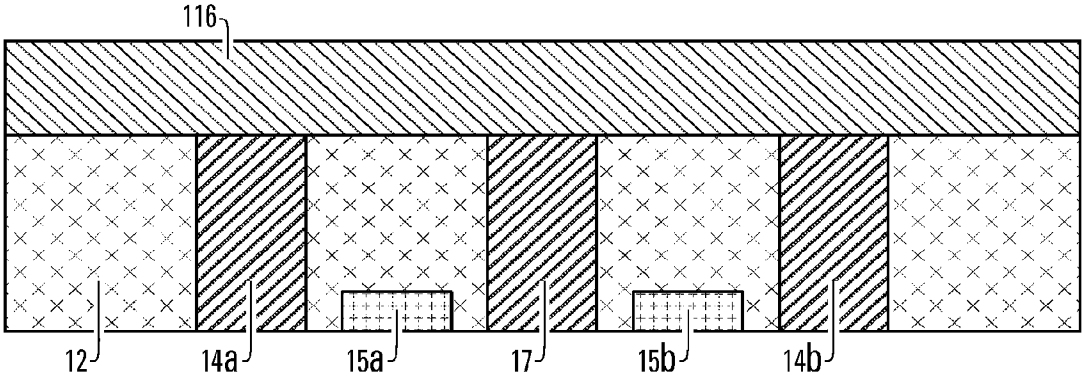


FIG. 2B

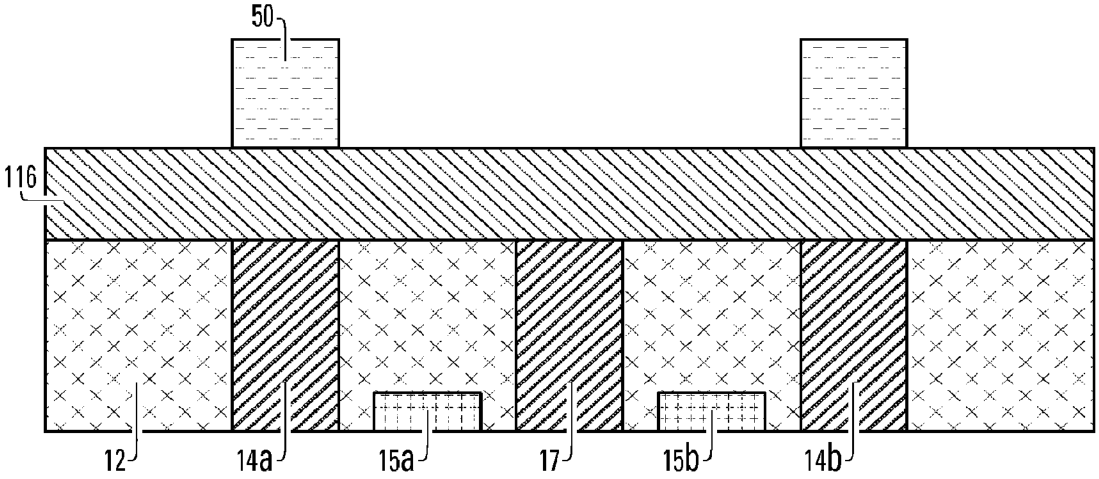


FIG. 2C

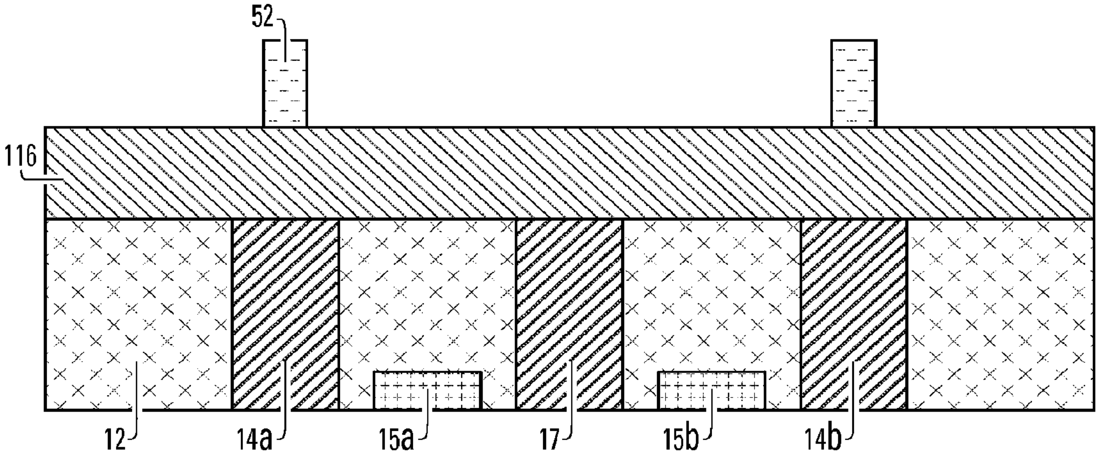


FIG. 2D

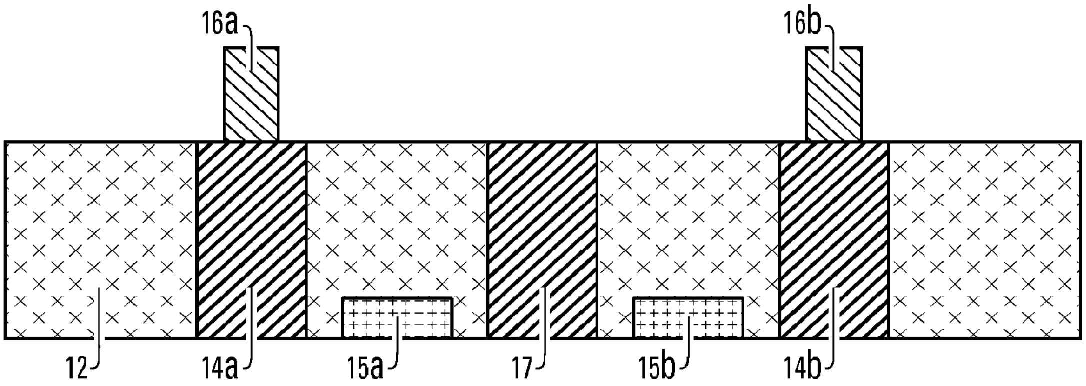


FIG. 2E

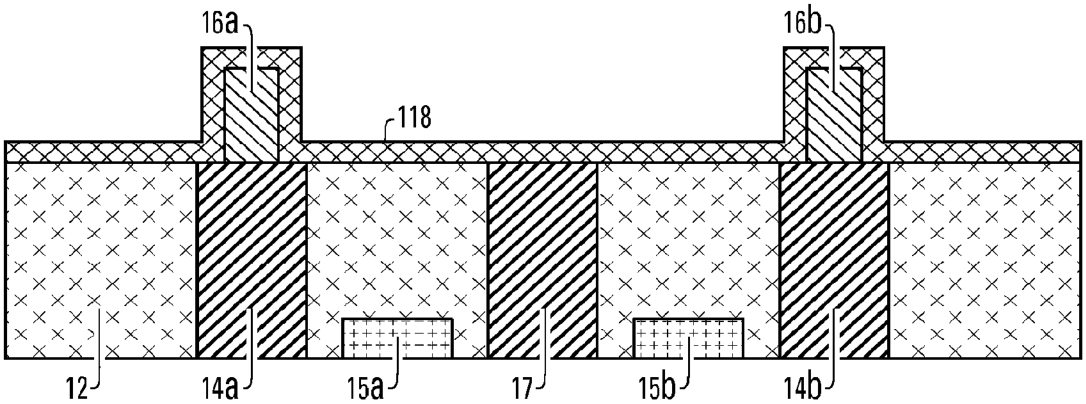


FIG. 2F

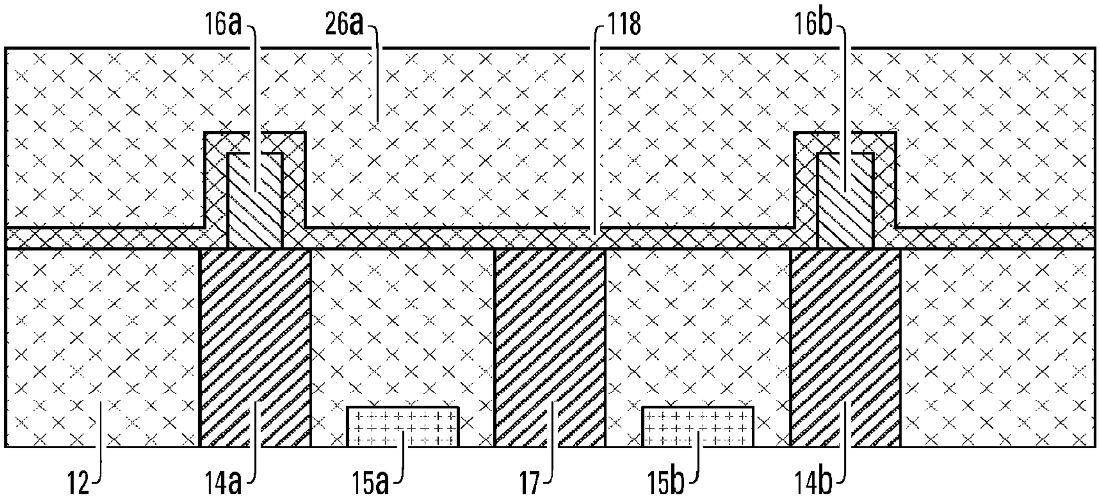

16a
26a
118
16b
12
14a
15a
17
15b
14b

FIG. 2G

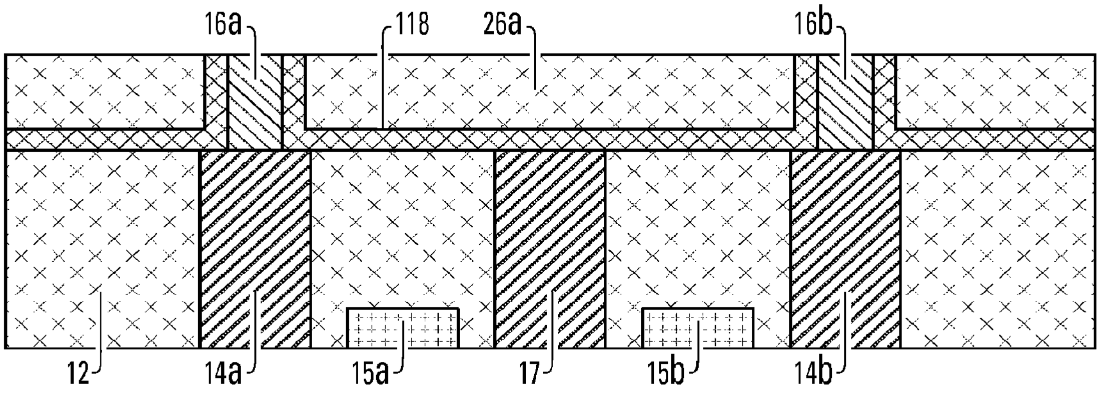

16a
118
26a
16b
12
14a
15a
17
15b
14b

FIG. 2H

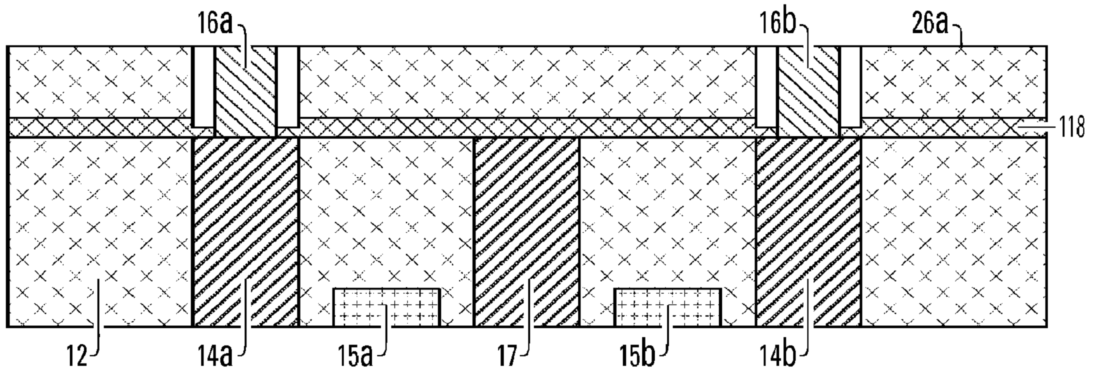

16a
16b
26a
118
12
14a
15a
17
15b
14b

FIG. 2I

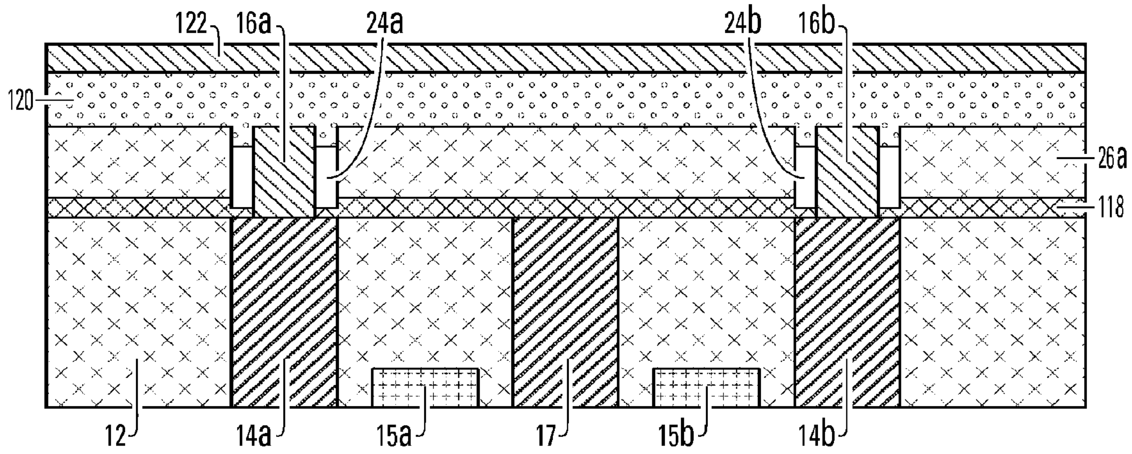

122
16a
24a
24b
16b
120
26a
118
12
14a
15a
17
15b
14b

FIG. 2J

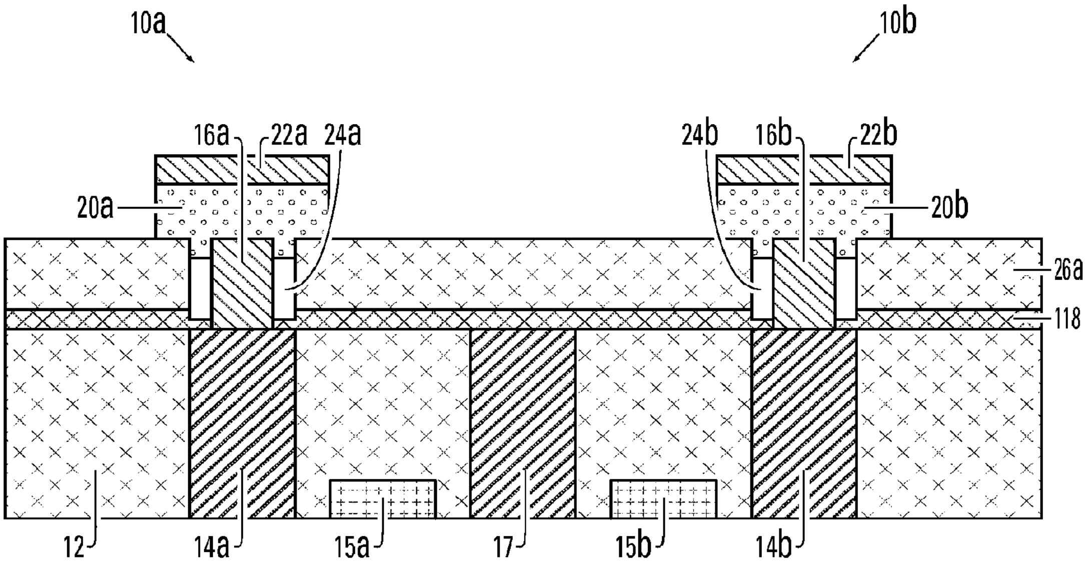

10a
10b
16a
22a
24a
24b
16b
22b
20a
20b
26a
118
12
14a
15a
17
15b
14b

FIG. 2K

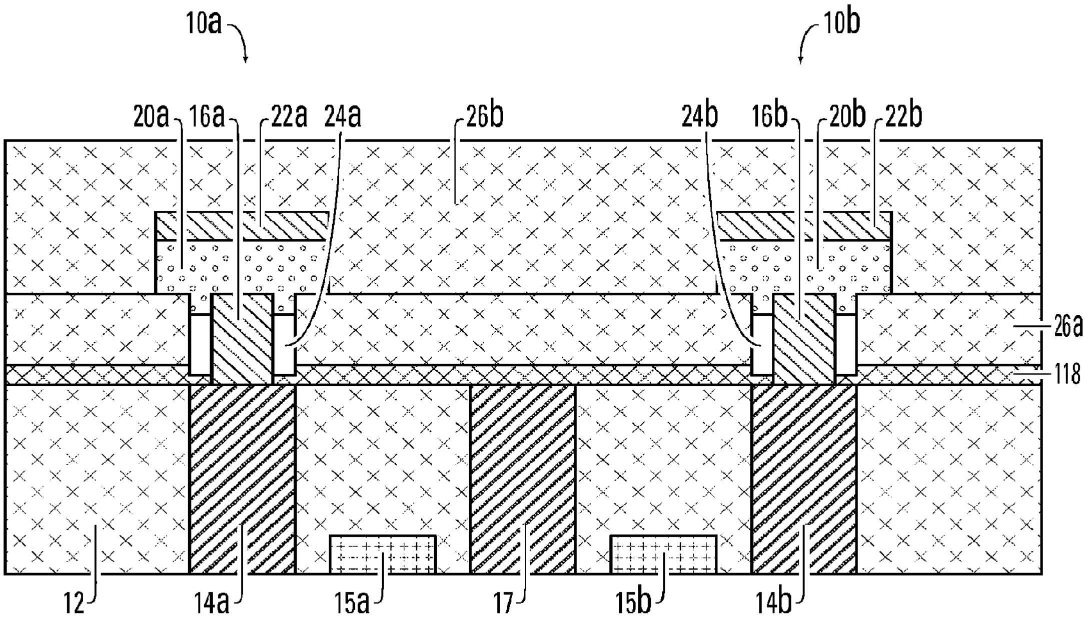

10a
10b
20a
16a
22a
24a
26b
24b
16b
20b
22b
26a
118
12
14a
15a
17
15b
14b

FIG. 2L

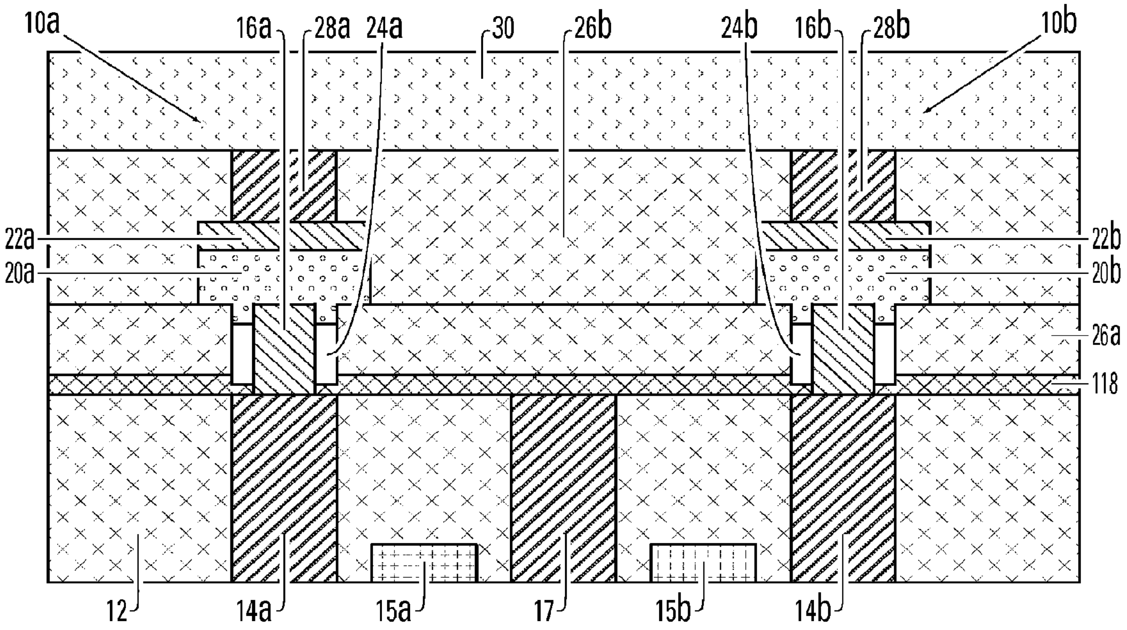

10a
16a
28a
24a
30
26b
24b
16b
28b
10b
22a
20a
22b
20b
26a
118
12
14a
15a
17
15b
14b

FIG. 2M

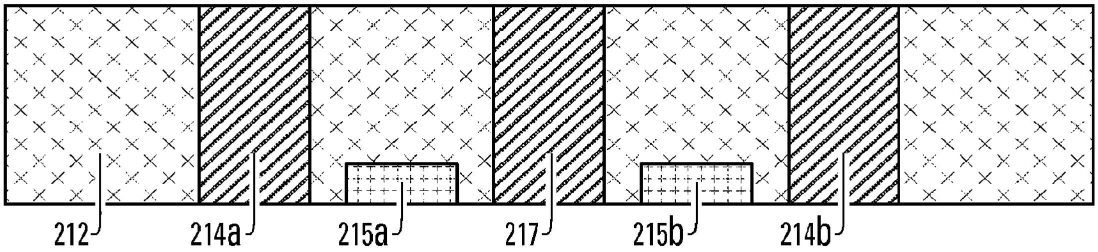


FIG. 3A

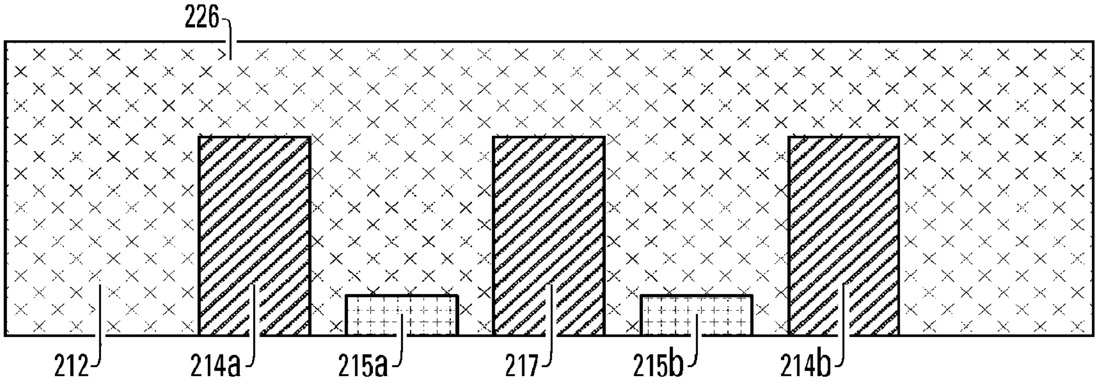


FIG. 3B

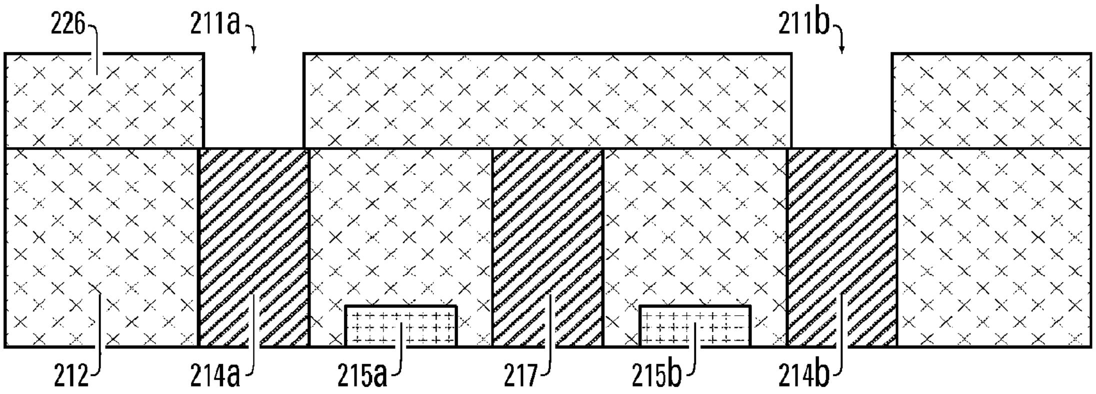

226
211a
211b
212
214a
215a
217
215b
214b

FIG. 3C

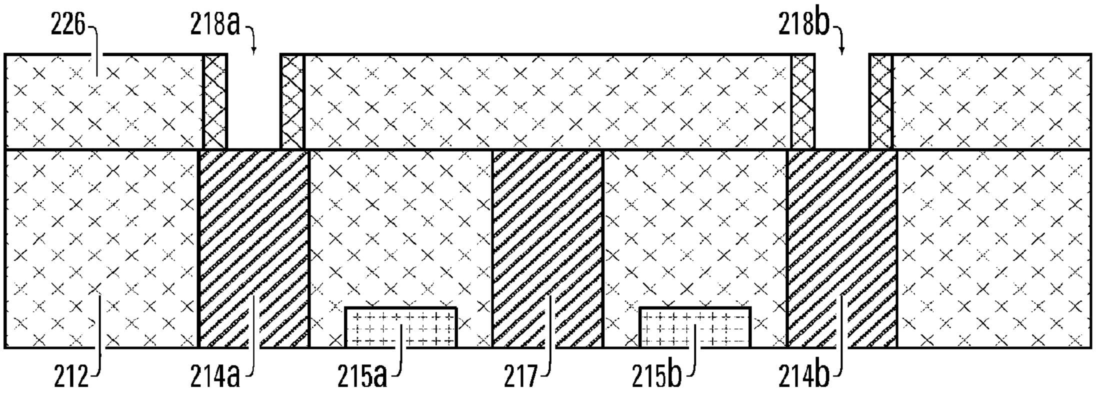

226
218a
218b
212
214a
215a
217
215b
214b

FIG. 3D

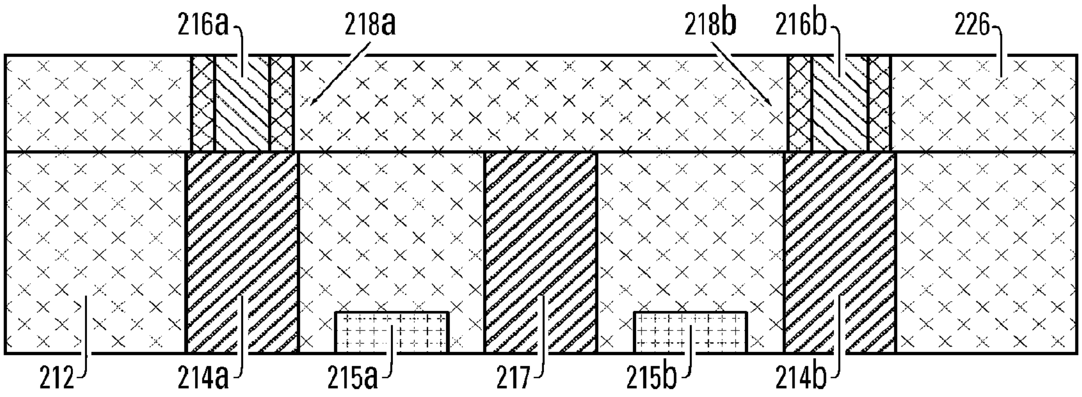

216a
218a
218b
216b
226
212
214a
215a
217
215b
214b

FIG. 3E

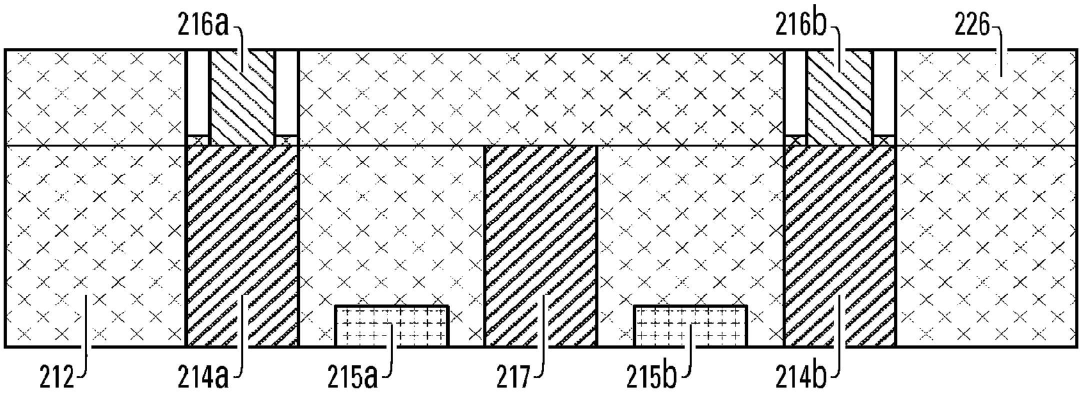

216a
216b
226
212
214a
215a
217
215b
214b

FIG. 3F

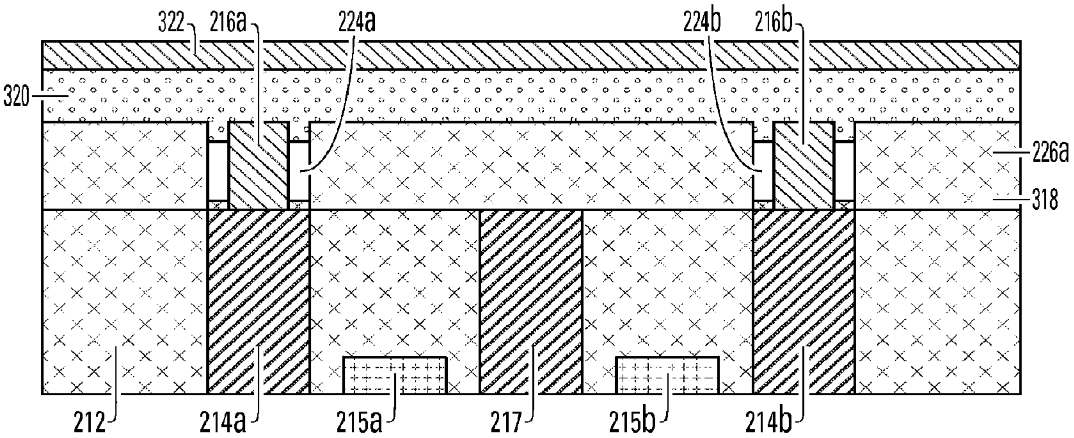

322
216a
224a
224b
216b
320
226a
318
212
214a
215a
217
215b
214b

FIG. 3G

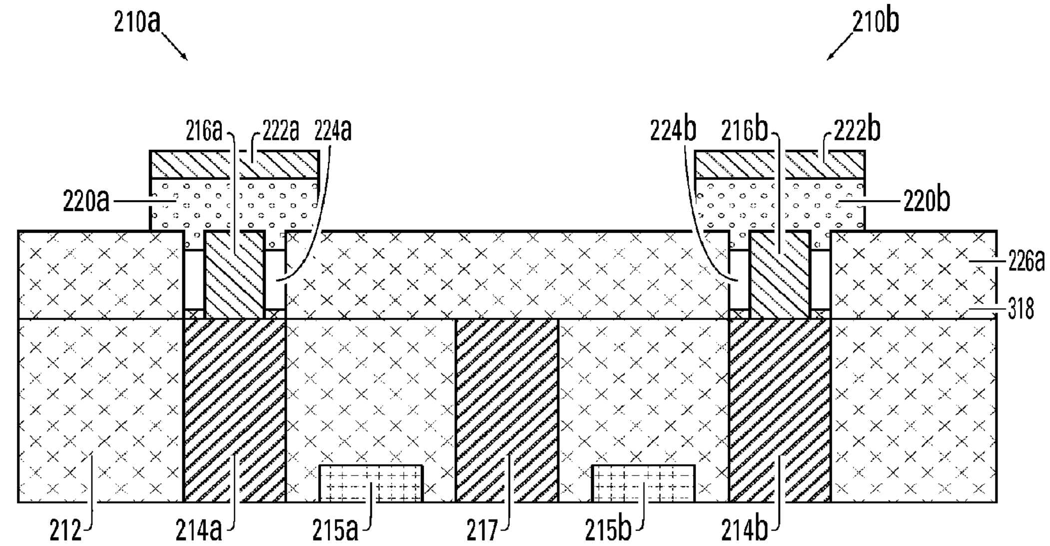

210a
210b
216a
222a
224a
224b
216b
222b
220a
220b
226a
318
212
214a
215a
217
215b
214b

FIG. 3H

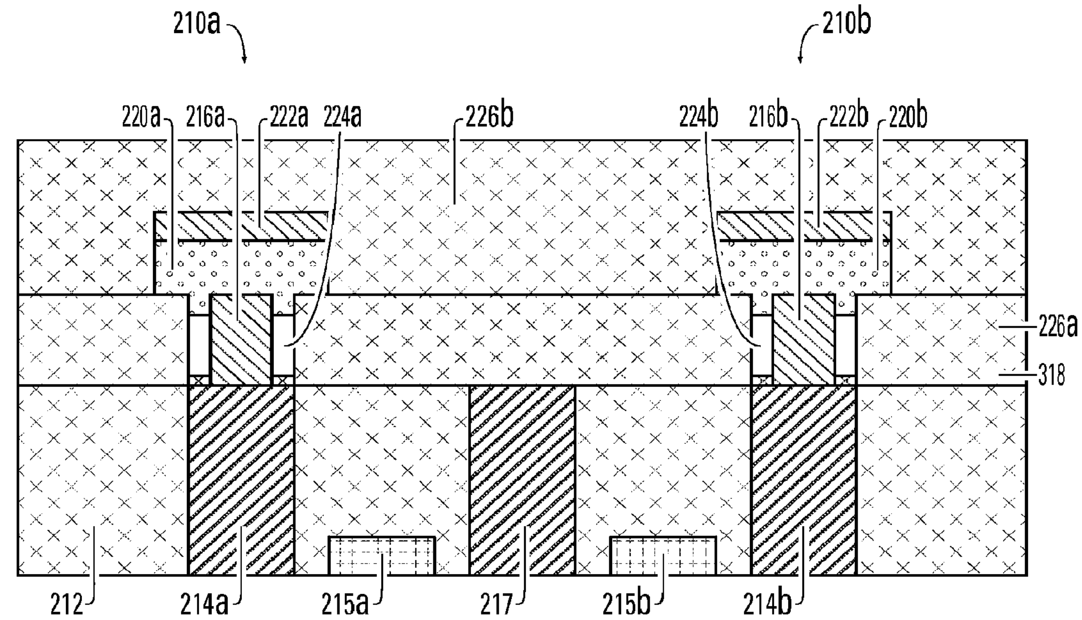

210a
210b
220a
216a
222a
224a
226b
224b
216b
222b
220b
226a
318
212
214a
215a
217
215b
214b

FIG. 3I

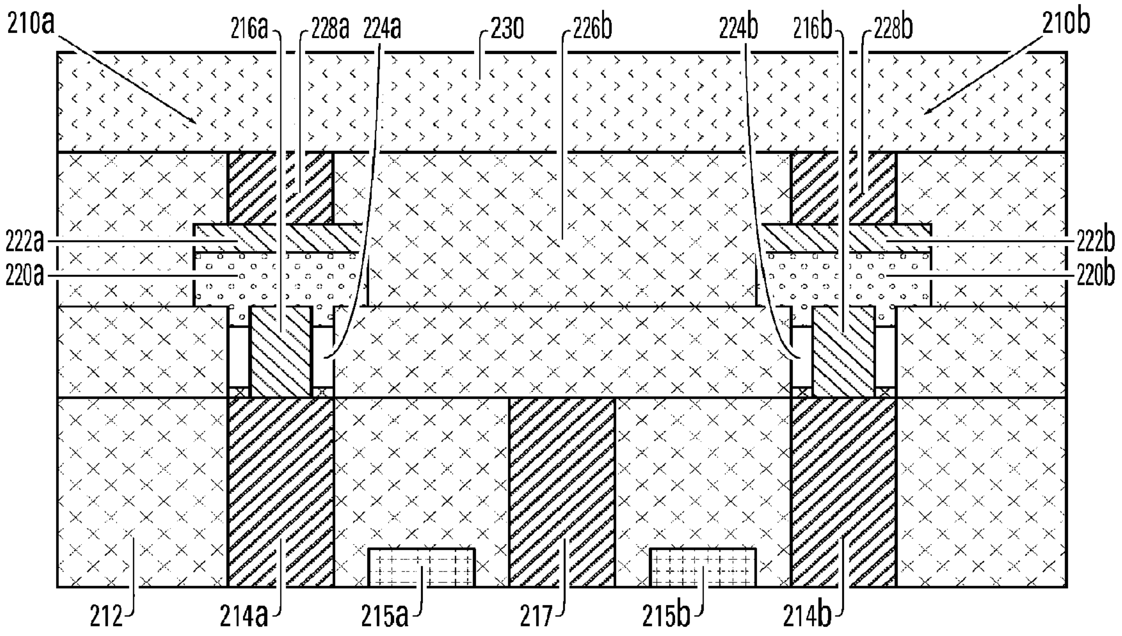

210a
216a
228a
224a
230
226b
224b
216b
228b
210b
222a
220a
222b
220b
212
214a
215a
217
215b
214b

FIG. 3J

VACUUM JACKETED ELECTRODE FOR PHASE CHANGE MEMORY ELEMENT

REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional of U.S. patent application Ser. No. 11/408,596, filed on Apr. 21, 2006, which application claims the benefit of U.S. Provisional Patent Application No. 60/738,883 entitled "Vacuum Jacketed Electrode for Phase Change Memory Element" filed on Nov. 21, 2005.

PARTIES TO A JOINT RESEARCH AGREEMENT

[0002] International Business Machines Corporation, a New York corporation; Macronix International Corporation, Ltd., a Taiwan corporation; and Infineon Technologies AG, a German corporation, are parties to a Joint Research Agreement.

BACKGROUND OF THE INVENTION

[0003] 1. Field of the Invention

[0004] The present invention is generally related to the field of non-volatile memory devices, and more particularly to the field of memory devices that employ phase change materials.

[0005] 2. Description of Related Art

[0006] Phase change based memory materials are widely used in read-write optical disks, and such materials are seeing increasing use in computer memory devices. These materials have at least two solid phases, including for example, a generally amorphous solid phase and a generally crystalline solid phase. Laser pulses are used in read-write optical disks to switch between phases and to read the optical properties of the material after the phase change, and electrical pulses are employed in the same manner in computer memory devices.

[0007] Phase change based memory materials, like chalcogenide based materials and similar materials, also can be caused to change phase by application of electrical current at levels suitable for implementation in integrated circuits. The generally amorphous state is characterized by higher resistivity than the generally crystalline state, which can be readily sensed to indicate data. These properties have generated interest in using programmable resistive material to form nonvolatile memory circuits, which can be read and written with random access.

[0008] The change from the amorphous to the crystalline state is generally a lower current operation. The change from crystalline to amorphous, referred to as reset herein, is generally a higher current operation, which includes a short high current density pulse to melt or break down the crystalline structure, after which the phase change material cools quickly, quenching the phase change process, allowing at least a portion of the phase change structure to stabilize in the amorphous state. It is desirable to minimize the magnitude of the reset current used to cause transition of phase change material from crystalline state to amorphous state. The magnitude of the reset current needed for reset can be reduced by reducing the size of the phase change material element in the cell and of the contact area between electrodes and the phase change material, so that higher current densities are achieved with small absolute current values through the phase change material element.

[0009] One direction of development has been toward forming small pores in an integrated circuit structure and using small quantities of programmable resistive material to fill the small pores. Patents illustrating development toward small pores include: Ovshinsky, "Multibit Single Cell Memory Element Having Tapered Contact," U.S. Pat. No. 5,687,112, issued Nov. 11, 1997; Zahorik et al., "Method of Making Chalogenide [sic] Memory Device," U.S. Pat. No. 5,789,277, issued Aug. 4, 1998; Doan et al., "Controllable Ovonic Phase-Change Semiconductor Memory Device and Methods of Fabricating the Same," U.S. Pat. No. 6,150,253, issued Nov. 21, 2000, and Reinberg, "Chalcogenide Memory Cell with a Plurality of Chalcogenide Electrodes," U.S. Pat. No. 5,920,788, issued Jul. 6, 1999.

[0010] A specific issue arising from conventional phase change memory structures is the heat sink effect of conventional designs. Generally, the prior art teaches the use of metallic electrodes on both sides of the phase change memory element, with electrodes of approximately the same size as the phase change member. Such electrodes act as heat sinks, the high heat conductivity of the metal rapidly drawing heat away from the phase change material. Because the phase change occurs as a result of heating, the heat sink effect results in a requirement for higher current, in order to effect the desired phase change.

[0011] One approach to the heat flow problem is seen in U.S. Pat. No. 6,815,704, entitled "Self Aligned Air-Gap Thermal Insulation for Nano-scale Insulated Chalcogenide Electronics (NICE) RAM", in which an attempt is made to isolate the memory cell. That structure, and the attendant fabrication process, is overly complex, yet it does not promote minimal current flow in the memory device.

[0012] It is desirable therefore to provide a memory cell structure having small dimensions and low reset currents, as well as a structure that addresses the heat conductivity problem, and a method for manufacturing such structure that meets tight process variation specifications needed for large-scale memory devices. It is further desirable to provide a manufacturing process and a structure, which are compatible with manufacturing of peripheral circuits on the same integrated circuit.

SUMMARY OF THE INVENTION

[0013] One aspect of the invention is a memory device having a vacuum jacket around the first electrode element for improved thermal isolation. The memory unit includes a first electrode element; a phase change memory element in contact with the first electrode element; a dielectric fill layer surrounding the phase change memory element and the first electrode element, wherein the dielectric layer is spaced from the first electrode element to define a chamber between the first electrode element and the dielectric fill layer; and wherein the phase change memory layer is sealed to the dielectric fill layer to define a thermal isolation jacket around the first electrode element.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. **1** is a cross-sectional view that illustrates an embodiment of a phase change memory element employing an air cell thermal isolation element.

[0015] FIGS. **2***a*-**2***m* illustrate an embodiment of a process for fabricating a phase change memory element as shown in FIG. **1**.

[0016] FIGS. **3***a*-**3***j* illustrate an alternative embodiment of a process for fabricating a phase change memory element as shown in FIG. **1**.

DETAILED DESCRIPTION

[0017] The following discussion describes embodiments of the invention with particular reference to FIGS. **1**-**3**. It will be understood that the examples and features shown are exemplary and illustrative in nature and not intended to limit the scope of the invention. That scope is defined solely by the claims appended hereto.

[0018] The present invention concerns memory elements and memory cells. As used herein, and as is well known in the art, a memory cell is a circuit device designed to hold a charge or state to indicate the logic level of a single data bit. Memory cells are arrayed to provide, for example, the random access memory for a computer. Within certain memory cells, a memory element performs the function of actually holding the charge or state. In a conventional dynamic random access memory cell, for example, a capacitor indicates the logic level of the cell, with a fully charged state indicating a logic 1, or high, state, and fully discharged indicating a logic 0, or low, state.

[0019] A memory element **10**, an embodiment of the present invention, is illustrated generally in FIG. **1**. As seen there, the memory element **10** is shown as a single unit, for purposes of clarity. In practice, each element is a part of a memory cell, which in turn is part of a larger memory array, as discussed more fully below. The structure of a memory element will be discussed first, followed by a description of the process for fabricating the same.

[0020] The memory element is formed on a substrate **12**, which is preferably a dielectric fill material such as silicon dioxide. Other suitable materials include polyimide, silicon nitride or other dielectric fill materials known in the art. Extending through the substrate to make electrical contact with exterior circuitry (not shown) is a plug element **14**, preferably formed from a refractory metal such as tungsten. Other suitable refractory metals include Ti, Mo, Al, Ta, Cu, Pt, Ir, La, Ni, and Ru.

[0021] Extending upward from the plug element are a lower electrode element **16**, a phase change element **20** and an upper electrode element **22**. The upper electrode element is in electrical contact with outside circuitry (not shown).

[0022] The phase change element **20** can be formed from a class of materials preferably including chalcogenide based materials. Chalcogens include any of the four elements oxygen (O), sulfur (S), selenium (Se), and tellurium (Te), forming part of group VI of the periodic table. Chalcogenides comprise compounds of a chalcogen with a more electropositive element or radical. Chalcogenide combinations denote chalcogenides amalgamated with other materials such as transition metals. A chalcogenide combination usually contains one or more elements from column six of the periodic table of elements, such as germanium (Ge) and tin (Sn). Often, chalcogenide combinations include one or more of antimony (Sb), gallium (Ga), indium (In), and silver (Ag). Many phase change based memory materials have been described in technical literature, including combinations of: Ga/Sb, In/Sb, In/Se, Sb/Te, Ge/Te, Ge/Sb/Te, In/Sb/Te, Ga/Se/Te, Sn/Sb/Te, In/Sb/Ge, Ag/In/Sb/Te, Ge/Sn/Sb/Te, Ge/Sb/Se/Te and Te/Ge/Sb/S. In the family of Ge/Sb/Te materials, a wide range of compositions may be workable. The compositions can be characterized as $Te_aGe_bSb_{100-(a+b)}$.

[0023] One researcher has described the most useful combinations as having an average concentration of Te in the deposited materials well below 70%, typically below about 60% and ranged in general from as low as about 23% up to about 58% Te and most preferably about 48% to 58% Te. Concentrations of Ge were above about 5% and ranged from a low of about 8% to about 30% average in the material, remaining generally below 50%. Most preferably, concentrations of Ge ranged from about 8% to about 40%. The remainder of the principal constituent elements in this composition was Sb. These percentages are atomic percentages that total 100% of the atoms of the constituent elements. (Ovshinsky '112 patent, cols. 10-11.) Particular combinations evaluated by another researcher include Ge2Sb2Te5, GeSb2Te4 and GeSb4Te7. (Noboru Yamada, "Potential of Ge-Sb-Te Phase-Change Optical Disks for High-Data-Rate Recording", SPIE v. 3109, pp. 28-37 (1997).) More generally, a transition metal such as chromium (Cr), iron (Fe), nickel (Ni), niobium (Nb), palladium (Pd), platinum (Pt) and mixtures or combinations thereof, may be combined with Ge/Sb/Te to form a phase change material that has programmable resistive properties. Specific examples of memory materials that may be useful are given in Ovshinsky '112 at columns 11-13, which examples are hereby incorporated by reference.

[0024] Phase change materials are capable of being switched between a first structural state in which the material is in a generally amorphous solid phase, and a second structural state in which the material is in a generally crystalline solid phase in its local order in the active channel region of the cell. These materials are at least bistable. The term amorphous is used to refer to a relatively less ordered structure, more disordered than a single crystal, which has detectable characteristics, such as higher electrical resistivity than the crystalline phase. The term crystalline is used to refer to a structure relatively more ordered than in an amorphous state, which has detectable characteristics such as lower electrical resistivity than the amorphous phase. Typically, phase change materials may be electrically switched between different detectable states of local order across the spectrum between completely amorphous and completely crystalline states. Other material characteristics affected by the change between amorphous and crystalline phases include atomic order, free electron density and activation energy. The material may be switched either into different solid phases or into mixtures of two or more solid phases, providing a gray scale between completely amorphous and completely crystalline states. The electrical properties in the material may vary accordingly.

[0025] Phase change materials can be changed from one phase state to another by application of electrical pulses. It has been observed that a shorter, higher amplitude pulse tends to change the phase change material to a generally amorphous state. A longer, lower amplitude pulse tends to change the phase change material to a generally crystalline state. The energy in a shorter, higher amplitude pulse is high enough to allow for bonds of the crystalline structure to be broken and short enough to prevent the atoms from realigning into a crystalline state. Appropriate profiles for pulses can be determined, without undue experimentation, specifically adapted to a particular phase change combination. In the following sections of the disclosure, the phase change material is referred to as GST, and it will be understood that other types of phase change materials can be used. A material useful for implementation of a phase change element described herein is Ge2Sb2Te5.

[0026] The upper and lower electrode elements are preferably formed of titanium nitride (TiN) or similar material, such as one or more elements selected from the group consisting of Si, Ti, Al, Ta, N, O, and C. It should be noted that, for purposes of reference only, the direction from the bottom toward the top of the drawings herein is designated “vertical”, and the side-to-side direction is “lateral” or “horizontal.” Such designations have no effect on the actual physical orientation of a device, either during fabrication or during use.

[0027] It is preferred that the thickness (that is, the dimension parallel to the long axis of the printed page herein) of the phase change element **20** be from about 20 nm to about 150 nm, and most preferably about 70 nm. The thickness of the lower electrode **16** should be from about 20 nm to about 150 nm, and most preferably about 100 nm. The width (that is, the dimension parallel to the short axis of the printed page herein) of the lower electrode **16** should be from about 10 nm to about 70 nm, and most preferably about 50 nm. The width of the thermal isolation cell should be from about 2 nm to about 20 nm, and most preferably about 10 nm. Thus, the total width of the phase change element should be from about 50 nm to about 120 nm, and most preferably about 70 nm.

[0028] The electrode elements and phase change element are surrounded by an upper insulation layer **26***a*, preferably formed of the same or similar material as the substrate **12**. Between the two insulation layers is a barrier layer **18**, formed of SiN or similar material.

[0029] The upper insulation layer makes contact with the sides of both the phase change element and the upper electrode, but not with the lower electrode element. The phase change element extends laterally beyond the edges of the lower electrode, so that the ends of the phase change element, the sides of the lower electrode and upper insulation layer and a portion of the barrier layer define a thermal isolation cell **24** surrounding the lower electrode element **16**.

[0030] In operation, current flows through the memory element from plug assembly **14**, to the lower electrode element **16**, into the phase change element **20**, and out through the upper electrode **22**. Of course, the current direction could be altered by changes in element geometry, as will be understood by those in the art. In either event, the phase change material is subject to joule heating as current flows, as discussed above, resulting in a temperature rise in the center of the GST material. When the temperature exceeds the level required for phase change, a portion of the phase change material changes state. Temperature is not uniform throughout the phase change element, with changing values of current density producing significant variations. The temperature of the phase change material determines the effect produced, so the current is chosen to produce a temperature sufficient to create the desired result—either an amorphous state or a crystalline state—in the GST material. If it is desired to read the element status, a low current is employed for sensing purposes. The read operation is non-destructive, as the element temperature is kept below the threshold for a phase change.

[0031] The thermal isolation cell **24** functions to contain heat within the phase change element, which has several positive effects. First, by preventing the migration of heat away from the lower electrode element, this design reduces the total heat required to effect phase changes, which in turn reduces the current required for each SET or RESET operation. At the same time, retaining heat within the lower electrode element reduces the heat transferred to the remainder of the memory array, which translates directly into increased lifespan for the device. Given the vast numbers of memory elements within a complete integrated circuit—at least eight billion elements for a 1 GB memory device, for example—it can be appreciated that the effects of such a heat reduction will be significant. Thus, the illustrated design leads to reduced current consumption by the memory element.

[0032] An embodiment of a process for fabricating the memory device of the present invention is shown in FIGS. **2***a*-**2***m*. As known in the art, a memory array is preferably formed employing pairs of memory cells, which structure is shown here. The process begins with a base structure as seen in FIG. **2***a*, which is suitable for the formation of multiple memory cells, as will be shown below. Plug elements **14***a* and **14***b* extend through the substrate material **12**, serving separate memory elements. Materials for these two elements are described above. Word lines **15***a* and **15***b* extend in a direction perpendicular to the drawing, connecting a number of memory elements in a manner known in the art. It is preferred to form the word lines from polysilicon. Common source line **17** extends through the middle of the pair of memory elements, parallel to the word lines.

[0033] FIG. **2***b* depicts the addition of electrode material layer **116**, whose composition is set out above. In the succeeding two drawings, FIGS. **2***c* and **2***d*, the structure is prepared for an etching operation by first depositing and patterning photoresist material **50** in a desired position. Here, however, the conventional lithographic process is not sufficient to achieve the degree of resolution required, in that the width of the lower electrode element (to be formed from the TiN layer **116**) is less than the minimum feature size achievable by conventional lithography. Thus, the photoresist is patterned to the smallest possible size in the step shown in FIG. **2***c*, followed by a trimming step in FIG. **2***d* to produce the etch masks **52** at the required size. The process for achieving this result is disclosed in pending patent applications owned by the assignee hereof, the details of which are not material to the invention herein.

[0034] The etching step follows, with results shown in FIG. **2***e*, in which lower electrode elements **16***a* and **16***b* are formed, preferably employing s a dry anisotropic etch using a reactive ion etching (RIE), utilizing a chlorine-based plasma chemistry. An optical emission tool may be used to identify and control the end point of the etch, when the substrate layer is encountered.

[0035] Following the etching, a barrier layer **118** is deposited, composed of SiN, as discussed above, as seen in FIG. **2***f*. That layer is followed by the deposition of an upper insulation layer **26***a*, composed of material the same or similar to that of the substrate **12**, such as SiO_2, as seen in FIG. **2***g*. That layer is deposited such that it completely covers the lower electrode element and barrier layer. Then, the upper insulation layer is subjected to planarization to expose the upper level of the lower electrode members **16***a* and **16***b*, as seen in FIG. **2***h*.

[0036] The thermal isolation cells are formed in the next two steps. First, the portions of the barrier layer **118** lying next to the lower electrode elements are etched away, as shown in FIG. **2***i*. A wet etch, chosen to selectively etch the barrier layer material, is employed for this step. For the preferable material, SiN, a phosphoric acid etch is used. Control is exercised to stop the etching step before an appreciable etching of either the lower electrode or the dielectric material occurs.

[0037] Following the etching step, a two-stage deposition is undertaken to deposit a layer of GST material **120** atop the dielectric material, followed by a layer of electrode material (preferably TiN) **122**, as shown in FIG. **2***j*. This deposition must suffice to form the thermal isolation cells **24***a* and **24***b*, by sealing the voids remaining after the previous etching step. The preferred process for this step is sputtering, so that GST material extends into and seals the cell. Process parameters must be chosen such that the sputtering does not altogether fill the cells, as will be understood in the art.

[0038] The next step defines the pair of memory elements **10***a* and **10***b*. FIG. **2***k* depicts the results of a patterning and etching step by which the GST and electrode material layers deposited in the previous step are etched to leave phase change elements **20***a* and **20***b* as well as upper electrode elements, generally centered on the lower electrodes **16***a* and **16***b*. This pattern and etch operation is entirely conventional.

[0039] The final two steps complete the fabrication of the memory element. In FIG. **21**, a cap oxide layer **26***b* is applied to the structure shown in FIG. **2***k*. The material should be the same as that employed for the insulation layer **26***a*, and it should be deposited to a depth sufficient to cover the memory elements **10***a* and **10***b* completely. In FIG. **2***m*, the final step, metallization, is illustrated, showing the formation of contact elements **28***a* and **28***b*, extending from the upper electrode elements **22***a* and **22***b*, and bit line **30** spanning memory elements **10***a* and **10***b* and extending in both directions to other memory elements, as is known in the art.

[0040] An alternative process is illustrated in FIGS. **3***a*-**3***j*. Generally, this method follows the "damascene" approach, which generally avoids the conventional method of depositing metals and active materials over wide areas, followed by lithographic patterning and dielectric filling, by first depositing the dielectric fill and then forming and filling the (relatively small) metal and active material areas.

[0041] The process begins with a base structure as seen in FIG. **3***a*, which is suitable for the formation of multiple memory cells, as will be shown below. Plug elements **214***a* and **214***b* extend through the substrate material **212**, serving separate memory elements. Materials for these two elements are described above. Word lines **215***a* and **215***b* extend in a direction perpendicular to the drawing, connecting a number of memory elements in a manner known in the art. It is preferred to form the word lines from polysilicon. Common source line **217** extends through the middle of the pair of memory elements, parallel to the word lines.

[0042] FIG. **3***b* depicts the addition of upper dielectric layer **226**, preferably of the same material employed for the substrate. In the succeeding four drawings, FIGS. **3***c*-**3***f*, the lower portions of each memory element are formed. First, the upper dielectric layer is patterned and etched to open two cavities **211***a* and **211***b*, positioned atop the plugs **214***a* and **214***b*. The etching step, which could be performed by RIE, should be controlled so that the upper surfaces of the plug elements are exposed. The lithographic operation that produces these cavities is known in the art. Next, as shown in FIG. **3***d*, side walls **218***a* and **218***b* are formed in each cavity. The side walls are preferably composed of SiN or similar material. Preferably, the material is deposited employing chemical vapor deposition (CVD) or a similar process, followed by RIE to form the sidewalls. A deposition step follows, shown by FIG. **3***e*, in which lower electrode elements **216***a* and **216***b* are formed, preferably employing CVD or other known deposition technique. These elements are preferably composed of TiN or similar material, as discussed above. Finally, side walls **218***a* and **218***b* are etched away, as shown in FIG. **3***f*. A wet etch, chosen to selectively etch the side wall layer material, is employed for this step. For the preferable material, SiN, a phosphoric acid etch is used. Control is exercised to stop the etching step before an appreciable etching of either the lower electrode or the dielectric material occurs.

[0043] The thermal isolation cells and the upper portions of the memory elements are formed in the next two steps. A two-stage deposition, illustrated in FIG. **3***g*, is undertaken to deposit a layer of GST material **320** atop the dielectric material **226***a*, followed by a layer of electrode material (preferably TiN) **322**. This deposition must suffice to form the thermal isolation cells **224***a* and **224***b*, by sealing the voids remaining after the previous etching step. The preferred process for this step is sputtering, so that GST material extends into and seals the cell, as shown. Process parameters must be chosen such that the sputtering does not altogether fill the cells, as will be understood in the art.

[0044] The next step defines the pair of memory elements **210***a* and **210***b*. FIG. **3***h* depicts the results of a patterning and etching step by which the GST and electrode material layers deposited in the previous step are etched to leave phase change elements **220***a* and **220***b* as well as upper electrode elements **222***a* and **222***b*, generally centered on the lower electrodes **216***a* and **216***b*. This pattern and etch operation is entirely conventional.

[0045] The final two steps complete the fabrication of the memory elements. In FIG. **3***i*, a cap oxide layer **226***b* is applied to the structure shown in FIG. **3***h*. The material should be the same as that employed for the insulation layer **226***a*, and it should be deposited to a depth sufficient to cover the memory elements **210***a* and **210***b* completely. In FIG. **3***j*, the final step, metallization, is illustrated, showing the formation of contact elements **228***a* and **228***b*, extending from the upper electrode elements **222***a* and **222***b*, and bit line **230** spanning memory elements **210***a* and **210***b* and extending in both directions to other memory elements, as is known in the art.

[0046] While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will readily occur to those skilled in the art, which modifications and combinations will be within the spirit of the invention and the scope of the following claims. What is claimed is:

I claim:

1. A method of fabricating a memory device, comprising:
forming a first electrode;
forming a dielectric element around the first electrode, wherein the dielectric element and the first electrode are separated by a gap; and
forming a memory element over the first electrode, the dielectric element and the gap.

2. The method of claim **1**, wherein the memory element includes memory material that comprises a combination of Ge, Sb, and Te.

3. The method of claim **1**, wherein the memory element includes memory material that comprises a combination of two or more materials from the group of Ge, Sb, Te, Se, In, Ti, Ga, Bi, Sn, Cu, Pd, Pb, Ag, S, and Au.

4. The method of claim **1**, wherein the first electrode has a top surface electrically coupled with the memory element, the dielectric element has a top surface and the phase change memory element lies on the top surface of the first electrode and the top surface of the dielectric element across the gap.

5. The method of claim **4**, wherein the dielectric element has a top surface that is co-planar with the top surface of the first electrode.

6. A method of fabricating a memory device, comprising the steps of:
forming a first electrode element;
depositing a liner layer on the first electrode element;
forming a dielectric layer surrounding the first electrode element, the upper surface of the dielectric layer being adjusted such that the liner layer surrounding the first electrode element is exposed;
selectively etching the liner layer to open a void between the first electrode element and the dielectric layer; and
depositing a phase change element to seal the void and make electrical contact with the first electrode element, thereby defining a thermal isolation jacket around the first electrode element.

7. The method of claim **6**, wherein the phase change element comprises a combination of Ge, Sb, and Te.

8. The method of claim **6**, wherein the phase-change element comprises a combination of two or more materials from the group of Ge, Sb, Te, Se, In, Ti, Ga, Bi, Sn, Cu, Pd, Pb, Ag, S, and Au.

9. The method of claim **6**, wherein the phase change element is about 70 nm wide and about 70 nm thick, and the diameter of bottom electrode is about 50 nm.

10. The method of claim **6**, wherein the thermal isolation jacket is about 10 nm thick.

11. A method of fabricating a memory device, comprising the steps of:
forming a substrate, the uppermost layer of which is composed of a dielectric fill material;
removing selected portions of the dielectric fill material to form cavities therein;
forming a first electrode element having sidewalls formed from liner material within the cavities;
selectively etching the liner material to open a void between the first electrode element and the dielectric layer; and
depositing a phase change element to seal the void and make electrical contact with the first electrode element, thereby defining a thermal isolation jacket around the first electrode element.

12. The method of claim **11**, wherein the phase change element comprises a combination of Ge, Sb, and Te.

13. The method of claim **11**, wherein the phase change element comprises a combination of two or more materials from the group of Ge, Sb, Te, Se, In, Ti, Ga, Bi, Sn, Cu, Pd, Pb, Ag, S, and Au.

14. The method of claim **11**, wherein the phase change element is about 70 nm wide and about 70 nm thick, and the diameter of bottom electrode is about 50 nm.

15. The method of claim **11**, wherein the thermal isolation jacket is about 10 nm thick.

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