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Song et al.

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(54) **NON-LINEAR TRANSITION SHIFT IDENTIFICATION AND COMPENSATION**

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(73) Assignee: **Marvell International Ltd.** (BM)

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(51) **Int. Cl.**
G11B 5/09 (2006.01)

(52) **U.S. Cl.** **360/45**

(58) **Field of Classification Search** ..... None
See application file for complete search history.

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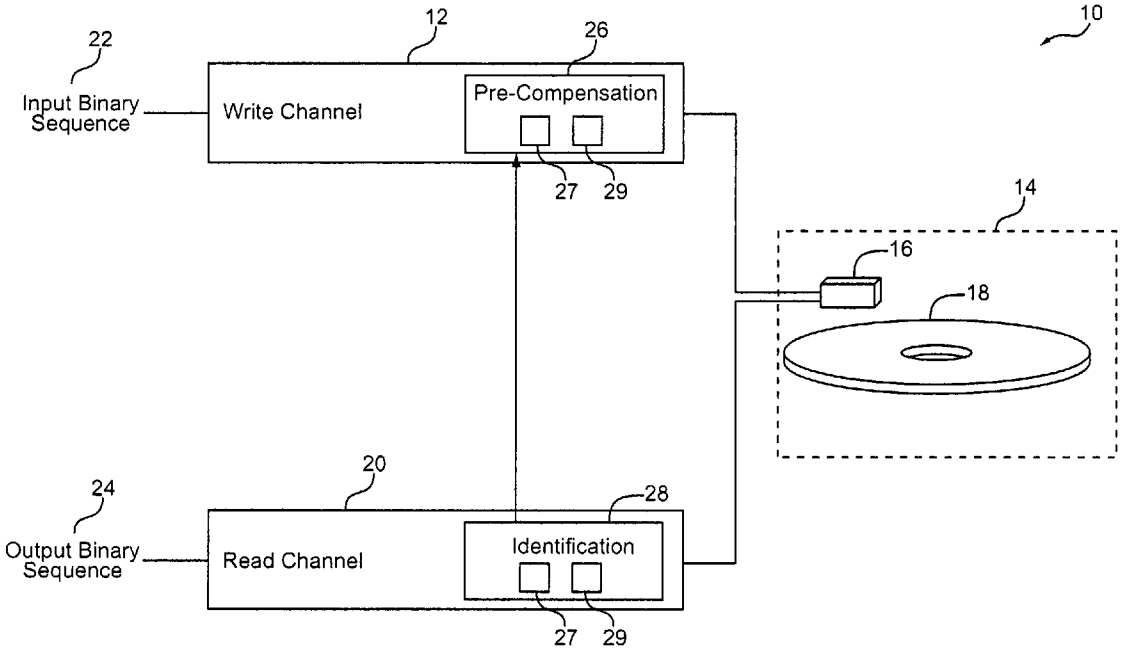
Primary Examiner — Daniell L Negrón

(57) **ABSTRACT**

A system for identifying and compensating for non-linear transition shift in a magnetic medium data storage device is disclosed. The non-linear transition shift compensation system includes a non-linear transition shift estimation module adapted to generate non-linear transition shift estimates for specific bit patterns. The system further includes a pre-compensation module adapted to adjust the temporal spacing of binary transitions written to the magnetic medium based on the non-linear transition shift estimates generated by the non-linear transition shift estimation module for specific bit patterns corresponding to bit patterns appearing in the data being written to the magnetic medium.

43 Claims, 11 Drawing Sheets



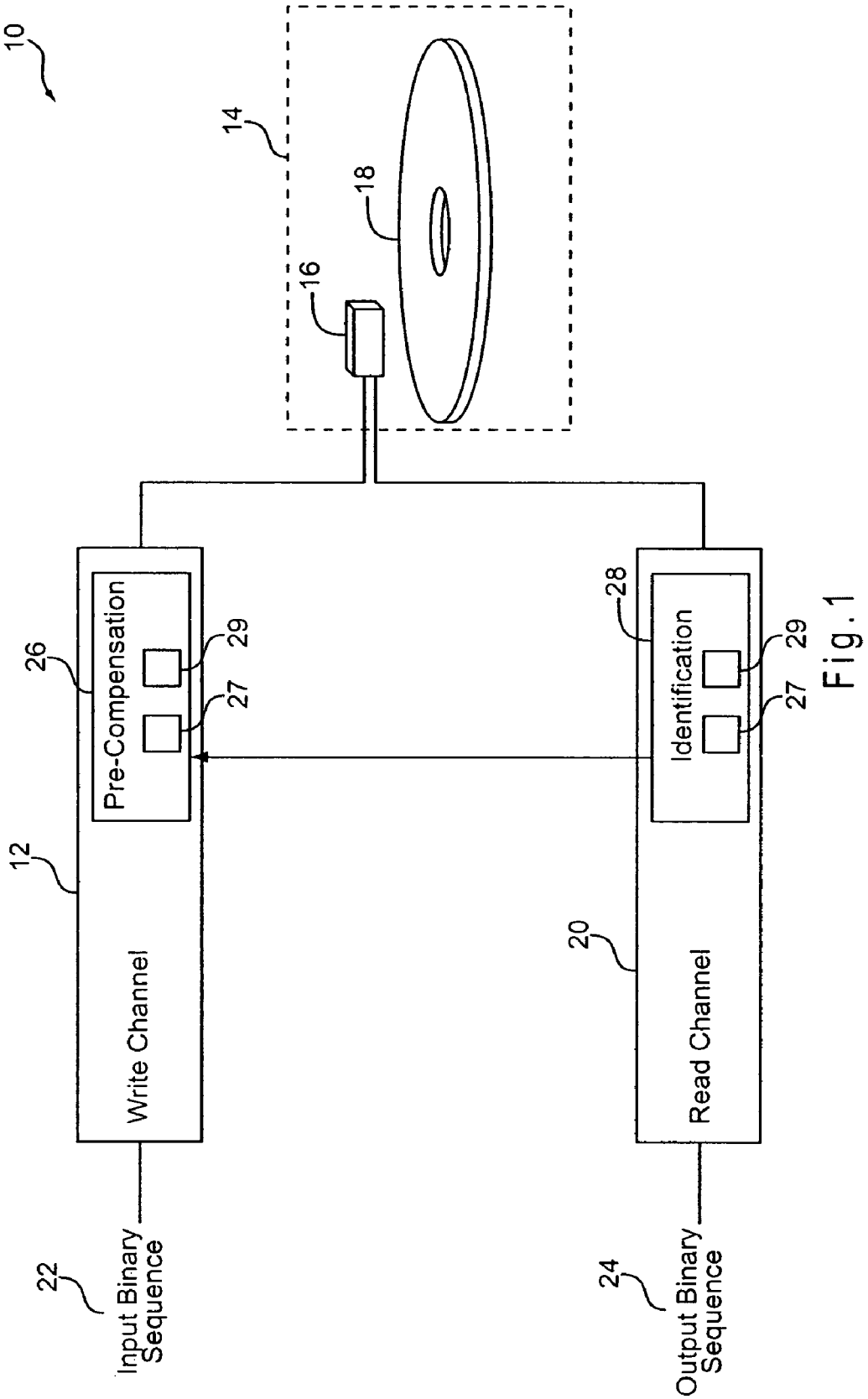

10
14
18
16
Pre-Compensation
26
29
27
Identification
28
29
27
12
Write Channel
20
Read Channel
22
Input Binary Sequence
24
Output Binary Sequence

Fig. 1

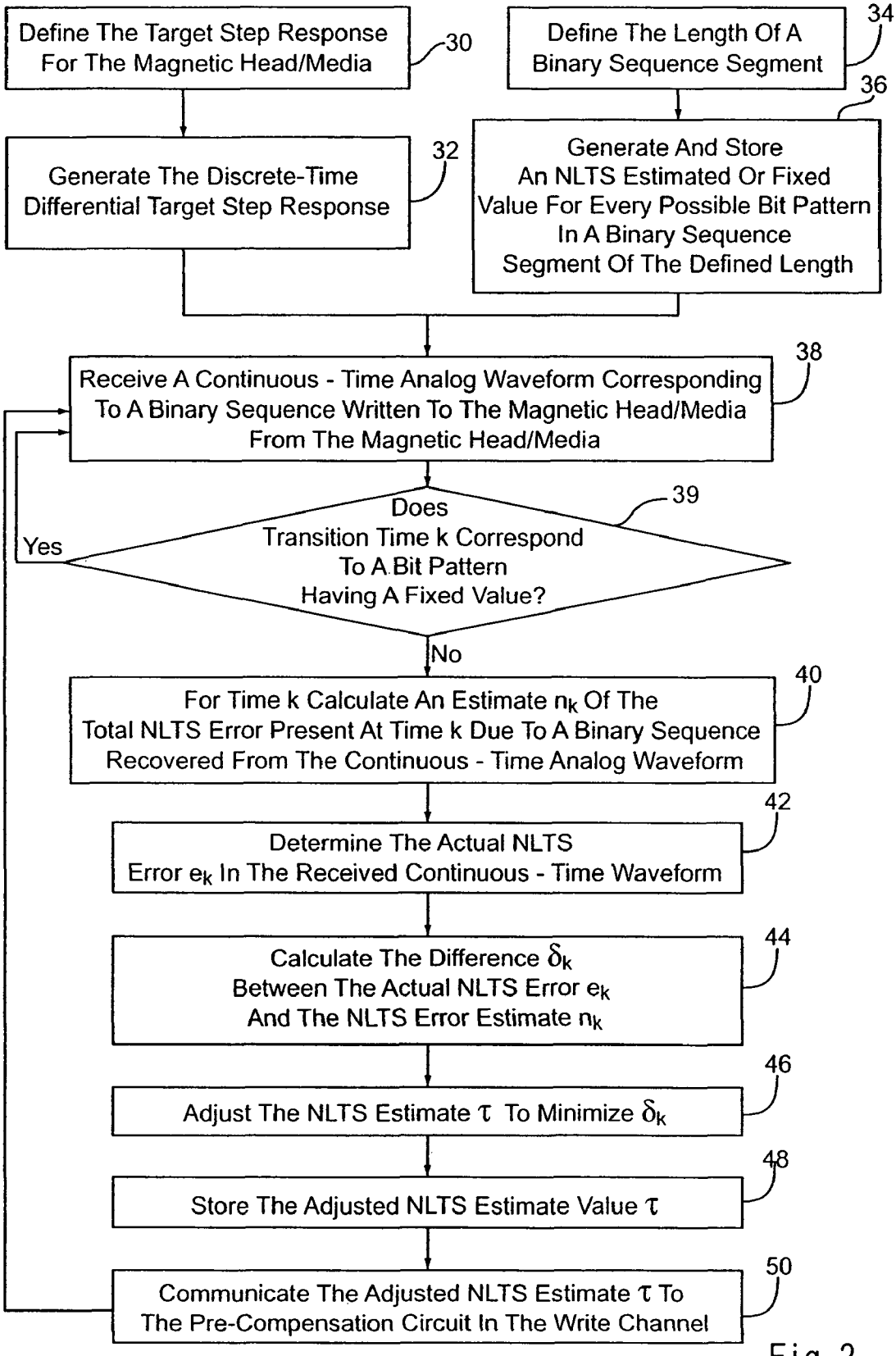

Define The Target Step Response For The Magnetic Head/Media
30
Define The Length Of A Binary Sequence Segment
34
36
Generate The Discrete-Time Differential Target Step Response
32
Generate And Store An NLTS Estimated Or Fixed Value For Every Possible Bit Pattern In A Binary Sequence Segment Of The Defined Length
Receive A Continuous - Time Analog Waveform Corresponding To A Binary Sequence Written To The Magnetic Head/Media From The Magnetic Head/Media
38
Does Transition Time k Correspond To A Bit Pattern Having A Fixed Value?
39
Yes
No
For Time k Calculate An Estimate n_k Of The Total NLTS Error Present At Time k Due To A Binary Sequence Recovered From The Continuous - Time Analog Waveform
40
Determine The Actual NLTS Error e_k In The Received Continuous - Time Waveform
42
Calculate The Difference δ_k Between The Actual NLTS Error e_k And The NLTS Error Estimate n_k
44
Adjust The NLTS Estimate τ To Minimize δ_k
46
Store The Adjusted NLTS Estimate Value τ
48
Communicate The Adjusted NLTS Estimate τ To The Pre-Compensation Circuit In The Write Channel
50

Fig. 2

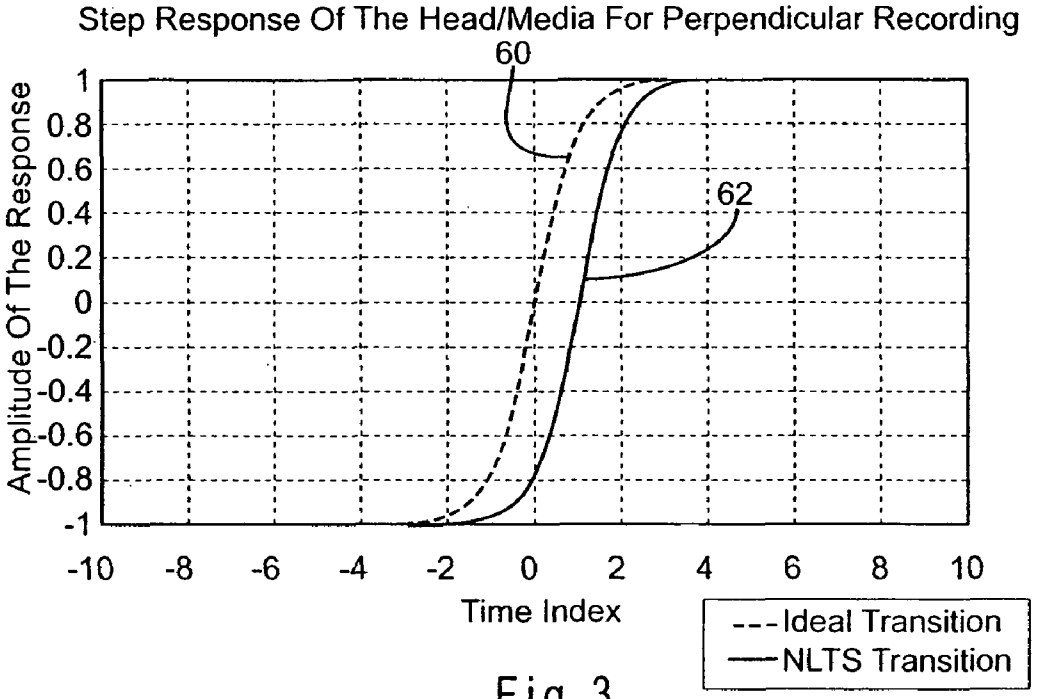

Step Response Of The Head/Media For Perpendicular Recording
60
62
Amplitude Of The Response
1
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
-10 -8 -6 -4 -2 0 2 4 6 8 10
Time Index
---Ideal Transition
—NLTS Transition

Fig.3

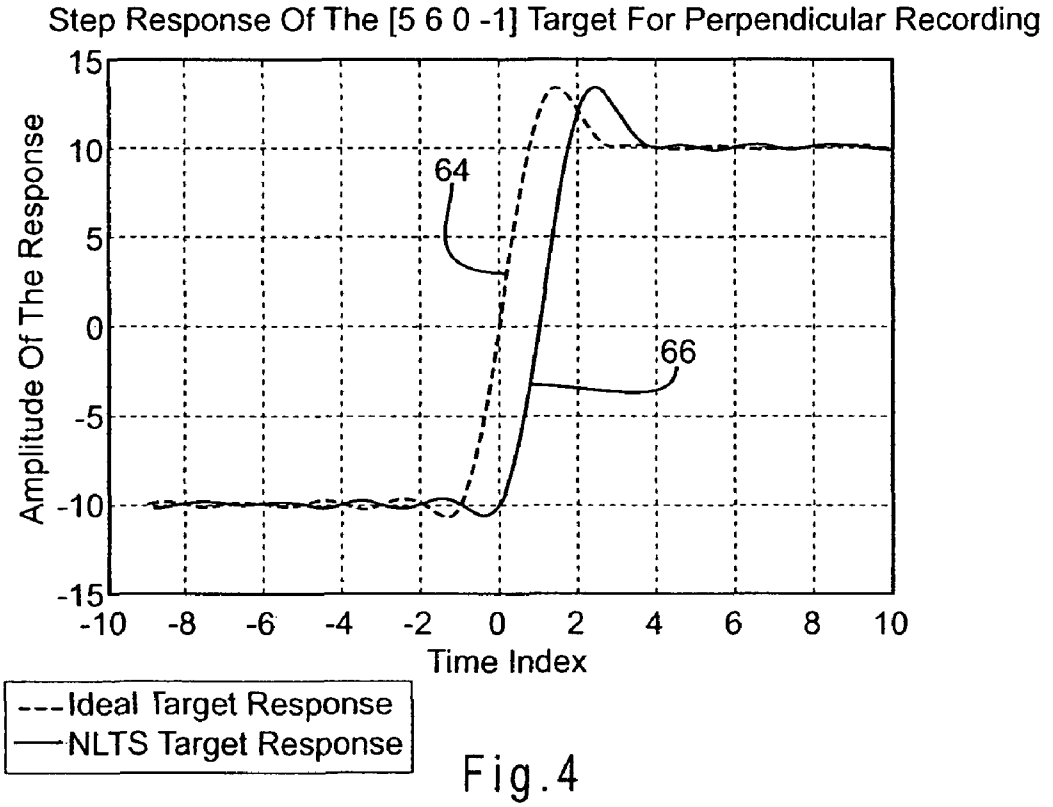

Step Response Of The [5 6 0 -1] Target For Perpendicular Recording
64
66
Amplitude Of The Response
15
10
5
0
-5
-10
-15
-10 -8 -6 -4 -2 0 2 4 6 8 10
Time Index
---Ideal Target Response
—NLTS Target Response

Fig.4

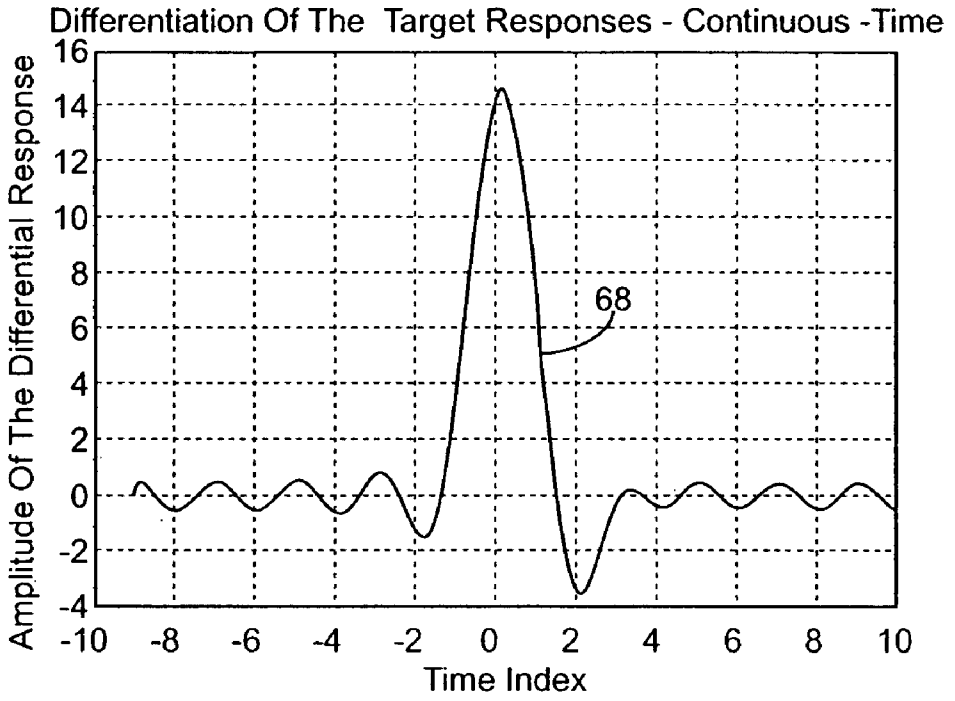

Differentiation Of The Target Responses - Continuous -Time
Amplitude Of The Differential Response
Time Index
68
16
14
12
10
8
6
4
2
0
-2
-4
-10
-8
-6
-4
-2
0
2
4
6
8
10

Fig.5

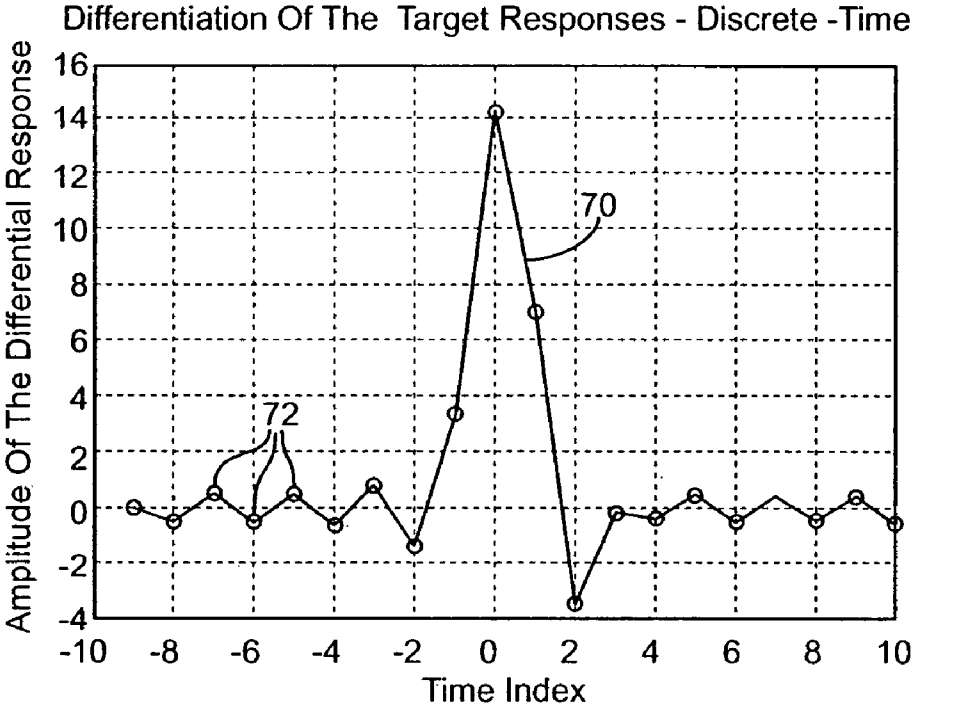

Differentiation Of The Target Responses - Discrete -Time
Amplitude Of The Differential Response
Time Index
70
72
16
14
12
10
8
6
4
2
0
-2
-4
-10
-8
-6
-4
-2
0
2
4
6
8
10

Fig.6

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τ	b_1	b_1	b_1	b_1
A	0	0	0	0
B	0	0	0	1
C	0	0	1	0
D	0	0	1	1
E	0	1	0	0
F	0	1	0	1
G	0	1	1	0
H	0	1	1	1
I	1	0	0	0
J	1	0	0	1
K	1	0	1	0
L	1	0	1	1
M	1	1	0	0
N	1	1	0	1
O	1	1	1	0
P	1	1	1	1

Fig.7

76

b_{k-4}	b_{k-3}	b_{k-2}	b_{k-1}	b_k	b_{k+1}	b_{k+2}	b_{k+3}	b_{k+4}
1	0	1	1	0	0	0	0	1

Fig.8

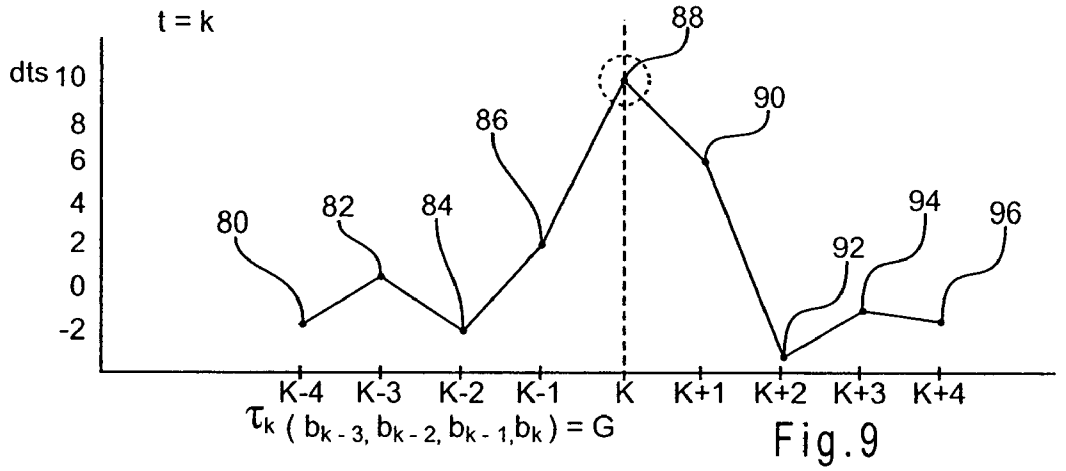

Fig.9

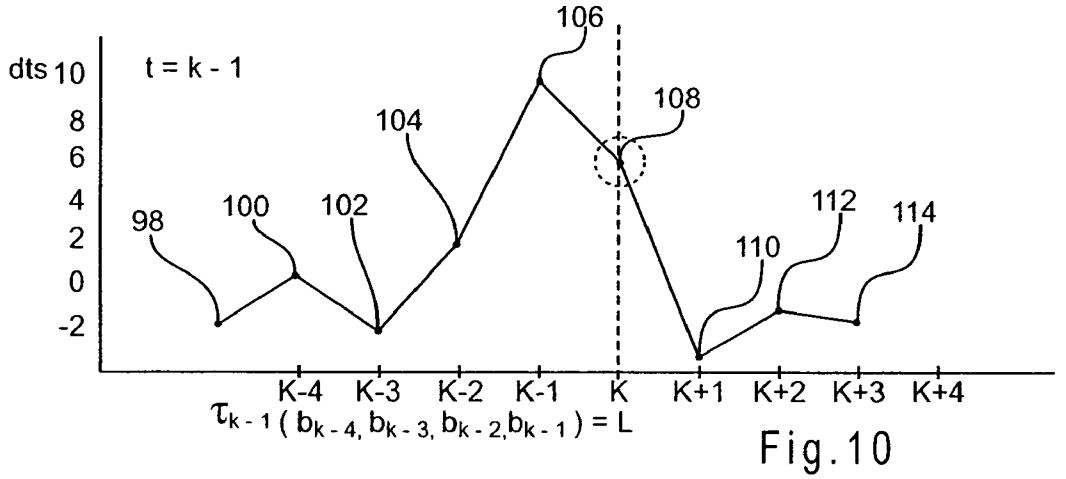

Fig.10

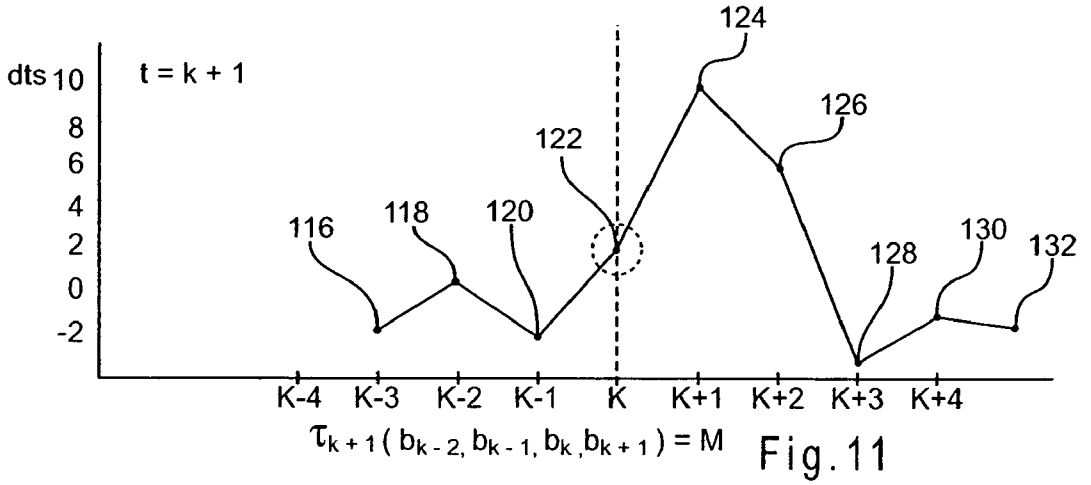

Fig.11

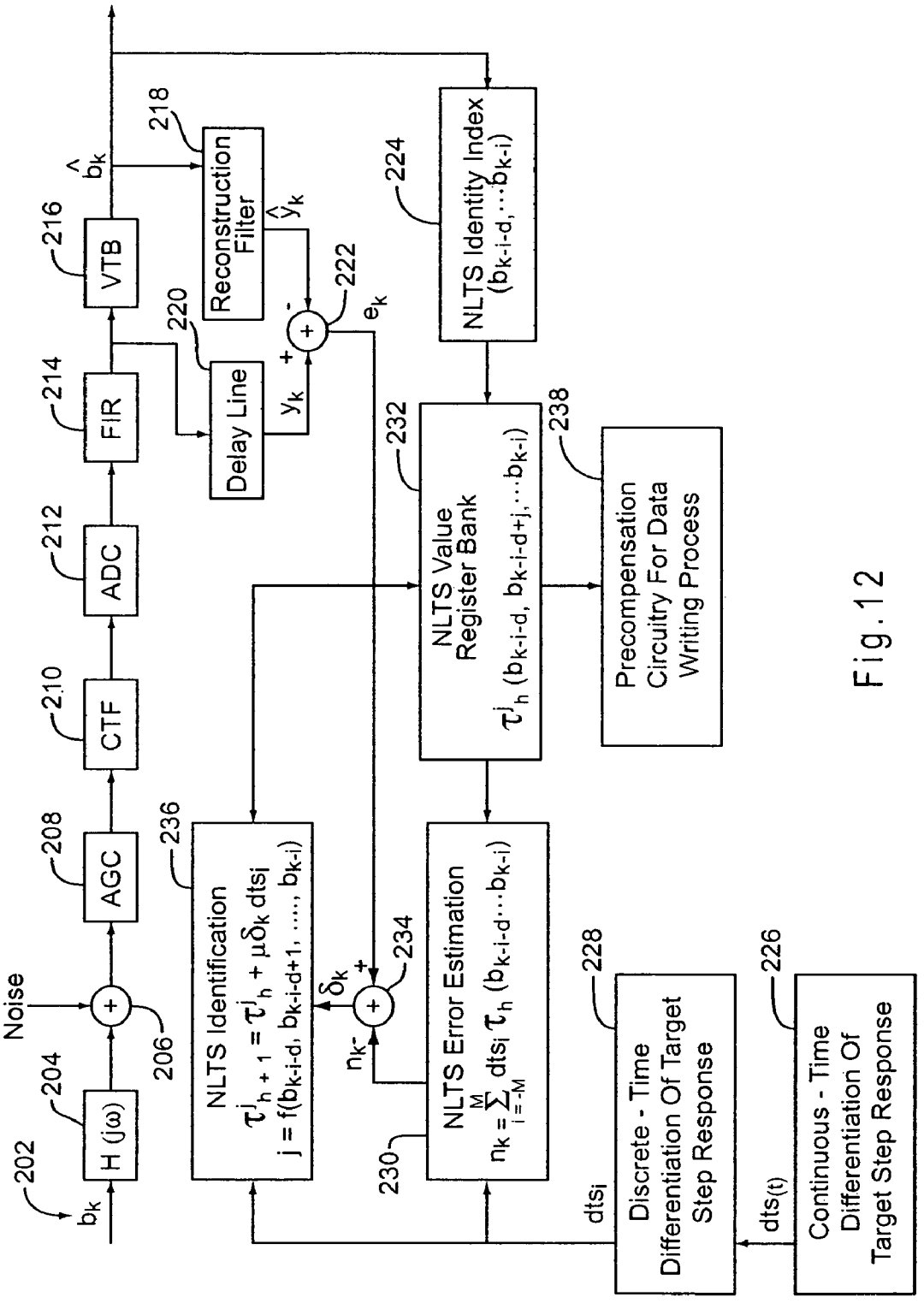
202
b_k
H (jω)
204
Noise
206
AGC
208
CTF
210
ADC
212
FIR
214
VTB
216
$\hat{b}_k$
218
Reconstruction Filter
$\hat{y}_k$
220
Delay Line
y_k
222
e_k
224
NLTS Identity Index
$(b_{k-i-d}, \cdots b_{k-i})$
232
NLTS Value Register Bank
$\tau^j_h (b_{k-i-d}, b_{k-i-d+j}, \cdots b_{k-i})$
238
Precompensation Circuitry For Data Writing Process
236
NLTS Identification
$\tau^j_{h+1} = \tau^j_h + \mu\delta_k dts_i$
$j = f(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$
δ_k
234
n_k
230
NLTS Error Estimation
$n_k = \sum_{i=-M}^{M} dts_i \tau_h (b_{k-i-d} \cdots b_{k-i})$
228
dts_i
Discrete - Time Differentiation Of Target Step Response
226
$dts_{(t)}$
Continuous - Time Differentiation Of Target Step Response

Fig. 12

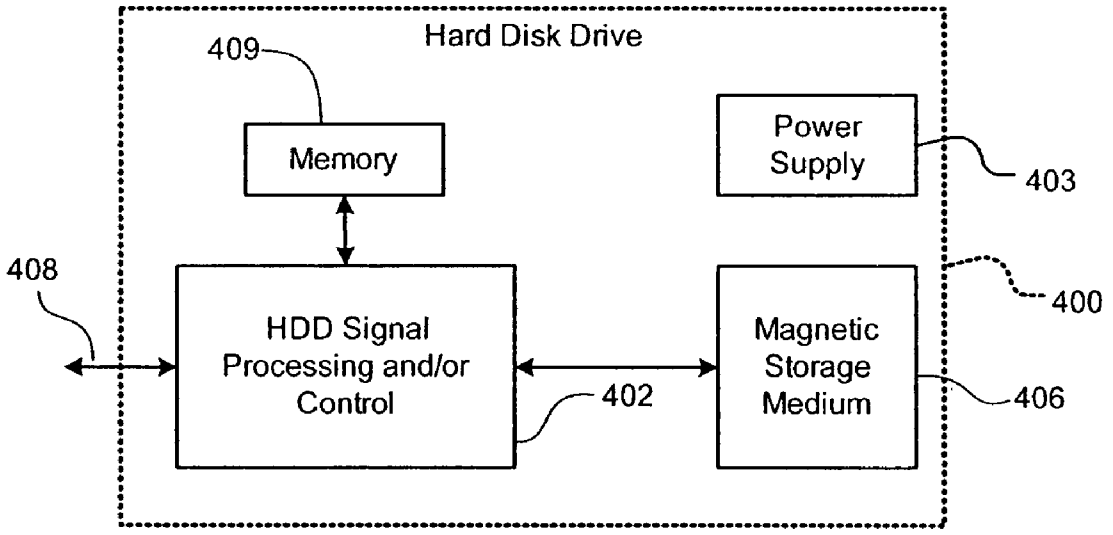

Fig.13A

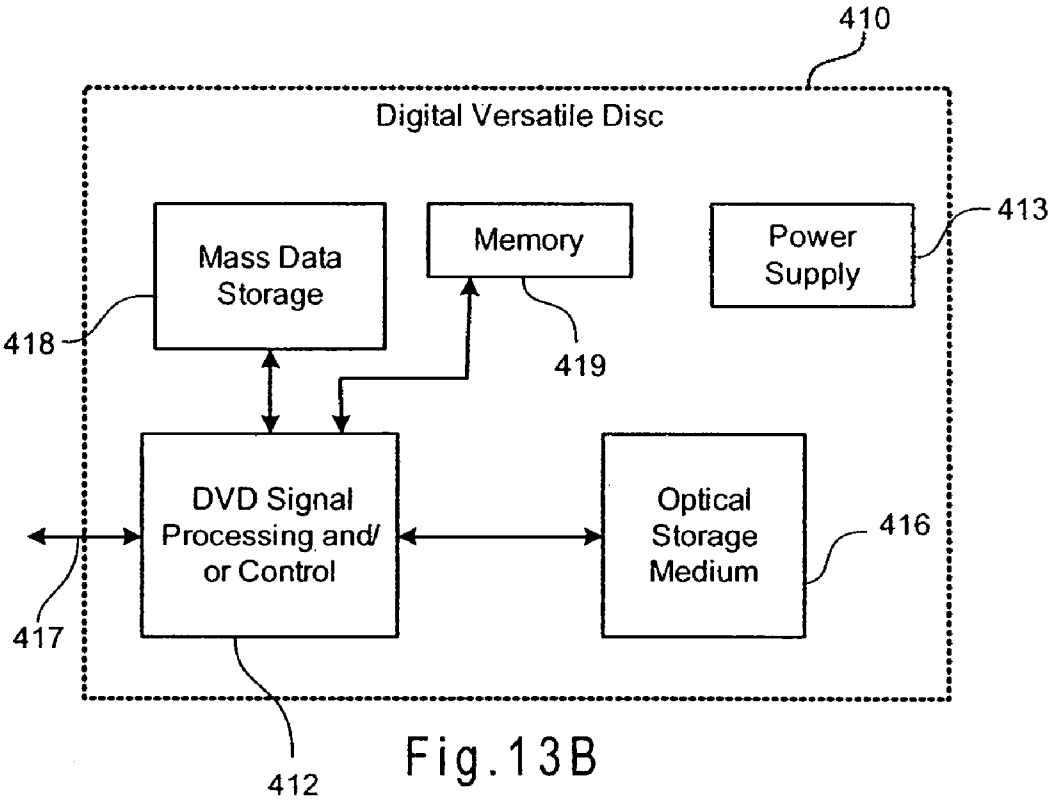

Fig.13B

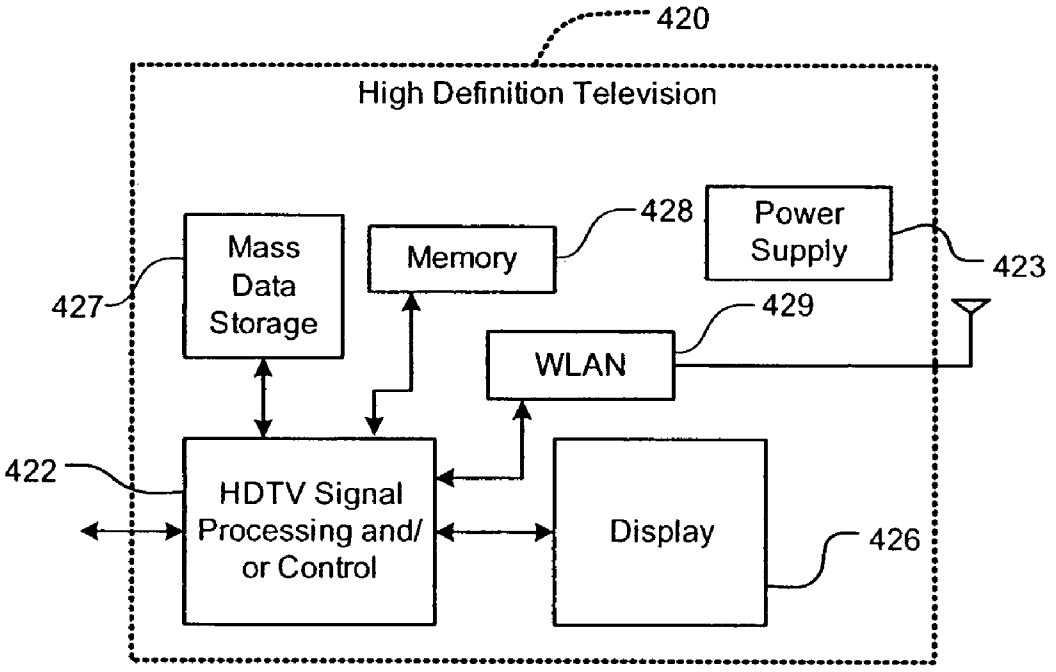

Fig.13C

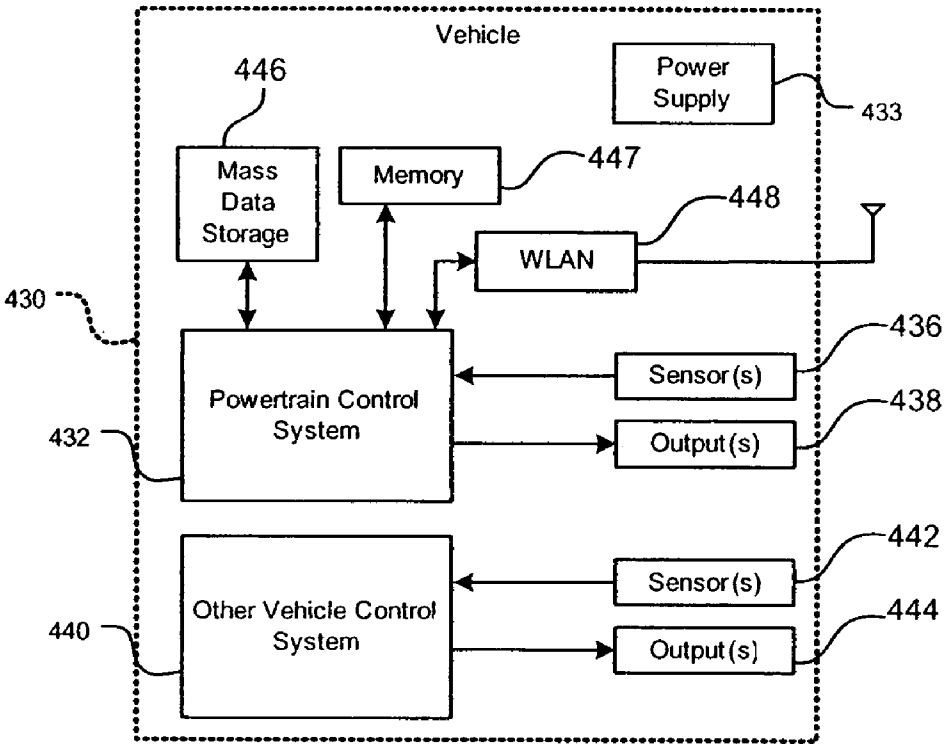

Fig.13D

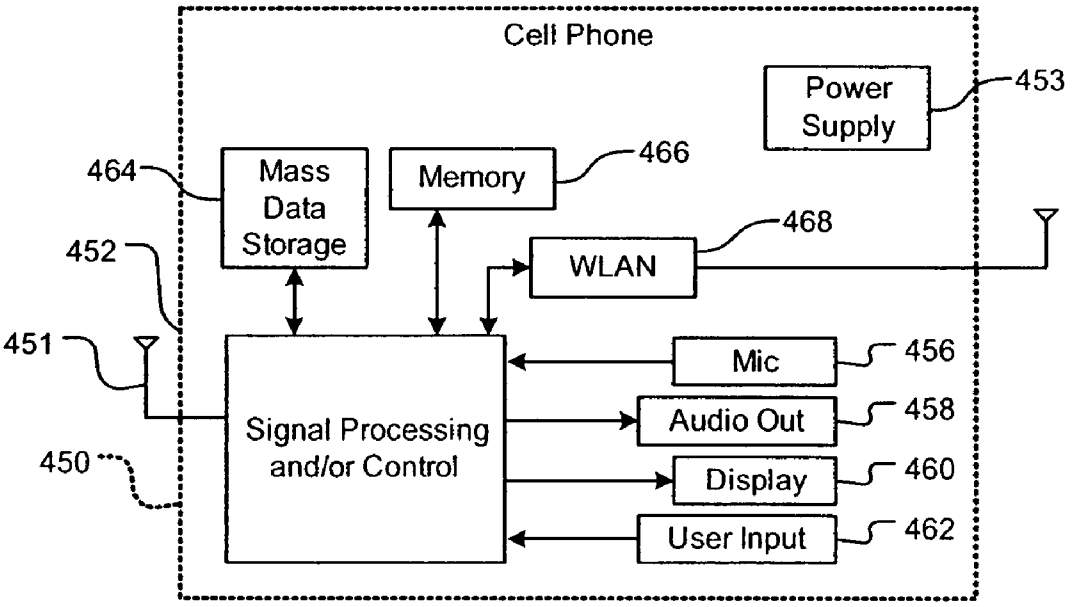

Fig.13E

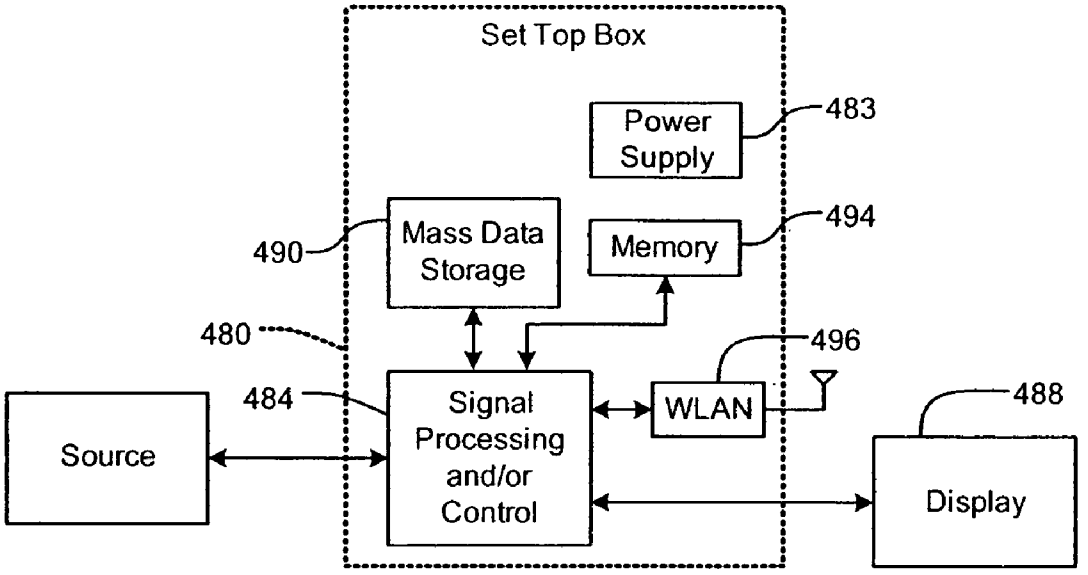

Fig.13F

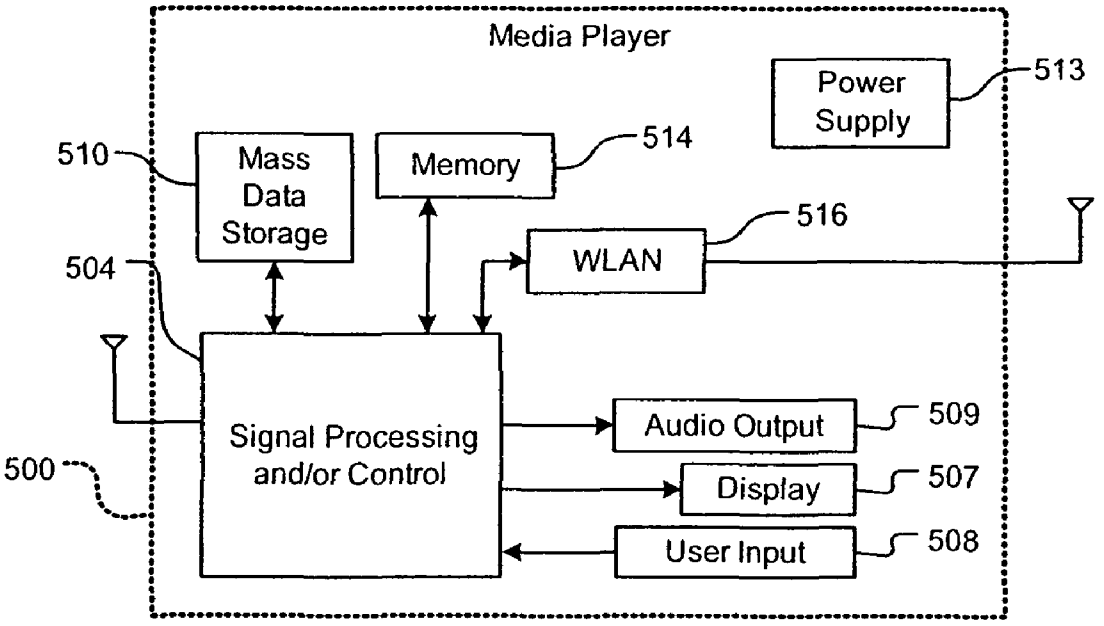
Media Player
Power Supply
513
510
Mass Data Storage
Memory
514
516
WLAN
504
Signal Processing and/or Control
Audio Output
509
Display
507
User Input
508
500

Fig. 13G

NON-LINEAR TRANSITION SHIFT IDENTIFICATION AND COMPENSATION

RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 60/790,877, filed Apr. 11, 2006, and 60/883,871, filed Jan. 8, 2007, which are incorporated herein by reference.

BACKGROUND

1. Technical Field

The present disclosure relates to magnetic media data storage devices. More particularly, the disclosure relates to a system and method for identifying and compensating for non-linear transition shift in magnetic media data storage devices.

2. Related Art

Non-linear transition shift is a phenomenon that affects the timing of the binary transitions of data signals written to the magnetic media in magnetic media data storage devices. When the recording head of a magnetic media data storage device attempts to write a binary transition to the recording medium, the current transition is affected by the magnetic fields of previously written transitions. These magnetic fields can cause the current transition to be shifted in time such that the transition is written either earlier or later than intended. Such time shifts can be a source of noise leading to unacceptable bit error rates when data stored on the magnetic medium are subsequently read back and used by associated data processing equipment.

If the amount of non-linear transition shift affecting a particular binary transition is known in advance, it is possible to compensate for the shift when the transition is written to the magnetic recording medium. For example, if it is known that a particular transition will be delayed by 0.1 nanoseconds, it is possible to write the transition 0.1 nanoseconds earlier. When the timing of a transition is pre-compensated in this manner, the transition will occur precisely where intended when it is subsequently read from the recording medium. A problem, however, is that non-linear transition is inconsistent. The magnetic fields that cause non-linear transition shift depend on the sequence of bits near a particular binary transition. Thus, the amount and direction of non-linear transition shift experienced by a particular binary transition will be dependent on the particular data sequence being written to the magnetic storage medium.

A traditional approach to compensating for non-linear transition shift involves generating a pseudorandom sequence of binary data, writing the pseudorandom sequence to the magnetic recording medium, and reading it back. The recovered sequence is then analyzed to determine the effect that the various bit patterns in the pseudorandom sequence have had on the corresponding binary transitions recorded on the magnetic medium. This traditional approach suffers from a number of drawbacks. The main drawbacks of this approach are that it typically requires over-sampling of the waveforms, it is not very accurate, and only a limited number of data patterns may be specified for defining the associated NLTS values. Furthermore, the compensation values may not be refined over time under actual operating conditions. An improved approach is desirable.

BRIEF SUMMARY

The following embodiments relate to systems and methods of identifying and compensating for non-linear transition shift in binary transitions written to magnetic media data storage devices. It is noted that throughout the specification the term "data" may relate to a data carrying waveform (e.g., an analog signal carrying binary transition information) or a binary sequence of bits, depending on the component in the pipeline being discussed.

In the embodiments described below, non-linear transition shift is measured "on-the-fly" and non-linear transition shift pre-compensation values are continuously updated to ensure that the most accurate and up-to-date pre-compensation values are employed when writing data (an analog waveform transition) to the magnetic storage medium.

In one embodiment a system for identifying non-linear transition shift of a transition in a waveform is disclosed. The system includes a bit pattern identification module adapted to identify bit patterns in segments of a data sequence read from the magnetic storage medium. A non-linear transition shift value register bank stores a non-linear transition shift value for each bit pattern. Each non-linear transition shift value is either an estimate value or a fixed value. The non-linear transition shift estimate values are updatable by an algorithm implemented in the system. The non-linear transition shift fixed values are predetermined and unchangeable. The non-linear transition shift fixed values may be based upon one or more known characteristics of non-linear transition shift behavior. The various non-linear transition shift values stored in the non-linear transition shift value register bank are associated with specific bit patterns of finite length. Finally, the system includes a non-linear transition shift error estimation module for calculating a non-linear transition shift error estimate based on the non-linear transition shift values stored in the non-linear transition shift value register bank.

In another embodiment a magnetic media data storage device is disclosed. The magnetic media data storage device includes a magnetic medium and a magnetic read/write head for reading data from and writing data to the magnetic medium. A write channel prepares binary data to be written to the magnetic medium via the magnetic write head. A magnetic head/media channel generates a continuous-time analog waveform that corresponds to the data that was previously written to the magnetic medium, although the magnetic head/media channel (output) waveform may be corrupted by some noise. The magnetic media data storage device includes a non-linear transition shift identification module adapted to identify the non-linear transition shift of binary transitions (introduced during the write operation) in the waveform received from the magnetic head/media channel. A non-linear transition shift compensation module is adapted to temporally adjust when the binary transitions associated with specific bit patterns are written to the magnetic head/media channel. The adjusted timing of writing a binary transition to the magnetic head/media channel may be based on the actual non-linear transition shift identified by the non-linear transition shift identification module for a specific bit pattern.

In another embodiment a system for compensating for non-linear transition shift in a magnetic medium data storage device is disclosed. In this embodiment a non-linear transition shift compensation system includes a non-linear transition shift estimation module adapted to generate non-linear transition shift estimates for specific bit patterns. The system further includes a pre-compensation module adapted to adjust the temporal spacing of binary transitions written to the magnetic head/media channel. The amount of pre-compensation applied to a transition is based on a non-linear transition shift estimate generated by the non-linear transition shift estimation module. The non-linear transition shift estimate selected as a pre-compensation value depends on the specific bit pat-

tern associated with the transition. Preferably, at least one bit pattern is associated with a non-linear transition shift value that is fixed, and therefore unchangeable by the non-linear transition shift estimation module.

A method of compensating for non-linear transition shift in a binary transition written to a magnetic data recording medium is also provided. The method includes defining a binary segment length. According to the method, non-linear transition shift values are provided for the various bit patterns that may be found in a binary segment of the defined binary segment length. Each non-linear transition shift value is either an estimate value or a fixed value. Binary data are read from the magnetic recording medium. The bit patterns in segments of the binary data read from the magnetic medium are identified. The non-linear transition shifts associated with binary transitions read from the magnetic medium is determined, and the corresponding bit pattern associated with each non-linear transition shift is identified. The actual non-linear transition shifts and their associated bit patterns are compared to the non-linear transition shift estimates generated for the corresponding bit patterns. The non-linear transition shift estimate values are adjusted based on the comparison. The time at which a binary transition associated with a particular bit pattern is written to the magnetic head/media channel is adjusted based on the non-linear transition shift estimates. The preferred embodiments will now be described with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a simplified block diagram of a magnetic medium data storage device.

FIG. **2** is a flowchart illustrating a method of identifying non-linear transition shift in a data sequence read from a magnetic storage medium.

FIG. **3** is a continuous-time plot of the magnetic head/media channel step response of an ideal binary transition and a binary transition subject to non-linear transition shift.

FIG. **4** is a continuous-time plot of the equalized target step response of an ideal binary transition and a binary transition subject to non-linear transition shift.

FIG. **5** is a continuous-time plot of the differentiated target step response shown in FIG. **4**.

FIG. **6** is a discrete-time plot of the differentiated target step response shown in FIG. **4**.

FIG. **7** is a table showing an example of non-linear transition shift values for all of the possible bit patterns of a 4-bit segment of a binary sequence.

FIG. **8** is a representative portion of a binary sequence.

FIG. **9** is a discrete time plot of the differentiated target step response of a binary transition occurring at a time k.

FIG. **10** is a discrete time plot of the differentiated target step response of a binary transition occurring at a time k−1.

FIG. **11** is a discrete time plot of the differentiated target step response of a binary transition occurring at a time k+1.

FIG. **12** is a block diagram of the read channel, including the read/write head, of a magnetic medium data storage device.

FIG. **13**A is a functional block diagram of a hard disk drive;

FIG. **13**B is a functional block diagram of a digital versatile disk (DVD);

FIG. **13**C is a functional block diagram of a high definition television;

FIG. **13**D is a functional block diagram of a vehicle control system;

FIG. **13**E is a functional block diagram of a cellular phone;

FIG. **13**F is a functional block diagram of a set top box; and

FIG. **13**G is a functional block diagram of a media player.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

The embodiments below relate to identifying non-linear transition shift (NLTS) that may occur when a binary transition is written to a magnetic data storage medium. The NLTS is identified in the read channel of a read/write magnetic data storage device and applied to data in the write channel of the device to pre-compensate for anticipated NLTS.

FIG. **1** is a simplified block diagram of a magnetic media data storage device **10** including NLTS identification and compensation. The magnetic data storage device **10** includes a write channel **12**, a magnetic read/write head **16**, a storage medium **18**, and a read channel **20**. The magnetic read/write head **16** may include a separate read head and a separate write head, or the two may be combined into a single read/write head as shown. The magnetic read/write head **16** and the storage medium **18** may be referred to in combination as a magnetic head/media channel **14**.

The write channel **12** is adapted to receive user data in the form of input binary sequences **22** to be written to the magnetic read/write head **16** and stored on the storage medium **18**. The read channel **20** receives a waveform from the magnetic head/media channel **14** corresponding to data retrieved from the storage medium **18** and outputs binary sequences **24**.

The read channel **20** includes an NLTS identification block **28**. The NLTS identification block **28** identifies NLTS in the waveform received from the magnetic head/media channel **14**. Similarly, the write channel **12** includes an NLTS pre-compensation block **26**. The information obtained by the NLTS identification block **28** may be provided to the NLTS pre-compensation block **26** so that the effects of NLTS may be reduced or eliminated by delaying or advancing the individual binary transitions written to the magnetic head/media channel **14**.

Both the read channel NLTS identification block **28** and the write channel pre-compensation block **26** may include a processor **27**, e.g. a central processing unit (CPU), and a memory **29**, or have access to a processor **27** and memory **29**. The memory **29** may be configured to store instructions that may be executed by the processor **27** for executing the NLTS identification and pre-compensation algorithms described below. The memory **29** may also be adapted to store parameters and variable data associated with identifying and compensating for NLTS. Both the NLTS pre-compensation block **26** and the NLTS identification block **28** may employ their own processor **27** and memory **29**, or they may share a common processor **27** and memory **29**. Alternatively, one or both of the NLTS identification block **28** and the pre-compensation block **26** may access a remote processor **27** and memory **29**. In alternative embodiments, dedicated hardware implementations, such as application specific integrated circuits, programmable logic arrays and other hardware devices, may be constructed to implement one or more of the NLTS identification and compensation algorithms described herein. Accordingly, the present system encompasses software, firmware, and hardware implementations or a combination thereof.

NLTS is bit pattern specific. The amount and direction of NLTS for a particular transition depends on the sequence of bits near the transition. The NLTS identification block **28** identifies the amount and direction of NLTS associated with individual transitions and the particular bit patterns near them. The NLTS pre-compensation block **26** adjusts the timing of a transition written to the magnetic head/media channel **14** by an amount and in a direction necessary to compensate for anticipated NLTS based on the bit pattern of the binary

sequence near the transition. The pre-compensation combines with the actual NLTS such that NLTS error is substantially reduced or eliminated.

The NLTS identification block **28** employs an algorithm for identifying NLTS "on-the-fly" as a waveform is received from the magnetic head/media channel **14**. FIG. **2** is a flowchart outlining the NLTS identification process. A first preliminary step **30** is to define the target (ideal) step response for the magnetic head/media channel **14**. FIG. **3** shows the continuous-time step response **60** for an ideal binary transition occurring at time **0**. FIG. **3** also shows the continuous-time step response **62** for a binary transition subject to an NLTS. The continuous-time NLTS step response **62** is substantially identical to the continuous-time ideal step response **60**, but translated in time by an amount τ. For a particular transition, the pattern of bits near the transition will determine the magnitude and direction of the NLTS shift τ.

Typically the read channel **20** of a magnetic data storage device will equalize the data signal received from the magnetic head/media channel **14** so that the magnetic head/media channel **14** transfer function will conform to a desired target polynomial. FIG. **4** shows the equalized continuous-time step response **64** for the continuous-time ideal step response **60**, and the equalized continuous-time step response **66** for the continuous-time NLTS step response **62**. Again, the equalized continuous-time NLTS step response **66** has substantially the same shape as the equalized continuous-time ideal step response **64** but is translated in time by the amount τ.

The equalized continuous-time ideal step response **64** may be represented as a function TS(t). The equalized continuous-time NLTS step response **66** may be represented by the function TS(t+τ). The difference between the equalized continuous-time ideal step response **64** and the equalized continuous-time NLTS step response **66** may be determined by the equation

$$DTS(t)=TS(t+\tau)-TS(t) \quad [1]$$

For sufficiently small values of τ the difference DTS(t) may be approximated as

$$DTS(t) \approx \frac{dTs}{dt} \cdot \tau = dts(t), \text{ where } dts(t) = \frac{dTS(t)}{dt} \quad [2]$$

The term dts(t) is simply the time derivative of the equalized continuous-time ideal step response **64** of a transition at time **0** (the target response). Equation [2] says that, for small valves of τ, the difference between the equalized continuous-time NLTS step response **66** and the equalized continuous-time ideal step response **64**, the error introduced by the NLTS shift, is approximately equal to the time derivative of the equalized continuous-time ideal step response **64** multiplied by the amount of the shift. This relationship is employed by the NLTS identification algorithm in the NLTS identification block **28** to estimate the NLTS error in the waveform received from the magnetic head/media channel **14**.

The next step in the NLTS identification process calls for generating the discrete-time differential ideal step response **32**. The continuous-time differential ideal step response dts(t) is not dependent on the sequence of bits read from the head/media channel **14** and may be calculated directly from the equalized continuous-time ideal step response **64** (TS(t)). FIG. **5** shows the continuous time differentiation **68** of the equalized continuous-time ideal step response **64** of FIG. **4**. The discrete-time differentiation of the ideal step response may be obtained by sampling the continuous time differentiation **68** at regular intervals over a predefined window of time. FIG. **6** shows the discrete-time differentiation **70** of the equalized continuous-time ideal step response **64** of FIG. **4**. The discrete-time differentiation **70** comprises a plurality of discrete data points **72** corresponding to the values of the continuous-time differentiation **68** of the equalized continuous-time ideal step response **64** at specific instances of time.

As has been mentioned, NLTS is determined by the specific bit pattern of the binary sequence in the vicinity of a particular binary transition. The influence a particular bit has on a specific transition diminishes with its physical and temporal distance from the transition. In other words, those bits within a binary sequence that are nearest a transition will have the greatest impact on any NLTS shift experienced by the transition. Those bits further away from the transition will have less impact. At some point, the impact of bits further away from a transition become negligible. Accordingly, another preliminary step in the NLTS identification process is to define the length of a binary sequence segment **34** that will be considered when identifying and compensating for NLTS. As will be described in more detail below, a parameter d may be defined such that a bit sequence d+1 bits long will be considered for identifying and compensating for NLTS. In most cases a value of d in the range of 3-5 will be appropriate, although other values may be applied as well.

The length of the binary sequence defined by the parameter d determines the resolution of the NLTS identification process. Because the amount of NLTS shift experienced by a binary transition is dependent on the pattern of the waveform in the vicinity of the transition, the number of NLTS gradations that may be identified is determined by the number of bits in the binary sequence whose impact is considered on NLTS. Consider a situation where a two bit segment of a binary sequence is employed for identifying NLTS. This is another way of saying that the total amount of NLTS shift experienced by a binary transition is determined by a two bit segment of a binary sequence. A two bit segment can generate four distinct bit patterns:

00

01

10

11

Because NLTS is dependent on the bit pattern near a binary transition, any amount of NLTS shift experienced by a binary transition must be ascribed to one of these four bit patterns. Obviously increasing the length of the binary segment will increase the NLTS identification resolution. A three bit segment can generate 8 distinct bit patterns, a four bit sequence can generate 16 bit patterns, and so forth, doubling the resolution with each additional bit.

A final preliminary step **36** in the NLTS identification process is to generate estimates for the amount of NLTS shift τ associated with bit patterns in a binary segment of the length defined at step **34**. For example, FIG. **7** is a table **74** showing NLTS shift values τ for every possible bit pattern of a four bit binary segment (d=3). Some NLTS shift values may be estimated values that can be updated and some NLTS shift values may be fixed values. For example, in FIG. **7** the bit pattern 0000 may correspond to a fixed amount of NLTS shift τ=A; the bit pattern 0001 may initially correspond to an estimated amount of NLTS shift τ=B, and so forth. Initially, the various NLTS shift estimated values need not be particularly accurate, as they will be adaptively adjusted later in the process.

The fixed NLTS shift values are based upon known properties of a particular bit pattern, are assumed to be accurate, and are not adjusted.

Once the discrete-time differentiated ideal step response has been generated and NLTS shift estimated and/or fixed values have been determined and stored for the various bit patterns that may be encountered in the d+1 bit long segments of a binary sequence, a continuous-time analog waveform corresponding to a binary sequence written to the magnetic head/media channel **14** is received from the magnetic head/media channel **14** at step **38**. FIG. **8** shows a sample binary segment **76** corresponding to a continuous-time analog waveform received from the magnetic head/media channel **14**. The binary segment **76** is centered around a time k. The binary segment **76** includes the bit b_k received at time k, the four bits b_{k-1}, b_{k-2}, b_{k-3}, and b_{k-4} preceding b_k, and the four bits immediately following b_k, b_{k+1}, b_{k+2}, b_{k+3}, and b_{k+4}. In FIG. **8**, the binary segment **76** has the bit pattern 101100001.

The next step **40** in the NLTS identification process is to calculate an estimate n_k of the total NLTS error present in a signal received from the magnetic head/media channel **14** at a given time k, provided that the bit pattern surrounding k does not correspond to an NLTS fixed value (step **39**).

An estimate of the total NLTS error n_k for a particular time is based upon the binary transition that occurs at that particular time as well as neighboring transitions. In other words, the total NLTS error at a particular time k is equal to the sum of the NLTS error contribution from the transition at time k plus the NLTS error contributions of several neighboring transitions. This phenomenon is best understood graphically.

Recall that FIG. **6** shows the discrete-time differentiation **70** of the ideal step response for the magnetic head/media channel **14** for a binary transition occurring at time t=0. FIG. **9** shows the discrete-time differentiation of the ideal step response for the magnetic head/media channel **14** for a transition occurring at time t=k. The two curves are substantially identical except that the curve in FIG. **9** has been translated in time and is centered around t=k rather than t=0. From Equation [2] the NLTS error due to the transition at time k is given by

$$\mathrm{DTS}(t)=\mathrm{dts}(t)\cdot\tau$$

In the discrete time domain Equation [2] may be restated as

$$\mathrm{DTS}_i=\mathrm{dts}_i\cdot\tau$$

Where i is a sampling index identifying the various data points **80**, **82**, . . . **96** of the discrete time differentiation of the ideal step response of the magnetic head/media channel **14** for a transition at time k. τ is a function of the bit pattern in a segment of the received binary sequence (b_{k-d}, b_{k-d+1}, . . . , b_k). In the example given earlier, the parameter d was assigned a value d=3. Thus, τ for the transition occurring at time k is a function of the bit pattern of the segment of the received binary sequence (b_{k-3}, b_{k-2}, b_{k-1}, b_k). Referring to FIG. **8**, $\tau(b_{k-3}, b_{k-2}, b_{k-1}, b_k)=\tau(0110)$. Referring to the table in FIG. **7**, τ(0110) corresponds to an NLTS shift τ(0110)=G. The NLTS error caused by the binary transition at time k is approximately equal to the discrete-time differentiated ideal step response for a binary transition occurring at time k times τ(0110), or $\mathrm{dts}_{88}\cdot G$. Graphically this means multiplying each data point 80, 82 . . . 96 of the discrete-time differentiation of the ideal step response for the binary transition at time k by an amount G. As is quite clear from FIG. **9**, the NLTS shift of the binary transition at time k based on the bit pattern 0110 will cause NLTS error at times other than time k. For example, at time k+1 the NLTS of a binary transition at time k will cause NLTS shift error equal to the value 90 of the discrete-time differentiated ideal step response at time k+1 times G. Similarly, at time k−1 the NLTS of the binary transition at time k will cause NLTS shift error equal to the discrete-time value 86 of the differentiated ideal step response at k−1 times G.

Just as the NLTS shift incurred by the binary transition at time k causes residual NLTS error at times other than time k, the NLTS shift of binary transitions occurring at times other than time k will similarly cause residual NLTS error at time k. For example, FIG. **10** shows the discrete-time differentiation of the ideal step response for the magnetic head/media channel **14** for a binary transition occurring at a time k−1. τ for the transition shift occurring at k−1 is a function of the bit pattern of the received binary sequence segment (b_{k-4}, b_{k-3}, b_{k-2}, b_{k-1}). Referring to FIG. **8**, $\tau(b_{k-4}, b_{k-3}, b_{k-2}, b_{k-1})=(1011)$. Referring to the table in FIG. **7**, τ(1011)=L. The NLTS error caused by the binary transition at time k−1 is approximately equal to $\mathrm{dts}_i\cdot\tau(1011)=\mathrm{dts}_i\cdot L$. Graphically this corresponds to multiplying each discrete value 98, 100, . . . 114 of the discrete-time differentiated ideal step response of the binary transition occurring at time k−1 by an amount L. As can be seen in FIG. **10**, the NLTS shift of the binary transition at time k−1 will generate NLTS error at time k in an amount equal to the discrete value 108 of the discrete time differentiated ideal step response for the binary transition occurring at time k−1 times L, or $\mathrm{dts}_{108}\cdot L$.

Similarly, FIG. **11** shows the discrete-time differentiation of the ideal step response for the magnetic head/media channel **14** for a binary transition occurring at time k+1. τ for the transition occurring at k+1 is a function of the bit pattern of the received binary sequence segment (b_{k-2}, b_{k-1}, b_k, b_{k+1}). Referring to FIG. **8**, $\tau(b_{k-2}, b_{k-1}, b_k, b_{k+1})=\tau(1100)$. Referring to the table in FIG. **7**, τ(1100)=M. The NLTS error caused by the binary transition at time k+1 is approximately equal to $\mathrm{dts}_i\cdot\tau(1100)=\mathrm{dts}_i\cdot M$. Graphically this corresponds to multiplying each discrete value 116, 118, . . . , 130 of the discrete-time differentiated ideal step response of the binary transition occurring at time k+1 by an amount M. As can be seen in FIG. **11**, the NLTS shift of the binary transition at time k+1 will generate NLTS error at time k in an amount equal to the discrete value 122 of the discrete-time differentiated ideal step response for the binary transition occurring at time k+1 times M, or $\mathrm{dts}_{122}\cdot M$.

The total NLTS error at time k resulting from the NLTS shift experienced by the binary transitions occurring at times k−1, k, and k+1 is equal to the sum of the NLTS error at time k from each transition, or

$$n_k=\mathrm{dts}_{108}\cdot L+dts_{88}\cdot G+dts_{122}\cdot M.$$

The discrete-time differentiated ideal step response is the same for each binary transition in the sequence, only translated in time. Thus, the discrete values of discrete-time differentiated step response of a transition at time **0** (FIG. **6**) may be applied to the calculation of the NLTS error estimate at other times. A time window may be defined where $-M\leqq i\leqq+N$. The time window may be symmetrical about the time τ=0 such that N=M and $-M\leqq i\leqq+M$. The estimate of the total NLTS error at a given time k anywhere in the read back waveform may be given by

$$n_k=\sum_{i=-M}^{+M} dts_i\cdot\tau_{k-i}(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i}). \qquad [3]$$

Returning to the flowchart of FIG. **2**, once the NLTS error estimate is calculated for time k, the next step **42** is to determine the actual NLTS error e_k in the read back waveform. The

NLTS error e_k may be obtained by subtracting an equalized waveform from a reconstructed ideal waveform created based on the most likely bit sequence corresponding to the received waveform. The NLTS error e_k can be compared to the estimated NLTS error n_k to determine the accuracy of the estimate. A difference function δ_K may be defined as

$$\delta_k = e_k - n_k = e_k - \sum_{i=-M}^{+M} dts_i \cdot \tau_{k-i}(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i}). \quad [4]$$

Ideally $|\delta_K|$ will be as small as possible. In other words, the estimated NLTS error n_K will be close or equal to the actual NLTS error e_k in the waveform received from the magnetic head/media channel **14**. Recall that the original values of $\tau(b_1, b_2, b_3, b_4)$ in the table **74** of FIG. **7** were either estimated or fixed values. The estimated values may be adjusted to minimize δ_K as indicated at step **46** of the NLTS identification process.

In one embodiment, the value of τ (FIG. **7**) may be fixed to a predetermined value(s) for one or more selected binary sequences. A predetermined value may be based upon one or more known characteristics of NLTS behavior. For example, the value for $\tau(0,0,0,0)$ may be fixed such that A=0 (FIG. **7**) if it is known that a succession of four bits without transition does not cause NLTS for a fifth bit having a transition.

For the values of τ that are adjustable, minimization of δ_K may be accomplished using the least mean squared algorithm. A new function c may be defined as

$$c = \delta_k^2 = (e_k - n_k)^2 = \left(e_k - \sum_{i=-M}^{N} dts_i \cdot \tau_{k-i}(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})\right)^2 \quad [5]$$

The gradient of C may be calculated as

$$\frac{\partial c}{\partial \tau_{k-i}} = -2 \cdot \delta_k \cdot dts_i. \quad [6]$$

The identity index of τ_{k-i} is $(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$. The time index k–i is the location where the binary transition with which τ_{k-i} is associated occurs. The identity index is limited by $[0, 2^{d+1}-1]$. The NLTS values can be adaptively obtained by

$$\tau_{n+1}^{j} = \tau_n^{j} + \mu\delta_k \cdot dts_i; \text{ where } j = f(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i}) \quad [7]$$

The variable μ defines the size of an incremental adjustment step, and the sign of δ_k determines the direction of adjustment. The new values for τ_{k-i} $(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$ are stored in an NLTS value register bank. In other words, the adjustable z values stored in table **74** of FIG. **7** may be replaced with the adjusted i values at step **488**. The adjusted values are communicated to the pre-compensation block **26** in the write channel **12** at step **50**.

The steps **38-50** of the NLTS identification process in FIG. **2** may be repeated for each binary transition in the received waveform. Over time the adjusted NLTS estimates become more and more accurate and the difference δ_K between the actual NLTS error e_k and the estimated NLTS error n_k becomes smaller and smaller.

The pre-compensation block **26** in the write channel **12** may use the values of $\tau(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$ stored in the NLTS value register bank to adjust the timing of binary transitions written to the head/media channel **14**. For example, assume the values in table **74** of the FIG. **7** have been adjusted, and the pre-compensation block **26** identifies the bit sequence $(b_{k-3}, b_{k-1}, b_{k-1}, b_k)$=0100. The estimated value of τ is E. In other words, it is estimated that the binary transition will be shifted by an amount E (in light of the bit pattern $(b_{k-3}, b_{k-1}, b_{k-1}, b_k)$=0100) when it is written to the storage medium **18**. The pre-compensation block **26** may alter the timing of the transition at time k by an amount –E. The pre-compensation amount –E will combine with the NLTS shift amount E to cancel-out the NLTS shift and the transition will occur at the proper time k when the transition is written to the storage medium.

FIG. **12** is a block diagram of a preferred embodiment of a magnetic data storage device read channel implementing the NLTS identification process described above. User data b_k **202** are written to the magnetic head/media channel **204**. The magnetic head/media channel **204** is characterized by the transfer function H(jω). White gaussian system noise is added at **206**. The read channel **20** includes automatic gain control (AGC) **208**; a continuous time filter (CTF) **210**; an analog-to-digital converter (ADC) **212**; and a finite impulse response filter (FIR) **214**. The output of the FIR filter **214** is input to a Viterbi detector (VTB) **216**, and a delay line **220**. The VTB detector **216** outputs a binary signal $\hat{b}_k$ which is a high reliability estimate of the original user data signal b_k **202** written to the magnetic head/media channel **204**. The output $\hat{b}_k$ of the VTB detector **216** is input to a reconstruction filter **218** and an NLTS identity index module **224**. The NLTS identity index module **224** identifies the bit patterns of finite segments of binary sequence $\hat{b}_k$ output from the VTB detector **216**. The reconstruction filter **218** generates the ideal waveform $\hat{y}_k$ from the binary sequence $\hat{b}_k$ based on the target polynomial of the read channel. The ideal waveform $\hat{y}_k$ is subtracted from the output of the FIR filter **214** y_k at summing junction **222**. The output of the FIR filter **214**, is delayed by delay line **220** in order to maintain synchronization with the output of the reconstruction filter **218**. The difference between y_k and $\hat{y}_k$ provides the error signal e_k.

The target polynomial dst(t) is provided at **226** and the discrete-time differentiation of the target (ideal) step response is calculated at **228**. The discrete-time differentiation of the target step response dts, is provided to an NLTS error estimation module **230**, and an NLTS identification module **236**. When a waveform is received from the magnetic head/media channel **204**, and the VTB detector **216** outputs the most likely binary sequence $\hat{b}_k$ corresponding to the received waveform, the NLTS identity index module **224** identifies the bit pattern in each successive segment of the binary sequence. The length of the bit patterns identified by the NLTS identify index module **224** is determined by the value of the parameter d. The binary segment length being equal to d+1. The bit patterns identified by the NLTS identity index module **224** are used to identify values for the NLTS shift estimate. Each value of the NLTS shift estimate τ is a function of the preceding bit pattern $(\tau_{k-i}$ $(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-1}))$. An NLTS value register bank **232** identifies the appropriate value of τ for each successive binary segment. The τ values are provided to the NLTS estimation module **230**, as well as to the pre-compensation circuitry **238** in the write channel. The τ values provided to the NLTS error estimation module **230** are used to calculate the NLTS error estimate n_k for the binary transitions in the received waveform. The NLTS estimate n_k is subtracted from the error signal e_k at summing junction **234** to produce the difference signal δ_k. δ_k is provided to the NLTS identification module **236** along with the discrete-time differentia-

tion of the target step response **228**. The NLTS identification module **236** adjusts the values of τ as described above in an effort to reduce the magnitude of δ_k. The adjusted values of τ are then stored in the NLTS value register bank **232**, replacing the previous estimates corresponding to the various bit patterns generated by the binary segments of length d+1. Thus, the NLTS values that are not fixed are continually refined, and improved NLTS values are provided to the pre-compensation circuitry **238** so that the write channel can compensate for expected NLTS shift when it writes data to the magnetic head/media channel **14**.

In various embodiments, two or more of the modules and/or blocks shown in FIG. **12** or discussed herein may be physically and/or functionally combined. Any one or combination of modules and/or blocks may be referred to in general as an NLTS module. Module is not to be regarded as a limiting term but rather as a term encompassing any type of device, circuit, component, or element to perform at least the function discussed in relation thereto.

Referring now to FIGS. **13**A-**13**G, various exemplary implementations of the present invention are shown. Referring now to FIG. **13**A, the present invention can be implemented in a hard disk drive **400**. In some implementations, the signal processing and/or control circuit **402** and/or other circuits (not shown) in the HDD **400** may process data, perform coding and/or encryption, perform calculations, and/or format data that is output to and/or received from a magnetic storage medium **406**.

The HDD **400** may communicate with a host device (not shown) such as a computer, mobile computing devices such as personal digital assistants, cellular phones, media or MP3 players and the like, and/or other devices via one or more wired or wireless communication links **408**. The HDD **400** may be connected to memory **409** such as random access memory (RAM), low latency nonvolatile memory such as flash memory, read only memory (ROM) and/or other suitable electronic data storage.

Referring now to FIG. **13**B, the present invention can be implemented in a digital versatile disc (DVD) drive **410**. For example, the present invention may be implemented on a mass data storage device of the DVD drive **410**. The signal processing and/or control circuit **412** and/or other circuits (not shown) in the DVD **410** may process data, perform coding and/or encryption, perform calculations, and/or format data that is read from and/or data written to an optical storage medium **416**. In some implementations, the signal processing and/or control circuit **412** and/or other circuits (not shown) in the DVD **410** can also perform other functions such as encoding and/or decoding and/or any other signal processing functions associated with a DVD drive.

The DVD drive **410** may communicate with an output device (not shown) such as a computer, television or other device via one or more wired or wireless communication links **417**. The DVD **410** may communicate with the mass data storage **418**, which stores data in a nonvolatile manner. The mass data storage **418** may include a hard disk drive (HDD). The HDD may have the configuration shown in FIG. **13**A. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The DVD **410** may be connected to memory **419** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage.

Referring now to FIG. **13**C, the present invention can be implemented in a high definition television (HDTV) **420**. For example, the invention may be implemented on a mass data storage of the HDTV **420**. The HDTV **420** receives HDTV input signals in either a wired or wireless format and generates HDTV output signals for a display **426**. In some implementations, signal processing circuit and/or control circuit **422** and/or other circuits (not shown) of the HDTV **420** may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other type of HDTV processing that may be required.

The HDTV **420** may communicate with the mass data storage **427** that stores data in a nonvolatile manner such as on a magnetic storage devices. At least one HDD may have the configuration shown in FIG. **13**A and/or at least one DVD may have the configuration shown in FIG. **13**B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The HDTV **420** may be connected to memory **428** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The HDTV **420** also may support connections with a WLAN via a WLAN network interface **429**.

Referring now to FIG. **13**D, the present invention may be implemented in a mass data storage device of a vehicle control system. In some implementations, a powertrain control system **432** receives inputs from one or more sensors such as temperature sensors, pressure sensors, rotational sensors, airflow sensors and/or any other suitable sensors and/or that generates one or more output control signals such as engine operating parameters, transmission operating parameters, and/or other control signals.

The present invention may also be implemented in relation to other control systems **440** of the vehicle **430**. For example, the control system **440** may likewise receive signals from input sensors **442** and/or output control signals to one or more output devices **444**. In some implementations, the control system **440** may be part of an anti-lock braking system (ABS), a navigation system, a telematics system, a vehicle telematics system, a lane departure system, an adaptive cruise control system, a vehicle entertainment system such as a stereo, DVD, compact disc and the like. Still other implementations are contemplated.

The powertrain control system **432** may communicate with mass data storage **446** that stores data in a nonvolatile manner. The mass data storage **446** may include magnetic storage devices such as hard disk drives HDD. At least one HDD may have the configuration shown in FIG. **13**A and/or at least one DVD may have the configuration shown in FIG. **13**B. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The powertrain control system **432** may be connected to memory **447** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The powertrain control system **432** also may support connections with a WLAN via a WLAN network interface **448**. The control system **440** may also include mass data storage, memory and/or a WLAN interface (all not shown).

Referring now to FIG. **13**E, the present invention can be implemented in a cellular phone **450** that may include a cellular antenna **451**. The present invention may be implemented in the mass data storage of the cellular phone **450**. In some implementations, the cellular phone **450** includes a microphone **456**, an audio output **458** such as a speaker and/or audio output jack, a display **460** and/or an input device **462** such as a keypad, pointing device, voice actuation and/or other input device. The signal processing and/or control circuits **452** and/or other circuits (not shown) in the cellular phone **450** may process data, perform coding and/or encryption, perform calculations, format data and/or perform other cellular phone functions.

The cellular phone **450** may communicate with mass data storage **464** that stores data in a nonvolatile manner on magnetic storage devices such as hard disk drives HDD. At least one HDD may have the configuration shown in FIG. **13**A. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The cellular phone **450** may be connected to memory **466** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The cellular phone **450** also may support connections with a WLAN via a WLAN network interface **468**.

Referring now to FIG. **13**F, the present invention can be implemented in a set top box **480**. The present invention be implemented in the mass data storage of the set top box **480**. The set top box **480** receives signals from a source such as a broadband source and outputs standard and/or high definition audio/video signals suitable for a display **488** such as a television and/or monitor and/or other video and/or audio output devices. The signal processing and/or control circuits **484** and/or other circuits (not shown) of the set top box **480** may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other set top box function.

The set top box **480** may communicate with the mass data storage **490** that stores data in a nonvolatile manner. The mass data storage **490** may include magnetic storage devices for example hard disk drives HDD. At least one HDD may have the configuration shown in FIG. **13**A. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The set top box **480** may be connected to memory **494** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The set top box **480** also may support connections with a WLAN via a WLAN network interface **496**.

Referring now to FIG. **13**G, the present invention can be implemented in a media player **500**. The present invention may be implemented in a mass data storage of the media player **500**. In some implementations, the media player **500** includes a display **507** and/or a user input **508** such as a keypad, touchpad and the like. In some implementations, the media player **500** may employ a graphical user interface (GUI) that typically employs menus, drop down menus, icons and/or a point-and-click interface via the display **507** and/or user input **508**. The media player **500** further includes an audio output **509** such as a speaker and/or audio output jack. The signal processing and/or control circuits **504** and/or other circuits (not shown) of the media player **500** may process data, perform coding and/or encryption, perform calculations, format data and/or perform any other media player function.

The media player **500** may communicate with mass data storage **510** that stores data such as compressed audio and/or video content in a nonvolatile manner. In some implementations, the compressed audio files include files that are compliant with MP3 format or other suitable compressed audio and/or video formats. The mass data storage may include magnetic storage devices for example hard disk drives HDD. At least one HDD may have the configuration shown in FIG. **13**A. The HDD may be a mini HDD that includes one or more platters having a diameter that is smaller than approximately 1.8". The media player **500** may be connected to memory **514** such as RAM, ROM, low latency nonvolatile memory such as flash memory and/or other suitable electronic data storage. The media player **500** also may support connections with a WLAN via a WLAN network interface **516**.

It is intended that the foregoing detailed description be understood as an illustration of selected forms that the invention can take and not as a definition of the invention. It is only the following claims, including all equivalents, that are intended to define the scope of this invention.

The invention claimed is:

1. A system comprising:

a register to store a plurality of non-linear transition shift (NLTS) values, at least one of the plurality of NLTS values being an adjustable NLTS estimate value, wherein the NLTS values correspond to finite length data patterns; and

a NLTS module adapted to:

compensate for NLTS using the adjustable NLTS estimate value;

determine a NLTS error in a write time of a binary transition from a received waveform after compensating for NLTS; and

adjust the NLTS estimate value stored in the register based at least in part on the NLTS error.

2. The system of claim **1** wherein the plurality of NLTS values includes at least one NLTS fixed value.

3. The system of claim **1** wherein the NLTS module is adapted to determine a NLTS error estimate for a waveform transition based at least in part upon at least one of the plurality of NLTS values, the NLTS error being based at least in part on the NLTS error estimate.

4. The system of claim **1** wherein the NLTS module is adapted to adjust the NLTS estimate value based on a discrete-time differentiation of a read channel target step response.

5. The system of claim **4** wherein the read channel target step response is an ideal step response.

6. The system of claim **1** wherein the NLTS error is based at least in part on an actual NLTS error in the received waveform.

7. The system of claim **1** wherein the NLTS module is adapted to estimate NLTS error according to a formula:

$$n_k = \sum_{i=-M}^{N} dts_i \cdot \tau_{k-i}(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$$

where

n_k is a non-linear transition shift error estimate at time k,

i is a discrete time sample index,

−M and N define a time window,

k is a point in time,

dts_i is a discrete-time differentiation of a read channel target step response,

$\tau_{k-i}(b_{k-i-d}, b_{k-i+1}, \ldots, b_{k-1})$ is a non-linear transition shift value for a transition, wherein τ_{k-i} is a function of the finite length data patterns, and

d is a parameter defining a finite length.

8. The system of claim **1** comprising a NLTS identification module to adjust the NLTS estimate value.

9. The system of claim **1** comprising a NLTS identification module to adjust the NLTS estimate value according to a formula:

$$\tau_{h+1}{}^{j} = \tau_h{}^{j} + \mu\delta_k \cdot dts_i,$$

where

$j = f(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$,

i is a discrete time sample index,

k is a point in time,

μ defines a size of an incremental adjustment step,

δ_k is the NLTS error, the NLTS error being based on a difference between an NLTS error estimate and an actual NLTS error in a received waveform,

dts_i is a discrete-time differentiation of a read channel target step response,

$(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$ is a bit pattern corresponding to a segment of a data sequence, and

d is a parameter defining a finite length.

10. The system of claim **1**, wherein the received waveform comprises a first received waveform; and wherein the NLTS module is further adapted to reduce the NLTS error based on a second received waveform.

11. The system of claim **1**, wherein the NLTS module is configured to iterate in order to reduce the NLTS error.

12. A system comprising:

means for storing a plurality of non-linear transition shift (NLTS) values, at least one of the plurality of NLTS values being an adjustable NLTS estimate value, wherein the NLTS values correspond to finite length data patterns; and

means for compensating for NLTS using the adjustable NLTS estimate value;

means for determining a NLTS error in a write time of a binary transition from a received waveform after compensating for NLTS; and

means for adjusting the NLTS estimate value stored in the register based on the NLTS error.

13. The system of claim **12** wherein the plurality of NLTS values includes at least one NLTS fixed value.

14. The system of claim **12** comprising means for determining a NLTS error estimate for a waveform transition based at least in part upon at least one of the plurality of NLTS values, the NLTS error being based at least in part on the NLTS error estimate.

15. The system of claim **12** comprising means for adjusting the NLTS estimate value based on a discrete-time differentiation of a read channel target step response.

16. The system of claim **15** wherein the read channel target step response is an ideal step response.

17. The system of claim **12** wherein the NLTS error is based in part on an actual NLTS error in the received waveform.

18. The system of claim **12** wherein the means for adjusting the NLTS estimate value receives a difference between a NLTS error estimate and an actual NLTS error in the received waveform.

19. The system of claim **12** wherein the means for adjusting the NLTS estimate value uses a least mean squared algorithm.

20. The system of claim **12**, wherein the received waveform comprises a first received waveform, the system further comprising means for reducing the NLTS error based on a second received waveform.

21. The system of claim **12**, further comprising means for iterating in order to reduce the NLTS error.

22. A method comprising:

storing a plurality of non-linear transition shift (NLTS) values, including an adjustable NLTS estimate value, wherein the NLTS values correspond to finite length data patterns

compensating for NLTS using the adjustable NLTS estimate value;

determining a NLTS error in a write time of a binary transition from a received waveform after compensating for NLTS; and

adjusting the NLTS estimate value based on the NLTS error.

23. The method of claim **22** wherein the plurality of NLTS values includes at least one NLTS fixed value.

24. The method of claim **22**, wherein the NLTS error is based at least in part on a NLTS error estimate.

25. The method of claim **22** comprising adjusting the NLTS estimate value based on a discrete-time differentiation of a read channel target step response.

26. The method of claim **25** wherein the read channel target step response is an ideal step response.

27. The method of claim **22**, wherein the NLTS error is based at least in part on an actual NLTS error in the received waveform.

28. The method of claim **22** comprising estimating NLTS error according to a formula:

$$n_k = \sum_{i=-M}^{N} dts_i \cdot \tau_{k-i}(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$$

where

n_k is a non-linear transition shift error estimate at time k,

i is a discrete time sample index,

−M and N define a time window,

k is a point in time,

dts_i is a discrete-time differentiation of a read channel target step response,

τ_{k-i} $(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$ is a non-linear transition shift value for a transition, wherein τ_{k-i} is a function of the finite length data patterns, and

d is a parameter defining a finite length.

29. The method of claim **22** comprising adjusting the NLTS estimate value based on a difference between a NLTS error estimate and an actual NLTS error in the received waveform.

30. The method of claim **22** comprising adjusting the NLTS estimate value using a least mean squared algorithm.

31. The method of claim **22** comprising adjusting the NLTS estimate value according to a formula:

$$\tau_{h+1}{}^{j} = \tau_h{}^{j} + \mu\delta_k \cdot dts_i,$$

where

$j = f(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$,

i is a discrete time sample index,

k is a point in time,

μ defines a size of an incremental adjustment step,

δ_k is the NLTS error, the NLTS error being based on a difference between an NLTS error estimate and an actual non-linear transition shift error in the received waveform,

dts_i is a discrete-time differentiation of a read channel target step response,

$(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$ is a bit pattern corresponding to a segment of a data sequence, and

d is a parameter defining a finite length.

32. The method of claim **22**, wherein the received waveform comprises a first received waveform, the method further comprising reducing the NLTS error based on a second received waveform.

33. The method of claim **22**, further comprising iterating in order to reduce the NLTS error.

34. A computer readable tangible storage medium having processor executable instructions to:

store a plurality of non-linear transition shift (NLTS) values, including a NLTS estimate value, wherein the NLTS values correspond to finite length data patterns;

compensate for NLTS using the adjustable NLTS estimate value;

determine a NLTS error in a write time of a binary transition from a received waveform after compensating for NLTS; and

adjust the NLTS estimate value based on the NLTS error.

35. The computer readable storage medium of claim **34** wherein the plurality of NLTS values includes at least one NLTS fixed value.

36. The computer readable storage medium of claim **34** having processor executable instructions to determine a NLTS error estimate for a waveform transition based at least in part upon at least one of the plurality of NLTS values, the NLTS error being based at least in part on the NLTS error estimate.

37. The computer readable storage medium of claim **34** having processor executable instructions to adjust the NLTS estimate value based on a discrete-time differentiation of a read channel target step response.

38. The computer readable storage medium of claim **37** wherein the read channel target step response is an ideal step response.

39. The computer readable storage medium of claim **34**, wherein the NLTS error is based at least in part on an actual NLTS error in the received waveform.

40. The computer readable storage medium of claim **34** having processor executable instructions to estimate NLTS error according to a formula:

$$n_k = \sum_{i=-M}^{N} dts_i \cdot \tau_{k-i}(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$$

where

n_k is a non-linear transition shift error estimate at time k,

i is a discrete time sample index,

−M and N define a time window,

k is a point in time,

dts_i is a discrete-time differentiation of a read channel target step response,

τ_{k-i} (b_{k-i-d}, $b_{k-i-d+1}$, b_{k-i}) is a non-linear transition shift value for a transition, wherein τ_{k-i} is a function of the finite length data patterns, and

d is a parameter defining a finite length.

41. The computer readable storage medium of claim **34** having processor executable instructions to adjust the NLTS estimate value based on a difference between a NLTS error estimate and an actual NLTS error in the received waveform.

42. The computer readable storage medium of claim **34** having processor executable instructions to adjust the NLTS estimate value using a least mean squared algorithm.

43. The computer readable storage medium of claim **34** having processor executable instructions to adjust the NLTS estimate value according to a formula:

$$\tau_{k+1}^{j} = \tau_k^{j} + \mu\delta_k \cdot dts_i,$$

where

$j = f(b_{k-i-d}, b_{k-i-d+1}, \ldots, b_{k-i})$,

i is a discrete time sample index,

k is a point in time,

μ defines a size of an incremental adjustment step,

δ_k is the NLTS error, the NLTS error being based on a difference between a NLTS error estimate and an actual non-linear transition shift error in the received waveform,

dts_i is a discrete-time differentiation of a read channel target step response,

(b_{k-i-d}, $b_{k-i-d+1}$, . . . , b_{k-i}) is a bit pattern corresponding to a segment of a data sequence, and

d is a parameter defining a finite length.

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