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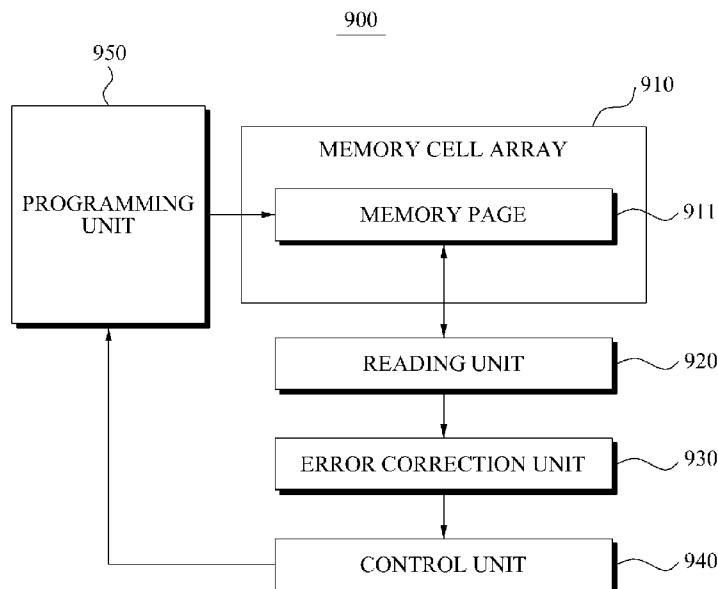
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(54) Title: MEMORY DEVICE AND METHOD OF MANAGING MEMORY DATA ERROR

[Fig. 9]



(57) Abstract: Memory devices and/or methods of managing memory data errors are provided. A memory device detects and corrects an error bit of data read from a plurality of memory cells, and identifies a memory cell storing the detected error bit. The memory device assigns a verification voltage to each of the plurality of first memory cells, the assigned verification voltage corresponding to the corrected bit for the identified memory cell, the assigned verification voltage corresponding to the read data for the remaining memory cells. The memory device readjusts the data stored in the plurality of memory cells using the assigned verification voltage. Through this, it is possible to increase a retention period of the data of the memory device.



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PCT/KR 2009/002530

## A. CLASSIFICATION OF SUBJECT MATTER

IPC<sup>8</sup>: **G11C 16/04** (2006.01); **G11C 16/06** (2006.01); **G06F 7/32** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC<sup>8</sup>: G11C 16/04; G11C 16/06; G06F 7/32

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, WPODOC

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages              | Relevant to claim No. |
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| A         | US 5936890 A (Yeom) 10 August 1999 (10.08.1999)<br><i>Abstract; claim 1</i>                     | 1                     |

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Information on patent family members

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