



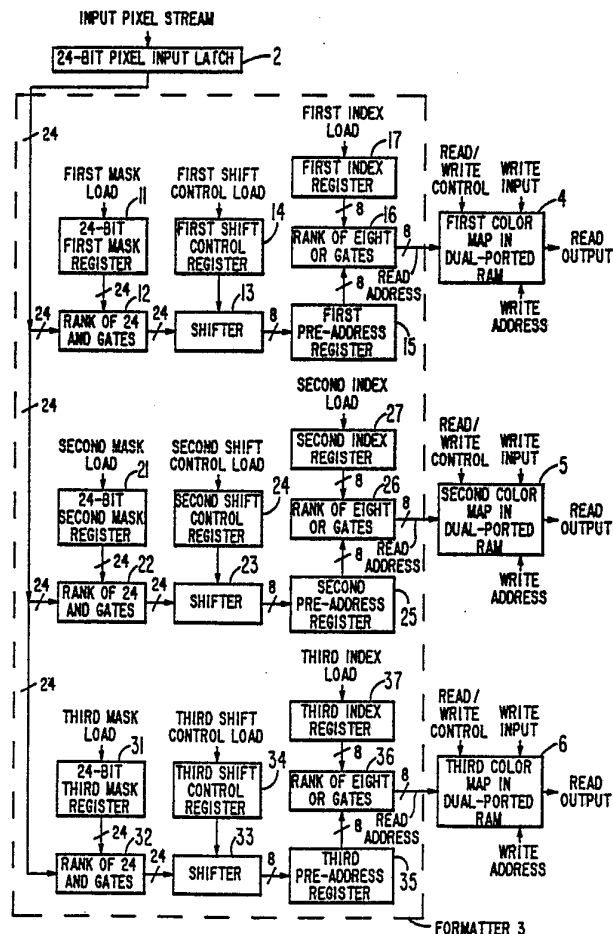
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(54) Title: A DISPLAY PROCESSOR

(57) Abstract

A display processor, as for a small computer, processes pixel codes of various lengths. Three addressable color maps have their read addresses generated independently from portions of each pixel code. The portions of each pixel code used in generating each read address can be selected by programming.



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A DISPLAY PROCESSOR

The present invention relates to improved display processors as may be used in developing computer-generated displays.

5 The graphic images used in computer-generated displays have been stored in image memories at address locations mapping respective points at regular intervals along the raster scanning of a display image space. Each addressed location in image memory has contained a digital
10 word, at least a portion of which has encoded the brightness, hue and saturation of a color pixel at the corresponding point in image space (and, in run-length encoding schemes, the value of succeeding pixels). A number of different schemes for encoding the brightness,
15 hue and saturation of color pixels exist in the prior art.

 One may analyze each color pixel as the sum of the three additive primary colors, red, green and blue, for example. The amplitudes of the red, green and blue components may each be coded in a number n of bits, n
20 normally being in the range five to eight inclusive. Coding may be linear, logarithmic, or in accordance with some other function. It is also known to linearly encode red, green and blue in different numbers p , q and r of bits depending on their relative contributions to luminance.
25 Encoding green in seven bits, red in five bits and blue in four bits is an example of such coding. The reader is referred to M. F. Cowlshaw's paper "Fundamental Requirements for Picture Presentation" appearing on pages 101-107 of PROCEEDINGS OF THE SID, Vol. 26/2, 1985, for a
30 comprehensive treatment of coding additive primary colors in differing numbers of bits.

 One may analyze each color pixel as the sum of a luminance-only primary color and two chrominance-only primary colors. The luminance-only primary represents
35 whiteness or brightness of the pixel. The chrominance-only primaries do not correspond with any real color, but together are representative of the difference of any real

color from the luminance-only primary. The number of bits in these chrominance-only primaries normally differ little from the number of bits in the luminance-only primary, in order to avoid quantization errors in the summation of the primaries. Fewer number of bits in the chrominance-only primaries may give rise to degradation in the display.

One may arbitrarily code color values as addresses for memories, referred to as a color map memories. The memories respond to these addresses to supply, as read output, drive signals to the color display device that cause the desired color to be displayed. The memories, though operated as a read-only memories, may have provisions for changing the color maps they store. To facilitate changing the color maps these memories may be electrically-erasable programmable read-only memories or they may be random-access memories.

It is desirable in a computer display system to provide interchangeability among these various modes of image handling, so that composite displays comprising both computer-generated and camera-originated images as components may be created. A problem encountered in attempting to make such an image display processor is that pixels in camera-originated images of high quality are described by codes up to twenty-four bits long, which pixel codes are substantially longer codes in terms of bits than those normally used to describe the pixels of a graphics image in a computer-generated display.

A display processor embodying the invention uses first, second and third color map memories. The display is generated from the three primary colors that the outputs of these three color map memories respectively supply. Pixel data are encoded in several-bit word per pixel format, the several bits being provided by augmenting with ZEROS any pixel data originally encoded in fewer-bit-word per pixel format. Addressing for the first color map memory is generated from a first selected portion of each several-bit word. Addressing for the second color map memory is generated from a second selected portion of each

several-bit word. Addressing for the third color map is generated from a third selected portion of each several-bit word. Provision is made for allowing, at least part of the time, one of the first, second and third selected portions of each several-bit word to differ from the others.

In the drawings:

FIGURES 1, 2 and 3 are block diagrams of embodiments of a display processor including the invention.

FIGURES 4, 5 and 6 are diagrams illustrating pixel data formatting schemes possible in the FIGURE 2 display processor.

FIGURES 7, 8, 9 and 10 are diagrams illustrating pixel data formatting schemes possible in the FIGURE 3 display processor.

FIGURES 11 and 12 are block diagrams of modified display processors, also including the invention.

FIGURE 13 is a block diagram of two display processors of the type in FIGURE 1, 2, 3, 11 or 12 arranged to be operated in parallel or in banked operation.

FIGURE 14 is a block schematic of display apparatus which may be used with the display processor of FIGURES 1, 2, 3, 11 or 12.

The FIGURE 1 display processor can be used together with a data storage system using disks or tape, a digital random-access memory (RAM), a general data processor, a drawing processor, and a display device to form a small computer with graphics capability. The drawing processor processes graphics information supplied by the data storage system and writes image data into portions of the RAM allocated to image storage, to be stored in a format convenient for the display processor to utilize. The image data are stored in the RAM in bit-map-organization; i.e., for each component of the description of a picture element (pixel) in the image displayed by the display device, there is a respective storage location in memory. During the read of the image storing portions of the RAM, these storage locations are

addressed in raster scan order in synchronism with scanning of the display device screen, to supply pixel data to the display processor. The RAM in addition to storing graphics information may also store data for processing in the
5 general data processor. The RAM may also store operating instructions for the general data processor, for the drawing processor, and/or for the FIGURE 1 display processor. Several purpose usage of RAM is common in a small computer, and this RAM shall hereinafter be called
10 "computer main memory".

In the FIGURE 1 display processor an input latch
2 receives successive words, each descriptive of a pixel. These words can be selected from pixel data supplied from computer main memory, which is bit-map-organized with
15 respect to stored images. A favored computer main memory architecture is one using video dynamic random-access memory (VRAM) integrated circuits. Such a circuit is dual-ported, having a random-access input/output port like
20 a conventional dynamic random-access memory, but also having an additional serial output port. This serial output port is at the end of a shift register that can be side-loaded with a complete line of video samples in the time required for a normal random access. The shift
25 register when loaded can be clocked at high rate to deliver the line of video samples at rates much higher than attainable by normal random access.

The computer main memory output port may be thirty-two bits wide, for example. The breaking up into individual words descriptive of respective pixels is
30 carried out in pixel unwrapping circuitry (not shown in FIGURE 1). This breaking up is in accordance with instructions appropriate to the type of pixel descriptions used for storing pixel data. The largest pixel
35 descriptions will contain twenty-four bits, one byte width for each of three primary color components of a pixel. Accordingly, input latch 2 is provided with twenty-four bit places of storage. If there are fewer than twenty-four bits in a word descriptive of a respective pixel that is

supplied to input latch 2, the remaining bit places are loaded as ZEROS.

The twenty-four bit word held in latch 2 is the input for a formatter 3 that generates read addresses for a first color map memory 4, a second color map memory 5 and a third color map memory 6. The color map memories 4, 5, 6 supply respective color component signals, which can be applied to display apparatus (not shown) used for reconstructing a color image on a screen. The color maps are preferably RAMs operated as read-only memories (ROMs), so that they can be loaded with any desired color map data by down-loading from the computer main memory. It is convenient to do this down-loading during the field retrace intervals in the video signal samples color map memories 4, 5 and 6 deliver to the display apparatus. Supposing the computer main memory uses VRAMs, down-loading from the serial output port of that memory can be done at so high a rate that it is practical to down-load during line trace interval, as well. Assuming, for example, that the computer main memory has a serial output port thirty-two bits wide, eight bits of that output can be used to address the color map memories 4, 5 and 6 during their writing. The other twenty four bits can be apportioned into byte-width groups respectively applied to color map memories 4, 5 and 6 as write inputs.

Color map memories 4, 5 and 6 are shown as being dual-ported in the sense of having separate read output and write inputs, but multiplexing arrangements may be made so that RAMs having a single input/output bus may be used instead. Color map memories are shown as having separate read addresses and write address inputs, but there may be arrangements for multiplexing both sets of addresses through the same address bus in each of the color map memories 4, 5 and 6. The contents of registers in the formatter 3 may be programmed by down-loading from the random access input/output port of computer main memory. Or, the multiplexing of computer main memory read-out through its serial output port may be made more

complicated, so these registers can be programmed from that read-out.

The first, second and third color map memories 4, 5 and 6 may store values of green, red and blue drive signals, respectively, for direct application to the color display device. This permits the number of bits in the outputs of the three color map memories to be apportioned in accordance with the contributions of the three additive primaries to luminance. Green values may be stored with two bits more resolution than red values and with three bits more resolution than blue values, for example. This tends to apportion total color map memory capability to provide better overall apparent resolution in the color display.

Where the computer generally handles graphic images and seldom or never has to process camera-originated images making the color map memories 4, 5 and 6 store red, green and blue display-device drive signals is a likely design choice. This is because these additive primaries are always positive-valued and are truly independent variables, so image calculations can be more simply made. Also most display apparatus ultimately requires red, green and blue drive signals.

But where the computer often is called upon to handle camera-originated images, the drawing processor is likely to receive pixel data in terms of luminance-only information with full spatial resolution and chrominance-only information with reduced spatial resolution. That is, in the original digitized camera responses, luminance is sampled at full density in both horizontal and vertical directions in display image, while chrominance is subsampled at sparser density in at least one of these directions and preferably in both of them. The drawing processor is simplified by storing images in the computer main memory in terms of a luminance-only variable and chrominance-only variables.

To implement pixel data in such formats being routed through formatter 3 to generate read addressing for

color map memories 4, 5 and 6, it is desirable to make one of these memories store a luminance-only variable and be addressable in a luminance-only coordinate system; and it is further desirable to make each of the other two memories to store respective ones of two chrominance-only variables and be addressable in a chrominance-only coordinate system. This chrominance-only coordinate system may consist of two orthogonal chrominance-only component coordinates descriptive of respective chrominance-only primary colors, for example. Or it may consist of a set of arbitrary chrominance codes, as another example. The second color map memory 5 stores values of the luminance-only primary color. The first and third color map memories 4 and 6 store values of a first chrominance-only primary color and values of a second chrominance-only primary color, respectively. The values of these primary colors as read from color map memories 4, 5 and 6 are then matrixed (in circuitry not shown in FIGURE 1) to generate red, blue and green drive signals for the color display device.

In order to combine the chrominance-only signals with the luminance-only signal they must be restored to full spatial resolution by interpolation. Spatial interpolation can be carried forward successfully only when pixels are described in terms of primary color components. If any of the color map memories 4, 5 and 6 can be addressed in other terms (such as arbitrary chrominance codes, for example) interpolation should be among color map memory read-outs, rather than among their read addresses.

Assuming spatial interpolation is to be done in two dimensions (i.e., in both the horizontal and vertical directions), it is best arranged for as follows. A rate-buffering memory (not shown in FIGURE 1) is provided between computer main memory and pixel input latch 2, which rate-buffering memory supplies on a time-interleaved basis, during any line trace interval, the color map memory read addresses associated with two adjacent lines of pixels. These successive read addresses are temporarily stored in those bit positions of pixel input latch 2 that are

associated with the chrominance-only coordinates used to address color map memories 5 and 6. This arrangement for four successive read-outs of the color map memories 5 and 6 to define the sets of four closely grouped subsamples needed for two-dimensional (e.g., bilinear) spatial interpolation. Spatial interpolation circuitry (not shown in FIGURE 1) brings the four subsamples into temporal alignment, and they are weighted according to the position the full-density sample resulting from interpolation is to have in the image field respective to the positions of the subsamples. Differential delay between the luminance-only primary color samples (on one hand) and the chrominance-only primary color samples obtained by interpolation (on the other hand) are compensated for. It is usually best to provide this compensation in the rate-buffering memory located between computer main memory and the pixel input latch 2 of the formatter.

A preferred arrangement is to load the rate-buffering memory with chrominance-only information downloaded during line retrace intervals from the serial output ports of VRAMs serving as computer main memory, so the serial output ports are free to supply only luminance-only information during line trace intervals. In embodiments of the invention wherein ones of the color map memories 4, 5 and 6 are re-written by data also downloaded from the serial output ports of these VRAMs during line retrace intervals, there will be competition for the limited time available during line retrace intervals, a fact which a designer must take into account.

If there is to be interpolation of the chrominance-only primary colors read from color map memories 4 and 6, the independent addressing of color map memories 4 and 6 from color map memory 5 (used as a luminance map) is required. This because the sampling pattern of read addresses supplied color map memories 4 and 6 differs from the sampling pattern of read addresses supplied to color map memory 5.

Consider now the construction of formatter 3. Formatter 3 is used to generate read addresses for color map memories 4, 5 and 6 from the pixel data held in input latch 2. Respective portions of this pixel data are
5 selected as bases for generating these read addresses, selection being made in accordance with first, second and third masks for the twenty-four bits of this data.

A first twenty-four bit mask has a group of contiguous ONES identifying positions in latch 2 output to
10 be selected as a basis for generating first color map memory 4 read address, has ZEROS identifying positions in latch 2 output not to be so selected, and has been previously loaded into a mask register 11 from computer main memory under direction of the data processor. The
15 bit-places in mask register 11 output are respective first inputs to a rank 12 of twenty-four AND gates, the respective second inputs of which are respective bit places of the output from input latch 2. The output of the rank 12 of AND gates is ZERO-valued in all its places
20 corresponding to ZEROS in the first mask output of mask register 11. The remaining bit places in the output of the rank 12 of AND gates are a first selected portion of input latch 2 output. The output of the rank 12 of AND gates is supplied as input to a shifter 13 which will justify the
25 first selected portion of latch 2 output.

Shifter 13 performs a barrel-shift function wherein the twenty-four bits supplied as output from the rank 12 of AND gates are shifted in one of two ways. The bits in the twenty-four bit places of shifter 13 output
30 could be shifted towards increased significance with any overflow bit being shifted into the vacated least significant bit place, or the bits in the twenty-four bit places of shifter 13 output could be shifted towards decreased significance with any underflow bit being shifted
35 into the vacated most significant bit place. Either direction of shifts can achieve the same result given enough bit places of shift, so shifter 13 is more simply constructed if it invariably shifts in one direction. The

number of bit places of shift in the selected direction can then be programmably specified by a positive binary number previously loaded into a first shift control register 14 and stored there until register 14 contents are up-dated.

5 As each pixel is scanned, a first pre-address register 15 is loaded from eight of the bit places of shifter 13 output, which bit places contain the first selected portion of latch 2 output passing through the first mask. Shifter 13 customarily justifies this first
10 selected portion of latch 2 output, either so its most significant bit is in the most significant of the eight-bit places of shifter 13 output which loads first pre-address register 15, or so its least significant bit is in the least significant of these eight-bit places of shifter 13
15 output. Pre-address register 15 stores the first selected portion of latch 2 output and applies respective ones of its bit places as respective first inputs to a rank 16 of OR gates. OR gates in rank 16 receive as their respective second inputs respective ones of the bit places of a first
20 index supplied from a first index register 17. The first index has previously been loaded from computer main memory. The output of the rank 16 of OR gates is the read address for first color map memory 4.

 The read addresses for second color map memory 5
25 are generated by elements 21-27 in a similar manner to the read addresses for first color map memory generated by elements 11-17. The read addresses for third color map memory 6 are generated by elements 31-37 in a similar manner to the read addresses for first color map memory
30 being generated by elements 11-17.

 It is convenient to make the shifters 13, 23 and 33, in the following way so that they shift in accordance with a binary number control signal. Each of the shifters 13, 23 and 33 is a cascade connection of a number of
35 component shifters. A first component shifter has a respective multiplexer selecting between no shift and one-bit place shift responsive to the least significant bit of counter output being ZERO and being ONE respectively. A

second component shifter has a respective multiplexer selecting between no shift and two-bit places shift responsive to the second last significant bit of counter output being ZERO and being ONE respectively. Any k^{th} one
5 of the component shifters, that is, has a respective multiplexer selecting between no shift and 2^k -bit-places shift responsive to the k^{th} -least significant bit of counter output being ZERO and being ONE, respectively. The
10 total shift available from any of the shifters 13, 23 and 33 is then the sum of the bit places of shift of its cascaded component shifters. In the remaining portion of this specification it will be assumed that shifters 13, 23 and 33 shift in the direction of increased significance as the binary numbers used as their respective control signals
15 are incremented in value.

Modifications may be made to the FIGURE 1 display processor formatter 3 so that its programming can be simplified. If one is willing to justify the input to the pre-address registers 15, 25 and 35 always in the same
20 direction, the justifications can be performed automatically using the information stored in the mask registers. This avoids the need for programming to load first, second and third shift control data into shift control registers 14, 24 and 34. FIGURE 2 display
25 processor formatter 7 is such a modification wherein automatic pre-address justification, if required, is always in the direction of increased significance. FIGURE 3 display processor formatter 8 is such a modification wherein automatic pre-address justification, if required,
30 is always in the direction of decreased significance. After describing the structure of the FIGURE 2 and FIGURE 3 display processor formatters 7 and 8 in more detail, the justification procedures will be described in more detail based on operation in formatters 7 and 8. These
35 descriptions will make apparent the operation possible in the FIGURE 1 display processor, since formatter 3 is capable of simulating any operation that is possible in either of formatters 7 and 8.

In the FIGURE 2 display processor, data which completely describe a pixel in less than twenty-four bits are loaded into input latch 2 so that they occupy the most significant bit places in its output. Any remaining less significant bit places in latch 2 output are preferably filled with ZEROs. Data which completely describe a pixel in exactly twenty-four bits are loaded into pixel input latch 2 without using ZERO insertion.

The pixel data on which first color map memory 4 read addresses are to be based are constrained invariably to be grouped in the eight most significant bits of latch 2 output. The first selected portion of latch 2 output is constrained to be no more than eight bits wide. This allows the mask register 11 (of FIGURE 1) with twenty-four bit places storage to be replaced by a mask register 38 with only eight bit places storage. This also allows the rank 12 of twenty-four AND gates (of FIGURE 1) to be replaced by a rank 39 of only eight AND gates for selecting the first portion of latch 2 output. No shifter is required for aligning the output of the rank 39 of AND gates with pre-address register 15 input.

The pixel data on which second color map memory 5 read addresses are to be based are constrained invariably to be grouped in the sixteen most significant bits of latch 2 output. The second selected portion of latch 2 output is constrained to be no more than eight bits wide, but this byte-width need not coincide with nor overlap the byte-width allocated for pixel data on which read addresses of first color map memory 4 are based. Mask register 41 with only sixteen bit places storage suffices to store the second mask, then, and replaces the wider mask register 21 (of FIGURE 1). A rank 42 of only sixteen AND gates replaces the rank 22 of twenty-four AND gates (of FIGURE 1).

A shifter 43 with only 16-bit input capacity replaces shifter 23 (of FIGURE 1) with 24-bit input capacity. The justification is to be made so shifter 43 will barrel-shift that second selected portion of latch 2

output to the most significant bit places for loading pre-address register 25. In a barrel-shift in the direction towards increased significance, the less significant bits of a number with a fixed number of bit places are shifted towards increased significance, with the overflowing more significant bits being inserted into the vacated less significant bit places. The number of bit places involved in the barrel-shift that shifter 43 provided is specified by the count output of a clocked counter 44, which count output also specifies the number of bit places another shifter 45 barrel-shifts towards more significance in its output the first mask it receives as input from first mask register 41. The most-significant bit place of shifter 45 is applied to a detector 46 to generate a shift signal if that bitplace be ZERO, which shift signal is transmitted as count input to counter 44. More particularly, detector 46 may comprise a simple bit complementor, with the clocking of counter 44 sampling the complementor output. The second pre-address register 25 is loaded from the eight most significant bit places of shifter 43 output, with justification of the second selected portion of latch 2 pixel data being in the direction of increased significance.

The pixel data on which third color map memory 6 read addresses are to be based can be grouped anywhere in the twenty-four bits of input latch 2. The third selected portion of latch 2 output is selected by the rank 32 of twenty-four AND gates responsive to a third mask stored in the mask register 31, just as in the formatter 3 of the FIGURE 1 display processor. The third selected portion of latch 2 output is justified in the direction of increased significance by the shifter 33 in formatter 7, just as in formatter 3 (of FIGURE 1). But in formatter 7 of the FIGURE 2 display processor the number of bit places of shift through shifter 33 is specified by the count stored in counter 47. This count also specifies the number of bits by which the third mask content of register 31 is shifted in the output of a shifter 48, similar to shifter

33. Shifters 33 and 48 shift towards increased significance in their outputs as the count in counter 47 is augmented. The most significant bit of shifter 48 output is applied to a detector 49 to generate a shift signal if that bit place be ZERO, which shift signal is transmitted as count input to counter 47. The third pre-address register 35 is loaded from the eight most significant bit places of shifter 33 output, with justification of the third selected portion of latch 2 pixel data being in the direction of increased significance.

In formatter 8 of the FIGURE 3 display processor the justifications of the first, second and third pre-addresses loaded into registers 15, 25 and 35 is automatic and is invariably in the direction of decreasing significance, rather than increasing significance as was the case in the formatter 7 of the FIGURE 2 display processor. In the FIGURE 3 data processor, data which completely describe a pixel in less than twenty-four bits are loaded into input latch 2 so that they occupy the least significant places in its output. Any remaining more significant bit places in input latch 2 output are preferably filled with ZEROS. As before, data which completely describe a pixel in exactly twenty-four bits are loaded into pixel input latch 2 without using ZERO insertion. The differences formatter 8 in FIGURE 3 has from formatter 7 in FIGURE 2 will now be described.

The pixel data on which first color map memory 4 read addresses are to be based are constrained invariably to be grouped in the eight least significant bit places of input latch 2 output. The pixel data on which second color map memory 5 read addresses are to be based are constrained to be grouped in the sixteen least significant bit places of input latch 2 output.

The outputs of shifters 43' and 45' shift another bit place towards decreased significance responsive to the count contained in counter 44 being augmented. The count in counter 44 is augmented when a detector 28 detects a ZERO in the least significant bit place of shifter 45'

output. The eight least significant bit places of shifter 43' output load the second pre-addresses into register 25.

The outputs of shifters 33' and 48' shift another bit place towards decreased significance responsive to the count contained in counter 47 being augmented. The count in counter 47 is augmented when a detector 29 detects a ZERO in the least significant bit place of shifter 48' output. The eight least significant bit places of shifter 33' output load the third pre-addresses into register 35.

10 Consider now how different pixel data formats are accommodated by the FIGURE 2 formatter 7; these considerations will also educate the reader concerning how the more flexible FIGURE 1 formatter 3 may be employed. FIGURES 4-6 abstract the FIGURE 2 block diagram to indicate the nature of the pixel data contained in input pixel data latch 2; in mask registers 38, 41 and 31; and in pre-address registers 15, 25 and 35. In considering FIGURES 4-6 assume the first, second and third indices to be zero-valued, so the contents of the pre-address registers 15, 25 and 35 correspond to the read addresses of color map memories 4, 5 and 6 respectively.

FIGURE 4 shows how pixel data flows from latch 2 to pre-address registers 15, 25 and 35 in formatter 7 when 8-bit red (R), 8-bit green (G), 8-bit blue (B) pixel descriptions, for example, are used in computer main memory. Alternatively, FIGURE 4 may be considered to show how pixel data flows from latch 2 to pre-address registers 15, 25 and 35 when 8-bit Y, 8-bit (R-Y), 8-bit (B-Y) or 8-bit Y, 8-bit I, 8-bit Q pixel descriptions are used. (Y is luminance-only primary; (R-Y) and (B-Y) or I and Q are first and second chrominance-only primaries.) The three-byte pixel data input latch 2 is filled with a 24-bit number ABCD EFGH JKLM NPQR STUV WXYZ where each letter represents either a ONE or ZERO. The eight-bit first mask (as stored in mask register 38) is all ONES; and ABCD EFGH, the initial eight bits of latch 2 content, are selected by AND gates in rank 39 for insertion into first pre-address register 15. The sixteen-bit second mask (as stored in

mask register 41) is eight ZEROS in its more significant places followed by eight ONES in its less significant places. JKLM NPQR, the middle eight bits of latch 2 content, are selected by AND gates in rank 42, are shifted
5 by shifter 43, and are inserted into second pre-address register 25. The twenty-four bit third mask (as stored in mask register 31) is sixteen ZEROS in its more significant places followed by eight ONES in its less significant places. STUV WXYZ, the eight least significant bits of
10 latch 2 content, are selected by AND gates in rank 32, are shifted by shifter 33, and are inserted into third pre-address register 35.

In this mode of operation the first, second and third indices are zero-valued; and each of the color map
15 memories 4, 5, 6 may store in its storage locations output signals equal to the read addresses for those storage locations. This in effect forwards the contents of the pre-address registers 15, 25 and 35 as drive signals to the display device. Alternatively, each of the first, second
20 and third indices are zero-valued; and the color map memories may be programmed to provide non-linear response to the contents of pre-address registers 15, 25 and 35. This procedure can be used to remove unwanted gamma correction from broadcast television images, for example,
25 to suit the images for display on a computer monitor designed to use non-gamma-corrected video, as is common in digital graphics images. In Y,I,Q operation non-linear responses from the color map memories 4, 5, 6 may be used to provide better rendition in pastels in
30 computer-originated images by allowing resolution of the chrominance-only primaries to be higher near white than for saturated red, green or blue. The independent addressing of color map memories 4, 5, 6 is what permits them to be used to provide, at the computer programmer's option,
35 linear or non-linear processing of the component video signals descriptive of camera-originated images or images simulating them. The independent addressing of memories 4, 5, 6 enables them to function for these purposes in

addition to performing the more conventional color mapping chores associated with graphic image handling. The independent addressing of color map memories 4, 5 and 6 also facilitates the generation of false-color presentations.

FIGURE 5 shows another way for pixel data to flow from input pixel data latch 2 to pre-address registers 15, 25 and 35 in formatter 7. The pixel data in latch 2 is sixteen-bit pixel data, to conserve computer main memory, and has been padded with eight succeeding ZEROS prior to being entered into latch 2. These two bytes of pixel data comprise four bits ABCD of blue primary, five bits JKLMN of red primary and seven bits STUVWXY of green primary.

The eight-bit first mask (as stored in mask register 38 has four ONES as most significant bits to select blue information followed by four ZEROS as less significant bits to mask red information. Accordingly, the four most significant bits ABCD of latch 2 contents are selected by AND gates in rank 39 for insertion into first pre-address register 15 as more significant bits succeeded by four ZERO less significant bits.

The sixteen-bit second mask (stored in mask register 41) has four ZEROS as most significant bits for masking blue information, followed by five ONES for selecting red information, followed by seven ZEROS for masking green information. Shifter 43 justifies the 0000 JKLM N000 0000 red information response at the outputs of rank 42 of AND gates to JKLM N000 0000 0000; and the first eight bits, JKLM N000, of shifter 43 output are inserted into second pre-address register 25.

The twenty-four bit third mask (as stored in mask register 31) has nine ZEROS as most significant bits to mask blue and red information, followed by seven ONES for selecting green information, followed by any eight bits, shown as ZEROS. Shifter 33 justifies the 0000 0000 OSTU VWXY 0000 0000 green information response at the outputs of rank 32 of AND gates to STUV WXYO 0000 0000 0000 0000; and

the initial eight bits, STUV WXYO, of shifter 33 output are inserted into third pre-address register 35.

Organizing the pixel data in input latch 2 with the four bits of blue information first, the five bits of red information second and the seven bits of green information last minimizes the number of shift signals to be generated to justify the data loaded into pre-address registers 15, 25 and 35. This shortens the time required to re-program the formatter 7.

FIGURE 6 illustrates how formatter 7 can handle pixel data coded in color map addresses. Six-bit color map read addresses AB CDEF encode 2^6 colors, each color having a unique combination of hue, color saturation and luminance. These six-bit color map read addresses are padded with eighteen less significant bits in pixel latch 2. If these eighteen less significant bits are ZEROs, whether the two least significant bits of the first mask, the ten least significant bits of the second mask and the eighteen least significant bits of the third mask are ONES or ZEROs is of consequence only if pixel input latch 2 is called upon to perform pixel-grabbing, a function to be considered further on in the specification. Alternatively, if the two least significant bits in the first mask are ZEROs, if the ten least significant bits in the second mask are ZEROs and if the eighteen least significant bits in the third mask are ZEROs, whether the eighteen least significant bits of latch 2 contents are ONES or ZEROs is of no consequence. At least one of these alternative conditions should be satisfied; the presence of both is indicated in FIGURE 6.

The first mask (as stored in mask register 38) has six ONES as more significant bits and two ZEROs as less significant bits, so the rank 39 of AND gates supplies ABCD EF00 as input for pre-address register 15. The second mask (as stored in mask register 41) has six ONES as more significant bits and ten ZEROs as less significant bits, so the rank 42 of AND gates supplies ABCD EF00 0000 0000 as input to shifter 43. Since the second mask has a ONE in

its most significant place, this input requires no justification to form shifter 43 output; and pre-address register 25 is loaded with its eight most significant bits, ABCD EF00. The third mask (as stored in mask register 31) has six ONES as more significant bits followed by eighteen ZEROS, so the rank 32 of AND gates supplies ABCD EF00 0000 0000 0000 0000 as input to shifter 33. Again justification is not required and shifter 33 loads pre-address register 35 with ABCD EF00. The color map memories 4, 5 and 6 are loaded with color map data for operating with the read addresses per FIGURE 6; this will be illustrative of the general process for loading these memories with color map data. The 2^6 color map addresses possible with six-bit pixel data codes are sequentially generated as write addresses for color map RAMs 4, 5, 6 and the respective primary color component drive signals to the display device to be associated with that address are written into the RAMs at suitable times. This can always be done prior to the FIGURE 2 display processor processing display or during field retrace interval. Where computer main memory uses VRAMs permitting rapid down-loading to rewrite RAMs 4, 5 and 6, these color map memories can be rewritten in whole or in substantial part during a line retrace interval, as well. If RAMs 4, 5, 6 are dual-ported, updating of the color maps these RAMs contain can be done piecemeal during line trace intervals, too.

Eight-bit color map read addresses may be used as pixel data to encode 2^8 colors, or a fewer number m of bits may be used as pixel data to encode 2^m colors, assuming the same color map read addresses are applied to each of the RAMs 4, 5, 6. This is similar to prior art color mapping practice. However, since the color map memories are independently addressed, three eight-bit color map read addresses permit $2^8 \times 2^8 \times 2^8$ or 2^{24} different colors to be mapped. Where the read addresses are p -bits, q -bits and r -bits long, respectively, $2^{(p+q+r)}$ colors can be mapped. Where $p=q=r=m$, 2^{3m} colors can be mapped, 2^{2m} times as many as in prior art color mapping practice where the three

color maps all receive the same read address. However, all of these extra colors may not be truly useful, because they have large chrominance values without correspondingly large luminance values.

5 Consider now how different pixel formats are accommodated by the FIGURE 3 formatter 8. The FIGURE 1 of formatter 3 not only can be operated to simulate the performance of the FIGURE 2 formatter 7, but also can be operated to simulate the performance of the FIGURE 3
10 formatter 8 now to be described. FIGURES 7-10 abstract the FIGURE 3 block schematic diagram to indicate the nature of the pixel data contained in input pixel data latch 2; in mask registers 38, 41 and 31; and in pre-address registers 15, 25 and 35. In considering FIGURES 7-9 assume the
15 first, second and third indices to be zero-valued, so the contents of the pre-address registers 15, 25 and 35 correspond to the read addresses of color map memories 4, 5 and 6 respectively. FIGURE 10 also indicates the nature of the indices stored in index registers 17, 27 and 37 and the
20 nature of the read addresses applied to color map memories 4, 5 and 6 from the output connections of the ranks 16, 26 and 36 of OR gates.

 FIGURE 7 shows how pixel data flows from latch 2 to pre-address registers 15, 25 and 35 in formatter 8 when
25 8-bit red, 8-bit green, 8-bit blue pixel descriptions, for example, are used in computer main memory. The same type of pixel data flow occurs when 8-bit Y, 8-bit I, 8-bit Q or 8-bit Y, 8-bit (R-Y), 8-bit (B-Y) pixel descriptions are used in computer main memory.

30 The three-byte pixel data input latch 2 is filled with a 24-bit number STUV WXYZ JKLM NPQR ABCD EFGH where each letter represents either a ONE or ZERO. The eight-bit first mask (as stored in mask register 38) is all ONES; and ABCD EFGH, the lesser significant eight bits of latch 2
35 content, are selected by AND gates in rank 39 for insertion into first pre-address register 15. The sixteen-bit second mask (as stored in mask register 41) is eight ONES in its more significant places followed by eight ZEROS in its less

significant places. JKLM NPQR, the middle eight bits of latch 2 content, are selected by AND gates in rank 42, are shifted by shifter 43', and are inserted into second pre-address register 25. The twenty-four bit third mask
5 (as stored in mask register 31) has eight ONES in its more significant places followed by sixteen ZEROS in its less significant places. STUV WXYZ, the eight most significant bits of latch 2 content, are selected by AND gates in rank 32, are shifted by shifter 33', and are inserted into third
10 pre-address register 35.

In this mode of operation the first, second and third indices are zero-valued; and each of the color map memories 4, 5, 6 may store in its storage locations output signals equal to the read addresses for those storage
15 locations. This in effect forwards the contents of the pre-address registers 15, 25 and 35 as drive signals to the display device. Alternatively, each of the first, second and third indices are zero-valued; and the color map memories may be programmed to provide non-linear response
20 to the contents of pre-address registers 15, 25 and 35.

FIGURE 8 shows another way for pixel data to flow from input pixel data latch 2 to pre-address registers 15, 25 and 35 in formatter 8. The pixel data in latch 2 is sixteen-bit pixel data, to conserve computer main memory,
25 and has been padded with eight preceding ZEROS prior to being entered into latch 2. These two bytes of pixel data comprise seven bits STUVWXY of green primary, five bits JKLMN of red primary and four bits ABCD of blue primary.

The eight-bit first mask (as stored in mask
30 register 38) has four ZEROS as most significant bits to mask red information followed by four ONES as least significant bits to select blue information. Accordingly, the four least significant bits ABCD of latch 2 contents are selected by AND gates in rank 39 for insertion into
35 first pre-address register 15 as least significant bits preceded by four ZERO more significant bits.

The sixteen-bit second mask (stored in mask register 41) has seven ZEROS as most significant bits for

masking green information, followed by five ONES for selecting red information, followed by four ZEROS for masking blue information. Shifter 43' justifies the 0000 000J KLMN 0000 red information response at the outputs
5 of rank 42 of AND gates to 0000 0000 000J KLMN and the final eight bits, 000J KLMN, of shifter 43' output are inserted into second pre-address register 25.

The twenty-four bit third mask (as stored in mask register 31) has any eight most significant bits (shown as
10 ZEROS), followed by seven ONES for selecting green information, followed by nine ZEROS to mask red and blue information. Shifter 33' justifies the 0000 0000 STUV WXY0 0000 0000 green information response at the outputs of rank 32 of AND gates to
15 0000 0000 0000 0000 OSTU VWXY; and the final eight bits, OSTU VWXY of shifter 33' output are inserted into third pre-address register 35.

FIGURE 9 illustrates how formatter 8 can handle pixel data coded in color map addresses. Six-bit color map read addresses AB CDEF encode 2^6 colors, each color having
20 a unique combination of hue, color saturation and luminance. These six-bit color map read addresses are padded with eighteen more significant bits in pixel latch 2. If these eighteen more significant bits are ZEROS, whether the two most significant bits of the first mask,
25 the ten most significant bits of the second mask and the eighteen most significant bits of the third mask are ONES or ZEROS is of consequence only if pixel input latch 2 is called upon to perform pixel-grabbing, a function to be
30 considered further on in the specification. Alternatively, if the two most significant bits in the first mask are ZEROS, if the ten most significant bits in the second mask are ZEROS and if the eighteen most significant bits in the third mask are ZEROS, whether the eighteen most significant
35 bits of latch 2 contents are ONES or ZEROS is of no consequence. At least one of these alternative conditions must be satisfied; the presence of both is indicated in FIGURE 9.

The first mask (as stored in mask register 38) has two ZEROS as more significant bits and six ONES as less significant bits, so the rank 39 of AND gates supplies 00AB CDEF as input for pre-address register 15. The second mask (as stored in mask register 41) has ten ZEROS as more significant bits and six ONES as less significant bits, so the rank 42 of AND gates supplies 0000 0000 00AB CDEF as input to shifter 43'. Since the second mask has a ONE in its least significant place, this input requires no justification to form shifter 43' output; and pre-address register 25 is loaded with its eight least significant bits, 00AB CDEF. The third mask (as stored in mask register 31) has eighteen ZEROS as more significant bits followed by six ONES, so the rank 32 of AND gates supplies 0000 0000 0000 0000 00AB CDEF as input to shifter 33'. Again justification is not required and shifter 33' loads pre-address register 35 with 00AB CDEF.

The formatter 3 of FIGURE 1 provides unusual flexibility in handling a plurality of pixel data modes without having to reload the color map RAMs 4, 5 and 6. This facilitates on-the-fly, real-time generation of displays that are composite images using components drawn from separate image sources. Much of this flexibility is retained in each of the formatters 7 and 8 of FIGURES 2 and 3.

Consider composite display imagers wherein: a first component image is described in terms of a linear color code, similar to that customarily used with camera-originated image processing, which code lends itself to supplying independent read addresses to RAMs 4, 5, 6; and a second component image is a graphics image described in terms of another, arbitrary color code, which requires supplying read addresses in parallel to RAMs 4, 5, 6. When going from one pixel data format to the other, the first, second and third masks are re-loaded into the mask registers 11, 21, 31 or 38, 41, 31. But additionally the first, second and third indices are re-loaded into index registers 17, 27 and 37 to address different portions of

the RAMs 4, 5 and 6 than were addressed for the other component image.

For example, consider the formatter 7 of FIGURE 2 operated so the first component image uses the sixteen-bit pixel code format described in conjunction with FIGURE 5 and the second component image uses the six-bit pixel code format described in conjunction with FIGURE 6. Neither set of codes results in a pre-address that has a ONE as its least significant bit. So all the pre-addresses that can be generated by either one of the coding schemes cannot claim more than half the storage locations available in each of the RAMs 4, 5, 6. This means that the respective color map information of each coding scheme can be multiplexed into the RAMs.

A first half of the locations in the respective RAMs 4, 5, and 6 are allocated to storing the linear pixel code information, as described in conjunction with FIGURE 5. These locations all have addresses in which the least significant bit is a ZERO. A second half of the locations in the respective RAMs 4, 5 and 6 are allocated to storing the arbitrarily coded color mapping information, as described in conjunction with FIGURE 6. The locations all have addresses in which the least significant bit is a ONE.

When the input pixel stream consists of pixels representing the first component image, which uses the sixteen-bit pixel code format described in conjunction with FIGURE 5, then the pre-addresses in registers 15, 25 and 35 may be applied without modification as read addresses to RAMs 4, 5 and 6 for reading locations storing color pixel data in terms of a linear pixel code. The least significant bit of the read address is, thus, a ZERO, thereby addressing the first half of the RAM locations. This is done responsive to the first, second and third indices in index registers 17, 27 and 37 each being ZERO in all bit places.

When the input pixel stream consists of pixels representing the second component image, which uses the six-bit arbitrarily coded format described in conjunction

with FIGURE 6, then the pre-addresses in registers 15, 25, and 35 must be modified before being applied as read addresses to RAMs 4, 5 and 6, for reading locations storing color pixel data in terms of color mapping information.

5 The modification, in this case, is to force the least significant bit of the read address to be a ONE, thus, addressing the second half of the RAM locations. The first, second and third indices in index registers 17, 27 and 37 may each be made 0000 0001 to read the second half

10 of the locations in RAMs 4, 5 and 6 when the pixel data is arbitrarily coded. That is, the pre-addresses in registers 15, 25 and 35 are augmented by unity to supply read addresses to RAMs 4, 5 and 6; and in these alternate sets of storage locations the RAMs store the decoding

15 information for the arbitrary color codes in accordance with the color mapping principle.

In actuality, since the two least significant bits of the first, second and third pre-addresses stored in registers 15, 25 and 35 are ZEROS in the FIGURE 6 pixel coding scheme, the pixel coding schemes of FIGURES 5 and 6

20 take up no more than three-fourths of the addressable storage locations in color map memories 4, 5 and 6. An additional pixel coding scheme can be accommodated by using 0000 0011 indices in index registers 17, 27 and 37, as long

25 as this pixel coding scheme involves pre-addresses that have ZEROS as their two least significant bits.

In another example of going from one pixel data format to another, consider the formatter 8 of FIGURE 3 operated so the first component image uses the sixteen-bit

30 pixel code format described in conjunction with FIGURE 8 and the second component image uses the six-bit pixel code format described in conjunction with FIGURE 9. Neither set of codes results in a pre-address that has a ONE as its most significant bit. So all the pre-addresses that can be

35 generated by either one of the coding schemes cannot claim more than half of the storage locations available in each of the RAMs 4, 5, 6. This means that the respective color

map information of each coding scheme can be multiplexed into the RAMs.

Half of the locations in the respective RAMs 4, 5 and 6 are allocated to storing the linear pixel code information, described in conjunction with FIGURE 8, and another half of the locations in the respective RAMs are allocated to storing the arbitrarily coded color mapping information described in conjunction with FIGURE 9. The first half of the RAM locations all have addresses in which the most significant bit is a ZERO, and the second half of the RAM locations all have addresses in which the most significant bit is a ONE. When the input pixel stream consists of pixels representing the first component image, which uses the sixteen-bit pixel code format (FIGURE 8), the the pre-addresses in registers 15, 25 and 35 may be applied without modification as read addresses to RAMs 4, 5 and 6 for reading locations storing the pixel data linearly coding color information. The most significant bit of the read address is, thus, a ZERO, thereby addressing the first half of the RAM locations. This is done responsive to the first, second and third indices in index registers 17, 27 and 37 each being ZERO in all bit places.

When the input pixel stream consists of pixels representing the second component image, which uses the six bit arbitrarily coded pixel format (FIGURE 9), then the pre-addresses in registers 15, 25 and 35 must be modified before being applied as read addresses to RAMs 4, 5 and 6. The modification, in this case, is to force the most significant bit of the read address to be a ONE, thus, addressing the second half of the RAM locations. The first, second and third indices in index registers 17, 27 and 37 can each be made 1000 0000 to read the second half of the locations in RAMs 4, 5 and 6 when the pixel data is arbitrarily coded. An additional pixel coding scheme wherein pre-addresses never have ONES in their most significant and secondmost significant bits can also be employed without having to extend or re-program the color map memories 4, 5 and 6. The first, second and third

indices in index registers 17, 27 and 37 will be 1100 0000 for such an additional pixel coding scheme.

In formatter 8 of the FIGURE 3 display processor the storage locations in color map memories 4, 5 and 6 to serve different sets of pixel codes are allocated in ranges that are integral powers of two in extent. This is the limitation imposed by using ranks 16, 26 and 36 of OR gates to combine the first, second and third indices with the first, second and third pre-addresses. It is possible to allocate portions of the RAM locations into arbitrary ranges. If the ranks 16, 26 and 36 of OR gates are replaced by respective adders, the code ranges may be arbitrarily chosen.

Consider composite display images wherein each component image is camera-originated or consists of linearly coded pixel color components, but where one component image is specified in color coordinates having higher amplitude resolution than those another component image is specified in. The pixel data for these two component images might be coded as in FIGURES 4 and 5 respectively assuming formatter 3 of FIGURE 1 or formatter 7 of FIGURE 2 is being used. Since mask justification and the justifications of pixel data passed through the first, second and third masks are in the direction of more significance, the same functions in color map RAMs 4, 5 and 6 will accommodate the pixel data of either component image. The composite display image can be assembled in real time, on-the-fly. A transition period between component images would appear in the composite image if color map memories 4, 5 and 6 had to be reloaded, presuming the transition did not fall between scan lines in the display.

In the formatter 3 of FIGURE 1, the transition between component images linearly-coded with differing amplitude resolutions requires only first, second and third mask loads to registers 11, 21 and 31 and first, second and third shift control loads to registers 14, 24 and 34. This register loading can proceed much more rapidly than the

re-loading of color map RAMs 4, 5 and 6, especially if the loading procedures are performed at least to a degree parallel in time.

In the formatter 7 of FIGURE 2, the transition
5 between component images linearly coded with differing amplitude resolutions requires only first, second and third mask loads to mask registers 38, 41, 31. Transition in formatter 7 takes the time to load the masks and to perform justifications, a time much shorter than loading RAMs 4, 5,
10 6. Faster justification circuits can make these transitions invisible in display. Alternatively, to increase transition speed, several formatters (such as formatter 7 of FIGURE 2) may be coupled in parallel between the pixel input latch 2 and the color map RAMs 4, 5 and 6
15 and operated in staggered phasing; a technique known as banking. A data processor that utilizes banking, can be operated to make these transitions invisible in the display also, even using the slower justification circuits. The above techniques may also be used in combination.

20 In the formatter 8 of FIGURE 3 the justification of the first, second and third pre-address in the direction of least significance results in two sets of read addresses for each of the RAMs 4, 5 and 6 for pixels from the two different sources. If underlength pixel data are extended
25 by entering ZEROS in the more significant bit places of pixel input latch 2 output, the resulting set of shorter-bit-length read addresses is not a subsampling of the set of longer-bit-length read addresses. So, the color map memories 4, 5 and 6 undesirably have to be re-loaded
30 going from one component image to the other. More complex formatting of the data loaded into pixel input latch 2 can be done to overcome this shortcoming, however.

This shortcoming in a formatter like 8 also can be remedied by providing for color map read addresses that
35 have one bit more resolution than that required to map any video source. The indexing schemes previously described to provide multiplexing in color map memory storage locations can then be employed to avoid the need for color map

reloading when making the transition from one video source to another video source with a differing degree of amplitude resolution in one or more of its components.

The index registers 17, 27 and 37 are shown in
5 FIGURES 1, 2 and 3 as having as many bit places as the pre-address registers 15, 25 and 35; and there is a commensurate number of OR gates in ranks 16, 26 and 36. The FIGURE 2 formatter 7 can be simplified so that the OR gates and the index registers which supply their first
10 inputs may be arranged to process second inputs from only the less significant bit places of the pre-address register 15, 25, 35 outputs. The more significant bit places of the pre-address register 15, 25, 35 outputs may be applied directly to RAMs 4, 5 and 6 as the more significant
15 portions of their read addresses. Simpler indexing arrangements are also possible in the FIGURE 3 formatter 8. The OR gates and the index registers which supply their first inputs may be arranged to process second inputs from only the more significant portions of their read addresses.
20 The less significant bit places of the pre-address registers 15, 25 and 35 are then applied directly to RAMs 4, 5 and 6 as the less significant portions of their read addresses. Reducing the number of OR gates in ranks 16, 26 and 36 in the FIGURE 3 formatter 8, however, interferes
25 with a programming trick, which is very powerful in reducing image memory requirements in computer main memory and is more easily carried out in the FIGURE 2 display processor than in the FIGURE 3 display processor.

FIGURE 10 is helpful in understanding
30 specifically how this programming trick is carried out in the FIGURE 2 display processor. It is desired to describe pixels in terms of eight-bit primary color components, as in the FIGURE 7 case, but to take advantage of the fact that the more significant bits of these primary colors
35 change less frequently than their less significant bits. By way of example, presume that the two most significant bits AB of the first primary color component do not change over a number of successively scanned pixels. Then it is

not necessary to reiterate AB in the pixel codes for this succession of pixels as stored in the image memory portion of the main computer memory. Presume further that the two most significant bits JK of the second primary color component also change relatively infrequently compared to pixel scan rate, so it is unnecessary to reiterate JK at pixel scan rate in the pixel codes: Presume still further that the two most significant bits ST of the third primary color component also change relatively infrequently compared to pixel scan rate so its unnecessary to reiterate ST at pixel scan rates in the pixel codes.

The pixel codes introduced at pixel scan rate into pixel input latch 2 take the format 0000 00UV WXYZ LMNP QRCD EFGH. That is, the relatively slow changing bits A, B, J, K, S and T are suppressed in the pixel codes supplied at the pixel scan rate. Whenever there is a change in the two most significant bits AB of the first primary component, the updated bits AB could be down-loaded from computer main memory into the two most significant bit places of first index register 17. Whenever there is a change in the two most significant bits JK of the second primary color component, the updated bits JK could be down-loaded from computer main memory into the two most significant bit places of second index register 27. Whenever there is a change in the two most significant bits ST of the third primary color component, the updated bits ST could be down-loaded into the two most significant bit places of third index register 37. The six least significant bit places in each of the index register 17, 27 and 37 have ZEROS maintained in them.

Generally, it is preferable from the standpoint of simplifying computer control of the display to arrange that the down-loading of the index registers 17, 27 and 37 be constrained to occur during an index register load interval that is a short portion of line retrace interval. When this is done, the pixel codes for each successive line scan can be changed during index register load interval, based on how many more significant bits in each of the

primary color components are subject to change before the next index register load interval. The FIGURE 1 display processor can carry forward this pixel code abbreviation process for all bit places, although it is likely to be
5 useful only for more significant bit places in the primary color components.

Suppose one arranges for formatting the pixel codes loaded into input pixel latch 2 to include not just prefix ZEROS, or just suffix ZEROS, but also interspersed
10 ZEROS. Then, substantially the same color mapping functions can be carried forward in formatter 7 as in formatter 8, and vice versa.

The loading of the mask registers 11, 21 and 31 of formatter 3 in FIGURE 1 and of the mask registers 38, 41 and 31 of formatters 7 and 8 of FIGURES 2 and 3 is normally carried forward by down-loading from the computer main memory during portions of line retrace intervals. The loading of the index registers 17, 27 and 37 of formatters 3, 7 and 8 is normally carried forward by down-loading from
15 the computer memory during other portions of line retrace intervals. The loading of the shift control registers 14, 24 and 34 of FIGURE 1 formatter 3 normally takes place similarly. One can provide for transitions between various modes of operation during line scan, however. This may be
20 done by providing sets of each of these registers which can be multiplexed among. The multiplexing between two registers in a set--say, two first mask registers 11a and 11b--can be controlled conveniently as follows. A set-reset flip-flop controls the multiplexer selecting
25 between first mask registers 11a and 11b. During each line retrace interval this flip-flop is reset, so the first mask register 11a is selected for supplying the first mask. The outputs of color map RAMs 4, 5 and 6 are applied to first and second decoders that respond to respective conditions
30 of the RAMs outputs designated as SET FLAG and RESET FLAG condition. When the pixel code transferred from computer main memory into pixel input latch 2 is one that causes RAMs 4, 5 and 6 outputs to be in the SET FLAG condition,

the first decoder responds to set the flip-flop so the multiplexer selects first mask register 11b for supplying the first mask. When the pixel code transferred from computer main memory into pixel input latch 2 is one that
5 causes RAMs 4, 5 and 6 outputs to be in the RESET FLAG condition, the second decoder responds to reset the flip-flop so the multiplexer again selects the first mask register 11a for supplying the first mask. The same flip-flop can control selection between paired second mask
10 registers, paired third mask registers, paired first index registers, paired second index registers, paired third index registers, etc. More complex multiplexing arrangements of registers are also readily designed.

FIGURE 11 display processor is a simplification
15 of the FIGURE 2 display processor. In the formatter 18 of the FIGURE 11 display processor the 24-bit third mask register 31, the rank 32 of twenty-four AND gates, shifters 33 and 48, most-significant-bit detector 49, counter 47, third pre-address register 35, the rank 36 of twenty-four
20 OR gates, and the third index register 37 are eliminated. The third color map memory 6 receives the same read addresses as the first color map memory 4. The serial output port of computer main memory supplies an input pixel stream, and connects to a bus that is two bytes (sixteen
25 bits) wide from which bus a shortened pixel input latch 2' is loaded.

The FIGURE 11 display processor is especially adapted for operation wherein the first color map memory 4 contains in its storage locations respective values of a
30 first chrominance-only primary color such as I or (R-Y), wherein the second color map memory 5 contains in its storage locations respective values of a luminance-only primary color Y, and wherein the third color map memory 6 contains in its storage locations respective values of a
35 second chrominance-only primary color. This second chrominance-only primary color would be Q if the first chrominance-only primary color were I and would be (B-Y) if the first chrominance primary color were (R-Y), by way of

specific examples. The two color map memories 4 and 6 may be combined in a single color map memory with address width being unchanged, but with write input and read output widths being doubled in number of bit places; this
5 equivalency should be considered when construing the claims. When simple computer generated graphics are being used, the color map memories 4, 5 and 6 can be re-loaded by down-loading from computer main memory during a portion of a field retrace interval or (usually) a portion of a line
10 retrace interval.

Displays of the quality normally associated with camera-originated images can also be processed. The second color map memory 5 storing Y values is preferably reloaded by down-loading from computer main memory during field
15 retrace intervals. The first color map memory 4 and the third map memory 6 storing chrominance values are reloaded by down-loading from computer main memory during field retrace intervals, as well as during line retrace intervals to the extent needed when tracing the field. In a display
20 with 3:4 aspect ratio, 480 active lines and square pixels, there will be 640 pixels per line corresponding to 6MHz video bandwidth in luminance for a thirty frame per second display device. If chrominance is restricted to 1.2 MHz video bandwidth, there are only 128 pixels per line for
25 chroma. This number of pixels can be specified in a chrominance-only color map with seven-bit read addresses, such as that provided by color map memories 4 and 6 receiving the same read addresses in parallel.

Consider the case where during any line trace
30 interval color map memories 4 and 6 have read addresses descriptive of two adjacent scan lines supplied to them on time-interleaved basis, so the read outputs of these memories can be spatially-interpolated. Assume the rate at which the rate-buffering memory preceding the display
35 process is loaded to be the same rate as luminance pixels are written in the display, and line retrace interval to be 128 luminance pixel durations. The 128 read addresses that must be loaded into the rate-buffering memory every second

line of each field of two-field frame will take one line retrace interval to load. This leaves alternate line retrace intervals to re-write color map memories 4 and 6, supposing the mask and index registers are updated during
5 field trace from the random-access port of computer main memory. Suppose the rate at which color map memories 4 and 6 are rewritten is also the same as that at which luminance pixels are written in the display. If color map memories 4 and 6 have 128 entries in them, it will require two scan
10 line intervals to elapse before they can be completely rewritten. This is usually adequate because it is likely that substantial correlation will be found among chrominance pixels in the two line wide region. It is rare that a line trace interval does not have a number of
15 similar chrominance pixels, or that a pair of successive line trace intervals do not have similar chrominance pixels. Where problems arise spatial resolution in chrominance must be sacrificed for a time.

When displays of the quality normally associated
20 with camera-originated images are processed, normally the read addresses supplied in parallel to color map memories 4 and 6 will not comprise two groups of bits, one group representing a first linearly coded chrominance-only primary color to be decoded by, for example, color map RAM
25 4, and a second group representing a second linearly coded chrominance-only primary color to be decoded by color map RAM 6.

This is because, the input pixel stream may be considered to consist of successive pixels in which each
30 pixel comprises a first group of bits representing the luminance-only primary value of the corresponding location of the image. A second group of bits in each pixel represents one of the two chrominance-only primary values at the corresponding location of the image. The
35 chrominance-only primary represented by the second group of bits in each pixel alternates in successive pixels. That is, in a particular pixel, the second group of bits represents the value of the first chrominance-only primary;

in a next succeeding pixel, the second group of bits represents the value of the second chrominance-only primary; in a next succeeding pixel, the second group of bits represents the value of the first chrominance-only primary, and so forth. Thus, only every other pixel contains bits representing the value of only the first chrominance-only primary color, and the intervening pixels contain bits representing the value of only the second chrominance-only primary color.

Using the arrangement of FIGURE 11, it is possible to time division multiplex the use of color map RAMs 4 and 6 with RAM 4 processing the pixels containing the 8 bits representing the first chrominance-only primary color (e.g. I or (R-Y)), and RAM 7 processing the pixels containing the second chrominance-only primary color (e.g. Q or (B-Y), respectively). It is desirable to specify the chrominance-only value with as much precision as possible those pixels in the image space actually containing chrominance-only primary color information in the current line trace intervals, and not to specify it for pixels not containing the information in the image space. One is attempting to describe, with eight-bit read addresses for both color map memories 4 and 6, the chrominance values for that specific line trace interval with precision in the chrominance amplitude domain that is at least as good as that available with independent eight-bit read addresses for color map memories 4 and 6 in FIGURE 2 formatter 7. That is, one is attempting to replace up to sixteen bits of read addressing capability with at most eight bits of read addressing. Since the read addresses supplied to color map memories 4 and 6 are not linear codes of chrominance values, assuming these read addresses are supplied from computer main memory in a relatively sparse spatial sampling compared to the read addresses supplied to color map memory 5, the spatial interpolation of chrominance values in the FIGURE 11 display processor has to be carried

out on the color map memory 4 and 6 read outputs, rather than on the their read addresses, in the FIGURE 11 display processor.

The FIGURE 12 display processor is a
5 simplification of the FIGURE 3 display processor. In the formatter 19 of the FIGURE 12 display processor the 24-bit third mask register 31, the rank 32 of twenty-four AND gates, shifters 33' and 48', least-significant-bit detector 29, counter 47, third pre-address register 35, the rank 36
10 of twenty-four OR gates, and the third index register 37 are eliminated. The operation is similar to, and the same constraints on operation noted with regard to the FIGURE 11 display processor apply also to the FIGURE 12 display processor.

15 The advantages of color map operation to be obtained when the color map memories can be reloaded during line retrace interval are even greater in the FIGURE 1, FIGURE 2 and FIGURE 3 display processors. In them the twenty-four bit wide bus from the serial output port of the
20 computer main memory facilitates all three color map memories 4, 5 and 6 being written in parallel during line retrace intervals. This capability permits more complex montaging in the display, for example.

In FIGURE 13 a pair of similar display processors
25 50 and 60, each of the same general type as the display processors of FIGURES 1, 2, 3, 11 and 12 are arranged so that they may be operated in banked operation. Banked operation provides display processing speed double that available with just one of the display processors 50, 60.
30 In banked operation serially supplied input data is time-division-multiplexed into a plurality of separate data processing paths, and after data processing is completed in each path the parallel streams of individually processed data are time-division-multiplexed back into one stream of
35 serial output data. This allows system throughput rate to be faster than the individual data processing throughput rate by a factor equal to the number of individual data processing streams.

Image data is supplied from the serial output port of a dual-ported RAM 70, which serves as main computer memory, to a serial-to-parallel converter 71 which converts the image data to successive blocks of thirty-two bits on 32-bit bus 72. A justifier 73 responds to commands from control circuitry 74, (respective parts of which are disposed in the drawing processor and in display processors 50 and 60) to align the most significant bit of the output of justifier 73 to correspond to the most significant bit of data for a pixel. A data splitter 76, which is a network of multiplexers controlled by control circuitry 74, breaks apart the 32-bit block on bus 75 into separate pixels. Pixel code lengths are constrained to be at 2^x values, where x ranges from zero to five inclusive, so the break up is exclusively in terms of whole pixel codes. The separate pixels are numbered modulo two, either by the computer keeping count of pixels or by including a bit in each pixel datum to indicate its being even or being odd.

If pixel data do not have more bits in them than can be stored in pixel input latches 52 and 62 of display processors 50 and 60, data splitter 76 will load successive even pixels into pixel input latch 52 and will load successive odd pixels into pixel input latch 62. Assume, for example, latches 52 and 62 each have 16-bit capacity. Formatters 57 and 67 are similar to FIGURE 2 formatter 7, then, except for shorter input and third mask registers, shorter ranks of AND gates, smaller counters and smaller shifters. Color map memories 54, 55 and 56 in display processor 50 store blue, red and green drive signals, respectively, in digitized form. Color map memories 64, 65 and 66 in display processor 60 store blue, red and green drive signals, respectively, in digitized form. Multiplexers 81, 82 and 83 select read-outs from color map memories 54, 55 and 56 to the inputs of digital-to-analog converters 84, 85 and 86 respectively to be converted to analog blue, red and green drive signals when the display is to be written responsive to even pixel data. Multiplexers 81, 82 and 83 select read-out from color map

memories 64, 65 and 66 to the inputs of DACs 84, 85 and 86 respectively to be converted to analog blue, red and green drive signals when the display is to be written responsive to odd pixel data.

5 If the data concerning one pixel have more bits than can be accommodated by one of the pixel input latches 52 and 62, this image data can be processed by operating display processors in truly parallel operation, where parallel operations are aligned in time, rather than in
10 banked operation where parallel operations are skewed in time by one-pixel-duration offset. The speed advantage of banked operation must be foregone, but practically speaking this is usually acceptable. Many small computers are operated at double "normal" horizontal sweep rate when
15 presenting graphics or text information, so that horizontal display resolution is doubled. The data describing graphics or text information are normally encoded in few bits per pixel format. Large number of bits per pixel formats are normally used for linearly coded
20 camera-originated images or computer simulations of such images, and these images are almost invariably presented at "normal" horizontal sweep rate.

The concept of pixels being even or odd is not used during truly parallel operation. The
25 lower-amplitude-resolution primary color data (i.e., blue and red) is routed through display processor 50 and the higher-amplitude-resolution color data (i.e., green) is routed through display processor 60. Then, multiplexer 81 selects color map memory 54 read-out to the input of DAC 84
30 to generate blue drive signal for all pixels. Multiplexer 82 selects color map memory 55 read-out to the input of DAC 85 to generate red drive signal for all pixels. Multiplexer 83 selects color map memory 66 read-out to the
input of DAC 86 to generate green drive signal for all
35 pixels. Truly parallel operation can be adapted to Y,I,Q operation, processing Y in one display processor, and processing I and Q in another display processor.

Multiplexers 81, 82 and 83 are shown in FIGURE 13 as being controlled by control circuitry 74, assuming that the computer keeps count of pixels modulo two. If pixel evenness or oddness is encoded in one bit of the data concerning each pixel, this bit is decoded to control multiplexers 81, 82 and 83 instead.

The proper working of cascade connection of serial-to-parallel converter 71, justifier 73 and data splitter 76 relies on the lengths of the pixel codes being 2^m bits where m is a positive integer from zero to five inclusive. This makes an even number of pixel codes fit into each four-byte (32-bit) output of serial-to-parallel converter 71. More flexibility with regard to code length can be achieved by using a regularly shifting serial-input/parallel-output register as converter 71 and timing the loading of pixel input latches 52 and 62 to operate them as "pixel grabbers". Loading is done each time the most significant bit of a pixel code is in the most significant bit place of converter 71 output. Latches 52 and 62 are alternately loaded, on even and odd pixels respectively, when banked operation of display processors 50 and 60 is employed. Latches 52 and 62 are loaded in parallel on every pixel when display processors 50 and 60 are operated truly parallel with each other.

FIGURE 14 shows how the display processors described in connection with FIGURES 1, 2, 3, 11 and 12 may be connected to display apparatus. More specifically, connection to a color kinescope 90 will be described. A switch 91 is used for selectively routing the read outputs from color map memories 4, 5 and 6 through or around spatial interpolation circuitry 92. Where banking is used, as described in connection with FIGURE 13, switch 91 will be preceded by the color map memory read out multiplexer. Spatial interpolation circuitry 92 does spatial interpolation after display processing, when this form of processing is selected, and it is most convenient to do spatial interpolation when the pixels are described in digitized sample data form. Preferably, spatial

interpolation is carried out in both vertical and horizontal directions in the image field. This is done by transversal filtering having low-pass characteristics in both of the spatial dimensions. As noted previously in this specification, it is convenient to use a rate-buffering memory between computer main memory and the display processor, so that two adjacent lines of pixel samples can be time interleaved, alternately selecting samples from each line to be applied to the display processor to generate sequentially the groups of spatially adjacent pixel samples need for spatial interpolation circuitry 92.

Digital-to-analog converters 93, 94 and 95 convert to respective continuous analog signals the three parallel streams of pixel descriptions in digitized sample data form supplied from control map memories 4, 5 and 6. A switch 96 is used for selectively routing these analog signals to or around color matrix circuitry 97. If the analog signals from digital-to-analog converters 93, 94 and 95 are not blue, red and green signals switch 96 will route them through color matrix circuitry 97 for conversion to blue, red and green signals. Alternatively, color matrixing could be done prior to digital-to-analog conversion, but it is generally preferable to avoid doing multiplications in the digital domain.

With regard to color matrix circuitry 97, it is preferable to express the digital chrominance-only primary color components in positive numbers to simplify the digital-to-analog converters 93, 94 and 95. Also these digital chrominance-only primary color components may be scaled in amplitude so their maximum amplitudes more completely fill the dynamic range available in the number of bit places describing them. This preserves amplitude resolution in the color map memories 4, 5 and 6 and in digital-to-analog converters 93, 94 and 95. If these measures are taken, color matrix circuitry 97 will include means to remove the offsets in the chrominance-only primary color components, such as I and Q or (R-Y) and (B-Y), to

restore them to signal quantities. This is done before these components are rescaled and linearly combined with luminance-only primary color component to generative additive primary color components.

5 The blue, red and green analog signals as amplified by video amplifiers 101, 102 and 103 are supplied as drive signals to color kinescope 90. The transconductances of video amplifiers 101, 102 and 103 are preferably made linear.

10 If spatial interpolation circuitry 92 after display processing is not required, it can be discarded, and selector switch 91 can be replaced by wired connections. If one of the color map memories 4, 5 and 6 always stores values of a luminance-only primary color, and
15 if the other two color map memories store values of respective chrominance-only primary colors, color matrix circuitry 97 will invariably be needed. Circuitry 97 can then be wired in permanently, dispensing with selector switch 96. If the color map memories 4, 5 and 6 always
20 store values of the additive primaries, color matrix circuitry 97 can be discarded, and selector switch 91 can be replaced by respective wired connections between the digital-to-analog converters 93, 94, 95 and the video amplifiers 101, 102, 103.

25 Consider the way that the main computer memory can be connected to the pixel input latch 2 or 2'. The main memory supplies serial output on a bus wider in terms of bit places than the pixel input latch 2 or 2' (e.g. on a 32-bit wide bus). Parallel storage registers are provided
30 for two successive main memory outputs. The inputs of the parallel storage registers are multiplexed, and the outputs of the parallel storage registers also are multiplexed. This multiplexing is controlled by modular counting of successive accesses from main memory. Accordingly, the
35 next-to-last main memory output and the last memory output are simultaneously available in a continuous 64-bit-wide window that scans along scan line in the bit-map-organized pixel storage in main memory. A shifter shifts these

parallel-in-time data to justify one pixel at a time. Shifting is controlled in accordance with the modular count of accesses from main memory and knowledge as to the number of bit places per pixel code. A masking procedure

5 (controlled by knowledge as to the number of bit places per pixel code) is carried out to load one pixel at a time into the pixel input latch 2 or 2' and to fill with ZEROS the bit places left over in the pixel input latch.

10 In a more practical design parallel storage registers can be provided for one main computer memory read-out and part of the preceding main computer memory read-out. This is readily done with more complex input and output multiplexers to the parallel storage registers. The shifter used to justify pixels can then be made narrower in
15 number of bit places input, and bit place shifts will be smaller.

As alluded to earlier in the specification, the circuitry to multiplex pixel codes described in the previous two paragraphs may be modified to include
20 rate-buffering memory where there is to be spatial interpolation of the outputs of any of the color map memories 4, 5 and 6.

CLAIMS

1. A display processor comprising:
 - a first color map memory addressable by a first read address of p bits during its reading, p being a positive integer;
 - a first pre-address register for temporarily storing a p -bit first pre-address;
 - means for generating from said p -bit first pre-address said first read address;
 - a second color map memory addressable by a second read address of q bits during its reading, q being a positive integer;
 - a second pre-address register for temporarily storing a q -bit second address;
 - means for generating from said q -bit first pre-address said second read address;
 - a pixel input latch having a width of at least $(p+q)$ bits into which the data for respective pixels are serially loaded;
 - means for selecting from the contents of said pixel input latch a first number of bits from adjacent bit places, said first number being no larger than p ;
 - means for applying the first number of bits in justified format to said first pre-address register as at least a portion of said first pre-address and applying ZEROS as any remaining portion of said first pre-address, to be temporarily stored in said first pre-address register;
 - means for selecting from the contents of said pixel input latch a second number of bits from adjacent bit places, said second number being no larger than q ;
 - means for selecting a second number of bits being of a type in which there is a choice of which bit places are to be included in said second number that is independent of which bit places are included in said first number; and
 - means for applying the second number of bits in justified format to said second pre-address register as at least a portion of said second pre-address and applying

ZEROs as any remaining portion of said second pre-address, to be temporarily stored in said second pre-address register.

2. A display processor as set forth in Claim 1 having a width of at least $(p+q+r)$ bits in its said input latch and further including:

a third color map memory addressable by a third read address of r bits during its reading, r being a positive integer;

a third pre-address register for temporarily storing an r -bit third pre-address;

means for generating from said r -bit pre-address said third read address;

means for selecting from the contents of said pixel input latch a third number of bits from adjacent bit places, said third number being no larger than r , said means for selecting a third number of bits being of a type in which there is a choice of which bit places are to be included in said third number that is independent of which bit places are included in said first number and in said second number respectively; and

means for applying the third number of bits in justified format to said third pre-address register as at least a portion of said third pre-address and applying ZEROs as any remaining portion of said third pre-address, to be temporarily stored in said third pre-address register.

3. A display processor as set forth in Claim 2, wherein said means for generating said first read address includes:

a first index register storing a first index therein having p bits, and

means for combining said first index with first pre-address temporarily stored in said first pre-address register to generate said first read address.

4. A display processor as set forth in Claim 3 wherein said means for combining said first index with the first pre-address consists of:

a first rank of OR gates ORing the bits temporarily stored in said first pre-address register with respective bits of said first index register to generate said first read address.

5. A display processor as set forth in Claim 3; wherein said means for generating said second read address includes:

a second index register storing a second index therein having q bits, and

means for combining said second index with the second pre-address temporarily stored in said second pre-address register to generate said second read addresses.

6. A display processor as set forth in Claim 5 wherein said means for combining said second index with the second pre-address consists of:

a second rank of OR gates ORing the bits temporarily stored in said second pre-address register with respective bits of said second index register to generate said second read address.

7. A display processor as set forth in Claim 5; wherein said means for generating said third read address includes:

a third index register storing a third index therein having r bits, and

means for combining said third index with the third pre-address temporarily stored in said third pre-address register to generate said third read address.

8. A display processor as set forth in Claim 7 wherein said means for combining said third index with the third pre-address consists of:

a third rank of OR gates ORing the bits temporarily stored in said third pre-address register with respective bits of said third index register.

9. A display processor as set forth in Claim 2, wherein said means for generating said first read address includes:

a first index register storing a first index therein having a number of bits therein corresponding to the number of bits in any remaining portion of said first pre-address, and

means for combining said first index with first pre-address temporarily stored in said first pre-address register to generate said first read address.

10. A display processor as set forth in Claim 9 wherein said means for combining said first index with the first pre-address consists of:

a first rank of OR gates ORing the bits of said any remaining portion of said first pre-address with bits of said first index to generate said first read address.

11. A display processor as set forth in Claim 9, wherein said means for generating said second read address includes:

a second index register storing a second index therein having a number of bits therein corresponding to the number of bits in any remaining portion of said second pre-address, and

means for combining said second index with the second pre-address temporarily stored in said second pre-address register to generate said second read addresses.

12. A display processor as set forth in Claim 11 wherein said means for combining said second index with the second pre-address consists of:

a second rank of OR gates ORing the bits of said any remaining portion of said second pre-address with bits of said second index to generate said second read address.

13. A display processor as set forth in Claim 11, wherein said means for generating said third read address includes:

a third index register storing a third index therein having a number of bits therein corresponding to the number of bits in any remaining portion of said third pre-address, and

means for combining said third index with the third pre-address temporarily stored in said third pre-address register to generate said third read address.

14. A display processor as set forth in Claim 7 wherein said means for combining said third index with the third pre-address consists of:

a third rank of OR gates ORing the bits of said any remaining portion of said third pre-address with bits of said third index to generate said third read address.

15. A display processor as set forth in Claim 2 wherein said justified format is one in which justification is in the direction of increased significance.

16. A display processor as set forth in Claim 2 wherein said justified format is one which justification is in the direction of decreased significance.

17. A display processor as set forth in Claim 2 wherein said means for selecting from the contents of said pixel input latch a first number of bits is of a type that invariably selects the most significant bits in said pixel input latch.

18. A display processor as set forth in Claim 2 wherein said means for selecting from the contents of said pixel input latch a first number of bits is of a type that invariably selects the least significant bits in said pixel input latch.

19. A display processor as set forth in Claim 2 in combination with:

a color kinescope;

digital-to-analog converter means for converting the streams of successive digitized read-outs from said first, second and third color map memories, to respective continuous analog signals each descriptive of a respective additive primary color component; and

first, second and third video amplifiers for supplying to said color kinescope as blue, red and green drive signals amplified responses to the continuous analog signals supplied to said video amplifiers from said digital-to-analog converter means.

20. A display processor as set forth in Claim 2 in combination with:

digital-to-analog converter means for converting to respective analog signals the streams of successive digitized read-outs from said first, second and third color map memories; and

color matrixing circuitry for converting those analog signals to analog signals each descriptive of a respective additive primary color component.

21. A combination as set forth in Claim 20 further including means for providing spatial interpolation to the read-out from at least one of said first, second and third color map memories prior to its conversion to a respective analog signal by said digital-to-analog converter means.

22. A combination as set forth in Claim 20 further including:

a color kinescope; and

first, second and third video amplifiers for supplying to said color kinescope as blue, red and green drive signals amplified responses to the continuous analog signals supplied to said video amplifiers from said analog-to-digital converter means.

23. A plurality of display processors as set forth in Claim 2 in combination with;

means for providing banked operation of said plurality of display processors.

24. A pair of display processors as set forth in Claim 2 in combination with;

means for selectively providing banked operation of said pair of display processors or truly parallel operation of said pair of display processors.

25. A display processor as set forth in Claim 1 further including:

a third color map memory addressable by said first read address during its reading.

26. A display processor as set forth in Claim 25, wherein said means for generating said first read address includes:

a first index register storing a first index therein having p bits, and

means for combining said first index with first pre-address temporarily stored in said first pre-address register to generate said first read address.

27. A display processor as set forth in Claim 26 wherein said means for combining said first index with the first pre-address consists of:

a first rank of OR gates ORing the bits temporarily stored in said first pre-address register with respective bits of said first index register to generate said first read address.

28. A display processor as set forth in Claim 27; wherein said means for generating said second read address includes:

a second index register storing a second index therein having q bits, and

means for combining said second index with the second pre-address temporarily stored in said second pre-address register to generate said second read addresses.

29. A display processor as set forth in Claim 28 wherein said means for combining said second index with the second pre-address consists of:

a second rank of OR gates ORing the bits temporarily stored in said second pre-address register with respective bits of said second index register to generate said second read address.

30. A display processor as set forth in Claim 25; wherein said means for generating said second read address includes:

a second index register storing a second index therein having q bits, and

means for combining said second index with the second pre-address temporarily stored in said second pre-address register to generate said second read address.

31. A display processor as set forth in Claim 30 wherein said means for combining said second index with the second pre-address consists of:

a second rank of OR gates ORing the bits temporarily stored in said second pre-address register with respective bits of said second index register.

32. A display processor as set forth in Claim 25, wherein said means for generating said first read address includes:

a first index register storing a first index therein having a number of bits therein corresponding to the number of bits in any remaining portion of said first pre-address, and

means for combining said first index with first pre-address temporarily stored in said first pre-address register to generate said first read address.

33. A display processor as set forth in Claim 32 wherein said means for combining said first index with the first pre-address consists of:

a first rank of OR gates ORing the bits of said any remaining portion of said first pre-address with bits of said first index to generate said first read address.

34. A display processor as set forth in Claim 32, wherein said means for generating said second read address includes:

a second index register storing a second index therein having a number of bits therein corresponding to the number of bits in any remaining portion of said second pre-address, and

means for combining said second index with the second pre-address temporarily stored in said second pre-address register to generate said second read addresses.

35. A display processor as set forth in Claim 34 wherein said means for combining said second index with the second pre-address consists of:

a second rank of OR gates ORing the bits of said any remaining portion of said second pre-address with bits of said second index to generate said second read address.

36. A display processor as set forth in Claim 25, wherein said means for generating said second read address includes:

a second index register storing a second index therein having a number of bits therein corresponding to the number of bits in any remaining portion of said second pre-address, and

means for combining said second index with the second pre-address temporarily stored in said second pre-address register to generate said second read address.

37. A display processor as set forth in Claim 36 wherein said means for combining said second index with the second pre-address consists of:

a second rank of OR gates ORing the bits of said any remaining portion of said second pre-address with bits of said second index to generate said second read address.

38. A display processor as set forth in Claim 25 wherein said justified format is one in which justification is in the direction of increased significance.

39. A display processor as set forth in Claim 25 wherein said justified format is one which justification is in the direction of decreased significance.

40. A display processor as set forth in Claim 25 wherein said means for selecting from the contents of said pixel input latch a first number of bits is of a type that invariably selects the most significant bits in said pixel input latch.

41. A display processor as set forth in Claim 25 wherein said means for selecting from the contents of said pixel input latch a first number of bits is of a type that invariably selects the least significant bits in said pixel input latch.

42. A display processor as set forth in Claim 25 in combination with:

digital-to-analog converter means for converting to respective analog signals the streams of successive digitized read-outs from said first, second and third color map memories; and

color matrixing circuitry for converting those analog signals to analog signals each descriptive of a respective additive primary color component.

43. A combination as set forth in Claim 42 further including means for providing spatial interpolation to the read-out from at least one of said first, second and third color map memories prior to its conversion to a respective analog signal by said digital-to-analog converter means.

44. A combination as set forth in Claim 42 further including:

a color kinescope; and

first, second and third video amplifiers for supplying to said color kinescope as blue, red and green drive signals amplified responses to the continuous analog signals supplied to said video amplifiers from said analog-to-digital converter means.

45. A plurality of display processors as set forth in Claim 25 in combination with;

means for providing banked operation of said plurality of display processors.

46. A pair of display processors as set forth in Claim 25 in combination with;

means for selectively providing banked operation of said pair of display processors or truly parallel operation of said pair of display processors.

47. A display processor comprising:

first, second and third color map memories;

means responsive to the read-outs from each of said first, second and third color map memories for generating a color display image;

means for supplying pixel data encoded in several-bit words;

means for generating read addresses for said first color map memory from a selected portion of the bits in each word of pixel data;

means for generating read addresses for said second color map memory from a selected portion of bits in each word of pixel data differing from the selected portion of the bits in each word of pixel data from which read addresses for said first color map memory are generated and

means for generating read addresses for said third color map memory from a selected portion of the bits in each word of pixel data, differing from the selected portion of the bits in each word of pixel data from which addresses for said first color map memory are generated, and differing from the selected portion of the bits in each word of pixel data from which read addresses for said second color map memory are generated.

48. A display processor as set forth in Claim 47 wherein said means responsive to the read-outs of said first, second and third color map memories for generating a color display image includes:

combining by addition or subtraction processes the read-outs from said first and third color map memories with the read-out from said second color map memory for generating red, green and blue drive signals.

49. A display processor comprising:
first, second and third color map memories;
means for supplying pixel data encoded in
several-bit words;
means for generating read addresses for said
first color map memory from a selected portion of the bits
in each word of pixel data;
means for generating read addresses for said
second color map memory from a selected portion of bits in
each word of pixel data differing from the selected portion
of the bits in each word of pixel data from which read
addresses for said first color map memory are generated
means for generating read addresses for said
third color map memory from a selected portion of the bits
in each word of pixel data, differing from the selected
portion of the bits in each word of pixel data from which
addresses for said second color map memory are generated;
means combining by addition or subtraction
processes the read-outs from said first and second color
map memories with the read-out of said second color map
memory for generating red, green and blue drive signals.

50. A display processor comprising:
first, second and third color map memories;
means for supplying pixel data encoded in
several-bit words;
means for generating read addresses for said
first and third color map memories from a selected portion
of the bits in each word of pixel data;
means for generating read addresses for said
second color map memory from a selected portion of bits in
each word of pixel data differing from the selected portion
of the bits in each word of pixel data from which read
addresses for said first color map memory are generated and
means combining by addition or subtraction
processes the read-outs from said first and third color map
memories with the read-out of said second color map memory
for generating red, green and blue drive signals.

51. In combination:

a color map memory addressable with read addresses of a plurality, n in number, of bits;

means for generating successive pixel codes each having a plurality of bits, m in number, which number m never exceeds n and at least at times is less than n ;

means for applying said m bit places of each said pixel code to said color map memory as m adjacent bit places of its read address;

means for applying as the remaining $n-m$ bit places of said color map memory read address a selected one of 2^{n-m} bit patterns; and

means for programmably changing said one of 2^{n-m} bit patterns.

52. In combination as set forth in Claim 51, said m adjacent bit places of said color map memory input address being least significant bit places of said color map memory input address.

53. In combination as set forth in Claim 51, said m adjacent bit places of said color map memory input address being most significant bit places of said color map memory input address.

54. In combination:

a color map memory addressable with read addresses of a plurality, n in number, of bits;

means for generating members of any selected one of a plurality of sets of pixel codes, each set of pixel codes consisting of a succession of consecutive pixel codes ranging from zero to an upper limit number; and

means for generating read addresses for said color map memory by linearly combining the generated pixel codes with a number associated with the set to which they belong, the numbers respectively associated with said sets of pixel codes being chosen so those sets of pixel codes generate read addresses for different portions of said color map memory.

55. A display processor comprising:

a first color map memory addressable by a read address of p bits during its reading, p being a positive integer;

a second color map memory addressable by a read address of q bits during its reading, q being a positive integer;

a pixel input latch having a width of at least $(p + q)$ bits into which data for respective pixels are loaded;

means for selecting from the contents of said pixel input latch a first and a second number of bits, wherein the bits of said pixel input latch included in said first number of bits is independent of the bits of said pixel input latch included in said second number of bits, and said first and second numbers may vary; and

means for coupling said first and second numbers of bits to said first and second color map memories respectively as read addresses.

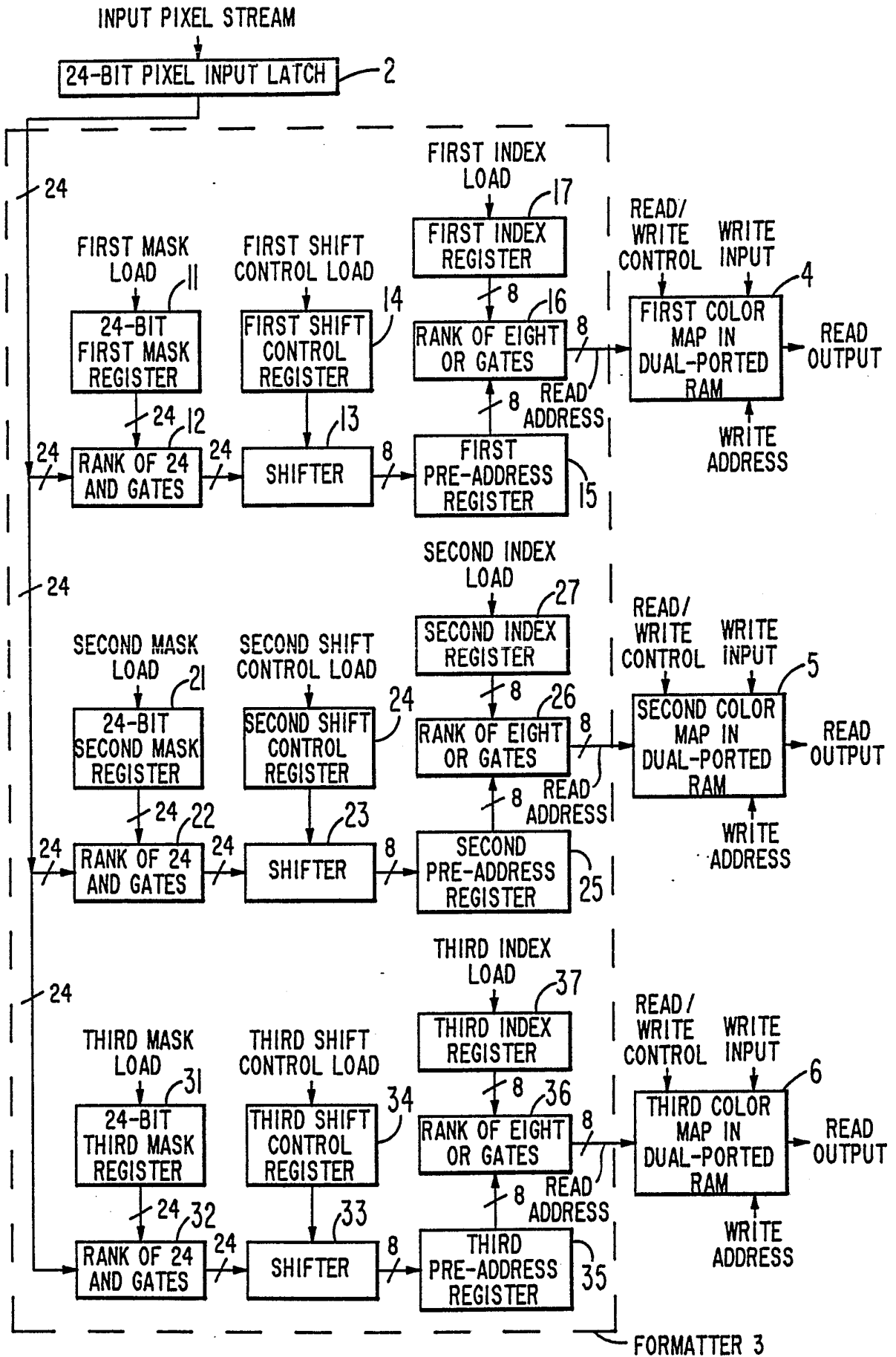


Fig. 1

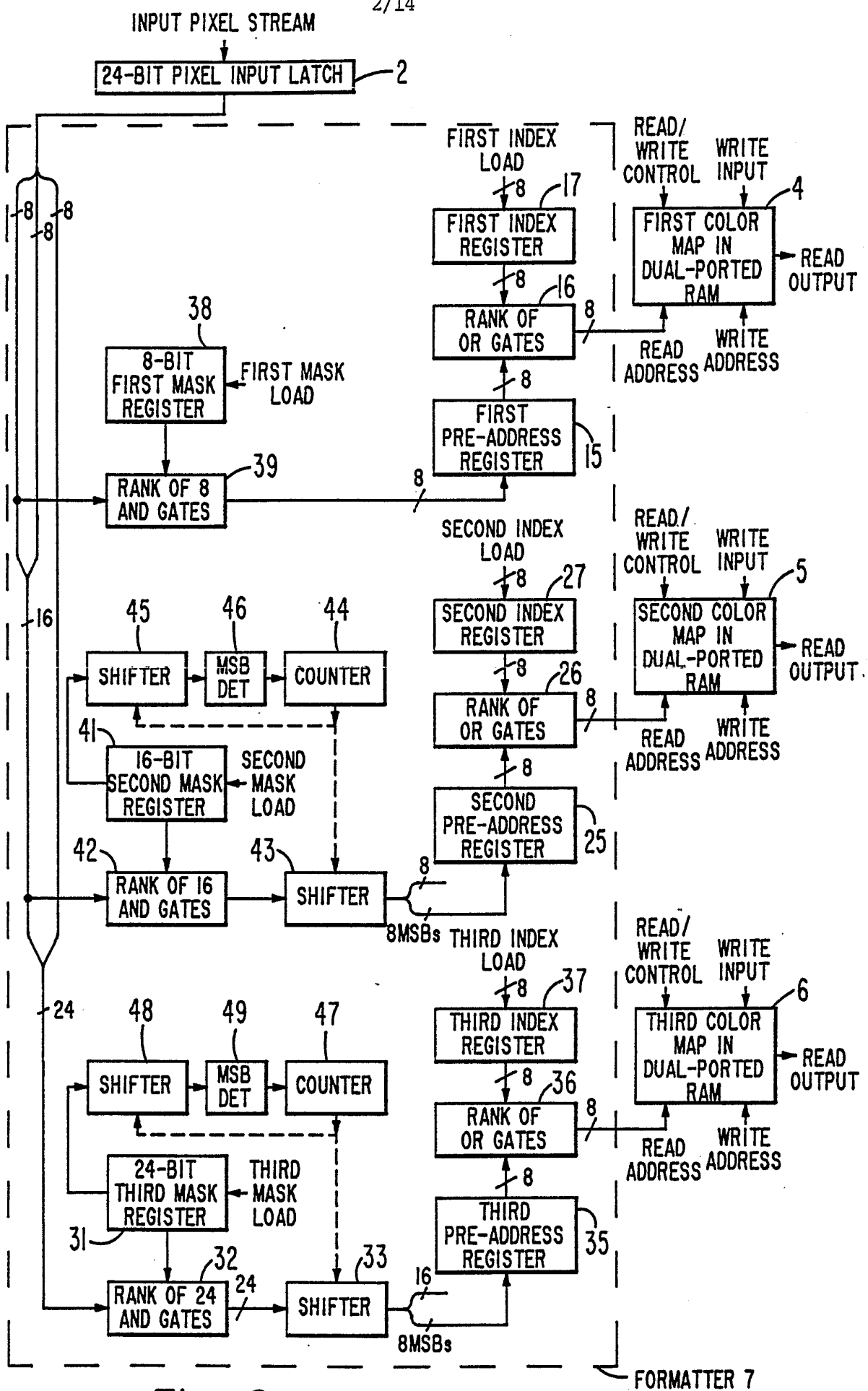


Fig. 2

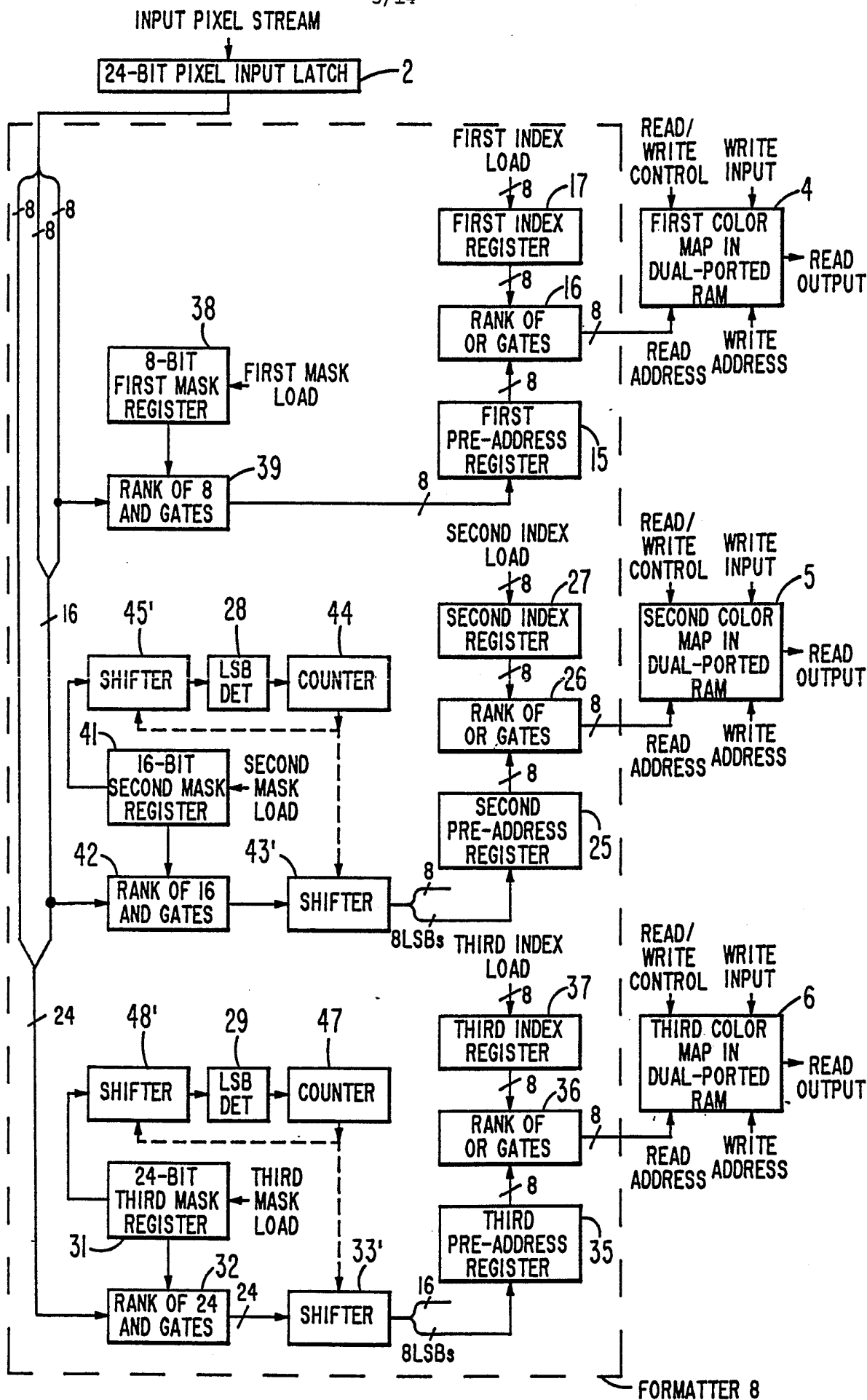


Fig. 3

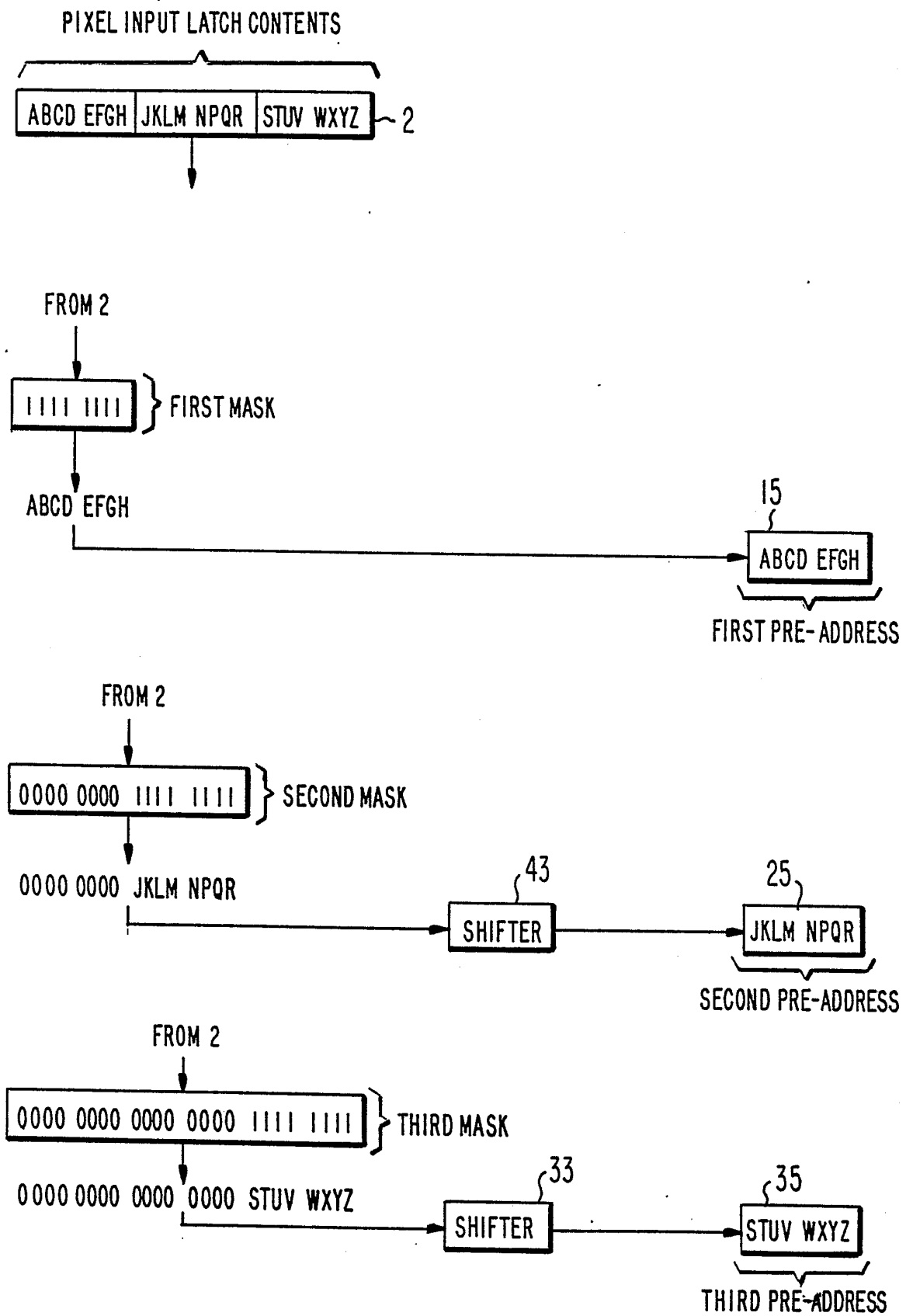


Fig. 4

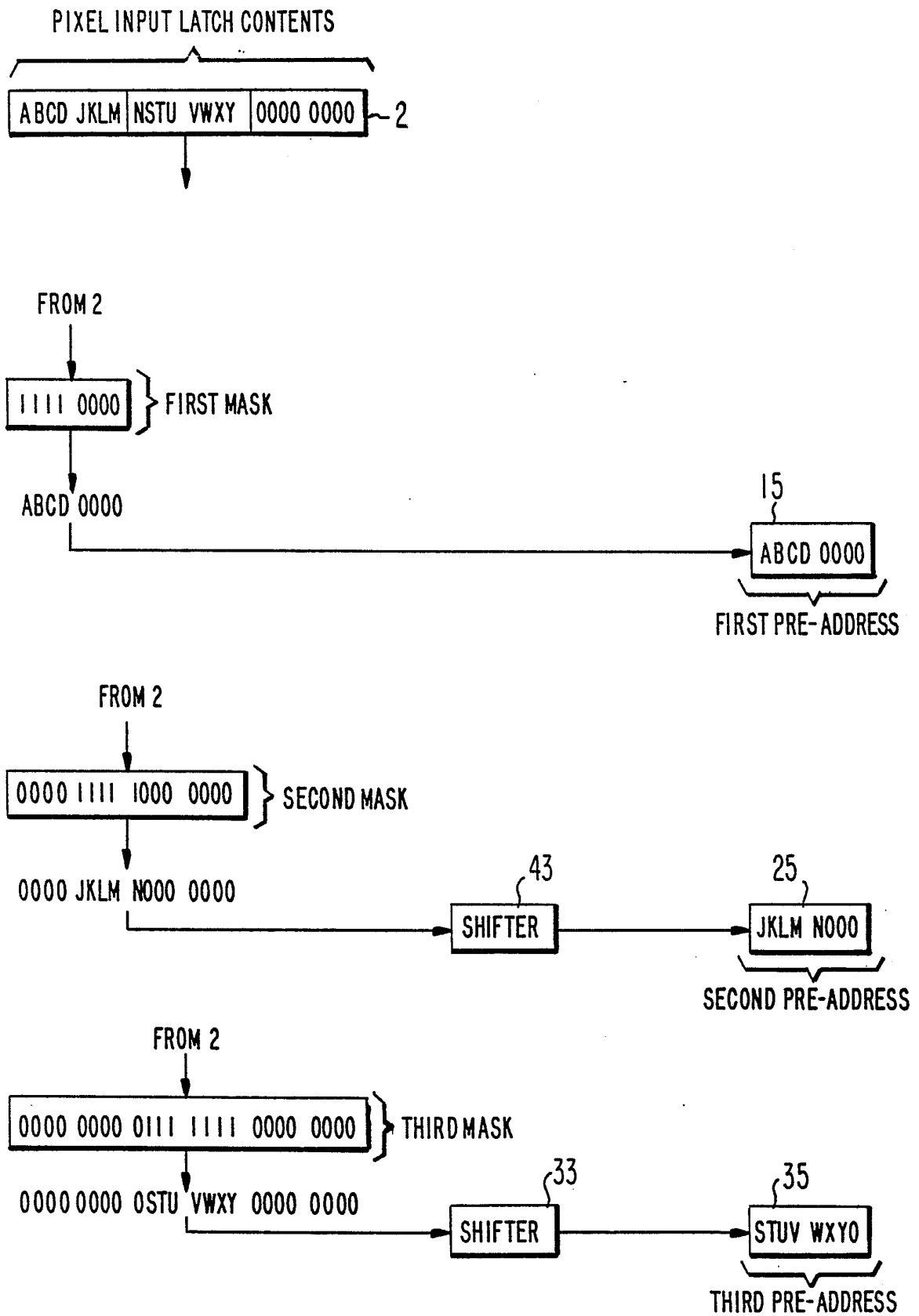


Fig. 5

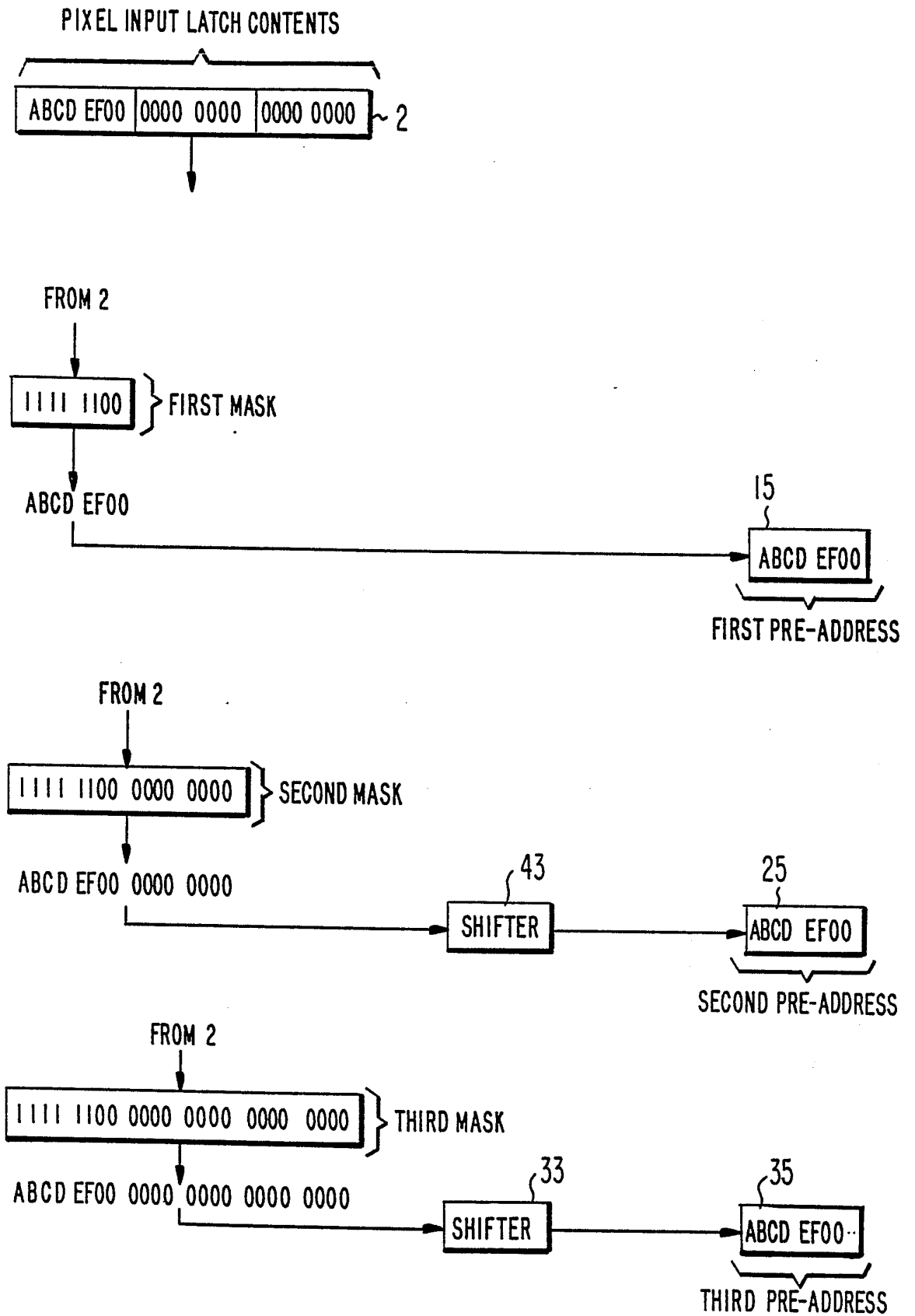


Fig. 6

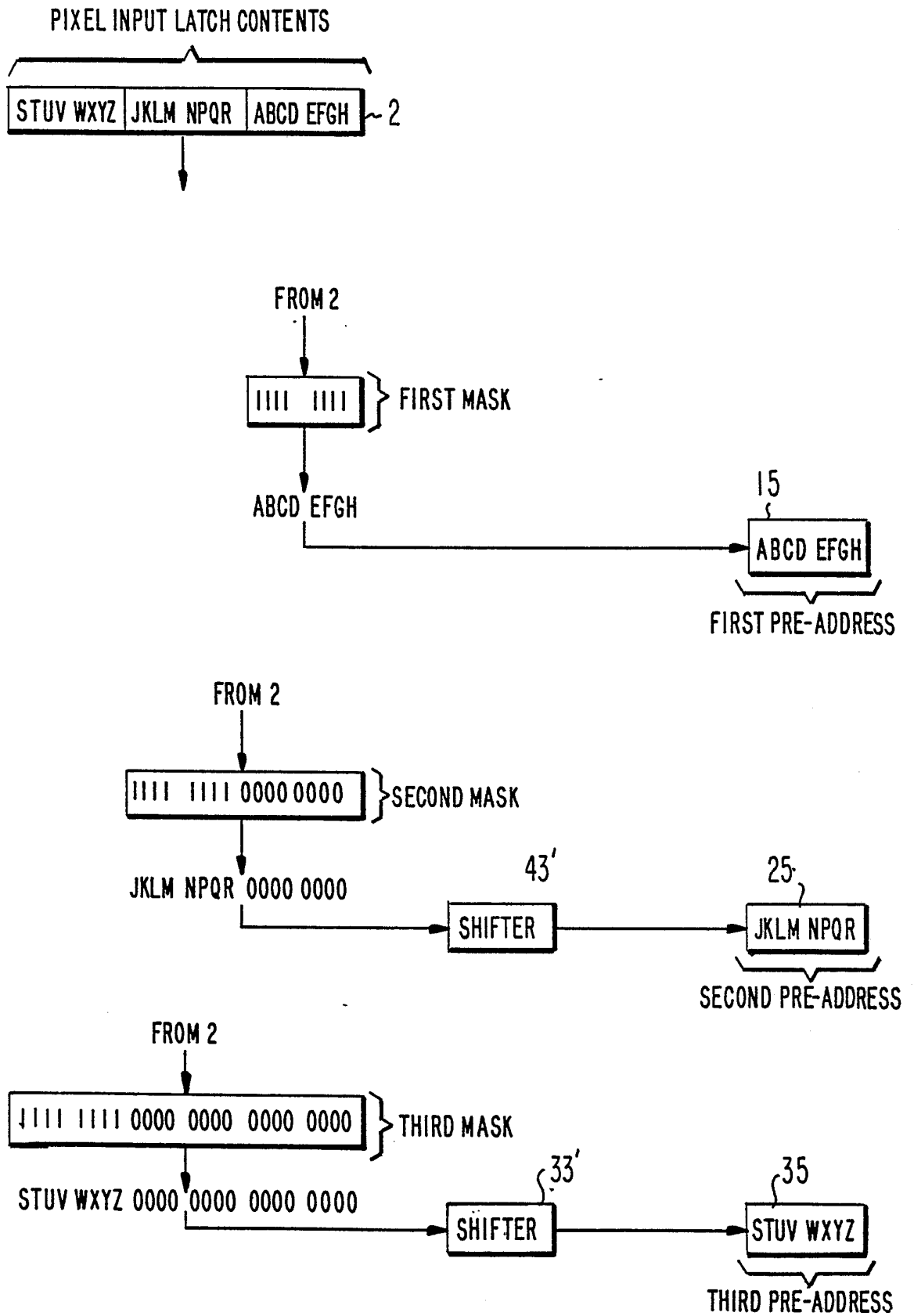


Fig. 7

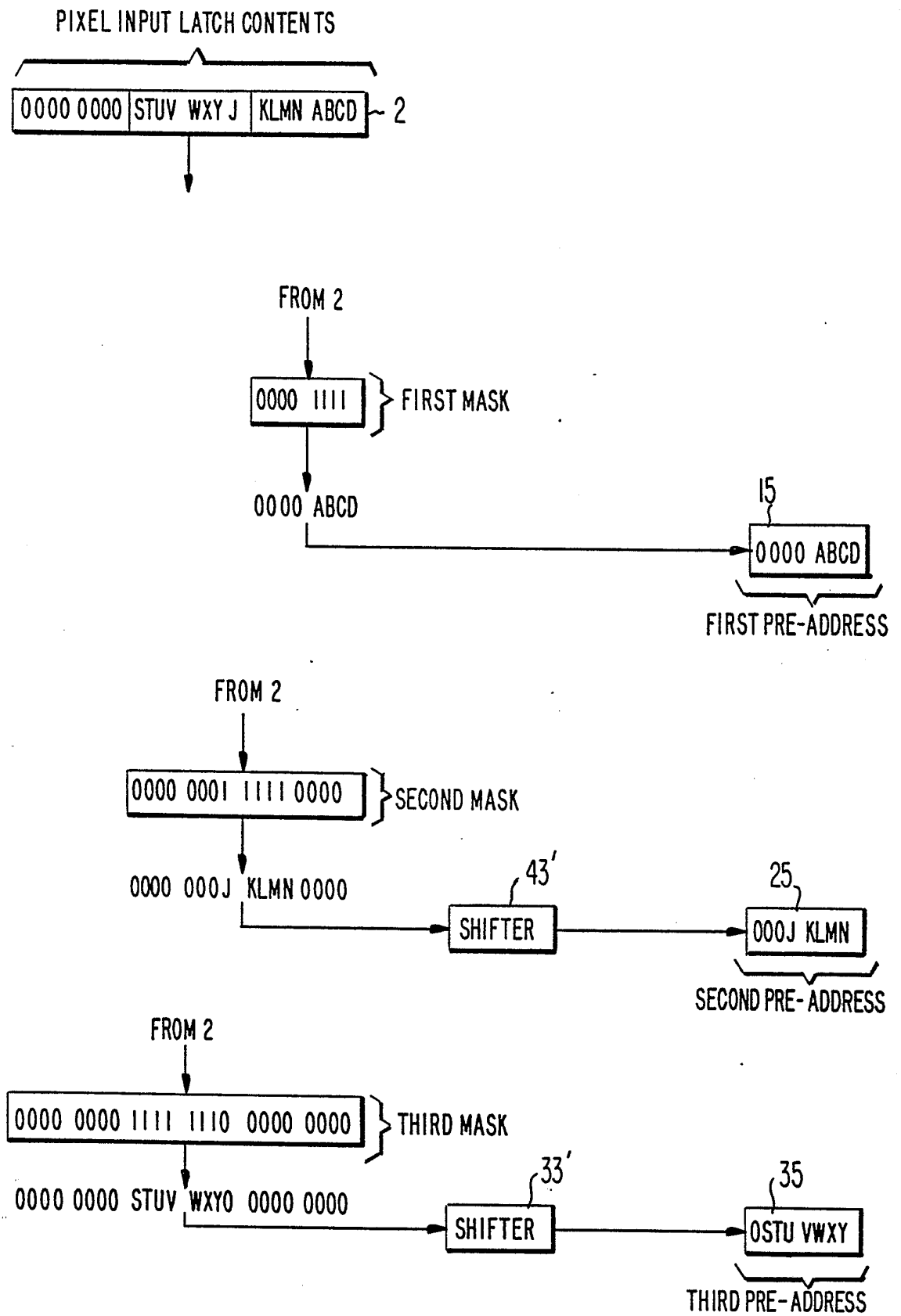


Fig.8

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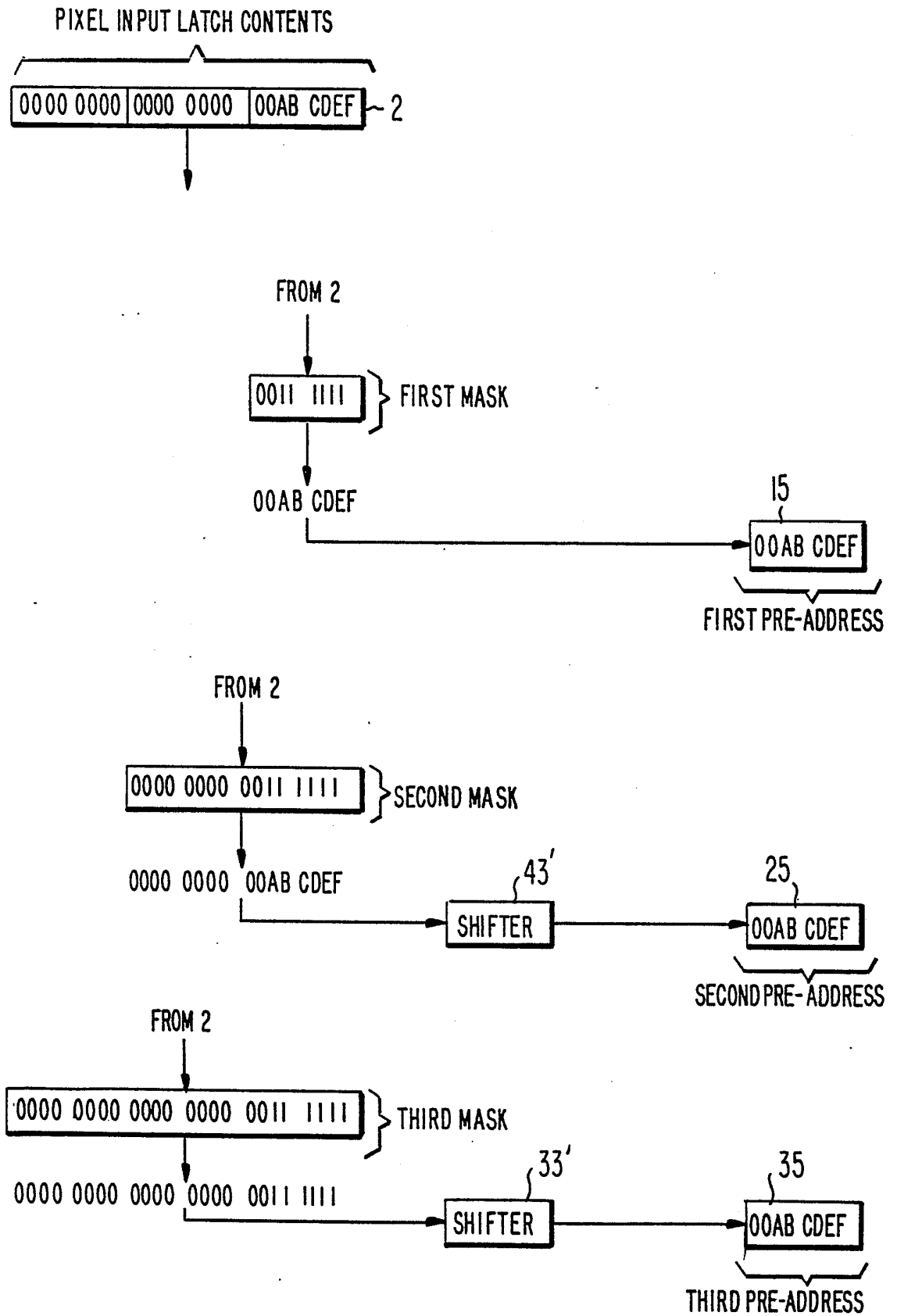


Fig. 9

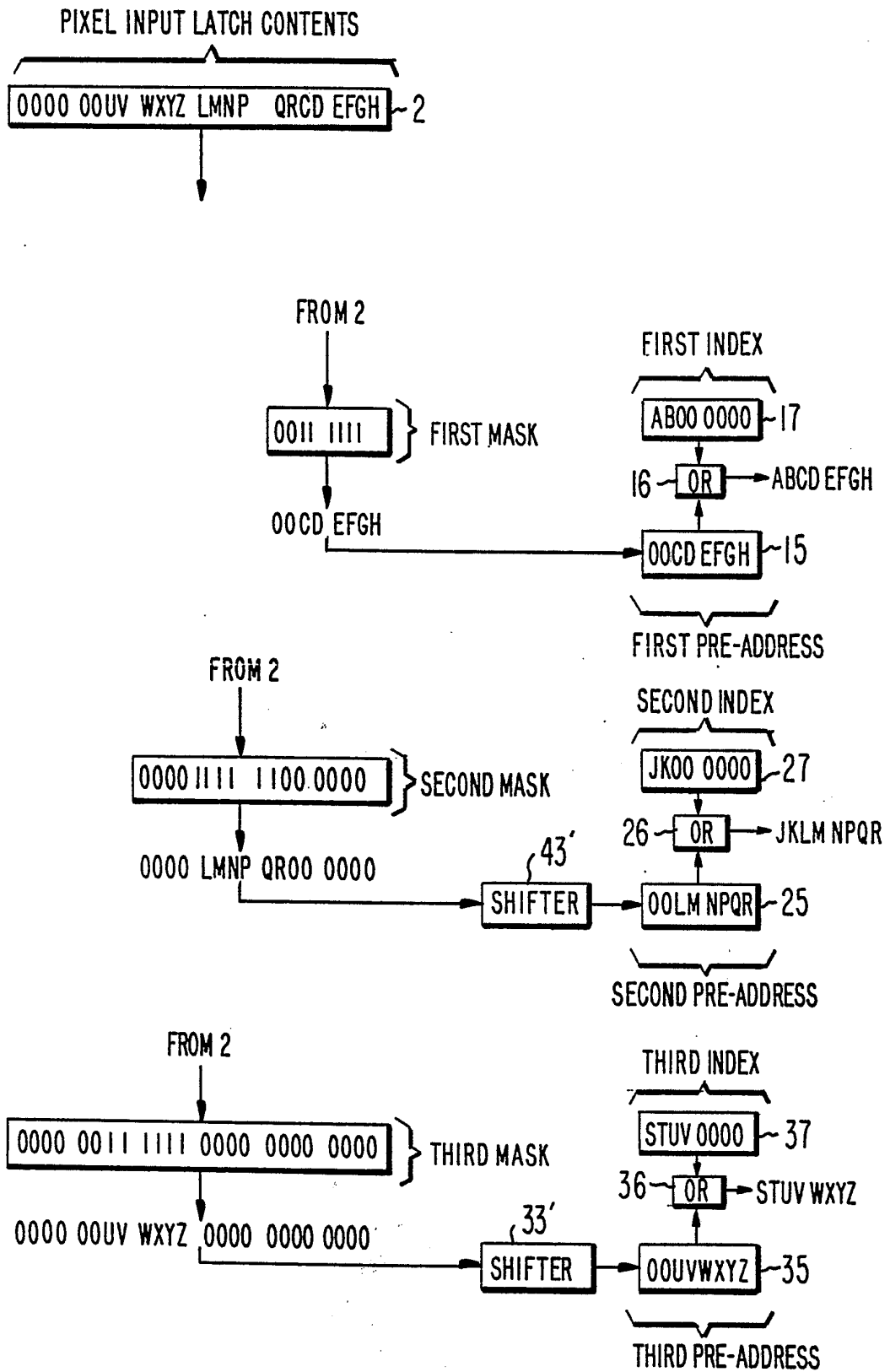


Fig. 10

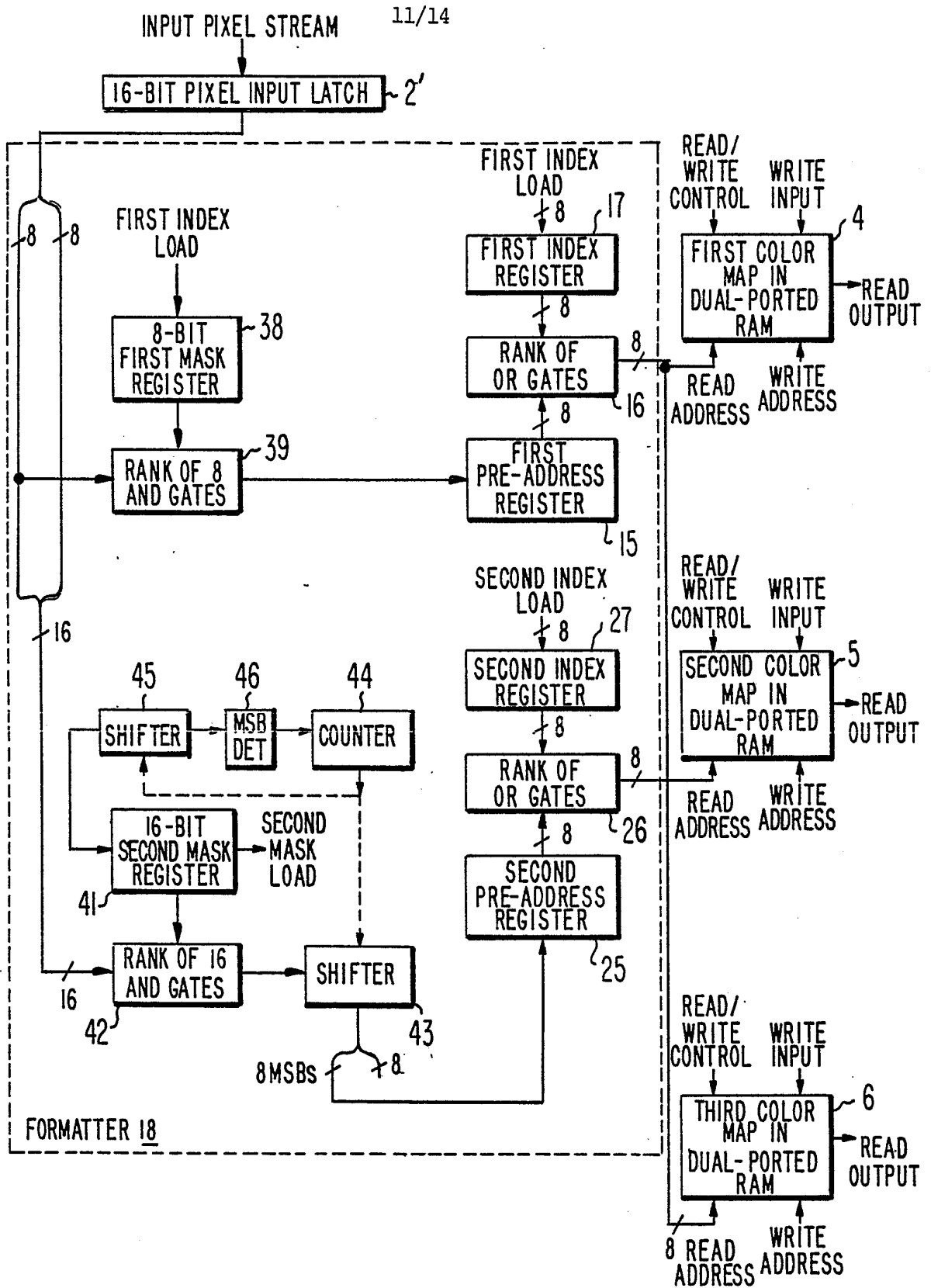


Fig.11

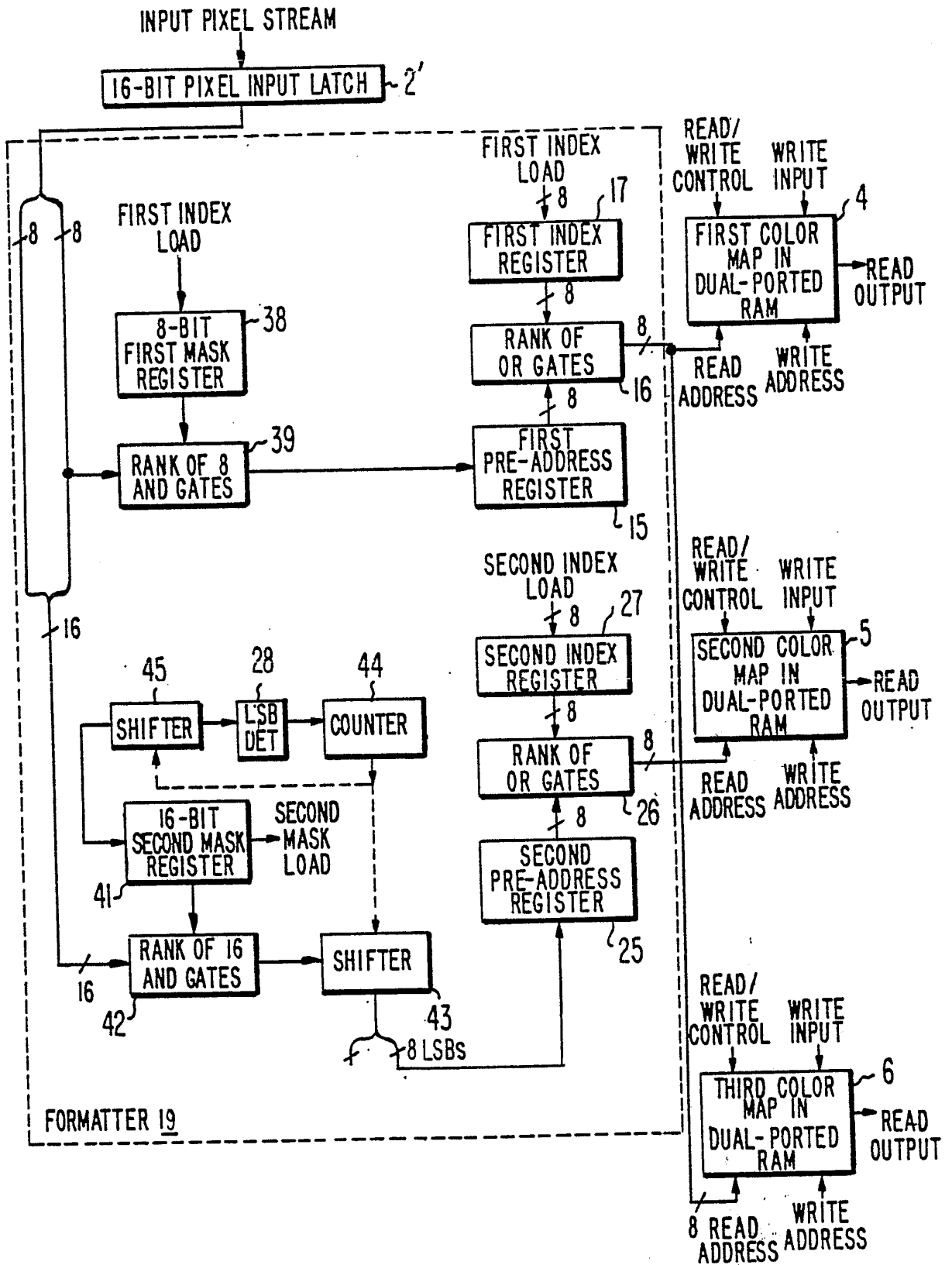


Fig.12

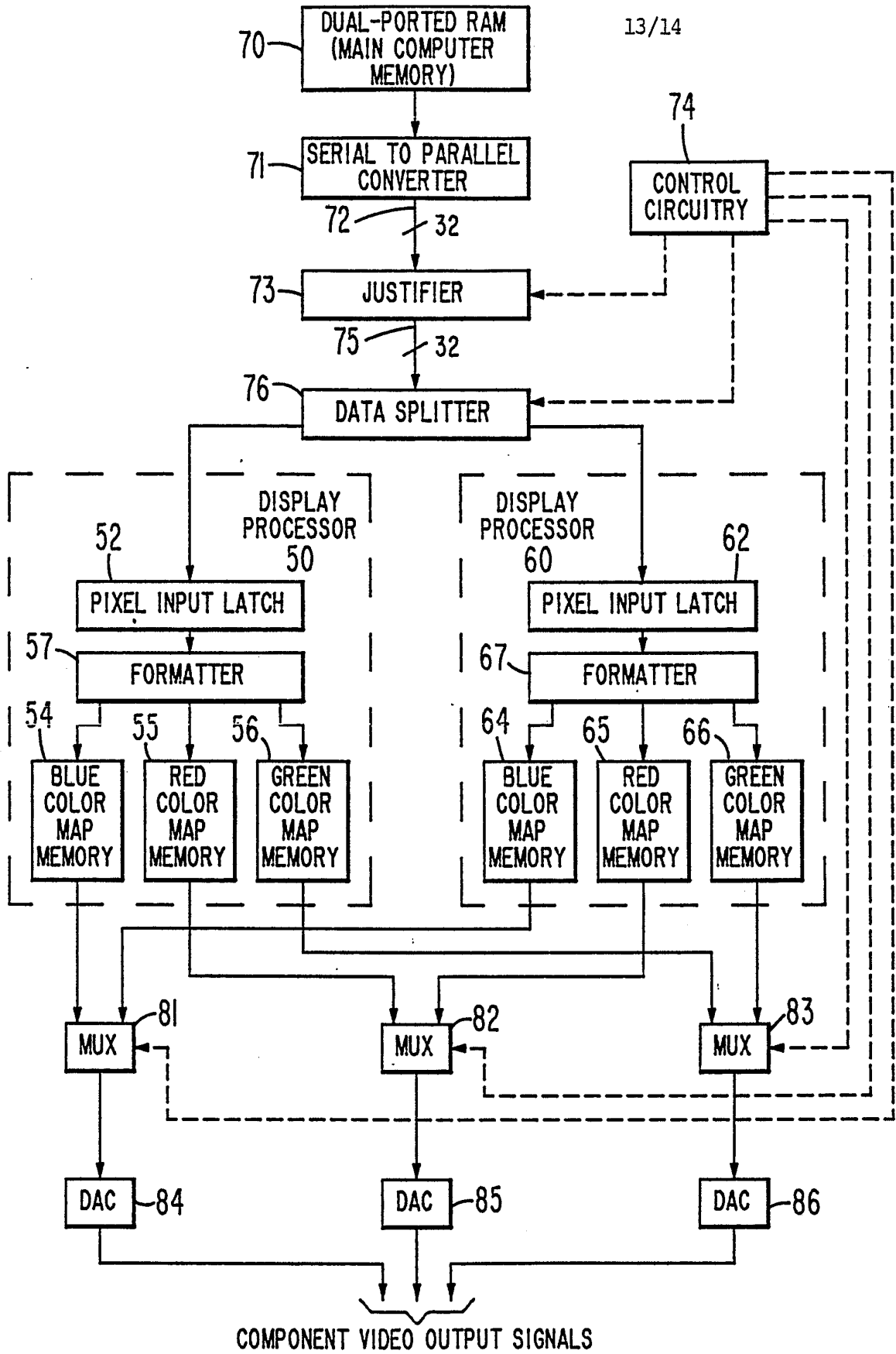


Fig. 13

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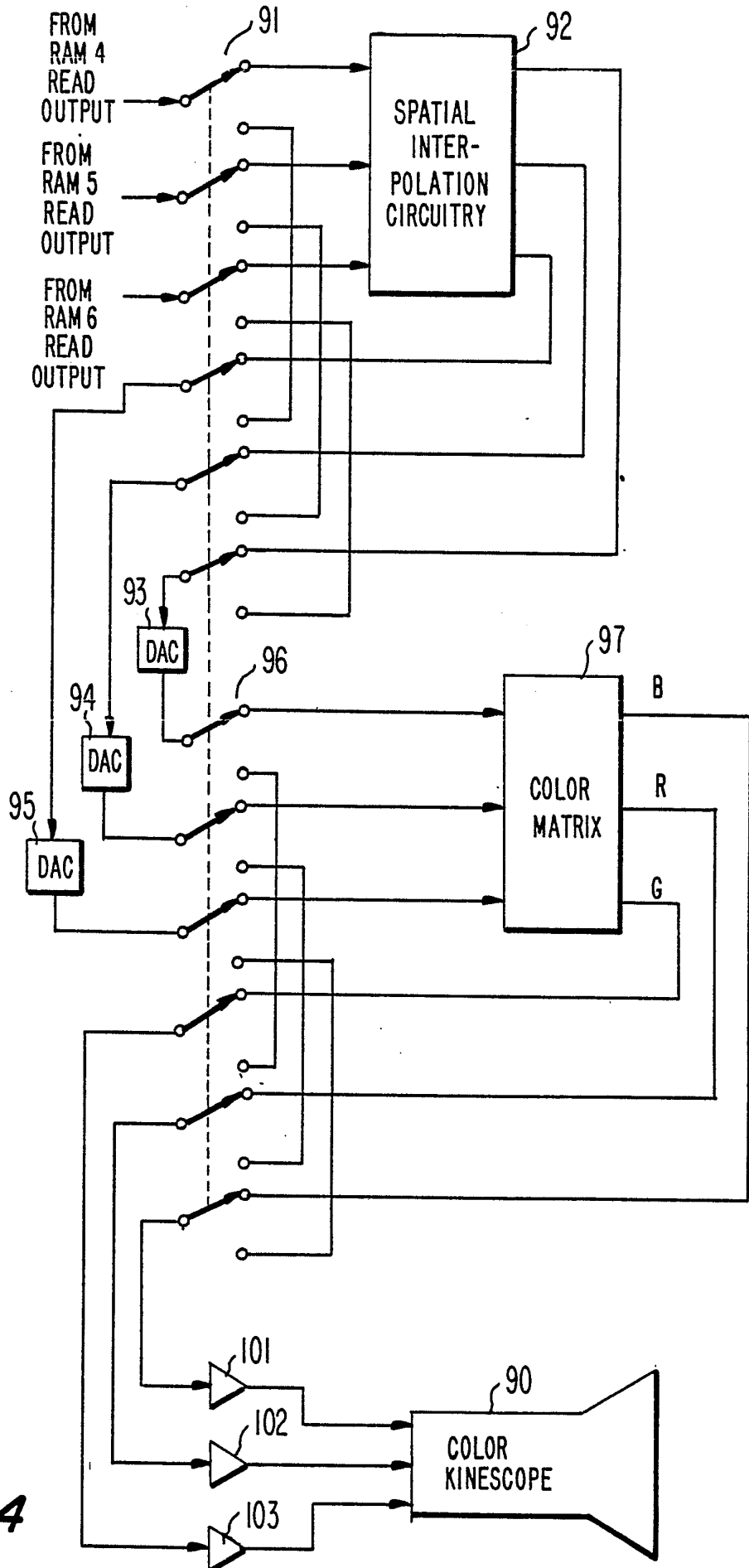



Fig.14

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 87/01390

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC ⁴ : G 09 G 1/28		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
IPC ⁴	G 09 G 1/28	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category ⁹	Citation of Document, ¹¹ with Indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
A	EP,A1, 0061213 (PHILIPS) 29 September 1982 see figure 2; abstract; page 2, lines 6-34	1
--		
A	Proceedings of the SID, volume 26, no. 2, 1985, SID, (New York, US), M.F. Cowlshaw: "Fundamental requirements for picture presentation", pages 101-107 see pages 101-107 cited in the application	1

<p>¹⁰ * Special categories of cited documents:</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"A" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	
13th October 1987	- 9 NOV 1987	
International Searching Authority	Signature of Authorized Officer	
EUROPEAN PATENT OFFICE	M. VAN MOL 	

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 87/01390 (SA 17644)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 23/10/87

The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A- 0061213	29/09/82	NL-A- 8101339	18/10/82
		JP-A- 57167087	14/10/82
		US-A- 4500875	19/02/85

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see Official Journal of the European Patent Office, No. 12/82