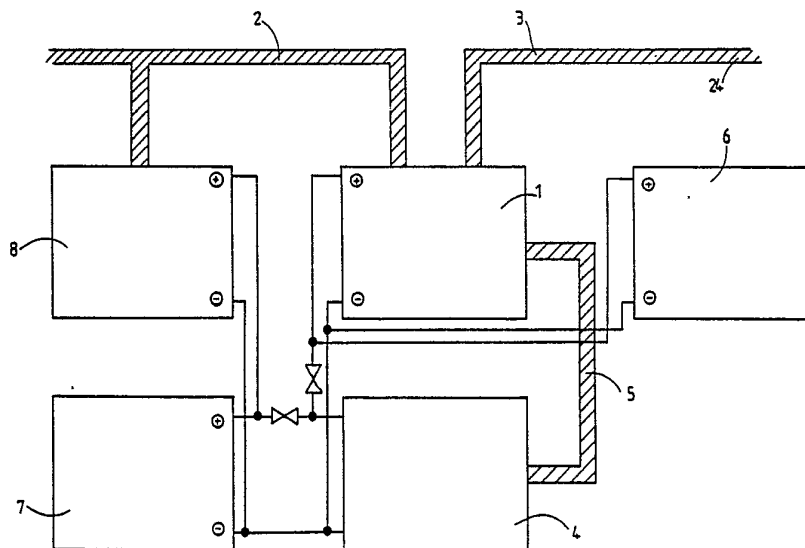




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(54) Title: STAND-BY POWER SUPPLY**(57) Abstract**

An electrical distribution means auxiliary device for providing a substitute alternating current supply when the power from a domestic mains outlet fails. The auxiliary device comprises a mains failure sensor and switch-over unit (1) which detects when the mains fail and switches over supply to an apparatus from the mains to a supply provided by an inverter (4). The inverter (4) receives power from a rechargeable battery (7) and the battery (7) is continuously recharged by a battery charger (8) whenever the mains supply is available. An emergency shut-down and alarm circuit (6) is provided to activate an alarm when failure occurs and to disable the auxiliary device when the battery (7) becomes overloaded. The auxiliary device is designed so as to provide a relatively inexpensive means for detecting when power fails and generating a substitute AC supply.

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STAND-BY POWER SUPPLY

This invention relates to an electrical distribution mains auxiliary device which is primarily used as a means of providing an alternating current supply when the power from the mains fails. The
5 object of the invention is to provide a less expensive and more efficient device for providing a substitute ac supply during mains failure, with respect to previous devices used for this purpose.

10 In accordance with the present invention there is provided an electrical distribution mains auxiliary device for an apparatus normally powered by an electric mains supply comprising:

15 monitoring means for determining when a fault condition occurs in a mains supply;

converting means for converting a direct current input to an alternating current supply which is
20 substantially equivalent to the mains supply; and

switching means responsive to said monitoring means which, in use, when a fault condition has occurred, switches the input to the apparatus from the
25 mains supply to the alternating current supply

provided by the converting means, and when the fault condition no longer exists switches the input to the apparatus back from the alternating current supply provided by the converting means to the mains supply.

5

Preferably said mains auxiliary device further comprises protection means which disables the device and activates an alarm, on detection of predetermined conditions.

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A detailed description of a preferred embodiment of the invention is provided below, by way of example only, with reference to the attached drawings, in which:

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Figure 1 is a block diagram of an auxiliary device in accordance with the invention;

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Figure 2 is a circuit diagram of a mains failure and switch over unit of the device;

Figure 3 is a circuit diagram of an inserting circuit of the device;

25

Figure 4 is a circuit diagram of a shutdown and alarm circuit of the device;

Figure 5 is a circuit diagram of an indicator circuit of the device;

30

Figure 6 is a circuit diagram of a battery charger of the device;

Figure 7 is a first waveform diagram; and

Figure 8 is a second waveform diagram.

The electrical distribution mains auxiliary device, as shown in Figure 1 comprises a mains failure and switch over unit 1, an inverting unit 4, an emergency shut down and alarm unit 6, a battery 7 and a battery charger 8. The switch over unit 1 constantly monitors the mains supply voltage on a mains input line 2. The mains voltage is then outputted from the unit 1 via an output line 3 to an apparatus (not shown) connected to a three pin socket 24. If the mains voltage is determined to be too low or too high for a set period of time the mains failure sensor and switch over unit 1 will switch the source of the output on line 3 from the mains supply 2 to an ac voltage generated by an inverting unit 4.

The inverting unit 4 converts a 12V dc voltage provided by the battery 7 to a 240V ac voltage, which is equivalent to the mains supply voltage. The AC voltage generated by the inverting unit 4 is a square wave which contains only lower frequency harmonics or, alternatively, is a sinusoidal wave comprising a number of super-imposed low frequency harmonics. A voltage waveform 500 generated by the inverting unit 4 is shown in Figure 7.

The output of the inverting unit 4 is coupled to the mains failure sensor and switch over unit 1 via a supply line 5. Power to the units 1, 4 and 6 is provided by the battery 7 which is recharged whenever the mains are operational by the battery charger 8.

The emergency shut-down and alarm unit 6 is arranged to short-circuit the input of the unit 6 whenever battery overload occurs. By short-circuiting the input power to the unit 6, the mains failure sensor and switch over unit 1 is disconnected. Current overload protection is provided by fuses as described below.

The circuit layout of the mains failure sensor and switch over unit 1 is illustrated in Figure 2. The unit 1 monitors the mains voltage using a 1VA 240V:12V transformer 10. The secondary 12V winding is connected to a bridge rectifier 11 having four diodes.

The output of the rectifier 11 is connected in series with the contact of a relay 152. The contact of the relay 152 is closed whenever power is applied to the mains failure sensor and switchover unit 1. The relay 152 disconnects the sensing circuitry, described below, of the unit 1 from the transformer when power is not supplied to the unit 1 so as to prevent any over voltage from damaging NAND gates 16, 17 and 18 of the unit. A zenerdiode 154 is provided in parallel with the output of the bridge rectifier 11 in order to provide further overvoltage protection for the gates 16, 17 and 18. When power is supplied to the unit 1, the output of the rectifier 11 is filtered by a shunt capacitor 12 and a combination of resistances 156 which give rise to a ripple voltage waveform 502, as shown in Figure 8. The decay constant associated with each period of the ripple voltage is determined by the resistors 156. The ripple voltage is applied to two potentiometers 14 and 15. The wipers of the potentiometers 14 and 15 are

adjusted so as to give signals which indicate when the ripple voltage is either too low or too high respectively. When the mains voltage is at the correct level, the wiper of potentiometer 14 supplies a "high" signal to the input of the NAND gate 16 while the wiper of potentiometer 15 supplies a "low" signal to the input of the NAND gate 17. This ensures that the output of the NAND gate 18 connected to the other two gates remains "high".

10

When, an irregularity in the mains voltage occurs and the voltage is either too high or too low for a selected period below 10 milliseconds, say 5 milliseconds, the output of the NAND gate 18 will go "low" and trigger an LM555 timer 19. The timer 19 is set up so that it will function in a monostable mode. The resistance 20 and the capacitance 21 connected to the timer 19 are such that when the timer 19 is triggered at its input T2, the timer will output a 6 volt pulse of duration 0.7 seconds minimum to two normally activated open relays 22 and 23, which upon deactivation due to zero potential will close for the duration of the pulse.

25

The duration of the pulse ends, after a minimum of 0.7 seconds, when the input T2 of the timer 19 returns to a "high" voltage. This condition will only occur when the mains voltage reverts to a normal level and is not too high or too low as determined by the mains failure sensor and switch over unit 1.

30

The unit 1 includes a delay circuit which comprises a resistor 158 connected to the input of the gate 18 and in series with a capacitor 160 and

resistors 162, which are connected in parallel and to ground. The delay circuit ensures that the pulses which trigger the timer 19 reach a "low" voltage after a certain period of time, so that if a power failure
5 does not occur but the mains voltage fluctuates between a low level and an acceptable level the timer will not be continuously triggered whenever the voltage is at the low levels, unless the mains voltage remains below the acceptable low level. This is
10 illustrated in Figure 8, where if we assume the low level to be at a certain voltage 504, if the unit 1 did not include the delay circuit then a voltage 506, resulting from the ripple voltage 502, would be inputted to the timer 19. However, with the delay
15 circuit, a voltage 508 is inputted, instead and the timer 19 does not produce any output until the ripple voltage is below the level 504 for a certain period of time. A diode 163 is provided between the output of the gate 16 and the input of the gate 18, so as to
20 ensure that the input of the gate 18 remains high for a short period of time when the output of the gate 16 becomes low.

Power to the mains failure sensor and switchover
25 unit 1 is provided by the battery 7 through a fuse 30, a thermal overload switch 166 and a manually operable on/off switch 28 in a DC supply line 101. The line 101 also supplies power to other units. The thermal overload switch 166 senses the heat generated by the
30 transistors in the inverting unit 4, described hereafter, and opens if the heat reaches an unacceptable level. A LED 168 is connected in series between two resistors 169 and 171 which are connected between a positive supply and the node 170,

respectively which is between the switch 166 and the switch 28, so as to provide an indication when the fuse 30 blows or the switch 166 is opened. An LED 29 coupled to ground and connected to the node of the switch 28 opposite the node 170, provides an indication as to when power is supplied to the failure sensor and switchover unit 1.

The relay 22, when deactivated, connects the dc supply line 101 to output line 100 which supplies power to the inverting unit 4 and the emergency shut down and alarm unit 6. A capacitor 172 is placed in parallel with the relay 22 so as to reduce noise and prevent induced spikes on a DC supply line 102. A diode 174 is placed in parallel with the relay 22 so as to ensure that the voltage at the output of the timer 19 does not exceed that of the supply line 102 by no more than 0.7 volts.

The relay 23, when deactivated, disconnects the mains supply 2 and connects the ac supply voltage generated by the inverting unit 4 to the output line 3, via a low band pass filter 174 and a fuse 27. The band pass filter prevents voltage spikes and noise from appearing on the output line 3.

The band pass filter 174 comprises two inductances 178 and 180, each connected in series with output lines 3a and 3b, each node of the inductances 178 and 180 being connected to a capacitor which is connected to ground. Resistances 182 and 184 are connected from the output lines 3a and 3b to ground, respectively, so as to discharge the capacitors. The band pass filter 176 has a 3 dB cut off point at 2.5

kHz and a 40 dB cut-off point at 20 kHz. A fuse 27, and a resistor 186 connected in series to the input of the band pass filter 176, together with a metal oxide thyristor 188 connected in parallel with the input of the band pass filter are used to prevent high current and high voltage, respectively, being supplied to an electrical apparatus, such as a computer (not shown) connected to the socket 24.

A resistor circuit 190 is connected, as shown in Figure 1, to each of the relay contacts of the relay 23. The relay circuits 190 minimize arcing across the relay contacts.

The dc supply line 101 is connected to the input of a voltage regulator 31 which provides a 6V supply for the timer 19 and the emergency shut down and alarm unit 6 on line 102. The 6V supply is also used as the positive supply (vdd) for each of the gates 16, 17 and 18.

20

The inverting unit 4, shown in Figure 3, produces a 240V, 50Hz signal from the 12V dc voltage line 10. The unit 4 includes, oscillator circuit 40 which comprises a 4 MHz quartz crystal oscillator 41. The output of the oscillator 41 is connected to five dual 4 bit binary counters 42, 43, 44, 45 and 46. The first four counters divide the frequency by a factor of 10 and the last counter 46 divides the frequency by a factor of 8 so as to produce a 50 Hz signal. A circuit 200 is connected to the binary counter 46, so as to provide an indication as to when the inverter 4 is operating. The circuit 200, connected as shown in Figure 3, comprises a transistor 202, a resistor 204 connected to the emitter of the transistor 202 and a

LED 206 connected between ground and the resistor 204. Selected outputs from the counters are inputted to a digital circuit 103 which produces two square waves at the outputs A and B which are 180° out of phase and
5 have a duty cycle of approximately 49.5%. The square waves also have a frequency of 50 Hz. The digital circuit 103 comprises three NOR gates 47, 48, 49, three NAND gates 50, 51, 52 and two inverters 53 and 54, connected together as shown.

10

The outputs A and B are each connected to standard driver circuits 60 and 61 which amplify and shape the square waves into a 10V ac signal suitable for supply to an apparatus which normally receives
15 supply from the domestic mains supply. The outputs 104 and 105 of the two driver circuits are connected to opposite ends of the primary winding of a transformer 62. Each driver circuit comprises two pnp transistor amplifier stages 63 and 64 connected via an
20 emitter follower stage 65 to a npn transistor amplifier stage 66. Three transistors operating in parallel in the stage 66 are capable of supplying a current of 25A R.M.S. A 6A diode 67 is provided at the output of each driver circuit for protection of
25 the transistors in the stage 66 against excessive transients and currents induced in the transformer 62. At the input of each driver circuit, a capacitor 68 is connected in series such that when the 50 Hz input signal ceases, the driver circuits will no longer
30 operate.

The circuit of the unit 4 includes decoupling capacitors 105 connected to the line 100 prior to the binary counters. The positive terminal 106 of the

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battery 7 is connected to the centre tap of the primary winding of the transformer 62 via three 15A fuses connected in parallel which effectively act as 45A fuse 69. A capacitor 208 is connected in parallel with the secondary winding of the transformer 62 so as to provide filtering and improve the power factor, which enables the inverting to run efficiently on low loads.

The emergency shut down and alarm unit 6, illustrated in Figure 4, comprises a battery overload circuit 70. The battery overload circuit 70 monitors the voltage on supply line 10 via a potential divider network which comprises a resistor 72 and a potentiometer 73.

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The wiper of the potentiometer 73 is set such that when the supply voltage on line 10 is below 11.1V a "high" signal is passed from the wiper through an inverting NAND gate 74 to the base of a npn transistor 75. The transistor 75 then connects the 6V supply line 102 to a relay 76. A high signal is passed from the emitter of the transistor 75 via a diode 300 to a line 302 activating the alarm 77 and switching on two LED's 304 and 306, all connected as shown in Figure 4. The LED 306 is connected to the supply line 302 by a diode 308 and is switched on after the LED 304 is switched on. The LED's 304 and 306 and the alarm 75 are all switched on before the relay 80 receives sufficient current closes contact and provided a "battery low" indicator and an "alarm on" indicator, respectively. When the contact of the relay 76 is closed the supply line 101 is short-circuited which blows the fuse 30 and disables the auxiliary device.

The alarm is activated whenever contacts of the relays 22 and 23 are opened and a switch 83, connected in series with the line 101 prior to the alarm 77, is provided so that the alarm may be switched off when
5 the switch 83 is open. However, regardless of the state of the switch 83, the alarm 77 will be activated whenever the supply line 101 has a voltage below 11.1 volts.

10 An indicator circuit 71, as shown in Figure 5 is connected to the supply line 101 so as to provide an indication by means of an LED 400 as to whether or not the battery 7 is fully charged. The circuit comprises
15 a potentiometer 402, two inverting NAND gates 404 and 406 connected in series, a transistor 410 and a resistor 412 connected to the LED 400, or connected as shown in Figure 5. The LED 400 is switched on whenever the supply on line 101 is below 13.5 volts.

20

The battery charger 8, shown in figure 5, comprises a standard circuit which receives power from the mains 2 via a 240V:18V transformer 90. The
25 secondary of the transformer 90 is connected to a bridge rectifier 91 which supplies a ripple voltage to the input of a voltage regulator network 92. The output of the network 92 is connected to a relay 96. The coil of the relay 96 is connected to the secondary
30 of the transformer 90 via diode 97 and resistor 98, a capacitor 93 being connected in parallel with the operating coil. The arrangement is such that the contacts of the relay connect the output of the network 92 to the battery 7 when the mains supply

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voltage is present. A LED 94, connected to a resistance 95 which is connected to ground, is provided to indicate when the battery charger 8 is operating.

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Many modifications will be apparent to those skilled in the art without departing from the spirit and scope of the invention.

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CLAIMS

1. An electrical distribution mains auxiliary device for an apparatus normally powered by an electric mains supply (2) comprising:

monitoring means (1) for determining when a fault condition occurs in a mains supply;

converting means (4) for converting a direct current input to an alternating current supply which is substantially equivalent to the mains supply; and

switching means (23) responsive to said monitoring means which, in use, when a fault condition has occurred, switches the input to the apparatus from the mains supply to the alternating current supply provided by the converting means, and when the fault condition no longer exists switches the input to the apparatus back from the alternating current supply provided by the converting means to the mains supply.

2. A device as claimed in claim 1 wherein the monitoring means includes rectifying means (11) for producing a rectified voltage level from the mains supply and gating means (16, 17, 18) for producing a fault signal when said rectified voltage is above or below predetermined voltage levels.

3. A device as claimed in claim 2 wherein the monitoring means includes timing means (19) responsive to output from said gating means to generate an enable signal to connect said direct current input to the converting means (4) and to activate the said

switching means (23) to switch the input of the apparatus to the output of the converting means.

4. A device as claimed in claim 3 wherein said timing means (19) functions a monostable circuit which generates said enable signal in response to a transient fault signal from the gating means.

5. A device as claimed in claim 4 wherein the switching means comprises a first relay (22) the contacts (22) of which are operable to connect or disconnect the direct current input to the converting means and a second relay (23) the contacts of which are operable to change input of the apparatus from the mains supply to the output of the converting means.

6. A device as claimed in claim 5 wherein a capacitor (172) and diode (174) are connected in parallel with the operating coil of the first relay to filter transient voltages.

7. A device as claimed in claims 5 or 6 wherein resistors (190) are coupled between the contacts of the second relay to minimize arcing.

8. A device as claimed in claim 7 including an outlet connector 24 to which the apparatus is in use connected, and wherein a low pass filter (176) is connected between the contacts of the second relay and the connector.

9. A device as claimed in claim 8 wherein said low pass filter comprises an LC filter, having a frequency response such that the 3dB down level is at about 2kHz.

10. A device as claimed in any one of claims 2 to 9 including a holding circuit (158, 160, 162) to hold the enable circuit for at least a predetermined period.

11. A device as claimed in claim 10 wherein said predetermined period is at least 0.5 seconds.

12. A device as claimed in any preceding claim wherein the converting means includes an oscillator (41) coupled to counters (42, 43, 44, 45 and 46) and counter gating means arranged to produce first and second square waves which are out of phase with one another, said square waves being coupled to opposite ends of a centre tap transformer 62, the centre tap of which is coupled to said direct current input.

13. A device as claimed in claim 12 including shaping circuits (61, 62) coupled between the counter gating means and said opposite ends of the transformer, each shaping circuit being operable to produce an output waveform which approximates half a cycle of a sinusoidal waveform.

14. Apparatus as claimed in any preceding claim wherein said direct current input is derived from a

storage battery and wherein the device includes a battery protection circuit which operates to disconnect the battery when its voltage falls below a predetermined level.

15. Apparatus as claimed in claim 14 including voltage sensing means for sensing the output voltage of the battery and arranged to activate switching means when the battery voltage falls below said predetermined level to short circuit said battery, thereby blowing a fuse in circuit therewith.

16. Apparatus as claimed in any preceding claim including an alarm circuit to generate an audible and/or visual alarm signal when said monitoring means detects a fault condition.

AMENDED CLAIMS

[received by the International Bureau on 13 January 1987 (13.01.87);
original claim 10 cancelled; claims 1-5, 11, 12 and 14 amended; other claims
unchanged (4 pages)]

1. (Amended) An electrical distribution mains auxiliary device for an apparatus normally powered by an electric mains supply (2) comprising:

monitoring means (1) for producing a fault signal when a fault condition has occurred, having rectifying means (11) for producing a rectified voltage level from the mains supply and gating means (16, 17, 18) for producing said fault signal when said rectified voltage is above or below predetermined voltage levels;

converting means (4) for converting a direct current supply to an alternating current supply which is substantially equivalent to the mains supply; and

switching means (23) responsive to said monitoring means which, in use, when said fault signal is produced, switches the input to the apparatus from the mains supply to the alternating current supply provided by the converting means, and when said fault condition no longer exists switches the input to the apparatus back from the alternating current supply provided by the converting means to the mains supply.

2. (Amended) A device as claimed in claim 1 wherein the monitoring means produces said fault signal when said fault condition has occurred for a predetermined period of time and includes delay means (158, 160, 162) for delaying a signal representative of said fault condition so that said fault signal is inhibited until said fault condition has occurred for said predetermined period of time.

3. (Amended) A device as claimed in claim 2 wherein the monitoring means includes timing means

(19) responsive to output from said gating means to generate an enable signal to connect said direct current supply to the converting means (4) and to activate the said switching means (23) to switch the input of the apparatus to the output of the converting means.

4. (Amended) A device as claimed in claim 3 wherein said timing means (19) is a monostable circuit which generates said enable signal in response to said fault signal from the gating means.

5. (Amended) A device as claimed in claim 4 wherein the switching means comprises a first relay (22) the contacts (22) of which are operable to connect or disconnect the direct current supply to the converting means and a second relay (23) the contacts of which are operable to change input of the apparatus from the mains supply to the output of the converting means.

6. A device as claimed in claim 5 wherein a capacitor (172) and diode (174) are connected in parallel with the operating coil of the first relay to filter transient voltages.

7. A device as claimed in claims 5 or 6 wherein resistors (190) are coupled between the contacts of the second relay to minimize arcing.

8. A device as claimed in claim 7 including an outlet connector (24) to which the apparatus is in use connected, and wherein a low pass filter (176) is

connected between the contacts of the second relay and the connector.

9. A device as claimed in claim 8 wherein said low pass filter comprises an LC filter, having a frequency response such that the 3dB down level is at about 2kHz.

10. (Cancelled).

11. (Amended) A device as claimed in claim 2 wherein said predetermined period is at least 0.5 seconds.

12. (Amended) A device as claimed in any preceding claim wherein the converting means includes an oscillator (41) coupled to counters (42, 43, 44, 45 and 46) and counter gating means arranged to produce first and second square waves which are out of phase with one another, said square waves being coupled to opposite ends of a centre tap transformer (62), the centre tap of which is coupled to said direct current supply.

13. A device as claimed in claim 12 including shaping circuits (61, 62) coupled between the counter gating means and said opposite ends of the transformer, each shaping circuit being operable to produce an output waveform which approximates half a cycle of a sinusoidal waveform.

14. (Amended) Apparatus as claimed in any preceding claim wherein said direct current supply is derived from a storage battery and wherein the device

includes a battery protection circuit which operates to disconnect the battery when its voltage falls below a predetermined level.

15. Apparatus as claimed in claim 14 including voltage sensing means for sensing the output voltage of the battery and arranged to activate switching means when the battery voltage falls below said predetermined level to short circuit said battery, thereby blowing a fuse in circuit therewith.

16. Apparatus as claimed in any preceding claim including an alarm circuit to generate an audible and/or visual alarm signal when said monitoring means detects a fault condition.

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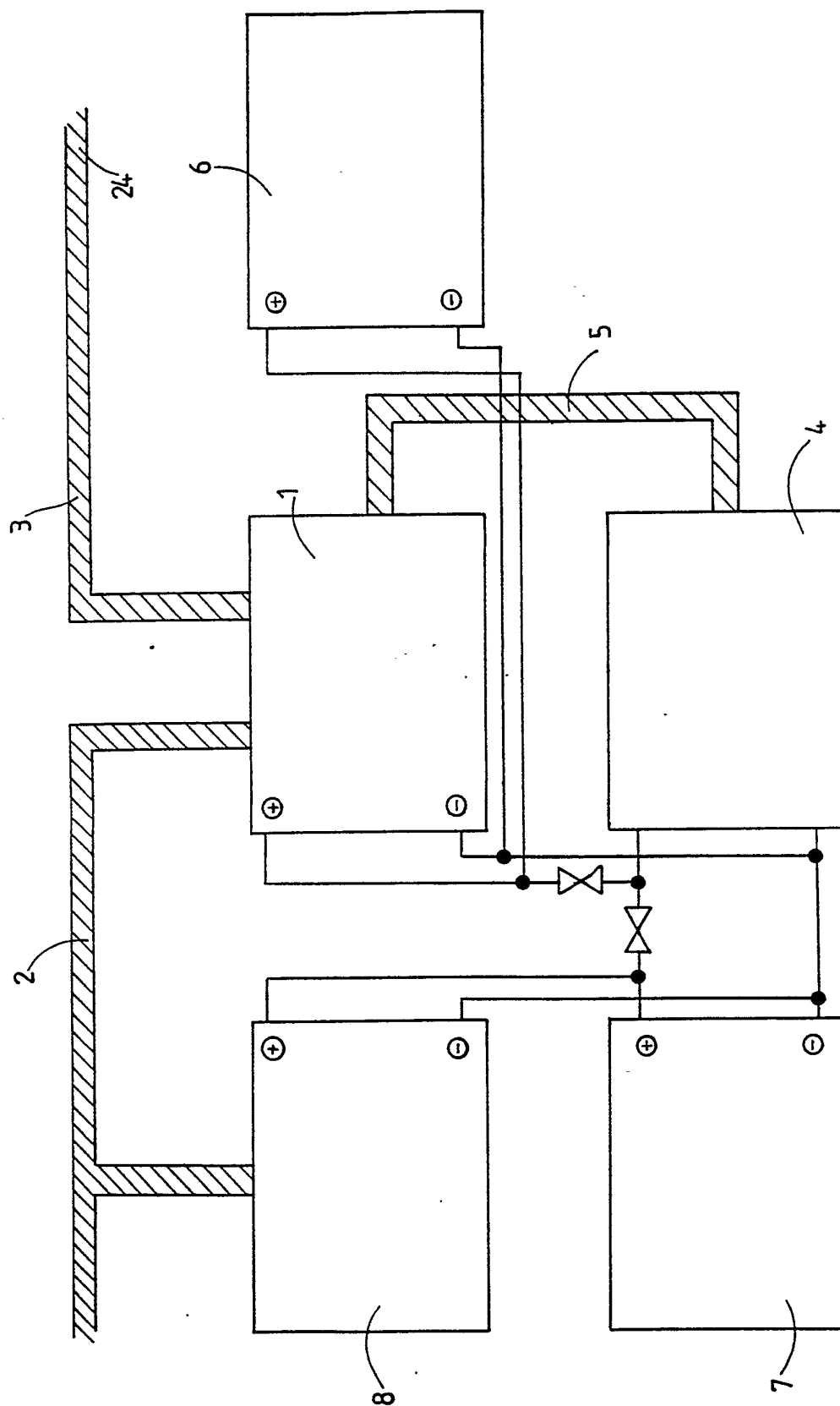


FIG 1

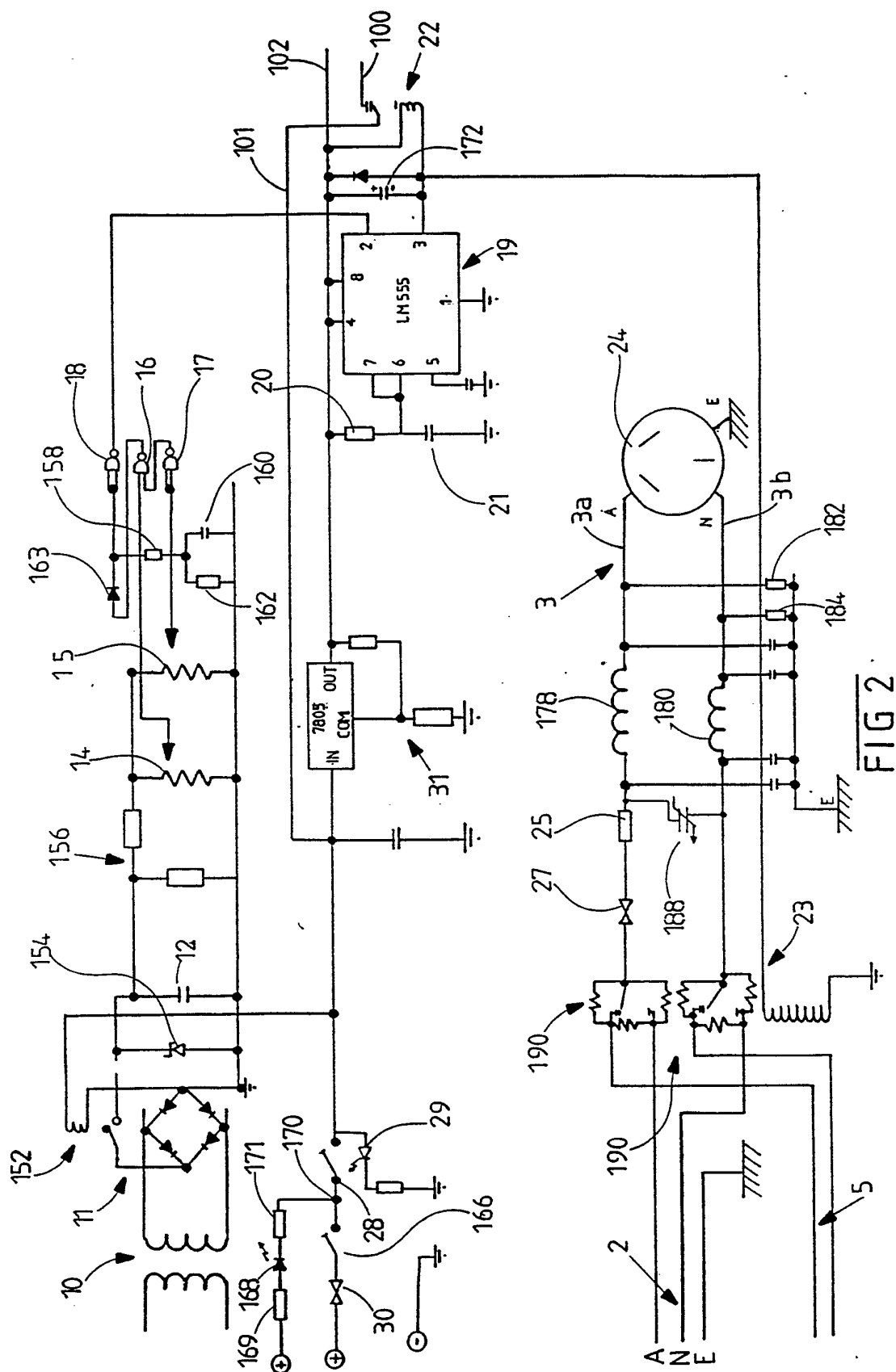


FIG 2

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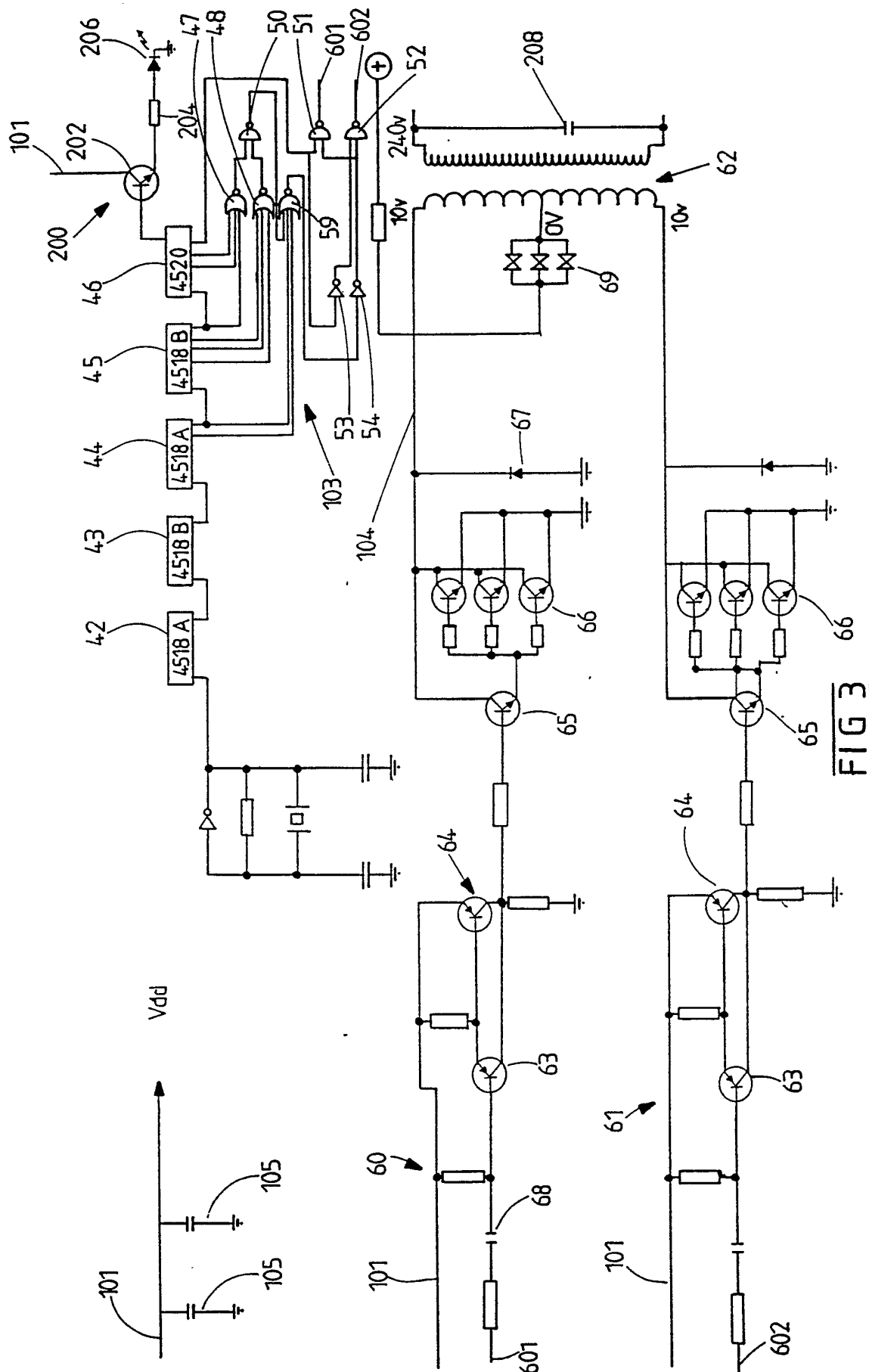


FIG 3

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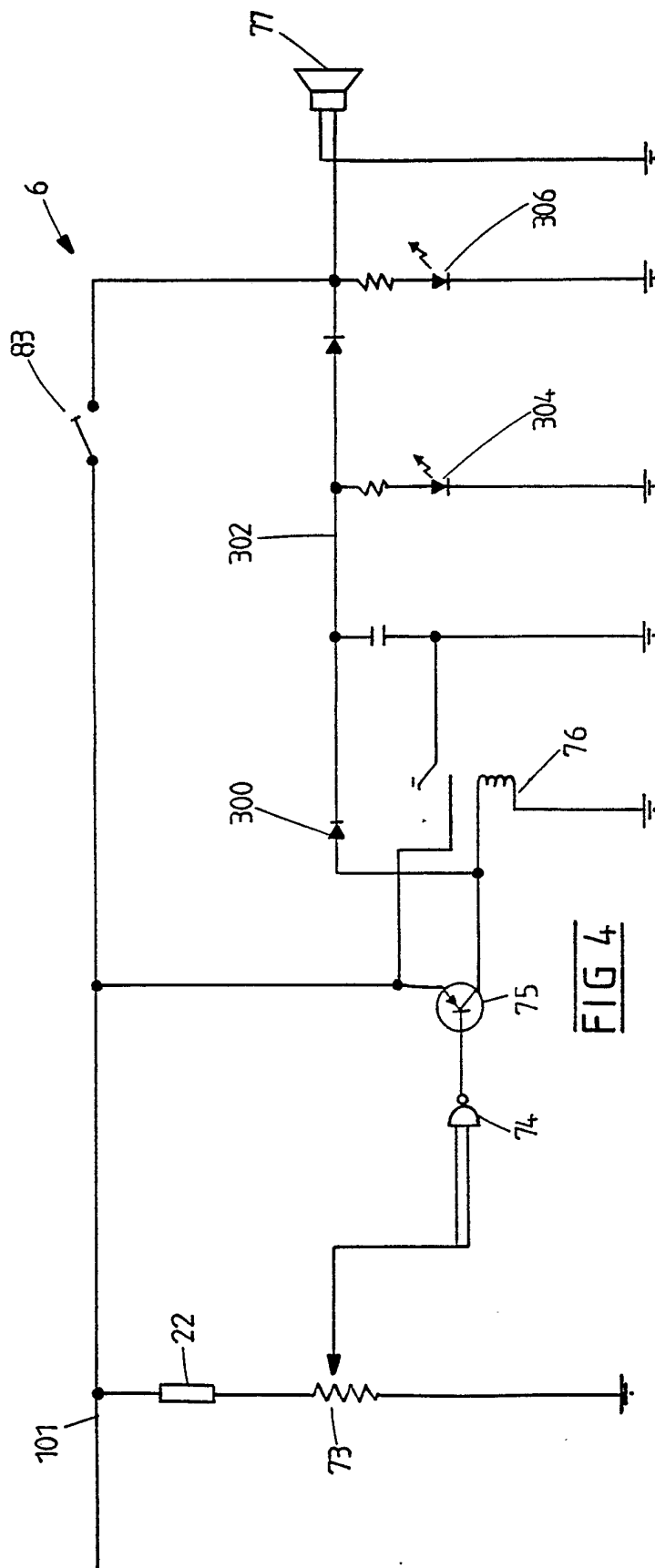


FIG 4

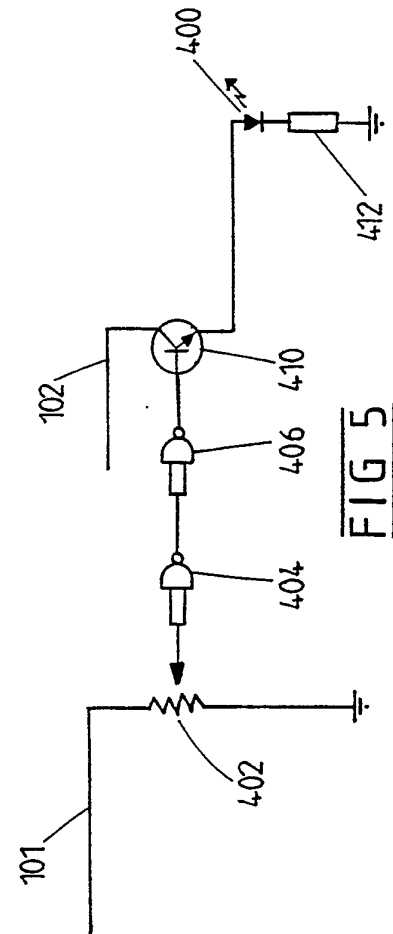
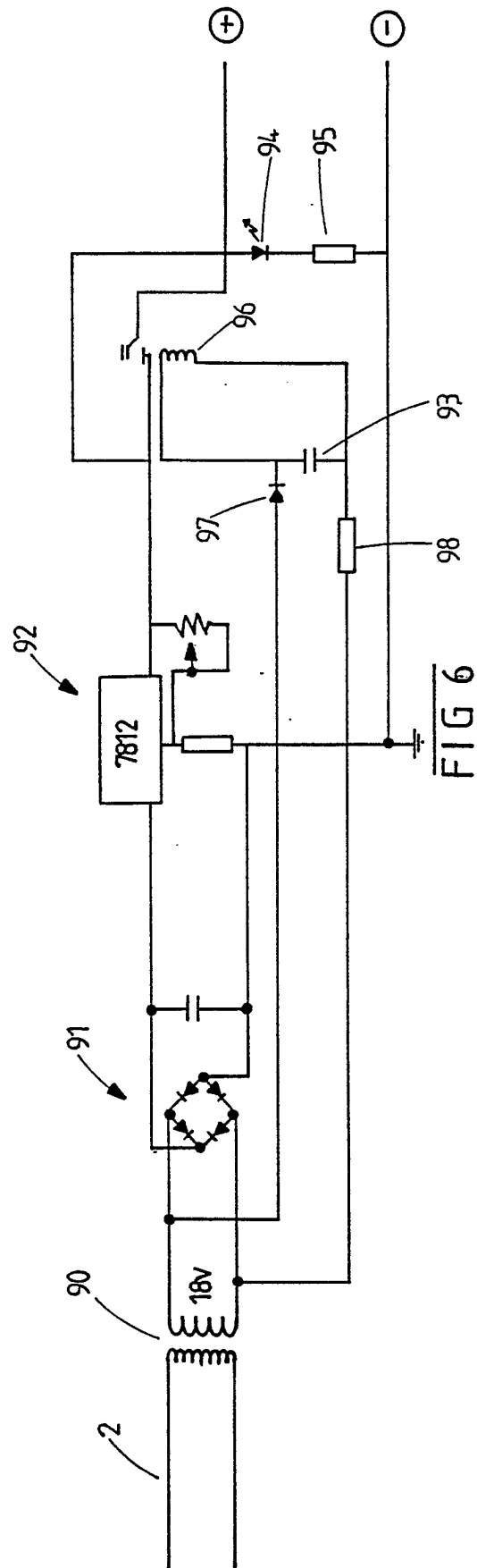


FIG 5

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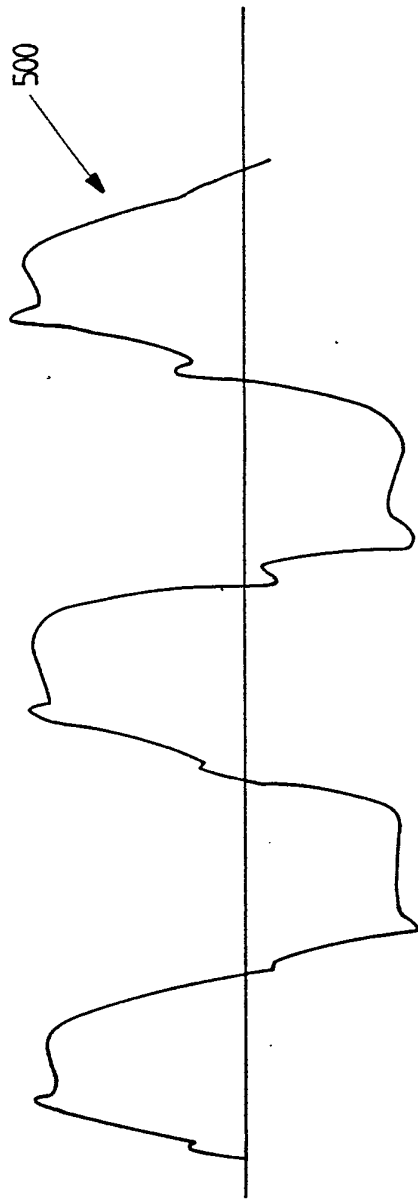


FIG 7

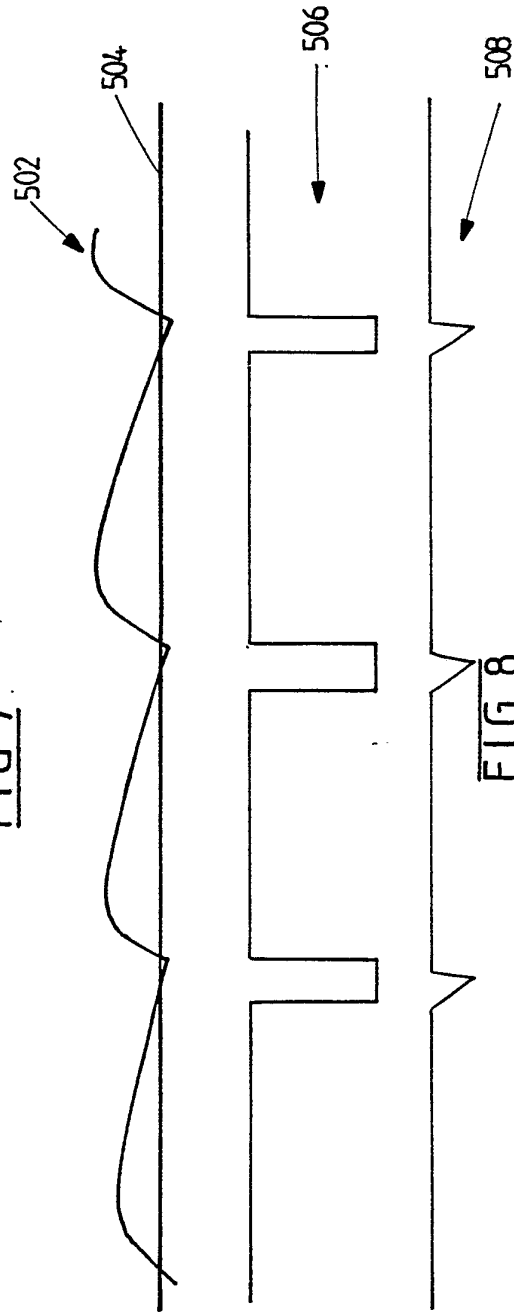


FIG 8

INTERNATIONAL SEARCH REPORT

International Application No PCT/AU 86/00210

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) According to International Patent Classification (IPC) or to both National Classification and IPC Int. Cl.⁴ H02J 9/06, 7/02																																			
II. FIELDS SEARCHED Minimum Documentation Searched⁷ <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 30%; padding: 5px;">Classification System</td> <td style="padding: 5px;">Classification Symbols</td> </tr> <tr> <td style="text-align: center; padding: 10px;">IPC</td> <td style="text-align: center; padding: 10px;">H02J 9/04, 9/06</td> </tr> </table> Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched⁸ AU: IPC as above, and H02J 7/02			Classification System	Classification Symbols	IPC	H02J 9/04, 9/06																													
Classification System	Classification Symbols																																		
IPC	H02J 9/04, 9/06																																		
III. DOCUMENTS CONSIDERED TO BE RELEVANT⁹ <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 10%; padding: 5px;">Category⁹</th> <th style="width: 70%; padding: 5px;">Citation of Document,¹¹ with indication, where appropriate, of the relevant passages¹²</th> <th style="width: 20%; padding: 5px;">Relevant to Claim No.¹³</th> </tr> <tr> <td style="text-align: center; padding: 5px;">X,Y</td> <td style="padding: 5px;">US,A, 4010381 (FICKENSCHER & SCUDERI) 1 March 1977 (01.03.77)</td> <td style="text-align: center; padding: 5px;">(1-3,12,14)</td> </tr> <tr> <td style="text-align: center; padding: 5px;">X</td> <td style="padding: 5px;">US,A, 4366389 (HUSSEY) 28 December 1982 (28.12.82)</td> <td style="text-align: center; padding: 5px;">(1-3)</td> </tr> <tr> <td style="text-align: center; padding: 5px;">X,Y</td> <td style="padding: 5px;">US,A, 4473756 (BRIGDEN & SHATTO) 25 September 1984 (25.09.84)</td> <td style="text-align: center; padding: 5px;">(1,2,12)</td> </tr> <tr> <td style="text-align: center; padding: 5px;">X</td> <td style="padding: 5px;">US,A, 3229111 (SCHUMACHER et al) 11 January 1966 (11.01.66)</td> <td style="text-align: center; padding: 5px;">(1,2)</td> </tr> <tr> <td style="text-align: center; padding: 5px;">X</td> <td style="padding: 5px;">CH,A, 338230 (LICENTIA PATENT-VERWALTUNGS-GmbH) 30 June 1959 (30.06.59)</td> <td style="text-align: center; padding: 5px;">(1,2)</td> </tr> <tr> <td style="text-align: center; padding: 5px;">Y</td> <td style="padding: 5px;">AU,B, 115663 (2444/41) (STANDARD TELEPHONES & CABLES PTY LIMITED) 4 August 1942 (04.08.42)</td> <td style="text-align: center; padding: 5px;">(1-3,12)</td> </tr> <tr> <td style="text-align: center; padding: 5px;">X,Y</td> <td style="padding: 5px;">Wireless World, Vol.87, No.1548, issued September 1981 (IPC Electrical-Electronic Ltd, Surrey) A.K.H. Miller, "Simple 100W Inverter", pp. 82-83</td> <td style="text-align: center; padding: 5px;">(1,12)</td> </tr> <tr> <td style="text-align: center; padding: 5px;">X</td> <td style="padding: 5px;">FR,A, 2549652 (HENNERE) 25 January 1985 (25.01.85)</td> <td style="text-align: center; padding: 5px;">(1,16)</td> </tr> <tr> <td style="text-align: center; padding: 5px;">X</td> <td style="padding: 5px;">DE,A, 1956486 (STANDARD ELEKTRIK LORENZ AG) 5 August 1971 (05.08.71)</td> <td style="text-align: center; padding: 5px;">(1)</td> </tr> <tr> <td colspan="3" style="text-align: right; padding: 10px;">(continued)</td> </tr> </table> ⁹ Special categories of cited documents: ¹⁰ "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family			Category ⁹	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³	X,Y	US,A, 4010381 (FICKENSCHER & SCUDERI) 1 March 1977 (01.03.77)	(1-3,12,14)	X	US,A, 4366389 (HUSSEY) 28 December 1982 (28.12.82)	(1-3)	X,Y	US,A, 4473756 (BRIGDEN & SHATTO) 25 September 1984 (25.09.84)	(1,2,12)	X	US,A, 3229111 (SCHUMACHER et al) 11 January 1966 (11.01.66)	(1,2)	X	CH,A, 338230 (LICENTIA PATENT-VERWALTUNGS-GmbH) 30 June 1959 (30.06.59)	(1,2)	Y	AU,B, 115663 (2444/41) (STANDARD TELEPHONES & CABLES PTY LIMITED) 4 August 1942 (04.08.42)	(1-3,12)	X,Y	Wireless World, Vol.87, No.1548, issued September 1981 (IPC Electrical-Electronic Ltd, Surrey) A.K.H. Miller, "Simple 100W Inverter", pp. 82-83	(1,12)	X	FR,A, 2549652 (HENNERE) 25 January 1985 (25.01.85)	(1,16)	X	DE,A, 1956486 (STANDARD ELEKTRIK LORENZ AG) 5 August 1971 (05.08.71)	(1)	(continued)		
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IV. CERTIFICATION <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; padding: 5px;"> Date of the Actual Completion of the International Search 3 November 1986 (03.11.86) </td> <td style="width: 50%; padding: 5px;"> Date of Mailing of this International Search Report (13-11-86) 13 NOVEMBER 1986 </td> </tr> <tr> <td style="padding: 5px;"> International Searching Authority Australian Patent Office </td> <td style="padding: 5px;"> Signature of Authorized Officer N.C. PETERSEN </td> </tr> </table>			Date of the Actual Completion of the International Search 3 November 1986 (03.11.86)	Date of Mailing of this International Search Report (13-11-86) 13 NOVEMBER 1986	International Searching Authority Australian Patent Office	Signature of Authorized Officer N.C. PETERSEN																													
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International Searching Authority Australian Patent Office	Signature of Authorized Officer N.C. PETERSEN																																		

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

X	DE,A, 2014680 (ATELIERS DE CONSTRUCTIONS ELECTRIQUES DE CHARLEROI) 15 October 1970 (15.10.70)	(1)
X	DE,A, 3246930 (LICENTIA PATENT-VERWALTUNGS-GmbH) 20 June 1984 (20.06.84)	(1)
X	CH,A, 604406 (ROVO AG) 15 September 1978 (15.09.78)	(1)
X	DE,B, 1237666 (BLESSING-ETRA BELGE S.A.) 30 March 1967 (30.03.67)	(1)

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE ¹

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claim numbers because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claim numbers because they are dependent claims and are not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING ²

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

- ☐ The additional search fees were accompanied by applicant's protest.
☐ No protest accompanied the payment of additional search fees.

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON
INTERNATIONAL APPLICATION NO. PCT/AU 86/00210

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Members			
US 4010381	AU 13187/76	BE 841009	BR 7602392		
	CA 1053753	CH 615786	CE 26180892		
	ES 447269	FR 2309065	GB 1487049		
	IL 49445	IT 1059912	JP 51130835		
	NL 7604353	SE 7604335			
US 4366389	CA 1169124				
US 4473756	EP 132022				
DE 2014680	BE 730850	FR 2042217	NL 7004655		

END OF ANNEX