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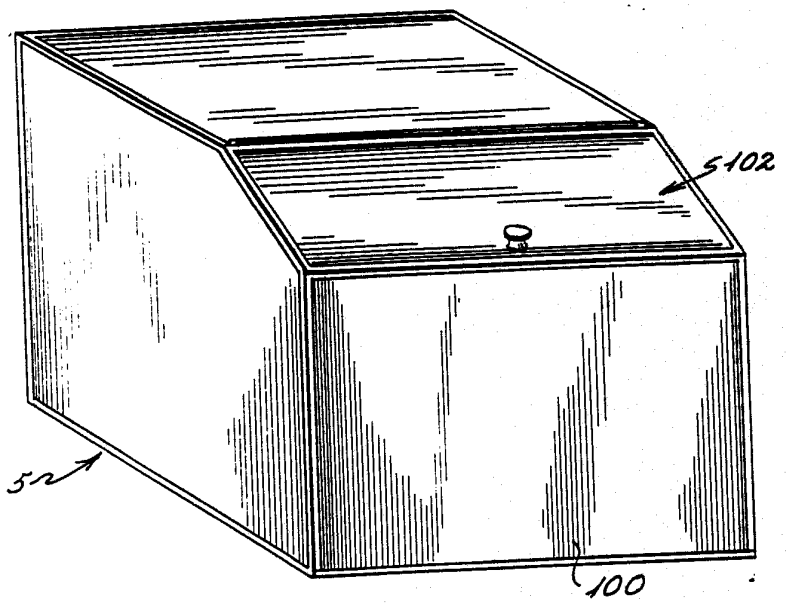

(57) Abstract

An integrated, multimode FM radio system including a common reference clock (4) providing synchronized digital signal processing for both transmission (1) and reception (2). The radio system according to the present invention also includes a novel digital frequency synthesizer (3, 8, 9, 43, 44), a digital FM demodulator (17) and a digital FM modulator (16) which together provide improved FM modulation and demodulation fidelity thereby assuring interoperation with other radios in all analog and digital modulation formats, improved spectral purity and faster channel switching speed for the frequency hopping synthesizer (71), improved reliability through reduction in complexity, and reduction of radio production cost, including reduction in testing and adjustments needed for certification to radio emission standards.

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DIGITAL CIRCUIT FOR FREQUENCY MODULATION AND CARRIER SYNTHESIS IN A DIGITAL RADIO SYSTEM

RELATED APPLICATION

The present application for U.S. Patent is a continuation-in-part of Application Serial No. 07/295,270, filed on January 10, 1989.

FIELD OF THE INVENTION

The present invention relates to radio modulation and demodulation for application to two-way radio. In particular, the invention relates to waveform and carrier synthesis for radio systems having the capacity to provide a wide variety of analog and digital information formats using FM modulation, including both conventional single-carrier FM modulation and fast frequency hopping amongst a plurality of alternate carrier frequencies.

BACKGROUND OF THE INVENTION

Typical digital frequency synthesis techniques, as shown in references 1 through 3, use a digital accumulator to synthesize a selected numerical sequence representing a desired signal phase ramp, and use various digital phase comparison means to phase lock a voltage tunable oscillator (VTO) to the digital ramp. These techniques produce unacceptable spurious frequency lines in the synthesizer output spectrum; these lines are caused by VTO frequency modulation associated with timing and amplitude quantization in the digital logic. The frequency sideband spurs are variable with synthesizer output frequency, and correspond to intermodulation products of the clock frequency and the desired output frequency. In these systems the loop filter bandwidth must be reduced to a value much smaller than the frequency step size in order to attenuate these noise components and the ability of the

loop to track intended modulation and frequency hopping is thereby impaired.

A second related synthesis method is the dual modulus "Fractional N" indirect synthesizer exemplified by the description in Reference 3 through 6. In the prior art scheme of Reference 3 a phase comparison frequency is used that is several octaves higher than the frequency resolution step size, and a constant division ratio N is used in the VTO divider to synthesize any frequency that is an exact harmonic of the comparison frequency. The comparison frequency is programmable to expand the number of harmonic frequencies that can be generated. For all other frequencies the synthesizer is required to interpolate between two harmonics of the comparison frequency using dual divider modulii N and N-1 in a series of cycles of the comparison frequency. However, each transition of the divide ratio produces a phase jump in the phase comparator output signal that is equivalent to a complete RF cycle, and the spectrum of this disturbance sequence appears as spurious sidebands of the synthesized frequency. Reference 5 shows how to reduce the power level of these spurious frequencies by means of an elaborate compensation network, but the reference also shows that careful circuit alignment is necessary to achieve useful cancellation.

A third related scheme is the direct digital synthesizer (DDS) exemplified by References 7 and 8. Like the first related scheme, this scheme also uses a digital phase ramp accumulator to synthesize the desired frequency. However, in this case the digital phase sequence is converted directly to a sinusoidal waveform by means of a Sine/Cosine table, a digital-to-analog converter (DAC), and a low pass filter. The maximum output frequency for these systems is about 1/3 of the digital clock speed, to avoid frequency alias signals at the output of the loop filter. Reference 8 shows that DDS

synthesizers also produce spurious sidebands at harmonics of a phantom waveform that corresponds to the replication error associated with signal quantization in the SINE tabulation and DAC. Phase quantization restricts the frequencies that are exactly replicated by Sine/Cosine Tabulation to harmonics of the frequency step

$$DF = f_0/M, \quad (1)$$

where f_0 is the clock frequency and M is the number of phase steps per cycle. For other frequencies, the intended phase ramp is quantized to the M available phase states of the Sine/Cosine table; the resulting phase error sequence is a sawtooth of magnitude π/M with a repetition frequency

$$f_n = f_0 f_d/DF = Mf_d , \quad (2)$$

where f_d is the frequency difference between the synthesized frequency and the closest harmonic of DF. The error sawtooth is rich in harmonics and all of these appear in the broadband synthesizer output. Elimination of these spectral lines requires use of high precision sine tabulations and DAC converters. Expansion of the synthesis bandwidth by frequency multiplication raises the power of the spurious sidebands by the square of the multiplication ratio, thereby further increasing the required precision of the DAC and SINE tabulations in the DDS.

Many radio systems are required to alternately operate carrying voice and data traffic using a variety of modulation formats requiring both analog/FM and binary/FM modulators. Audio squelch circuits of several types are required to recognize the several forms of voice traffic and to disable the audio sound during intervals containing no voice traffic. Insensitive squelch circuits can result in missed voice messages and overly sensitive squelch circuits create annoying sound bursts.

Improvement in accuracy and speed of response for all forms of squelch circuits is of value to users. All of the above requirements impact radio complexity and cost and thereby restrict widespread application of high performance features.

Conventional analog radios have several undesirable performance characteristics associated with component variability and with affordable production tolerances. These undesirable characteristics are obviated in the subject invention by precise numerical control of all technical parameters associated with carrier frequency synthesis, modulation, demodulation, baseband filterings, squelch and synchronization.

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SUMMARY OF THE INVENTION

The present invention improves the technical performance of the radio in the following specific areas:

1. The digital modulator and demodulator circuits produce exact and invariable waveform responses so that the demodulated signal is free from anomalous center-frequency bias, distortion, and deviation scaling errors that are common for analog modulation systems.

2. The improved accuracy of the digital modulation/demodulation system permits the use of binary-FM waveforms with more tightly constrained bandwidth than is available with existing radio systems.

3. All of the digital signal processing operations for carrier frequency synthesis, modulation, demodulation, and baseband processing are performed in a single inexpensive VLSI gate array chip.

4. The digital processing circuits effectively control the emission spectrum of the radio, this prevents variability of analog circuit components for influencing the performance of the radio in key areas associated with radio interoperability and compliance with emission specifications. In most emission compliance areas and link performance related areas the radio performance is governed by digital number sequences and not by factory tuning alignments, so producibility is improved and factory acceptance testing is simplified.

5. The novel frequency synthesizer provides improved frequency resolution, improved spectral purity,

and faster frequency switching than is available with prior-art frequency synthesizers.

6. The digital synthesizer prevents intermodulation of the clock frequency and the synthesized frequency, thereby eliminating spurious line spectra associated with prior art direct digital synthesizers (DDS).

7. An alternative embodiment of the digital synthesizer reduces the signal dynamic range of the system at the synthesizer digital to analog converter (DAC), thereby reducing the synthesizer quantization noise for equivalent bit precision in the digital to analog conversion process or for a given noise performance, reducing the required bit precision, thereby permitting the use of a DAC requiring as little as one bit of precision.

8. A second alternative embodiment of the digital synthesizer includes a circuit which nulls certain intermodulation beat frequencies in the digital frequency synthesizer generated by intermodulation of harmonic frequencies of the clock and carrier signals.

9. Yet another alternative embodiment of the digital synthesizer provides for the injection of a digital dither signal into the digital input to the DAC wherein the dither signal is further filtered to suppress periodic components of the error signal associated with bit field truncation.

10. Harmonics of the clock frequency and controlled frequency in the digital synthesizer are isolated from the synthesizer output frequency, by means of a phase lock loop; the tuning bandwidth is thereby extended threefold as compared to prior art DDS synthesizers.

11. The digital baseband processor achieves significant improvement in squelch reliability and symbol synchronization accuracy as compared to conventional

radios, permitting independent hop to hop operation for frequency-hopped carrier modes of operation.

In sum, the invention combines the functions of channel frequency selection and frequency modulation (FM) into a single, high resolution, digital frequency synthesis circuit in a manner that is adaptable to all analog and digital voice and data FM transmission modes in common use. The available transmission modes include fast frequency hopping; in this mode great importance is given to achieving the highest possible frequency switching speed.

BRIEF DESCRIPTION OF THE DRAWINGS

These and further features of the present invention will be better understood by reading the following detailed description, taken together with the drawing, wherein:

Fig. 1 is a block diagram of one embodiment of the present invention;

Fig. 2 is a more detailed block diagram of the Difference Phase Accumulator (DPA), Phase Ramp Accumulator (PRA), and Phase Lock Loop Filter (PLLF) according to the embodiment of Fig. 1;

Fig. 2A is a truth table for the "E" signal;

Fig. 2B is a truth table for the "M" signal according to one embodiment of the present invention;

Fig. 3A is a graph of the error signal from the Difference Phase Accumulator (DPA);

Fig. 3B is a graph of pulses relating to the Difference Phase Accumulator (DPA);

Fig. 3C is a graph of jitter compensation pulses for one mode of operation of the present invention;

Fig. 4 is a more detailed block diagram of the Modulator according to the embodiment of Fig. 1;

Fig. 5 is a more detailed block diagram of the Demodulator/Squelch/Delay Buffer according to the embodiment of Fig. 1;

Figs. 7A and 7B are graphs of the impulse responses to the smoothing filter of the present invention with the filter as a median filter and as a centroid filter, respectively.

Fig. 8 is a block diagram of one embodiment of the frequency synthesizer of the present invention.

Fig. 9 is a block diagram of a second embodiment of the frequency synthesizer of the present invention including various processing circuits for improved noise performance.

Fig. 10A is a graph of the composite output signal from the linear summing amplifier.

Fig. 10B is a graph of the asynchronous "V" input to the linear summing amplifier.

Fig. 10C is a graph of the synchronous input to the linear summing amplifier.

Fig. 11 is a block diagram of one embodiment of the enhancement combination of the Digital Signal Compression Filter (DSCF), the Error-Recursive Signal Quantizer (ERSQ), and the Analog Signal Equalization Filter (ASEF) of the present invention.

Fig. 12 is an embodiment of the enhanced synthesizer using the Error Recursive Signal Quantizer (ERSQ) and one bit-quantization with Automatic Ballance Control.

Fig. 12A is a block diagram of the ERSQ circuit of the present invention showing the bit breakdown of the input and feedback signals thereof.

Fig. 13 is a block diagram of the Dither Generator (DG) of the present invention.

Fig. 14 is a block diagram of the Adaptive Balance Control (ABC) circuit of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 shows a block diagram of one embodiment of a radio according to the present invention comprising a two-way FM voice radio operating in the mobile radio band

30-88 MHz. The present invention minimizes the use of analog circuits in order to obtain highly consistent radio transmission quality and maximum production economy. Analog circuits are used only for audio input-output circuits 40 which are required for interface with conventional sound projectors 42 (speakers) and microphone 41. Immediately beyond the analog interface circuits 40, ADC and DAC circuits 30 convert between the analog and digital signal domain. Thereafter the voiceband signals are handled in digitized form for all filtering, modulation and demodulation operations.

The RF/IF portion of the radio also employs analog circuits for signal amplification and tuning. The receiver related circuits 2, 5, 6 and the transmission related circuits 1, 35 are similar to designs known in the art for RF and IF portions of frequency hopping radios, including electronic bandswitching controls for RF filters in RCVR 2 and the XMTR 1. Tuneable filters are included to prevent saturation or desensitization of the receivers when in close proximity to operating transmitters. The band switching control 37 for the RF filters and other frequency switched components are provided by a control mapping memory 36 that converts channel code commands 38 to appropriate tuning selection commands 37. For other applications, the channel code can be randomized at predetermined instants to transmit a frequency hopped waveform. This is accomplished by means of a time-of-day clock 70 which designates a unique time code 73 for each frequency dwell interval, and a random number generator 71 which transforms the time code 73 into a corresponding channel code 38.

A single voltage-tuneable varactor oscillator (VTO) 3, implemented with known designs, (see Reference 6) is used as the RF frequency source for both transmitting and receiving. The VTO operates at a power level that is sufficient for use as the first local oscillator during

receive operation; and for transmission, the VTO output is amplified and filtered in transmitter 1 and conducted to the antenna via T/R switch 35. To confine the required tuning range of the VTO to the essential 30-88 MHz band needed for transmission, the heterodyning reference frequency for reception is above the carrier at the low end of the band, and below the carrier at the high end of the band. Carrier frequency tuning over approximately ± 10% of the VTO center frequency is achieved by means of an analog control signal 10 appearing at the output of a filter 9 in a feedback control loop. The VTO center frequency is selectable over the required 30-88 MHz frequency coverage using a set of switchable inductor tuning elements selected by control bus 37. For transmission, the feedback control loop, comprising elements 8, 14, and 9, superimposes a frequency modulating signal on VTO control signal 10 in exact accordance with a digital sequence 132 provided by the phase ramp accumulator (PRA) 13, providing the intelligence to be transmitted.

In the preferred architecture for the invention, shown in Figure 1, a single 12.8 MHz reference oscillator 4 controls all the timing and frequency synthesis, including the generation of a fixed second local oscillator (LO) 401. Precise timing derived from reference oscillator 4 governs: the FM deviation and modulating waveform of signal 11 from the modulator 16; the deviation sensitivity, center frequency, distortion, of the demodulator 17; and the gain, bandwidth, shape factor and detection thresholds for baseband filtering operations 22, 23, 24 and 27. As a result of the common clocking scheme, all modulation and demodulation parameters, as well as the carrier center frequency are controlled to the same precision as the frequency accuracy of the reference oscillator 4, and no factory alignments or periodic calibrations are required to maintain

modulation emission specifications or demodulation performance specifications. Adequate frequency accuracy for all these functions is obtainable with a single low cost crystal resonator within reference oscillator 4.

The 12.8 MHz reference signal is used directly in mixer 6 as the second local oscillator (LO) 401 for reception, and as sampling frequency 43 for digital synthesizer circuits 13, 14 during both transmission and reception. Divider 12 divides the reference frequency by a factor 32 to obtain a 400 kHz sampling clock signal 121 for wideband digital signal processing circuits 162, 163 in the modulator 16, circuits 172, 179 in demodulator 17, and symbol synchronizer 26. Divider 12 further selectively divides the clock frequency 121 by factors of 25 and 20 to obtain a both 16kHz and 20kHz clock lines 122 for digital signal processing circuits 21 and 162. The 16kHz clock is also used by digital baseband circuits 22, 23 and 30. All the clock frequency scaling circuits and the digital signal processing circuits shown in Figure 1 are internal to a single digital integrated circuit. This is an important advantage with respect to reducing the need for metal enclosures for circuit shielding; elimination of most circuit board wiring carrying digital signals reduces radiation of these signals into sensitive RF and IF circuits that are in close proximity.

In the preferred embodiment, a single CMOS gate array VLSI device combines all the digital circuits associated with the functions of the synthesizer, modulator, demodulator and baseband circuits. All low speed signal processing stages are implemented with bit-serial arithmetic circuits, as illustrated by reference 10, to minimize logic complexity and minimize the cost of the VLSI device. Using available CMOS gate array VLSI technology and bit-serial arithmetic, design implementation for the individual signal processing

stages, excluding ROM memory in code converter 36 and modulator 16, discussed below, has a complexity of fewer than 20,000 gates and a total power dissipation less than 1/4 watt. To achieve an N-fold reduction in circuit complexity, the logic circuit for arithmetic requires an N-fold increase in clock speed. This tradeoff favors the bit-serial design for this application because most of the required signal processing operations involve sampling rates of 16 kHz or 400 kHz, well below the speed capacity of currently available CMOS gate array integrated circuits. Alternative designs under the invention could employ a VLSI gate array composed of standard parallel arithmetic stages or a software controlled signal processing computer integrated circuit.

THE FREQUENCY SYNTHESIS

The subject invention includes a novel frequency synthesis means that provides a unique combination of fast frequency switching, high spectral purity, low quantization noise, fine frequency resolution, and simple circuitry. Background related to the digital PLL techniques of the frequency synthesis according to the invention is provided in References 1 through 3.

The frequency synthesizer according to the present invention shown in more detail in Fig. 2, uses a digital accumulator 137 to synthesize a numerical sequence corresponding to the desired carrier phase, and uses a digital difference phase accumulator 14 to derive the loop error signal. The present invention further includes filter 91, DAC 93, jitter synchronizer 81, adder 92, counter 141, and Logic 143 to derive an analog error signal for control of the VTO 3 that is virtually free of spurious line spectra and unwanted modulation products.

In a further embodiment, shown in Fig. 9 and described herein, a digital signal compression filter (DSCF) 21 is integrated into the frequency synthesizer in

combination with a compensating analog signal equalization filter (ASEF) 22. This filter combination functions to reduce the dynamic range of the input signal to the DAC 93, thereby reducing the resultant quantization noise produced by the frequency synthesizer or allowing for the use of a DAC requiring fewer bits of precision. Additionally, or alternatively, an Error-Recursive Signal Quantizer (ERSQ) 400 is provided to compress the filtered or unfiltered signal to the bit field of the DAC in a manner whereby quantization residue is accumulated and summed with unquantized signal at subsequent quantization cycles. Optionally, in another alternative embodiment an Adaptive Balance Control (ABC) 29 is employed to null certain intermodulation frequencies generated by the frequency synthesizer to improve noise performance. In yet another alternative embodiment, a digital Dither Generator (DG) 27 is utilized to generate and inject a digital dither signal into the DAC input signal, providing supression of periodic components of error signal associated with bit-field truncation at the DAC. The capacity of the present invention for fine frequency resolution in combination with low noise output is exploited to combine carrier frequency synthesis and frequency modulation operations into a single frequency synthesis operation.

The synthesizer of Fig. 2 uses digital logic in the phase ramp accumulator (PRA) 13 to create a numerical ramp sequence bus 132 that represents the intended signal phase at precisely periodic sampling instants, which are established by the reference oscillator 4. The difference phase accumulator (DPA) 14 accumulates a corresponding digital ramp sequence that represents the phase difference between the desired phase 132 and the actual phase of the VTO as evidenced by level-transition instants of the controlled frequency on lead 15. The DPA 14 creates a loop control error signal 95 on bus 134 that comprises the

linear difference in accumulated phase between the intended phase signal on bus 132 and the measured phase of controlled frequency on lead 15. The feedback control loop composed of loop filter (PLLF) 9, VTO 3, and frequency scaler 8 operate in conjunction with DPA 14 to effectively lock the VTO to a prescribed harmonic of the frequency defined by phase ramp signal 149 on bus 134, the harmonic multiple being equal to the division ratio (eight in the present embodiment) in frequency scaler 8.

One feature of the present invention, compared to the prior art, results from the particular spectrum characteristics of the error signal 10 that is derived from the signals 95 and 132 on bus 134. In the present invention, the net error signal on bus 134 is the integrated linear difference of two periodically sampled constants. The DPA 14 includes jitter synchronizer logic 81 and linear adder 92 that strictly isolate the timing of the differenced signals; therefore no sampling clock intermodulation products are produced. Accordingly, after an ideal digital-to-analog conversion, the noise spectrum of the analog error signal includes only the harmonics of the two sampling frequencies. In the design of one embodiment of the present invention, both of the sampling frequencies are many octaves above the loop passband, and the rolloff of the loop filter 9 attenuates the sampling noise to prevent noise modulation of the VTO 3.

In one embodiment of the invention digital-to-analog conversion will typically not be ideal, and some other sources of spurious signals will result. Typically, the DAC resolution bus 134 may be coarser than the digital resolution of phase ramp 132 of accumulator 13; this gives rise to a periodic phase round off error at the DAC output as explained in Reference 8. In the exemplary design shown in Fig. 2, the 9-bit DAC provides phase resolution equivalent to seven bits per cycle and, as explained

below, the lowest spurious frequency components (for 25kHz channel steps) are 400kHz from the carrier; these are strongly attenuated by loop filter 9 so that the spectrum of the output frequency signal on lead 42 is virtually free from spurious spectral lines.

The present invention may include various alternative embodiments implemented through circuitry in the digital frequency synthesizer for improving overall system performance. A block diagram of the synthesizer including four independent digital resolution and/or noise performance enhancement circuits namely, a Digital Signal Compression Filter (DSCF) 21, Analog Signal Equalization Filter (ASEF) 22 system, an Error Recursive Signal Quantizer (ERSQ) 400, an Adaptive Balance Control (ABC) 29, and a Dither Generator (DG) 27, is shown in Fig. 9, wherein each enhancement circuit can be implemented indepedently or collectively with any of the other enhancement circuits. In a first embodiment a filter system comprising the combination of the DSCF 21 and matching ASEF 22 is integrated into the frequency synthesizer to compress and filter the input to the DAC 93 and to further process the resultant output from the DAC 93. The DSCF 21 compresses the digital input signal and truncates it to the available bit field of the DAC 93, thereby reducing the required signal dynamic range at the input to the DAC 93. Thereafter, this reduced dynamic range digital signal is converted to an analog signal by the DAC 93, and the analog output signal is equalized by the ASEF 22 to compensate for the spectral shaping imposed by the DSCF 21. This digital/analog filter combination produces a flat frequency response over the band occupied by the phase lock control loop such that the dynamics of the control loop remain unaffected.

A second embodiment of the frequency synthesizer of the present invention includes an ERSQ 400 which compresses a wide bit-field signal into a reduced

bit-field signal. The ERSQ 400 provides a significant reduction of the inband noise of the PLL control loop relative to simple bit-field truncation and therefore permits the use of a DAC 93 having fewer bits of precision. The ERSQ 400 accumulates quantization error residue from each operational cycle and sums the resultant accumulated residue with the quantizer input signal to supress low frequency quantization noise. This recursive process assures that every component of input signal is ultimately transmitted through the DAC 93 to the analog filter loop regardless of the coarseness of the quantization process.

Several alternative embodiments of the frequency synthesizer of the present invention may be implemented with or without the DSCF/ASEF combination or the ERSQ 400 described above. For example, ABC 29 can be introduced to the circuit to adjust the analog weighting of the "V" signal 150 from the DPA 14. The summing amplifier 92 sums input signals 150 and 94. However, these signals contain some undesirable intermodulation products of the clock and carrier frequency appearing with equal and opposite phase in signals 150 and 94. The ABC 29 provides an adaptive nulling control loop to adjust the weight of the "V" signal 150 and effectively null line spectra associated with intermodulation products resulting from frequency harmonics in the clock and carrier signals.

In another alternative embodiment of the frequency synthesizer of the present invention, DG 27 is implemented to generate and inject a random digital noise signal into the input signal to the DAC 93. As in the case of the ABC 29, the dither generator 27 can be implemented with or without the the digital/analog filter combination 21,22 or the quantizer 400, as well as the ABC 29. The dither generator 27 operates to improve the effective linearity of the DAC 93 by superimposing a digital noise sequence on the digital input signal to the DAC 93. This superimposed

digital noise sequence eliminates line spectra associated with quantization error in the DAC, thereby reducing the tendency for inherent DAC quantization error to create a line spectrum at the synthesizer output.

The frequency synthesis circuit of the present invention provides fast frequency switching (hopping) because the low quantization and jitter noise associated with the PRA 13 and DPA 14 permits a relatively wide bandwidth for the loop filter 9, and by extension, for the overall frequency stabilization loop. In the design of the embodiment shown, the loop bandwidth is 50 kHz, and the loop time constant is about 6 microseconds. Faster response can be attained by using a higher loop gain and a broader passband in the loop filter 9.

The frequency resolution of the synthesizer is limited only by the bit precision used to produce the phase ramp sequence signal on bus 132. One exemplary design of Figure 2 uses 20-bit arithmetic in the PRA 13. The combination of 20-bit arithmetic with the 12.8 MHz sampling rate provided by oscillator 4 and by the times-eight loop multiplication ratio set by the division ratio in frequency divider 8 provides a synthesizer frequency resolution of 100 Hz over the VHF radio band 30-88 MHz, and can be improved by using a longer arithmetic word length. Alternatively, the DSCF 21 and the ERSQ 400 can be implemented to reduce the necessary bit field of the DAC to as low as 1 bit, thereby reducing cost and increasing clock speed capacity for the DAC and synthesizer while maintaining an adequately low level of quantization noise.

Figure 3 shows the asynchronous timing relationship between the differenced signals that comprise the loop error signal. The figure also shows an equivalent periodic impulse model for the error waveform that is composed of two series. Each impulse in the series representing the controlled frequency has a value equal to

2 π, corresponding to a complete phase cycle for each positive level-transition instant; these impulses appear at a regular rate f, where f is the controlled frequency. Each impulse in the series representing the synthesized phase ramp has a value equal to 2 π times the fractional cycle ratio f/f_o, where f_o is the 12.8 MHz clock frequency. These impulses appear at the rate f_o and the noise components are harmonics of the two impulse frequencies. In the embodiment shown in Figure 2, the smallest impulse frequency f is 3.75 MHz; this is the eighth subharmonic of the minimum synthesized frequency, 30 MHz.

In order to achieve noise performance that approximates the theoretical model described above it is necessary to employ a phase differencing circuit that faithfully reproduces the exact timing and exact phase step size of the impulse series model. The timing instants for the synthesized phase ramp are directly defined by the reference clock, however the required fractional cycle phase step $2\pi*f/f_o$ will typically be irrational with respect to the quantization steps of the DAC and the accumulated phase step sequence 132 will have to be truncated to a smaller bit field 149 that is available at the DAC. Conversely, the required 2 π phase step increment for the controlled frequency ramp is precisely achieved with a digital cycle counter, but the true time of level transition is asynchronous with the synchronous f_o reference clock such that an asynchronous jitter compensating circuit is required to achieve low noise performance.

One intended application for the invention includes the need for fast loop acquisition of frequency and phase lock after a frequency hop transition. Before frequency alignment, the difference phase as defined above changes at a rapid rate and will eventually overrun the linear range capacity of a linear difference-phase accumulator.

To prevent such events from reversing the direction of frequency slewing, the design includes a count limit level for both polarities of accumulated phase difference. In the example design of Figure 2, the limit levels are set at +/- one cycle (2 π radians) from the nominal zero difference position.

With the design objectives so specified we next present a detailed circuit design for the difference phase accumulator that performs the required phase differencing using appropriate means to compensate for asynchronous timing of the controlled frequency, irrational fractional phase steps in the synthesized phase ramp, and bidirectional frequency slewing for fast acquisition.

Difference Phase Accumulator (DPA)

As shown in Fig. 2, the accumulated difference phase between the synthesized frequency signal on bus 132 and the controlled frequency signal on lead 15 is measured and sampled by means of the 2-bit bidirectional synchronous counter 141, the timing jitter coincidence gate 142, the controlled-frequency cycle detector gate 146, and limit logic 143. The counter 141 is synchronized with the 12.8 MHz reference clock signal, and is incremented or decremented respectively according to presence of "U", the overflow bit 133 from PRA 13, and "D", the cycle flag signal on lead 153 from cycle detector gate 146. The limit logic 143 prevents increment or decrement of the counter if both inputs "U" and "D" are true. The increment or decrement is also inhibited to prevent overflow or underflow of the 2-bit counter. To accomplish this the Q1, Q2 counter states are combined with the U, D inputs to obtain counter enable signal "E", according to the truth table of Figure 2a. The count direction "up/down" is provided by the overflow pulse signal on lead 133 of PRA 13. The counter MSB (M) of difference phase 144 corresponds to the counter MSB(Q_2), but M

leads Q_2 by one clock cycle. M is derived from look ahead logic by circuit 143 according to truth table figure 2A. Output 144 is combined with vernier phase 150 in linear adder 92. Two-bit (4 ary) adder output 95 is applied to DAC 93 where it is weighted according to a phase value of 2π so that it has consistent binary coded weighting as compared to the other seven data bits on bus 149. Furthermore, bidirectional counter 141 and accumulator 137 are synchronously clocked with the 12.8 MHz reference, and transition edges of MSB 144 are therefore synchronous with the other seven data bits 149 from accumulator 137.

The scheme for detecting phase cycles of the controlled frequency is explained next. In the preferred embodiment, positive-going transitions of controlled frequency signal on lead 15 cause toggling of divider 151 to produce half-frequency output on lead 155; this is synchronously sampled in shift register 152 to obtain a synchronized half-frequency signal on lead 156. Half-frequency wave-form 155 is a constant binary logic level over a complete cycle of controlled frequency 15, which cycle interval exceeds the clock period, thereby assuring detection by register 152 and therefore assuring reliable operation of vernier phase circuit 142. The waveform on lead 156 is further delayed by one clock cycle in flip flop 152 to obtain waveform on lead 157. Exclusive-or gate 146 compares signals 156 and 157 to obtain a down count flag "D" 153 for application to bidirectional counter 141 via limit logic 143.

The scheme for jitter compensation uses the cycle-detection logic signals on leads 155 and 156 and exclusive-or gate 142 to produce a vernier timing signal on lead 150 to compensate for the variable timing lag between the level transition of controlled frequency 15 and next synchronous clock cycle. A logic one output signal on lead 150 occurs during intervals that the

waveform on lead 156 lags the waveform on lead 155. This interval corresponds to the timing jitter interval that must be replicated in the loop error waveform, according to the timing diagram in Figure 3. Vernier signal on lead 150 is applied to DAC 93 with weighting exactly equal to that applied to MSB 144 derived from counter 141 via look ahead logic 143. In one embodiment, shown in Figure 2, equal weighting is assured by digital combining of signals on leads 144 and 150 using linear binary adder circuit 92; the sum and carry are applied to the DAC where they are weighted by 2π and 4π respectively. This scheme makes use of a standard 9-bit binary-weighted DAC; in this case DAC 93 must operate asynchronously with the logic clock to accommodate the variable timing of vernier signal 150. Alternate implementations could use a synchronous DAC for synchronous signals 144 and 149, and use a separate 2π weighting branch for asynchronous signal 150. Utilization of a separate synchronous DAC permits use of a synchronous signal strobing gate to avoid excise timing error transients in the output of the multibit DAC. This effectively suppresses slight timing variations in the DAC bit paths that otherwise result in increased noise in the VFO. In either case loop filter 91 smooths output 94 of the DAC to eliminate harmonics represented by Figure 3 to obtain overall loop control signal 10 for VTO 3.

It is the nature of synchronous logic circuits, such as 152, 141, and 137 that output level transitions occur only in response to positive going edges of the clock, and that logic signals propagated through such devices are thereby quantized in time according to the clock period. For best replication of ideal error waveform in figure 3, it is desirable to avoid time quantization in the processing path of controlled frequency signal 15. Because contents of counter 141 are quantized, MSB Q2 is inappropriate for best performance because it lags the

vernier signal 150 by one clock cycle. To eliminate this relative timing mismatch at DAC 93, look ahead logic 143 combines counter outputs Q1, Q2 and count flags "D" and "U" to produce MSB output "M" 144, Fig. 2a. The logic is arranged so that output "M" is identical to counter output Q2, but leads Q2 by exactly one clock cycle.

To provide a capacity for fast frequency hopping over a wide bandwidth the synthesizer design includes logic for detecting an out-of-lock condition and for applying a full-scale frequency slewing signal to the loop filter 91. The slewing signal is removed when the VTO 3 frequency reaches the approximate value needed for stable frequency operation. Immediately after a frequency hop, and before loop lockup, cycle slipping drives bidirectional counter 141 to a limiting count (0 or 3), and the logic value of MSB 144 indicates the proper polarity required for the slewing signal. To prevent interference with frequency slewing by vernier signal 150, this signal is disabled by gate 148 during slewing operation. It is not necessary to disable DAC signals 149 during this interval because the digital values rapidly cycle over the range $0-2\pi$ and appear as a consistent DC bias of π during both slewing and tracking operation of the loop. Exclusive-or gate 147 compares the two count bits of counter 141 to sense when the counter is in either of the two slewing states. Application of MSB 144 to DAC 93 in absence of signal 150 causes loop filter output 10 to slew toward the voltage needed for stable loop operation. When this point is passed, the direction of cycle slipping in bidirectional counter 141 reverses until a single cycle difference phase occurs, and the counter content is changed from a slewing state (0 or 3) to a nonslewing state (1 or 2) in response to the up/down control signals. At this point the count toggles between states 1 and 2 in response to the up/down control signals from circuit 143.

Phase Ramp Accumulator (PRA)

The phase ramp accumulator (PRA) 13 accumulates a running numerical sum corresponding to intended carrier phase for the controlled frequency 15. There are two digital code signal inputs to the PRA 13; these are the frequency channel selection code signal on lead 33, and the FM modulation code signal on lead 11. Both input signals are binary coded indices, such that the sum specifies the instantaneous carrier frequency. In the design of Figure 2, the modulation deviation is linearly combined with the channel select code by means of modulation combiner (digital adder) 138. The modulation combiner operates at 400 kHz to accommodate the sampling rate of the modulator 16.

In order to achieve 100 Hz frequency resolution over 30-88 MHz the combination of frequency selection words 33 and 131 require 20-bit precision overall. The indicated design provides 12-bit words for the frequency channelization control word 33, with the MSB equal to 6.4 MHz and the LSB equal to 3.125 kHz. (Taking into account the times-eight deviation expansion in the VFO control loop, the MSB and LSB of the channelization word 33 correspond respectively to 51.2 MHz and 25kHz at carrier frequency). The modulation code 11 requires 8 bits precision to achieve 100 Hz resolution with peak deviation +/- 12.5 kHz. Accordingly, the logic component of the PRA 13 provide 20-bit word length, with appropriate sign extension for the modulation code.

The phase ramp is produced by means of digital accumulator 137. The accumulator input signal on lead 131 is a digital word denoting the instantaneous frequency, and the output signal on lead 132 denotes the instantaneous phase. The MSB of input 131 has a value of equal to half the clock frequency (6.4 MHz in the example), and the LSB has a value equal to 2^{-11} of the

MSB (3.125kHz). The MSB of the output signal on lead 132 has a value equal to π radians; and the overflow bit of accumulator 137 has a value of 2π radians. For the exemplary design, only the seven MSB of the twenty-bit accumulator output signal on lead 132 are used to represent the fractional-cycle phase to the DAC 93, and the overflow (carry) bit on lead 133 provides the cycle incrementing for the bidirectional counter 141.

The far-sideband noise of the synthesizer is governed by the PLL loop filter attenuation of the two pulse series 101, 102 shown in Figure 3, and near-sideband noise is dominated by a sawtooth error signal associated with phase quantization by DAC 93. Just as in the case of direct digital synthesizer (see Reference 8, pp. 139-240), phase quantization associated with using fewer than the full 20-bit output of accumulator 137 restricts the frequencies that are exactly replicated by the DAC to harmonics of the frequency step:

$$DF = f_0/M, \qquad (1)$$

where f_0 is the clock frequency and M is the number of phase steps per cycle that are resolvable in input word on bus 134 to DAC 93. For other frequencies, the PRA phase ramp is quantized to the M available phase states of the DAC; the resulting phaseerror sequence is a periodic sawtooth of magnitude π/M with a repetition frequency given by:

$$f_n = f_0 f_d/DF = Mf_d\ , \qquad (2)$$

where

$$f_d = (DF)K/2^k;\ 0 \leq K(\text{integer}) \leq 2^{k/2} \qquad (3)$$

is the frequency difference between the controlled frequency 15 and the closest harmonic of DF.

In the exemplary design shown: f_o is 12.8 MHz; M equals 128; DF equals 100 kHz; and (for 25 kHz channel

steps at RF) f_d is a multiple of 3.125 kHz in the range 0-50 kHz. Therefore, from equation 2, in absence of modulation code 11, the lowest periodic disturbance frequency is 400 kHz, which is well outside the passband of the loop filter 91, so the output frequency on lead 42 is free of spurious modulation from DAC truncation error. The lowest disturbance frequency can be increased in octave steps for each additional resolution bit at input 134 to DAC 93. In the presence of modulation the variable modulation code 11 effectively provides a dither to randomize truncation error at DAC input lead 149. This suppresses periodic error patterns in signal 94 that otherwise cause discrete line spectra in the synthesized signal.

Synthesizer Loop Filter (PLLF)

The PLLF 9 is optimized to reject far-spectrum phase noise and to provide a wide frequency-tuning lock range. The in channel and near channel noise floor of the synthesizer is influenced by sampling quantization noise. The noise is of two types, timing quantization error (jitter Fig. 3, 103) associated with the level-transition instants of the controlled frequency signal on lead 15, and level quantization error (Fig. 3, 104) associated with the individual phase steps of synthesized phase ramp signal on lead 94. Periodic noise components associated with channel tuning are well outside the 50 kHz nominal loop filter bandwidth, and these components are easily suppressed with a several-pole filter.

References 5 and 6, incorporated by reference, provide design methods for filter specification. Interaction of DAC truncation error with nonperiodic modulation waveform 11 results in a flat random noise spectrum at the DAC output. This does not impair synthesizer performance because only a small fraction of this noise is in the passband of the loop filter. The

overall noise level can be reduced to a selected level desired by using a DAC with the requisite linearity and phase step resolution. For non-critical synthesizer applications, adequate performance can be obtained by eliminating the DAC 93 and adder 92 and using only the MSB signal on lead 144 as a binary error signal to the loop filter 91.

In order to increase the digital resolution and noise performance of the novel frequency synthesis circuit described above, processing circuits described below are incorporated into the system.

Compression And Equalization Filtering (DSCF & ASEF)

As shown in Fig. 9, both the synthesized frequency signal output from the PRA 13 on bus 132 and the counter MSB (M) output from the DPA 14 on bus 144 are input to a digital signal compression filter (DSCF) 21. The digital signal output of the DSCF 21 is thereafter converted to an analog signal by DAC 93 for input to an analog signal equalization filter (ASEF) 22. The digital/analog filter combination 21,22 gives rise to compression of the dynamic range of the input to the synthesizer DAC 93, thereby reducing the quantization noise produced by the synthesizer for equivalent DAC bit precision or for the same noise performance, permitting the use of a DAC with fewer bits of precision.

One embodiment of a suitable DSCF/ASEF filter combination is shown in Fig. 11 wherein the DSCF 21 comprises a 1-pole, 1-zero configuration and the ASEF 22 comprises a complimentary 1-zero, 1-pole configuration. The DSCF 21 synchronously samples the output signals from PRA 13 and DPA 14 to produce a composite data word signal representative of the difference between the intended carrier phase and the most recent integer cycle accumulation of the controlled frequency. Thereafter, a first stage digital filter in the DSCF 21 functions to

smooth and compress the composite input signals 132, 144 by means of a digital pole formed by the combination of adder 100, scaling operator 103, and accumulator 101, 102, producing an interstage signal 201. A second stage digital filter comprising adder 300, scaler 301, and delay circuit 302, forms a transfer function zero. This examplary second stage filter receives a difference signal 305 from the first stage filter for summing with the output 201 of the first stage filter scaled by a factor of 2^{-n} in scaler 301. This scaler operation provides a damping effect for the transfer function zero, while delay circuit 302 provides compensation for delay circuit 102 in the first stage filter. The DSCF 21 output is further quantized to the bit field of the DAC by way of a bit-field truncation operator or, alternatively, by means of an error-recursive signal quantizer, as hereinafter described.

ASEF 22 performs an inverse operation on the analog output of DAC 93 to equalize the compression and smoothing operation of DSCF 21. This equalization process is carried out by the amplifier 105 in combination with RC circuit 103, which forms a transfer function pole to equalize the compression filter zero and with RC circuit 104 forming a transfer function zero, equalizing the compression filter pole. The time constant provided by parallel RC circuit 103 is equal to the scalar 2^{-r} divided by the clock frequency such that the zero of DSCF 21 is equalized. The time constant generated by RC circuit 104 forms a zero where R_oC_o is equal to 2^{-n} divided by the clock frequency such that the pole of DSCF 21 is equalized.

In order to more particularly describe the circuit of DSCF 21, the Z-transform transmission equations for the first and second digital filter sections are given respectively as:

$$H_1(z) = \frac{(2^{-r})(z^{-1})}{1-(1-2^{-r})z^{-1}} \quad (4)$$

$$H_2(z) = 1-z^{-1}(1-2^{-n}) \quad (5)$$

The low frequency response equations for these two filters are:

$$H_1(\omega) \equiv \frac{1}{j2^r(\omega/f)+1} \quad (6)$$

where ω is much less than f

$$H_2(\omega) \equiv j2^n(\omega/f)+1 \quad (7)$$

Finally, the equation for the frequency response of the ASEF 22 is:

$$G(\omega) = \frac{j2^r(\omega/f)+1}{j2^n(\omega/f)+1} \quad (8)$$

As previously noted, the composite input signal 132, 144 to the DSCF 21 is a synchronously sampled data word denoting the difference between the intended carrier phase and the most recent integer cycle accumulation of the controlled frequency. The sequence on bus 132 is strictly confined by the bit field to a value between 0-2π. Thus, the linear sum of signals 144 and 132 is strictly confined to a linear range between 0 and 4π from the

available bit field for the composite signal 132,144. Under these conditions, the mean of the signal is likewise confined to the same range such that the DSCF 21 filter coefficients r and n can be chosen in a manner that rejects the high-amplitude carrier frequency sawtooth signal on bus 132,144 but passes the desired low-amplitude, low frequency PLL control spectrum without distortion. Figs. 10A-10C show the relationship of the waveforms as required at the input of the PLLF 91 and the inputs 150 and 132, 144 to linear amplifier 92. It can be seen from these waveforms that the difference phase is strictly confined to cyclic sawtooth data from 0 to 4π. It should be noted that over the span of several hundred cycles of the carrier frequency sawtooth, the control variable of interest is essentially a constant in which the value is equal to the short term average of the binary signal appearing on line 144.

DSCF 21 generates output 304 in response to a 2π phase step input to the DSCF at 132, 144. The scaling operator of the digital pole of the DSCF 21 reduces output 304 by a scaling factor of 2^{-r} relative to the 2π step input such that the required data field necessary to accommodate the amplitude of the sawtooth signal at the DAC 93 is reduced by r bits while the signal quantization distortion produced by the system is not increased. It will be appreciated that filters having multiple poles and multiple zeros can be substituted for the elementary single-pole, single zero design disclosed herein

Error-Recursive Signal Quantizer (ERSQ)

An examplary Error-Recursive Signal Quantizer (ERSQ) comprising a digital adder 401 and combinatorial logic or Read Only Memory (ROM) 406 is shown in fig. 12. The ERSQ receives an n-bit input signal 408 representing a composite of the counter MSB (M) output from the DPA 14

and the synthesized phase ramp output from the PRA 13. This composite input signal 408 is summed at adder 401 with an n-bit feedback signal 409 comprising an error residue signal 404 and the output 405 from the combinatorial logic 406. Adder 401 generates an n+1 bit output signal 410 comprising three individual components: MSB overflow bit 402; a k-bit quantized signal field 403; and an n-k bit quantization error residue 404, wherein signals 402 and 403 are applied directly to combinatorial logic 406 while error residue 404 is recirculated into the feedback path thereof for combining with the output signal 405 forming a feedback signal 409.

The operation of the ERSQ will now be described. In normal operation, where no overflow exists, the MSB on line 402 is equal to zero, thereby programming logic 406 to switch the k-bit delta code on line 403 to output line 304, and simultaneously generating a low (null) output code on line 405. Conversely, when an overflow condition exists at output 402, logic 406 produces a high (full scale) output code on line 304 and generates a code on line 405 that is one greater than the delta code on line 403. As a result, all components of the n-bit input signal 408 are retained in the residue 409 and are then recirculated until they are output from the quantizer as a portion of a valid code on line 304. Thus, the quantizer passes the k-bit quantized signal field representing the delta code 410 when no overflow condition exists, and accumulates input signal 408 during intervals when an overflow signal does exist.

In practice of the invention, the signal components of input 408 are subjected to variable delays in the recirculating residue before they are output. These delays appear as noise at the output of the quantizer. Since the power of this noise is proportional to the square of its frequency, the power is well outside the passband of the PLLF 91 such that the noise from the ERSQ

circuit is reduced in comparison to the noise generated by signal truncation to an equivalent k-bit DAC field. Thus, the ERSQ permits coarser quantization than for the case of signal truncation.

It will be appreciated that a signal-recursive quantizer could be substituted for the error-recursive signal quantizer. For example, a 1-bit DAC using a signal recursive quantizer could be implemented in the present invention, wherein the DSCF and ASEF are related to the preemphisis filter and the output smoothing filter, respectively, as customary for use in voice signal conversion in delta modulation telephone systems. Likewise, a multibit DAC using a signal recursive quantizer could be implemented wherein the filter combination is related to a linear delta PCM modulation. Useful analytical models for performance evaluation of the synthesizer can be found in references 12-15, incorporated herein by reference.

Dither Generator

Fig. 13 shows a circuit diagram for a means for linearization of k-bit DAC circuits operating with truncated signals. This DAC linearization circuit includes a shift register 273 in combination with at least one exclusive OR gate 274 make up a dither generator 27. The output of the dither generator 27 is added to interstage signal 201 by way of gate array 275-278. The dither generator 27 is clocked at 1/2 the system clock frequency by means of divider 279 which also provides the clocking frequency for gates 275, 276, 277 and 278.

The dither generator comprises a maximal length shift register sequence generator which provides a pseudorandom digital output from shift register 273 to be added to interstage signal 201 by means of adder 272 in a manner such that gate arrangement 275-278 delivers a sample of the dither signal 271 to adder 272 at 1/2 the

system clock frequency. An inverted sample of the dither signal is later input to adder 272 during the second half cycle of the divider output.

The exemplary design of Fig. 13 injects the dither signal 272 at a random uniformly distributed level between discrete levels 0 and 1 relative to the least significant bit of the quantized signal wherein this range represents the same amplitude range of the quantization error. Each noise sample is first added to, and then subtracted from the synthesizer signal by adding the inverse signal from signal 201 by means of adder 272. The present invention shapes the spectrum of the dither signal to prevent noise performance degradation of the synthesizer output.

Adaptive Balance Control (ABC)

As previously described, it is desirable that the dual inputs to the linear summing amplifier 92 are precisely balanced. Fig. 14 shows an adaptive balance control 29 for maintaining a precise balance between these input signals, the asynchronous "V" noise reference signal 150 and the DAC analog output signal 96 (or the ASEF output signal 94 if an ASEF is implemented). The adaptive balance control 29 comprises a multiplier 600, an operational integrator made up of operational amplifier 602 and feedback capacitor 609, a summing network 610 and a binary switching network 606.

The multiplier 600 is fed the "V" noise reference signal 150 and the sum signal 95 via DC blocking capacitor 607 to obtain a nulling residue signal 601. This nulling residue signal 601 is input to the operational integrator 602 wherein the output thereof is combined with second input 94 to the summing amplifier in a two-resistor virtual ground summing network comprising resistors 610 and complimentary binary switches 606. The balance control stabilizes with a weight for the "V"

signal that minimizes the amplitude of intermodulation lines in the transition band of the synthesizer PLL loop.

In the present invention, the required noise reference for the nulling loop is the asynchronous "V" signal 150. This "V" signal normally contains an intermodulation line spectrum having certain components which lie in the critical transition bandwidth of the phase lock loop. When these components appear in the "V" signal 150, the same intermodulation components appear simaltaneously with equal amplitude in the other input 94 to summing amplifier 92, as previously explained. When an unbalanced weighting condition exists, the output 95 of the summing amplifier 92 contains an undesirable component of the intermodulation line spectrum. By cross correlating the "V" signal 150 with the summing amplifier output signal 95 the adaptive blance control 29 derives an adaptive weight for the "V" signal. The adaptive balance circuit extracts an error signal 601 by means of the cross correlator such that the "V" weight is driven in a direction to null the intermodulation noise at the output 95 of the summing amplifier 92. The adaptive balance control 29 provides the necessary balance between linear summing amplifier input signals 94, 150 with an accuracy appropriate for an uncompressed signal. When the intermodulation line spectrum is nulled from the correlation bandwidth of the nulling loop, the error signal 601 is eradicated.

OVERVIEW OF SIGNAL FLOW FOR MODULATION AND DEMODULATION

The modulator 16 and demodulator 17 of Fig. 1 operate using both analog/FM and binary/FM waveforms. The modulation deviation, linearity, and premodulation filtering are exactly controlled by means of numerical sequences so that required modulation standards are more strictly maintained than is possible for analog radio

designs. Reference 9, incorporated by reference, gives methods to determine the optimum premodulation spectrum shaping and corresponding time domain pulse shaping for binary/FM symbol transmission. For minimum bandwidth applications the required spectrum rolloff results in unavoidable intersymbol ringing with large amplitude, and accurate control of filter coefficients is required to constrain the ringing waveform so it has nulls at successive symbol decision instants (the Nyquist zero intersymbol distortion condition), thereby permitting successful recovery of the data sequence at the demodulator. The required filter accuracy is difficult to assure with analog circuits, but can be reliably achieved with the digital modulation circuits described here.

In the exemplary design, the binary FM modulator 162 produces a numerical sequence 11 representing modulation in response to 16 kb/s continuous (CVSD) data on path 227 or in response to 20 kb/s burst data (CVSD with frequency-hop buffering) on path 221. Alternately, the analog FM modulator 163 produces a numerical sequence 11 representing conventional analog FM modulation in response to digital samples 231 of voiceband signals. The voice band signals may be either actual voice signals or audio tone FSK data. Also, the design permits audio tone data to be transmitted directly as analog/FM, or to be processed in the CVSD coder/decoder (codec) and transmitted as 16 kb/s binary/FM. Baseband digital data up to 16 kb/s can be accommodated in place of the CVSD signals.

In either analog/FM and binary/FM transmission modes, the exemplary modulator 16 shown in Fig. 4 produces a 400 kHz output sample sequence that is the required frequency modulation series to represent the intended modulation pattern. The frequency modulation series is an 8-bit, 400 kHz sample sequence on lead 11 which specifies the required instantaneous frequency deviation for the

modulator. In the example design the MSB of the 8-bit signal field designates a frequency deviation of 12.5 kHz and the LSB corresponds to 100 Hz deviation wherein the deviation range can be increased by using a larger word length.

In Figure 1, the digital modulator 16 output signal on lead 11 is a 400 kHz sample sequence representing the intended instantaneous frequency deviation for the carrier. This sequence is summed with the channel select frequency code signal on lead 33 in PRA 13 to obtain a digital sequence denoting the instantaneous frequency of the carrier. The result is upsampled (upconverted by sampling at a higher frequency) to 12.8 MHz and integrated in the PRA 13 to obtain a phase ramp sequence to which the VTO is phase locked.

For demodulation, double-conversion heterodyning by mixers 5 and 6 of the received signal results in a 300 kHz second IF signal on lead 7. This signal is demodulated in a digital phase lock loop demodulator 17 that comprises a reference phase sampler (RPS) 172 and a recursive phase filter (RPF) 179. The RPS uses positive edges of the 300 kHz IF signal 7 to sample the phase of a seven-bit, 400 kHz reference signal 124. This reference signal is produced by clocking a 7-bit counter 12 with the 12.8 MHz output signal on lead 43 of the reference oscillator 4. The RPS scales the resulting 7-bit sample by a factor of 3 (modulo 2π) to obtain a 7-bit number representing the instantaneous phase of the 300 kHz IF signal. The successive phase samples are smoothed in the RPF 179, which is updated once for each detected zero crossing of the 300 kHz IF signal 7. Each output sample 173 of the RPF is an optimally filtered estimate of the instantaneous frequency. This signal is received by squelch circuit 24, shift register delay 18, and bit synchronizer 26.

In the receiving signal direction the frequency-estimate signal at bus 173 from demodulator 17

is an 8-bit sample sequence at 400 kHz, with the same frequency deviation convention used at the modulator. In the analog/FM transmission mode, the synchronizer 26 produces a 16 kHz sampling clock 267 that is used to downsample the 400 kHz sequence on bus 173 to 16 kHz within the squelch circuit 24 and within shift delay register 18. The 16 kHz output of delay register 18 is fed to baseband filters via data path 232. In the binary/FM transmission modes, the delay register 18 truncates the received frequency estimate signal on lead 173 to one-bit quantization (the sign bit), delays the resulting 400 kHz binary sequence in delay register 18, and downsamples the delayed sequence with a symbol sampling clock 267 to obtain 16 or 20kb/s data stream 261. Sampling clock 267 is derived by synchronizer 26 at either 16 kHz or 20 kHz, as selected by control bus 342 for continuous and intermittent (frequency hopping) modes respectively; the phase of the clock signal on lead 267 is selected by the synchronizer 26 to achieve optimum center sampling of the delayed binary symbol sequence.

THE SQUELCH AND DELAY CIRCUIT

The design of Figure 1 includes three forms of squelch for disabling the audio in the absence of received carrier. The noise-squelch detector 24 in Fig. 5 senses absence of carrier by means of a counter that measures the rate of received FM clicks. Squelch detector 24 also senses disappearance of a sub-audio tone by means of digital filter 240 in Figure 5. This filter is a second order recursive filter tuned to the particular tone frequency. Design is described in Reference 11. In binary/FM transmission modes, the bit synchronizer 26 shown in Fig. 6 senses sync dropout to activate the audio squelch.

The appropriate two of three squelch indicator signals on leads 247,245,260 are selected by control bus 343 and combined in squelch combiner 27 to obtain the audio muting control 271.

The three squelch detection methods and combining methods used in the embodiment shown are generally known in the art, and are typically implemented using analog filter circuits that operate on the received analog baseband waveform. In conventional analog radios the squelch and synchronization performance is limited by the need to operate the associated filters and detection circuits in real time, as the received analog/FM waveform is demodulated. In the present invention this real time constraint is eliminated, so that improved squelch and symbol synchronization performance is achievable. In the preferred embodiment, all received signals, including analog/FM, appear as a digital sequence at the demodulator output 173. These samples are delayed in a delay register 18 and (for analog/FM) are then passed to baseband filter 23 via path 232, or (for binary/FM) are routed via path 261 to FIFO buffer 21 and the CVSD decoder 22. Relative to the delayed information stream the squelch combiner 24 and bit synchronizer 26 are provided lookahead time for continuous error-free control for squelch and symbol synchronization.

In the theory of FM demodulation, threshold operation (at low signal to noise ratio) is accompanied by noise-induced envelope fluctuation. Instants that correspond to reduced envelope can produce abrupt phase changes, and these produce wideband audio clicks in the demodulated signal. In the case of conventional analog demodulators, squelch control is usually derived by measuring the click power appearing in the spectrum above the audio signal band. A sudden burst of high frequency click power is interpreted as a loss of carrier, and the audio output is then disabled. In the digital noise

squelch design of Figure 5 the clicks are sensed directly from demodulator output 173, using a frequency-rate-of-change detector composed of a delay shift register 241, a frequency code differencer 242 and a frequency-magnitude threshold in comparator 243. A click is declared on enable line 249 if the comparator detects a frequency rate of change greater than threshold 246. Carrier-off transition will be evidenced by a rapid increase in the number of detected clicks accumulated in counter 244. If comparator 247 detects an excessive number of counts at the end of a count interval, the signal for that interval is squelched by means of squelch control line 247.

The squelch reliability for the digital scheme is greatly improved in comparison with analog designs by delaying the demodulated signal 173 in FIFO delay shift register 18. The delayed signal 232 is processed in baseband processor to recover communications traffic and undelayed signal 173 is used for deriving squelch and (for binary/FM operation) bit synchronization. This arrangement makes available a transient response interval for actuation of squelch and bit sync circuits before the associated control decisions are needed by the traffic path. For convenience, the transient response intervals for squelch and bit sync, and the traffic delay interval may be arranged so they all coincide with the frequency hop interval; under these conditions the squelch and bit sync control will be capable of independent operation for each frequency hop interval.

SYNCHRONIZER

The synchronizer 26 in Fig. 6 provides the sampling clock 267 for optimum center sampling of the received data bit in the binary FM transmission modes. Timing is derived by phase averaging of zero-crossing instants associated with the series of received data bits received

in an interval equal to the delay interval of delay register 18. In this manner, optimum clock timing is derived before the bit decisions are committed. In one embodiment of the present invention, bandwidth-efficient binary FM waveforms are employed which result in considerable intersymbol distortion. As a result, the zero crossing phase of the demodulator output 173 has very large data-dependent timing jitter, and it is difficult to derive optimum timing phase from a short sequence of data bits. Under these conditions, it is advantageous to align timing to the median of the observed zero crossing phase values. In the exemplary embodiment, the circuits are arranged to recover this median estimate. Alternative embodiments that are quite similar can be arranged to align timing with the centroid of the zero crossing phase values.

The sign and magnitude components of demodulated data appear at 400kHz sampling rate at the output of demodulator 17. For analog FM reception, the demodulated data 173 is downsampled to 16kHz by means of reference clock 122 at the input to squelch tone detector 24. The same data delayed at 400 kHz rate in register 18 is similarly downsampled at input 232 to base band filter 23. In binary FM modes, magnitude data in demodulator output 173 is ignored and sign bit 282 of Fig. 6 denotes optimum binary level slicing decisions at each sampling instant of the 400kHz series from demodulator 17. Note that unlike conventional analog circuit designs, the digital demodulator circuit has no center frequency tuning uncertainty so no AFC is required to eliminate level slicing bias. Sign bit 282 is processed to recover optimum sampling phase for bit decisions. State transitions, i.e. data zero crossings, are detected by means of flip flop 260 and exclusive-or gate 262. All transitions are accumulated as an L-point sliding histogram in recirculating FIFO buffer 264, 265.

The value L corresponds to the number of 400 kHz cycles in the period of the data bit; L=20 for 20 kb/s burst mode, and L=25 for 16kb/s continuous mode. Transitions older than the delay value of delay register 18 are systematically removed from the histogram data using a duplicate sign transition detector 260, 262 at the output of delay register 18; by this means the histogram content always denotes the activity in the most recent interval of delay register 18.

The zero-crossing histogram data is next processed in a cyclic smoothing filter composed of X2 scaler 275,delay FIFOs 266, adder 267 and accumulator 268. This filter extracts the timing phase corresponding to the median of the data in the histogram. The impulse response of the smoothing filter is a one-cycle square wave impulse of period L samples as shown in Fig. 7A. (Note that the use of a triangle wave impulse response (Fig. 7B) would result in a centroid filter rather than a median filter.) As the histogram data is circulated through the filter, one positive-to-negative sign change will occur at accumulator output 277. This occurs whether the median (or, alternatively, the centroid) point of the histogram passes through center point of the filter impulse response. The state transition is detected by means of flip flop 269 and sync filter logic 280, and used to initialize counter 270 via lead 281. After initialization, the counter produces periodic sampling pulses at the receive bit rate, with timing aligned to the median (or centroid) zero crossing phase. The sampling clock is used in register 272 to downsample the 400kHz delayed sign bit sequence at the output of delay register 18 to obtain a data bit sequence 261.

Sync filter 280 is combinatorial logic arranged to enable initialization of counter 270 under some conditions and inhibit initialization under other conditions. For example, in frequency hop operation, the radio will

occasionally occupy a channel that contains strong interference. Under these conditions, the resync can be inhibited; in fact, abrupt timing shifts detected by comparison of counter state 271 with timing of pulse 277 provide one means for discriminating between interference and the desired signal. In the event a bad hop is detected the logic 280 produces a squelch indication 260 for disabling the speaker. When logic 280 detects consistent timing, the squelch indication is removed.

BASEBAND SIGNAL PROCESSING

Analog/FM

In the exemplary embodiment of Fig. 1 the audio input/output is sampled at 16 kHz by means of an 8-bit A/D (or D/A) converter 30; this is chosen for convenience in converting the audio to both 16 kb/s CVSD binary/FM and to analog/FM. All required baseband signal processing operations, including all audio band filtering, pre-emphasis, de-emphasis, and squelch tone injection and detection operations are conducted at the same 16 kHz sampling rate. The baseband filtering operations for the present invention for analog/FM include known digital signal processing designs. Reference 11 describes numerical methods for reducing frequency domain filter specifications to equivalent digital filter coefficients for the prescribed 16 kHz sampling rate.

CVSD Coder/Decoder

In the binary FM "digital voice" transmission mode, the 16 kHz sample sequence signal on lead 231 from the audio filter 23 is further processed in a CVSD voice digitization coding/decoding (codec) circuit 22. The CVSD coding converts the signal from a 16 kHz sequence of multibit linear samples to a 16 kHz sequence of binary samples on lead 227. The decoding operation is the reverse; it converts 16 kb/s binary samples 228 or 261 to 16 kHz linear samples signal on leads 229. There are

several known analog circuit configurations or "coding laws" for performing the CVSD operation. Reference 12, pp. 410-417, incorporated by reference, describes logic structure for several standard versions of CVSD and shows comparative performance indices for different filter coefficients. It is sometimes necessary to achieve communications interoperability between systems which use different CVSD filter coefficients in their radios. The digital processor of the subject invention is adaptable to inclusion of a plurality of CVSD coefficient sets to provide for this contingency.

The CVSD codec 22 is fed to binary FM modulator 162 either directly via lead 227, or via FIFO buffer 21 on lead 221. The lead 227 signal is a continuous 16 kHz sample sequence that is used in the single channel operating mode and the lead 221 signal is an intermittent (burst) 20 kHz sample sequence used in the frequency hopping mode.

THE DIGITAL MODULATOR SIGNAL PROCESSOR

The binary FM sample sequence is produced by binary FM generator 162, and the analog/FM sample sequence is produced by upsampling filter 163. Switch 160 selects the operating mode in response to operator control 34.

Analog Mode Upsampling Filter

The 16 kHz sample sequence 231 for analog modulation modes contains the desired 300-3000 Hz information band, but it also contains unwanted alias signal bands that must be removed before the FM modulation process is performed. In the present invention, the 16 kHz samples of this input baseband signal are first upsampled to 400 kHz by means of an interpolating digital filter 163 shown in Fig. 4. The desired input signal spectrum is confined to the band 300 Hz to 3 kHz and the (unwanted) image band of greatest concern is between 13 kHz and 15.7 kHz. The upsampling

filter is arranged to pass the lower band and stop the upper band. In the preferred design in Figure 4 both logic circuitry and logic clocking speed are minimized by means of a cascade combination of second differencer 165 operating at 16 kHz and double accumulator 166 operating at 400 kHz. To prevent FM frequency offset in the synthesizer output, the accumulator integration constant must be initialized to conform to the modulating sequence 231. This is accomplished by means of press to talk (PTT) control signal on lead 341 applied via synchronizing buffer 170 as a register clearing control 171 to register 164 and accumulator 166. The overall impulse response of this filter is triangular in shape, and the frequency response of the filter is given by the equation

$$H(p) = [\sin(\pi p)/\pi p]^2 \qquad (4)$$

where $p = f/F$ is the normalized frequency and F is 16 kHz. This filter produces better than 30 dB rejection of the sampling image over the image band 13-16kHz. Other, more complex digital filters designed according to methods of Reference 11 may be used if desired.

Digital Modulation Shaping Filter

The digital transmission modes require binary FM modulation with premodulation filters (shaped bit transitions) to confine the spectrum to the unauthorized bandwidth. The required spectrum shaping introduces unavoidable intersymbol ringing, and the digital filter must faithfully replicate this ringing over several adjacent symbol intervals to meet the required spectrum confinement specification. Rather than perform a formal digital filter operation on the sequence of data bits, the preferred design uses preformatted ROM code to synthesize the desired shaped modulating waveform in accordance with Equation 5 shown below.

$$A_n(d_{-2},d_{-1},d_0,d_1,d_2) = \sum_{k=-2}^{+2} d_k P((k-1/2+n/N)T) \quad (5)$$

where T is the symbol interval, d_k is the sequence of data bits at modulator input, n is the time index, N is the number of clock cycles per bit interval, and P(t) is any of the FM waveforms defined in Reference 9.

In this scheme a symbol waveform is tabulated in the ROM 169 for all possible combinations of the current data symbol with the two precursor and two successor symbols. This is accomplished as follows: during each symbol interval the five most recent data bits $(d_{-2},d_{-1}, d_o,d_1,d_2)$ contained in shift register 167 are used as the waveform identifier address to the ROM. Another 5-bit address field (n) is provided to the ROM by the programmable symbol interval timer 168. On each successive cycle of the 400 kHz clock the output sample from the ROM represents an exact replica of the desired modulation waveform at that instant, including all essential intersymbol ringing associated with the two precursor and two successor data symbols.

The symbol interval timer 168 divides the 400 kHz clock by N equal to 25 or 20, to obtain the symbol clock equal to 16 kHz or 20 kHz respectively. The divider state represents the 5-bit time index for a predefined pulse template $A_n (d_{-2}, d_{-1}, d_o, d_1, d_2)$ stored in a 2048 X 8 ROM. There are 32 pulse templates stored, representing each of the 32 possible combinations of 5 adjacent binary symbols $(d_{-2}, d_{-1}, d_o, d_1, d_2)$. A five-stage symbol register clocked from the symbol clock holds the five most recent symbols at any instant. Two sets of templates are stored, one for the 20 kHz symbol rate and one for the 16 kHz symbol rate. The symbol rate selection is controlled by lead 342, a mode control from

operator's control 34. Other waveform templates can be accommodated for different waveforms and different symbol rates by expanding the ROM memory and expanding control field 342.

The 8-bit ROM code defining the FM pulse is scaled according to the convention defined for the phase ramp accumulator 13; so that the MSB has a frequency value (referenced to the carrier frequency) of 12.5 kHz, and the maximum deviation is +/- 12.5 kHz.

The described waveform synthesis method can be expanded to include more overlapping symbol intervals by simply expanding the ROM address space to include more waveform templates. Alternately, this expansion of ROM tabulations can be avoided by using separate ROM tabulations to represent the intersymbol ringing responses of individual data symbols or small groups of data symbols; these separate components may be linearly combined to obtain the net frequency modulating waveform response. This approach reduces the size of the ROM, but requires additional combining logic.

A further variation of the modulator accommodates transmission of phase modulation waveforms, either analog PM or binary PM. In these cases, the output of modulator 16 is summed with signal 132 at the output of PRA 13.

THE DIGITAL DEMODULATOR SIGNAL PROCESSOR

Figure 5 shows a block diagram of the digital PLL demodulator. The demodulator is composed of a 7-bit reference phase sampler 172 (RPS), and a recursive phase filter 179 (RPF). The RPS 172 is composed of a zero crossing detector 62,171 a reference phase state signal on bus 124 supplied by divider 12, a phase state register 173, event buffer 61, 69 and phase scaler 64. The flip flop and AND gate circuit 171 produces clock synchronization pulse 67 for each positive-going zero

crossing event of the input (300 kHz second IF) waveform 7. The reference clock is divided in 7-bit counter 12. The contents of counter 12 are sampled into the phase state register 173 at each detection event by means of clock enable pulse 67. The 7-bit counter 173 represents the phase state of a 100 kHz reference signal. This count is scaled by a factor three (modulo 2 π) by phase scaler 64 to convert the 100 kHz datum to an equivalent 300 kHz datum 65.

The detected 300 kHz event pulse from synchronizer 171 is also applied to asynchronous event buffer 61, 69. The buffer 69 is set by the event pulse 67 and reset by the slave clock 63 so that it is deactivated by the first 400 kHz system clock 66 after pulse 67; the event buffer output 63 also enables a single cycle update of filter 179 for each detected zero crossing event. The asynchronous readout of buffer 61 is sufficiently faster than the input pulses on leads 67 such that every event is recovered, and no event is counted twice.

The loop filter of the RPF 179 smooths the quantization noise in the phase state samples 65 and effectively extends the demodulation threshold. The digital implementation of the PLL avoids circuit stability problems associated with analog designs;the digital circuit has no frequency drift and the control loop dynamics are invariant.

The RPF 179 is composed of three functional circuits: an accumulator 178 that is analogous to the voltage controlled oscillator VCO of a conventional PLL demodulator; a lowpass filter 177 ,179, 175, that is analogous to the PLL loop filter; and a phase differencer 174 that is analogous to the phase detector of an analogous PLL. The input to phase differencer 174 is a 7-bit, two's complement number representing the instantaneous phase of the IF signal which is analogous to the signal phase at the input to a conventional PLL. The

output 172 of the accumulator 178 is the estimated phase, and the RPF output 173 is the estimated frequency. The loop filter coefficient 179 and the loop gain coefficient 176 are chosen to provide optimum smoothing of the phase error, while providing adequate bandwidth for the baseband signal and sufficient lock range to accommodate the largest anticipated frequency deviation. Best overall operation is obtained when the loop filter provides critical damping. The overall PLL response bandwidth is slightly wider than the baseband; nominal bandwith is 4 kHz for analog and 15 kHz for digital transmission modes. The loop filter parameters 176 and 179 are switchable for the two operating modes by means of control bus 343.

Modifications to or substitutions in the embodiment shown are within the scope of the present invention which is not to be limited except according to the claims which follow.

CLAIMS

What is claimed is:

1. A transceiver, comprising:

a transmitter section providing a transmitted RF signal, including:

a transmit frequency synthesizer for providing a transmit frequency signal;

means for receiving an incoming baseband signal and providing an incoming digitized signal therefrom, and

means for digitally modulating said transmit frequency signal according to said incoming baseband signal providing said transmitted signal;

a receiver section receiving a modulated RF signal, including;

a local oscillator providing a first local oscillator signal, and

digital demodulation means for combining said modulated RF signal and said first local oscillator signal to provide an outgoing digital baseband signal; and

a reference oscillator for synchronously controlling said transmit frequency synthesizer, said means for receiving, said means for digitally modulating, said local oscillator, and said digital demodulator.

2. The transceiver of claim 1, further comprising:

a digital processor for controlling the emission spectrum of said transmitter.

3. The transceiver of claim 2, wherein:

said digital processor includes a digital baseband filter.

4. A frequency synthesizer, comprising:

a reference oscillator providing a periodic oscillator signal precisely defining periodic sampling instants;

a phase ramp accumulator providing a numeric ramp sequence of digital representations of an intended phase of a signal whose frequency is to be controlled, each digital representation in the sequence being provided at corresponding ones of said precisely defined periodic sampling instants; and

a difference phase accumulator accumulating a numeric ramp sequence of digital representations of an actual phase of a signal whose frequency is to be controlled, each digital representation in the sequence being provided at time instants independent of said precisely defined periodic sampling instants according to level transition instants of the frequency to be controlled, wherein said digital phase accumulator provides a loop error signal comprising linear differences in accumulated phase between the intended phase and the actual phase of said signal whose frequency is to be controlled.

5. The frequency synthesizer of claim 4, including:

a loop filter;

a voltage tunable oscillator;

a frequency scaler having a division ratio responsive to said digital phase accumulator for locking the voltage tunable oscillator to an harmonic of the frequency defined by said phase ramp accumulator, said harmonic multiple being equal to the division ratio.

6. The frequency synthesizer of claim 4, further including:

means for detecting an out-of-lock condition; and

means for applying a full-scale frequency slewing

signal to said loop filter when an out-of-lock condition is detected in a manner that drives loop filter to in-lock condition.

7. The frequency synthesizer of claim 4, further including:

means for providing a composite digital signal representation of a difference between the intended phase of the controlled frequency and an integer cycle accumulation of the controlled frequency;

a first filter receiving the intended phase of the controlled frequency from said phase ramp accumulator and an integer cycle accumulation of the controlled frequency from said difference phase accumulator and providing a compressed digital representation thereof;

a digital-to-analog converter receiving a predetermined bit field of said compressed digital representation and providing an analog representation thereof; and

a second filter providing an equalized analog output signal having a spectrum equivalent to the spectrum of the original composite digital signal and compensated for effects resulting from compression by said first filter.

8. The frequency synthesizer of claim 7, wherein:

said first filter is a digital signal compression filter comprising at least one digital pole; and

said second filter is an analog signal equalization filter comprising at least one transfer function zero corresponding to said at least one digital pole of said digital signal compression filter.

9. The frequency synthesizer of claim 7, wherein:

said first filter is a digital signal compression filter comprising at least one digital zero; and

said second filter is an analog signal equalization filter comprising at least one transfer function pole corresponding to said at least one digital zero of said digital signal compression filter.

10. The frequency synthesizer of claim 7, wherein:

said first filter is a digital signal compression filter comprising at least one digital pole and at least one digital zero; and

said second filter is an analog signal equalization filter comprising at least one transfer function zero corresponding to said at least one digital pole and at least one transfer function pole corresponding to said at least one digital zero.

11. The frequency synthesizer of claim 4, further including:

a signal quantizer combining said numeric ramp sequence representing the intended phase of controlled frequency and said loop error signal to provide a compressed digital representation thereof.

12. The frequency synthesizer of claim 4, further including:

a controller responsive to said loop error signal for adaptively nulling spectra noise produced by intermodulation of the reference oscillator and the carrier frequencies.

13. The frequency synthesizer of claim 4, further including:

a generator producing and injecting a pseudorandom noise sequence into the numeric ramp output sequence of said phase ramp accumulator for suppressing periodic components of said loop error signal.

14. The frequency synthesizer of claim 7, further including:

a signal quantizer combining said numeric ramp sequence representing the intended phase of controlled frequency and said loop error signal to provide a compressed digital representation thereof to the bit field of said digital-to-analog converter.

15. The frequency synthesizer of claim 7, further including:

a controller responsive to said loop error signal for adaptively nulling spectra noise produced by intermodulation of the reference oscillator and the carrier frequencies.

16. The frequency synthesizer of claim 7, further including:

a generator producing and injecting a pseudorandom noise sequence into the numeric ramp output sequence of said phase ramp accumulator for suppressing periodic components of said loop error signal.

17. The frequency synthesizer of claim 11, further including:

a controller responsive to said loop error signal for adaptively nulling spectra noise produced by intermodulation of the reference oscillator and the carrier frequencies.

18. The frequency synthesizer of claim 11, further including:

a generator for producing and injecting a pseudorandom noise sequence into the numeric ramp output sequence of said phase ramp accummulator for suppressing periodic components of said loop error signal.

19. The frequency synthesizer of claim 12, further including:

a generator for producing and injecting a pseudorandom noise sequence into the numeric ramp output sequence of said phase ramp accummulator for suppressing periodic components of said loop error signal.

20. The frequency synthesizer of claim 14, further including:

a controller responsive to said loop error signal for adaptively nulling spectra noise produced by intermodulation of the reference oscillator and the carrier frequencies.

21. The frequency synthesizer of claim 14, further including:

a generator producing and injecting a pseudorandom noise sequence into the numeric ramp output sequence of said phase ramp accumulator for suppressing periodic components of said loop error signal.

22. The frequency synthesizer of claim 15, further including:

a generator producing and injecting a pseudorandom noise sequence into the numeric ramp output sequence of said phase ramp accumulator for suppressing periodic components of said loop error signal.

23. The frequency synthesizer of claim 17, further including:

a generator producing and injecting a pseudorandom noise sequence into the numeric ramp output siquence of said phase ramp accummulator for suppressing periodic components of said loop error signal.

24. The frequency synthesizer of claim 20, further including:

a generator producing and injecting a pseudorandom noise sequence into the digital input to said digital to analog convertor for suppressing periodic components of said loop error signal.

25. A frequency synthesizer, comprising:

a reference oscillator providing a clock frequency;

a phase ramp accumulator providing a numeric ramp sequence representative of the intended phase of controlled frequency;

a difference phase accumulator accumulating a numeric ramp sequence representative of actual phase of the controlled frequency to provide a loop error signal comprising the linear differences in accumulated phase between said intended phase and said actual phase of said controlled frequency, wherein said loop error signal has a first component signal synchronous with said reference oscillator and a second component signal synchronous with predetermined cycle increments of said controlled frequency;

a signal quantizer providing a quantized composite digital signal representation of a difference between said intended phase of said controlled frequency and an integer cycle accumulation of said controlled frequency and accumulating and summing a quantization error residue with said composite digital signal representation at cycles determined by said clock frequency;

a digital to analog converter receiving said quantized digital representation and providing an analog signal representation thereof;

a linear summing amplifier receiving said analog signal representation and said second component of said loop error signal synchronous with predetermined cycle increments of said controlled frequency and providing a linear sum thereof; and

a controller responsive to said linear sum and said loop error signal synchronous with predetermined cycle increments of said controlled frequency for adaptively nulling spectra noise produced by intermodulation of signal carrier frequencies with said clock frequency.

26. A digital modulation processor providing a signal corresponding to a desired instantaneous carrier frequency deviation, comprising:

means for processing an analog signal sample sequence comprising an upsampling filter wherein an expected unwanted image signal is suppressed;

means for processing a digital signal, including:

shift register means receiving said digital signals providing a plurality of bits corresponding to the most recent digital signal data bits,

a programmable symbol timer providing an address field signal, and

a preprogrammed memory having selected data stored therein readable according to said shift register bits and said timer address field, said memory data comprising the desired digital waveform output; and

means for selecting the output from one of said means for processing an analog signal and means for processing a digital signal, to provide said signal corresponding to the desired instantaneous carrier deviation.

27. A digital demodulator, comprising:

a reference phase sampler for providing a synchronization pulse for a undirectionally zero crossing of a received modulated signal;

a recursive phase filter for smoothing the reference phase sample output; and

a noise squelch detector for providing a squelch control signal in response to an increase of high

frequency click signals present at the output of the recursive phase filter output.

28. A modulation processor/frequency synthesizer comprising:

means for processing an analog signal sample sequence comprising an upsampling filter wherein an expected unwanted image signal is suppressed;

means for processing a digital signal, including;

shift register means receiving said digital signals providing a plurality of bits corresponding to the most recent digital signal data bits,

a programmable symbol timer providing an address field signal, and

a preprogrammed memory having selected data stored therein readable according to said shift register bits and said timer address field, said memory data comprising the desired digital waveform output;

means for selecting the output from one of said means for processing an analog signal and means for processing a digital signal, to provide said signal corresponding to the desired instantaneous carrier deviation;

a reference oscillator providing a periodic oscillator signal precisely defining periodic sampling instants;

a phase ramp accumulator for providing a numeric ramp sequence for representing the intended phase of controlled frequency at said precisely defined periodic sampling instants; and

a difference phase accumulator for accumulating a numerical ramp sequence representing the actual phase of controlled frequency at time instants independent of said precisely defined periodic sampling instants according to level transition instants of said controlled frequency, wherein said digital phase accumulator provides a loop

error signal comprising the linear differences in accumulated phase between the intended phase and the measured phase of said controlled frequency.

29. A digital modulation system comprising:

means for providing a signal transformation between an analog information signal and a digital representation thereof;

means for generating a signal for transmission having a controlled frequency; and

a digital modulation processor responsive to said means for signal transformation for controlling the frequency of said means for generating said signal for transmission at a frequency related to said digital representation, said processor comprising:

means for digitally defining a controlling frequency for said generating means in a closed loop;

means for applying to said loop a digital adjustment corresponding to said digital representation; and

means for applying a filtered analog control from said loop to said generating means.

30. The digital modulation system of claim 29 further comprising:

a digital phase locked loop wherein said digital defining means further includes means for defining the bandwidth of said signal for transmission as a function of digital characteristics of said loop.

31. The digital modulation system of claim 29 wherein said digital modulation processor comprises a VLSI chip.

32. The modulation processor of claim 29 wherein said digital modulation processor further includes means for providing frequency hopping with enhanced slewing of the

digitally defined frequency for fast lock up in response to frequency hops.

33. The modulation system of claim 29 wherein said digital defining means includes means for digitally defining said frequency without an analog type drift in amplitude, emission characteristics, and emission spectrum.

34. The digital modulation system of claim 29 wherein said digital defining means includes a clock and means for isolating harmonics of said clock and the digitally defined frequency from said signal for transmission.

35. The modulation system of claim 34 further including means for producing a linear sum of said clock frequency and said defined frequency avoiding intermodulation frequencies therebetween.

36. The digital modulation system of claim 29 further comprising:

means associated with said digital defining means for identifying the bit resolution of said digitally defined frequency whereby the lowest frequency of disturbance from transients in said closed loop is selectable.

37. The digital modulation system of claim 29 wherein said digital defining means includes means for identifying each zero crossing of said controlling frequency.

38. The digital modulation system of claim 29 wherein said digital defining means includes means for identifying each zero crossing in said digital representation once and only once.

39. The digital modulation system of claim 29 further including:

means associated with said closed loop for digitally identifying phase shift increments;

means for accumulating a phase shift representation for controlling said digitally defined controlling frequency as an accumulation of said defined shifts; and

means for balancing the levels of said digitally defined phase shifts and said accumulated phase shift signals.

40. A digital demodulation system comprising:

means for receiving a signal for demodulation; and

means for generating a digital representation of a frequency in a closed loop including:

means for responding to a clock signal and said received signal for developing a digital representation of the instantaneous phase difference between said received signal and said clock signal; and

means for producing an analog output representation of the information content of said received signal in response to said digitally defined phase difference.

41. The system of claim 39 further including means for delaying said digital definition; and

means for sampling said digital definition and for applying squelch control to the delayed digital representation.

42. The system of claim 39 wherein said digital representation generating means includes means insensitive to analog drifts affecting said digital representation with respect to DC level, center frequency, bias, distortion, and scaling errors.

43. The system of claim 40 further including:

means for generating frequency hops in said received signal;

means for detecting a frequency hop to a received signal including interference which impedes the operation of said developing means; and

means for disabling said analog output representation in response to a detected signal.

44. The system of claim 40 wherein:

said developing means includes means for providing a histogram of zero crossing data of said received signal; and

means are provided for smoothing said histogram according to a median or a centroid of data in said histogram.

Fig. 1

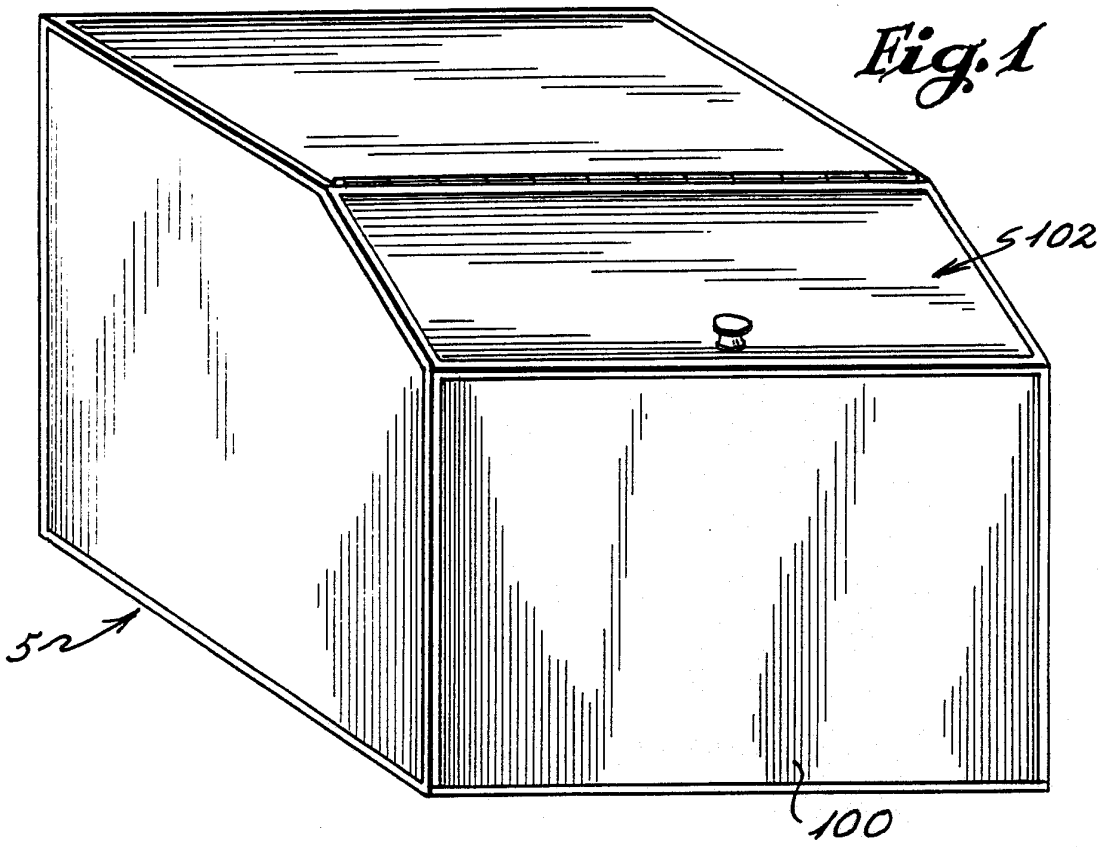
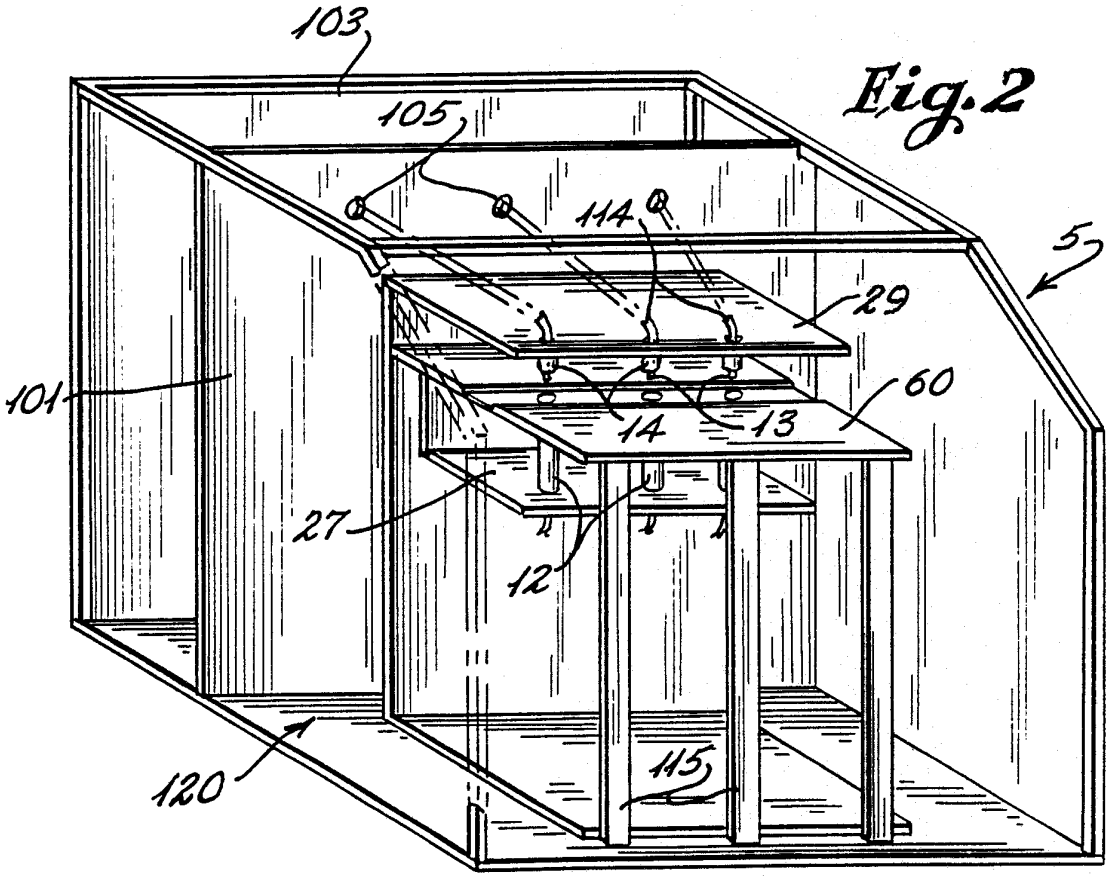


Fig. 2



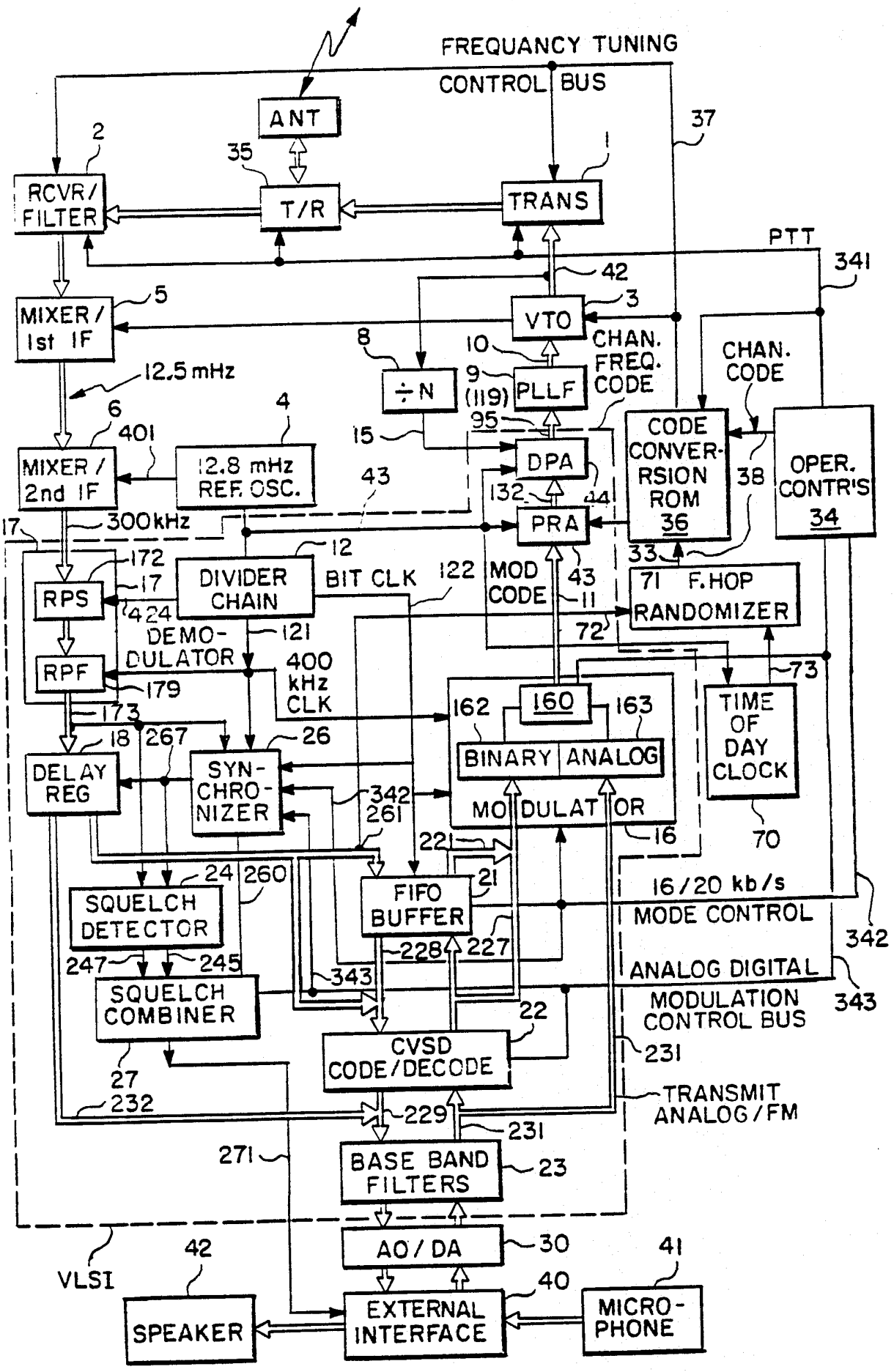

FREQUANCY TUNING
CONTROL BUS
ANT
RCVR/ FILTER
T/R
TRANS
PTT
MIXER/ 1st IF
VTO
÷N
PLLF
CHAN. FREQ. CODE
CHAN. CODE
12.5 mHz
MIXER/ 2nd IF
12.8 mHz REF. OSC.
DPA
PRA
CODE CONVER-RSION ROM 36
OPER. CONTR'S 34
300kHz
RPS
DIVIDER CHAIN
BIT CLK
MOD CODE
F.HOP RANDOMIZER
DEMO-DULATOR
RPF
400 kHz CLK
160
BINARY ANALOG
MODULATOR
TIME OF DAY CLOCK
DELAY REG
SYN-CHRO-NIZER
SQUELCH DETECTOR
FIFO BUFFER
16/20 kb/s
MODE CONTROL
ANALOG DIGITAL
MODULATION CONTROL BUS
SQUELCH COMBINER
CVSD CODE/DECODE
TRANSMIT ANALOG/FM
BASE BAND FILTERS
AO/DA
VLSI
SPEAKER
EXTERNAL INTERFACE
MICRO-PHONE

FIG.1

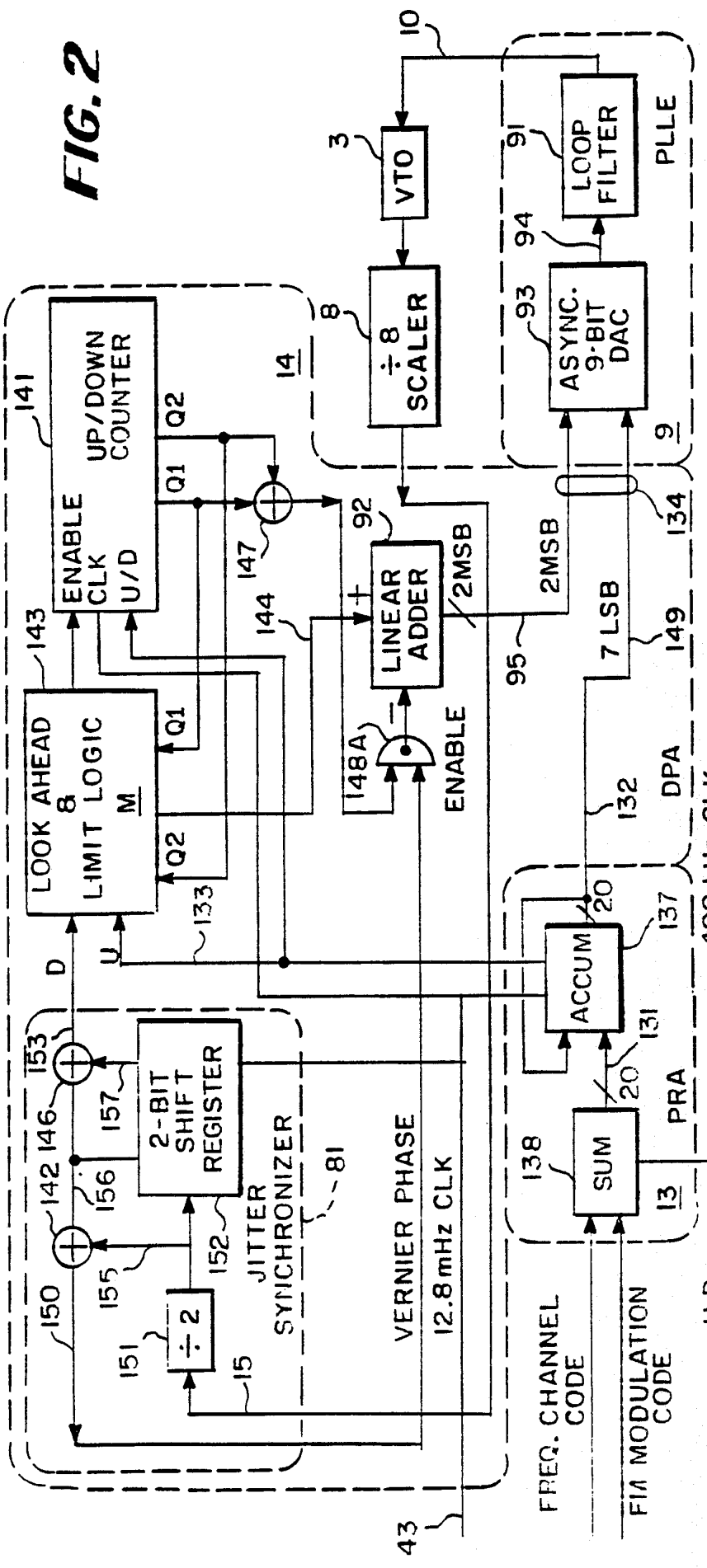


FIG. 2

U,D Q2,Q1	00	01	10	11
00	0	0	1	0
01	0	1	1	0
10	0	1	1	0
11	0	1	0	0

ENABLE, "E"

LIMIT LOGIC, 143

U,D Q2,Q1	00	01	10	11
00	0	0	0	0
01	0	0	1	0
10	1	0	1	1
11	1	1	1	1

MSB, "M"

FIG. 2A

FIG. 2B

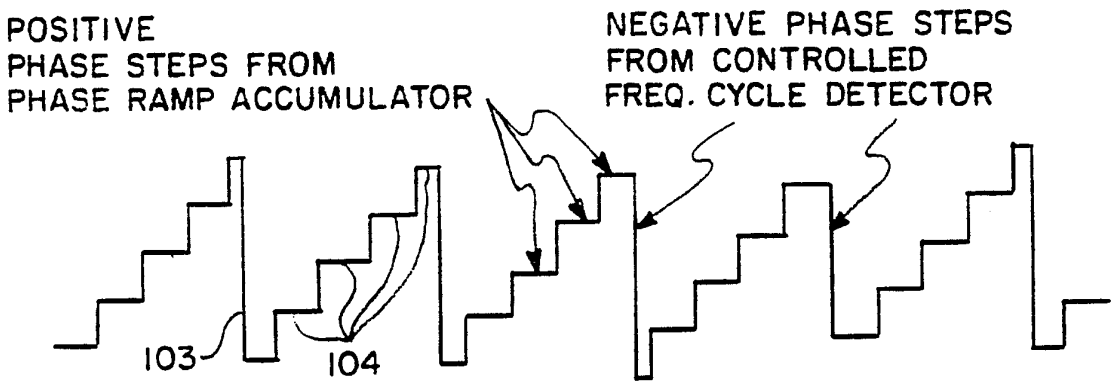


FIG. 3 A

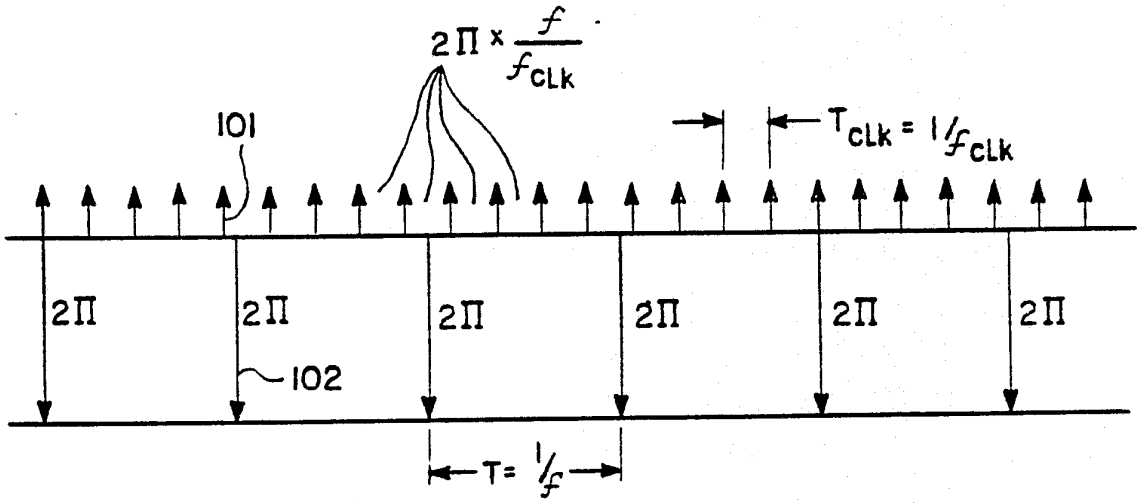


FIG. 3 B

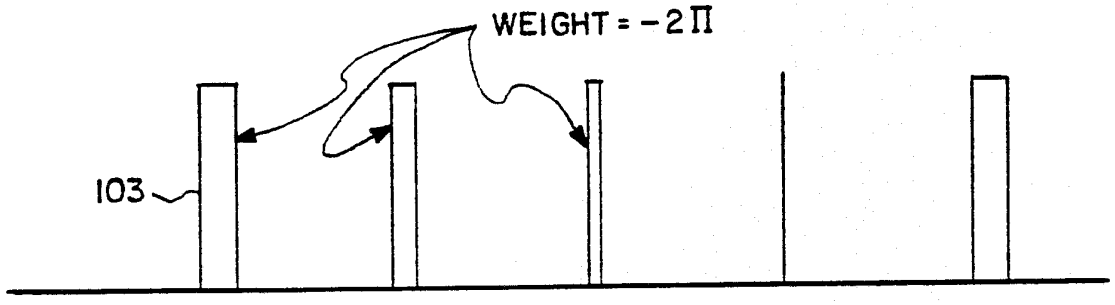


FIG. 3 C

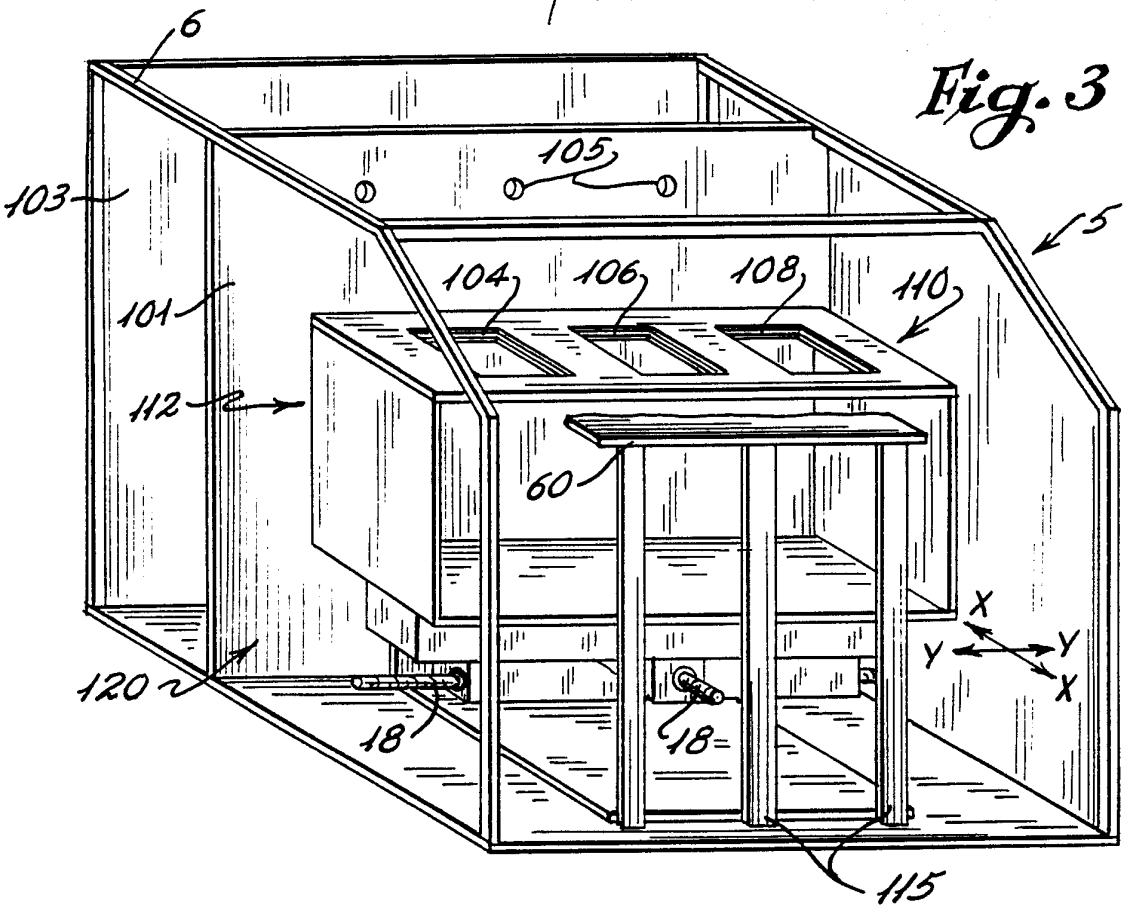

6
103
105
5
101
104
106
108
110
112
60
X
Y
Y
X
120
18
18
115

Fig. 3

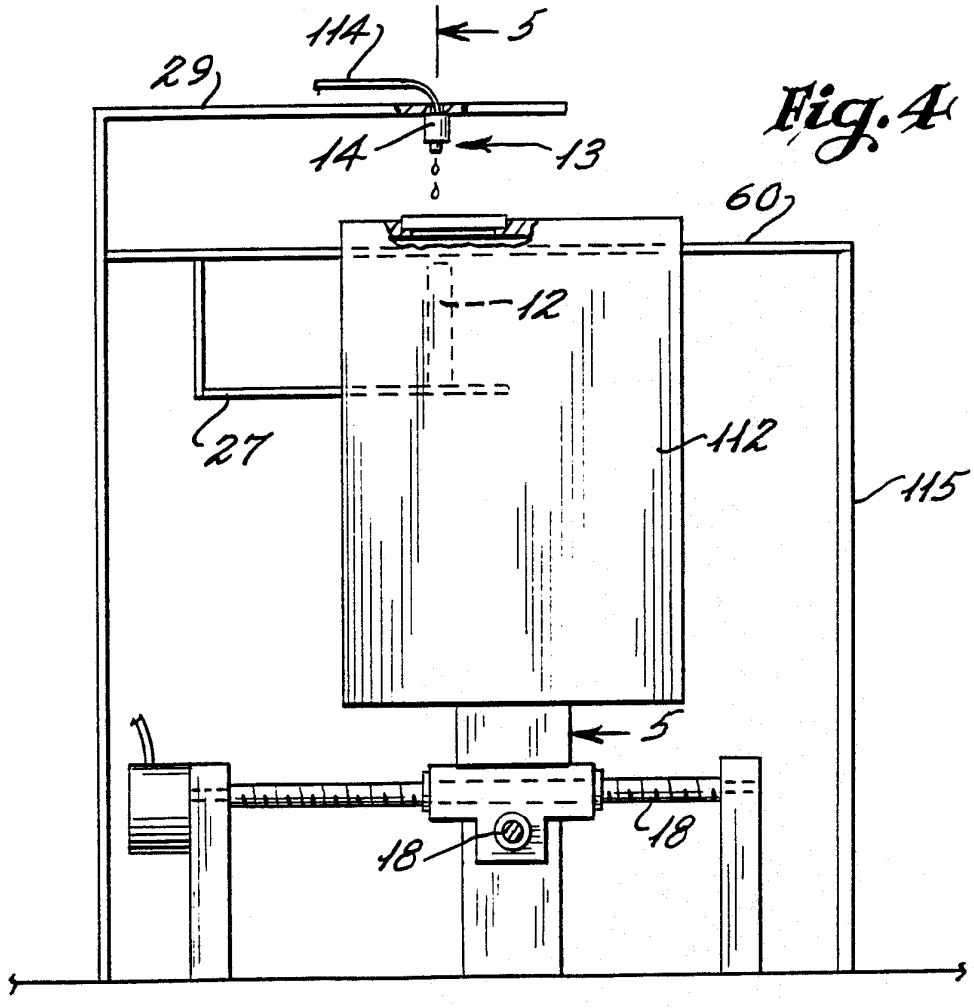

114
5
29
14
13
60
12
27
112
115
5
18
18

Fig. 4

Fig. 5

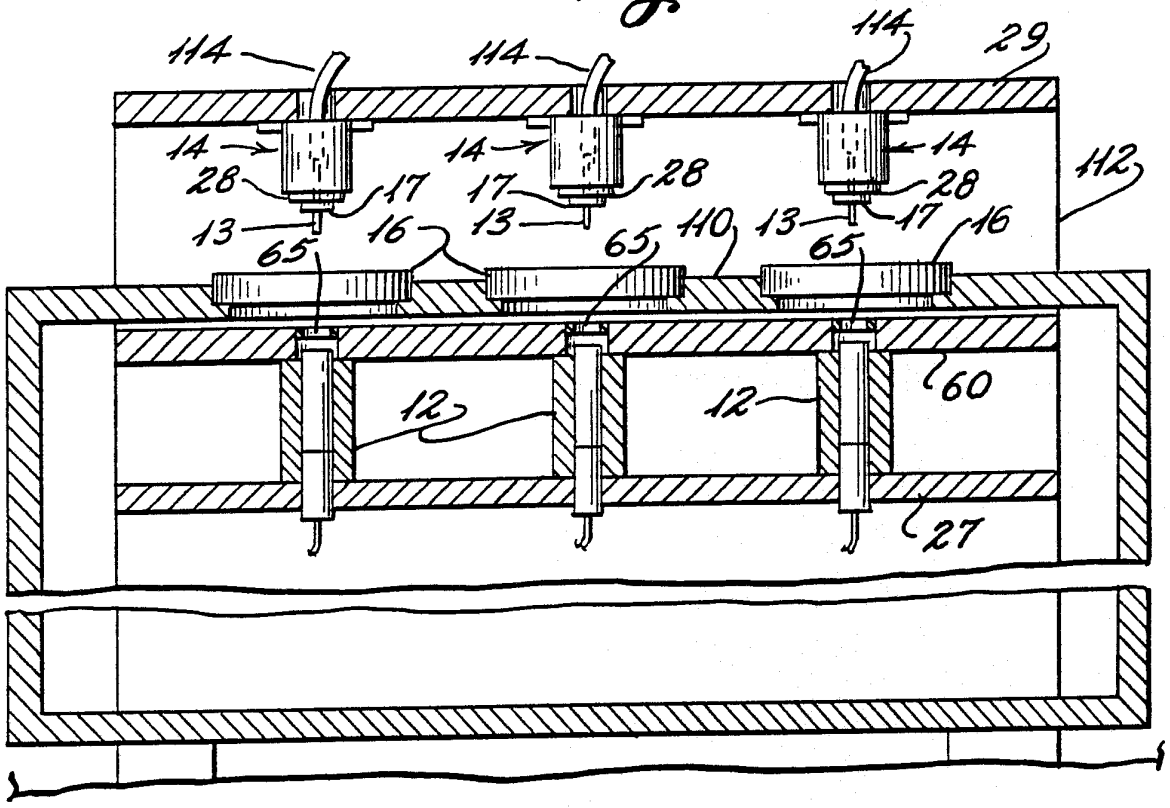
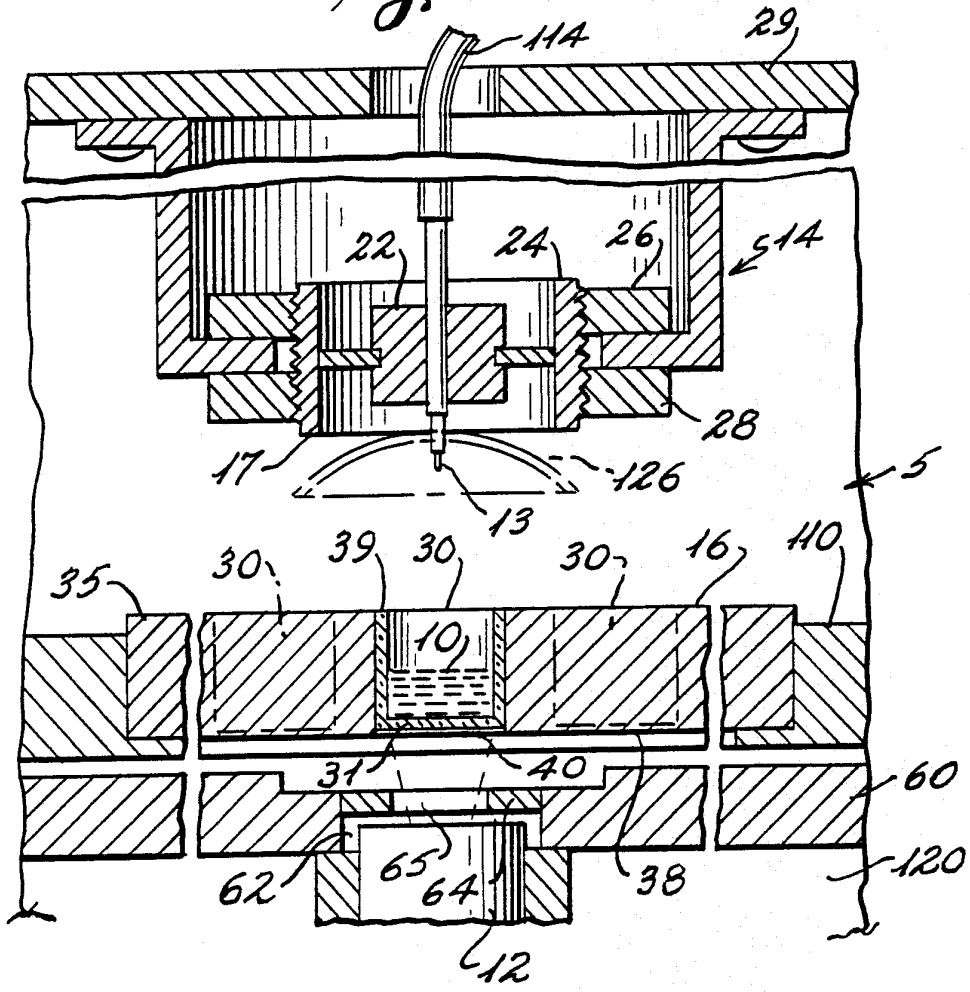

114
114
114
29
14
14
14
28
17
17
28
28
17
112
13
16
13
65
110
13
65
16
65
60
12
12
27

Fig. 6


114
29
22
24
26
14
28
17
126
13
5
35
30
39
30
30
16
110
10
31
40
60
62
65
64
38
120
12

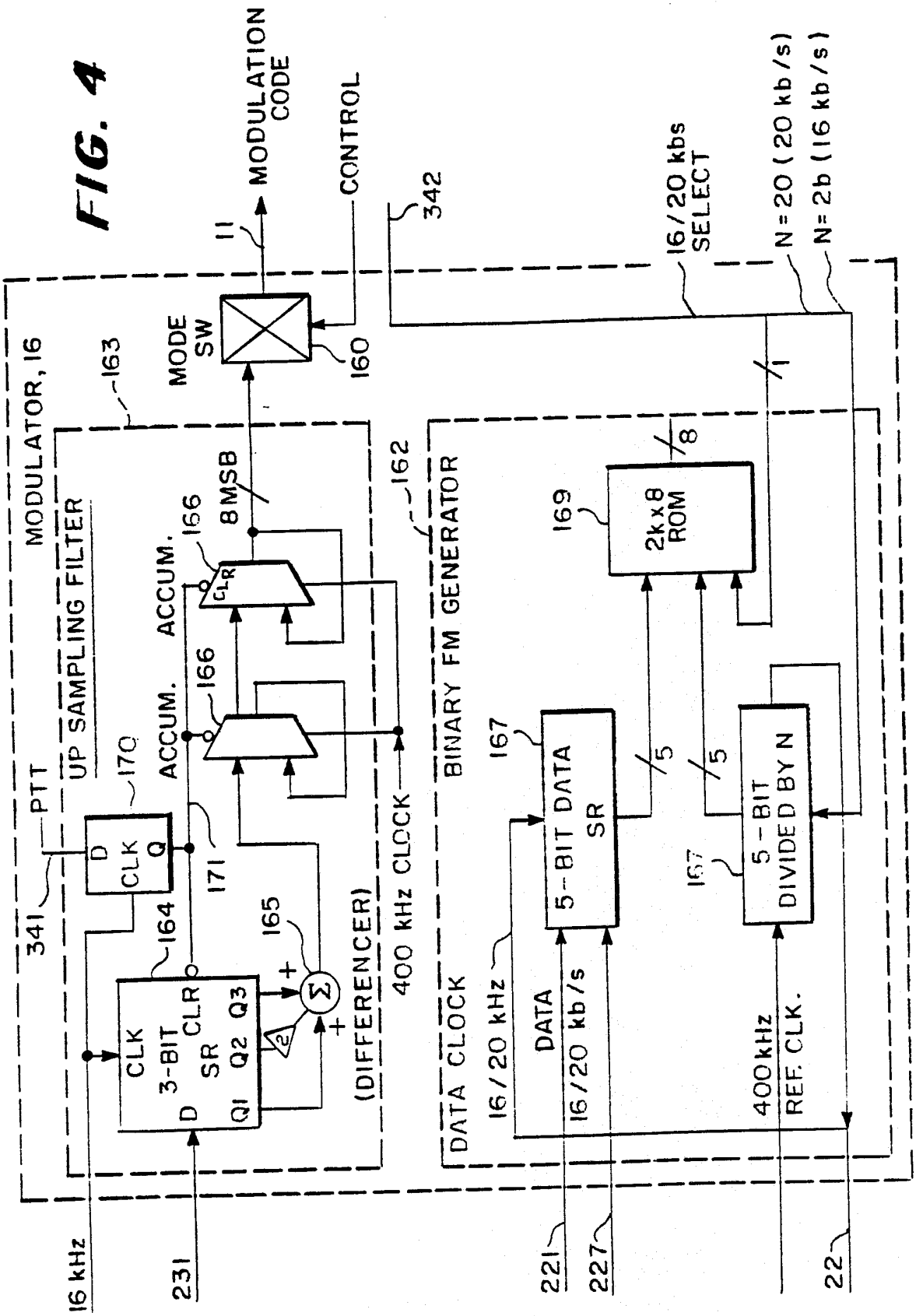
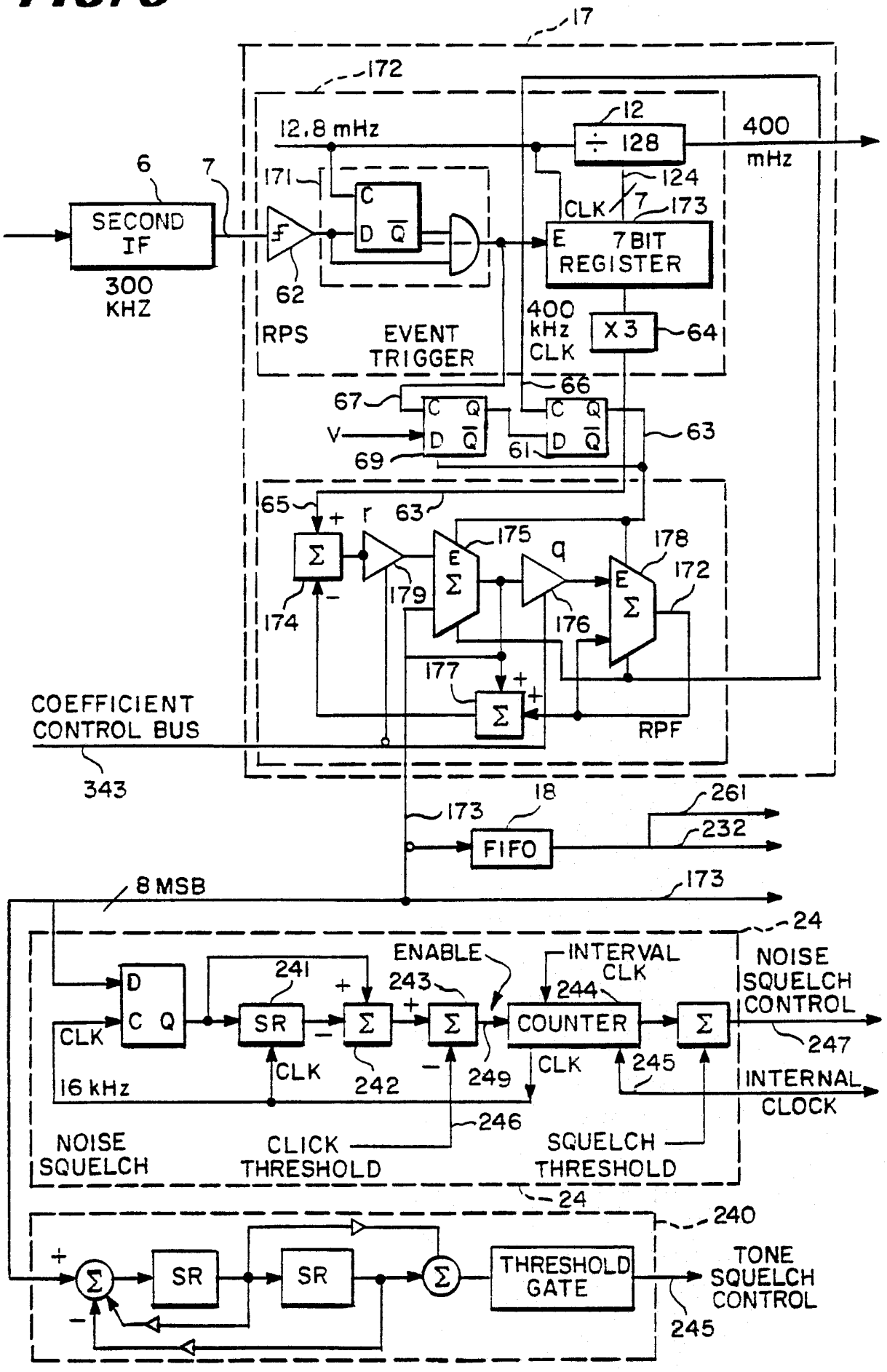

MODULATOR, 16
UP SAMPLING FILTER
163
MODE SW
160
11
MODULATION CODE
CONTROL
342
16/20 kbs SELECT
N=20 (20 kb/s)
N=2b (16 kb/s)
1
8MSB
166
ACCUM.
CLR
166
ACCUM.
170
PTT
D
CLK
Q
341
171
164
CLK
3-BIT
SR
CLR
D
Q1
Q2
Q3
165
Σ
(DIFFERENCER)
400 kHz CLOCK
162
BINARY FM GENERATOR
169
2k x 8 ROM
8
167
5-BIT DATA SR
5
5
167
5-BIT DIVIDED BY N
DATA CLOCK
16/20 kHz
DATA
16/20 kb/s
400 kHz REF. CLK.
16 kHz
231
221
227
22

FIG. 4

FIG. 5


17
172
12.8 mHz
÷ 128
12
400 mHz
6
7
171
SECOND IF
300 KHZ
62
C
D Q
124
CLK
7
173
E 7 BIT REGISTER
RPS
EVENT TRIGGER
400 kHz CLK
X 3
64
66
67
V
69
61
63
65
r
175
q
178
172
179
174
176
177
COEFFICIENT CONTROL BUS
343
RPF
18
261
232
FIFO
8 MSB
24
ENABLE
INTERVAL CLK
NOISE SQUELCH CONTROL
241
243
244
247
SR
COUNTER
CLK
16 kHz
242
249
245
INTERNAL CLOCK
246
NOISE SQUELCH
CLICK THRESHOLD
SQUELCH THRESHOLD
240
THRESHOLD GATE
TONE SQUELCH CONTROL

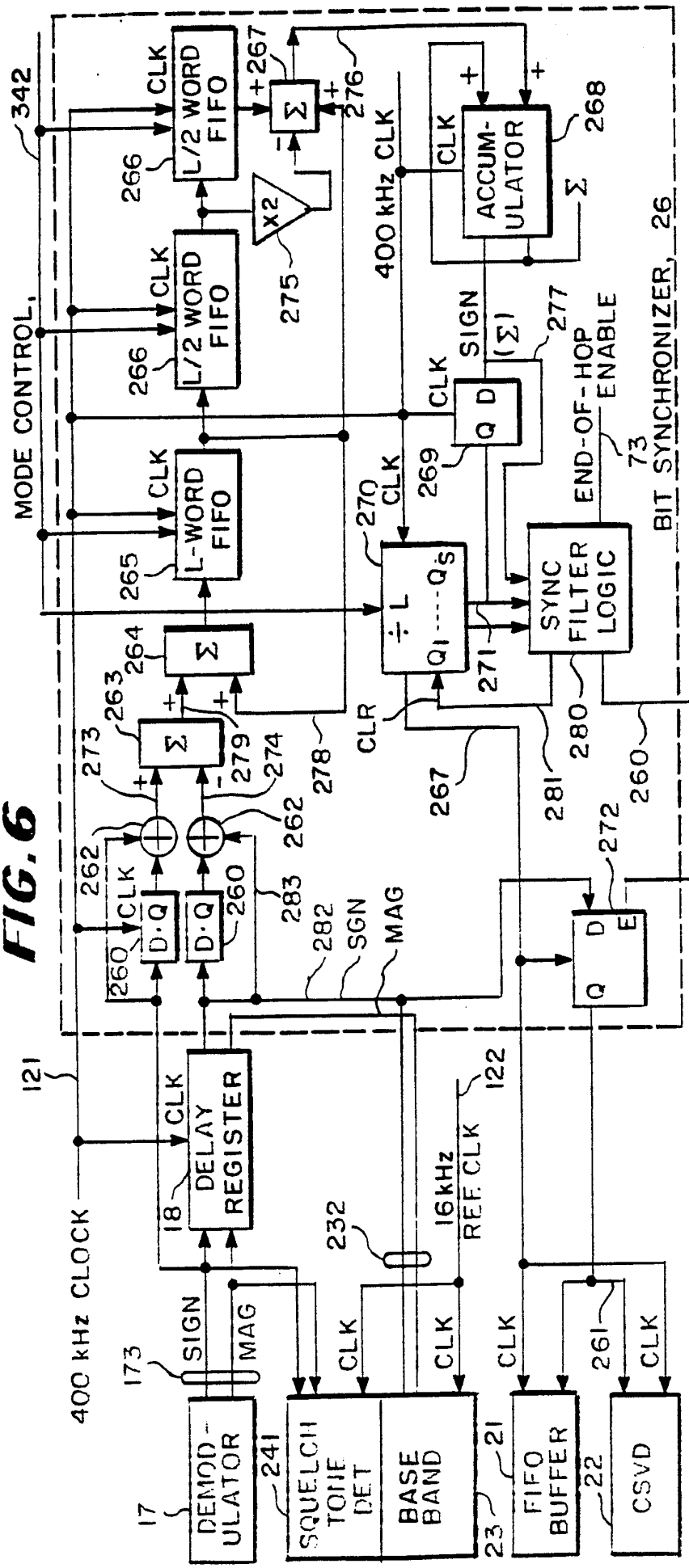
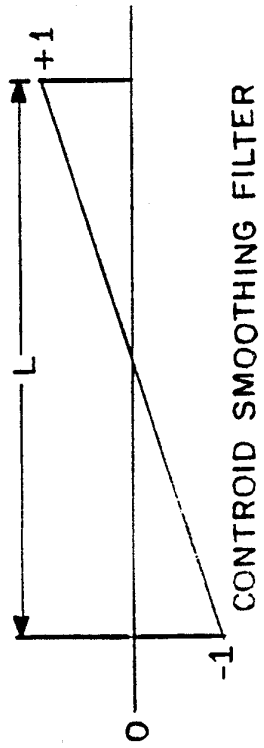
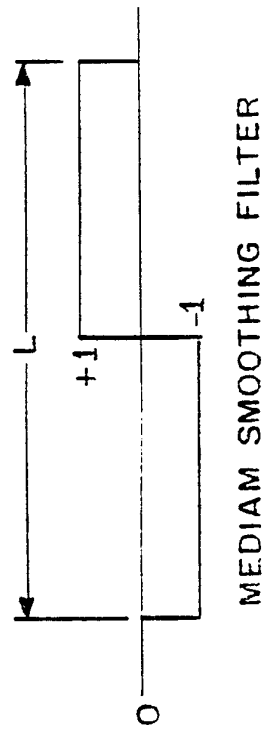


FIG. 6



CONTROID SMOOTHING FILTER
CYCLIC IMPULSE RESPONSE

FIG. 7B



MEDIAM SMOOTHING FILTER
CYCLIC IMPULSE RESPONSE

FIG. 7A

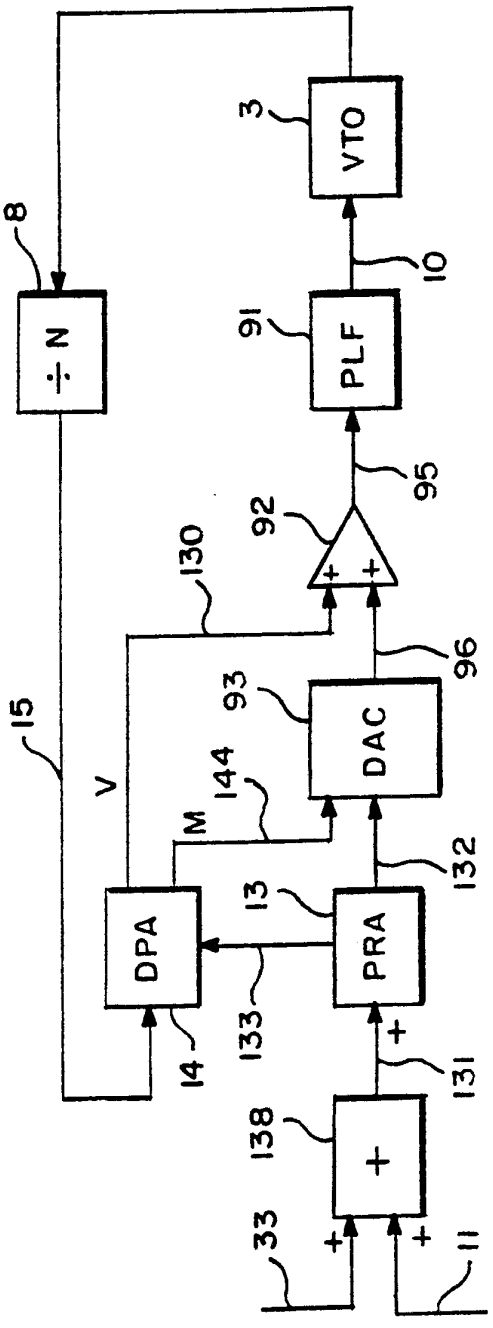

÷ N
8
15
V
M
DPA
14
PRA
13
133
131
138
+
33
11
DAC
93
144
132
130
92
96
95
PLF
91
10
VTO
3

FIG. 8

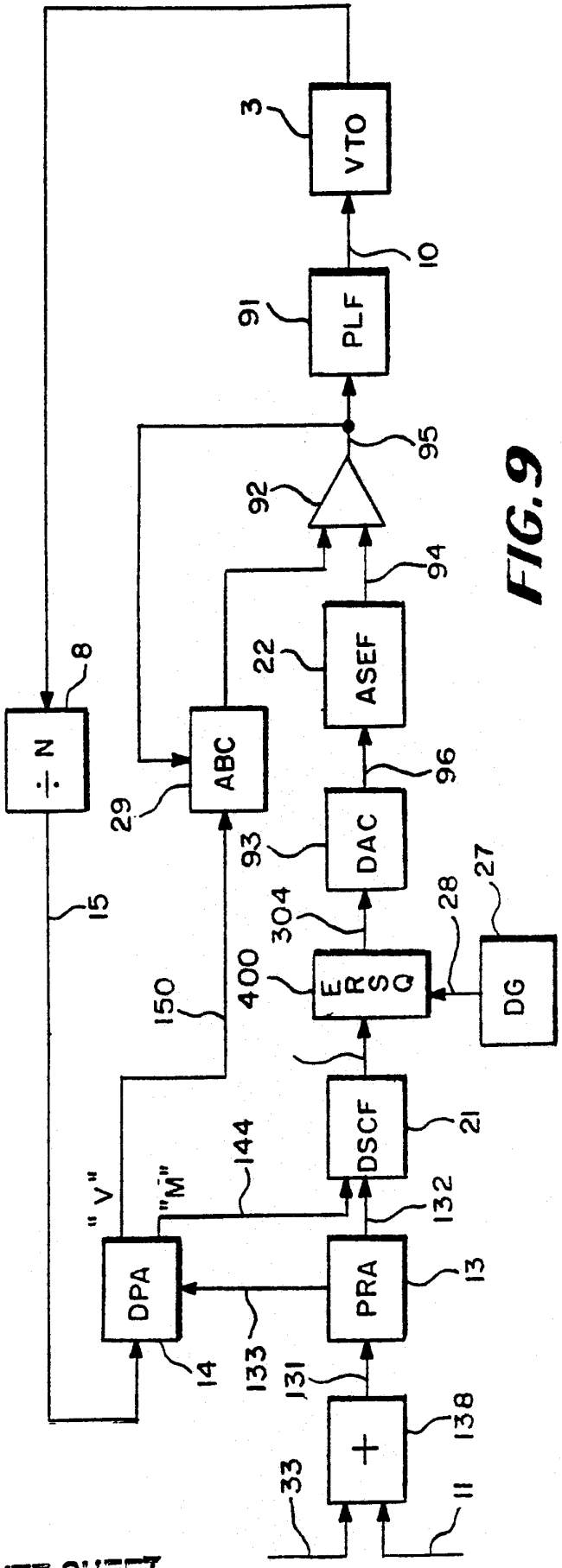

÷ N
8
15
"V"
"M"
DPA
14
PRA
13
133
131
138
+
33
11
DSCF
21
132
144
150
ERSQ
400
304
28
DG
27
DAC
93
96
ABC
29
ASEF
22
94
92
95
PLF
91
10
VTO
3

FIG. 9

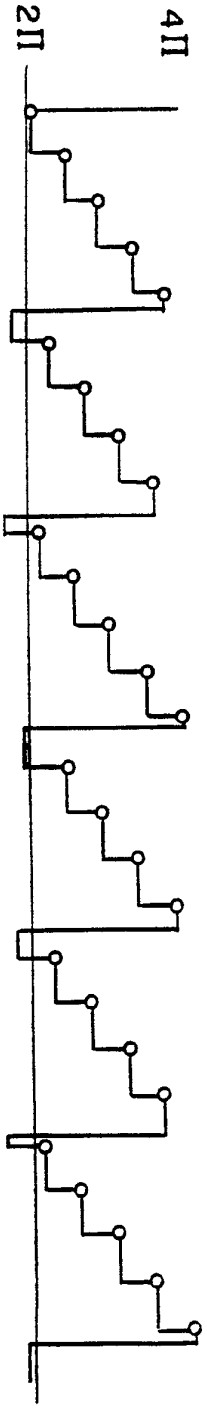


FIG. 10 A

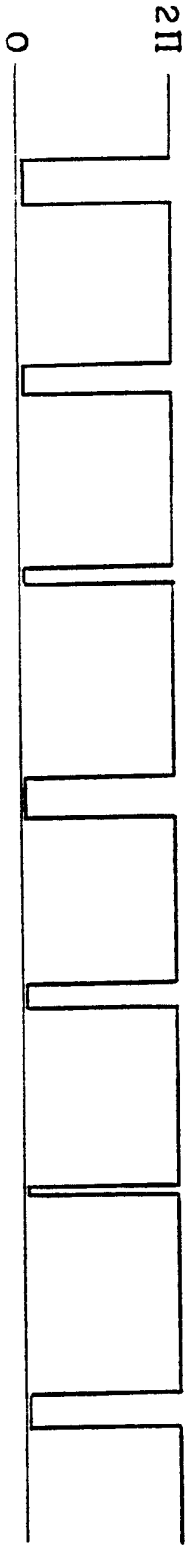


FIG. 10 B

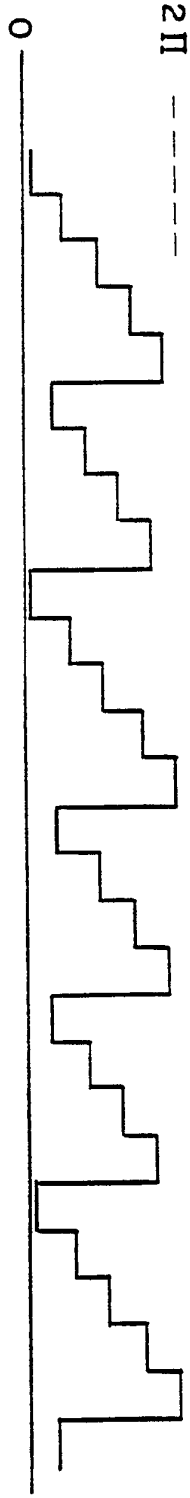


FIG. 10 C

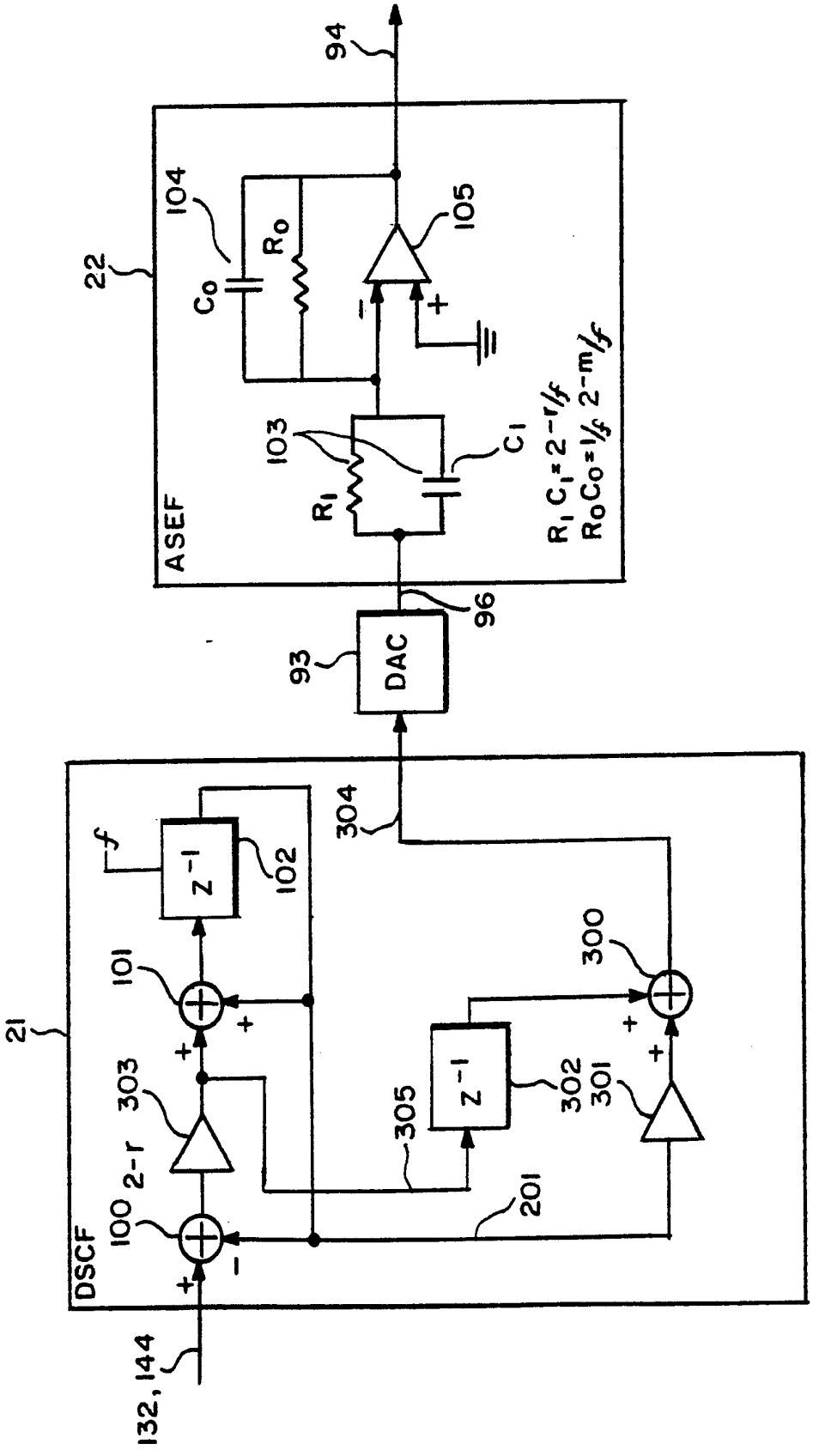

94
104
C_0
R_0
105
22
103
R_1
C_1
ASEF
$R_1 C_1 = 2^{-r}/f$
$R_0 C_0 = 1/f\ 2^{-m}/f$
96
93
DAC
304
f
Z^{-1}
102
101
300
21
303
2-r
305
Z^{-1}
302
301
100
201
DSCF
132, 144

FIG. 11

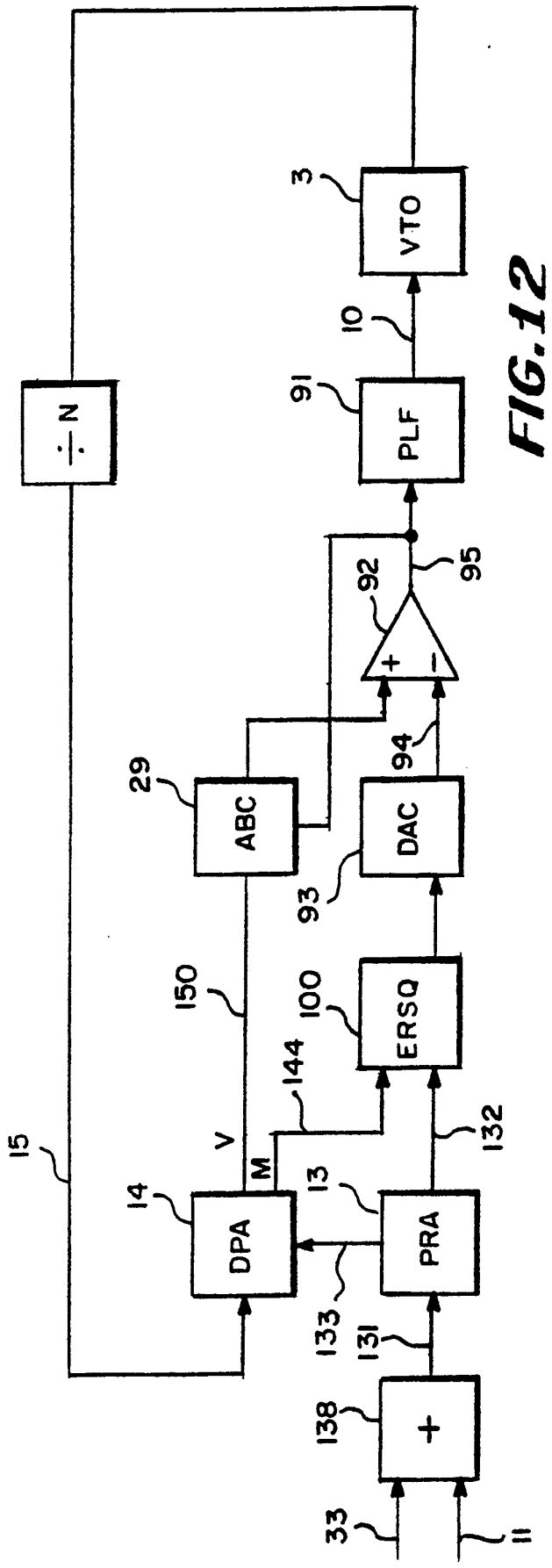


FIG. 12

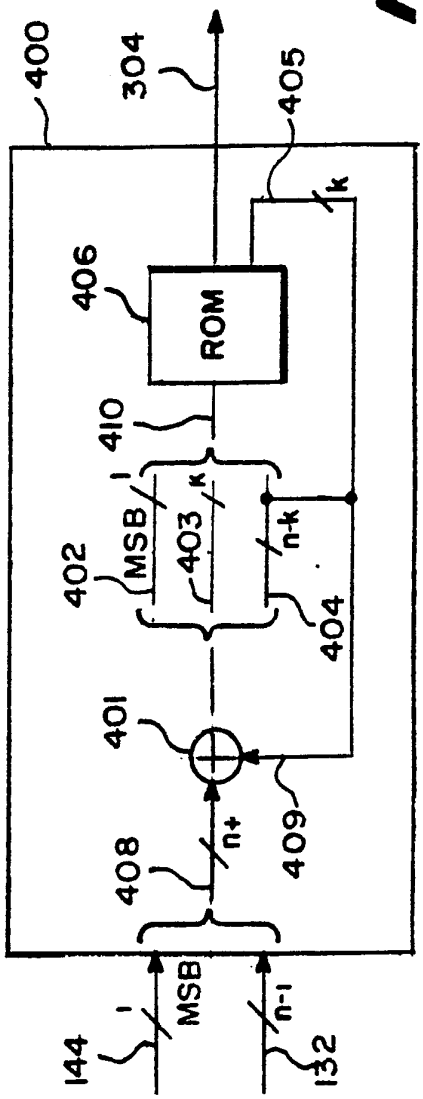


FIG. 12A

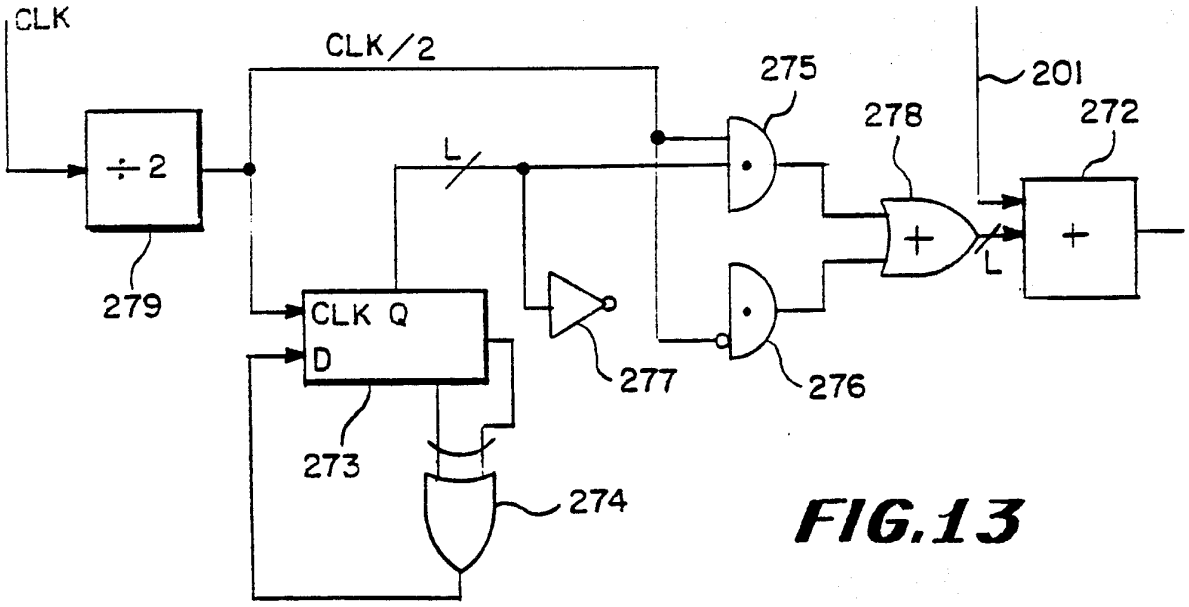

CLK
÷2
279
CLK/2
L
CLK Q
D
273
274
277
275
276
278
201
272
L

FIG.13

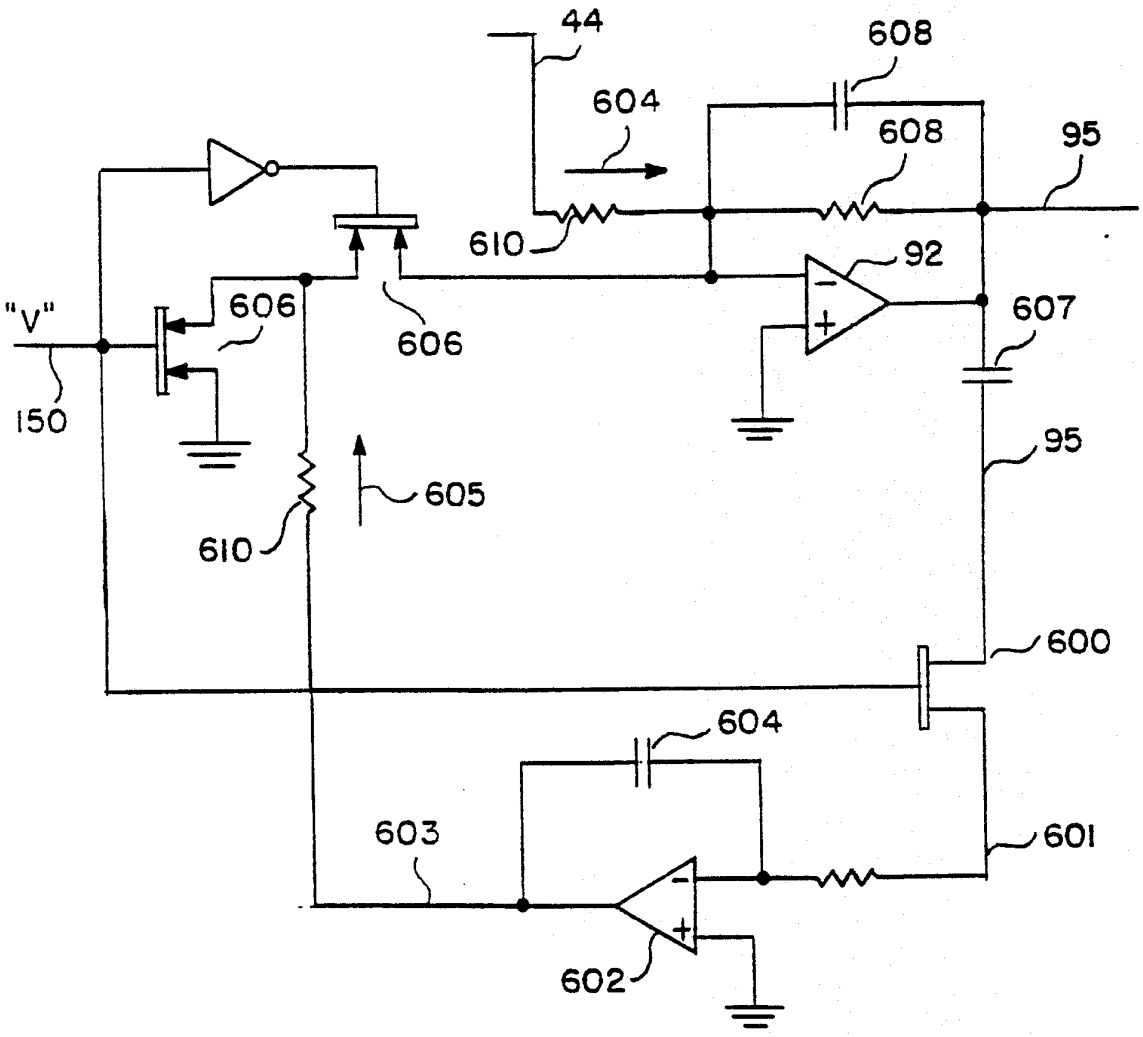

44
604
608
608
95
610
92
"V"
606
606
607
150
605
610
95
600
604
603
601
602

FIG.14

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/05988

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT CL.(5): H04B 1/38 H04L 5/16
US CL.: 375/7

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	375/7.8, 82, 104, 94 328/14 331/1A, 16 455/113 364/719, 720, 721

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X,P	US, A, 4,893,317 (CRITCHLOW et al.) 09 January 1990 See Fig. 1 and Abstract.	1-3
Y	US, A, 4,034,210 (COE) 05 July 1977, See Fig. 1 and column 2, lines 24-49.	4-6 and 12
Y	US, A, 4,879,729 (SALEMBIER et al.) 07 November 1989 See Fig. 3.	27
Y	US, A, 4,679,098 (CLOKE) 29 September 1987, See Fig. 1.	27
A	US, A, 4,490,688 (BORRAS et al.) 25 December 1984	4-25,26,28-39,41,42
A	US, A, 4,206,425 (NOSSEN et al.) 03 June 1980	4-25,26,28-39,41,42

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
03 JANUARY 1991	01 MAR 1991
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	STEPHEN CHIN

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers ..... , because they relate to subject matter [1] not required to be searched by this Authority, namely:

2. ☐ Claim numbers ..... , because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [1], specifically:

3. ☐ Claim numbers_____, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☒ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

Group I Claims 1-3, drawn to a Transceiver, classified in 375/7.

Group II Claims 4-26, 28-39, 41 and 42, drawn to a Digital Processor/ Frequency Synthesizer, classified in 375/82.

Group III Claims 27, 40, 43 and 44, drawn to a Digital Demodulator, classified 375/104.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application. Telephone Practice

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.