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[Continued on next page]

(54) Title: LINK TRAINING IN MULTIMEDIA INTERFACES

(57) Abstract: A source device and a sink device perform a link training process on a multimedia interface cable. The sink device includes one or more request registers. During the link training process, the sink device stores request codes in the request registers. Each request code is a request for the source device to perform a certain action. The source device reads the request codes and performs the corresponding actions. For example, if the source device reads request codes to send one or more training pattems, then the source device sends the training patterns over the multimedia link. In response to receiving the training patterns, the sink device can selects one or more updated request codes (e.g., to send different training patterns or to adjust link parameters, such as the link rate or a pre-emphasis level).

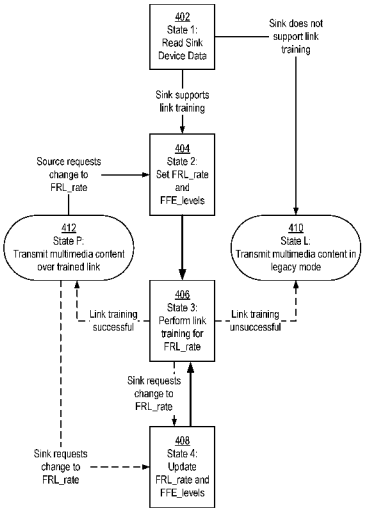

FIG. 4

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LINK TRAINING IN MULTIMEDIA INTERFACES

BACKGROUND

1. FIELD OF THE DISCLOSURE

[0001] This disclosure pertains in general to data communications, and more specifically to link training in multimedia interfaces.

2. DESCRIPTION OF THE RELATED ART

[0002] Different types of multimedia data are often transmitted from a source device to a sink device over an interface cable, such as an HDMI cable. Data transmission over interface cables can be subject to a number of parameters, such as pre-emphasis levels for an equalizer at the source device, bit rate, and (for interface cables that provide multiple data channels) the number of active channels. Conventionally, these parameters are set at fixed values. However, setting fixed parameter values ignores the fact that multimedia data transmission happens under a wide range of circumstances, such as transmission over different cable lengths and the effect of varying levels of electromagnetic interference, intersymbol interference, and radio frequency interference, and each set of circumstances may benefit from a different set of parameter values.

SUMMARY

[0003] Embodiments of the present disclosure are related to performing a link training process on a data interface cable capable of carrying data from source device to sink device. For example, the data interface cable may be a multimedia cable, such as an HDMI cable. In one embodiment, the sink device includes a memory device with one or more request registers. During the link training process, the sink device provides one or more request codes by storing the request codes in the request registers. Each request code is a request for the source device to perform a certain action (e.g., to send a particular training pattern or to adjust a parameter of the multimedia link between the source device and the sink device. The source device is configured to read the request codes and perform the action identified by the request code. For example, if the source device reads request codes to send one or more training patterns, then the source device sends the training patterns over the multimedia link. In response to receiving the training patterns, the sink device can select one or more updated request codes (e.g., to send different training patterns or to adjust link parameters, such as the link rate or a pre-emphasis level).

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The teachings of the embodiments disclosed herein can be readily understood by considering the following detailed description in conjunction with the accompanying drawings.

[0005] Figure (FIG.) 1 is a high-level block diagram of a system for data communications, according to one embodiment.

[0006] FIG. 2A is a high-level block diagram of a source interface device, according to one embodiment.

[0007] FIG. 2B is a high-level block diagram of a sink interface device, according to one embodiment.

[0008] FIG. 3A is high-level block diagram of the sink device data of the sink interface device, according to one embodiment.

[0009] FIG. 3B is a high-level block diagram of the link data of the sink interface device, according to one embodiment.

[0010] FIG. 4 is a flow chart illustrating the operation of the link training control circuit and the link training circuit, according to one embodiment.

[0011] FIG. 5 is an interaction diagram illustrating a link training process, according to one embodiment.

DETAILED DESCRIPTION

[0012] The Figures (FIG.) and the following description relate to various embodiments by way of illustration only. It should be noted that from the following discussion, alternative embodiments of the structures and methods disclosed herein will be readily recognized as viable alternatives that may be employed without departing from the principles discussed herein. Reference will now be made in detail to several embodiments, examples of which are illustrated in the accompanying figures. It is noted that wherever practicable similar or like reference numbers may be used in the figures and may indicate similar or like functionality.

[0013] FIG. 1 is a high-level block diagram of a system 100 for data communications, according to one embodiment. The system 100 includes a source device 110 communicating with a sink device 115 through one or more interface cables 120, 150, 180. Source device 110 transmits multimedia data streams (e.g., audio/video streams) to the sink device 115 and also exchanges control data with the sink device 115 through the interface cables 120, 150, 180. In one embodiment, source device 110 and/or sink device 115 may be repeater devices.

[0014] Source device 110 includes physical communication ports 112, 142, 172 coupled to the interface cables 120, 150, 180. Sink device 115 also includes physical communication ports 117, 147, 177 coupled to the interface cables 120, 150, 180. Signals exchanged between the source device 110 and the sink device 115 across the interface cables 120, 150, 180 pass through the physical communication ports 112, 142, 172.

[0015] Source device 110 and sink device 115 exchange data using various protocols. In one embodiment, interface cable 120 represents a High Definition Multimedia Interface (HDMI) cable. The HDMI cable 120 supports differential signals transmitted via data0+ line 121, data0- line 122, data1+ line 123, data1- line 124, data2+ line 125, data2- line 126, data3+ link 127, and data3- line 128. Each differential pair of lines forms a logical communication channel that can carry one or more multimedia data streams. In other embodiments, interface cable 120 (or a different interface cable, such as interface cables 150, 180) may contain additional differential pairs of lines that form additional logical communication channels. For example, interface cable 120 may further contain data4+ line and data4- line that form a fourth logical communication channel.

[0016] The HDMI cable may be capable of operating in multiple operating modes, and data3+ line 127 and data3- line 128 may perform different functions in different operating modes. For instance, the HDMI cable may be capable of operating in a legacy mode (e.g., transition minimized differential signaling with 8b10b encoding) and a standard mode (e.g., 16b18b encoding). In the legacy mode, data3+ line 127 and data3- line 128 operate as differential clock lines clock+ and clock-. In the standard mode, data3+ line 127 and data3- line 128 form a fourth logical communication channel that also is also capable of carrying one or more multimedia data streams. In standard mode, the clock signal is embedded in the signal being carried by the logical communication channels.

[0017] The HDMI cable 120 may further include Consumer Electronics Control (CEC) control bus 129, Display Data Channel (DDC) bus 130, power 131, ground 132, hot plug detect (HPD) 133, and four shield lines 134 for the differential signals. In some embodiments, the sink device 115 may utilize the CEC control bus 129 for the transmission of closed loop feedback control data to source device 110.

[0018] In one embodiment, interface cable 150 represents a Mobile High-Definition Link (MHL) cable. The MHL cable 150 supports differential signals transmitted via data0+ line 151 and data0- line 152, which form a single logical communication channel for carrying multimedia data streams. In some embodiments of MHL, there may be more than a single pair of differential data lines. In some versions of MHL, embedded common mode clocks

are transmitted through the differential data lines. The MHL cable 150 may further include a control bus (CBUS) 159, power 160 and ground 161. The CBUS 159 carries control data such as discovery data, configuration data and remote control commands.

[0019] The source device 110 includes a source control device 190 and the sink device 115 includes a sink control device 192. Examples of source control device 190 and sink control device 115 are integrated circuits (ICs) or other types of devices. The source control device 190 may include a transmitter that processes multimedia data streams and outputs signals for the multimedia data streams across the interface cables 120, 150, 180 to the sink control device 192. The sink control device 192 may include a receiver that receives the multimedia data streams and prepares the multimedia data streams for display. The source control device 190 and sink control device 192 may also exchange and process control data across the interface cables 120, 150, 180.

[0020] In one embodiment, a representation of the source device 110, the sink device 115, or components within the source device 110 or sink device 115 may be stored as data in a non-transitory computer-readable medium (e.g., hard disk drive, flash drive, optical drive, random access memory). These descriptions may be behavioral level, register transfer level, logic component level, transistor level, or layout geometry-level descriptions.

[0021] Embodiments of the present disclosure relate to performing link training when initializing a link on an interface cable. In the embodiments provided in the present disclosure, link training is performed when initializing a link on the HDMI cable 120 for operation in standard mode. In other embodiments, link training may be performed when operating in both standard mode and legacy mode. The link training process establishes configuration parameters for the link, such as the clock frequency, the number of active data lanes, and pre-emphasis levels for each data lane. In other embodiments, the link training process may be applied to other protocols such as MHL and DISPLAYPORT.

[0022] FIG. 2A is a high-level block diagram of a source interface device 200, according to one embodiment. The source interface device 200 prepares multimedia data for transmission over the multimedia lanes 210 through 213. Prior to beginning multimedia transmission, the source interface device 200 may perform link training tasks, such as sending training patterns over the multimedia lanes 210 through 213 and adjusting pre-emphasis levels for the multimedia lanes 210 through 213. In one embodiment, the source interface device 200 includes a multimedia transmission circuit 202, an equalization (EQ) circuit 204, a training pattern circuit 206, and a source link training circuit 208.

[0023] The multimedia transmission circuit 202 performs several tasks associated with preparing multimedia data, such as video and audio data, for transmission to the sink interface device over the multimedia lanes 210 through 213. In one embodiment, the multimedia transmission circuit 202 receives uncompressed audio and video data from a decoder, packetizes the data, scrambles the packetized data, and encodes the scrambled data with 16b18b encoding (or 8b10b encoding if operating in legacy mode). In an embodiment where the multimedia link includes multiple multimedia lanes, the multimedia transmission circuit 202 divides the encoded data into lanes and provides the data for each lane to the equalization circuit 204.

[0024] The equalization circuit 204 receives one or more lanes of encoded data from the multimedia transmission circuit 202 or training patterns for one or more lanes from the training pattern circuit 206, performs equalization on each lane of the received data, and sends the equalized data over one or more of the multimedia lanes 210 through 213 to the sink interface device 250. In one embodiment, the equalization circuit 304 includes a pre-emphasis circuit for each lane, and the pre-emphasis circuits may be configured to perform pre-emphasis for each lane based on different pre-emphasis parameters. The equalization circuit 304 may further include hardware registers for storing the pre-emphasis parameters for each pre-emphasis circuit. At a high level, a pre-emphasis circuit adds a short positive boost to transitions from zero to one and a short negative boost to transitions from one to zero in order to reduce inter-symbol interference in a communication link. In one embodiment, the pre-emphasis circuits perform feed forward equalization (FFE), and the pre-emphasis parameters include an FFE level specifying the magnitude of the boost.

[0025] The training pattern circuit 206 generates training patterns for transmission on one or more of the multimedia lanes 210 through 213. The training pattern circuit 206 is capable of generating a plurality of different predefined training patterns. Each training pattern is associated with a unique training pattern identifier. In one embodiment, each training pattern identifier is a four-bit binary value between 1 (binary 0001) and 9 (binary 1001). An example of training pattern identifiers and associated training patterns are provided below with reference to FIG. 3B and Table 3. The circuit 206 receives a training pattern identifier from the source link training circuit 208. When providing the training pattern identifier to the training pattern circuit 206, the source link training circuit 208 also specifies the lane on which the associated training pattern is to be transmitted. The training pattern circuit 206 generates the associated training pattern and provides the training patterns to the equalization circuit 204 to be transmitted on the specified lane.

[0026] The source link training circuit 208 reads data on the sink interface device 250 over a bidirectional channel 220 and performs tasks associated with a link training process based on the data. For example, the source link training circuit 208 may read a request code that specifies a request to transmit a particular training pattern on one of the multimedia lanes 210 through 213 (e.g., the request code may be a training pattern identifier that is stored in a request register associated with a particular multimedia lane 210 through 213). In response to reading the request codes, the source link training circuit 208 provides the corresponding training pattern identifier to the training pattern circuit 206. An example of the different request codes that may be read by the source link training circuit 208 is provided below with reference to FIG. 3B and Table 2. The operation of the source link training circuit 208 is described in detail with respect to FIG. 4 and FIG. 5.

[0027] The source interface device 200 is connected to the sink interface device 250 via a multimedia link that includes multimedia lanes 210 through 213 and bidirectional channel 220. In one embodiment, multimedia lanes 210 through 213 and bidirectional channel 220 are part of an HDMI cable, such as the HDMI cable 120 shown in FIG. 1. For example, multimedia lane 0 210 may correspond to data0+ line 121, data0- line 122, and one of the shield lines 134 of the HDMI cable 120. Similarly, the other multimedia lanes 211 through 213 may correspond to the other differential pairs 123 through 128 and the other shield lines 134. Meanwhile, the bidirectional channel 220 may correspond to Display Data Channel (DDC) bus 130. In other embodiments, the multimedia link may include a different number of multimedia lanes. For example, the multimedia link may include a single multimedia lane, two multimedia lanes, or five multimedia lanes.

[0028] In an embodiment where the multimedia link is an HDMI cable 120, the multimedia lanes 210 through 213 are capable of operating in a legacy mode or a standard mode. In the legacy mode, the first three multimedia lanes 210 through 212 carry multimedia data that is transmitted with transition minimized differential signaling (TMDS) (a form of 8b10b encoding), and the fourth multimedia lane 213 carries a clock signal. In the standard mode (also referred to as Fixed Rate Link (FRL) mode), all four multimedia lanes 210 through 213 are capable of carrying multimedia data, and the multimedia is transmitted with 16b18b encoding. The standard mode operates at one of six different link rates, with each link rate specifying a number of active multimedia lanes and a bitrate for the active multimedia lanes. Each link rate is associated with a link rate identifier. Table 1 provides an example of link rate identifiers and the bitrate and number of lanes corresponding to each link rate.

Table 1

Link Rate Identifier (Decimal)	Link Rate Identifier (Binary)	Number of Active Lanes	Bitrate per Lane (Gbps)
1	0001	3	3
2	0010	3	6
3	0011	4	6
4	0100	4	8
5	0101	4	10
6	0110	4	12

[0029] As noted in Table 1, the link rates identified by identifiers 1 (binary 0001) and 2 (binary 0010) make use of three of the four multimedia lanes 210 through 213. When operating at these link rates, the first three multimedia lanes 210 through 212 carry multimedia data (e.g., the multimedia lanes implemented by data lines 121 through 126 in FIG. 1) while the fourth multimedia lane 213 remains inactive. As used herein, the term active multimedia lanes refers to the multimedia lanes that are carrying multimedia data. Thus, the multimedia link has three active lanes when operating at the link rates identified by identifiers 1 and 2, and the multimedia link has four active lanes when operating at the other link rates shown in Table 1. In other embodiments, the multimedia link is capable of operating at additional or different link rates. For example, the multimedia link may be capable of operating at link rates that specify one or two active lanes (rather than three or four active lanes, as shown in Table 1), or at link rates that specify a different bitrate per lane, such as 1 Gbps, 4 Gbps, or 9 Gbps.

[0030] FIG. 2B is a high-level block diagram of a sink interface device 250, according to one embodiment. The sink interface device 250 receives multimedia data over the multimedia lanes 210 through 213 and prepares the multimedia data for playback. The sink interface device 250 also controls a link training process that establishes and/or changes parameters for the transmission of multimedia data over the multimedia lanes 210 through 213. In one embodiment, the sink interface device 250 includes a multimedia reception circuit 252, a link training control circuit 254, sink device data 256, and link data 258.

[0031] The multimedia reception circuit 252 receives multimedia data over the multimedia lanes 210, 211, 212, 213 and performs several tasks to prepare the multimedia

data for playback. For example, after receiving the multimedia data, the multimedia reception circuit 252 performs 16b18b decoding on the multimedia data, depacketizes the decoded data, and descrambles the depacketized data to recreate the uncompressed multimedia data that the multimedia transmission circuit 202 received as input. The multimedia reception circuit 252 may then output the uncompressed multimedia data for playback.

[0032] The link training control circuit 254 controls the link training process by writing data, such as request codes for the multimedia lanes 210 through 213, in the link data 258. For example, the link training control circuit 254 writes a request code to a request register associated with one of the multimedia lanes 210 through 213 to request that a particular training pattern be transmitted over the multimedia lane. As described above, the source link training circuit 208 can then read the request code and configure the training pattern circuit 206 to generate and send the training pattern over the multimedia lane.

[0033] The sink device data 256 is a data structure that stores information about the capabilities of the sink device. In one embodiment, the sink device data 256 is the Extended Display Identification Data (EDID) or Enhanced EDID (E-EDID) of the sink device and is stored in a memory device such as a serial PROM or EEPROM on the sink device. The contents of the sink device data 256 are described in further detail below with reference to Fig. 3A.

[0034] The link data 258 is a data structure that stores data about the current status of the multimedia link and also stores data that controls the operation of the source interface device 200. The link data 258 is stored on a memory device comprising a plurality of registers. In an embodiment where the multimedia link is an HDMI connection, the link data 258 is the Status and Control Data Channel Structure (SCDCS). In one embodiment, the link data 258 is stored on the same memory device as the sink device data 256. In another embodiment, the link data 258 is a stored on a separate memory device. The contents of the link data 258 are described in further detail below with reference to FIG. 3B.

[0035] Although the link data 258 is shown in FIG. 2B as part of the sink interface device 250, in other embodiments the link data 258 may instead be implemented in a memory device that is part of the source interface device 200. In these embodiments, the link training control circuit 254 is communicatively coupled to the link data 258 via the bidirectional channel 220, whereas the source link training circuit 208 is communicatively coupled to the link data 258 via an internal connection within the source interface device 200.

[0036] FIG. 3A is high-level block diagram of the sink device data 256 of the sink interface device 250, according to one embodiment. The sink device data 256 includes Max_FRL_rate 302, which is a data item specifying the maximum link rate that the sink device can support. In an embodiment where the multimedia link is an HDMI cable, Max_FRL_rate 302 is a four-bit field specifying the link rate identifier (as provided in Table 1) of the maximum link rate that the sink device can support. For example, if Max_FRL_rate 302 has a decimal value of 5, then the sink device supports the link rates associated with link rate identifiers 1, 2, 3, 4, and 5 (as provided in Table 1) but does not support the link rate associated with link rate identifier 6.

[0037] The value of Max_FRL_rate 302 may also indicate whether the sink device supports link training. For example, in an embodiment where the multimedia link is an HDMI cable, Max_FRL_rate 302 may have a value of 0, which indicates that the sink device supports HDMI operation in legacy mode but not in standard mode (i.e., the sink device does not support any of the link rates shown in Table 1). Because link training is not performed in HDMI legacy mode, a value of 0 for Max_FRL_rate 302 indicates that the sink device does not support link training, whereas a value of 1 to 6 indicates that the sink device does support link training.

[0038] Although not shown in FIG. 3A, the sink device data 256 may also include additional data items that specify other capabilities of the sink device. For example, the sink device data 254 may include data items specifying the maximum horizontal and vertical image sizes supported by the sink device and the range of colors that the sink device is capable of displaying.

[0039] FIG. 3B is a high-level block diagram of the link data 258 of the sink interface device 250, according to one embodiment. The link data 258 includes three categories of data items: update flags 350, configuration parameters 360, and status flags 380.

[0040] Each update flag 350 is a value (e.g., a one-bit binary value) that is associated with an instruction for the source interface device 200. The source link training circuit 208 is configured to periodically poll the update flags (e.g., once every 250 milliseconds). If one of the update flags has a first value (e.g., a value of 1) when its value is polled by the source link training circuit 208, then the source link training circuit 208 performs the instruction associated with the update flag 350. Thus, the update flags 350 provide a method for the link training control circuit 254 control source interface device 200. Throughout this disclosure, it is stated that a value of 1 in an update flag 350 causes the source link training circuit 208 to perform the associated instruction. In other embodiments, the values in one or more of the

update flags 350 may be reversed (i.e., a value of 0, rather than a value of 1, causes the source link training circuit 208 to perform the associated instruction).

[0041] The update flags 350 include FLT_ready 351, FLT_update 352, and FRL_start 353. The link training control circuit 254 writes a value of 1 to FLT_ready 351 to indicate to the source interface device 200 that the sink interface device 250 is ready for the link training process to begin. The control circuit 254 writes a value of 1 to FLT_update 352 to indicate to the source interface device 200 that the control circuit 254 has updated the value in one or more of the LTP_req status flags 390 through 393 (described in further detail below). The control circuit 254 writes a value of 1 to FRL_start 353 to indicate to the source interface device 200 that the link training process has been completed successfully and that the sink device is ready to receive multimedia data over the multimedia lanes 210 through 213. The instructions that the source link training circuit 208 performs in response to each of these update flags 350 is described below with reference to FIGS. 4 and 5.

[0042] The configuration parameters 360 are parameters that describe the current data transmission parameters of the multimedia link. The configuration parameters 360 include FRL_rate 361, FFE_levels 362, Lane0_LTP_set 370, Ch1_LTP_set 371, Ch2_LTP_set 372, and Ch3_LTP_set 373. FRL_rate 361 is the link rate identifier for the current link rate. For example, if the example link rates and link rate identifiers provided in Table 1 are used, then FRL_Rate 361 is a four-bit register storing the link rate identifier for the link rate at which the link is currently operating. FFE_levels 362 specifies the number of pre-emphasis settings for the equalization circuit 204. In one embodiment, FFE_levels 362 is a two-bit register.

[0043] The source link training circuit 208 stores the current status of each lane in the parameters Lane0_LTP_set 370, Lane1_LTP_set 371, Lane2_LTP_set 372, and Lane3_LTP_set 373 (hereinafter referred to collectively as the lane setting flags 370 through 373). For instance, if the source interface device 200 is sending a particular training pattern over a multimedia lane, the source link training circuit 208 stores the associated training pattern identifier in the corresponding lane. Examples of training pattern identifiers and their associated training patterns are provided below in Table 2.

Table 2

Training Pattern Identifier (Decimal)	Training Pattern Identifier (Binary)	Training Pattern
1	0001	A continuous string of 1's without 16b18b encoding
2	0010	A continuous string of 0's without 16b18b encoding
3	0011	A 100-MHz clock pattern (e.g, if the bitrate for the lanes is 6 Gbps, then the training pattern is 30 1's followed by 30 0's)
4	0100	A Nyquist frequency pattern (e.g., an alternating pattern of 1's and 0's)
5	0101	A first predefined sequence of 4096 18-bit characters
6	0110	A second predefined sequence of 4096 18-bit characters
7	0111	A third predefined sequence of 4096 18-bit characters
8	1000	A fourth predefined sequence of 4096 18-bit characters
9	1001	Continuous repeat of a scrambler reset character

[0044] The status flags 380 are values that describe the current status of the sink interface device 250. In one embodiment, the status flags 380 can be read and written by the link training control circuit 254 but can only be read (and cannot be written) by the source link training circuit 208. The status flags 380 include Lane0_LTP_req 390, Lane1_LTP_req 391, Lane2_LTP_req 392, and Lane3_LTP_req 393 (hereinafter referred to collectively as the request registers 390 through 393). Each request register 390 through 393 is associated with one of the four multimedia lanes 210 through 213 and stores a request code for the associated lane. As referred to herein, a request code specifies an action to be performed at the source interface device 200. When a request code read by the source link training circuit 208, the source link training circuit 208 performs the specified action. For example, a request code can request: a change to pre-emphasis level for a lane; a change to a parameter associated with swing control, jitter control, or rise/fall time; a change to the signal encoding performed by the multimedia transmission circuit 202; different error correction methods; the transmission of a link training pattern over a lane; or termination of the link training process and the beginning of multimedia transmission. In one embodiment, each lane request register

390 through 393 is a four-bit register, and each request code is a four bit value. Examples of request codes are provided below in Table 3.

Table 3

Request Code (Decimal)	Request Code (Binary)	Request
0	0000	No Action Requested
1 to 9	0001 to 1001	Send Training Pattern Whose Identifier Matches the Request Code
14	1110	Change the Pre-Emphasis Level
15	1111	Change the Link Rate

[0045] FIG. 4 is a flow chart illustrating the operation of the link training control circuit 254 (hereinafter referred to as the "control circuit 254") and the source link training circuit 208 (hereinafter referred to as the "source circuit 208"), according to one embodiment. The control circuit 254 and the source circuit 208 implement a finite state machine that performs link training by transitioning between six states 402 through 412.

[0046] The finite state machine enters state 1 402 after an interface cable is connected between the source 110 and the sink 115. Immediately after an interface cable is connected, the source 110 and the sink 115 may perform one or more link initialization steps before the finite state machine enters state 1 402. For example, in an embodiment where the interface cable is an HDMI cable 120, the source 110 raises power 131 to 5 V upon detecting that the HDMI cable 120 has been plugged in to both the source 110 and the sink 115. In response, the sink 115 raises HPD 133 to high, which signals to the source 110 that the source 110 can read the sink device data 256. Once the sink raises HPD 133 to high, the finite state machine enters state 1 402. In an embodiment where the interface cable is a different type of cable, such as a DISPLAYPORT cable, a different series of link initialization steps may occur after the cable is plugged in and before the finite state machine enters state 1.

[0047] In state 1 402, the source circuit 208 reads the sink device data 256 over the bidirectional channel 220. In particular, the source circuit 208 reads Max_FRL_rate 302 to determine whether the sink device supports link training. For example, an embodiment where the multimedia link is an HDMI cable 120, Max_FRL_rate 302 has a value of 0 if the sink device supports operation in legacy mode but does not support operation in standard mode, and thus does not support link training. In this example, the source circuit 208

transitions to state L 410 if Max_FRL_rate 302 has a value of 0 and transitions to state 2 404 if Max_FRL_rate has a value other than 0 (i.e., a value between 1 and 6).

[0048] In state 2 404, the source circuit 208 and the control circuit 254 perform several actions to prepare the multimedia link for the link training process. The control circuit 254 writes a value of 1 to FLT_ready 351 to indicate that the sink device is ready for the link training process to begin, and then the control circuit 254 transitions to state 3 404. Meanwhile, the source circuit 208 periodically reads FLT_ready 351 while operating in state 2 404. If the source circuit 208 reads a value of 1 in FLT_ready 351, the source circuit 208 selects a link rate and writes an identifier for the selected link rate (e.g., as provided in Table 1) in the FRL_rate register 361. The source circuit 208 selects a link rate that is less than the maximum link rate specified by Max_FRL_rate 302 and is also fast enough to support transmission of the multimedia content. In one embodiment, the source circuit 208 reads metadata associated with the content and selects a link rate that is fast enough to transmit the content, but no faster than the maximum link rate supported by the sink device (i.e., as specified by Max_FRL_rate 302). While operating in state 2 404, the source circuit 208 also selects a value for FFE_levels and stores the value in the FFE_levels register 362. After selecting and writing values for FRL_rate 361 and FFE_levels 362, the source circuit 208 transitions to state 3 406.

[0049] In state 3 406, the control circuit 254 and the source circuit 208 perform the link training process. During the link training process, the control circuit 254 provides request codes to the source circuit 208 by storing request codes in the request registers 390 through 393 and writes a value of 1 to the FLT_update register 352. Meanwhile, the source circuit 208 periodically polls the FLT_update register 352. If the source circuit 208 reads a value of 1 during one of these polling requests, the source circuit 208 reads the request registers 390 through 393, performs the task associated with the request codes, and resets of value of FLT_update 352 to 0. This allows the control circuit 254 to control the operation of the source circuit 208 by providing instructions (in the form of request codes) for the source interface device 200 to perform certain actions. The operation of state 3 406, including the circumstances under which the control circuit 254 transitions from state 3 406 to state 4 408, state L 410, and state P 412, is described in further detail below with respect to FIG. 5.

[0050] In state 4 408, the source circuit sends 208 control signals to other components of the source interface device 200 to stop transmission at the current link rate and begin the link training process for a new link rate. The source circuit 208 also writes an identifier for the new link rate (e.g., as provided in Table 1) to FRL_rate register 361 and writes an updated

value to the FFE_levels register 362. After storing new values in FRL_rate 361 and FFE_levels 362, the source circuit 208 transitions to state 3 406 so that link training can be performed at the new link rate.

[0051] If the source circuit 208 and the control circuit 254 transition to state L 410, then the link training process has failed, and the source circuit 208 prepares the link for multimedia transmission in legacy mode. For example, the source circuit 208 writes a value of 0 to the FRL_rate register 361 to indicate that the link will begin operating in legacy mode, and the multimedia transmission circuit 202 begins multimedia transmission in legacy mode (e.g., with 8b10b encoding). The source circuit 208 and the control circuit 254 remain in state L 410 while multimedia transmission takes place in legacy mode.

[0052] If the source circuit 208 and the control circuit 254 transition to state P 412, then the link training process was successful, and the source circuit 208 and control circuit 254 prepare the link for multimedia transmission in standard mode (e.g., fixed rate link mode). In particular, the control circuit 254 writes a value of 1 to the FRL_start register 353 to indicate that the sink device is ready to receive multimedia data over the multimedia lanes 210 through 213. Meanwhile, the source circuit 208 is configured to periodically poll the FRL_start register 353 and, upon reading a value of 1, the source circuit 208 configures the multimedia transmission circuit 202 to begin transmitting multimedia content at the link rate specified by the link rate identifier stored in the FRL_rate register 361. The source circuit 208 also writes a value of 0 to each of the lane setting flags 370 through 373 to indicate that the source device is no longer transmitting a training pattern over any of the multimedia lanes 210 through 213. The source circuit 208 and the control circuit 254 remain in state P 412 while multimedia transmission takes place in standard mode.

[0053] While multimedia transmission takes place in standard mode, either the source circuit 208 or the control circuit 254 can initiate the link training process again. For instance, the source circuit 208 can initiate the link training process at a different link rate if the source circuit 208 detects that new multimedia content is to be transmitted (e.g., if the user switches from displaying 4K multimedia content to 8K multimedia content). In one embodiment, the source circuit 208 initiates the link training process by writing a value of 15 (binary 1111) in the lane setting flags 370 through 373 to indicate to the sink device that the source device has initiated link training at a different link rate. After writing the value in the lane setting flags 370 through 373, the source circuit 208 transitions to state 2 404. The control circuit 254 also transitions to state 2 404. The sink may also perform actions to prepare for the change to the link rate, such as freezing the screen and muting the audio.

[0054] The control circuit 254 can also initiate the link training process at a different link rate. For example, if control circuit 254 detects that the quality of the received multimedia data has dropped during the course of multimedia transmission (e.g., due to a change in the levels of interference in the environment surrounding the interface cable), then the control circuit 254 may initiate link training at a lower link rate. In one embodiment, the control circuit 254 writes a value of 1 to the FLR_update register 352 and a request code of 15 (binary 1111) to each of the request registers 390 through 393 to indicate to the source circuit that the sink device is initializing link training at a different link rate. The control signal can alternatively initiate the link training at the same link rate but with a different value in the FFE_levels register 362 (e.g., a different number of pre-emphasis settings). In one embodiment, the control circuit 254 writes a value of 1 to the FLR_update register 352 and a request code of 14 (binary 1110) to each of the request registers 390 through 393 to indicate to the source circuit that the sink device is initializing link training at a different FFE setting.

[0055] FIG. 5 is an interaction diagram illustrating a link training process, according to one embodiment. As discussed above with reference to FIG 4, the link training process takes place when the source circuit 208 and the control circuit 254 are operating in state 3 406. At a high level, the link training process involves executing a plurality of link training loops. In each loop, the control circuit 254 provides requests for each active multimedia lane to the source circuit 208, and the source circuit 208 performs the actions specified by the requests. If any of the requests specified the transmission of a training pattern, the control circuit 254 receives the training pattern, evaluates the quality of the received training pattern, and selects one or more updated request codes to provide to the source circuit 208. The updated request codes can request different training patterns or request a change to one of the link parameters. In this manner, the link training process can iterative change link parameters until the received training patterns are of satisfactory quality.

[0056] The process begins when the control circuit 254 writes 502 an initial set of request codes to the request registers 390 through 393. In one embodiment, the initial set of request codes request a clock training pattern on one or more of the active multimedia lanes 210 through 213 (e.g., training patterns 3 and/or 4 in Table 2) so that the control circuit 254 can perform clock recovery. The control circuit 254 also writes 504 a value of 1 to the FLT_update flag 352 to indicate to the source circuit 208 that the request registers 390 through 393 have been updated. The source circuit 208 polls 506 the FLT_update flag 352 and upon reading a value of 1, the source circuit 208 reads 508 the request codes in the request registers 390 through 393 and resets the FLE_update flag 510 by writing a value of 0.

[0057] After reading 508 the request codes, the source circuit 208 performs the action specified by the request codes. For instance, if one of the request codes requests an update to a pre-emphasis parameter for the corresponding multimedia lane (e.g., request code 14 in Table 3), then the source circuit 208 sends a control signal to the equalization circuit 204 to update 512 the pre-emphasis parameter. Meanwhile, if the request codes request a change to a different link rate (e.g., the request registers for every active lane store request code 15 in Table 3), then the source circuit 208 switches 512 to state 4.

[0058] If one of the request codes requests a link training pattern (e.g., request codes 1 to 9 in Table 3), then the source circuit 208 provides the corresponding training pattern identifier to the training pattern circuit to the training pattern circuit 206. In the examples shown in Tables 2 and 3, a request code for a training pattern is identical to the identifier for the training pattern. In an embodiment where the request codes and training pattern identifiers are implemented in this manner, the source circuit 208 simply provides the request code to the training pattern circuit 206. The training pattern circuit 206 generates the training pattern and provides the training pattern to the equalization circuit 204 for transmission 516 to the sink device over the corresponding multimedia lane 210 through 213. The source circuit 208 also writes the identifier for training pattern to the setting flag 370 through 373 for the corresponding multimedia lane.

[0059] Upon receiving one or more training patterns, the control circuit 254 evaluates 518 the quality of the received link training patterns and selects one or more updated request codes. For instance, if the quality of the received link patterns is inadequate, the control circuit 254 may select updated request codes that specify an update to a pre-emphasis parameter, a switch to a different link rate, or for the link training process to end. The control circuit 254 may also select updated request codes to request the transmission of different training patterns. For example, after successfully performing clock recovery on the clock training signals, the control circuit 254 may select link patterns comprising predefined sequences of characters in order to perform equalization training, symbol locking, and inter-lane deskewing (e.g., training patterns 5 to 8 in Table 2). As another example, the control pattern may select a link pattern comprising a predefined sequence of characters for one of the multimedia lanes 210 through 213 and select request codes that cause source interface device 200 to cease transmission on the remaining multimedia lanes 210 through 213 (e.g., request codes 1 or 2 in Table 3). This allows the sink to evaluate the influence of crosstalk on the multimedia lane that carries the predefined sequence of characters.

[0060] If the request codes request that the link training process end, then the source circuit 208 transitions 520 to state P. In an embodiment that implements the request codes in Table 3, a request to end link training is represented by a request code of 0 (binary 0000) in the request register 390 through 393 for each active multimedia lane.

[0061] In some embodiments, the source circuit 208 also implements two timers that can cause the link training process shown in FIG. 5 to time out and cause the source circuit 208 to transition to state L 410. The source circuit 208 starts a first timer when the link training process begins. In one embodiment, the first timer starts at a value of 0 ms (milliseconds) and stops at a value of 200 ms. If the first timer stops before the link training process shown in FIG. 5 successfully concludes and transitions 520 to state P 412, then the link training process is deemed to have timed out and the source circuit 208 transitions to state L 410. The source circuit 208 starts a second timer at the beginning of each link training loop. In one embodiment, the second timer starts at a value of 0 ms and stops at a value of 10 ms. If the second time stops before the source circuit 208 reads another value of 1 in the FLT_update register 352 (i.e., if it takes longer than 10 ms for the control circuit 254 to end the link training loop by writing new values to the request registers 390 through 393), then the training loop is deemed to have timed out and the source circuit 208 transitions to state L 410.

[0062] Upon reading this disclosure, those of skill in the art will appreciate still additional alternative embodiments for a link training process for a multimedia interface. Thus, while particular embodiments and applications of the present disclosure have been illustrated and described, it is to be understood that the embodiments are not limited to the precise construction and components disclosed herein and that various modifications, changes and variations which will be apparent to those skilled in the art may be made in the arrangement, operation and details of the method and apparatus of the present disclosure disclosed herein without departing from the spirit and scope of the disclosure as defined in the appended claims.

What is claimed is:

1. A sink device, comprising:

a memory device comprising a plurality of registers, the registers configured to store link data about a multimedia link for performing multimedia data transmission from a source device to the sink device, the registers comprising:

a plurality of request registers, each request register associated with a multimedia lane of the multimedia link and configured to store a request code for the associated multimedia lane, each request register capable of being read by the source device over a bidirectional channel of the multimedia link; and

a link training control circuit communicatively coupled to the memory device and configured to:

provide one or more request codes to the source device in one or more of the request registers,

receive one or more training patterns, each of the training patterns received over a multimedia lane of the multimedia link and identified by the request code stored in the request register associated with the multimedia lane, and

select, based on the one or more received training patterns, one or more updated request codes for one or more of the multimedia lanes.

2. The sink device of claim 1, wherein the one or more received training patterns comprise a first training pattern and a second training pattern, the second training pattern different from the first training pattern.

3. The sink device of claim 1, wherein the plurality of request registers comprises:

a first request register associated with a first multimedia lane of the multimedia link and configured to store a first request code for the first multimedia lane;

a second request register associated with a second multimedia lane of the multimedia link and configured to store a second request code for the second multimedia lane;

a third request register associated with a second multimedia lane of the multimedia link and configured to store a third request code for the third multimedia lane; and

a fourth request register associated with a fourth multimedia lane of the multimedia link and configured to store a fourth request code for the fourth multimedia lane.

4. The sink device of claim 1, wherein the registers further comprise a request update register storing a binary value having a first value when one or more request codes have been stored in one or more of the request registers, wherein the link training circuit is further configured to write the first value to the request update register after storing the one or more request codes, and wherein the source device is configured to:

automatically read the request update register over the bidirectional channel of the multimedia link; and

responsive to reading the first value in the request update register, read the one or more request registers over the bidirectional channel of the multimedia link and write second value to the request update register.

5. The sink device of claim 1, wherein one of the updated request codes is a request to change a pre-emphasis parameter for one of the multimedia lanes of the multimedia link.

6. A method for performing link training on a multimedia interface, comprising:

providing one or more request codes to a source device in one or more request registers, the request registers part of a memory device in a sink device, the sink device capable of receiving multimedia data from a source device over a multimedia link, each request register associated with a multimedia lane of the multimedia link and capable of being read by the source device over a bidirectional channel of the multimedia link;

receiving one or more training patterns, each of the training patterns received over a multimedia lane of the multimedia link and identified by the request code stored in the request register associated with the multimedia lane; and

selecting, based on the one or more received training patterns, one or more updated request codes for one or more of the multimedia lanes.

7. The method of claim 6, wherein the one or more received training patterns comprise a first training pattern and a second training pattern, the second training pattern different from the first training pattern.

8. The method of claim 6, wherein storing one or more request codes in one or more request registers comprises:

storing a first request code in a first request register, the first request register associated with a first multimedia lane of the multimedia link;

storing a second request code in a first request register, the second request register associated with a second multimedia lane of the multimedia link;

storing a third request code in a first request register, the third request register associated with a third multimedia lane of the multimedia link; and

storing a fourth request code in a first request register, the fourth request register associated with a fourth multimedia lane of the multimedia link.

9. The method of claim 6, wherein the memory device further comprises a request update register storing a binary value having a first value when one or more request codes have been written in one or more of the request registers, and further comprising:

writing the first value to the request update register after storing the one or more request codes,

wherein the source device is configured to:

automatically read the request update register over the bidirectional channel of the multimedia link, and

responsive to reading the first value in the request update register, read the one or more request registers over the bidirectional channel of the multimedia link and write a second value to the request update register.

10. The method of claim 6, wherein one of the updated request codes is a request to change a pre-emphasis parameter for one of the multimedia lanes of the multimedia link.

11. A source device, comprising:

a training pattern circuit configured to generate one or more training patterns for transmission to a sink device over one or more multimedia lanes of a multimedia link in response to receiving identifiers for the one or more training pattern; and

a link training circuit capable of reading a memory device at the sink device via a bidirectional channel of the multimedia link, the link training circuit configured to:

read one or more request registers of the memory device, each request register associated with a multimedia lane and storing a request

code for the multimedia lane, wherein each request code is an identifier for a training pattern, and

provide the identifiers for the training patterns as input to the training pattern circuit.

12. The source device of claim 11, wherein the one or more training patterns comprise a first training pattern and a second training pattern different from the first training pattern.

13. The source device of claim 11, wherein the one or more request codes comprises:

a first request code for a first multimedia lane of the multimedia link, the first request code stored in a first request register of the memory device;

a second request code for a second multimedia lane of the multimedia link, the second request code stored in a second request register of the memory device;

a third request code for a third multimedia lane of the multimedia link, the third request code stored in a third request register of the memory device; and

a fourth request code for a fourth multimedia lane of the multimedia link, the fourth request code stored in a fourth request register of the memory device.

14. The source device of claim 11, wherein the link training circuit is further configured to:

automatically read a request update register of the memory device over the bidirectional channel of the multimedia link, the request update register storing a binary value having a first value when one or more request codes have been written in one or more of the request registers; and

responsive to reading the first value in the request update register, read the one or more request registers over the bidirectional channel of the multimedia link and write a second value to the request update register.

15. A method for performing link training on a multimedia interface, comprising:

reading, by a source device, a request register over a multimedia link between the source device and a sink device, the request register being part of a memory written by the sink device, the request register associated with a multimedia lane of the multimedia link and storing a request code for the multimedia lane, the request code indicating an action to be taken by the

source device, from a predefined set of actions, the predefined set of actions comprising sending a selection of one or more predetermined training patterns identified by the request code; and

responsive to reading a request code indicating sending of one or more training patterns, generating one or more training patterns identified by the request code for transmission to the sink device over the multimedia lane of the multimedia link.

16. The method of claim 15, wherein the one or more training patterns comprise a first training pattern and a second training pattern different from the first training pattern.

17. The method of claim 15, wherein reading the one or more request registers comprises:

reading a first request register associated with a first multimedia lane of the multimedia link and storing a first request code for the first multimedia lane;

reading a second request register associated with a second multimedia lane of the multimedia link and storing a second request code for the second multimedia lane;

reading a third request register associated with a third multimedia lane of the multimedia link and storing a third request code for the third multimedia lane; and

reading a fourth request register associated with a fourth multimedia lane of the multimedia link and storing a fourth request code for the fourth multimedia lane.

18. The method of claim 15, further comprising:

automatically reading a request update register of the memory device over the bidirectional channel of the multimedia link, the request update register storing a binary value having a first value when one or more request codes have been written in one or more of the request registers; and

responsive to reading the first value in the request update register, reading the one or more request registers over the bidirectional channel of the multimedia link and writing a second value to the request update register.

19. A method for performing link training on a multimedia interface, comprising:

reading, by a source device, a request register over a multimedia link between the source device and a sink device, the request register being part of a

memory written by the sink device, the request register associated with a multimedia lane of the multimedia link and storing a request code for the multimedia lane, the request code indicating an action to be taken by the source device, from a predefined set of actions, the predefined set of actions comprising sending a selection of one or more predetermined training patterns identified by the request code; and

responsive to reading a request code indicating sending of one or more training patterns, generating one or more training patterns identified by the request code for transmission to the sink device over the multimedia lane of the multimedia link.

20. A method for performing link training on a multimedia interface, comprising:

providing, by a sink device, a request code to a source device by storing the request code in a request register that is writable by the source device and readable by the source device, the sink device capable of receiving multimedia data from the source device over a multimedia link, the request register associated with a multimedia lane of the multimedia link, wherein the request code indicates an action, selected from a predefined set of actions, that the sink device requests to be taken by the source device, the predefined set of actions comprising sending, over the multimedia lane, a training pattern identified by the request code;

receiving a training pattern, from the source device, over the multimedia lane, the training pattern being identified by a request code stored in the request register; and

selecting, based on the one or more received training patterns, one or more updated request codes for storing in the request register.

21. A multimedia system comprising a source device, a sink device, and an interface comprising a multimedia lane for carrying multimedia data, wherein the sink device is configured to control a link training phase of the multimedia lane by requesting one or more training patterns, selected from among a plurality of pre-determined training patterns, to be sent by the source device to the sink device on the multimedia lane by providing request codes for reading by the source device, the request codes indicating a desired training pattern, and indicating to the source device, via a provided request code, readiness to receive multimedia data on the multimedia lane.

22. The multimedia system of claim 21, wherein the interface comprises a plurality of multimedia lanes, and the sink device is configured to separately control a respective training phase on each of the multimedia lanes, by providing respective request codes for each multimedia lane that indicates a desired training pattern to be sent to the sink device on that multimedia lane.

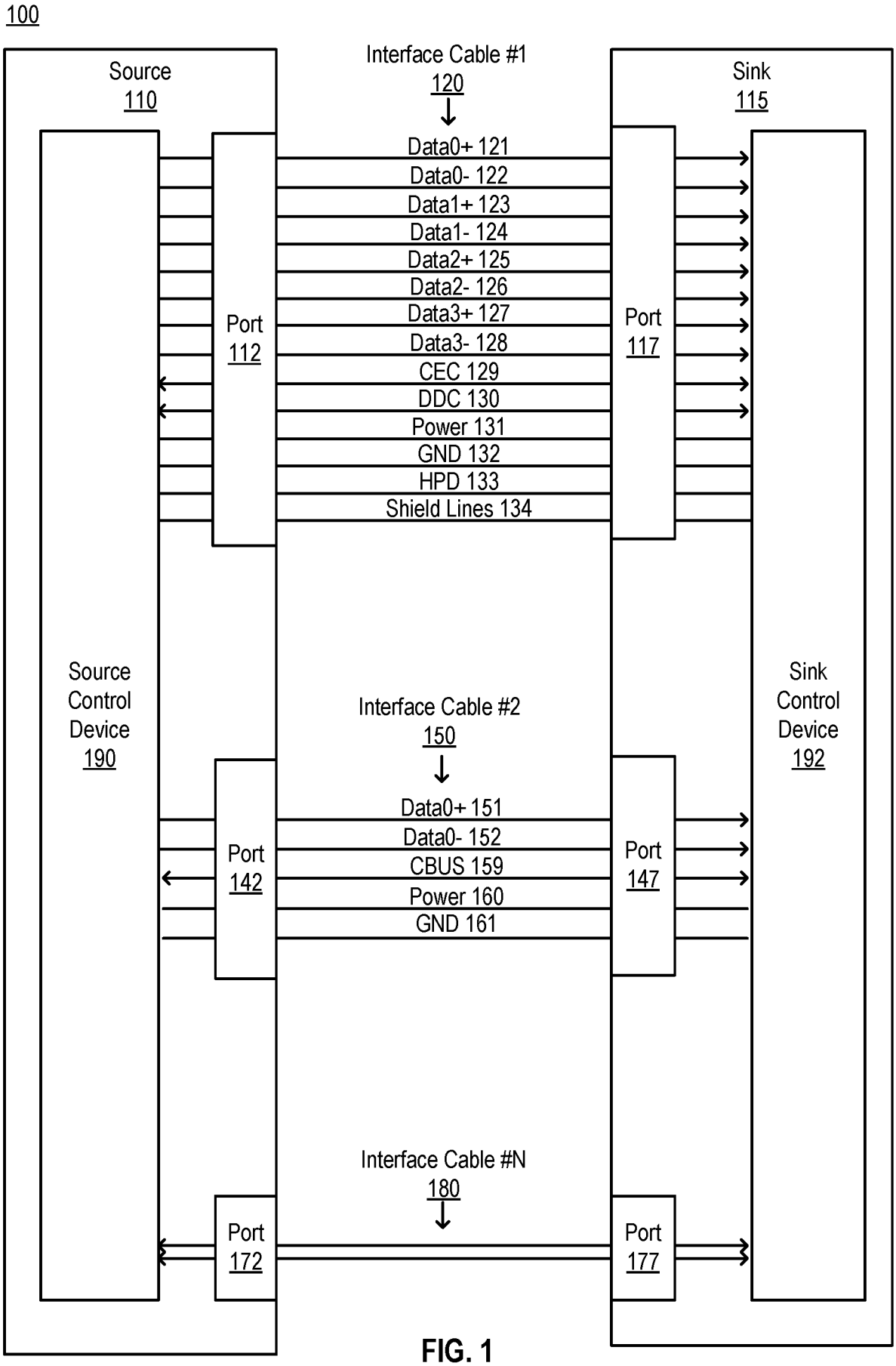
100
Source
110
Interface Cable #1
120
Sink
115
Data0+ 121
Data0- 122
Data1+ 123
Data1- 124
Data2+ 125
Data2- 126
Data3+ 127
Data3- 128
CEC 129
DDC 130
Power 131
GND 132
HPD 133
Shield Lines 134
Port
112
Port
117
Source
Control
Device
190
Sink
Control
Device
192
Interface Cable #2
150
Data0+ 151
Data0- 152
CBUS 159
Power 160
GND 161
Port
142
Port
147
Interface Cable #N
180
Port
172
Port
177

FIG. 1

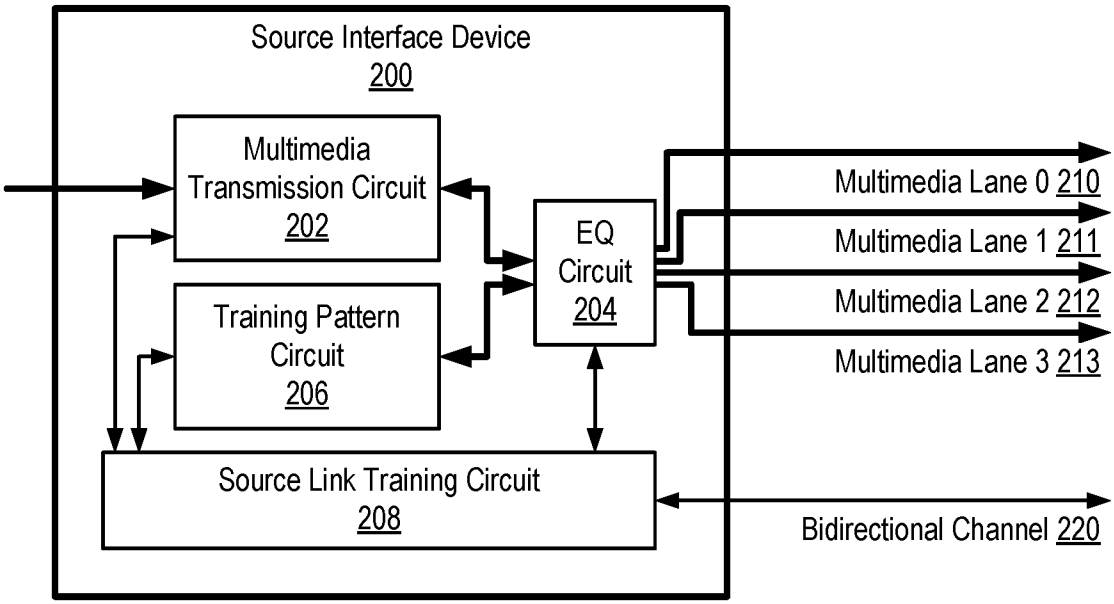
Source Interface Device
200
Multimedia Transmission Circuit
202
Training Pattern Circuit
206
EQ Circuit
204
Source Link Training Circuit
208
Multimedia Lane 0 210
Multimedia Lane 1 211
Multimedia Lane 2 212
Multimedia Lane 3 213
Bidirectional Channel 220

FIG. 2A

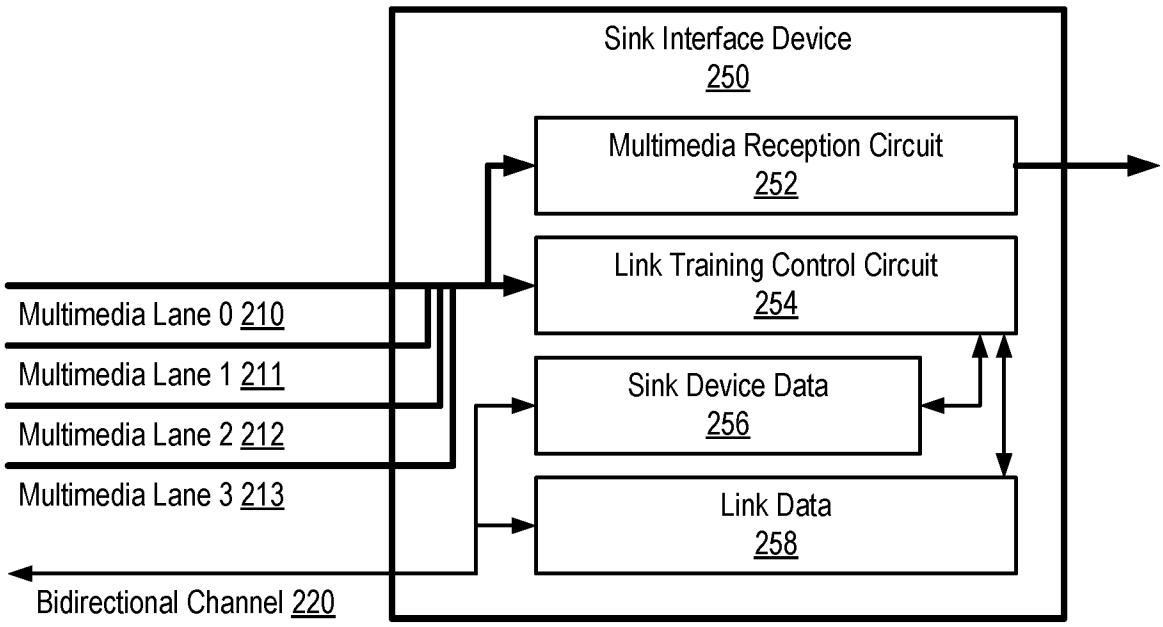
Sink Interface Device
250
Multimedia Reception Circuit
252
Link Training Control Circuit
254
Sink Device Data
256
Link Data
258
Multimedia Lane 0 210
Multimedia Lane 1 211
Multimedia Lane 2 212
Multimedia Lane 3 213
Bidirectional Channel 220

FIG. 2B

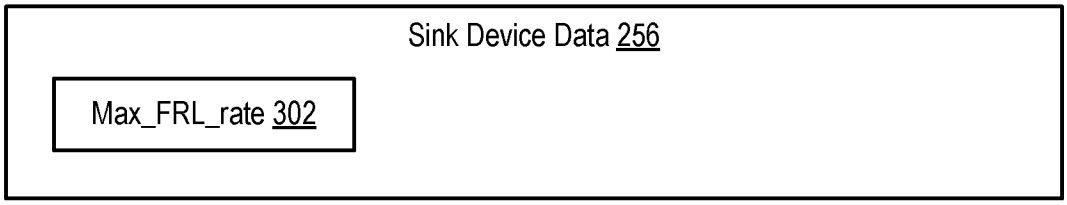
Sink Device Data 256
Max_FRL_rate 302

FIG. 3A

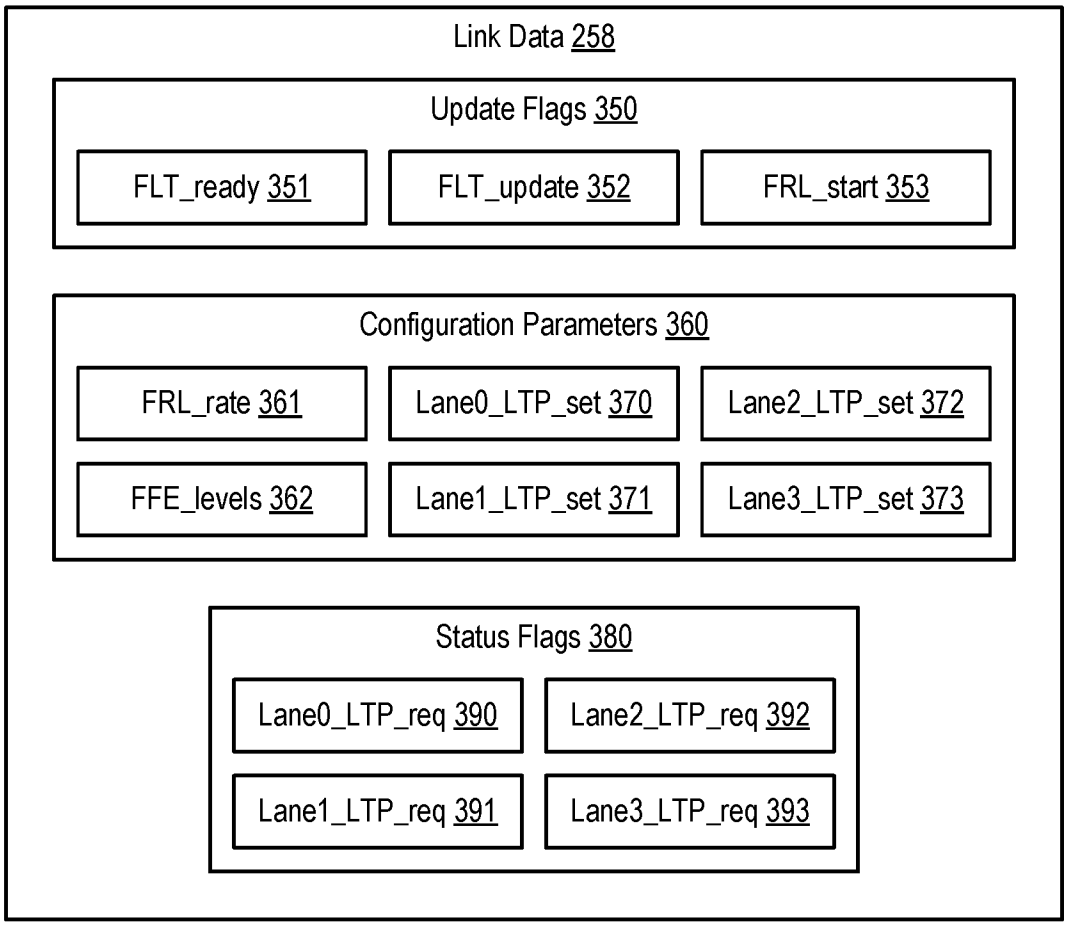
Link Data 258
Update Flags 350
FLT_ready 351
FLT_update 352
FRL_start 353
Configuration Parameters 360
FRL_rate 361
Lane0_LTP_set 370
Lane2_LTP_set 372
FFE_levels 362
Lane1_LTP_set 371
Lane3_LTP_set 373
Status Flags 380
Lane0_LTP_req 390
Lane2_LTP_req 392
Lane1_LTP_req 391
Lane3_LTP_req 393

FIG. 3B

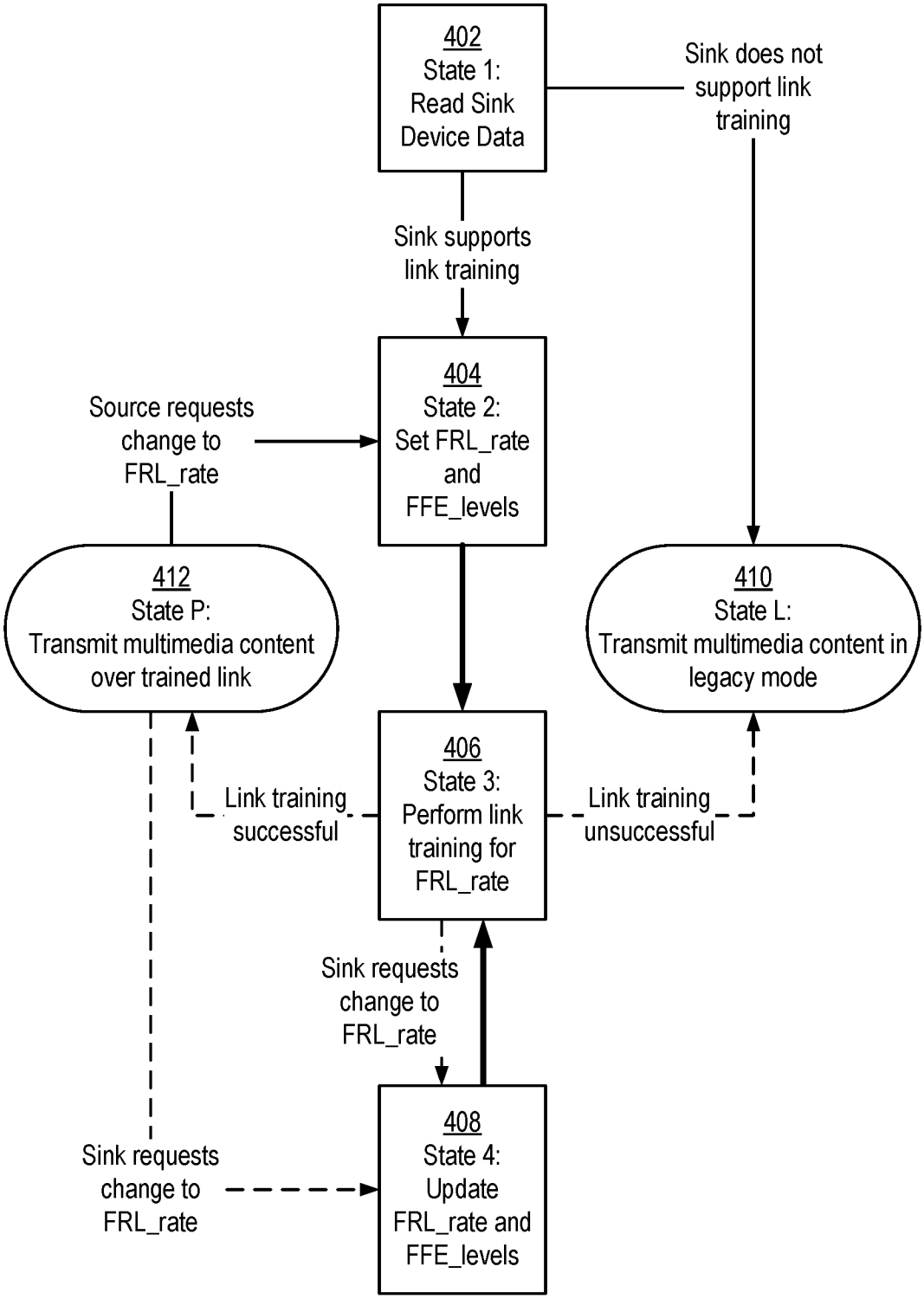
402
State 1:
Read Sink
Device Data
Sink does not
support link
training
Sink supports
link training
404
State 2:
Set FRL_rate
and
FFE_levels
Source requests
change to
FRL_rate
412
State P:
Transmit multimedia content
over trained link
410
State L:
Transmit multimedia content in
legacy mode
406
State 3:
Perform link
training for
FRL_rate
Link training
successful
Link training
unsuccessful
Sink requests
change to
FRL_rate
408
State 4:
Update
FRL_rate and
FFE_levels
Sink requests
change to
FRL_rate

FIG. 4

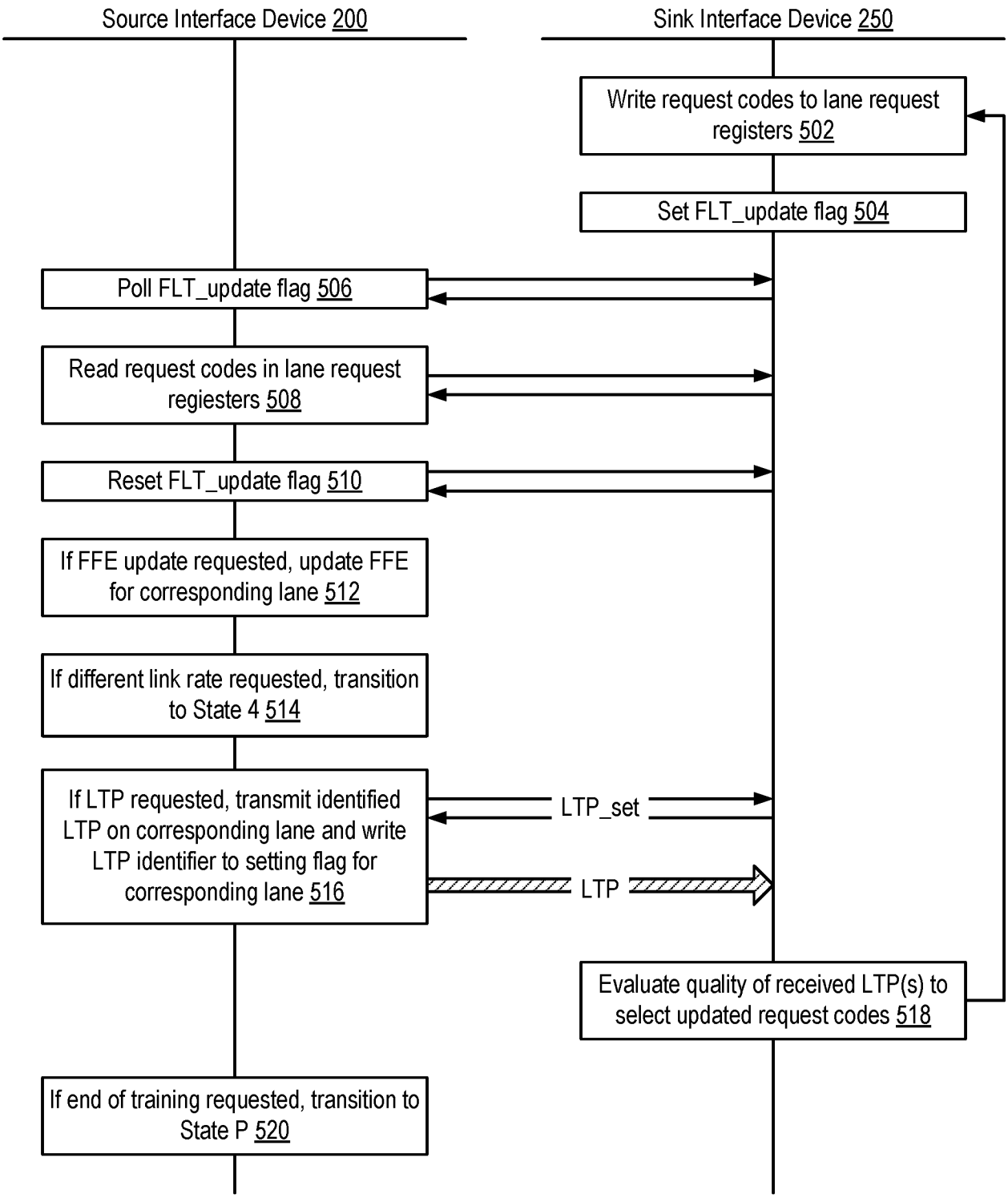
Source Interface Device 200
Sink Interface Device 250
Write request codes to lane request registers 502
Set FLT_update flag 504
Poll FLT_update flag 506
Read request codes in lane request regiesters 508
Reset FLT_update flag 510
If FFE update requested, update FFE for corresponding lane 512
If different link rate requested, transition to State 4 514
If LTP requested, transmit identified LTP on corresponding lane and write LTP identifier to setting flag for corresponding lane 516
LTP_set
LTP
Evaluate quality of received LTP(s) to select updated request codes 518
If end of training requested, transition to State P 520

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/020454

A. CLASSIFICATION OF SUBJECT MATTER

H04N 5/268(2006.01)i, H04N 5/765(2006.01)i, H04N 21/4363(2011.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N 5/268; G01R 31/28; H04N 7/16; H04L 12/26; H04L 29/06; H04N 17/00; H04N 17/04; H04N 21/63; H04N 5/765; H04N 21/4363

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: sink device, source device, multimedia lane, request register, request code, link traning pattern, and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 2140689 B1 (ATI TECHNOLOGIES ULC) 23 July 2014 See paragraphs [0014], [0016], [0027]-[0028], [0043]-[0045]; claims 10, 15; and figures 1-3, 5.	1-22
A	US 2014-0254640 A1 (KENT C. LUSTED et al.) 11 September 2014 See paragraphs [0053], [0083]; claim 11; and figure 15.	1-22
A	US 2010-0037283 A1 (NING ZHU) 11 February 2010 See paragraphs [0029]-[0031], [0040], [0047]-[0048]; and figures 1-2, 7, 12.	1-22
A	US 2010-0031098 A1 (OSAMU KOBAYASHI) 04 February 2010 See paragraphs [0069], [0109]; and figures 11, 28.	1-22
A	US 2013-0191872 A1 (DONGYUN LEE et al.) 25 July 2013 See paragraphs [0066]-[0067].	1-22

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
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