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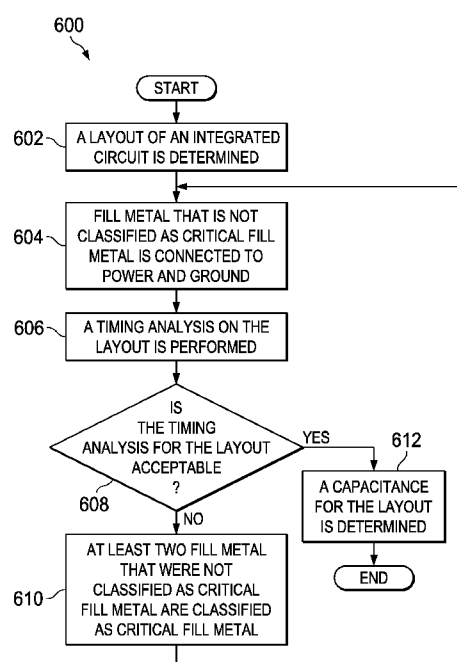


FIG. 6

(57) Abstract: Substrates, assemblies, and techniques for an integrated circuit that includes at least one metal layer. The at least one metal layer includes an electronic element and connected metal, where the connected metal was fill metal and is connected to a power grid for the integrated circuit. The connected metal can create an intrinsic capacitance and can reduce or eliminate an inherent capacitor for the integrated circuit.

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POWER DELIVERY USING CONNECTED FILL METAL**Technical Field**

[0001] The present disclosure relates generally to the field of integrated circuits, and more particularly, to power delivery using connected fill metal.

Background

[0002] A system on a chip or system on chip (SoC or SOC) is an integrated circuit (IC) that integrates components of a computer or other electronic system into a single chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions all on a single chip substrate. Metal fill is a mandatory step at advanced nodes to ensure manufacturability and high yield. The metal fill process involves filling the empty or white spaces near the IC design with metal to ensure regular planarization of the wafer that includes the IC. Also, mandated fill requirements stipulate that the fill density be within specified maximum and minimum parameters. In advanced node IC designs, metal fills can be added to maintain layer planarity during chemical mechanical polishing.

Brief Description of the Drawings

[0003] Embodiments will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements. Embodiments are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0004] FIGURE 1 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0005] FIGURE 2 is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0006] FIGURE 3A is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0007] FIGURE 3B is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0008] FIGURE 3C is a simplified block diagram illustrating an embodiment of a portion of an electronic device, in accordance with one embodiment of the present disclosure;

[0009] FIGURE 4 is a simplified flowchart illustrating potential operations that may be associated with the communication system in accordance with an embodiment;

[0010] FIGURE 5 is a simplified flowchart illustrating potential operations that may be associated with the communication system in accordance with an embodiment;

[0011] FIGURE 6 is a simplified flowchart illustrating potential operations that may be associated with the communication system in accordance with an embodiment;

[0012] FIGURE 7 is an interposer implementing one or more of the embodiments disclosed herein; and

[0013] FIGURE 8 is a computing device built in accordance with an embodiment disclosed herein.

[0014] The figures of the drawings are not necessarily drawn to scale, as their dimensions can be varied considerably without departing from the scope of the present disclosure.

Detailed Description

[0015] The following detailed description sets forth example embodiments of apparatuses, methods, and systems relating to an access transmission gate. Features such as structure(s), function(s), and/or characteristic(s), for example, are described with reference to one embodiment as a matter of convenience; various embodiments may be implemented with any suitable one or more of the described features.

[0016] In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the embodiments disclosed herein may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the embodiments disclosed herein may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

[0017] Disclosed herein are substrates, assemblies, and techniques for enabling power delivery using connected fill metal. Current input/output devices and cores working at a high data rate call for stringent noise specifications, drop specifications, and/or jitter specifications

which require higher on die intentional capacitance. To increase the on-die intrinsic capacitance (or inherent capacitance) and reduce intentional capacitance, unused fill metals can be converted to power and ground and effectively use the converted fill metals as decoupling or intrinsic capacitors. This can reduce the intentional capacitance on the die and reduce the overall die area. In addition, the converted unused fill metals can also be implemented in reducing high frequency noise and thereby reducing deterministic jitter.

[0018] The terms “over,” “under,” “below,” “between,” and “on” as used herein refer to a relative position of one material layer or component with respect to other layers or components. For example, one layer disposed over or under another layer may be directly in contact with the other layer or may have one or more intervening layers. Moreover, one layer disposed between two layers may be directly in contact with the two layers or may have one or more intervening layers. In contrast, a first layer “on” a second layer is in direct contact with that second layer. Similarly, unless explicitly stated otherwise, one feature disposed between two features may be in direct contact with the adjacent features or may have one or more intervening layers.

[0019] Implementations of the embodiments disclosed herein may be formed or carried out on a substrate, such as a non-semiconductor substrate or a semiconductor substrate. In one implementation, the non-semiconductor substrate may be silicon dioxide, inter-layer dielectric composed of silicon dioxide, silicon nitride, titanium oxide and other transition metal oxides. Although a few examples of materials from which the non-semiconducting substrate may be formed are described here, any material that may serve as a foundation upon which a non-semiconductor device may be built falls within the spirit and scope of the embodiments disclosed herein.

[0020] In another implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. In other examples, the substrate may be a flexible substrate including 2D materials such as graphene and molybdenum disulphide, organic materials such as pentacene, transparent oxides such as indium gallium zinc oxide poly/amorphous (low temperature of

dep) III-V semiconductors and germanium/silicon, and other non-silicon flexible substrates. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the embodiments disclosed herein.

[0021] In the following detailed description, reference is made to the accompanying drawings that form a part hereof wherein like numerals designate like parts throughout, and in which is shown, by way of illustration, embodiments that may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense.

[0022] Various operations may be described as multiple discrete actions or operations in turn, in a manner that is most helpful in understanding the claimed subject matter. However, the order of description should not be construed as to imply that these operations are necessarily order dependent. In particular, these operations may not be performed in the order of presentation. Operations described may be performed in a different order from the described embodiment. Various additional operations may be performed, and/or described operations may be omitted in additional embodiments. For the purposes of the present disclosure, the phrase "A and/or B" means (A), (B), or (A and B). For the purposes of the present disclosure, the phrase "A, B, and/or C" means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B, and C).

[0023] The description uses the phrases "in an embodiment" or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous. An integrated circuit (IC) is a set of electronic circuits or elements on a substrate. As used herein, a "package" and an "IC package" are synonymous. As used herein, the terms "chip" and "die" may be used interchangeably. Typically, ICs are produced in large batches on a single wafer or other semiconductor. The wafer is cut into many pieces, each containing one copy of the IC. Each of these pieces of the IC is called a "die" or "die area".

[0024] FIGURE 1 is a simplified block diagram of an electronic device 100 that includes one or more ICs that include power delivery using connected fill metal in accordance with an embodiment of the present disclosure. Electronic device 100 can be any electronic device that

includes an IC (e.g., computer, smartphone, laptop, desktop, Internet-of-Things (IoT) device, vehicle electronics, handheld electronic device, personal digital assistant, wearable, household electronics, etc.). Electronic device 100 can include one or more electronic elements 102a-102d. Each electronic element 102a-102d can include one or more ICs 104 that include power delivery using connected fill metal and/or one or more IC arrays 106 that include power delivery using connected fill metal. Each IC array 106 can be a systematic arrangement of a plurality of ICs 104, (e.g., in rows and columns).

[0025] IC 104 can be configured to include modified or connected fill metal, logic, one or more transistors, and/or one or more memory elements. Each transistor can be an electronic switch that can be either in an "on" or "off" state and the term "transistor" includes a metal-oxide-semiconductor (MOS), complementary MOS (CMOS), n-channel MOS (NMOS) p-channel MOS (PMOS), MOS field-effect transistors (MOSFET), bipolar junction transistor (BJT), filed effect transistor (FET), finFET, junction gate FET (JFET), insulated gate FET (IGFET), n-channel field effect transistor (NFET) insulated-gate bipolar transistor, or other similar transistor. In an example, the transistor can be a backend transistor. A backend transistor is a thin filmed transistor above a metal one layer. Backend transistors can allow device functionally to be scaled by stacking memory and logic in the backend.

[0026] The transistor can be coupled to a capacitive element. The capacitive element may be a memory element such as embedded dynamic random access memory (eDRAM). In another example, the transistor can be coupled to a resistive element such as resistive random-access memory (RRAM). In yet another example, the transistor can be coupled to some other type of memory or element. eDRAM can be integrated on the same die or multi-chip module (MCM) of an application-specific IC (ASIC) or microprocessor.

[0027] One issue with current ICs is that the high-speed input/output data rate is increasing with every process generation. In addition, the die area is reduced due to process improvement on the IC and, as a result, conforming to the on-die power delivery noise specification can become highly challenging. In almost every process generation with sub-nano meter technology, the die area is targeted to be reduced and the device sizes and interconnect geometries also shrink due to process improvement on the IC. Performance requirements for core and input/output interfaces are also increasing with each generation. As a result, providing efficient power delivery solutions to meet noise specification is highly challenging given the provided power per area verses available on die capacitance for noise filtering. Also,

the deterministic jitter that primarily impacts high speed input/outputs due to the power delivery noise is gaining a significant part of the overall jitter budget for the input/output design of ICs.

[0028] Traditionally, on die power delivery solutions need intentional decapacitance to be placed on the die to reduce high frequency power delivery network noise. The term intentional decapacitance includes the use of a capacitor, herein referred to as an intentional capacitor, to reduce high frequency power delivery network noise. The term “intentional capacitance” includes the on die dedicated capacitance or MOSFET capacitance. Typically, the intentional capacitor needs a relatively large die area which increases the overall size of the die or IC area. What is needed is a way to increase the intrinsic capacitance and reduce the intentional capacitor or intentional capacitance requirement.

[0029] In an example, unused fill metal or unutilized metals on the die can be converted by connecting the fill metal to the power grid of the IC. The fill metal can be connected to power and ground, thereby increasing the overall intrinsic capacitance on the power delivery network without increasing die area of the IC. The term “intrinsic capacitance” includes the inherent capacitance. Utilization of the fill metals can help to increase the intrinsic capacitance of the IC and reduce or remove the intentional capacitors.

[0030] Fill metal, sometimes referred to as float metal, is typically added to design data during die or chip finishing just before tape-out. The fill metal may be added using physical verification tools. Moreover, the fill metal added must follow conservative rules not to degrade timing or performance. Fill metals are required to be placed close to signal nets to meet minimum density requirements and should not affect circuit performance, chip timing, signal integrity and even functionality to a larger degree.

[0031] In an example, the fill metal can be coupled to a power grid of an IC such that the fill metal, now connected metal, is converted to respective power and ground signals with no impact (or a relatively small impact) to the layout of the IC. This can create additional intrinsic capacitance from the connected metal as compared to current ICs with unconnected fill metal. This additional intrinsic capacitance can help in reducing or removing the required intentional capacitance for the IC.

[0032] In a specific illustrative example, a layout verses schematic (LVS), base density, and design rule check (DRC) clean data base is taken to a fill flow. The layout is filled with a preferred power and ground pattern by reading the fill constraints. A user defined fill

constraint file can include the timing critical nets and pad routes where power nets are restricted to be filled adjacent to the timing critical nets and pad routes, which effects circuit performance. Then, the fill metals are filled adjacent to the critical nets. Via fill is run to connect or couple the power and ground metals with a DRC clean option. Opens flow can be run to check for any open nets. Unconnected nets can be renamed back to fill metal. The nets that fail for timing are considered as fill constraint for consequent loops. Extraction and die modelling can be done to extract the intrinsic capacitance for power delivery analysis after the timing report is clean. The connected metal can improve overall uniform jitter numbers as well as drop overall jitter static voltage (IR) with respective metal fill conversions. The IR drop can improve Vmin and in some examples (e.g., physical input/output ports), can enable higher performance even at worst case scenarios.

[0033] By converting the fill metal to connected metal, relatively significant area reduction can be achieved by reducing the size of or even eliminating the intentional capacitor. This can enable cost reduced smaller form factor products such as mobile devices, tablets, IoT devices, etc. Area savings could be even higher in a core/CPU region due to lesser utilization of higher level metals. In some instances, the connected metal can reduce the bill of materials (BOM) cost by removing the intentional capacitor from the IC. The connected metal can enable improved power deliver in terms of supply noise reduction and achieve lower jitter. This can result in improved IC performance (e.g., a die which meets 5.4Gbps specification, could be made to work at 6Gbps without any extra intentional capacitors). In an illustrative example, if about eighty percent (80%) to about ninety percent (90%) of fill metals can be converted to power and ground, the on-die capacitance could be increased without any impact (or a relatively small impact) to the layout of the IC. Timing analysis using the connected metal can be performed to reduce the effect of the connected metal on circuit performance, chip timing, signal integrity, etc.

[0034] Turning to FIGURE 2, FIGURE 2 illustrates one embodiment of IC 104. IC 104 can include a base substrate 108, a first metal layer 110, a second metal layer 112, a third metal layer 114, a fourth metal layer 116, a fifth metal layer 118, and a sixth metal layer 120. Each of first metal layer 110, second metal layer 112, third metal layer 114, fourth metal layer 116, fifth metal layer 118, and sixth metal layer 120 can include a plurality of connected metal (i.e., fill metal coupled to power and ground) and one or more electronic elements. In addition, each of first metal layer 110, second metal layer 112, third metal layer 114, fourth metal layer

116, fifth metal layer 118, and sixth metal layer 120 may include unconnected fill metal or may not include any unconnected fill metal (i.e., all the fill metal is coupled to power and ground).

[0035] For example, sixth metal layer 120 can include power grid metal 122a and 122b, connected metal 124a-124d, and a first electronic element 126. Fourth metal layer 116 can include fill metal 130a-130d. Second metal layer 112 can include power grid metal 122c and 122d, connected metal 124e and 124f, fill metal 130e and 130f, and a second electronic element 128. Power grid metal 122a-122d includes the power and ground metal created during the design of the IC. Connected metal 124a-124f includes converted fill metal or metal that is connected to the power grid of the IC. Fill metal 130a-130d is fill metal that is not connected to the power grid of the IC.

[0036] It should be noted that more or less metal layers than illustrated in FIGURE 2 may be present. Also, one or more first electronic elements 126 and one or more second electronic elements 128 may be in or on one or more different metal layers. Further, IC 104 can include other electronic elements than first electronic element 126 and second electronic element 128.

[0037] Base substrate 108 can be a non-semiconducting substrate and may be composed of silicon dioxide, inter-layer dielectric composed of silicon dioxide, silicon nitride, titanium oxide, other transition metal oxides, aluminum oxide, sapphire substrates, silicon carbide, or other material that may serve as a non-conductive layer. Typically, fill metal is the same metal used in the metal layer that includes the fill metal. For example, if the metal layer (e.g., first metal layer 110) included a source or a drain, then the fill metal may be composed of different metals with various work functions from ranges of about 5.6 eV to about 3.8 eV. More specifically, the fill metal may be composed of layers or bi-layers of tungsten, cobalt, titanium nitride, tantalum nitride, titanium, aluminum, indium tin oxide, tantalum, ruthenium, hafnium, and other similar materials. If the metal layer (e.g., third metal layer 114) included a channel, then the fill metal may be composed of indium gallium zinc oxide, zinc oxide, zinc oxynitrides, gallium oxide, tin oxide, copper oxide, indium zinc oxide, indium oxide some other semiconducting metal oxide, or other semiconducting material.

[0038] Turning to FIGURE 3A, FIGURE 3A illustrates one embodiment of a metal layer in IC 104. In a specific implementation, the metal layer can include power grid metal 122a and 122b, first electronic element 126, and fill metal 130a-130d. Power grid metal 122a may be a power “in” supply or positive supply voltage (i.e., V+) and power grid metal 122b may be a

power “out” supply or negative supply voltage (i.e., V-). Power grid metal 122a and 122b may be connected to a power grid 134 for the IC. Fill metal 130a-130d is typically added to the metal layer to ensure that the design and specifications are clean or within predetermined specifications. The fill metals are typically the same material as the layer that includes the fill metal. The fill metals help clean the density of the metal to get a higher yield on the silicon and to make sure the design and layout verifications are clean and within predetermined specifications.

[0039] As illustrated in FIGURE 3A, power grid metal 122a is coupled to first electronic element 126 and to power grid metal 122b. Power grid metal 122b is also coupled to first electronic element 126. An intrinsic capacitance 132b is created between power grid metal 122a and first electronic element 126 and an intrinsic capacitance 132c is created between power grid metal 122b and first electronic element 126. Intrinsic capacitance 132a can be an intentional capacitance, or intentional capacitor, to reduce the change in power supply voltage and to try and keep the voltage more constant. Intrinsic capacitance 132a can provide a near reservoir of energy to smooth out the voltage during very short term changes in current draw. Intrinsic capacitance 132b and 132c may be an intrinsic or inherent capacitance that is created between the connected metal. The intrinsic capacitance 132a (and intrinsic capacitance 132b and 132c) can be determined using the parallel plate capacitor formula $C=EA/D$ where “C” is the capacitance, “E” is the permittivity of space, “A” is the area, and “D” is the distance.

[0040] Turning to FIGURE 3B, FIGURE 3B illustrates one embodiment of a metal layer in IC 104. For example, the metal layer may be sixth metal layer 120. In a specific implementation, fill metal 130a-130d illustrated in FIGURE 3A has been connected or coupled to power grid 134 for the IC to create connected metal. For example, power grid metal 122a and 122b may be connected to power grid 134. In addition, power grid metal 122a may be coupled to connected metal 124a, connected metal 124a may be coupled to connected metal 124b, connected metal 124b may be coupled to first electronic element 126, connected metal 124c may be coupled to first electronic element 126 and to connected metal 124d, and connected metal 124d may be coupled to power grid metal 122b. Power grid metal 122a and connected metal 124b and 124d may be a positive supply voltage (i.e., V+). Power grid metal 122b and connected metal 124a and 124c may be a negative supply voltage (i.e., V-).

[0041] An intrinsic capacitance 132e may be created between power grid metal 122a and connected metal 124a, an intrinsic capacitance 132f may be created between connected

metal 124a and 124b, an intrinsic capacitance 132g may be created between connected metal 124b and first electronic element 126, an intrinsic capacitance 132h may be created between first electronic element 126 and connected metal 124c, an intrinsic capacitance 132i may be created between connected metal 124c and 124d, and an intrinsic capacitance 132j may be created between connected metal 124d and power grid metal 122b. By using connected metal 124a-124d, the distance in the parallel plate capacitor formula is reduced to 1/6 as compared to the metal layer illustrated in FIGURE 3A. As a result, using the the metal layer illustrated in FIGURE 3B, the parallel plate capacitor formula is $C=EA/(D/6)$ or $C=6(EA/D)$ and the capacitance can increase by 6 times using intrinsic capacitance 132e-132j as compared only once using intrinsic capacitance 132a in FIGURE 3A. This helps reduce the required decoupling capacitance and, as illustrated in FIGURE 3B, may even eliminate intrinsic capacitance 132a if intrinsic capacitance includes an intentional capacitor.

[0042] Turning to FIGURE 3C, FIGURE 3C illustrates one embodiment of a metal layer in IC 104. Connected metal 124e and 124f may have been fill metal but were converted to connected metal. In a specific implementation, not all the fill metal in the metal layer was converted to connected metal. For example, fill metal 130e and 130f may not have been converted to connected metal. Fill metal 130e and 130f may not have been converted to connected metal because fill metal 130e and 130f may be too small to be connected to power grid 134 or the location of fill metal 130e and 130f may be such that they cannot be connected to power grid 134. For example, if second electronic element 128 is a clock signal and if fill metal 130e and 130f were connected metal, the timing constraints of the IC, or more specifically, the clock signal, may be affected.

[0043] First electronic element 126 and second electronic element 128 may each be a transistor, capacitive element, resistive element, logic circuitry, logic (e.g., adders, registers, etc.), micro-processor circuits for processing data, a signal, and/or other circuitry or electronic element. If base substrate 108 is a semiconductor substrate, the semiconductor substrate (and any additional silicon based layers) may be formed using alternate materials, which may or may not be combined with silicon. This includes, but is not limited to, silicon, silicon germanium, germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. In other examples, the substrate of any layer may be a flexible substrate including 2D materials such as graphene and molybdenum disulfide, organic materials such as

pentacene, transparent oxides such as indium gallium zinc oxide poly/amorphous (low temperature of dep) III-V semiconductors and germanium/silicon, and other non-silicon flexible substrates.

[0044] In an example, a plurality of electrical components can include one or more ICs 104 and/or one or more arrays 106 of ICs 104. Each IC 104 can include a plurality of transistors, such as MOSFET or simply MOS transistors, and may be fabricated on base substrate 108. In various embodiments, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that various embodiments may also be carried out using nonplanar transistors.

[0045] Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[0046] The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type work function metal or N-type work function metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are work function metal layers and at least one metal layer is a fill metal layer. Further metal layers may be included for other purposes, such as a barrier layer.

[0047] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal

oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a work function that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a work function that is between about 3.9 eV and about 4.2 eV.

[0048] In some implementations, when viewed as a cross-section of the transistor along the source-channel-drain direction, the gate electrode may consist of a U-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further embodiments, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0049] In some embodiments, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process steps. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[0050] Source and drain regions can be formed within base substrate 108 adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form

recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations, the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[0051] One or more interlayer dielectrics (ILD) may be deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in IC structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide, carbon doped oxide, silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass, and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[0052] Turning to FIGURE 4, FIGURE 4 is an example flowchart illustrating possible operations of a flow 400 that may be associated with power delivery using connected fill metal, in accordance with an embodiment. At 402, a layout of an IC is determined. At 404, fill metal is added to the layout. At 406, the fill metal is connected to power and ground. For example, fill metal 130a-130d illustrated in FIGURE 3A may be connected to power grid 134 and converted to connected metal 124a-124d illustrated in FIGURE 3B.

[0053] Turning to FIGURE 5, FIGURE 5 is an example flowchart illustrating possible operations of a flow 500 that may be associated with power delivery using connected fill metal, in accordance with an embodiment. At 502, a layout of an IC is determined. At 504, fill metal to be added to the layout is determined. At 506, the system determines if any of the fill metal is critical fill metal. If none of the fill metal is critical fill metal, then the fill metal is connected to power and ground, as in 508. If any of the fill metal is critical fill metal, then the critical fill metal is classified as critical fill metal, as in 510. At 512, fill metal that is not classified as critical fill metal is connected to power and ground. For example, fill metal 130e and 130f illustrated in FIGURE 3C may be classified as critical fill metal and therefore is not converted to connected metal. The term “critical fill metal” includes fill metal that must remain fill metal and not be

converted to connected metal. For example, if the critical fill metal were to be coupled to power and ground, second electronic element 128 may be adversely affected. In another example, a location and/or size of the fill metal may not allow for the fill metal to be coupled to power and ground.

[0054] Turning to FIGURE 6, FIGURE 6 is an example flowchart illustrating possible operations of a flow 600 that may be associated with power delivery using connected fill metal, in accordance with an embodiment. At 602, a layout of an IC is determined. At 604, fill metal that is not classified as critical fill metal is connected to power and ground. At 606, a timing analysis on the layout is performed. At 608, the system determines if the timing analysis for the layout is acceptable. If the timing analysis for the layout is acceptable, then a capacitance for the layout is determined, as in 612. If the timing analysis for the layout is not acceptable, then at least two fill metal (e.g., a positive and a negative) that were not classified as critical fill metal are classified as critical fill metal, as in 610 and the system returns to 604 where fill metal that is not classified as critical fill metal is connected to power and ground. For example, fill metal 130a-130d illustrated in FIGURE 3A may be connected to power grid 134 and converted to connected metal 124a-124d illustrated in FIGURE 3B. A timing analysis on the layout may be performed and the analysis may not be acceptable. As a result of the unacceptable timing analysis, fill metal 130e and 130f illustrated in FIGURE 3C may be classified as critical fill metal and the timing analysis may be run again.

[0055] Turning to FIGURE 7, FIGURE 7 illustrates an interposer 700 that can include or interact with one or more embodiments disclosed herein. The interposer 700 is an intervening substrate used to bridge a first substrate 702 to a second substrate 704. The first substrate 702 may be, for instance, an IC die. The second substrate 704 may be, for instance, a memory module, a computer motherboard, or another IC die. Generally, the purpose of an interposer 700 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 700 may couple an IC die to a ball grid array (BGA) 706 that can subsequently be coupled to the second substrate 704. In some embodiments, the first and second substrates 702/704 are attached to opposing sides of the interposer 700. In other embodiments, the first and second substrates 702/704 are attached to the same side of the interposer 700. And in further embodiments, three or more substrates are interconnected by way of the interposer 700.

[0056] The interposer 700 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0057] The interposer may include metal interconnects 708 and vias 710, including but not limited to through-silicon vias (TSVs) 712. The interposer 700 may further include embedded devices 714, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 700. In accordance with various embodiments, apparatuses or processes disclosed herein may be used in the fabrication of interposer 700.

[0058] Turning to FIGURE 8, FIGURE 8 illustrates a computing device 800 in accordance with various embodiments. The computing device 800 may include a number of components. In one embodiment, these components are attached to one or more motherboards. In an alternate embodiment, some or all of these components are fabricated onto a single system-on-a-chip (SoC) die. The components in the computing device 800 include, but are not limited to, an IC die 802 and at least one communications logic unit 808. In some implementations, the communications logic unit 808 is fabricated within the IC die 802 while in other implementations the communications logic unit 808 is fabricated in a separate IC chip that may be bonded to a substrate or motherboard that is shared with or electronically coupled to the IC die 802. The IC die 802 may include a CPU 804 as well as on-die memory 806, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STT-MRAM).

[0059] Computing device 800 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 810 (e.g., DRAM), non-volatile memory 812 (e.g., ROM or flash memory), a graphics processing unit 814 (GPU), a digital signal processor 816, a crypto processor 842 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 820, an antenna 822, a display or a

touchscreen display 824, a touchscreen controller 826, a battery 828 or other power source, a power amplifier (not shown), a voltage regulator (not shown), a global positioning system (GPS) device 828, a compass 830, a motion coprocessor or sensors 832 (that may include an accelerometer, a gyroscope, and a compass), a speaker 834, a camera 836, user input devices 838 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 840 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0060] The communications logic unit 808 enables wireless communications for the transfer of data to and from the computing device 800. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communications logic unit 808 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 800 may include a plurality of communications logic units 808. For instance, a first communications logic unit 808 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communications logic unit 808 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0061] The processor 804 of the computing device 800 can communicate with one or more devices that are formed in accordance with various embodiments. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0062] The communications logic unit 808 may also include one or more devices, such as transistors or metal interconnects, that are in communication with various ones of the embodiments disclosed herein. In further embodiments, another component housed within the computing device 800 may contain one or more devices, such as transistors or metal interconnects, that are formed in accordance with implementations of the embodiments disclosed herein.

[0063] In various embodiments, the computing device 800 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 800 may be any other electronic device that processes data.

[0064] The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the scope of the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the embodiments disclosed herein are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

OTHER NOTES AND EXAMPLES.

[0065] Example 1 is an integrated circuit including at least one metal layer that includes an electronic element and connected metal, where the connected metal was fill metal and is connected to a power grid for the integrated circuit.

[0066] In Example 2, the subject matter of Example 1 can optionally include where the connected metal is the same material as the metal layer.

[0067] In Example 3, the subject matter of any one of Examples 1 and 2 can optionally include where the at least one metal layer does not include an intentional capacitor.

[0068] In Example 4, the subject matter of any one of Examples 1-3 can optionally include where the at least one metal layer further includes fill metal that is not connected to the power grid.

[0069] In Example 5, the subject matter of any one of Examples 1-4 can optionally include where the fill metal that is not connected to the power grid is classified as critical fill metal.

[0070] In Example 6, the subject matter of any one of Examples 1-5 can optionally include where the fill metal that is not connected to the power grid would affect a timing analysis if the fill metal was converted to connected metal.

[0071] In Example 7, the subject matter of any one of Examples 1-6 can optionally include where the connected metal creates an intrinsic capacitance.

[0072] In Example 8, the subject matter of any one of Examples 1-7 can optionally include where the at least one metal layer satisfies a timing analysis for a design of the integrated circuit.

[0073] In Example 9, a method can include designing an integrated circuit, determining fill metal for the integrated circuit, and connecting at least a portion of the determined fill metal to a power grid for the integrated circuit.

[0074] In Example 10, the subject matter of Example 9 can optionally include determining if any of the fill metal is critical fill metal and not connecting the fill metal determined to be critical fill metal to the power grid.

[0075] In Example 11, the subject matter of any one of Examples 9 and 10 can optionally include determining timing specifications for the integrated circuit and performing a timing analysis on the integrated circuit with the connected fill metal.

[0076] In Example 12, the subject matter of any one of Examples 9-11 can optionally include disconnecting at least two fill metal that were connected to the power grid if the timing analysis does not satisfy the timing specifications for the integrated circuit.

[0077] In Example 13, the subject matter of any one of Examples 9-12 can optionally include determining an inherent capacitance of the connected fill metal.

[0078] In Example 14, the subject matter of any one of Examples 9-13 can optionally include determining an intentional capacitance for the integrated circuit.

[0079] In Example 15, the subject matter of any one of Examples 9-14 can optionally include where the integrated circuit includes an electronic element.

[0080] Example 16 is a computing device including a processor mounted on a substrate, a communications logic unit within the processor, a memory within the processor, a graphics processing unit within the computing device, an antenna within the computing device, a display on the computing device, a battery within the computing device, a power amplifier within the processor, a voltage regulator within the processor, and an integrated circuit including at least one metal layer. The at least one metal layer includes an electronic element and connected metal, where the connected metal was fill metal and is connected to a power grid for the integrated circuit.

[0081] In Example 17 the subject matter of Example 16 can optionally include where the at least one metal layer does not include an intentional capacitor.

[0082] In Example 18 the subject matter of any one of Examples 16 and 17 can optionally include where the at least one metal layer further includes fill metal that is not connected to the power grid.

[0083] In Example 19, the subject matter of any one of the Examples 16-18 can optionally include where the connected metal creates an intrinsic capacitance.

[0084] In Example 20, the subject matter of any one of the Examples 15-19 can optionally include where the at least one metal layer satisfies a timing analysis for a design of the integrated circuit.

[0085] Example 21 is an integrated circuit (IC) assembly including a non-silicon substrate and at least one metal layer, where the at least one metal layer includes an electronic element and connected metal, where the connected metal was fill metal and is connected to a power grid for the integrated circuit.

[0086] In Example 22, the subject matter of Example 21 can optionally include where the connected metal creates an intrinsic capacitance.

[0087] In Example 23, the subject matter of any one of the Examples 21 and 22-23 can optionally include where the at least one metal layer does not include an intentional capacitor.

[0088] In Example 24, the subject matter of any one of the Examples 21-23 can optionally include where the at least one metal layer further includes fill metal that is not connected to the power grid.

[0089] In Example 25, the subject matter of any one of the Examples 22-24 can optionally include where the fill metal that is not connected to the power grid would affect a timing analysis if the fill metal was converted to connected metal.

Claims

1. An integrated circuit comprising:
at least one metal layer that includes:
an electronic element; and
connected metal, wherein the connected metal was fill metal and is connected to a power grid for the integrated circuit.
2. The apparatus of Claim 1, wherein the connected metal includes a same metal that is in at least a portion of the electronic element.
3. The apparatus of Claim 1, wherein the at least one metal layer does not include an intentional capacitor.
4. The apparatus of Claim 1, wherein the at least one metal layer further includes: fill metal that is not connected to the power grid.
5. The apparatus of Claim 4, wherein the fill metal that is not connected to the power grid is classified as critical fill metal.
6. The apparatus of Claim 4, wherein the fill metal that is not connected to the power grid would affect a timing analysis if the fill metal was converted to connected metal.
7. The apparatus of any one of Claims 1-4, wherein the connected metal creates an intrinsic capacitance.
8. The apparatus of any one of Claims 1-4, wherein the at least one metal layer satisfies a timing analysis for a design of the integrated circuit.
9. A method comprising:
designing an integrated circuit;
determining fill metal for the integrated circuit; and

connecting at least a portion of the determined fill metal to a power grid for the integrated circuit.

10. The method of Claim 9, further comprising:
determining if any of the fill metal is critical fill metal; and
not connecting the fill metal determined to be critical fill metal to the power grid.

11. The method of Claim 9, further comprising:
determining timing specifications for the integrated circuit; and
performing a timing analysis on the integrated circuit with the connected fill metal.

12. The method of Claim 11, further comprising:
disconnecting at least two fill metal that were connected to the power grid if the timing analysis does not satisfy the timing specifications for the integrated circuit.

13. The method of any one of Claims 9-11, further comprising:
determining an inherent capacitance of the connected fill metal.

14. The method of any one of Claims 9-11, further comprising:
determining an intentional capacitance for the integrated circuit.

15. The method of any one of Claims 9-11, wherein the integrated circuit includes an electronic element.

16. A computing device comprising:
a processor mounted on a substrate;
a communications logic unit within the processor;
a memory within the processor;
a graphics processing unit within the computing device;
an antenna within the computing device;
a display on the computing device;
a battery within the computing device;

a power amplifier within the processor;
a voltage regulator within the processor; and
an integrated circuit including at least one metal layer that includes:
 an electronic element; and
 connected metal, wherein the connected metal was fill metal and is connected to a power grid for the integrated circuit.

17. The computing device of Claim 16, wherein the at least one metal layer does not include an intentional capacitor.

18. The computing device of any one of Claims 16 and 17, wherein the at least one metal layer further includes:
 fill metal that is not connected to the power grid.

19. The computing device of any one of Claims 16-18, wherein the connected metal creates an intrinsic capacitance.

20. The computing device of any one of Claims 16-18, wherein the at least one metal layer satisfies a timing analysis for a design of the integrated circuit.

21. An integrated circuit (IC) assembly, comprising:
a non-silicon substrate; and
at least one metal layer that includes:
 an electronic element; and
 connected metal, wherein the connected metal was fill metal and is connected to a power grid for the integrated circuit.

22. The IC assembly of Claim 21, wherein the connected metal creates an intrinsic capacitance.

23. The IC assembly of Claim 21, wherein the at least one metal layer does not include an intentional capacitor.

24. The IC assembly of any one of Claims 22-23, wherein the at least one metal layer further includes:

fill metal that is not connected to the power grid.

25. The IC assembly of Claim 24, wherein the fill metal that is not connected to the power grid would affect a timing analysis if the fill metal was converted to connected metal.

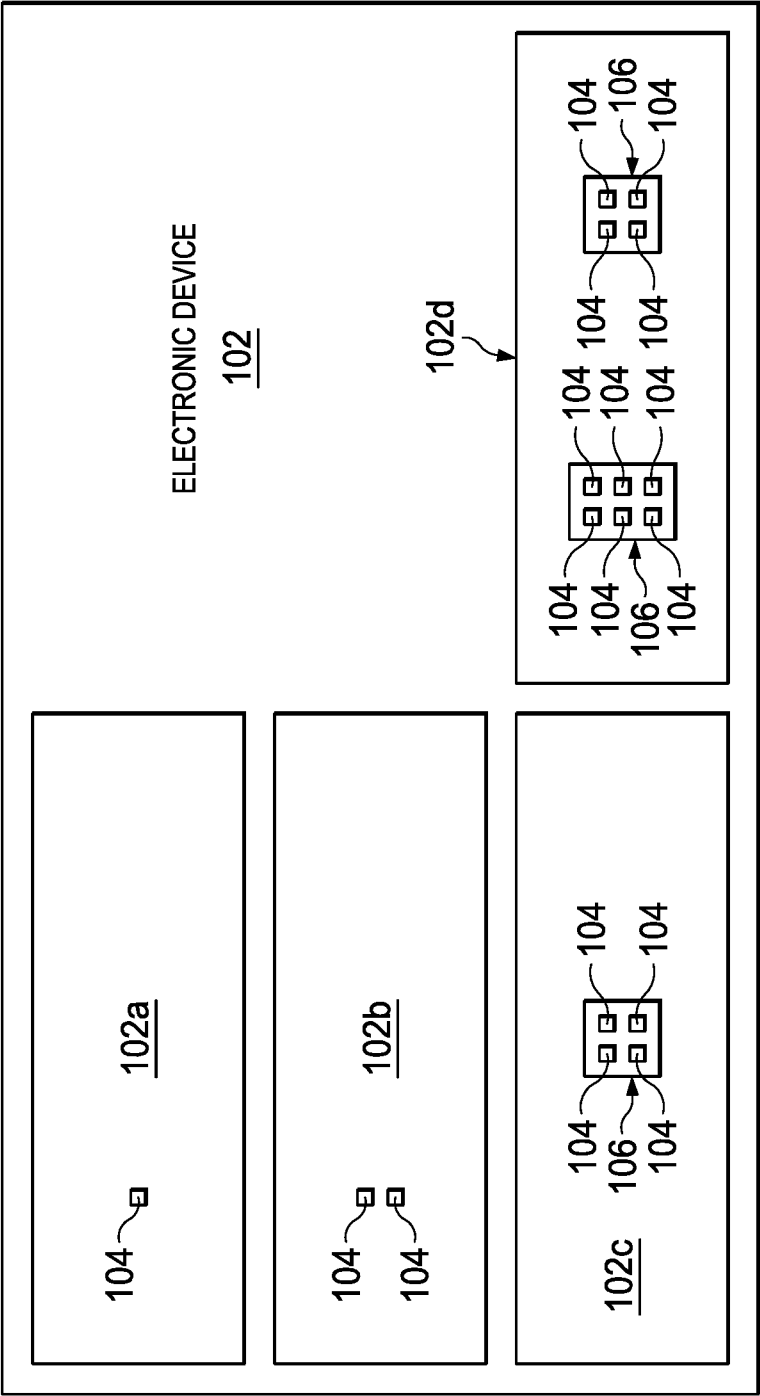


FIG. 1

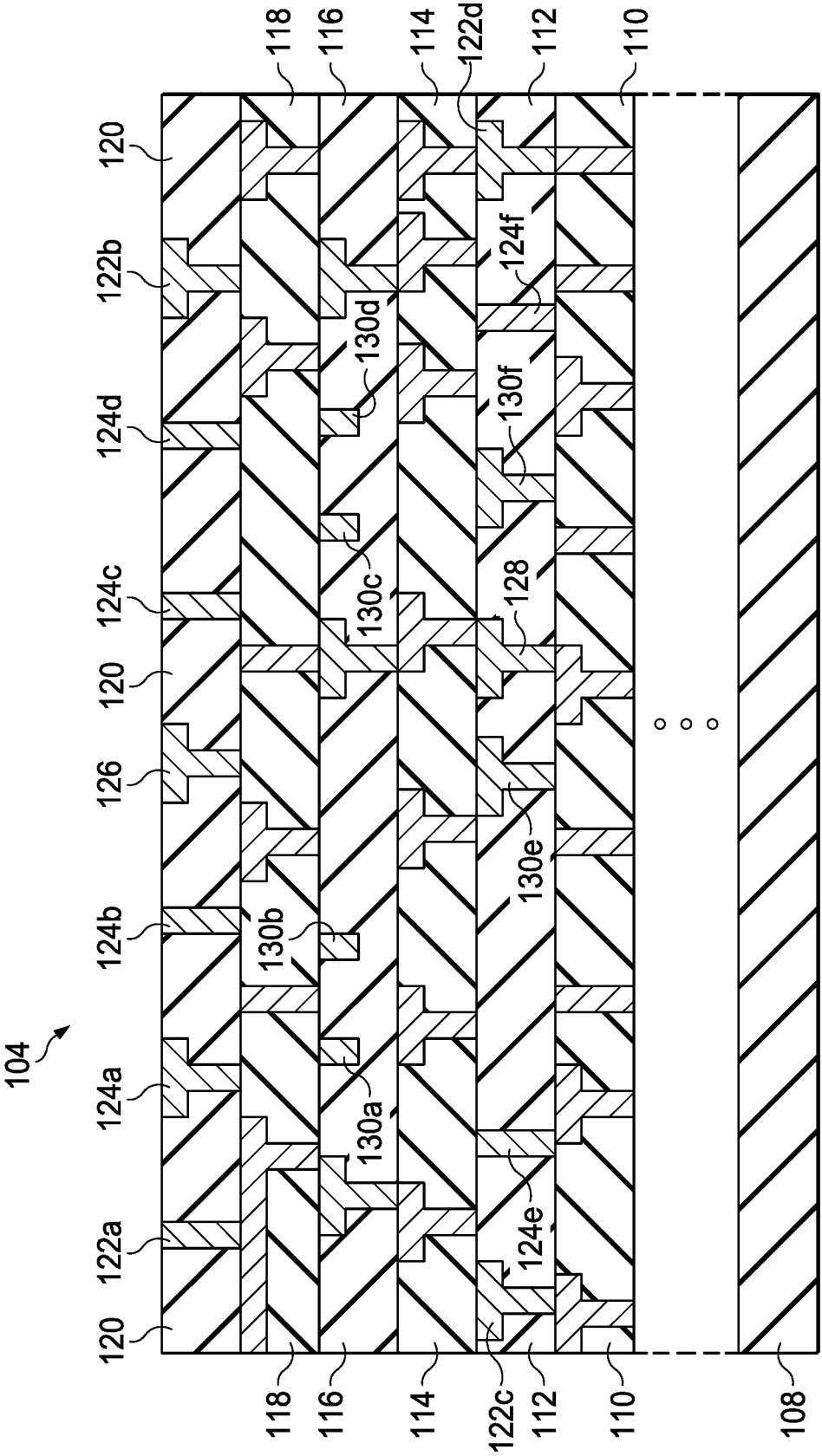


FIG. 2

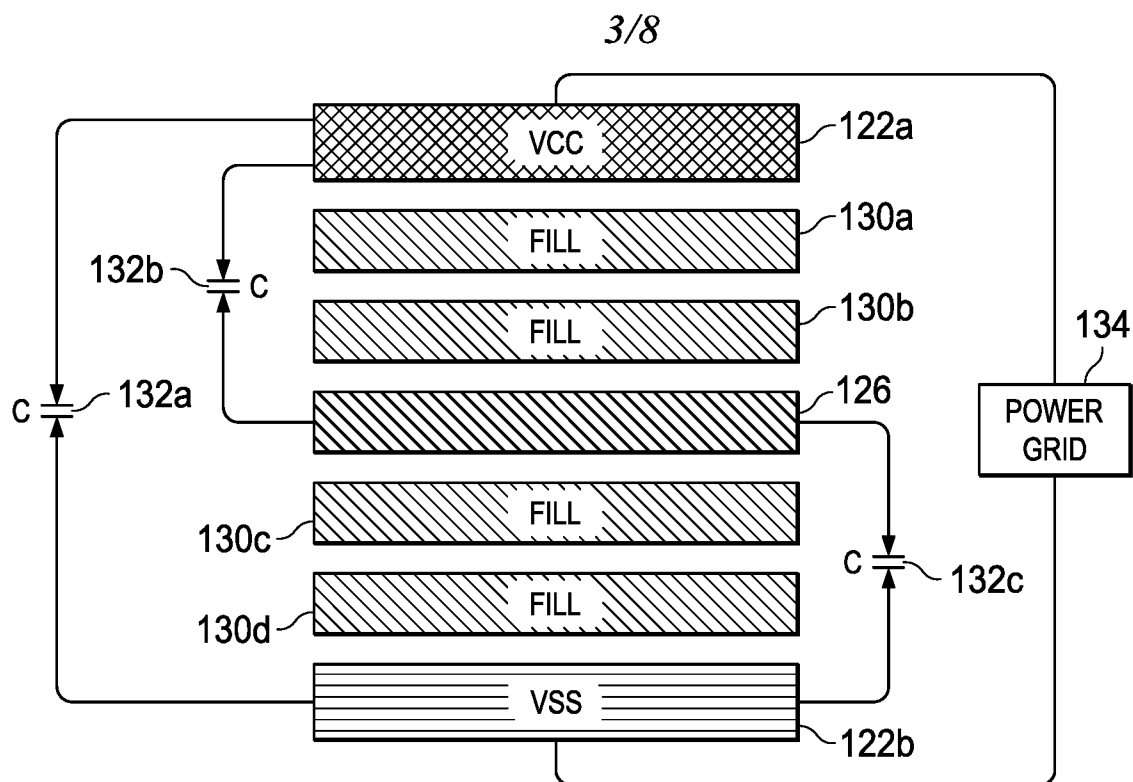


FIG. 3A

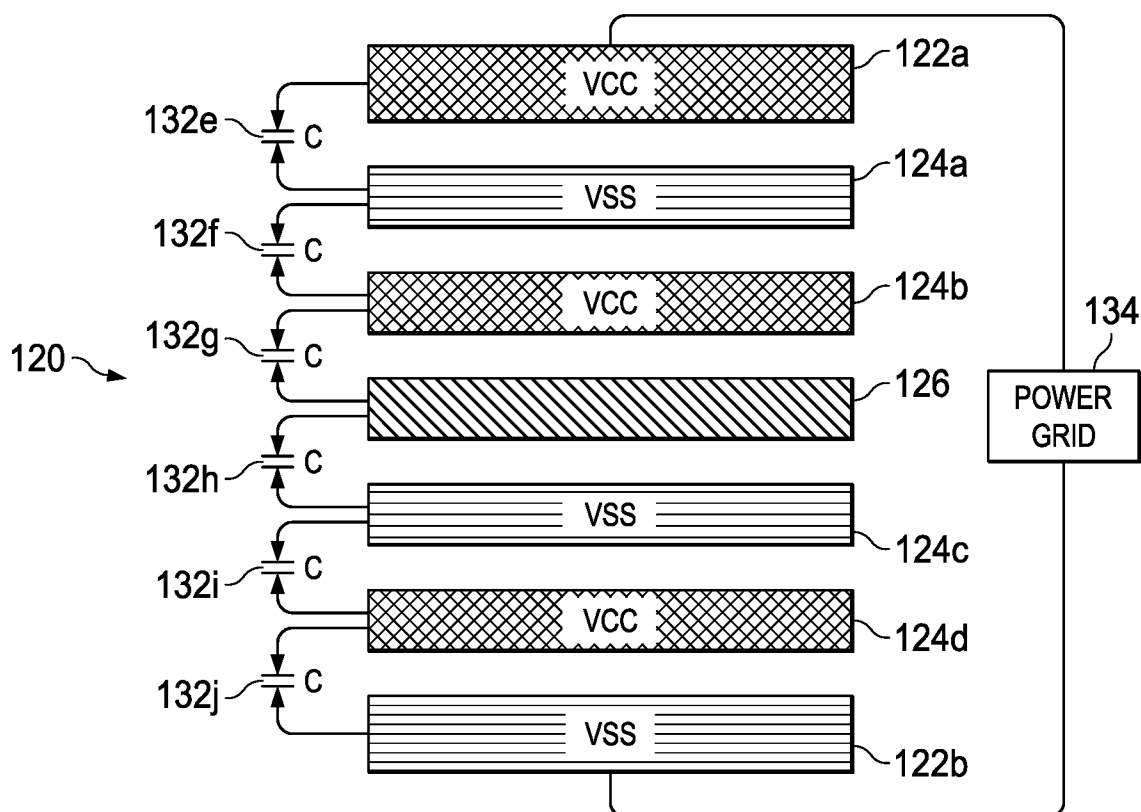


FIG. 3B

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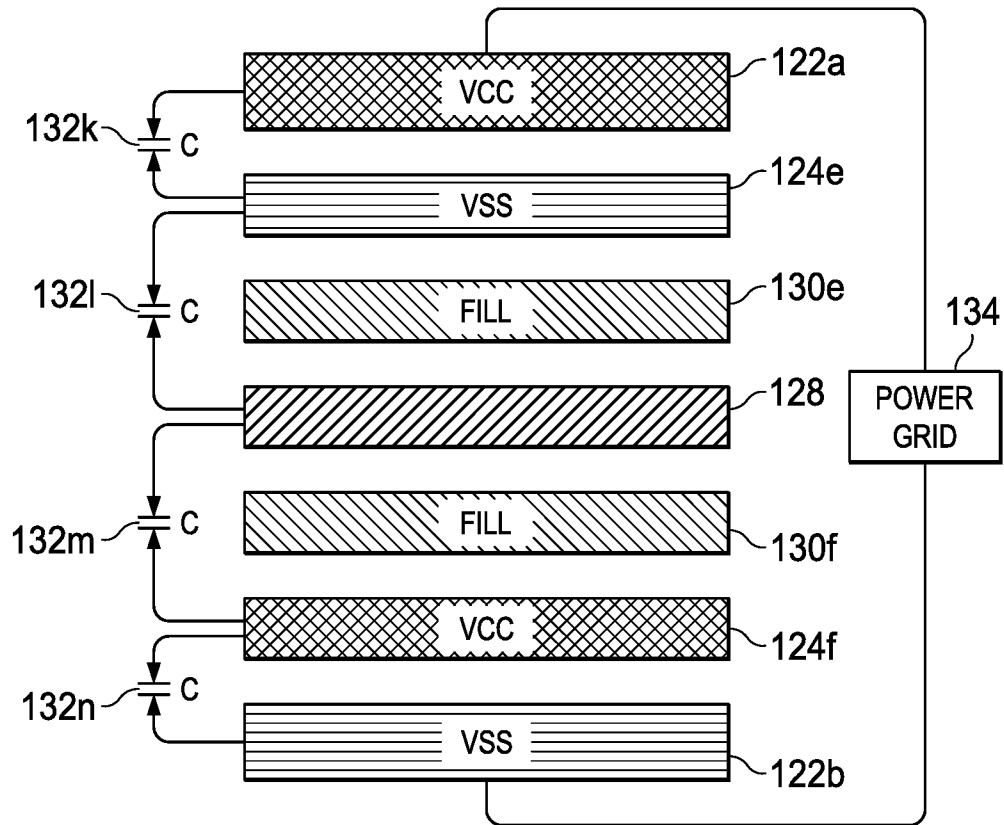


FIG. 3C

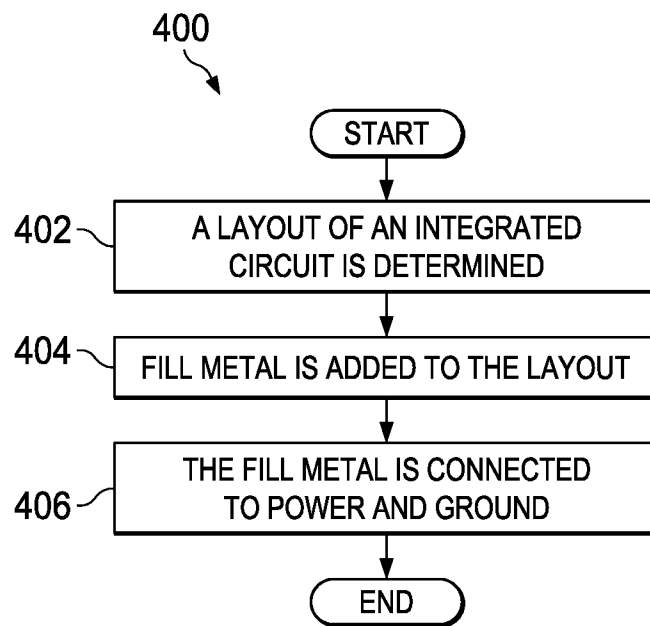


FIG. 4

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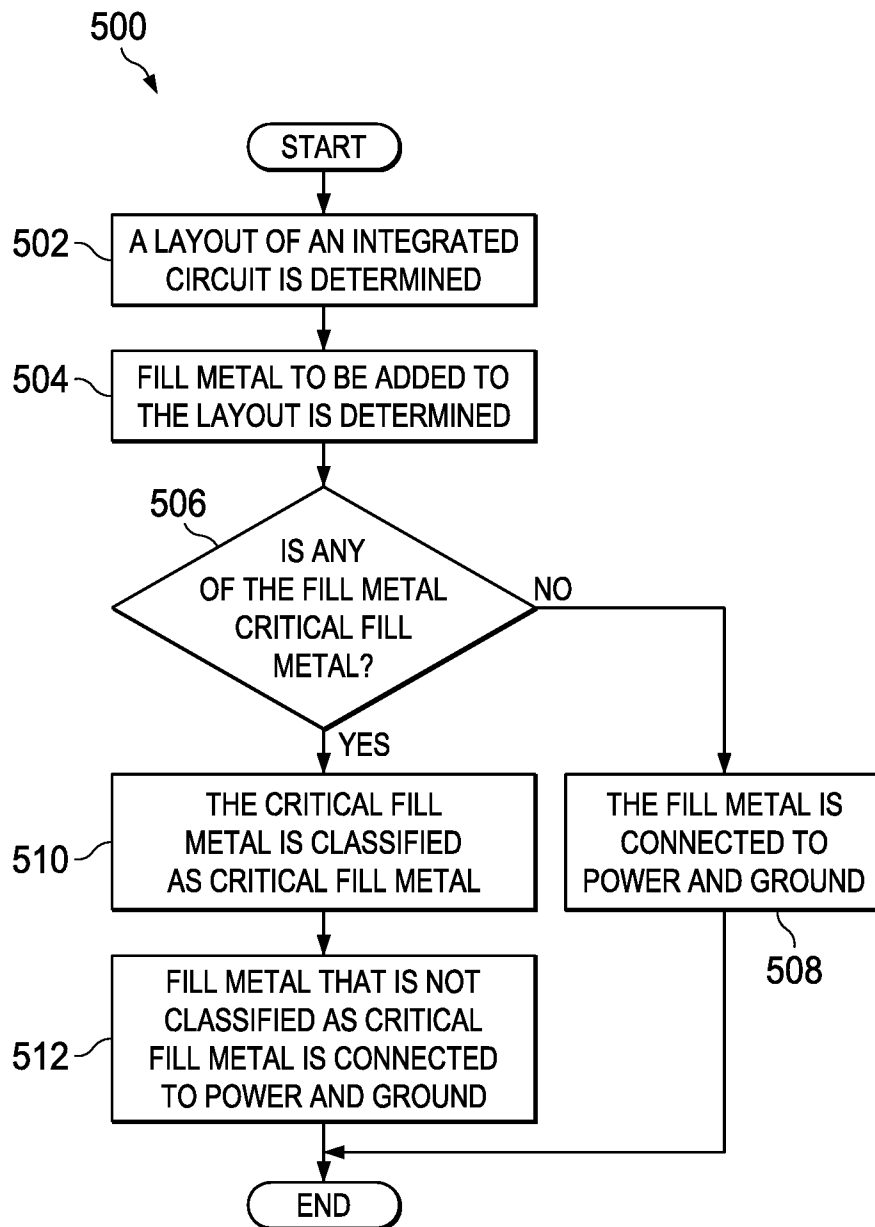


FIG. 5

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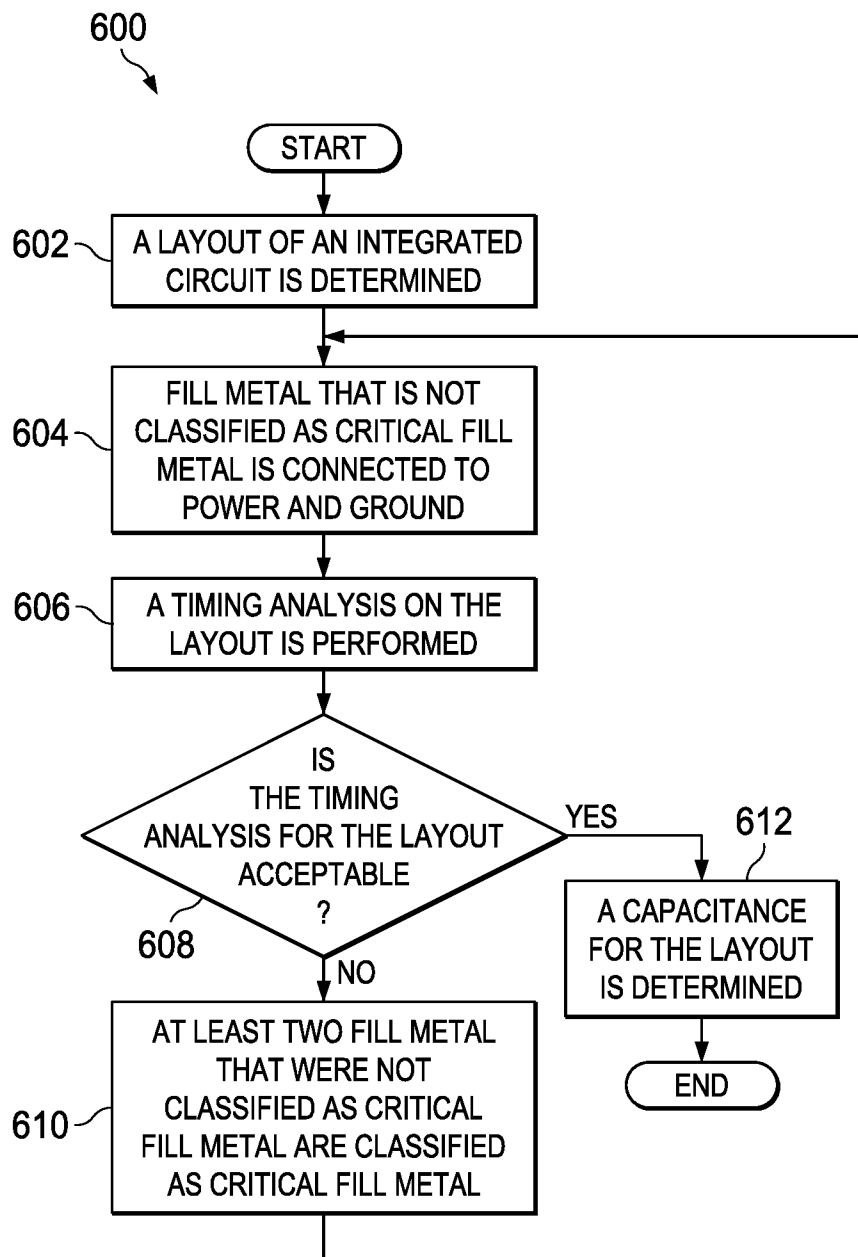


FIG. 6

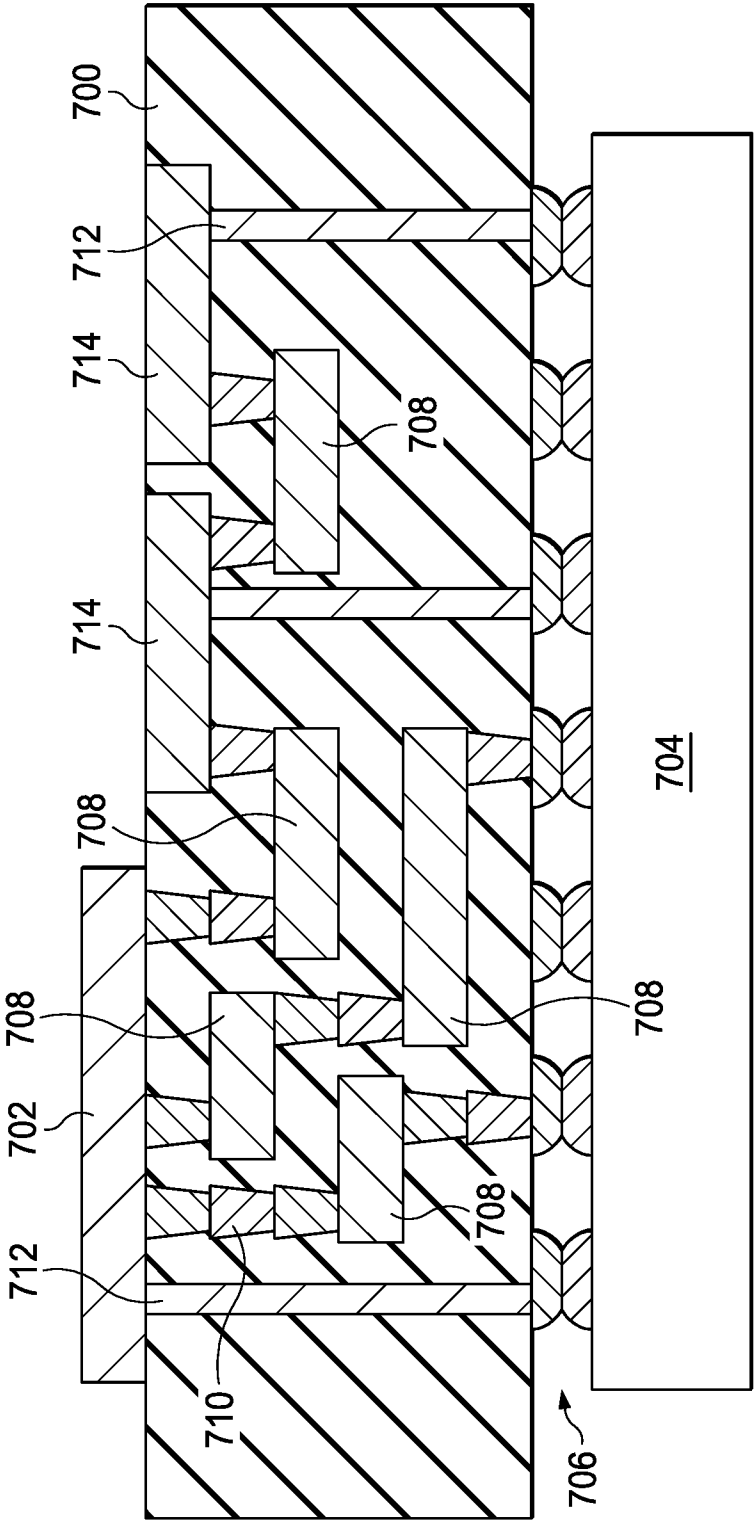


FIG. 7

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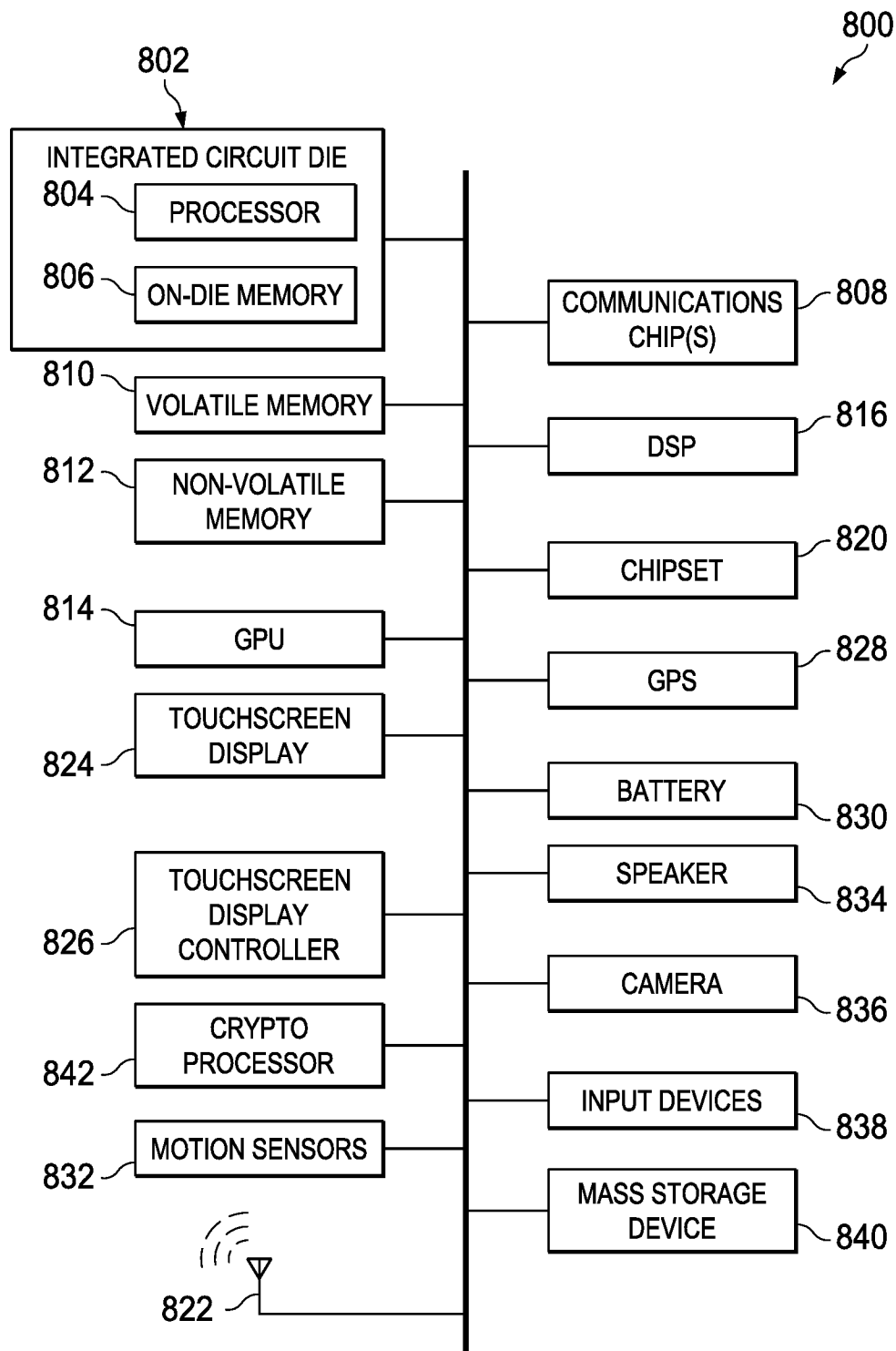


FIG. 8

A. CLASSIFICATION OF SUBJECT MATTER**H01L 23/14(2006.01)i, H01L 23/482(2006.01)i, H01L 23/522(2006.01)i, H01L 23/58(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 23/14; H01L 27/06; G06F 17/50; H01L 23/48; H01L 23/522; H03F 1/00; H04B 1/38; H01L 23/482; H01L 23/58

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: connected-metal, fill-metal, power, grid, capacitance, metal-layer timing-analysis, integrated-circuit

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011-0049721 A1 (KARAN B. KOTI et al.) 03 March 2011 See paragraphs [0031]-[0076]; claims 1, 15; and figures 1A-7.	1-15, 21-25
Y		16-20
Y	US 2012-0077551 A1 (FLORINEL G. BALTEANU et al.) 29 March 2012 See paragraphs [0034]-[0051]; and figures 1-6.	16-20
A	US 9552453 B1 (FREESCALE SEMICONDUCTOR, INC.) 24 January 2017 See claims 1-12; and figure 2.	1-25
A	US 2016-0155698 A1 (JAYONG KOO) 02 June 2016 See claims 1-8; and figures 4A, 5.	1-25
A	US 2008-0120586 A1 (STEPHAN HOEROLD) 22 May 2008 See claims 1-12; and figure 8.	1-25



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

20 December 2017 (20.12.2017)

Date of mailing of the international search report

20 December 2017 (20.12.2017)

Name and mailing address of the ISA/KR

International Application Division

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/027301

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