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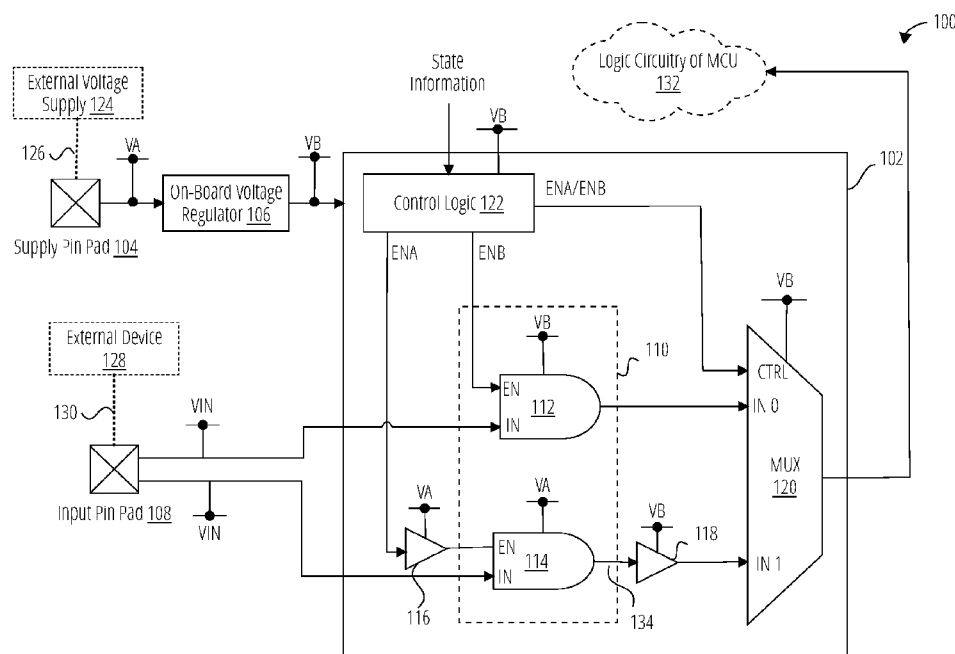


FIG. 1

(57) Abstract: One or more embodiments relate, generally, to microcontroller input/output (I/O) and limiting or disabling static current draw at general purpose inputs, including during low power situations where a voltage input may be lower than a supply voltage. In some embodiments, a general purpose input may include selectable input buffers and logic that is configured to selectively enable an input buffer associated with a voltage domain substantially the same as an input voltage of the general purpose input, and selectively disable the other input buffers.

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**SELECTABLE INPUT BUFFERS OF GENERAL PURPOSE INPUTS  
AND MICROCONTROLLERS HAVING THE SAME**

**PRIORITY CLAIM**

5           This application claims the benefit of the filing date of U.S. Provisional Patent Application No. 62/867,553, filed June 27, 2019 the entire contents and disclosure of which is hereby incorporated herein by this reference.

**FIELD**

10           The present disclosure relates, generally, to a general purpose input of a microcontroller, and more specifically, some embodiments relate to selectively disabling static current draw when a general purpose input is at a lower voltage domain than a voltage supply domain of a microcontroller associated with the input.

**BACKGROUND**

15           A general purpose input and output (GPIO) pin is an uncommitted digital signal pin in an integrated circuit (IC), such as a microcontroller without limitation. Since a GPIO pin has no predefined purpose, the purpose and behavior of a GPIO pin may be defined and implemented by a designer of a higher level system or circuitry. Typically,  
20           a GPIO pin is associated with an input (i.e., a “general purpose input”) or an output (i.e., a “general purpose output”) and with a specified supply voltage. An external device that interfaces with a microcontroller via a GPIO pin is chosen that operates at a voltage level (e.g., digital voltage levels) close to a supply voltage of the GPIO pin.

**BRIEF DESCRIPTION OF THE DRAWINGS**

25           While this disclosure concludes with claims particularly pointing out and distinctly claiming specific embodiments, various features and advantages of embodiments within the scope of this disclosure may be more readily ascertained from the following description when read in conjunction with the accompanying drawings,  
30           in which

          FIG. 1 is a block diagram depicting a general purpose input of a microcontroller, in accordance with one or more embodiments.

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FIG. 2 is a block diagram depicting general purpose inputs of a multi-voltage microcontroller system, in accordance with one or more embodiments.

FIG. 3 is a block diagram depicting a system for determining and/or generating control signals for setting a voltage domain of a general purpose input, in accordance  
5 with one or more embodiments.

FIG. 4 is a flowchart depicting a process, in accordance with one or more embodiments.

FIG. 5 is a block diagram depicting a multi-voltage sourced microcontroller, in accordance with one or more embodiments.

10 FIG. 6 is a block diagram depicting a wake circuit, in accordance with one or more embodiments.

FIG. 7 is a block diagram depicting a circuitry that may be used to implement various functions, operations, acts, processes, and/or methods, in accordance with one or more embodiments.

15

#### MODE(S) FOR CARRYING OUT THE INVENTION

In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which are shown, by way of illustration, specific examples of embodiments in which the present disclosure may be practiced.

20 These embodiments are described in sufficient detail to enable a person of ordinary skill in the art to practice the present disclosure. However, other embodiments may be utilized, and structural, material, and process changes may be made without departing from the scope of the disclosure.

The illustrations presented herein are not meant to be actual views of any  
25 particular method, system, device, or structure, but are merely idealized representations that are employed to describe the embodiments of the present disclosure. The drawings presented herein are not necessarily drawn to scale. Similar structures or components in the various drawings may retain the same or similar numbering for the convenience of the reader; however, the similarity in numbering  
30 does not mean that the structures or components are necessarily identical in size, composition, configuration, or any other property.

The following description may include examples to help enable one of ordinary skill in the art to practice the disclosed embodiments. The use of the terms

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“exemplary,” “by example,” and “for example,” means that the related description is explanatory, and though the scope of the disclosure is intended to encompass the examples and legal equivalents, the use of such terms is not intended to limit the scope of an embodiment or this disclosure to the specified components, steps, features,  
5 functions, or the like.

It will be readily understood that the components of the embodiments as generally described herein and illustrated in the drawing could be arranged and designed in a wide variety of different configurations. Thus, the following description of various embodiments is not intended to limit the scope of the present disclosure, but  
10 is merely representative of various embodiments. While the various aspects of the embodiments may be presented in drawings, the drawings are not necessarily drawn to scale unless specifically indicated.

Furthermore, specific implementations shown and described are only examples and should not be construed as the only way to implement the present disclosure  
15 unless specified otherwise herein. Elements, circuits, and functions may be shown in block diagram form in order not to obscure the present disclosure in unnecessary detail. Conversely, specific implementations shown and described are exemplary only and should not be construed as the only way to implement the present disclosure unless specified otherwise herein. Additionally, block definitions and partitioning of  
20 logic between various blocks is exemplary of a specific implementation. It will be readily apparent to one of ordinary skill in the art that the present disclosure may be practiced by numerous other partitioning solutions. For the most part, details concerning timing considerations and the like have been omitted where such details are not necessary to obtain a complete understanding of the present disclosure and are  
25 within the abilities of persons of ordinary skill in the relevant art.

Those of ordinary skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. Some drawings may illustrate signals as a single signal for clarity of presentation and description. It will be understood by a person of ordinary skill in the art that the signal  
30 may represent a bus of signals, wherein the bus may have a variety of bit widths and the present disclosure may be implemented on any number of data signals including a single data signal.

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The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a special purpose processor, a Digital Signal Processor (DSP), an Integrated Circuit (IC), an Application Specific Integrated Circuit (ASIC), a Field Programmable Gate Array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor (may also be referred to herein as a host processor or simply a host) may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, such as a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. A general-purpose computer including a processor is considered a special-purpose computer while the general-purpose computer is configured to execute computing instructions (e.g., software code) related to embodiments of the present disclosure.

The embodiments may be described in terms of a process that is depicted as a flowchart, a flow diagram, a structure diagram, or a block diagram. Although a flowchart may describe operational acts as a sequential process, many of these acts can be performed in another sequence, in parallel, or substantially concurrently. In addition, the order of the acts may be re-arranged. A process may correspond to a method, a thread, a function, a procedure, a subroutine, a subprogram, etc. Furthermore, the methods disclosed herein may be implemented in hardware, software, or both. If implemented in software, the functions may be stored or transmitted as one or more instructions or code on computer-readable media. Computer-readable media includes both computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another.

Any reference to an element herein using a designation such as “first,” “second,” and so forth does not limit the quantity or order of those elements, unless such limitation is explicitly stated. Rather, these designations may be used herein as a convenient method of distinguishing between two or more elements or instances of an element. Thus, a reference to first and second elements does not mean that only two elements may be employed there or that the first element must precede the second

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element in some manner. In addition, unless stated otherwise, a set of elements may comprise one or more elements.

As used herein, the term “substantially” in reference to a given parameter, property, or condition means and includes to a degree that one of ordinary skill in the art would understand that the given parameter, property, or condition is met with a small degree of variance, such as, for example, within acceptable manufacturing tolerances. By way of example, depending on the particular parameter, property, or condition that is substantially met, the parameter, property, or condition may be at least 90% met, at least 95% met, or even at least 99% met.

Static current is a leakage current that causes static power consumption at a buffer, or more specifically at one or more CMOS (Complementary Metal-Oxide Semiconductor) devices that form the buffer. In the case of a microcontroller, CMOS input buffers are expected (i.e., often assumed) to have 0 ampere static current draw. However, conventional CMOS input buffers known to inventors of this disclosure exhibit such a 0 ampere static current draw when their inputs voltages are at the voltage rails of a microcontroller’s supply, or at least within a device threshold of such rails, and when such CMOS input buffers include transistors that have negligible leakage (e.g., leakage current of a CMOS input buffer may be considered 0 amperes if less than 1 Nano Ampere (nA)).

When an external device (e.g., a sensor, a communication port, a bus, without limitation) operates at a lower voltage domain than a voltage domain of a microcontroller’s supply voltage, i.e. an input voltage is outside of the device threshold of such voltage rails, (and so lower than a voltage domain of a general purpose input that interfaces the external device to the microcontroller), the inventors of this disclosure now appreciate that an input buffer (e.g., a digital input buffer, a buffer gate, or a tristate buffer more generally, without limitation) of an input may draw a static current, irrespective of the logic state of a signal on the input pin. As a non-limiting example, if a microcontroller’s supply voltage is 5 volts and an input voltage received at an input buffer is 1.8 volts (e.g., a high logic state is observed in the voltage domain of the external device), then the input buffer will draw a static current due to the voltage difference between the input voltage and the microcontroller’s supply voltage.

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An option would be to change the voltage threshold in response to which an input buffer turns on (sometimes referred to as “lowering a trip-point”). Lowering a trip-point of an input buffer may cause static current draw to occur at input voltages closer to the voltage rails, however, the inventors of this disclosure appreciate that  
5 lowering a trip-point does not disable static current draw at a buffer when interfacing to a lower voltage domain than the voltage domain of a microcontroller’s supply voltage.

As used herein, the terms “no static current draw” and “zero static current draw” should be understood to encompass cases of zero current and cases of an  
10 inconsequential static current. Inconsequential may be defined by a threshold and so encompass a static current that is at or below a specified threshold. As non-limiting examples, a specified threshold may be a percentage of a specified sleep current of a device or a specified low power current of a device (*e.g.*, a microcontroller or other integrated circuit, without limitation). As a non-limiting example, for a low power  
15 microcontroller in some cases a static current equal to or less than 1% of a device’s sleep or low power current may be considered a zero static current.

As used herein, a reference to one or more elements as “selectable” herein means that such elements either collectively, individually, or as a combination, may operate responsive to one or more control signals. As a non-limiting example,  
20 selectable elements discussed herein may be enabled or disabled responsive to one or more control signals.

Some embodiments relate, generally, to means for selectively disabling static current draw while a general purpose input of a microcontroller (MCU) is at a lower voltage domain than an MCU’s supply voltage domain associated with the general  
25 purpose input.

Some embodiments relate, generally, to adjusting voltage rails of a general purpose input of an MCU when interfacing an input voltage domain with a supply voltage domain of an MCU, where the input voltage domain is lower than the MCU’s supply voltage domain.

30 One or more embodiments relate, generally, to a general purpose input of an MCU that includes a first input buffer and a second input buffer. The first input buffer is associated with the general purpose input and is supplied by an MCU supply voltage. The second input buffer is associated with the general purpose input and is

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supplied by a second supply voltage (e.g., a regulated voltage supply, without limitation) that has a lower voltage domain than a voltage domain of the MCU supply voltage, typically the second supply voltage is substantially equal to the lowest voltage domain of a general purpose input. The first input buffer and the second input buffer  
5 share a common input from an input pin pad of the general purpose input. Stated another way, the first input buffer and the second input buffer are each operatively coupled to the pad of the general purpose input.

In one or more embodiments, the first input buffer and a the second input buffer of the general purpose input may be selectively enabled and disabled via control  
10 signals, thereby selectively enabling/disabling static current draw at the general purpose input. In one embodiment, information for generating the control signals for enabling/disabling the first input buffer and the second input buffer may be stored at a read/write control register. In one embodiment, a read/write register may be accessible (e.g., by a designer or a host process, without limitation) by way of a register map of  
15 an MCU - in other words, a control register may be a memory mapped register. As non-limiting examples, bits of the control register may be operatively coupled to respective enablement inputs of the first and second input buffers, or may be read by digital logic configured to assert/de-assert enablement signals to respective enablement inputs of the input buffers.

20 In one or more embodiments, a second supply voltage is a regulated supply voltage generated internal to an MCU. As a non-limiting example, a first supply voltage may be regulated to the second supply voltage via an on-board voltage regulator of an MCU.

FIG. 1 is a schematic diagram depicting a general purpose input 100 of an  
25 MCU that includes circuitry configured to selectively disable static current draw at general purpose input 100, in accordance with one or more embodiments. As depicted by FIG. 1, general purpose input 100 may include static current draw cutoff circuit 102, a supply pin pad 104 of a supply pin 126, an input pin pad 108 of an input pin 130, and an on-board voltage regulator 106. As used herein, an “on-board”  
30 elements of a device (e.g., an on-board voltage regulator of an MCU, without limitation) is an element that is located at a device, as a non-limiting example, implemented by integrated circuitry of a device in a case of an integrated circuit chip, system or package.

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Supply pin pad 104 may be configured for operative coupling via a supply pin 126 to a voltage supply of an MCU that provides a supply voltage  $V_A$  (which may be one of many supply voltages of an MCU or a supply voltage of an MCU, without limitation). In the specific example depicted by FIG. 1, supply pin pad 104 is operable  
5 for operative coupling to external voltage supply 124, which may be a voltage supply of an MCU that includes general purpose input 100. Supply pin 126 and external voltage supply 124 are depicted by FIG. 1 with a dotted-line to denote they are external to general purpose input 100, and are optional elements of general purpose input 100.

10 An input of on-board voltage regulator 106 may be operatively coupled to supply pin pad 104 and an output of on-board voltage regulator 106 may be operatively coupled to static current draw cutoff circuit 102 and elements thereof as discussed herein. On-board voltage regulator 106 may be configured to generate and provide a regulated supply voltage  $V_B$  in response to supply voltage  $V_A$  received at an  
15 input of on-board voltage regulator 106. As discussed herein, in some embodiments regulated supply voltage  $V_B$  may be a digital supply voltage also characterized herein as a logic voltage level domain.

General purpose input 100 may be configured to provide both supply voltage  $V_A$  and regulated supply voltage  $V_B$  to static current draw cutoff circuit 102.

20 Input pin pad 108 may be configured for operative coupling via input pin 130 to external device 128, and more generally configured to facilitate operative coupling of external device 128 to general purpose input 100. It is specifically contemplated that a value of an input voltage  $V_{IN}$  at input pin pad 108 will be known or specified and so regulated supply voltage  $V_B$  may be chosen to match an input voltage domain of a  
25 device operatively coupled to input pin pad 108, namely input voltage  $V_{IN}$ . Notably,  $V_{IN}$  may be lower than  $V_B$  as long as  $V_{IN}$  is within a threshold voltage of  $V_B$ . In various embodiments, a value for  $V_B$  may be chosen to be within a threshold voltage of the lowest specified voltage of  $V_{IN}$ .

In one or more embodiments, general purpose input 100 may include circuitry  
30 arranged to selectively disable static current draw at general purpose input 100. In one embodiment the circuitry may include static current draw cutoff circuit 102, which is configured, generally, to selectively enable and disable static current draw of general purpose input 100. Static current draw cutoff circuit 102 may include selectable input

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buffers 110, here two input buffers - first input buffer 112 and second input buffer 114. Control logic 122 may be operatively coupled to respective “enable” inputs EN of first input buffer 112 and second input buffer 114, and to the select input of optional multiplexer (MUX) 120 having inputs IN0 and IN 1 operatively coupled to outputs of first input buffer 112 and second input buffer 114, respectively. Respective inputs IN of first input buffer 112 and second input buffer 114 may be operatively coupled to input pin pad 108. Supply voltage  $V_A$  and regulated supply voltage  $V_B$  may be provided to static current draw cutoff circuit 102 and components thereof, including power supply inputs of first input buffer 112 and second input buffer 114, respectively.

10 In some embodiments, control logic 122 may be configured to generate control signals such as assertions/desertions of ENA and ENB, without limitation. In some embodiments, control logic 122 may generate control signals in response to state information such as information about a power mode of a device that includes general purpose input 100.

15 In a contemplated use case, assume supply voltage  $V_A$  is 5 volts and regulated supply voltage  $V_B$  is 1.8 volts. Second input buffer 114 is supplied supply voltage  $V_A$  first input buffer 112 is supplied with regulated supply voltage  $V_B$ . Input voltage  $V_{IN}$  at input pin pad 108 is 1.8 volts (or within a device threshold of 1.8 volts as discussed above). So, external device 128 operates at a lower voltage domain than the rest of general purpose input 100 (i.e.,  $1.8v < 5v$ ), and more specifically, the input voltage  $V_{IN}$  at input pin pad 108 is at a lower voltage domain than supply voltage  $V_A$ . Control logic 122, in response to state information comprising, as non-limiting examples: a supplied control signal (e.g., a control bit of a control register - not shown), enables first input buffer 112 and disables second input buffer 114 (e.g., by de-asserting an enable signal ENA to input EN of second input buffer 114 and asserting an enable signal ENB to input EN of first input buffer 112). More specifically, in one embodiment, control logic 122 disables second input buffer 114 by holding a logic ‘0’ at an input EN of second input buffer 114 responsive to de-assertion of enable signal ENA, and enables first input buffer 112 by asserting and holding a logic ‘1’ at input EN of first input buffer 112 responsive to assertion of enable signal ENB. At first input buffer 112, since  $V_{IN}$  and  $V_B$  are both 1.8 volts (in practice,  $V_{IN}$  may be a little lower than  $V_B$  depending on device characteristics, for example,  $V_{IN}$  can be within a MOSFET device threshold voltage of  $V_B$ ), there is no static current draw at first input

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buffer 112. In other words, since  $V_{IN}$  is substantially equal to  $V_B$ , there is no static current draw at first input buffer 112.

MUX 120 is configured to select, and output, one or the other of the outputs of first input buffer 112 and second input buffer 114 provided at respective inputs IN 0 and IN 1 of MUX 120. In FIG. 1, outputs of first input buffer 112 and second input buffer 114 are operatively coupled to inputs IN 0 and IN 1 of MUX 120, respectively – in the case of second input buffer 114 via a voltage shifter, here a shift-down buffer 118 that translates the supply voltage level  $V_A$  down to the regulated supply voltage level  $V_B$ , the logic level. The output of MUX 120 may be supplied to the logic circuitry of the MCU 132 (e.g., integrated circuitry, without limitation) and components implemented therein as desired. MUX 120 is controllable via ENA/ENB to select between signals at inputs IN 0 and IN 1 by, or in response to, the enable means used to enable/disable second input buffer 114 and/or first input buffer 112 (by e.g., control logic 122, without limitation). In the specific example depicted by FIG. 1, MUX 120 is controllable via control signal ENA/ENB provided by control logic 122, such that when second input buffer 114 is enabled (and first input buffer 112 is disabled), IN 1 is selected, and when first input buffer 112 is enabled (and second input buffer 114 is disabled), IN 0 is selected. MUX 120 is optional, so in some embodiments not depicted by the figures, outputs of first input buffer 112 and second input buffer 114 may be un-multiplexed and, as a non-limiting example, operatively coupled to the same or different peripherals of an MCU via logic circuitry of MCU 132. Moreover, in some embodiments, it is specifically contemplated that control logic 122 may be configured such that ENA and ENB may both be set equal to 0, disabling both input buffers, in which case MUX 120 may be configured to randomly select one of IN 0 and IN 1.

In some cases, control logic 122, MUX 120 and/or the logic circuitry of MCU 132 may operate at a voltage domain substantially at regulated supply voltage  $V_B$ , as a non-limiting example, when  $V_B$  is substantially equal to logic voltage level of the MCU. Stated another way, second input buffer 114 may interface with an external device 128 that operates at a higher voltage domain than the voltage domain of the integrated circuitry of an MCU including general purpose input 100. In some embodiments, general purpose input 100 may include first and second voltage shifters, here, shift-up buffer 116 and shift-down buffer 118, on a path that includes second

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input buffer 114. Shift-up buffer 116 is configured to shift signal ENA provided by control logic 122 in a voltage domain commensurate with regulated supply voltage  $V_B$  (e.g., a logic voltage level) to a voltage level commensurate with supply voltage  $V_A$ . Shift-down buffer 118 is configured to shift the digitized result 134 output by second  
5 input buffer 114 from a level that is in a voltage domain commensurate with supply voltage  $V_A$  to a level commensurate with regulated supply voltage  $V_B$  appropriate for MUX 120 (e.g., a logic voltage level). Shift-up-buffer 116 is thus arranged on an enable input path of second input buffer 114 and shift-down-buffer is thus arranged on an output path of second input buffer 114.

10 Using an alternative case as an example to illustrate a contemplated operation of shift-up buffer 116 and shift-down buffer 118, if control logic 122 enables second input buffer 114 instead of first input buffer 112 while  $V_{in} = 1.8\text{ V}$  and supply voltage  $V_A$  is 5 V, the voltage supplied to shift-up buffer 116 is  $V_A$ , and so shift-up buffer 116 outputs a 5 volt signal in response to a logic '1' supplied by control logic 122 on  
15 signal ENA (in this example logic '1' on signal ENA is about 1.8 V, which is above a trip-point of shift-up buffer 116). A 5 volt signal at enable input EN and a 1.8 volt signal (i.e.,  $V_{in}$ ) at input IN of second input buffer 114 is sufficient to trip second input buffer 114, which also outputs a 5 volt signal because it is supplied by supply voltage  $V_A$ . The output of second input buffer 114 is provided to an input of shift-  
20 down buffer 118, which is configured to output a 1.8 volt signal (i.e., the level of commensurate with regulated supply voltage  $V_B$  in this example) in response to receiving a 5 volt signal from second input buffer 114.

Notably, in this alternative case, while  $V_{in}$  (1.8 v) is high enough to trip second input buffer 114, the difference between  $V_A$  and  $V_{IN}$  is sufficient to cause static current  
25 draw at second input buffer 114, as long as signal ENA is asserted. When signal ENA is de-asserted, there is no static current draw at second input buffer 114.

Some embodiments relate, generally to a multi-voltage MCU where one or more general purpose inputs (GPI(s)) are associateable with a first voltage domain (e.g., a supply voltage domain of an MCU, without limitation) and one or more general  
30 purpose inputs are associateable with a second voltage domain that is lower than the first voltage domain.

FIG. 2 shows a schematic diagram of a general purpose inputs 200 of a multi-voltage microcontroller system, in accordance with one or more embodiments. In the

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specific example depicted by FIG. 2, the general purpose inputs 200 of a multi-voltage microcontroller system include general purpose input 100 discussed with reference to FIG. 1 above, although for brevity, control logic 122 and external voltage supply 124 are not depicted. General purpose inputs 200 also includes a second general purpose  
5 input 204 associated, at least in part, with a different voltage domain than general purpose input 100, namely, voltage domain  $V_C$ . Input buffer 208 is supplied by regulated supply voltage  $V_B$  and input buffer 212 is supplied by supply voltage  $V_C$ .

Second general purpose input 204 includes an input pin pad 206 operatively coupled to respective inputs of input buffer 208 and input buffer 212. When input  
10 buffer 212 is enabled by enablement signals ENA/ENB, shift-up buffer 210 converts a digital enable signal ENA from the logic voltage level of regulated supply voltage  $V_B$  to the voltage level of supply voltage  $V_C$  (the voltage domain of input buffer 212) and provides shifted-up ENA to an enable input of input buffer 212. Input voltage  $V_{IN}$  is received at a respective input pin of input buffer 212, and in response to  $V_{IN}$  and  
15 shifted-up ENA, input buffer 212 provides digitized result 214 at voltage domain  $V_C$ . Digitized result 214 is received at shift-down buffer 216, which converts digitized result 214 to a voltage domain of regulated supply voltage  $V_B$ , here the logic level voltage domain of the MCU, and provides (now shifted-down) digitized result 214 to multiplexer 218.

20 When input buffer 208 is enabled by enablement signal ENB provided to an enable input of input buffer 208, an input voltage  $V_{IN}$  is received at a respective input of input buffer 208, and input buffer 208 outputs a digitized result 220 at voltage domain of regulated supply voltage  $V_B$ . The digitized result 220 is provided to multiplexer 218. Multiplexer 218 selects one of the inputs having the digitized  
25 result 214 or digitized result 220 in response to enablement signals ENA/ENB and provides the signal at its selected input to MCU logic.

Notably, general purpose input 100 and general purpose input 204 have a common digital voltage supply, the regulated voltage  $V_B$ .  $V_B$  is dependent on  $V_A$  and so general purpose input 204 can select between a supply voltage  $V_C$  and a regulated  
30 supply voltage  $V_B$  that is not dependent on supply voltage  $V_C$ . Stated another way,  $V_C$  and  $V_B$  are independent, which gives the system more flexibility.

The specific arrangement for supply of  $V_A$ ,  $V_B$ , and  $V_C$  depicted by FIG. 2 – supply voltage  $V_A$  regulated to regulated supply voltage  $V_B$  and supply voltage  $V_C$

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(and any additional supply voltages) – is exemplary and other arrangements are encompassed by this description. As non-limiting examples, one or more of supply voltages  $V_A$ ,  $V_B$ , and  $V_C$  may be supplied by a switch network. As a further non-limiting example, regulated supply voltage  $V_B$ , may be selected from among multiple on-board voltage regulators (e.g., by a multiplexer, without limitation). As a further non-limiting example, supply voltages  $V_A$  and  $V_B$  may both be regulated from another supply voltage by an on-board voltage regulator that is configured to regulate the other supply voltage to provide supply voltage  $V_A$  during a first mode and to regulate the other supply voltage to provide regulated supply voltage  $V_B$  during a second mode.

Notably, voltage shifters associated with an input buffer supplied by  $V_C$  (e.g., input buffer 212) may be configured to shift to voltage level  $V_C$  regardless of whether voltage level  $V_C$  is above or below voltage level  $V_B$ . So, what is generally referred to in the discussion above as a voltage upshift of ENA signal when  $V_C$  is above  $V_B$  may be generally referred to as a voltage downshift in a case where  $V_C$  is below  $V_B$ . Any suitable circuit and/or device known to a person having ordinary skill in the art may be used for voltage shifting. As non-limiting examples, dedicated up and down voltage shifters may be used as well as up/down shifters that operate without regard to which voltage domain is higher or lower.

As discussed herein, in some embodiments control signals for setting a voltage domain of GPIs and thereby selectively disabling static current draw may be determined and/or generated in response to one or more user specified parameters (i.e., a user of the GPI). Such user specified parameters may be provided, as non-limiting examples, in response detecting coupling of an external device to an input pin pad that has a lower voltage domain than a supply voltage domain of an MCU in response to a power management protocol, or in response to other settings.

FIG. 3 is a block diagram depicting a system 300 for determining and/or generating control signals (e.g., ENA, and ENB, without limitation) for setting a voltage domain of a GPI e.g., general purpose input 100 or general purpose inputs 200, without limitation, in accordance with one or more embodiments. As depicted by FIG. 3, system 300 may include a control register 302 and a control logic 304.

Control register 302 may be configured to store one or more control bits indicative of a voltage domain, and, in a contemplated operation, control logic 304 may be configured to read control bits of control register 302, determine a control

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signal responsive to read control bits, and provide a control signal Selection to selectable input buffers of a GPI. In the cases discussed with reference to FIG. 1 and FIG. 2, Selection may include enablement signals ENA/ENB. In one embodiment, the control bits stored at control register 302 and read by control logic 304 may be user-  
5 specified, as a non-limiting example, during setup of a GPI or in real-time.

FIG. 4 is a flowchart depicting a process 400 for selectively disabling static current draw at a general purpose input of an MCU, in accordance with one or more embodiments.

In operation 402, process 400 receives a supply voltage. In some embodiments,  
10 the supply voltage is generated by an external voltage supply (e.g., external voltage supply 124, without limitation) and received via a supply pin of an MCU (e.g., supply pin 126 or a pin operable for operative coupling to a supply pin such as supply pin pad 202, 502, 504, or 506, without limitation). In other embodiments the supply voltage may be regulated from an external supply voltage received at an MCU.

15 In operation 404, process 400 generates a regulated supply voltage responsive to the supply voltage. In some embodiments, a voltage regulator (e.g., on-board voltage regulator 106 or on-board voltage regulator 508, without limitation) generates the regulated supply voltage. A voltage level of the regulated supply voltage is within a device threshold of a lowest specified input voltage (e.g., a device threshold of a  
20 device (e.g., a MOSFET transistor, without limitation) of an input buffer 112, 208, or 518, without limitation).

In operation 406, process 400 provides the regulated supply voltage to a first input buffer (e.g., first input buffer 112, input buffer 208, or input buffer 518, without limitation) of a first general purpose input.

25 In operation 408, process 400 provides the supply voltage to a second input buffer (e.g., second input buffer 114, without limitation) of the first selectable input buffers of the first general purpose input.

In operation 410, process 400 enables the first input buffer and disables the second input buffer, and thereby selectively disable static current draw at the general  
30 purpose input when an input voltage at the first general purpose input is less than the first supply voltage. In some embodiments, control logic (e.g., control logic 122, without limitation) may generate enablement signals that enable the first input buffer

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and disable the second input buffer and thereby selectively disable static current draw at the first general purpose input.

In operation 412, process 400 may optionally continuously supply (i.e., generate and provide) the regulated supply voltage during a lowest voltage configurable sleep mode of the microcontroller. In some embodiments, the voltage regulator that generates the regulated supply voltage in operation 406 continuously supplies the regulated supply voltage. In some embodiments, the general purpose input uses about 1 microampere (uA) or less of current to operate while a microcontroller including the general purpose input is in a lowest voltage mode. More specifically, an onboard voltage regulator may use about 1 uA or less to generate a regulated supply voltage provided to the general purpose input during the lowest voltage mode.

FIG. 5 is a schematic diagram of a multi-voltage sourced microcontroller 500, in accordance with one or more embodiments. Arrangements depicted by FIG. 1 and FIG. 2 may be characterized as single-voltage sourced and multi-voltage sourced, respectively, because they include a single supply pin pad 104 and dual supply pin pads 104 and 202, respectively.

Multi-voltage sourced microcontroller 500 includes first supply pin pad 502, second supply pin pad 504, and optional more supply pin pads 506 operable for operative couplings to individual voltage supply sources, here the voltage supply sources including a first voltage supply, a second voltage supply and an Nth voltage supply providing supply voltages  $VA(0)$ ,  $VA(1)$  to  $VA(N)$ , respectively. At least one of the supply pin pads is operatively coupled to a voltage regulator, here, voltage regulator 508, which is configured to generate regulated supply voltage  $V_B$  responsive to supply voltage  $VA(0)$ .

Multi-voltage sourced microcontroller 500 may be configured to provide supply voltages  $VA(0)$ ,  $VA(1)$  to  $VA(N)$  and regulated supply voltage  $V_B$  to general purpose input 510, and to respective individual input buffers: input buffer 512, input buffer 514, input buffer 516, and input buffer 518. Input pin pad 520 is operatively coupled to an input of each of input buffer 512, input buffer 514, input buffer 516 and input buffer 518. Each of input buffer 512, input buffer 514, input buffer 516, and input buffer 518 may be controlled via control signals received at respective enable inputs operatively coupled to mapped control register 522. While not depicted by

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FIG. 5, the respective control signal paths between mapped control register 522 and the input buffers may include voltage shifting circuitry, e.g., shift-up buffer 116 and shift-down buffer 118, without limitation.

In operation, mapped control register 522 is arranged to enable a respective one  
5 of input buffer 512, input buffer 514, input buffer 516, and input buffer 518 whose supply voltage is commensurate with the voltage of input signal received at, or expected to be received at input pin pad 520, and disable the other ones of input buffer 512, input buffer 514, input buffer 516, and input buffer 518 so as to prevent static current draw. Mapped control register 522 is further arranged to disable input  
10 buffer 512, input buffer 514, and input buffer 516 and enable input buffer 518 when VIN is less than VA(0) to VA(N) and thereby disable static current draw at general purpose input 510.

In one or more embodiments, an on-board voltage regulator such as on-board voltage regulator 106, and on-board voltage regulator 508, without limitation, may be  
15 configured to continuously generate a regulated supply voltage disclosed herein. As a non-limiting example, such an on-board voltage regulator may be an “always on” type voltage regulator for providing a regulated supply voltage to at least some integrated circuitry of an MCU including integrated circuitry other than a general purpose input or selectable input buffers more generally.

In one or more embodiments, such an on-board voltage regulator may be  
20 configured to continuously generate a regulated supply voltage in response to a current source that is specified at least partially based on a lowest power consumption or other desired power consumption of a device that includes the on-board voltage regulator. In one or more embodiments, a lowest power consumption may correspond to a sleep  
25 mode or to lowest power mode of a device that includes the on-board voltage regulator. As a non-limiting example, a regulated supply voltage may be generated from 1uA current or less due to power consumption limits during a specific power mode of a device, and thereby power a general purpose input (e.g., general purpose input 100 or 204, without limitation) using 1uA current or less.

30 Using an always on type voltage regulator may be convenient because, among other reasons, MCU's often include such a voltage regulator for other purposes than supplying a general purpose input. Notably, a person having ordinary skill in the art will recognize many suitable arrangements for generating a regulated supply voltage

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encompassed by disclosed embodiments, including without limitation an on-board voltage regulator or an external voltage regulator that supplies a regulated supply voltage via a regulated supply voltage pin of an MCU.

A person having ordinary skill in the art will recognize many advantages and  
5 uses for described embodiments. One such use case is for valid activity detection at general purpose input while a device is in a low power mode of operation. Static current draw might deplete a power source such as a battery or cause a device to operate outside a specification for low power.

FIG. 6 is a block diagram depicting a wake circuit 600 for operative coupling to  
10 a transmission medium such as a coaxial cable or twisted pair for an Ethernet bus, without limitation, via GPIO 602. GPIO 602 may be or include a general purpose input 100, without limitation.

GPIO 602 and activity detector 604 can operate in a low power domain 614 associated with a low power mode or an operational domain, such as when  
15 transmitting and receiving data over the bus. When in a low power mode, power management unit 606 configures GPIO 602 via control signal power management control 616 to disable static current draw. By way of non-limiting example, the control signal power management control 616 may comprise ENA and ENB for disabling second input buffer 114 and enabling first input buffer 112 of FIG. 1, and thereby  
20 disabling static current draw at GPIO 602 while operating in low power mode. While in low power mode, GPIO 602 may receive bus activity 608 (e.g., voltage levels, without limitation) and provide digitized versions of those signals, as digitized bus activity 610, to activity detector 604. Activity detector 604 is configured to detect valid bus activity (e.g., voltage levels within a threshold or having a sufficient  
25 duration, without limitation) and provide activity reporting signal 612 to inform power management unit 606 that valid bus activity has been detected. Power management unit 606, in response to activity reporting signal 612 indicating valid bus activity, may take appropriate action, including without limitation, turning on supply of power to a device that includes wake circuit 600 and configuring GPIO 602 for an operational  
30 power mode via control signal power management control 616.

FIG. 7 is a block diagram depicting a circuitry 700 that, in some embodiments, may be used to implement various functions, operations, acts, processes, and/or methods disclosed herein. The circuitry 700 includes one or more processors 702

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(sometimes referred to herein as “processors 702”) operatively coupled to one or more apparatuses such as data storage devices (sometimes referred to herein as “storage 704”), without limitation. The storage 704 includes machine executable code 706 stored thereon (e.g., stored on a computer-readable memory) and the  
5 processors 702 include logic circuitry 708. The machine executable code 706 include information describing functional elements that may be implemented by (e.g., performed by) the logic circuitry 708. The logic circuitry 708 is adapted to implement (e.g., perform) the functional elements described by the machine executable code 706. The circuitry 700, when executing the functional elements described by the machine  
10 executable code 706, should be considered as special purpose hardware configured for carrying out functional elements disclosed herein. In some embodiments the processors 702 may be configured to perform the functional elements described by the machine executable code 706 sequentially, concurrently (e.g., on one or more different hardware platforms), or in one or more parallel process streams.

15 When implemented by logic circuitry 708 of the processors 702, the machine executable code 706 is configured to adapt the processors 702 to perform operations of embodiments disclosed herein. For example, the machine executable code 706 may be configured to adapt the processors 702 to perform at least a portion or a totality of the operations discussed for general purpose input 100, general purpose inputs 200,  
20 system 300, multi-voltage sourced microcontroller 500, and wake circuit 600, without limitation.

As a specific, non-limiting example, the machine executable code may be configured to instruct the processors 702 to perform at least some functions of general purpose input 100, general purpose inputs 200, system 300, process 400,  
25 microcontroller 500, and wake circuit 600, without limitation.

The processors 702 may include a general purpose processor, a special purpose processor, a central processing unit (CPU), an MCU, a programmable logic controller (PLC), a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field-programmable gate array (FPGA) or other programmable logic device,  
30 discrete gate or transistor logic, discrete hardware components, other programmable device, or any combination thereof designed to perform the functions disclosed herein. A general-purpose computer including a processor is considered a special-purpose computer while the general-purpose computer is configured to execute computing

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instructions (e.g., software code) related to embodiments of the present disclosure. It is noted that a general-purpose processor (may also be referred to herein as a host processor or simply a host) may be a microprocessor, but in the alternative, the processors 702 may include any conventional processor, controller, microcontroller, or  
5 state machine. The processors 702 may also be implemented as a combination of computing devices, such as a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

In some embodiments the storage 704 includes volatile data storage (e.g.,  
10 random-access memory (RAM), without limitation), non-volatile data storage (e.g., Flash memory, a hard disc drive, a solid state drive, erasable programmable read-only memory (EPROM), without limitation). In some embodiments the processors 702 and the storage 704 may be implemented into a single device (e.g., a semiconductor device product, a system on chip (SOC), without limitation). In some embodiments the  
15 processors 702 and the storage 704 may be implemented into separate devices.

In some embodiments the machine executable code 706 may include computer-readable instructions (e.g., software code, firmware code, without limitation). By way of non-limiting example, the computer-readable instructions may be stored by the storage 704, accessed directly by the processors 702, and executed by the  
20 processors 702 using at least the logic circuitry 708. Also by way of non-limiting example, the computer-readable instructions may be stored on the storage 704, transmitted to a memory device (not shown) for execution, and executed by the processors 702 using at least the logic circuitry 708. Accordingly, in some embodiments the logic circuitry 708 includes electrically configurable logic  
25 circuitry 708.

In some embodiments the machine executable code 706 may describe hardware (e.g., circuitry) to be implemented in the logic circuitry 708 to perform the functional elements. This hardware may be described at any of a variety of levels of abstraction, from low-level transistor layouts to high-level description languages. At a high-level  
30 of abstraction, a hardware description language (HDL) such as an Institute of Electrical and Electronics Engineers (IEEE) Standard hardware description language (HDL) may be used, without limitation. By way of non-limiting examples, Verilog™,

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SystemVerilog™ or very large scale integration (VLSI) hardware description language (VHDL™) may be used.

HDL descriptions may be converted into descriptions at any of numerous other levels of abstraction as desired. As a non-limiting example, a high-level description  
5 can be converted to a logic-level description such as a register-transfer language (RTL), a gate-level (GL) description, a layout-level description, or a mask-level description. As a non-limiting example, micro-operations to be performed by hardware logic circuits (e.g., gates, flip-flops, registers, without limitation) of the logic circuitry 708 may be described in a RTL and then converted by a synthesis tool into a  
10 GL description, and the GL description may be converted by a placement and routing tool into a layout-level description that corresponds to a physical layout of an integrated circuit of a programmable logic device, discrete gate or transistor logic, discrete hardware components, or combinations thereof. Accordingly, in some embodiments the machine executable code 706 may include an HDL, an RTL, a GL  
15 description, a mask level description, other hardware description, or any combination thereof.

In embodiments where the machine executable code 706 includes a hardware description (at any level of abstraction), a system (not shown, but including the storage 704) may be configured to implement the hardware description described by  
20 the machine executable code 706. By way of non-limiting example, the processors 702 may include a programmable logic device (e.g., an FPGA or a PLC) and the logic circuitry 708 may be electrically controlled to implement circuitry corresponding to the hardware description into the logic circuitry 708. Also by way of non-limiting example, the logic circuitry 708 may include hard-wired logic manufactured by a  
25 manufacturing system (not shown, but including the storage 704) according to the hardware description of the machine executable code 706.

Regardless of whether the machine executable code 706 includes computer-readable instructions or a hardware description, the logic circuitry 708 is adapted to perform the functional elements described by the machine executable code 706 when  
30 implementing the functional elements of the machine executable code 706. It is noted that although a hardware description may not directly describe functional elements, a hardware description indirectly describes functional elements that the hardware elements described by the hardware description are capable of performing.

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Terms used in the present disclosure and especially in the appended claims (e.g., bodies of the appended claims) are generally intended as “open” terms (e.g., the term “including” should be interpreted as “including, but not limited to,” the term “having” should be interpreted as “having at least,” the term “includes” should be  
5 interpreted as “includes, but is not limited to”).

Additionally, if a specific number of an introduced claim recitation is intended, such an intent will be explicitly recited in the claim, and in the absence of such recitation no such intent is present. For example, as an aid to understanding, the following appended claims may contain usage of the introductory phrases “at least  
10 one” and “one or more” to introduce claim recitations. However, the use of such phrases should not be construed to imply that the introduction of a claim recitation by the indefinite articles “a” or “an” limits any particular claim containing such introduced claim recitation to embodiments containing only one such recitation, even when the same claim includes the introductory phrases “one or more” or “at least one”  
15 and indefinite articles such as “a” or “an” (e.g., “a” and/or “an” should be interpreted to mean “at least one” or “one or more”); the same holds true for the use of definite articles used to introduce claim recitations.

In addition, even if a specific number of an introduced claim recitation is explicitly recited, those skilled in the art will recognize that such recitation should be  
20 interpreted to mean at least the recited number (e.g., the bare recitation of “two recitations,” without other modifiers, means at least two recitations, or two or more recitations). Furthermore, in those instances where a convention analogous to “at least one of A, B, and C, etc.” or “one or more of A, B, and C, etc.” is used, in general such a construction is intended to include A alone, B alone, C alone, A and B together, A  
25 and C together, B and C together, or A, B, and C together.

Further, any disjunctive word or phrase presenting two or more alternative terms, whether in the description, claims, or drawings, should be understood to contemplate the possibilities of including one of the terms, either of the terms, or both terms. For example, the phrase “A or B” should be understood to include the  
30 possibilities of “A” or “B” or “A and B.”

Additional non-limiting embodiments of the disclosure may include:

Embodiment 1: A general purpose input of a microcontroller, the general purpose input comprising: an input pin pad configured for operative coupling to a

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device external to a microcontroller; and a circuitry arranged to selectively disable static current draw at the general purpose input.

Embodiment 2: The general purpose input according to Embodiment 1, further comprising: a supply pin pad configured for operative coupling to a voltage supply of the microcontroller.

Embodiment 3: The general purpose input according to any of Embodiments 1 and 2, wherein the voltage supply of the microcontroller is an external voltage supply.

Embodiment 4: The general purpose input according to any of Embodiments 1 through 3, wherein the circuitry arranged to selectively disable static current draw at the general purpose input is configured to disable static current draw when an input voltage at the input pin pad is lower than a supply voltage of the voltage supply of the microcontroller.

Embodiment 5: The general purpose input according to any of Embodiments 1 through 4, wherein the voltage supply is for a logic circuitry of the microcontroller.

Embodiment 6: The general purpose input according to any of Embodiments 1 through 5, further comprising an on-board voltage regulator, the on-board voltage regulator comprising: an input, the input operatively coupled to the supply pin pad; and an output, the output operatively coupled to the circuitry arranged to selectively disable static current draw.

Embodiment 7: The general purpose input according to any of Embodiments 1 through 6, wherein the circuitry arranged to selectively disable static current draw at the general purpose input is configured to disable static current draw responsive to control signals.

Embodiment 8: A microcontroller, comprising: one or more general purpose inputs; and a first selectable input buffers of a first general purpose input of the one or more general purpose inputs, wherein a first input buffer of the first selectable input buffers is selectable to disable static current draw at the first general purpose input when an input voltage at the first general purpose input is less than a supply voltage.

Embodiment 9: The microcontroller according to Embodiment 8, further comprising a second input buffer of the first selectable input buffers of the first general purpose input.

Embodiment 10: The microcontroller according to any of Embodiments 8 and 9, further comprising: a control logic of the first general purpose input, the control

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logic configured to provide control signals for enabling one of the first input buffer and the second input buffer.

Embodiment 11: The microcontroller according to any of Embodiments 8 through 10, further comprising: a control register operatively coupled to respective  
5 enable inputs of the first input buffer and the second input buffer.

Embodiment 12: The microcontroller according to any of Embodiments 8 through 11, further comprising: a first voltage shifter arranged on an enable input path of the second input buffer; and a second voltage shifter arranged on an output path of the second input buffer.

10 Embodiment 13: The microcontroller according to any of Embodiments 8 through 12, wherein the first voltage shifter is arranged to adjust a control signal to a voltage level of the second input buffer, and the second voltage shifter is arranged to adjust an output signal of the second input buffer to the logic voltage level.

Embodiment 14: The microcontroller according to any of Embodiments 8  
15 through 13, further comprising: a voltage regulator of the first general purpose input, wherein an input of the voltage regulator is operatively coupled to a supply pin pad and an output of the voltage regulator is operatively coupled to the first input buffer.

Embodiment 15: The microcontroller according to any of Embodiments 8 through 14, wherein the voltage regulator is configured to receive the supply voltage  
20 and provide a regulated supply voltage responsive to the supply voltage.

Embodiment 16: The microcontroller according to any of Embodiments 8 through 15, wherein the voltage regulator is configured to continuously generate and provide the regulated supply voltage during a lowest voltage mode.

Embodiment 17: The microcontroller according to any of Embodiments 8  
25 through 16, wherein the voltage regulator is configured to generate the regulated supply voltage within a device threshold voltage of a lowest specified input voltage.

Embodiment 18: The microcontroller according to any of Embodiments 8 through 17, wherein the voltage regulator is an on-board voltage regulator.

Embodiment 19: A microcontroller, comprising: a first supply pin pad; a  
30 second supply pin pad; and a general purpose input, the general purpose input comprising: a first input buffer operatively coupled to the first supply pin pad; a second input buffer operatively coupled to the second supply pin pad; a third input buffer operatively coupled to a voltage regulator; and a mapped control register,

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wherein enable inputs of the first, second, and third input buffers are operatively coupled to the mapped control register.

Embodiment 20: The microcontroller according to Embodiment 19, wherein the general purpose input comprises an input pin pad, the input pin pad operatively  
5 coupled to the first input buffer, the second input buffer and the third input buffer.

Embodiment 21: A method, comprising: receiving a supply voltage, providing the supply voltage to first selectable input buffers of a first general purpose input; generating a regulated supply voltage responsive to the supply voltage; providing the regulated supply voltage to a first input buffer of the first selectable input buffers;  
10 providing the supply voltage to a second input buffer of the first selectable input buffers; and selecting the first input buffer and thereby selectively disable static current draw at the first general purpose input when an input voltage at the first general purpose inputs is less than the supply voltage.

While the present disclosure has been described herein with respect to certain  
15 illustrated embodiments, those of ordinary skill in the art will recognize and appreciate that the present disclosure is not so limited. Rather, many additions, deletions, and modifications to the illustrated and described embodiments may be made without departing from the scope of the invention as hereinafter claimed along with their legal equivalents. In addition, features from one or more embodiments may be combined  
20 with features of one or more other embodiments while still being encompassed within the scope of the disclosure as contemplated by the inventors.

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## CLAIMS

We claim:

- 5           1.       A general purpose input of a microcontroller, the general purpose input comprising:  
              an input pin pad configured for operative coupling to a device external to a microcontroller; and  
              a circuitry arranged to selectively disable static current draw at the general  
10       purpose input.
2.       The general purpose input of claim 1, further comprising:  
              a supply pin pad configured for operative coupling to a voltage supply of the microcontroller.  
15
3.       The general purpose input of claim 2, wherein the voltage supply of the microcontroller is an external voltage supply.
4.       The general purpose input of claim 2, wherein the circuitry arranged to  
20       selectively disable static current draw at the general purpose input is configured to disable static current draw when an input voltage at the input pin pad is lower than a supply voltage of the voltage supply of the microcontroller.
5.       The general purpose input of claim 2, further comprising an on-board  
25       voltage regulator, the on-board voltage regulator comprising:  
              an input, the input operatively coupled to the supply pin pad; and  
              an output, the output operatively coupled to the circuitry arranged to selectively disable static current draw.
- 30           6.       The general purpose input of claim 1, wherein the circuitry arranged to selectively disable static current draw at the general purpose input is configured to disable static current draw responsive to control signals.

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7. A microcontroller, comprising:  
one or more general purpose inputs; and  
a first selectable input buffers of a first general purpose input of the one or  
more general purpose inputs, wherein a first input buffer of the first selectable input  
5 buffers is selectable to disable static current draw at the first general purpose input  
when an input voltage at the first general purpose input is less than a supply voltage.
8. The microcontroller of claim 7, further comprising a second input buffer  
of the first selectable input buffers of the first general purpose input.
- 10 9. The microcontroller of claim 8, further comprising:  
a control logic of the first general purpose input, the control logic configured to  
provide control signals for enabling one of the first input buffer and the second input  
buffer.
- 15 10. The microcontroller of claim 9, further comprising:  
a control register operatively coupled to respective enable inputs of the first  
input buffer and the second input buffer.
- 20 11. The microcontroller of claim 8, further comprising:  
a first voltage shifter arranged on an enable input path of the second input  
buffer; and  
a second voltage shifter arranged on an output path of the second input buffer.
- 25 12. The microcontroller of claim 11, wherein the first voltage shifter is  
arranged to adjust a control signal to a voltage level of the second input buffer, and the  
second voltage shifter is arranged to adjust an output signal of the second input buffer  
to a logic voltage level.
- 30 13. The microcontroller of claim 8, further comprising:  
a voltage regulator of the first general purpose input, wherein an input of the  
voltage regulator is operatively coupled to a supply pin pad and an output of the  
voltage regulator is operatively coupled to the first input buffer.

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14. The microcontroller of claim 13, wherein the voltage regulator is arranged to receive the supply voltage and provide a regulated supply voltage responsive to the supply voltage.

5

15. The microcontroller of claim 14, wherein the voltage regulator is configured to continuously generate and provide the regulated supply voltage during a lowest voltage mode.

10

16. The microcontroller of claim 14, wherein the voltage regulator is configured to generate the regulated supply voltage within a device threshold voltage of a lowest specified input voltage.

15

17. The microcontroller of claim 14, wherein the voltage regulator is an on-board voltage regulator.

20

18. A microcontroller, comprising:

a first supply pin pad;

a second supply pin pad; and

a general purpose input, the general purpose input comprising:

a first input buffer operatively coupled to the first supply pin pad;

a second input buffer operatively coupled to the second supply pin pad;

a third input buffer operatively coupled to a voltage regulator; and

a mapped control register, and

25

wherein enable inputs of the first, second, and third input buffers are operatively coupled to the mapped control register.

30

19. The microcontroller of claim 18, wherein the general purpose input comprises an input pin pad, the input pin pad operatively coupled to the first input buffer, the second input buffer and the third input buffer.

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20. A method, comprising:
- receiving a supply voltage;
  - generating a regulated supply voltage responsive to the supply voltage;
  - providing the regulated supply voltage to a first input buffer of a first selectable
  - 5 input buffer;
  - providing the supply voltage to a second input buffer of the first selectable
  - input buffer; and
  - selecting the first input buffer and thereby selectively disable static current
  - draw at a first general purpose input when an input voltage at the first general purpose
  - 10 input is less than the supply voltage.

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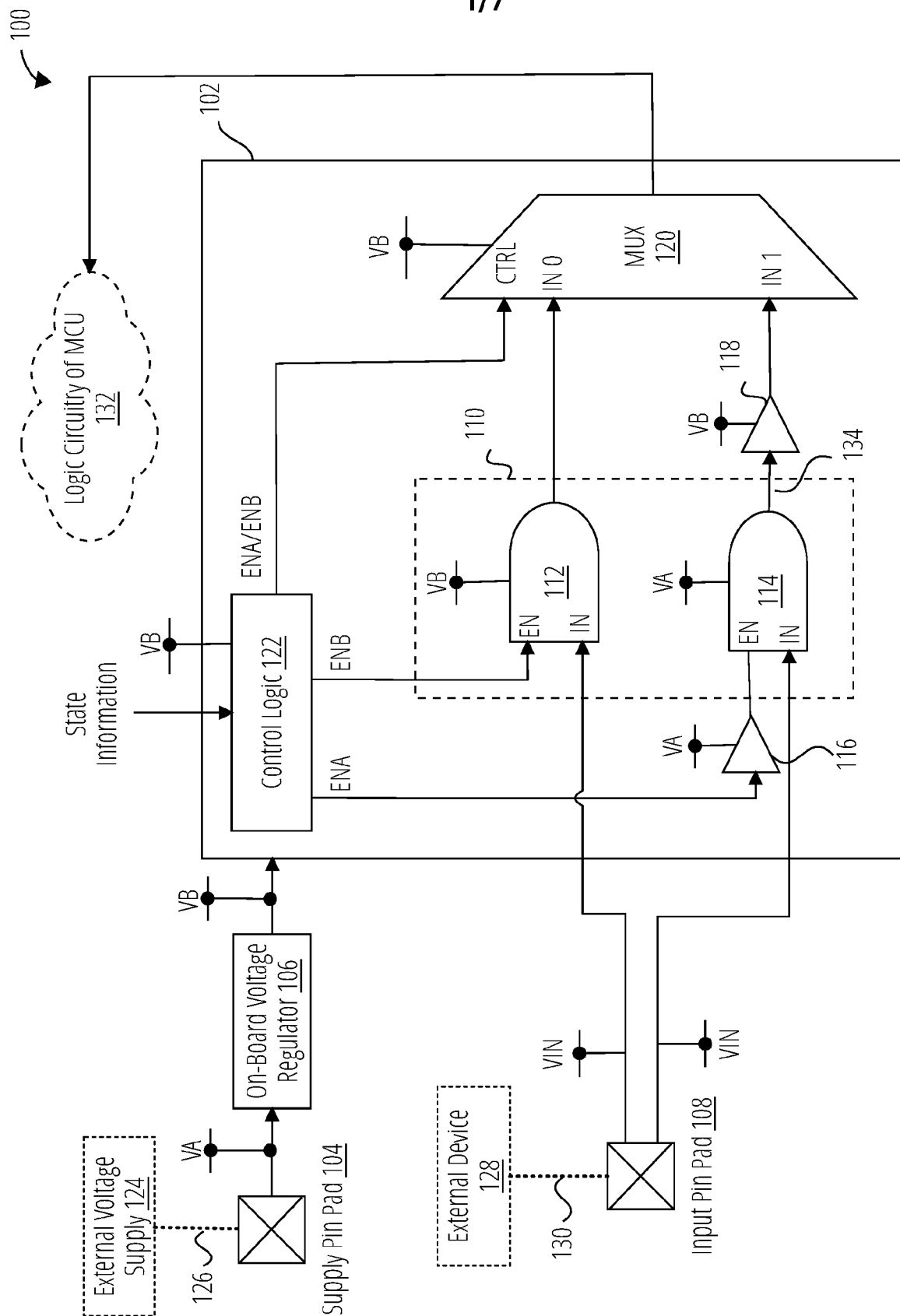


FIG. 1

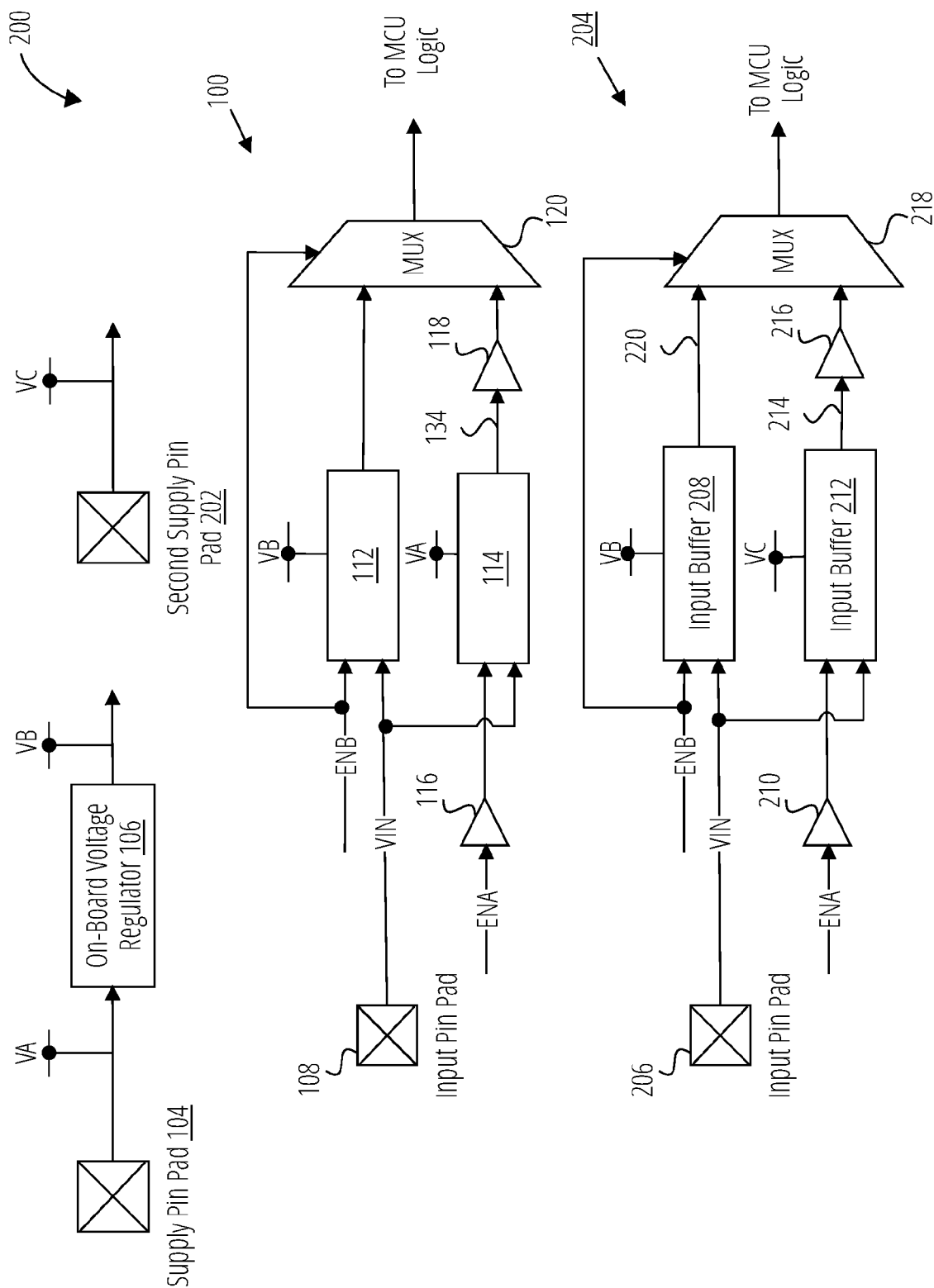


FIG. 2

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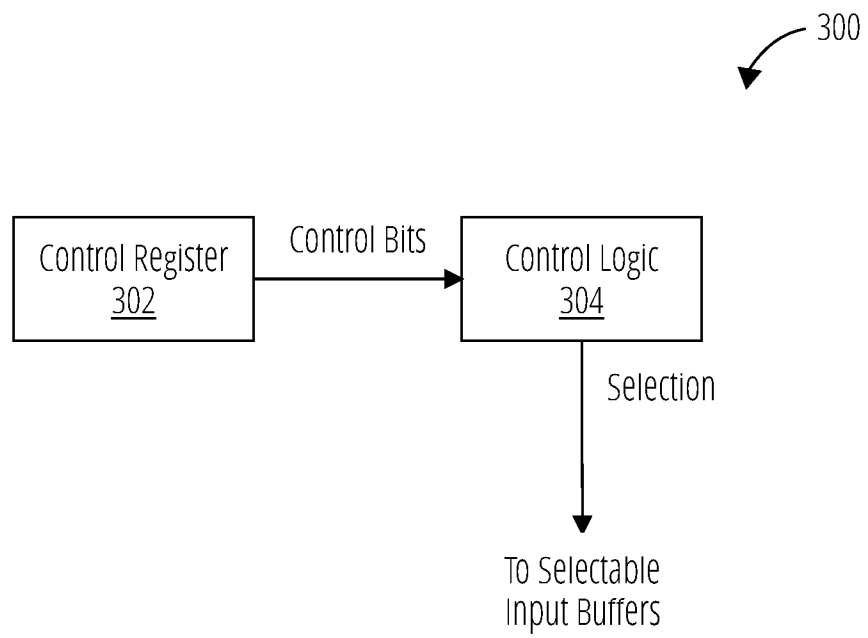


FIG. 3

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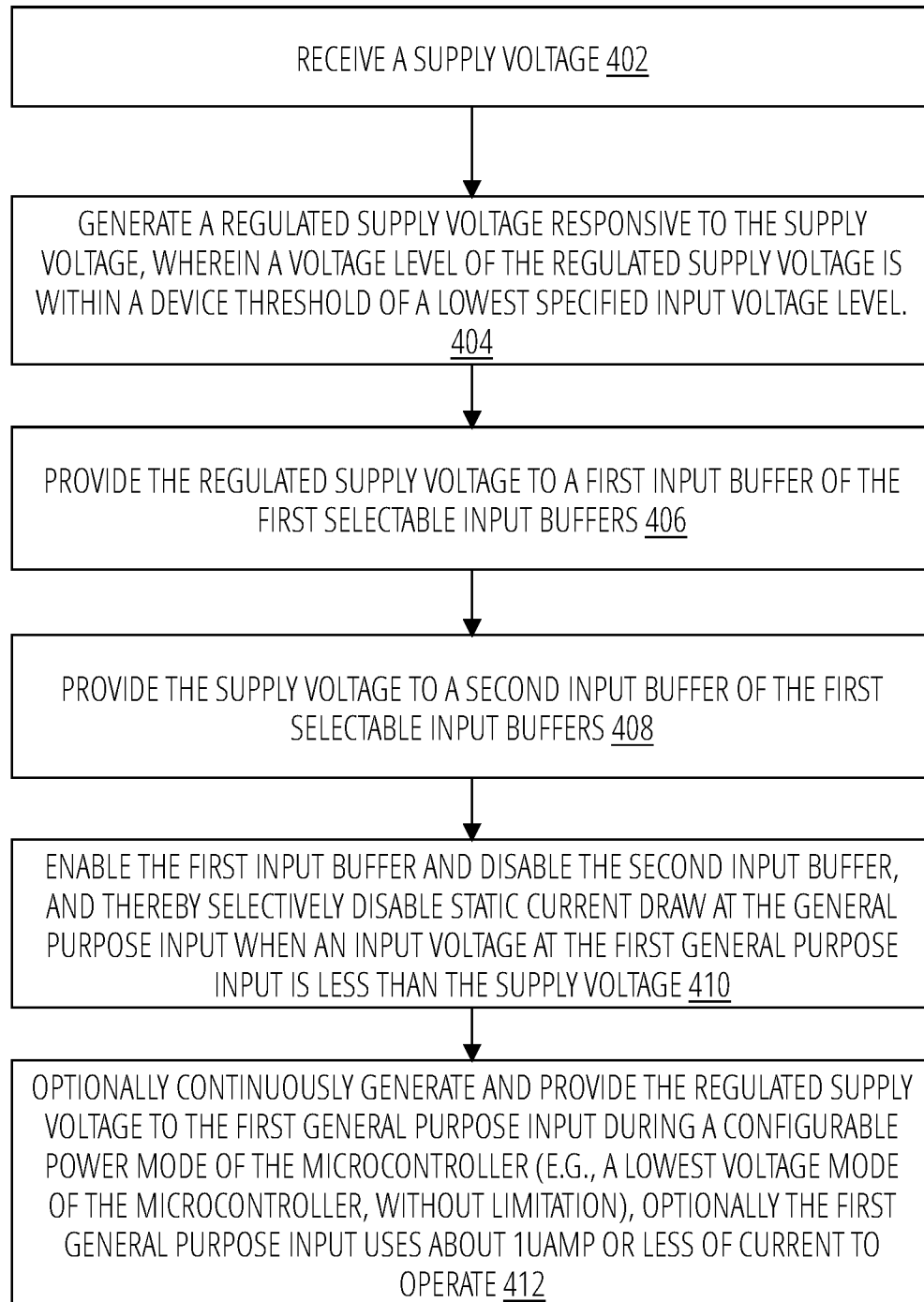


FIG. 4

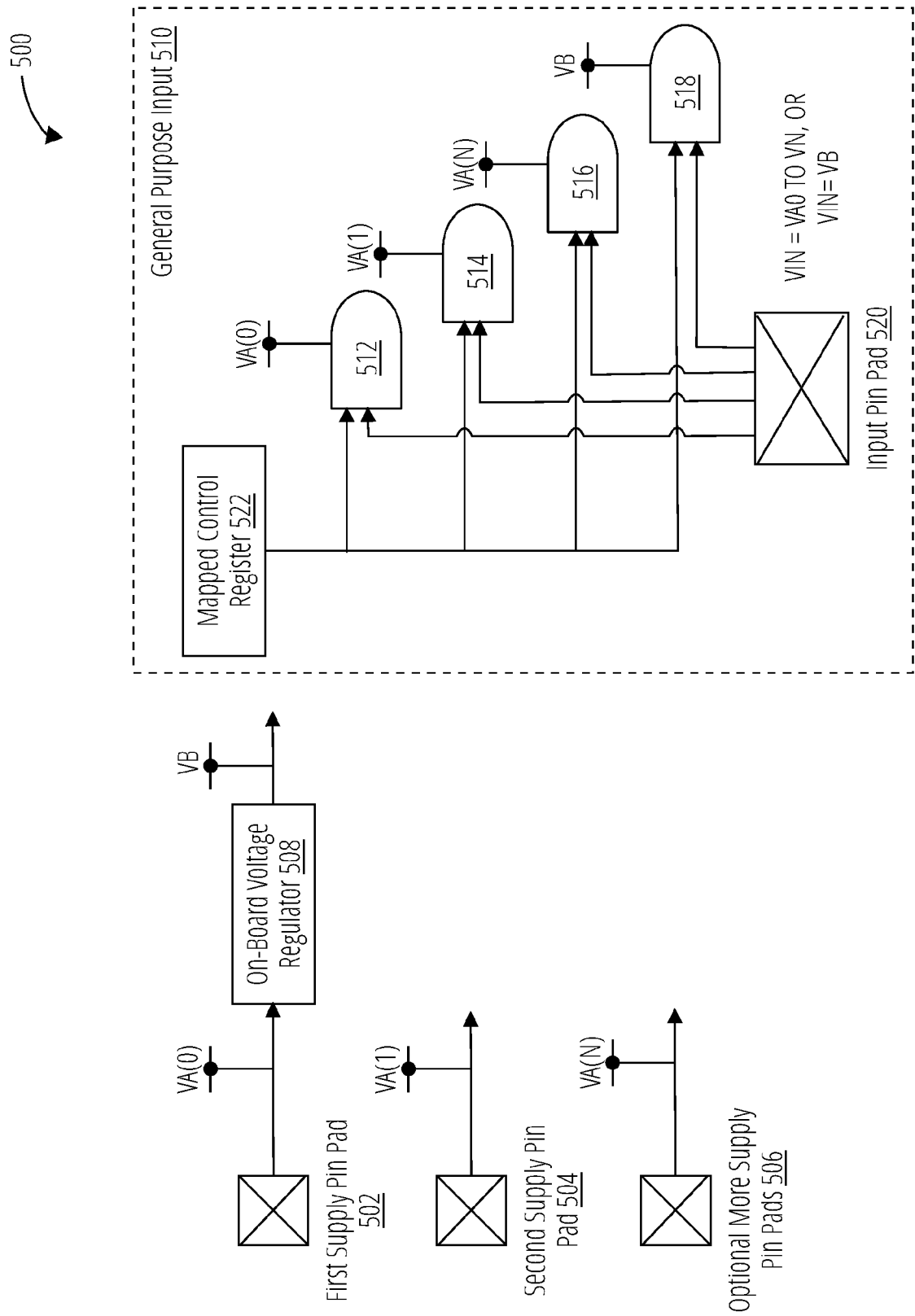


FIG. 5

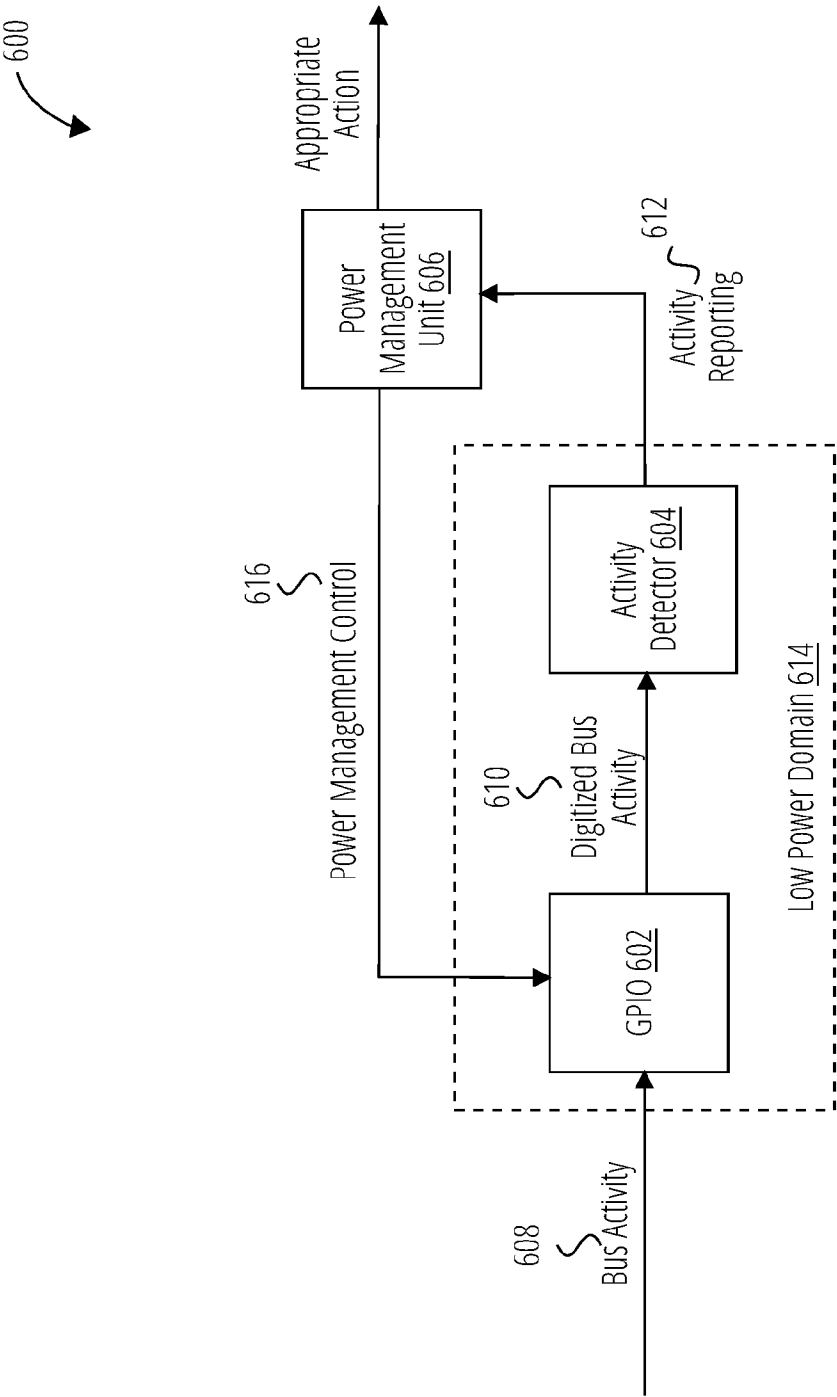


FIG. 6

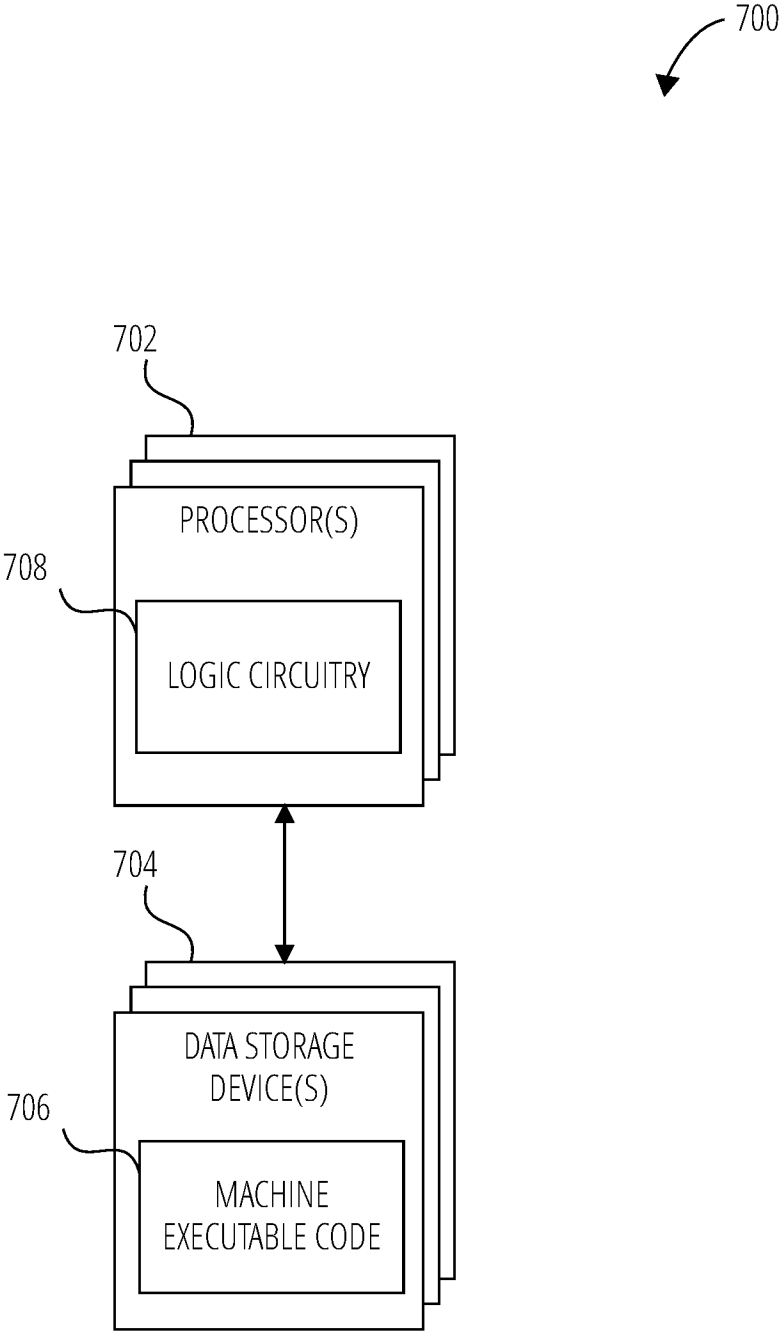


FIG. 7

## INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2020/070173

## A. CLASSIFICATION OF SUBJECT MATTER

INV. G06F1/3203 G06F1/3234 G06F1/3287  
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                         | Relevant to claim No. |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 6 323 704 B1 (PELLEY PERRY H [US] ET AL) 27 November 2001 (2001-11-27)<br>abstract; claims 1-9; figures 1-5<br>column 1, line 11 - line 33<br>column 2, line 8 - line 49<br>column 5, line 9 - line 11<br>column 6, line 9 - column 7, line 29<br>----- | 1-20                  |
| X         | US 2009/206875 A1 (TRAN HUAN HUU [US] ET AL) 20 August 2009 (2009-08-20)<br>abstract; figures 1A,1B,2,4,5-7<br>paragraph [0015] - paragraph [0019]<br>paragraphs [0042], [0052]<br>-----                                                                   | 18,19                 |
| A         | -/--                                                                                                                                                                                                                                                       | 1-17,20               |



Further documents are listed in the continuation of Box C.



See patent family annex.

## \* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search

18 September 2020

Date of mailing of the international search report

02/10/2020

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International application No  
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| C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT |                                                                                                                                                                                                                                           |                       |
|------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Category*                                            | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                        | Relevant to claim No. |
| A                                                    | EP 3 115 869 A1 (NXP BV [NL])<br>11 January 2017 (2017-01-11)<br>abstract; figures 1-8<br>paragraphs [0032], [0033], [0038]<br>paragraph [0052] - paragraph [0064]<br>-----                                                               | 1-20                  |
| A                                                    | US 2014/002162 A1 (WESTWICK ALAN [US])<br>2 January 2014 (2014-01-02)<br>abstract; claims 1-20; figures 1-5<br>paragraph [0005] - paragraph [0007]<br>paragraph [0017] - paragraph [0019]<br>paragraph [0029] - paragraph [0054]<br>----- | 1-20                  |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2020/070173

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s) | Publication<br>date         |
|-------------------------------------------|---------------------|----------------------------|-----------------------------|
| US 6323704                                | B1                  | 27-11-2001                 | NONE                        |
| -----                                     |                     |                            |                             |
| US 2009206875                             | A1                  | 20-08-2009                 | NONE                        |
| -----                                     |                     |                            |                             |
| EP 3115869                                | A1                  | 11-01-2017                 | CN 106341117 A 18-01-2017   |
|                                           |                     |                            | EP 3115869 A1 11-01-2017    |
|                                           |                     |                            | US 2017012627 A1 12-01-2017 |
| -----                                     |                     |                            |                             |
| US 2014002162                             | A1                  | 02-01-2014                 | NONE                        |
| -----                                     |                     |                            |                             |