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(71) Applicant (for all designated States except US): **AUCKLAND UNISERVICES LIMITED** [NZ/NZ]; Level 10, 70 Symonds Street, Auckland, (NZ).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **CHEN, Fei** [CN/NZ]; The University of Auckland, Department of Electrical and Computer Engineering, 38 Princess Street, Auckland (NZ). **SALCIC, Zoran** [NZ/NZ]; 22 Hororata Road, 0622 Takapuna, (NZ). **GAO, Wei** [NZ/NZ]; 131 Porritt Avenue, Birkenhead, Auckland (NZ).

(74) Agent: **SHELSTON IP**; 60 Margaret Street, Sydney NSW 2000 (AU).

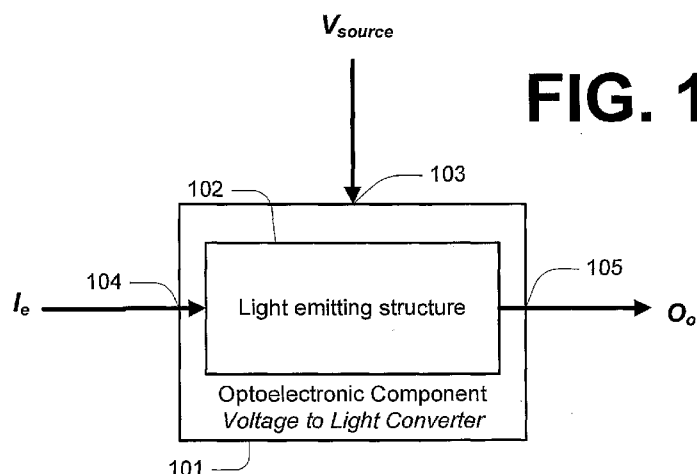
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(57) Abstract: An optoelectronic component comprising a light emitting structure that is configured to generate light in response to a voltage signal within a predetermined range, the predetermined range having a lower limit and upper limit; a primary input for receiving a source voltage signal that is applied to the light emitting structure; at least one secondary input for receiving an input signal and, in response to the input signal, providing a control voltage signal that is applied to the light emitting structure; and an output for providing an optical output signal on the basis of light generated by the light emitting structure, such that where the source voltage signal and control voltage signal combine to provide an overall voltage signal within the predetermined range, the light emitting structure generates light for driving the optical output signal. Additionally optical/electrical hybrid processors and methods for signal processing.



OPTOELECTRONIC COMPONENTS

TECHNICAL FIELD

The invention relates to optoelectronic components, and particularly to
5 optoelectronic components that comprise light emitting structures, and to the methods
for the preparation of such components, and to their uses. Embodiments have been
developed to provide optoelectronic components that output a light signal in response to
predefined inputs, which may be optical and/or electrical, with such components
comprising the likes of voltage to light converters, optoelectronic switches, and
10 optoelectronic logic elements.

BACKGROUND

Silicon (Si) is the backbone of the modern computer industry. The power and
size of computers has improved exponentially every year from the 1960's primarily as a
15 result of reducing the size of integrated circuits. Moore's law states that the number of
transistors that can be placed on an integrated circuit doubles every year. Such a
situation is subject to certain physical constraints and cannot continue indefinitely. In
fact, conventional computer circuitry is fast approaching the limits of Moore's law.
The conducting paths in modern circuits are now about 45 nm with the absolute
20 physical limit predicted to be around 10 or 11 nm. Realising the full extent and power
of very large scale integration is also currently not possible since there are considerable
interconnect bottlenecks in current chips.

Continuing increases in power and decrease in size are thus unlikely to continue
beyond the near future if current technologies alone are used. Scientists the world over
25 are looking for new ways to continue the advancement of computer technology and
enable such applications as, for example, real-time natural language translation,
automatic facial recognition or intelligent automatic chauffeuring involving
communication with a vehicle using voice and vision systems.

Photonic computing, that is computing using light to transmit signals between
30 integrated circuits, is believed to be a promising direction for providing increases in
computer speed and power. Because photonic computing is based upon photons, rather
than electrons, it has certain inherent advantages – in particular, photons move much
faster than electrons, and have inherently higher bandwidths (data carrying capacities).

In order to implement photonic computing, it is necessary to achieve light emission from Si based integrated circuits. Current light emitting devices are mainly made from III-V semiconductor compounds such as GaAs, GaN, GaP, InP, InAs, InGaAs, InGaAsP and the like. These light emitting compounds are, however, difficult to integrate into Si chips.

The concept of Si based light emission or light modulation is not new, but it has previously proved very difficult to achieve in a simple, reliable and robust way. Some approaches have been complicated, for example involving anti-crossing between coupled Si rings in light generation applications, and even that approach has not produced entirely satisfactory results. Recent advances, however, have lead to some particularly advantageous light emitting structures, such as those described in United States Patent Application No. 61/034883.

Identifying an appropriate solution to the problems associated with Si based light emission is only one step towards the more substantive goal of implementing optoelectronic computing. In particular, although it may be possible to generate light in response to the application of an electronic field, extending that technology so as to provide for meaningful information processing functionalities presents significant challenges.

Accordingly, it is an object of the present invention to overcome or ameliorate at least one of the disadvantages of the prior art, or to provide a useful alternative.

Any discussion of the prior art throughout the specification should in no way be considered as an admission that such prior art is widely known or forms part of common general knowledge in the field.

SUMMARY OF THE INVENTION

One embodiment of the invention provides an optoelectronic component comprising:

a light emitting structure that is configured to generate light in response to a voltage signal within a predetermined range, the predetermined range having a lower limit and upper limit;

a primary input for receiving a source voltage signal that is applied to the light emitting structure;

at least one secondary input for receiving an input signal and, in response to the input signal, providing a control voltage signal that is applied to the light emitting structure; and

an output for providing an optical output signal on the basis of light generated by the light emitting structure, such that where the source voltage signal and control voltage signal combine to provide an overall voltage signal within the predetermined range, the light emitting structure generates light for driving the optical output signal.

One embodiment of the invention provides an optoelectronic component comprising a secondary input in that is responsive to an optical input signal for providing the control voltage signal.

One embodiment of the invention provides an optoelectronic component comprising a secondary input that is responsive to an electrical input signal for providing the control voltage signal.

One embodiment of the invention provides an optoelectronic component comprising:

a first secondary input that is responsive to an optical input signal for providing a first control voltage signal; and

a secondary input that is responsive to an electrical input signal for providing a second control voltage signal.

One embodiment of the invention provides an optoelectronic component wherein the secondary input comprises a photoresistor that is responsive to the optical input signal for providing the control voltage signal.

One embodiment of the invention provides an optoelectronic component wherein the photoresistor is serially connected to the light emitting structure, such that the source voltage signal applies a potential difference proportionally between the light emitting structure and the photoresistor in accordance with their relative electrical resistances.

One embodiment of the invention provides an optoelectronic component wherein the photoresistor provides the voltage control signal by reducing its electrical resistance in response to the optical input signal, thereby to increase the proportion of the potential difference that is applied to the light emitting structure.

One embodiment of the invention provides an optoelectronic component comprising:

a light emitting structure that is configured to generate light in response to a voltage signal within a predetermined range, the predetermined range having a lower limit and upper limit;

5 a primary input for receiving a source voltage signal that is applied to the light emitting structure;

a secondary input for receiving an optical input signal and, in response to the optical input signal, varying the overall voltage applied to the light emitting structure; and

10 an output for providing an optical output signal on the basis of light generated by the light emitting structure, such that the component is operable in a first state wherein the optical output signal is provided, and a second state wherein the optical output signal is provided.

One embodiment of the invention provides an optoelectronic component wherein the secondary input comprises a photoresistor.

15 One embodiment of the invention provides an optoelectronic component comprising:

a light emitting structure that is configured to generate light in response to a voltage signal within a predetermined range, the predetermined range having a lower limit and upper limit;

20 a primary input for receiving a source voltage signal that is applied to the light emitting structure;

a secondary input for receiving an optical input signal and, in response to the optical input signal, varying the overall voltage applied to the light emitting structure;

25 a tertiary input for receiving an electrical input signal and, in response to the electrical input signal, varying the overall voltage applied to the light emitting structure; and

an output for providing an optical output signal on the basis of light generated by the light emitting structure, such that the component is operable in:

30 a first state wherein neither the optical input signal nor the electrical input signal is received, and the optical output signal is not provided;

a second state wherein one of the optical input signal and the electrical input signal is received, and the optical output signal is provided; and

a third state wherein both the optical input signal and the electrical input signal is received, and the optical output signal is not provided.

One embodiment of the invention provides an optoelectronic component comprising two or more optoelectronic logic elements as discussed above.

5 One embodiment of the invention provides an optoelectronic component wherein the respective outputs of two or more optoelectronic logic elements according to as discussed above are combined to provide an optical input signal for a further optoelectronic logic element as discussed above.

10 One embodiment of the invention provides an optoelectronic component wherein the light emitting structure configured to generate no light in response to a voltage signal within a first further predetermined range adjacent and below the lower limit and a second further predetermined range adjacent and above the upper limit.

15 One embodiment of the invention provides an optoelectronic component wherein the light emitting structure configured to generate an intensity of light below a predefined threshold intensity in response to a voltage signal within a first further predetermined range adjacent and below the lower limit and a second further predetermined range adjacent and above the upper limit.

20 One embodiment of the invention provides an optoelectronic component wherein the light emitting structure configured to generate substantially no light in response to a voltage signal within a first further predetermined range adjacent and below the lower limit and a second further predetermined range adjacent and above the upper limit.

25 One embodiment of the invention provides an optoelectronic component wherein the light generated by the light emitting structure in response to the voltage signal within the predetermined range is of greater than a predefined threshold intensity level.

One embodiment of the invention provides an optoelectronic component wherein the light emitting structure is silicon based.

30 One embodiment of the invention provides an optoelectronic component wherein the light emitting structure displays at least one current peak on an I-V curve, wherein the peak corresponds to the predetermined voltage.

One embodiment of the invention provides an optoelectronic component wherein the light emitting structure displays multiple current peaks on an I-V curve.

One embodiment of the invention provides an optoelectronic component wherein the light emitting structure comprises a hot electron source and a layer of optoelectronic material disposed thereon.

One embodiment of the invention provides an optoelectronic component
5 wherein the light emitting structure comprises a hot electron source; a layer of optoelectronic material disposed on the hot electron source; and p-type material disposed on the optoelectronic material.

One embodiment of the invention provides an optoelectronic component wherein the light emitting structure comprises a single crystal silicon substrate, a
10 polycrystalline silicon layer disposed thereon; and an uppermost layer of silicon oxide.

One embodiment of the invention provides an optoelectronic component wherein the light emitting structure comprises a single crystal silicon substrate having an aluminium or magnesium layer disposed thereon, with a corresponding uppermost layer of aluminium oxide or magnesium oxide.

15 One embodiment of the invention provides an optoelectronic component wherein the light emitting structure comprises a hot electron source and a zinc oxide layer disposed thereon.

One embodiment of the invention provides an optoelectronic component or light emitting structure wherein the light emitting structure comprises a hot electron source, a
20 zinc oxide layer disposed thereon; and an indium tin oxide (ITO) layer or a gold (Au) layer or a gold (Au) grating layer disposed on the zinc oxide layer. Additionally or alternatively, other layers of suitable materials may be applied in the form of a grating or other pattern.

One embodiment of the invention provides an optoelectronic component
25 wherein the light emitting structure comprises, in order, the following layers:
a polycrystalline silicon layer;
a silicon dioxide layer; and
a zinc oxide layer.

One embodiment of the invention provides an optoelectronic component
30 wherein the light emitting structure comprises, in order, the following layers:
a polycrystalline silicon layer;
a silicon dioxide layer;
a zinc oxide layer; and

an indium tin oxide (ITO) layer.

One embodiment of the invention provides an optoelectronic component wherein the light emitting structure comprises, in order, the following layers:

a polycrystalline silicon layer;
5 a silicon dioxide layer;
a zinc oxide layer; and
a gold (Au) layer.

One embodiment of the invention provides an optoelectronic component wherein the light emitting structure comprises, in order, the following layers:

10 a polycrystalline silicon layer;
a silicon dioxide layer;
a zinc oxide layer; and
a gold (Au) grating layer.

One embodiment of the invention provides an optoelectronic component wherein the light emitting structure comprises, in order, the following layers:

15 a single crystal silicon substrate;
a polycrystalline silicon layer;
a silicon dioxide layer; and
a zinc oxide layer.

20 One preferred embodiment of the invention provides an optoelectronic component wherein the light emitting structure comprises, in order, the following layers:

a single crystal silicon substrate;
a heavy doped polycrystalline silicon layer;
25 a silicon dioxide layer formed by wet oxidation of a surface of the polycrystalline silicon layer; and
a zinc oxide layer.

One embodiment of the invention provides an optoelectronic component wherein the light emitting structure comprises, in order, the following layers:

30 a single crystal silicon substrate;
polycrystalline silicon layer;
a silicon dioxide layer;
a zinc oxide layer; and

an indium tin oxide (ITO) layer.

One embodiment of the invention provides an optoelectronic component wherein the single crystal silicon substrate and the polycrystalline silicon layer are doped such that they are either n-type or p-type doped.

5 One embodiment of the invention provides an optoelectronic component wherein the single crystal silicon substrate and the polycrystalline silicon layer are heavy doped.

One embodiment of the invention provides an optoelectronic component wherein the single crystal silicon substrate and the polysilicon layer are both heavy
10 doped to be n-type silicon.

One embodiment of the invention provides an optoelectronic component wherein the single crystal silicon substrate and the polysilicon layer are both heavy doped to be or p-type silicon.

One embodiment of the invention provides a computing device which comprises
15 an optoelectronic component according as discussed above.

One embodiment of the invention provides an integrated circuit which comprises an optoelectronic component as discussed above.

One embodiment of the invention provides a method for signal processing including the steps of:

20 (a) providing light emitting structure that is configured to generate light in response to a voltage signal within a predetermined range;

(b) applying a source voltage across the light emitting structure;

(c) selectively applying a control voltage across the light emitting structure;

(d) receiving an optical input signal at a photoresistor coupled to the light
25 emitting structure thereby to vary the overall voltage applied across light emitting structure; and

(e) observing an output of the light emitting structure, wherein the output is dependent on the presence/absence of the control voltage signal and the optical input signal.

30 One embodiment of the invention provides an optical/electrical hybrid processor comprising:

one or more electrical processors, wherein each electrical process is coupled to a VLC array for converting electrical output signals from the electrical processors to an optical output signals;

an optical processor comprising an array of optical logic elements, wherein the
5 an optical processor is coupled to the VLC arrays for receiving the optical output signals and processing those thereby to provide further optical output signals; and

a photo-detector array for converting the further optical output signals to electrical signals.

One embodiment of the invention provides an optical/electrical hybrid processor
10 comprising:

one or more electrical processors coupled an optical processor, wherein the optical processor receives and processes optical signals that are propagated responsive to electrical signals emitted by the electrical processors.

As used herein, unless otherwise specified the use of the ordinal adjectives
15 "first", "second", "third", etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

In the claims below and the description herein, any one of the terms
20 "comprising", "comprised of", or "which comprises" is an open term that means including at least the elements/features that follow, but not excluding others. Thus, the term "comprising", when used in the claims, should not be interpreted as being limitative to the means or elements or steps listed thereafter. For example, the scope of the expression a device comprising A and B should not be limited to devices consisting
25 only of elements A and B. Any one of the terms "including", "which includes" or "that includes" as used herein is also an open term that also means including at least the elements/features that follow the term, but not excluding others. Thus, "including" is synonymous with and means the same as "comprising".

30 BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 schematically illustrates an optoelectronic component according to one embodiment of the present invention, in the form of a voltage to light converter.

FIG. 2 schematically illustrates a light emitting structure suitable for use in one embodiment of the present invention, shown in conjunction with a source of voltage.

FIG. 3 is a graph of voltage against current for a light emitting structure suitable for use in one embodiment of the present invention, showing light emitting and non-
5 light emitting regions.

FIG. 4 schematically illustrates states for a light emitting structure suitable for use in one embodiment of the present invention.

FIG. 5 illustrates the behaviour of voltage to light converter in time domain where input voltage is changed in four distinctive levels.

10 FIG. 6A schematically illustrates an optoelectronic component according to one embodiment of the present invention, in the form of an optoelectronic switch.

FIG. 6B provides an alternate representation of the optoelectronic switch of FIG. 6A.

15 FIG. 7A schematically illustrates an optoelectronic component according to one embodiment of the present invention, in the form of an optoelectronic logic element.

FIG. 7B provides an alternate representation of the optoelectronic logic element of FIG. 6A.

20 FIG. 8 schematically illustrates an optoelectronic logic element, according to one embodiment of the present invention, configured to function as a logical PASS gate.

FIG. 9 schematically illustrates an optoelectronic logic element, according to one embodiment of the present invention, configured to function as a logical NOT gate.

FIG. 10 schematically illustrates an optical combiner that is used in conjunction with optoelectronic components according to embodiments of the present intention.

25 FIG. 11 schematically illustrates an optoelectronic logic element, according to one embodiment of the present invention, configured to function as a logical AND gate.

FIG. 12 schematically illustrates an optoelectronic logic element, according to one embodiment of the present invention, configured to function as a logical OR gate.

30 FIG. 13A schematically illustrates a process for fabrication an optoelectronic element according to one embodiment.

FIG. 13B schematically illustrates a process for fabrication an optoelectronic element according to one embodiment.

FIG. 13C schematically illustrates a process for fabrication an optoelectronic element according to one embodiment.

FIG. 13D schematically illustrates a process for fabrication an optoelectronic element according to one embodiment.

5 FIG. 14A schematically illustrates an optoelectronic element according to one embodiment, shown as a side view.

FIG. 14B schematically illustrates the optoelectronic element of FIG. 14A, shown as a top view.

10 FIG. 15 schematically illustrates a plurality of the optoelectronic element of FIG. 14A, optically coupled with other like elements.

FIG. 16 schematically illustrates an array of elements in accordance with FIG. 14A, optically coupled with other like elements to provide a logical AND or OR gate.

FIG. 17 schematically illustrates a further array of elements in accordance with FIG. 14A.

15 FIG. 18 schematically illustrates an optical/electrical hybrid processor.

FIG. 19 shows voltage vs current for a light emitting structure suitable for use in one embodiment of the present invention, with a line showing the underlying increasing trend.

20 FIG. 20 shows the changes in energy states of a HEES suitable for use in one embodiment of the present invention,

FIG. 21A shows the current vs. Voltage (I-V) properties of a HEES suitable for use in one embodiment of the present invention.

FIG. 21B is a transformation of the curve in FIG 21A.

25 DESCRIPTION

The invention will now be described with reference to specific embodiments, although it will be appreciated that the invention is not limited to those specific embodiments.

30 In broad terms, various embodiments provide optoelectronic components that are configured to receive input signals, which include either or both of electrical input signals and optical input signals, and in response to those input signals selectively provide optical output signals. This is achieved by providing a light emitting structure that generates light across a predetermined voltage range, optionally in combination

with a component for converting an optical signal to an electrical signal. As described in more detail herein, such an approach is implemented to provide voltage to light converters, optoelectronic switches, logic elements, and more complex components.

Overview

FIG. 1 illustrates an optoelectronic component 101 according to one embodiment. Component 101 comprises a light emitting structure 102, which is configured to generate light in response to a voltage signal within a predetermined range. That is, when a voltage having a value within the predetermined range is applied across the light emitting structure, the light emitting structure generates light.

Otherwise, the light emitting structure does not generate light.

For the purposes of the present disclosure, the concept of “providing a voltage signal” to a particular item or location should be read to infer that the item has an input and output between which a voltage (potential difference) is able to be applied, and the provision of a voltage signal affects (either by way of increase or decrease) the level of voltage applied across the item between the input and output. It is not essential that the voltage signal be directly applied to the item. For example, in some cases a voltage signal is provided at an input location in a circuit other than a location directly adjacent the item (for example where a second item is provided intermediate the input location and the item).

Component 101 comprises a primary input 103 by which a source voltage signal V_{source} is provided to the light emitting structure. Component 101 additionally includes at least one secondary input for providing a control voltage signal to the light emitting structure. In the example of FIG. 1, a single secondary input is provided, in the form of an electrical input 104 for receiving an electrical control voltage signal I_e .

Component 101 further comprises an output O_o for providing an optical output signal on the basis of light generated by the light emitting structure. Where the source voltage signal and control voltage signal combine to provide an overall voltage signal within the predetermined range, the light emitting structure generates light. This drives the optical output signal. As discussed further below, the present configuration allows component 121 to operate as a voltage to light converter. That is, it operates as a component that is responsive to a voltage signal within a predetermined range for providing a light signal.

Other embodiments make use of a combination of optical and electrical secondary inputs, thereby to provide more complex components including switches, logical elements and the like.

Throughout the present specification, use is made of terminology whereby I and O refer respectively to inputs and outputs, and subscripts $_e$ and $_o$ are respectively used to designate whether a particular input or output is electrical or optical. For example, I_e designates an electrical input (such as a voltage signal), I_o designates an optical input signal, and O_o designates an optical output signal.

Light Emitting Structures

As foreshadowed, component 101 comprises a light emitting structure 102. The present disclosure is predominately focussed on a light emitting structure based on the teachings of United States Patent Application No. 61/034883, which particularly deals with on-chip ZnO-ITO light emitting structures. However, it should be appreciated that the present disclosure is by no means limited to the use of structures disclosed in that patent application, and that other light emitting structures may be used, on the proviso that they meet inherent functional requirements of the present embodiments. In particular, it is a general requirement that an appropriate light emitting structure be configured so as generate light in response to a voltage signal within a predetermined range having a lower limit and an upper limit. This should be a discrete range, in the sense that no light is generated in respect of a voltage signal falling proximally above or below this range. In other words, the light emitting structure is configured to generate no light in response to a voltage signal within a first further predetermined range adjacent and below the lower limit and a second further predetermined range adjacent and above the upper limit.

Although much of the present disclosure describes a light emitting structure that generates either “light” or “no light”, that should not be regarded as necessarily limiting in a strict literal sense. For example, in some embodiments rather than a black-and-white definition of “light” and “no light”, a grey area is considered whereby light of intensity above a predefined threshold intensity is deemed to be “light”, and light of intensity below that predefined threshold intensity is deemed to be “no light”. In that regard, in some embodiments a “no light” signal does include some light in a strict sense, albeit light of intensity that is for practical purposes regarded as “no light”.

The threshold value for the first further predetermined range and the second predetermined range can be independently variable. That is, the threshold value for the first further predetermined range is greater than that for the second predetermined range, or the threshold value for the first further predetermined range is less than that for the second predetermined range, or the threshold value for the first further predetermined range is the same as that for the second predetermined range.

In a preferred light emitting structure suitable for use in the present invention, a layer of polycrystalline silicon (poly-silicon) is deposited on a substrate or wafer of single-crystal silicon. The polysilicon can be deposited by any suitable means, for example, LPCVD (Low-pressure chemical vapour deposition) at 605°C. Theoretically, the wafer of single-crystal silicon can be of any thickness. Preferably, because the single-crystal silicon is used as substrate to support the upper structures, normal silicon wafer thickness is used. The thickness of polycrystalline silicon required is preferably sufficient for the polycrystalline oxide to be formed and a layer of poly-silicon to be present under the oxide layer after oxidation. Preferably, the layer of poly-silicon is 0.5 μm to 2 μm thick. The whole is then heavily doped. The single-crystalline silicon and the poly-silicon can either be doped to be n-type (electron conduction) or p-type (hole conduction). However, for best performance, n-type doping to the poly-silicon is normally preferred. The doping is preferably heavy, i.e. at the level of $\sim 10^{19} \text{ cm}^{-3}$ or above.

Any suitable known dopants can be used, for example, the group III or group V elements, such as boron, arsenic, gallium or phosphorus. In n-type silicon wafer, arsenic is preferably used for doping, with a dopant concentration of at least 10^{19} cm^{-3} . In p-type wafers, boron is preferably used for doping, with a dopant concentration of at least 10^{19} cm^{-3} . The doping is preferably carried out by ion implantation. After doping, the dopant is preferably activated, preferably by annealing. The annealing preferably takes place in He atmosphere at a suitable temperature.

Once the doped silicon construct is prepared, a very thin layer on the top surface of the poly-silicon is oxidised. The oxidation method used is most preferably wet-oxidation. The wet oxidation of the top poly-silicon layer preferably forms a layer of oxide with thickness of having a lower limit of about 4 nm, more preferably about 7 nm, and independently an upper limit of about 15 nm, more preferably about 12 nm. The oxidation temperature is preferably in the range of 850 to 950°C to ensure a slow

and controllable oxidation process. The duration of the oxidation is relatively short, however, it varies depending on the specification of used equipment. This process produces a layer of silicon dioxide (SiO_2) on the top of the polycrystalline silicone.

It is believed that wet oxidation leads to asperities being formed at the interface of the insulator SiO_2 layer and the polysilicon layer. Asperities are irregular surface projections, of the order of a several angstroms (less than 1 nm), which have small, sharp silicon conducting tips. When a voltage is applied to the structure, it results in an enhancement or amplification of the electric field due to the sharp tips of the asperities, and this in turn serves to produce high energy "hot" electrons.

Whilst polysilicon is the most preferred source of hot electrons, suitable "hot electrons" may also be produced from other types of materials beside polysilicon, for instance, aluminium or magnesium, with the layers of corresponding oxide on top. These tend to be less desirable due to the inherent difficulties in controlling the oxidation of these materials.

FIG. 2 illustrates a light emitting structure 201 suitable for use in one embodiment of the present invention. Structure 201 includes a single crystal silicon substrate 202, onto which a heavily doped poly-silicon layer 203 is deposited. A thin oxide layer 204 is added to the poly-silicon layer, for example by way of wet oxidation. This sub-assembly is the hot electron emitting structure (HEES), which provides hot electrons through FN tunnelling, as discussed in United States Patent Application No. 61/034883. Any suitable hot electron emitting structures may be used. An optoelectronic material 205, in the present example being ZnO, is deposited on top of oxide layer 204.

ZnO has a wide bandgap that requires high energy to emit light. On HEES's, the ZnO successfully emits light, which demonstrates that the HEES is able to provide sufficiently high energy to drive the process. Therefore, it would be expected that any other optoelectronic material (direct-band) that had a narrower bandgap than ZnO could be used in conjunction with a suitable HEES as a light emitting structure. Other optoelectronic materials, for example, could be GaN, InP, GaAs, etc. Phosphors with CVD deposition on HEES are also ideal as the optoelectronic materials.

The ZnO layer may be placed on the HEES using any conventional method. The most simple methods are either conventional Sol-Gel methods or magnetron sputtering. Depending on the desired emitting properties of ZnO including wavelengths

and intensities, other methods such as LECVD and MBE can be used to deposit ZnO. When using magnetron sputter to deposit a thin layer of ZnO, either DC or radio frequency (RF) current can be used, depending on the structure and thickness required. Processing parameters such as the working atmosphere and deposition current density
5 can also be varied to control the required properties of the ZnO layer.

ZnO is an important semiconductor material with many unique properties and potential applications. The photoluminescence spectrum of ZnO has been investigated and it emits light in the range of UV, green and red. However, the electroluminescence properties of ZnO have not been well reported due to its wide energy bandgap (3.37
10 eV). In order to emit light from ZnO using electricity, a ZnO p-n junction or high energy electrons are needed. However, p-type ZnO is not easy to achieve, nor is it easy to obtain high energy electrons that can readily be injected into ZnO, especially from integrated circuits.

The ZnO layer may be of any thickness, but is preferably between 200 nm and
15 1000 nm. The most preferable thickness is 300nm. The ZnO may be n-type (electron) or p-type (holes) if it is doped for example with excess lithium, aluminium, indium or nitrogen. It is preferable to dope ZnO with lithium for the red (630nm) light emission when the device is intended for use in modern optical communication applications. The intrinsic band gap for ZnO is 3.37 eV, corresponding to the UV emission. However,
20 ZnO often contains structural defects, and can be doped to have a reduced band gap, resulting in visible light emission with controlled wavelength (colour).

Because the emitting light is from the ZnO itself by electron-hole recombination, either p- or n- type ZnO can be used. However, if a ZnO p-n junction is put in conjunction with a HEES, the light emission exhibits lasering properties and
25 therefore the light emission performance is further enhanced.

It is possible to enhance the performance of the device by the addition of a further layer of p-type material on top of the ZnO. In this case, an ITO layer 206 is deposited, preferably by sputtering on top of optoelectronic material 205.

ITO is transparent over a wide range of thickness. In light emitting applications,
30 the thickness of ITO is preferably controlled to less than 200 nm and never exceeds 500 nm. Without the addition of any further topping layers, ITO alone is sufficient to be used as the electrode that the voltage can be directly applied to as it has good

conductivity. The ITO layer is here used only as an electrode, so it may be deposited by any means, for example, by magnetron sputtering.

ITO serves as a transparent electrode layer over the top of the ZnO, to which a voltage is applied. The light generated from the underlying ZnO layer is visible
5 through the ITO electrode.

Other types of top layer electrodes such as Au can be used. A layer of Au applied in the form of a grating can be also used as electrode. The gratings on the Au allow the light to emit out more easily. Au as an electrode is very stable. The selection of electrode of either ITO or Au depends on under what conditions and for what
10 application the light emitter will be used.

Voltage is able to be applied between ITO layer 206 and silicon substrate 202, for example by way of a source 207 as shown in FIG. 2. Typically, when a voltage in range from 4 V and 18 V is applied across the sandwich structure, light is generated. The wavelength of the light varies based upon the structure and composition of the ZnO
15 layer.

The current and voltage (I-V) properties of the substrate were examined and exhibit the Fowler-Nordheim effect. It was determined that the overall structure of the HEES was responsible for generating the hot electrons.

Experiments conducted in respect of a light emitting structure corresponding to structure 201 have revealed the phenomenon illustrated in FIG. 3. During the gradual
20 increase of applied voltage, light appears (i.e. light can be observed) when the voltage reaches a certain level. Further increase of voltage causes a corresponding increase of the light intensity until voltage reaches another level when the light intensity greatly decreases or totally disappears. By further increasing the voltage, the light re-appears
25 at another voltage threshold after which the light is present until the voltage increases to another threshold when the light disappears again. The correspondence of applied voltage and light appearance on the I-V curve is shown in FIG. 3. Based on presence/absence of the light, it is possible to divide the I-V curve into four regions, R1-R4.

Based on FIG. 3, it will be readily appreciated that the emission of light is able
30 to be controlled by varying the applied voltage. Region R1 corresponds to a state where there is no light due to insufficient current flow and lack of sufficient hot electron energy. Region R2 corresponds to a state where light is emitted. In region R3,

light is not emitted due to a decrease in electron energy (as compared with region R3). Light reappears in region R4.

As noted, the present embodiments are not necessarily limited to any particular physical form of light emitting structure, although there is a particular preference for Si based light emitting structures. Functionally, it is necessary that at least two states are able to be realized by way of voltage modification, being a state wherein light is emitted, and a state where light is not emitted. Preferably, the light emitting structure should display at least one current peak on the I-V curve corresponding to a predetermined voltage range for the emission of visible light. In some embodiments there are multiple current peaks, and it will be appreciated that such a characteristic allows for more distinct states, and therefore more complex operations. However, multiple peaks are by no means necessary, and for many applications of the present technology a single peak is entirely adequate.

Voltage to Light Converter

As noted above, component 101 of FIG. 1 is configured to operate as a voltage to light converter (VLC). This leverages the nature of the current peak on the I-V curve, which corresponds to a predetermined voltage range for the emission of visible light. Such a VLC enables bridging between the optical and electrical world in a manner that can be realised on Si chips. For example, a VLC may be implemented as an on-chip device, or as part of such an on-chip device.

By selecting a constant supply voltage (V_{source}), it is possible to affect the behaviour of the light emitting structure by making incremental adjustments to the input voltage signal (I_e). In particular, by controlling the input voltage signal (I_e) in a single step (for example “present” or “absent”) the output signal (O_o) is switched on and off respectively. This provides distinctive states for the component corresponding to presence and non-presence of generated light. In this manner, the light emitting structure acts as a discrete voltage controlled light generator, or VLC.

The output of a component such as the present VLC can be assigned basic logic values, such as “0” (for describing a situation where there is no light) and “1” (for describing a situation where there is light). As shown in FIG. 4, it is possible to identify four states (State 1 – State 4) for a VLC, with these corresponding to regions R1-R4 on the I-V curve. In States 1 and 3 the optical output is 0 (i.e. no light); while in

States 2 and 4 the optical output is 1 (i.e. light is generated). In this manner, the VLC behaves as a “light switch” having a discrete voltage input that results in the generation of light. It will be appreciated that this effect is realized due to a presence of a peak on the I-V curve.

5 The example above assumes the input voltage signal (I_e) is controlled only in a single step. However, if the input voltage can change in four distinctive levels, then the operation of a VLC such as component 101 becomes even more interesting. In this regard, reference is made to FIG. 5, which illustrates the behaviour of VLC in time domain where input voltage is changed in four distinctive levels.

10 A VLC is optionally utilised for conversion of electrical to light signals, and/or as a source of light signals for further optoelectronic information processing. Also, as discussed below, the concept of a VLC provides a basis for more complex optoelectronic components, including optoelectronic switches, logic gates, and the like. Such components add another dimension (specifically light) into the conventional
15 world of integrated circuits, which is presently wholly dominated by electrons. For example, such components are optionally provided as on-chip devices in the context of integrated circuits.

Optoelectronic Switch

FIG. 6A and FIG. 6B illustrate an optoelectronic switch 601 according to one
20 embodiment. In this regard, FIG. 6A illustrates switch 601 in a manner similar to component 101 of FIG. 1, whereas FIG. 6B illustrates switch 601 by way of a schematic circuit diagram. In overview, whereas component 101 of FIG. 1 is controlled by way of adjusting an input voltage signal (I_e), switch 601 is controlled by way of an optical input signal (I_o).

25 Switch 601 shares features with component 101, and these are identified by like reference numerals for the sake of consistency. Switch 601 additionally comprises a secondary input in the form of a photoresistor 602 that is responsive to an optical input signal (I_o) for providing a corresponding control voltage signal to light emitting structure 101. In this instance, the control voltage signal is provided by way of
30 affecting the extent to which V_{source} applies a potential difference across light emitting structure 102.

As both light emitting structure 102 and photoresistor 602 are based on silicon, their electrical connection can be considered as two resistors connected serially. When the constant voltage V_{source} is applied across the pair, the voltage is divided between the light emitting structure 102 and photoresistor 602 according to their respective resistances. In the event that photoresistor 602 is exposed to an optical input signal, the free carriers (electrons) receive energy and begin moving, thereby to generate current. Concurrently, the resistance of the photoresistor decreases and causes an increase in voltage across light emitting structure 102, resulting in the emission of light, and therefore the progression of switch 601 into a "light on" state wherein the optical output signal (O_o) is provided. Therefore, the operating state of the switch is dependent on the optical input of the photoresistor, and the output signal of the switch is activated and deactivated synchronously with the optical input signal. It will be appreciated that V_{source} is set at an appropriate level such that the extent of incremental adjustment brought about by the optical input signal is appropriate to adjust the overall voltage across the light emitting structure into the predetermined range for the emission of light.

Optoelectronic Logic Element

FIG. 7A and FIG. 7B illustrate an optoelectronic logic element (OLE) 701 according to one embodiment. These figures are respectively presented in a similar manner to FIG. 6A and FIG. 6B. In overview, OLE 701 extends the functionality of switch 601 such that the provision of an optical output signal (O_o) is dependent on either or both of an optical input signal (I_o) and an electrical input signal (referred to as V_{ctrl}). Once again, features present in previous examples have been designated corresponding reference numerals.

OLE 701 includes a first secondary input in the form of a photoresistor 602, which is responsive to an optical input signal (I_o) for providing a corresponding control voltage signal to light emitting structure 101, and second secondary input in the form of an electric input 104, which provides a control voltage signal V_{ctrl} . In this case, the overall voltage applied to the light emitting structure is dependent on both the optical signal input I_o and electrical control signal V_{ctrl} . This provides an optoelectronic logic element that selectively provides an optical output signal based on those signals.

It is possible to consider the behaviour of OLE 701 based on the states shown in FIG. 4. For example, one interpretation is detailed below:

- State 1 defines an initial state, which provides no output (optical “0”). Therefore, in the case that V_{ctrl} is “0”, when I_o is “0”, OLE 701 remains in the initial state (State 1) and the output of OLE is “0”.
- In the case that V_{ctrl} is “0”, and I_o is “1”, the OLE adopts State 2 and the output of OLE is “1”.
- In the case that V_{ctrl} is “1”, and I_o is “0”, the OLE adopts State 2 and outputs “1”.
- In the case that V_{ctrl} is “1”, and I_o is “1”, the OLE is in State 3 and outputs “0”.

It is apparent from the above analysis that the OLE passes the input signal to the output when V_{ctrl} is “0” and it reverses the input signal when V_{ctrl} is “1”. The OLE is, in this manner, used as foundation for optoelectronic logic gates, as discussed in more detail below.

Optoelectronic Logic Gates

Exemplary optoelectronic logic gates are discussed below. In overview, these make use of OLE 701 to perform basic logical functionalities. More particularly, by adjusting V_{ctrl} , it is possible to configure OLE 701 for various purposes.

FIG. 8 illustrates a “PASS” gate 801 according to one embodiment. PASS gate 801 includes OLE 701, with V_{ctrl} set to “0”. The input/output functionality of such a logic gate is described in the table below:

Optical Input (I_o)	Optical Output (O_o)
0	0
1	1

In absence of a light signal, only the source voltage (V_{source}) is applied on the OLE. If the optical signal “0” is provided as input, the OLE does not change state, and remains in State 1 in which optical output is “0”. When the optical signal “1” is provided as input, the OLE adopts in State 2, and an optical “1” is provided as output. Therefore, this logic gate passes the identical output as the input signal, and accordingly is regarded as a PASS gate.

FIG. 9 illustrates a “NOT” gate 901 according to one embodiment. NOT gate 901 includes OLE 701, with V_{ctrl} set to “1”. The input/output functionality of such a logic gate is described in the table below:

Optical Input (I_o)	Optical Output (O_o)
0	1
1	0

When $V_{ctrl}=1$, this causes OLE 701 to operate in State 2, in which it emits light (i.e. provides optical “1” as output). In the presence of optical input signal “0”, OLE 701 stays in State 2 and outputs “1”. When the optical input is “1”, OLE 701 adopts State 3 and outputs “0”. Therefore, this logic gate passes the contrary output to the
 5 input signal, and accordingly is regarded as a NOT gate.

Advantageously, an OLE is able to be converted from a PASS gate to a NOT gate (or vice versa) simply by adjusting V_{ctrl} . This provides for a particularly flexible and adaptable logical arrangement.

To achieve more complex logical structures, it is possible to, combine a
 10 plurality of OLEs. This is optionally achieved by way of an optical combiner, such as a waveguide. By way of example, FIG. 10 illustrates a waveguide-type optical combiner 1001, specifically being a Y-branch optical combiner. This is used as a 2-to-1 combiner, thereby to combine light from two sources (such as the respective outputs of two OLEs) to a single light signal (which may then be provided as optical input to a
 15 further OLE). Such an approach allows for the creation of a logical “AND” gate, as discussed below.

FIG. 11 illustrates a logical AND gate 1101 according to one embodiment. Gate 1101 comprises three OLEs, being OLE 701A, OLE 701B and OLE 701C. OLE 701A receives an optical input signal I_{oA} , and OLE 701B receives an optical input
 20 signal I_{oB} . The respective outputs of OLE 701A and OLE 701B are combined by way of optical combiner 1001 (although other approaches for combining these output signals are used in other embodiments) and provided as an optical input to OLE 701C. OLE 701C then provides an optical output signal (O_o).

In the illustrated arrangement, V_{ctrl} set to “1” for all the OLEs. As such, the
 25 operation of gate 1101 is described in the following table.

Optical Input 1 (I_{oA})	Optical Input 2 (I_{oB})	Optical Output (O_o)
0	0	0
0	1	0
1	0	0

1	1	1
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When I_{oA} and I_{oB} are both "0", OLE 701A and OLE 701B both operate in State 2, and provide light to OLE 701C through optical combiner 1001. When receiving a light signal (i.e. optical "1") from n th OLE 701A and OLE 701B, OLE 701C operates in State 3 which outputs "0". When I_{oA} is "0" and I_{oB} is "1", OLE 701A operates in State 2 and outputs "1", while OLE 701B operates in State 3 and outputs "0". The "1" and "0" combine thereby to provide "1" to OLE 701C, which adopts State and provides optical output "0". A similar situation applies where I_{oA} is "1" and I_{oB} is "0".

However, when both I_{oA} and I_{oB} are "1", OLE 701A and OLE 701B operate in State 3 and both output "0" to OLE 701C. As such, OLE 701C remains in State 2 which outputs "1". Therefore, an optical output of "1" is provided only in the event that both optical inputs are "1", and hence gate 1101 operates as an AND gate.

Referring now to FIG. 12, by using the same physical components as in FIG. 11, it is possible to configure a logical OR gate 1201. In essence, the only difference between AND gate 1101 and OR gate 1201 is that, in the case of the latter, V_{ctrl} set to "0" for all the OLEs. As such, the following table describes the operation of OR gate 1201:

Optical Input 1 (I_{oA})	Optical Input 2 (I_{oB})	Optical Output (O_o)
0	0	0
0	1	1
1	0	1
1	1	1

When both I_{oA} and I_{oB} are "0", OLE 701A and OLE 701B remain in State 1 and provide no light signal, corresponding to an optical "0". In response to the "0" input, OLE 701C also outputs "0". When I_{oA} is "0" and I_{oB} is "1", OLE 701A remains in state 1 and outputs "0", whilst OLE 701B moves into State 2 and outputs "1". A "1" signal and "0" signal are fed through the optical combiner, resulting in a combined "1" signal (light, combined with no light, results in light). In response to this "1" signal, OLE 701C moves from State 1 to State 2 and outputs optical "1". This is generally replicated for the situation when I_{oA} is "1" and I_{oB} is "0". When both I_{oA} and I_{oB} are "1", OLE 701A and OLE 701B each operate in State 2 output "1". A "1" signal and

“1” signal are fed through the optical combiner, resulting in a combined “1” signal (light, combined with light, results in light). As such, OLE 701C outputs a “1” signal.

From this, it will be recognised that gate 1201 passes a “1” signal in response to the receipt of a “1” signal at either or both of its inputs, and hence operates as an OR gate.

Advantageously, the functionality of a logic gate such as gate 1101 or 1201 is able to be remotely controlled and varied by adjusting V_{ctrl} for one or more OLEs. By way of example, adjusting gate 1101 such that for OLE 701C V_{ctrl} is set to “1” would provide an exclusive OR gate (a “1” signal is provided if a “1” signal is received at either input, but not both).

Systems/components that are built by combining OLEs operate on pure optical signals. As such, optoelectronic logic gates such as those considered above represent basic building blocks equivalent to conventional electronic logic gates, albeit with the fundamental difference that information processing is performed in the optical domain by means of photons. Furthermore, the ability to use electric signals to configure OLEs provides for a high degree of flexibility in terms of functional configuration and/or reconfiguration. This provides for significant advances in the field of photonic computation.

Fabrication of Optoelectronic Logic Elements

Described below, by reference to FIG. 13A to FIG. 13D, is an exemplary method for the fabrication of an OLE according to one embodiment. It will be appreciated that this is provided as an example only, and that other shapes, configurations or methods are applied in further embodiments.

In overview, fabrication is realised by way of a CMOS process. FIG. 13A to FIG. 13D provide a schematic side view of the present fabrication process. Referring initially to FIG. 13A, the starting point is to provide a substrate of n-type silicon 1303, presently being single crystal silicon. A portion 1302 is removed by way of an etching process, defining a silicon wafer body 1303. Body 1303 presently includes three cross-sectional steps. As shown in FIG. 13B, a removable shade 1304 is applied to body 1303. This shade shields the uppermost step during subsequent procedures, which presently include poly-silicon deposition, n+ doping and annealing, and is subsequently removed. Upon removal of shade 304, a layer 1305 is n+ poly-silicon extends across

and between the lower two steps of body 1303. The top step remains upwardly exposed.

Referring now to FIG. 13C, a removable shade 1306 is applied along the top step of body 1303, and extends to cover the adjacent portion of layer 1306. This protects the covered regions during subsequent steps, which presently include:

- Creation of a poly-oxide layer 1307 on the exposed regions of layer 1305, optionally by way of an oxidation process.
 - Sputtering of ZnO, presently across the entire component (including a region of layer 1307). This creates a ZnO portion 1308.
 - Sputtering of ITO, presently across the entire component (including a region of atop the ZnO on layer 1307). This creates an ITO layer 1309.
- In the present embodiment, this ITO layer has an upper extremity which is substantially flush with the upper extremity of layer 1305.

Upon removal of shade 1306, the component has an exposed upper surface including a region of ITO, which is separated by way of a layer of poly-oxide from a region of poly silicon, and a region of n- silicon. As shown in FIG. 13D, a shade 1301 is applied to allow selective p⁺ doping of a portion of the exposed n- silicon, thereby to provide a region 1311 of p- silicon. This provides a p-n junction, and hence a simple photoresistor.

In some embodiments an uppermost peripheral boundary of blank silicon is provide for the purposes of wiring, as shown in subsequent examples further below.

The final product of the above described fabrication process, being element 1401, is shown in FIG. 14A (which provides a schematic side view) and FIG. 14B (which provides a schematic top view). Electrical connections are made so as to allow V_{ctrl} and V_{source} to be appropriately applied to the component, much like in the example of FIG. 2. An optical signal is received as shown, and depending on the intensity of that optical signal, and the values electrical input signals V_{ctrl} and V_{source} , an optical output signal is selectively provided through ITO layer 1309.

Elements such as element 1401 are able to be optically interconnected. For example, FIG. 15 shows three elements 401 optically interconnected by way of a mirror array 1501. In this manner, light emitted via the ITO layer of a given element is provided to the p-n junction photoresistor of an adjacent element. It will be appreciated

that the present goal is readily achieved by approaches other than the use of a mirror array, such as by way of one or more waveguides.

Optoelectronic Logic Element Array

FIG. 16 illustrates a simple optoelectronic logic element array using three elements 1401, connected by portions of blank silicon 1600. It will be recognised that the illustrated array is able to provide an AND or OR gate as described further above. In particular, an optical input signal is provided to a pair of upstream elements, which in response provide either an optical “1” or “0”. In the case of an optical “1”, light is provided to the downstream element 1401, for example by way of a mirror or waveguide arrangement. In responsive to such input (or inputs), the downstream element 1401 provide either an optical “1” or “0”.

The basic array of FIG. 16 is readily expanded to provide a more complex array, such as array 1701 shown in FIG. 17. This provides for a large-scale integrated layout. It will be appreciated that the flow of optical signals in such an array is determined by optical connection configurations, for example based on waveguide or mirror arrangements. Furthermore, it will be appreciated that the array is particularly adaptable from a configuration/functionality perspective, given that logical rules are readily affected by varying the value of V_{ctrl} provided to one or more of the elements in the array.

In the example of FIG. 17, the basic optical logic elements are integrated and fabricated on silicon wafer by CMOS process. Once electrodes for each of these are connected respective power sources, they implement specific functionalities that process signals in optical domain only. Optical signals may propagate horizontally and/or vertically. Therefore, by connecting the individual logic elements to form the signal paths, more complicated functions can be realized. Programmability can be achieved through either or both of the following mechanisms:

- Using either a CMOS process or a MEMS (Micro-Electro-Mechanical Systems) process, different configurations of mirrors/waveguides are able to be created, with different configurations of mirrors/waveguides determining different functions of the optical integrated circuit.
- By applying similar principles as used in traditional semiconductor devices, in particular the notion of a Field-Programmable Gate Array

(FPGA), is it possible to realize Field Programmable Optical Arrays (FPOA) where the programmability would be achieved.

Arrays such as that shown in FIG. 17 are inherently adapted to provide a basis for computing in the optical domain, in a manner generally comparable to conventional computing in the electrical domain.

Large Scale Application of Optoelectronic Logic Elements

Based on the example of FIG. 17, optical logic element fabrication is able to be implemented by way of a CMOS process, and adapted for large scale integration. In terms of performance, provided that optical logic elements are small (in the order of tens of nanometres), which is readily achievable using technologies described herein, the time spent on optical propagation (which is at the speed of light) between the elements can generally be ignored. The response time of an optical logic element is predominately dependent on the photon-to-electron process: when one electron in conduct band “jumps” down to the valence band and is recombined with a hole, one photon is released at the energy of the bandgap. It has been suggested that for a fast carrier sweep-out, pulse response times of 3.5ps FWHM at room temperature are achievable. Noting that for conventional electrical logic elements, response times are in the nanosecond range, optical logic elements potentially can be used for faster information processing.

With this in mind, FIG. 18 illustrates an exemplary configuration whereby optical information processing is combined with traditional electronic processing. In this example, digital processors 1801 are coupled to VLC arrays 1802 (based on VLC technology described above, and optionally leveraging fabrication approaches noted above), thereby to convert electrical “1” and “0” signals to optical “1” and “0” signals, which are fed to an optical processor 1803 (such as an array along the lines of that shown in FIG. 17). The optical processor outputs optical signals to a photo-detector array 1804, which converts optical signals to electrical signals, and final output is provided by way of a digital logic output component 1805. The combination of electrical and optical components is conveniently realised on the basis that:

- Fabrication of the light emitting structure and hence the optical logic components is fully scaleable and compatible with a conventional CMOS (Complementary metal–oxide–semiconductor) process, thus

fabrication of the digital and optical components can be achieved on a common silicon substrate.

- All conventional (electrical) logic elements can be equally defined in terms of optical logic elements (for example based on discussion above), so functionalities are complementary.

Furthermore, advantages are able to be realized on the basis that an optical processor might be configured to provide a larger throughput and processing capacity than the electronic processor. By adopting the optical logic element to build such an optical processor, the overall system achieves higher capacity and increases opportunities for parallelisation of computation in the optical domain.

Example of Light Emitting Structure Formation and Performance (1)

The light emission performance of the present device with a Sol-Gel prepared ZnO layer and a top electrode of Au was determined. The thicknesses of ZnO and Au are 700 nm and 300 nm, respectively. The ZnO is deposited at the whole area of the sample (1.5 cm × 1.5 cm) and the Au electrode is a round plate of 1 mm diameter. The light emission was observed under microscope and with the naked eye. The light starts emitting at an applied voltage of 9.5 V, and emits up to the breakdown voltage of the device at 13 V. The device yielded yellow and red light.

Example of Light Emitting Structure Formation and Performance (2)

The light emission performance with a magnetron-sputtered ZnO layer and a top electrode of ITO was determined. The thickness of ZnO varies from 200 nm to 2 μm. The thickness of ITO is from 200 nm to 300 nm. The ZnO is sputtered at the whole surface of the sample while the ITO electrode is a round plate of 1 mm diameter. From the experiments, the samples with a ZnO thicknesses in the range of 300 nm to 700 nm and ITO thicknesses of 200 nm have the best light emitting performance relative to other devices. The light emission was stronger than that observed for the Sol-Gel ZnO/Au setting. The starting light emitting voltage was 5.7 V as observed by the naked eye and continued to the breakdown voltage of the device at 18 V. The starting emission voltage is lower and the breakdown voltage is also significantly higher than for the Sol-Gel ZnO/Au device. The device provides light of a wavelength of 520 nm (Green) and 620 nm (Red) electroluminescence. A weak emission of UV light is also observed.

This system is very stable in ambient pressure and temperature, which is a significant improvement over other electroforming devices which are reported to last from around 3 hrs to at most 2 days as reported. The devices of the present invention are found to be very stable with respect to the time, and no apparent degradation has been observed during the course of the research thus far.

As mentioned above, the Hot Electron Emitting Substrate (HEES) described herein exhibits a phenomenon which can be referred to as “double tunnelling”. At ambient atmospheres and at room temperatures, the I-V characteristic of HEES shows two current peaks during voltage sweep from 2V to 15V. Without wishing to be bound by theory, the two current peaks are believed to indicate two different tunnelling processes, Fowler Nordheim (FN) tunnelling and a tunnelling diode mechanism which occur at two different voltage ranges.

To examine the double tunnelling of the HEES, a layer of poly-crystalline silicon (poly-Si) was deposited on an *n*-type single-crystalline silicon wafer, and heavily doped with Boron at the level of $\sim 1 \times 10^{19} \text{ cm}^{-3}$. A very thin layer of silicon dioxide (SiO_2) was formed on the poly-Si by wet-oxidation. The single-crystalline silicon supports the upper layers and makes the contact with the electrode for testing.

A layer of electrode was then deposited on the SiO_2 . In one embodiment, an aluminium film was applied which is deposited with a metal mask to form a circular 300 nm thick Al plate of 1 mm diameter, which serves as an anode. The sample is placed on a metal plate which is used as a cathode. As the doped single-crystalline silicon wafer is conductive, the contact between the metal plate and single-crystalline silicon wafer has good conductivity. A voltage is applied between the cathode and a probe tip which contacts the Al anode. The testing was conducted at room temperature and in ambient atmosphere in a dark environment to avoid the possibility of photo stimulated electron emission. The voltage was swept from 2 V to 15 V with the step of 0.02 V. The resulting I-V curve is shown in Figure 19. Figure 19 shows clearly two current peaks. The current increases nonlinearly with the voltage in the beginning, and reaches the first current peak at around 3 V. Then the current drops a little and starts increasing again at around 4.5 V. At around 9 V, the second current peak is identified. Then the current decreases again, and resumes increasing at around 12 V. Apart from the two peaks, the curve keeps a steady increase trend as shown by the dashed line in Figure 19. As noted in the I-V curve shown in Figure 19, the current level is very low.

This current level is dependent on the doping concentration/resistivity of the single crystalline silicon substrate. Therefore, it can be increased by increasing the doping concentration and thus reducing the resistivity.

As indicated above, the two current peaks are believed to be the result of two different tunnelling processes. In lower voltage range, the first current peak exhibits the properties of FN Tunnelling while in the higher voltage range the mechanisms of Tunnelling Diode can be used to explain the second current peak.

In FN Tunnelling, only the electrons with energy sufficient to surmount the surface potential barrier are able to tunnel through the insulating layer and escape from the condensed phase. This can happen if two conditions are satisfied: (1) electrons have to be energetic (have high energy) and (2) the insulating layer through which electrons are to tunnel has to be thin enough that the electrons are not trapped in it. In the HEES structure of the present invention, the silicon dioxide is preferably present in a very thin layer (6 to 12 nm).

In FN Tunnelling, the current density J increases exponentially with the applied electric field E [1]:

$$J = K_1 \cdot E^2 \exp\left(-\frac{K_2}{E}\right) \quad (1)$$

where

$$K_1 = 1.5413 \times 10^{-6} \cdot \frac{m_o}{m_{ox}} \frac{1}{\phi} \quad K_2 = 6.828 \times 10^7 \cdot \sqrt{\frac{m_{ox}}{m_o}} \cdot \phi^{3/2} \quad (2)$$

In (2), ϕ is the barrier height between the semiconductor and insulator, m_o is the effective mass of an electron, and m_{ox} is the effective electron mass in oxide layer. $m_{ox} = 0.5 m_o$ [3].

To distinguish the FN tunnelling from other I-V properties which also exhibit the exponential relationship between voltage and current, a transformation of equation (1) is taken as shown in (3).

$$\frac{d(\log(J/E^2))}{d(1/E)} = -k\phi^{3/2} \quad (3)$$

where,

$$k = \frac{4}{3} \cdot \frac{\sqrt{2m_{ox}q}}{\hbar\sqrt{m_o}} \bigg/ \ln(10) ,$$

$q = 1.6 \times 10^{-19}$, C is the electron charge and $\hbar = 6.58 \times 10^{-16} \text{ eV}\cdot\text{s}$ is the Reduced Planck Constant

5 From (3), the relation between $\log(J/E^2)$ and $1/E$ is obtained as a straight line with negative slope $-k\phi^{3/2}$, which is used to characterize the FN tunnelling.

To verify the FN Tunnelling feature of HEES, the voltage was swept from 0 V to 3 V. The I-V curve of a typical HEES sample is shown in Figure 21(a).

Based on equation (3), the transformation of the curve is done under the
 10 following conditions: $J = I/A$ and $E = V/d$, where I is the collected current, V is the applied voltage, A is the area of the Al anode with a radius $r = 0.5$ mm, and the thickness of SiO_2 $d = 12$ nm. The result in Figure 21(b) shows an approximately straight line with negative slope, indicating the FN effect. Because the thickness of the silicon dioxide is not uniform due to the fabrication process, this analysis uses an approximate
 15 value of the potential barrier height and electric field (which actually varies from point to point under the same electrode). The potential barrier obtained from the curve in Figure 21b by using [3] is 3.3 eV. Because the thickness of SiO_2 was 12 nm, the tunnelling phenomenon presented above cannot be explained as direct tunnelling, which requires smaller SiO_2 thickness (<4 nm), but rather as FN tunnelling. Due to the
 20 FN tunnelling, the electrons tunnelled through SiO_2 provide an additional current component to the normal current flow. This additional current contributes to the overall abrupt current increase in the beginning. Then, according to Figure 19, the current drops and forms the first current peak. The reason for the drop of the current is still not clear. Without wishing to be bound by theory, the present applicant believes that
 25 changes in the material such as electroforming may have occurred, which causes the current to drop at this voltage level before it starts to increase again.

Turning to the second peak, it is known that by implementing a very thin p - n junction, electrons are tunnelled from the valence band of p -side to the conduction band of n -side. This electron tunnelling phenomenon is the basis of the tunnelling diode. It
 30 results in a current peak formed when the voltage is increased. Although HEES is not a

p-n junction, similar reasoning can be used to explain its behaviour at the higher voltage range where the second current peak appears.

In figure 20, item (a) shows the initial energy band structure state when HEES structure is formed. The behaviour of HEES structure is analysed when the voltage is applied from silicon dioxide side (anode) to poly-Si side (cathode). In Figure 20, items (b-d), q stands for the electron charge, while V_i ($i=1, 2, 3$) is the voltage applied to HEES. Because the poly-Si is heavily doped, when the voltage increases the electron energy band in the poly-Si side moves up relative to the energy band of silicon-dioxide. With further increase of the voltage (V_1), electron diffusion starts to occur when it reaches the state as shown in figure 20, item (b). When the applied voltage increases to a certain level V_2 , the energy band comes to the state as shown in figure 20, item (c). In this state the electrons in the valence band in doped poly-Si get enough energy to match the conduction band energy states in silicon dioxide, resulting in electron tunnelling from the doped poly-Si into silicon dioxide through the thinned band gap. At this stage, both electron diffusion and tunnelling are simultaneously present, resulting in an abruptly increased current. However, when the voltage increases further to V_3 (Figure 20, item (d)), the energy states become mismatched, electron tunnelling stops, and the current drops. Thus, the second current peak is formed. From this point on, electron diffusion dominates the transportation of electrons in HEES.

Thus, without wishing to be bound by any specific theoretical interpretation for the observed phenomena, the applicants suggest that the two tunnelling effects as explained above are the main contributors to the current peaks in I-V curve of HEES structure, which they have "the double tunnelling effect". Since tunnelling needs an amplified electric field, it appears that an electric field amplification mechanism is operative within the HEES structure. It is believed that very small and sharp conductive tips (asperities) formed at the interface area between poly-Si and SiO₂ during the fabrication processes amplify and accelerate electrons under an applied electric field.

Although the invention has been described with reference to specific examples, it will be appreciated by those skilled in the art that the invention may be embodied in many other forms. While there has been described what are believed to be the preferred embodiments of the invention, those skilled in the art will recognize that other and further modifications may be made thereto without departing from the spirit of the

invention, and it is intended to claim all such changes and modifications as fall within the scope of the invention. For example, any formulae given above are merely representative of procedures that may be used. Functionality may be added or deleted from the block diagrams and operations may be interchanged among functional blocks.

- 5 Steps may be added to or deleted from methods described herein whilst remaining within the scope of the present invention.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. An optoelectronic component comprising:
 - a light emitting structure that is configured to generate light in response to a voltage signal within a predetermined range, the predetermined range having a lower limit and upper limit;
 - a primary input for receiving a source voltage signal that is applied to the light emitting structure;
 - at least one secondary input for receiving an input signal and, in response to the input signal, providing a control voltage signal that is applied to the light emitting structure; and
 - an output for providing an optical output signal on the basis of light generated by the light emitting structure, such that where the source voltage signal and control voltage signal combine to provide an overall voltage signal within the predetermined range, the light emitting structure generates light for driving the optical output signal.
2. An optoelectronic component according to claim 1 comprising a secondary input in that is responsive to an optical input signal for providing the control voltage signal.
3. An optoelectronic component according to claim 1 or claim 2 comprising a secondary input that is responsive to an electrical input signal for providing the control voltage signal.
4. An optoelectronic component according to claim 1 comprising:
 - a first secondary input that is responsive to an optical input signal for providing a first control voltage signal; and
 - a second secondary input that is responsive to an electrical input signal for providing a second control voltage signal.
5. An optoelectronic component according to any preceding claim comprising a secondary input comprising a PIN photoresistor that is responsive to an optical input signal for providing the control voltage signal.

6. An optoelectronic component according to claim 5 wherein the photoresistor is serially connected to the light emitting structure, such that the source voltage signal applies a potential difference proportionally between the light emitting structure and the photoresistor in accordance with their relative electrical resistances.
7. An optoelectronic component according to claim 6 wherein the photoresistor provides the voltage control signal by reducing its electrical resistance in response to the optical input signal, thereby to increase the proportion of the potential difference that is applied to the light emitting structure.
8. An optoelectronic component comprising:
a light emitting structure that is configured to generate light in response to a voltage signal within a predetermined range, the predetermined range having a lower limit and upper limit;
a primary input for receiving a source voltage signal that is applied to the light emitting structure;
a secondary input for receiving an optical input signal and, in response to the optical input signal, varying the overall voltage applied to the light emitting structure; and
an output for providing an optical output signal on the basis of light generated by the light emitting structure, such that the component is operable in a first state wherein the optical output signal is not provided, and a second state wherein the optical output signal is provided.
9. An optoelectronic component according to claim 8 wherein the secondary input comprises a photoresistor.
10. An optoelectronic component comprising:
a light emitting structure that is configured to generate light in response to a voltage signal within a predetermined range, the predetermined range having a lower limit and upper limit;
a primary input for receiving a source voltage signal that is applied to the light emitting structure;

a secondary input for receiving an optical input signal and, in response to the optical input signal, varying the overall voltage applied to the light emitting structure;

a tertiary input for receiving an electrical input signal and, in response to the electrical input signal, varying the overall voltage applied to the light emitting structure; and

an output for providing an optical output signal on the basis of light generated by the light emitting structure, such that the component is operable in:

a first state wherein neither the optical input signal nor the electrical input signal is received, and the optical output signal is not provided;

a second state wherein one of the optical input signal and the electrical input signal is received, and the optical output signal is provided; and

a third state wherein both the optical input signal and the electrical input signal is received, and the optical output signal is not provided.

11. An optoelectronic component comprising two or more constituent optoelectronic components according to claim 10.

12. An optoelectronic component according to claim 11 wherein the respective outputs of two or more constituent optoelectronic components according to claim 10 are combined to provide an optical input signal for a further optoelectronic logic element according to claim 10.

13. An optoelectronic component according to any preceding claim wherein the light emitting structure configured to generate no light in response to a voltage signal within a first further predetermined range adjacent and below the lower limit and a second further predetermined range adjacent and above the upper limit.

14. An optoelectronic component according to any preceding claim wherein the light emitting structure configured to generate an intensity of light below a predefined threshold intensity in response to a voltage signal within a first further predetermined range adjacent and below the lower limit and a second further predetermined range adjacent and above the upper limit.

15. An optoelectronic component according to any preceding claim wherein the light emitting structure configured to generate substantially no light in response to a voltage signal within a first further predetermined range adjacent and below the lower limit and a second further predetermined range adjacent and above the upper limit.
16. An optoelectronic component according to any preceding claim wherein the light generated by the light emitting structure in response to the voltage signal within the predetermined range is of greater than a predefined threshold intensity level.
17. An optoelectronic component according to any preceding claim wherein the light emitting structure is silicon based.
18. An optoelectronic component according to any preceding claim wherein the light emitting structure displays at least one current peak on an I-V curve, wherein the peak corresponds to the predetermined voltage.
19. An optoelectronic component according to claim 18 wherein the light emitting structure displays multiple current peaks on an I-V curve.
20. An optoelectronic component according to any one of claims 1 to 19 wherein the light emitting structure comprises a hot electron source and a layer of optoelectronic material disposed thereon.
21. An optoelectronic component according to any one of claims 1 to 19 wherein the light emitting structure comprises a hot electron source; a layer of optoelectronic material disposed on the hot electron source; and p-type material disposed on the optoelectronic material.
22. An optoelectronic component according to claim 20 or claim 21 wherein the light emitting structure comprises a single crystal silicon substrate, a polycrystalline silicon layer disposed thereon; and an uppermost layer of silicon oxide.
23. An optoelectronic component according to claim 20 or claim 21 wherein the light emitting structure comprises a single crystal silicon substrate having an

aluminium or magnesium layer disposed thereon, with a corresponding uppermost layer of aluminium oxide or magnesium oxide.

24. An optoelectronic component according to any one of claims 1 to 19 wherein the light emitting structure comprises a hot electron source and a zinc oxide layer disposed thereon.
25. An optoelectronic component according to any one of claims 1 to 19 wherein the light emitting structure comprises a hot electron source, a zinc oxide layer disposed thereon; and an indium tin oxide (ITO) layer or a gold (Au) layer or a gold (Au) grating layer disposed on the zinc oxide layer.
26. An optoelectronic component according to any one of claims 1 to 19 wherein the light emitting structure comprises, in order, the following layers:
a polycrystalline silicon layer;
a silicon dioxide layer; and
a zinc oxide layer.
27. An optoelectronic component according to any one of claims 1 to 19 wherein the light emitting structure comprises, in order, the following layers:
a polycrystalline silicon layer;
a silicon dioxide layer;
a zinc oxide layer; and
an indium tin oxide (ITO) layer.
28. An optoelectronic component according to any one of claims 1 to 19 wherein the light emitting structure comprises, in order, the following layers:
a polycrystalline silicon layer;
a silicon dioxide layer;
a zinc oxide layer; and
a gold (Au) layer.
29. An optoelectronic component according to any one of claims 1 to 19 wherein the light emitting structure comprises, in order, the following layers:
a polycrystalline silicon layer;

a silicon dioxide layer;
a zinc oxide layer; and
a gold (Au) grating layer.

- 5 30. An optoelectronic component according any one of claims 1 to 19 wherein the light emitting structure comprises, in order, the following layers:
a single crystal silicon substrate;
a polycrystalline silicon layer;
a silicon dioxide layer; and
a zinc oxide layer.
- 10 31. An optoelectronic component according to any one of claims 1 to 19 wherein the light emitting structure comprises, in order, the following layers:
a single crystal silicon substrate;
a polycrystalline silicon layer;
a silicon dioxide layer;
15 a zinc oxide layer; and
an indium tin oxide (ITO) layer.
32. An optoelectronic component according to any one of claims 26 to 31 wherein the single crystal silicon substrate and the polycrystalline silicon layer are doped such that they are both n-type or p-type doped.
- 20 33. An optoelectronic component according to claim 32 wherein the single crystal silicon substrate and the polycrystalline silicon layer are heavy doped and annealed.
34. An optoelectronic component according to claim 32 wherein the single crystal silicon substrate and the polysilicon layer are both heavy doped to be n-type
25 silicon and annealed.
35. An optoelectronic component according to claim 32 wherein the single crystal silicon substrate and the polysilicon layer are both heavy doped to be or p-type silicon and annealed.

36. A computing device which comprises an optoelectronic component according to any preceding claim.

37. An integrated circuit which comprises an optoelectronic component according to any preceding claim.

5 38. A method for signal processing including the steps of:

(a) providing light emitting structure that is configured to generate light in response to a voltage signal within a predetermined range;

(b) applying a source voltage across the light emitting structure;

(c) selectively applying a control voltage across the light emitting structure;

10 (d) receiving an optical input signal at a photoresistor coupled to the light emitting structure thereby to vary the overall voltage applied across light emitting structure; and

(e) observing an output of the light emitting structure, wherein the output is dependent on the presence/absence of the control voltage signal and/or the optical input signal.

15 39. An optical/electrical hybrid processor comprising:

one or more electrical processors, wherein each electrical processor is coupled to a VLC array for converting electrical output signals from the electrical processors to optical output signals;

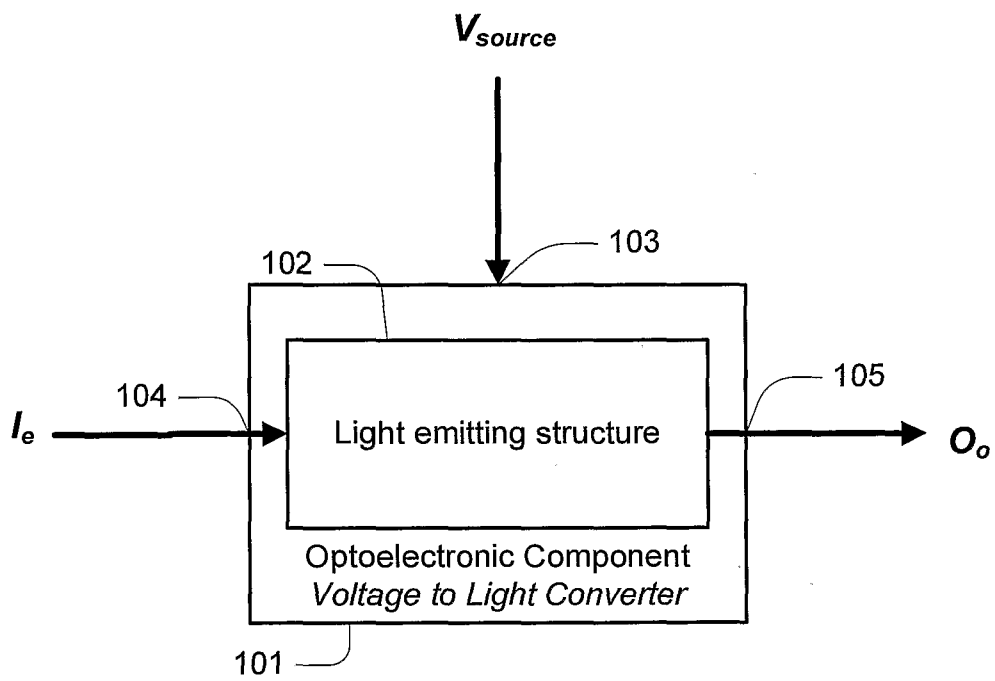
20 an optical processor comprising an array of optical logic elements, wherein the an optical processor is coupled to the VLC array for receiving the optical output signals and processing those thereby to provide further optical output signals; and

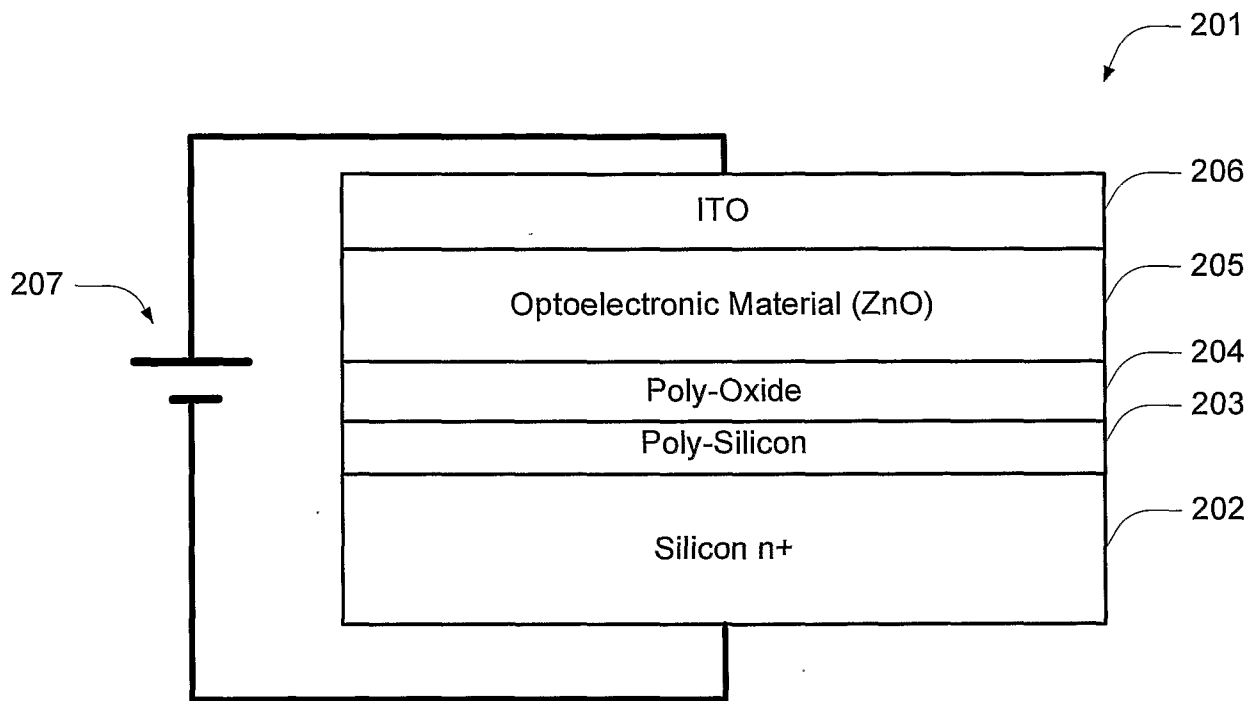
a photo-detector array for converting the further optical output signals to electrical signals.

25 40. An optical/electrical hybrid processor comprising:

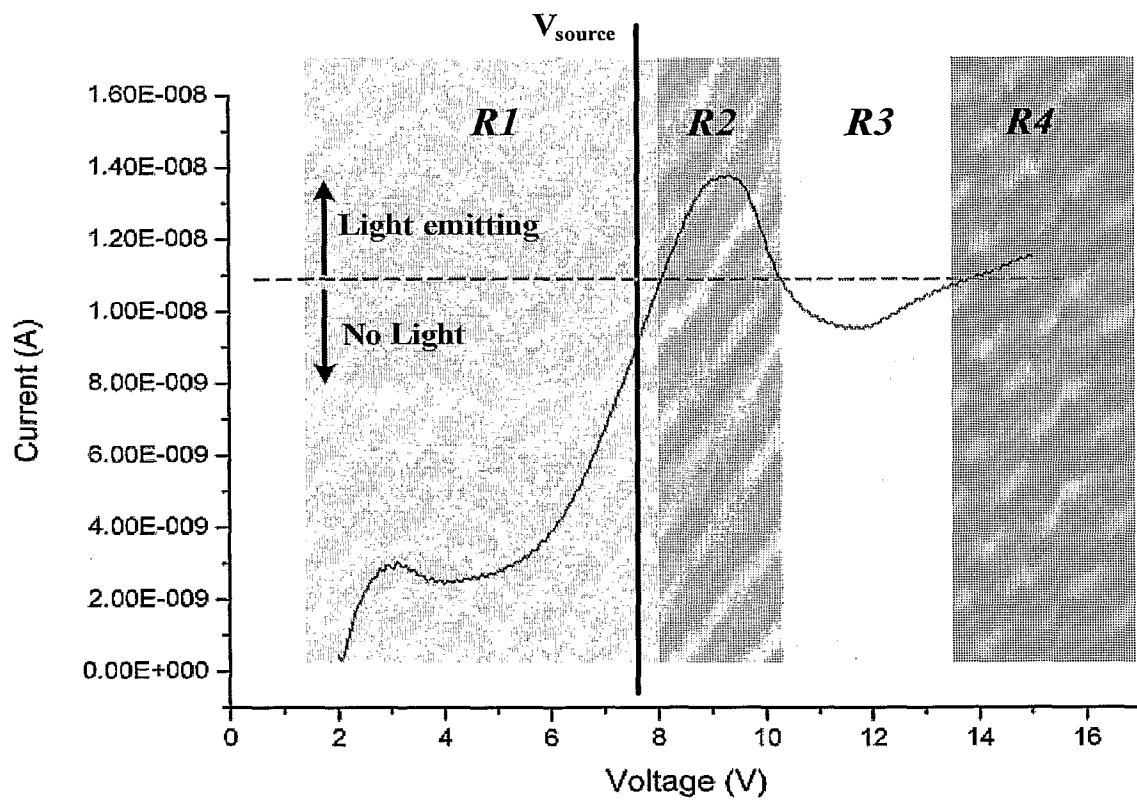
one or more electrical processors coupled an optical processor, wherein the optical processor receives and processes optical signals that are propagated responsive to electrical signals emitted by the electrical processors.

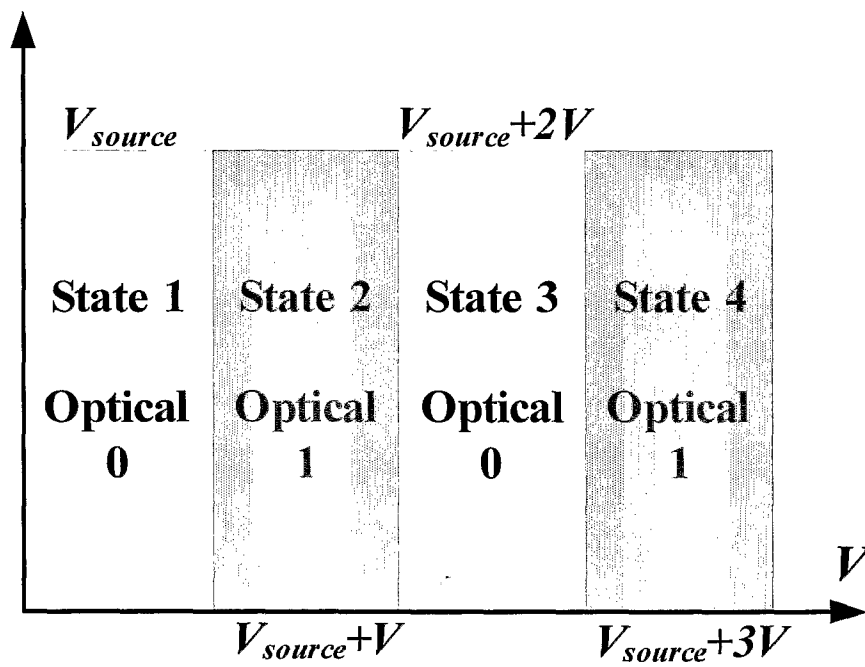
41. An optoelectronic component substantially as herein described with reference to any one of the embodiments of the invention illustrated in the accompanying drawings and/or examples.
42. A method for signal processing substantially as herein described with reference to
5 any one of the embodiments of the invention illustrated in the accompanying drawings and/or examples.
43. An optical/electrical hybrid processor substantially as herein described with reference to any one of the embodiments of the invention illustrated in the accompanying drawings and/or examples.

**FIG. 1**

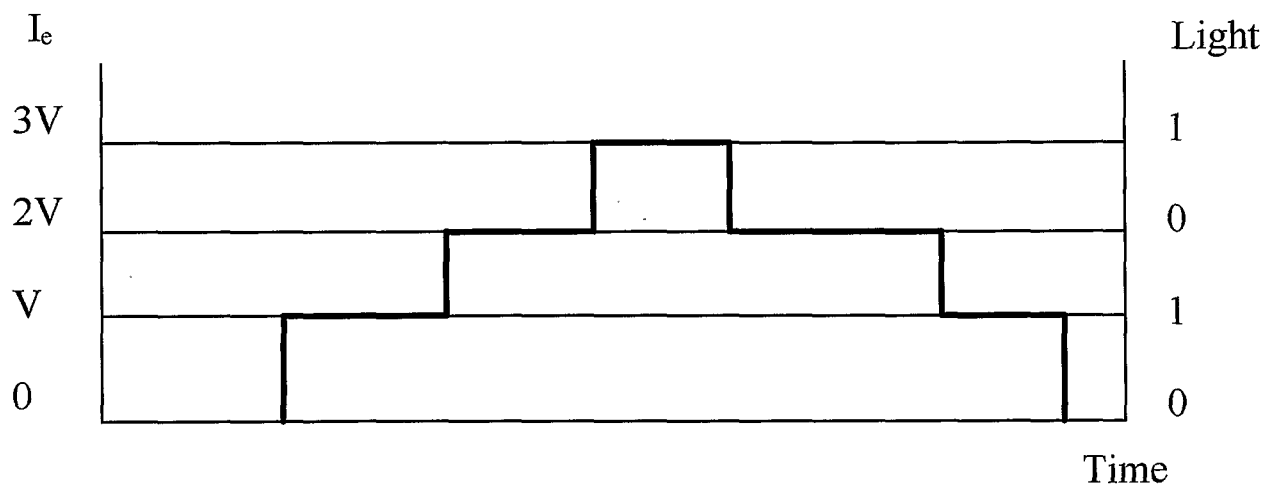
**FIG. 2**

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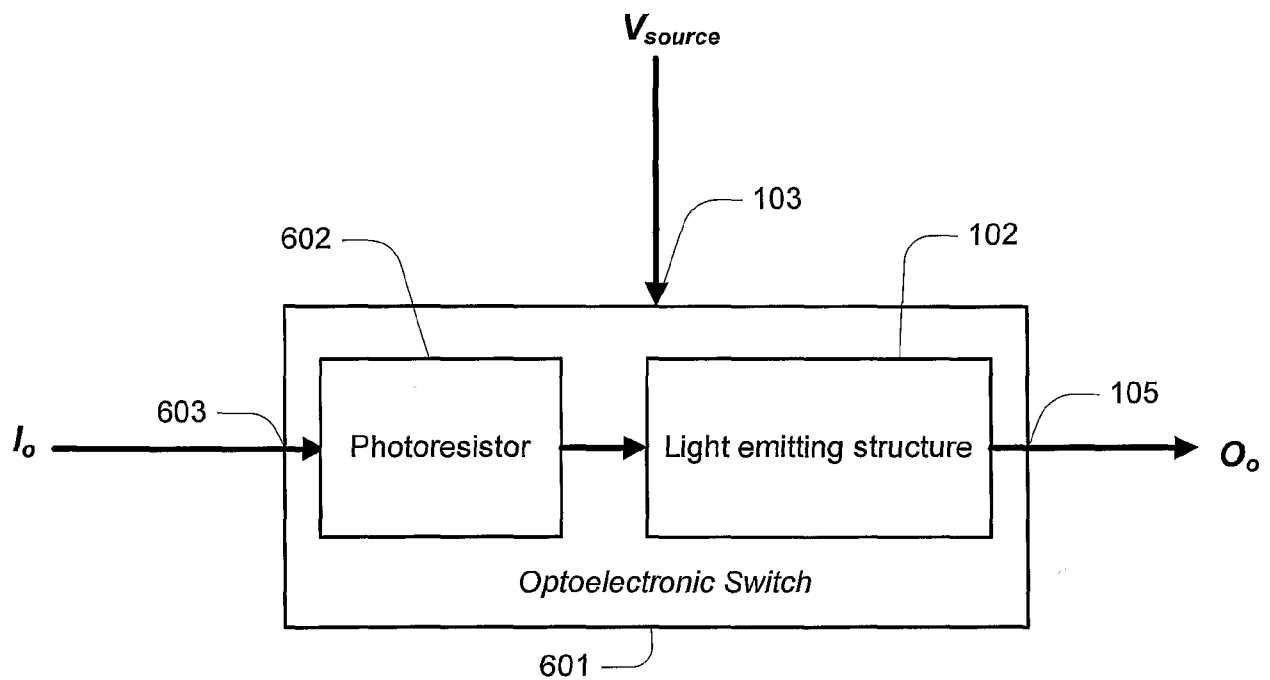
**FIG. 3**

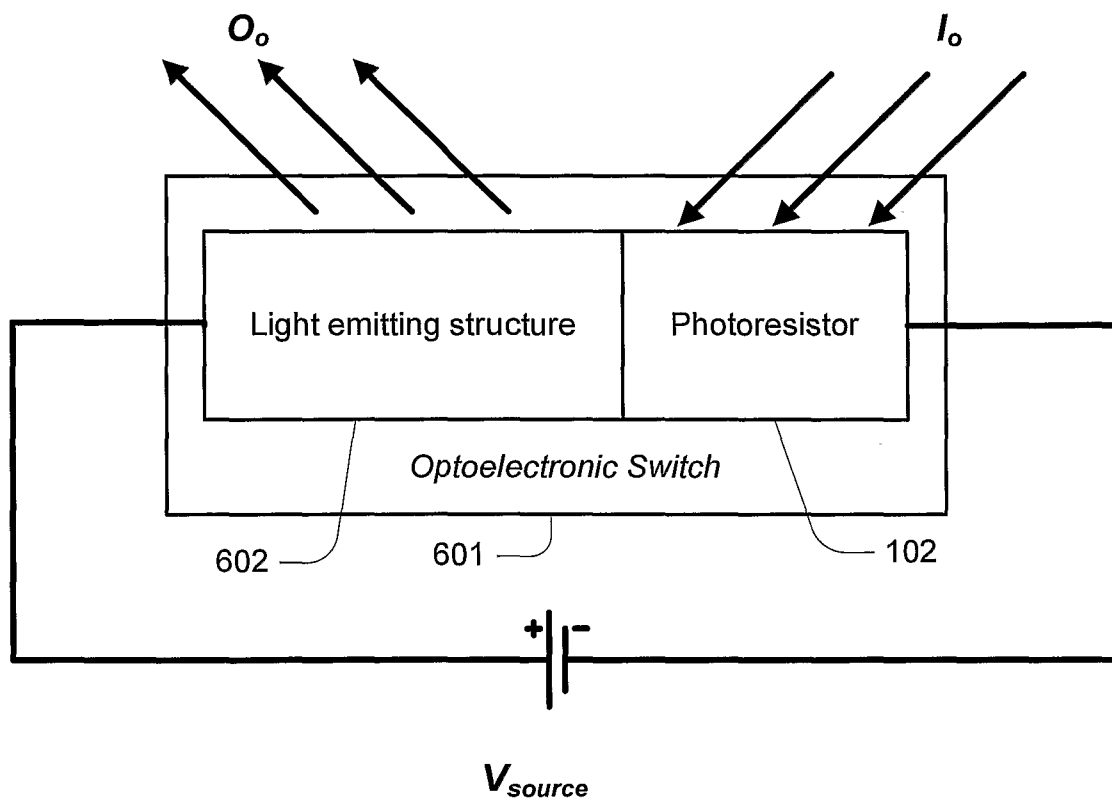
**FIG. 4**

5/27

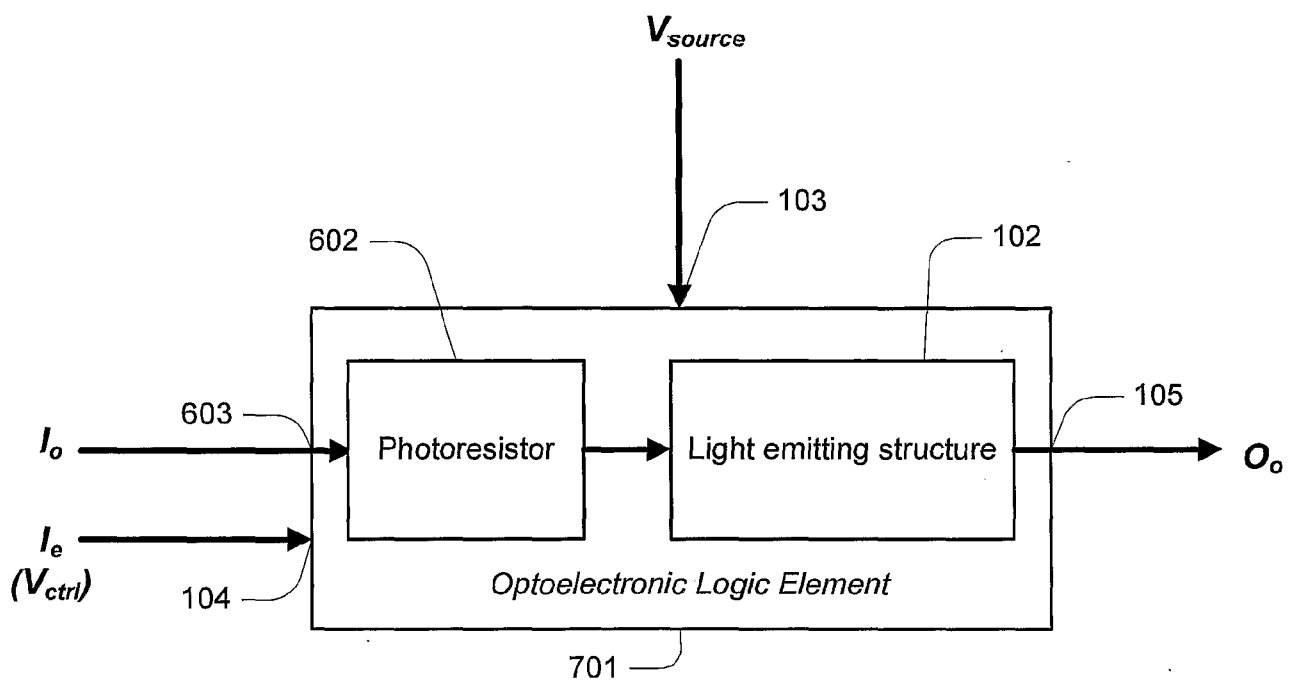
**FIG. 5**

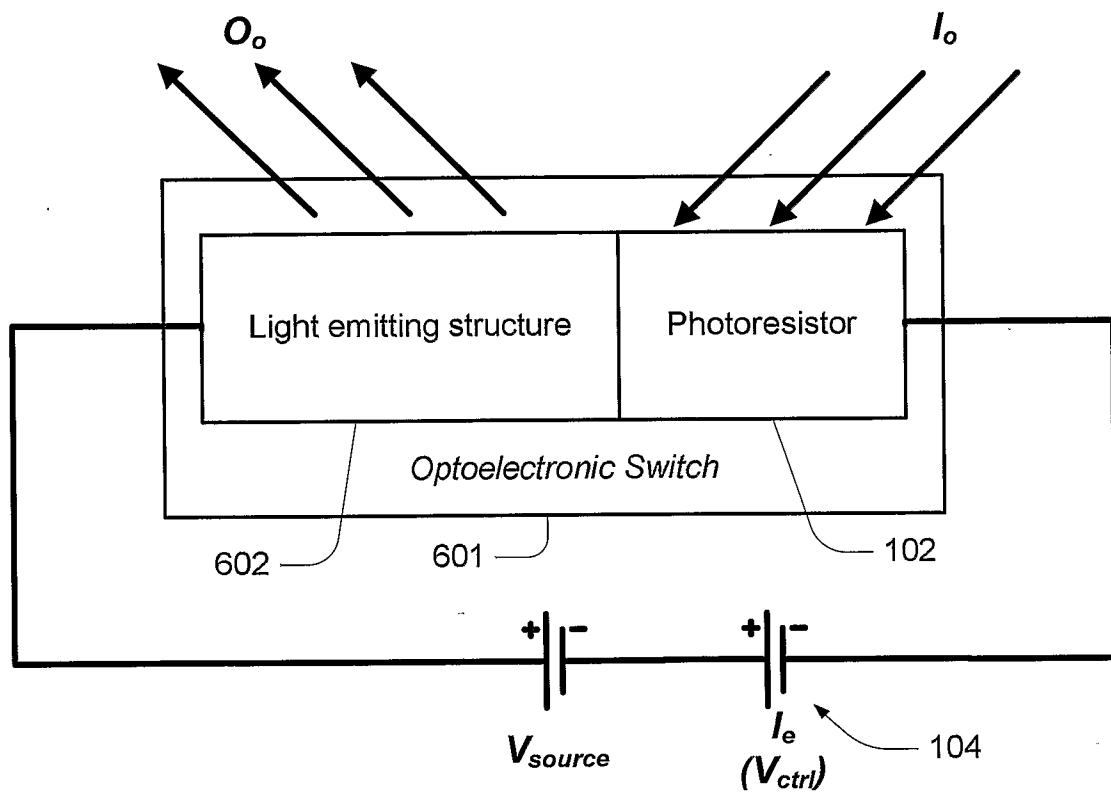
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**FIG. 6A**

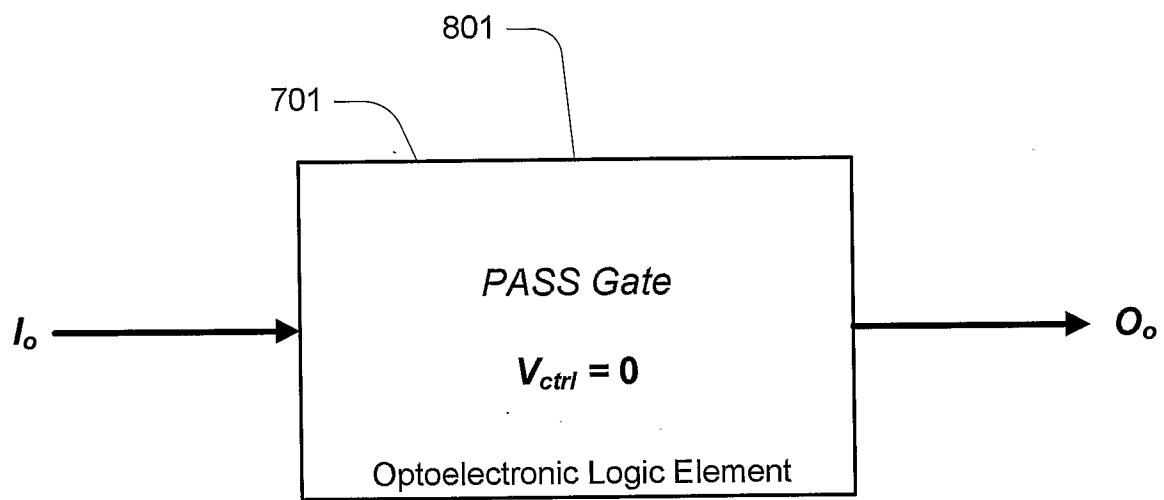
**FIG. 6B**

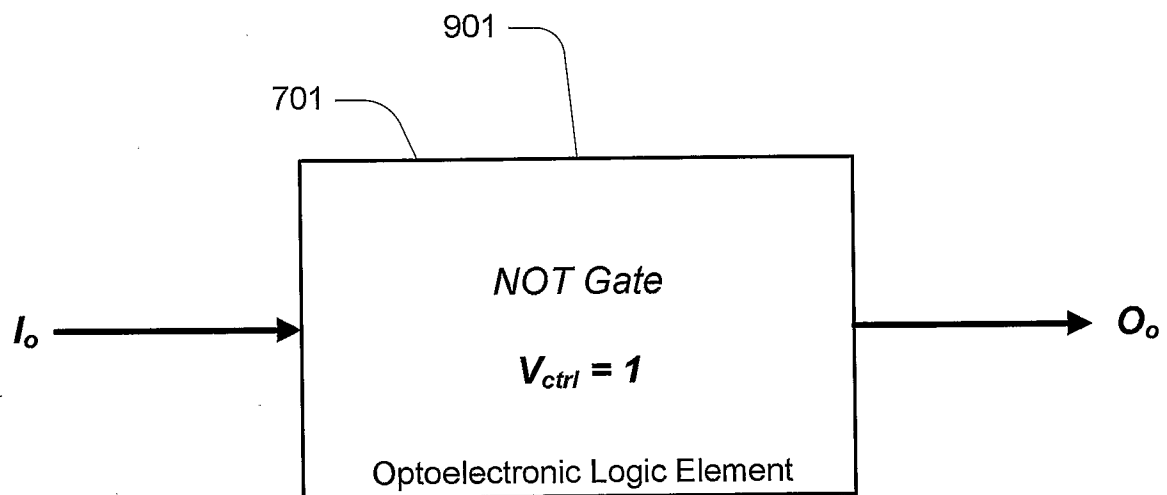
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**FIG. 7A**

**FIG. 7B**

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**FIG. 8**

**FIG. 9**

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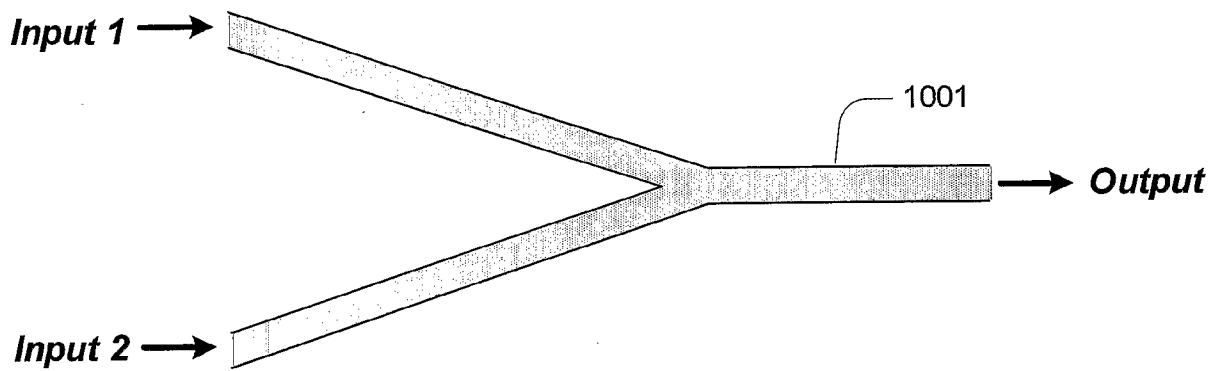
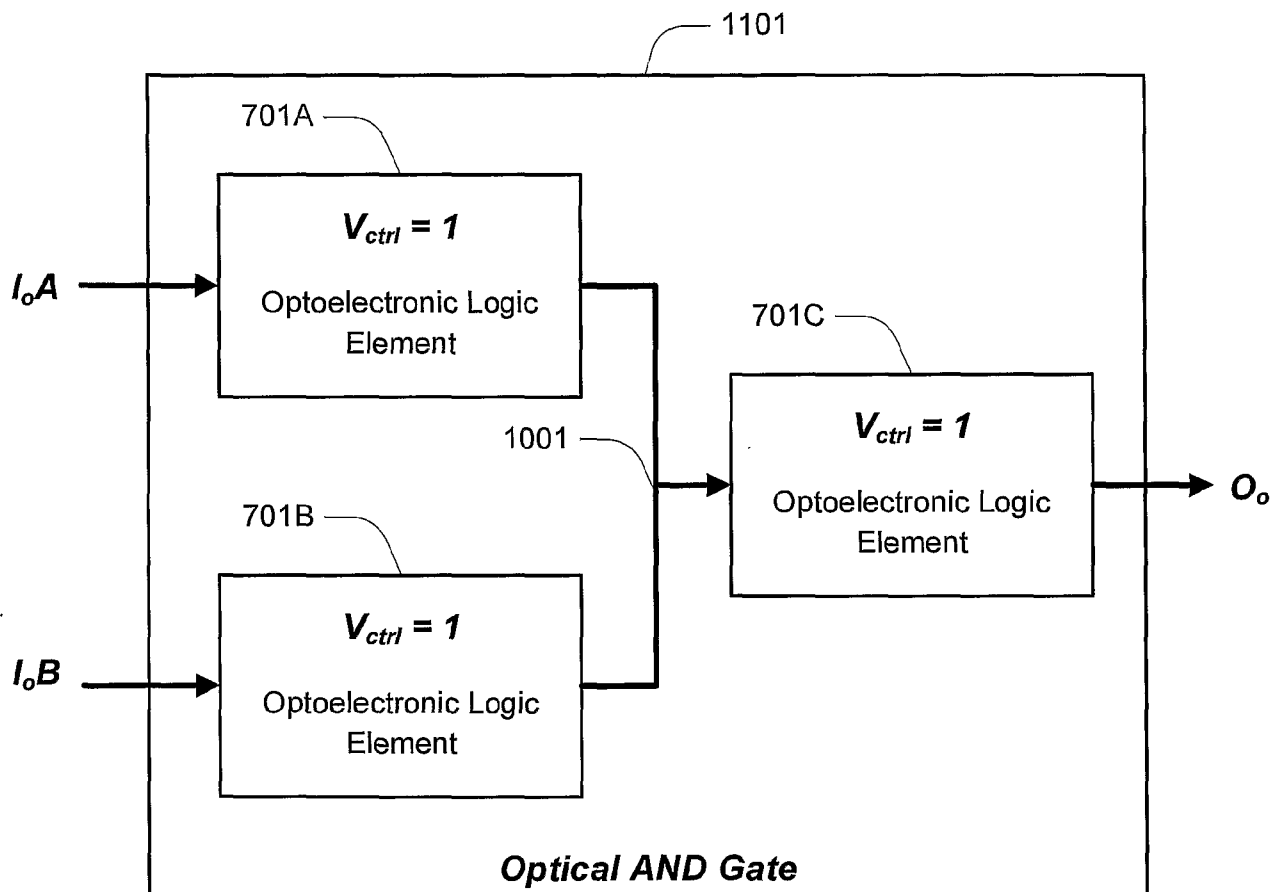
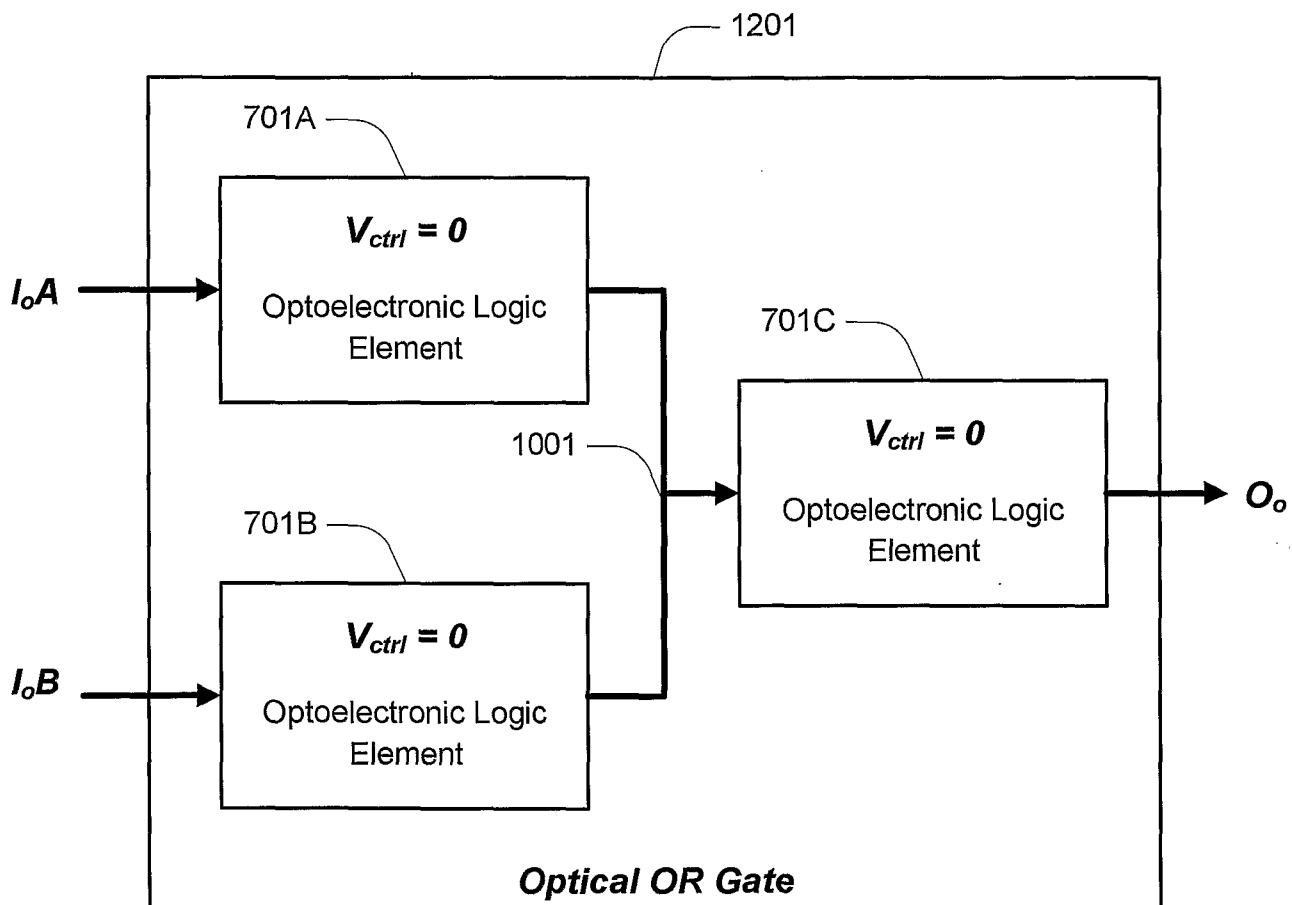


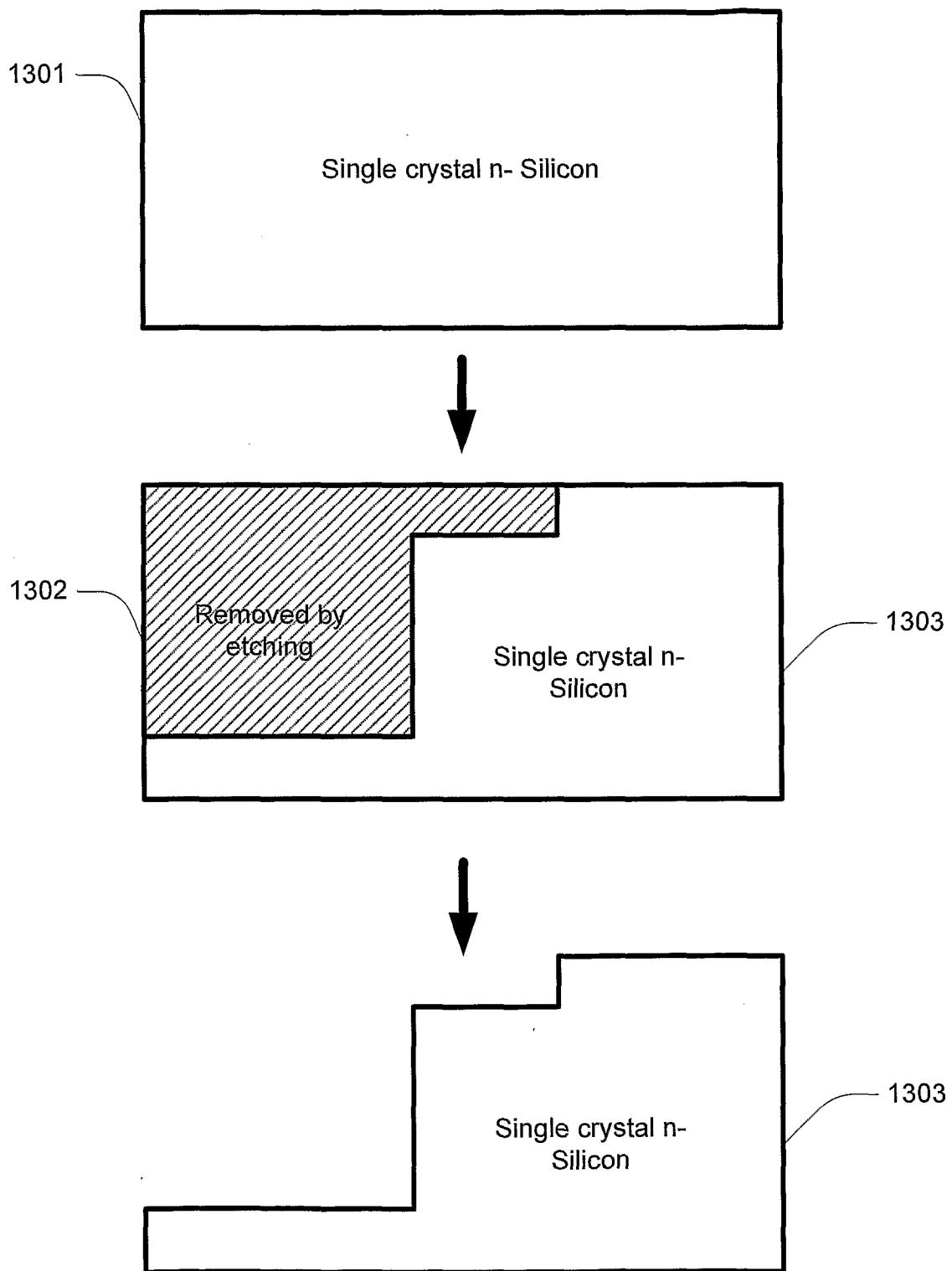
FIG. 10

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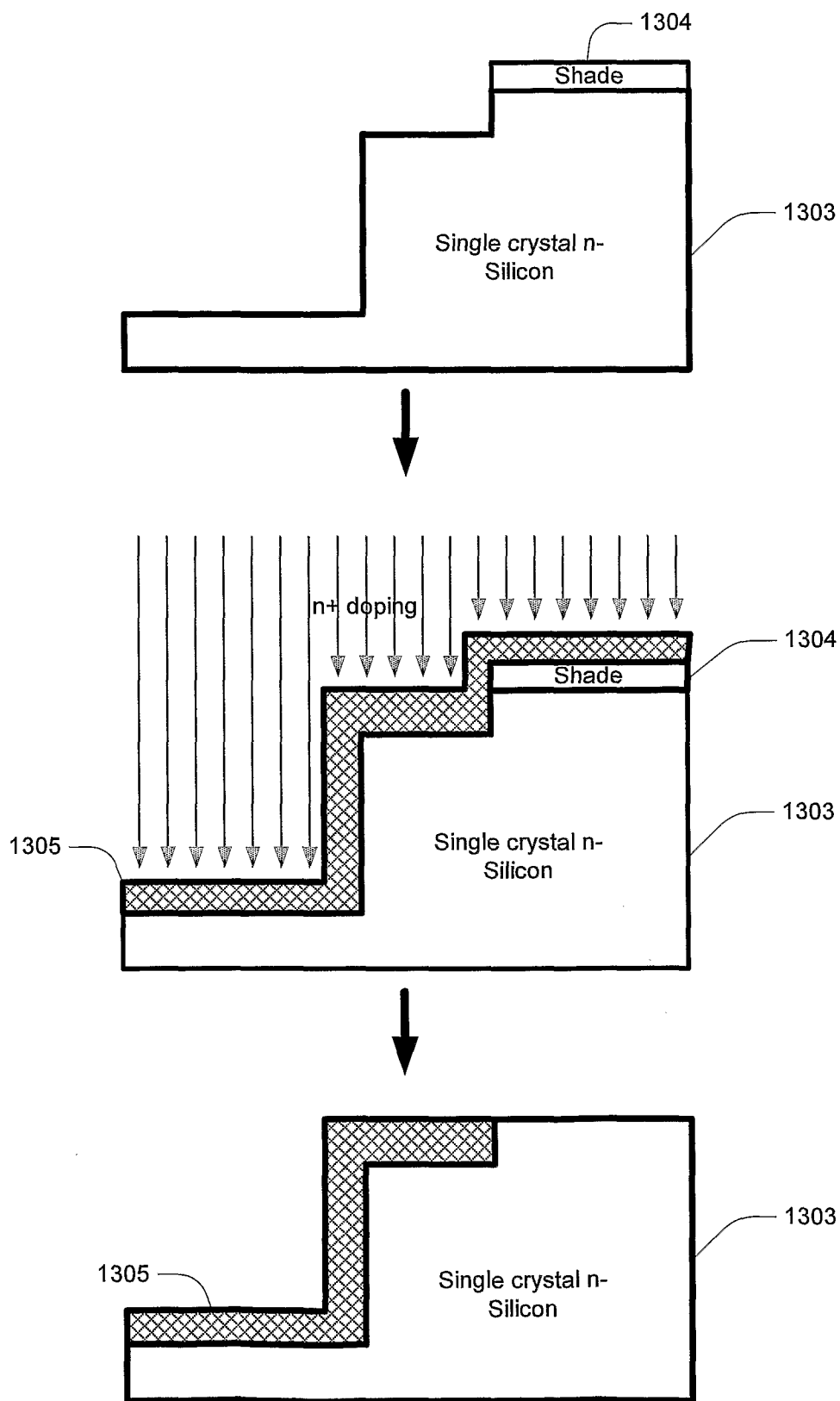
**FIG. 11**

**FIG. 12**

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**FIG. 13A**

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**FIG. 13B**

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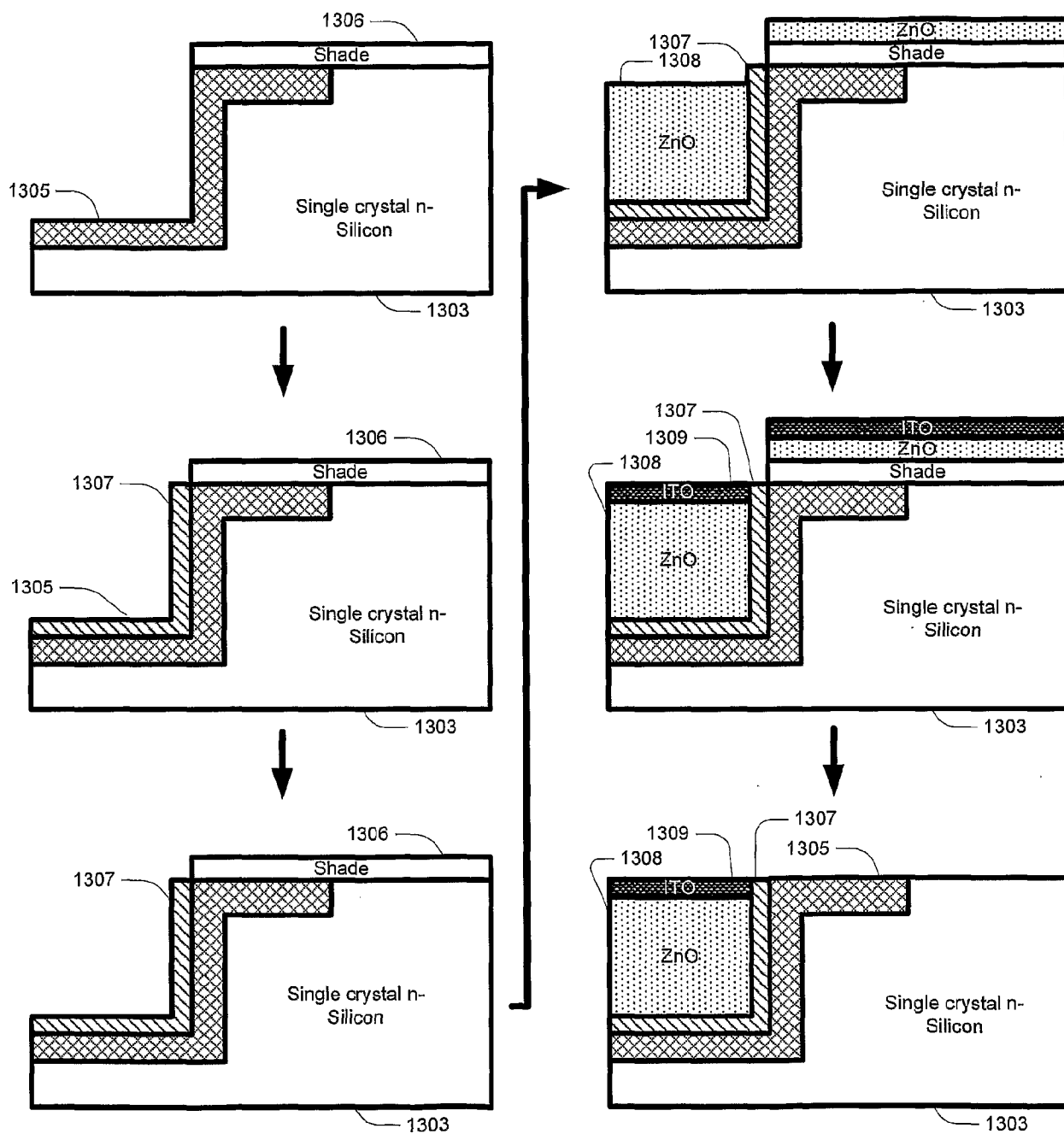


FIG. 13C

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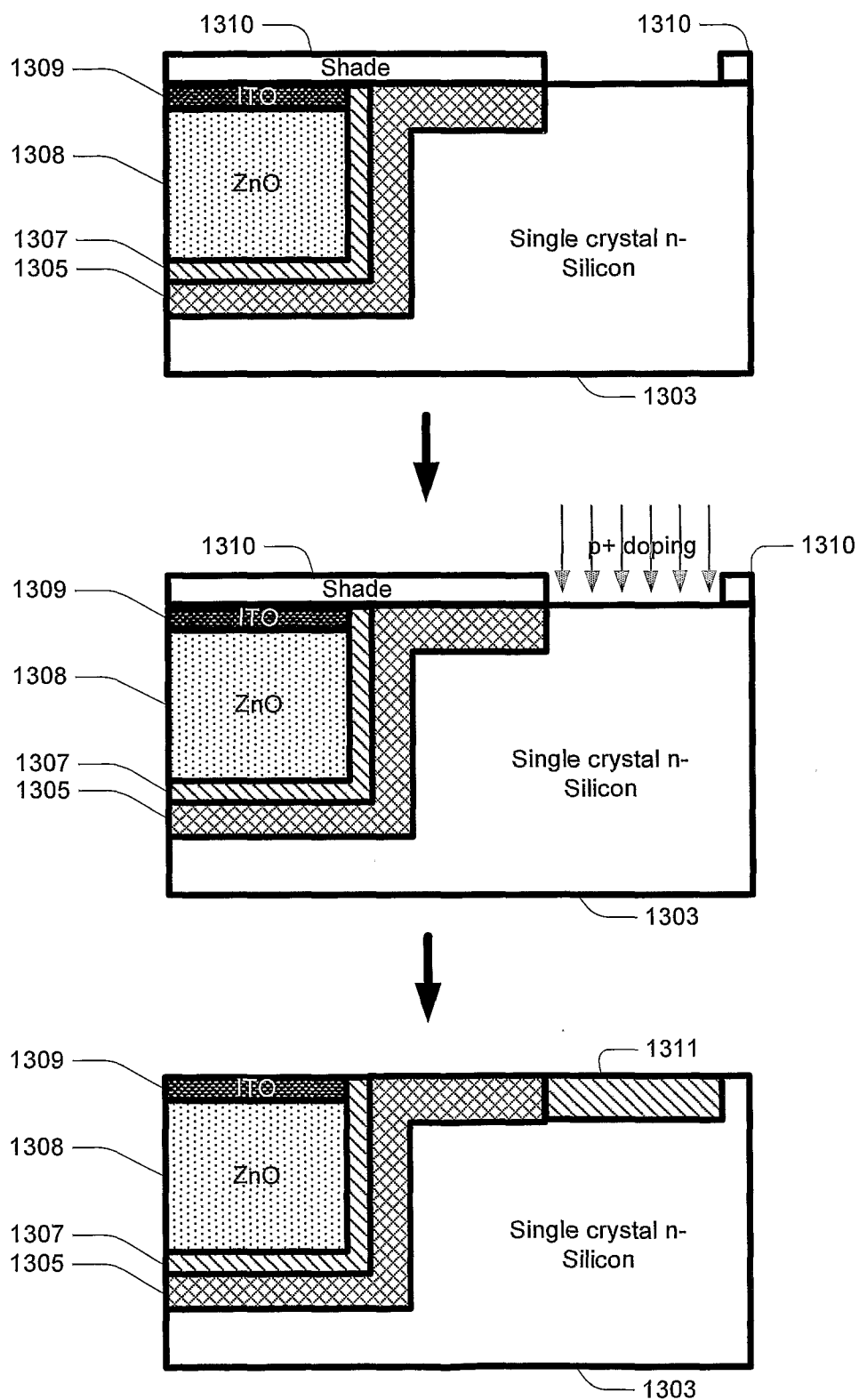
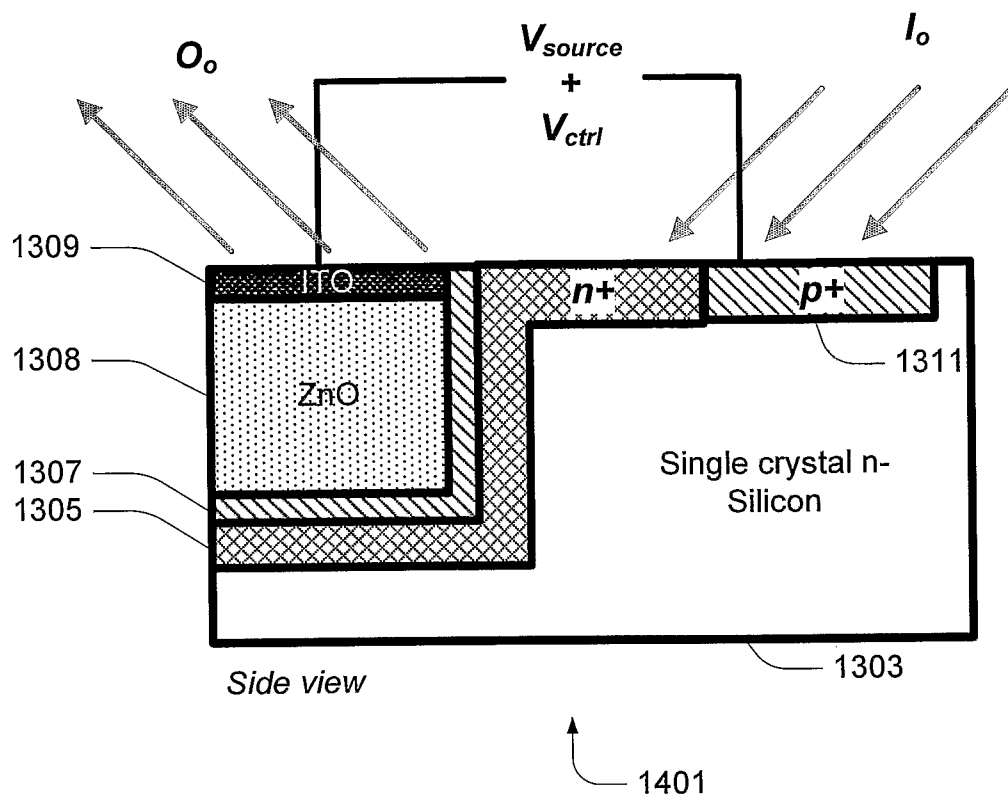
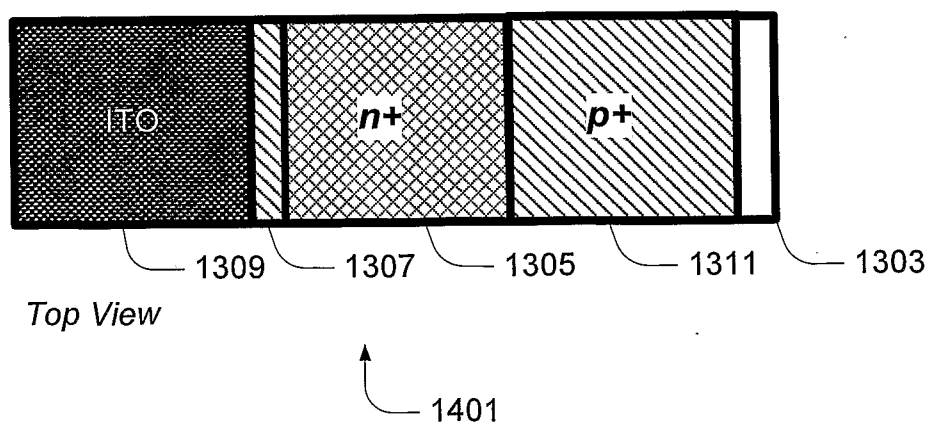


FIG. 13D

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**FIG. 14A****FIG. 14B**

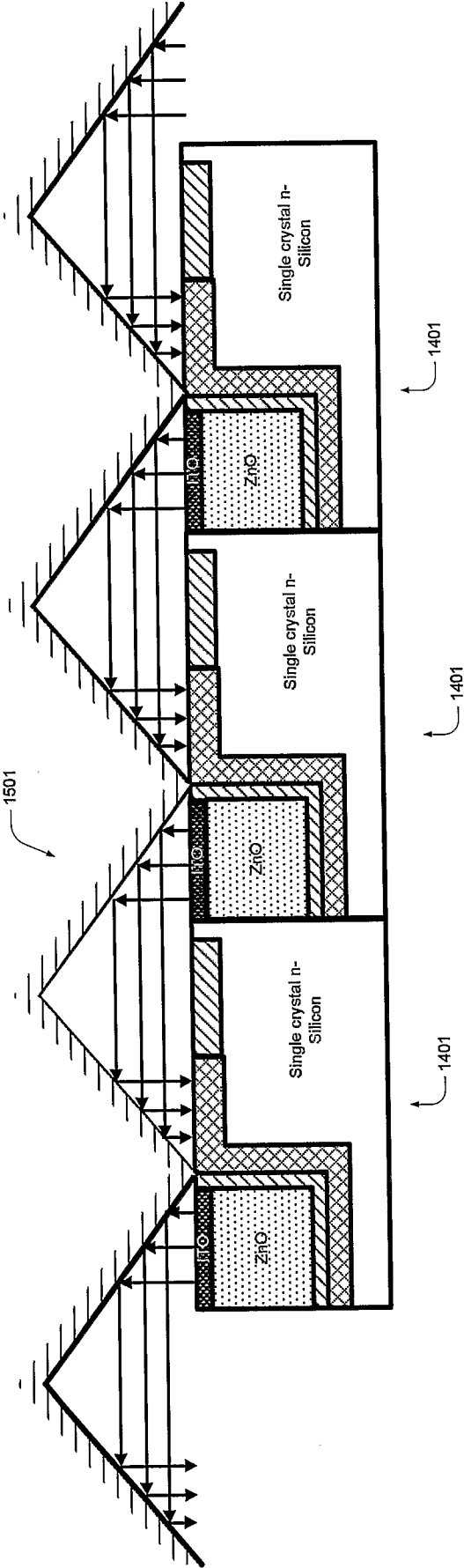


FIG. 15

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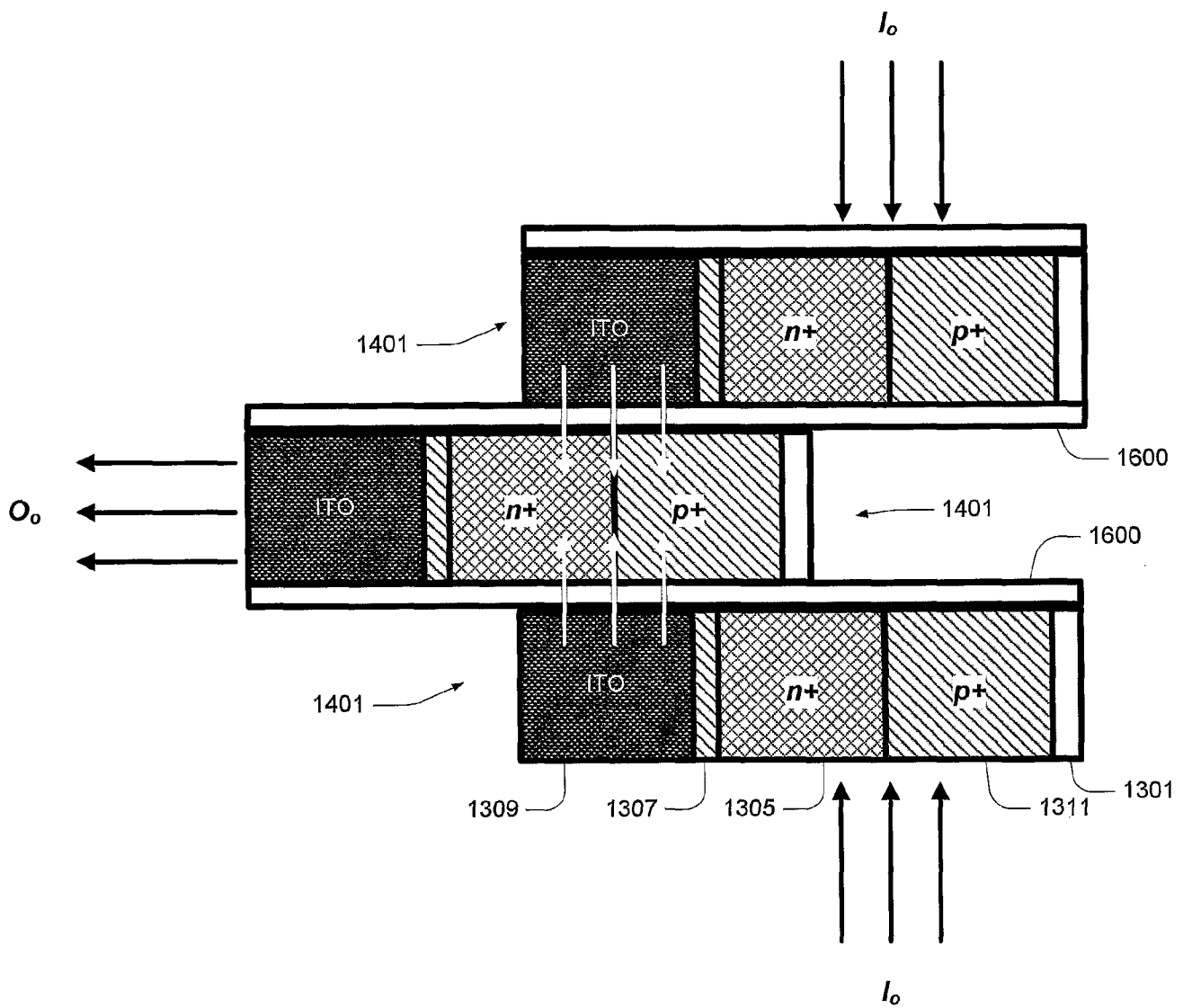
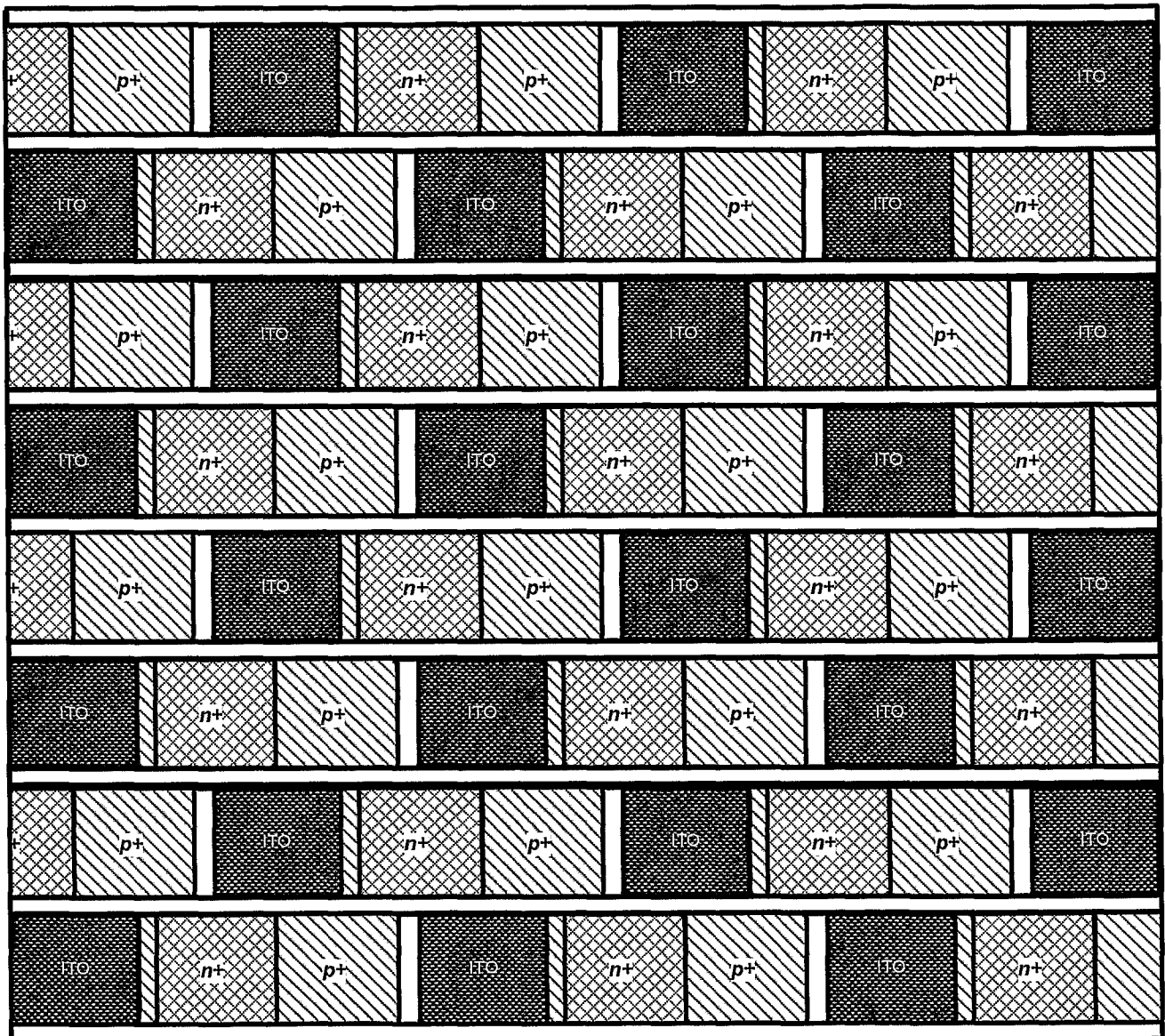
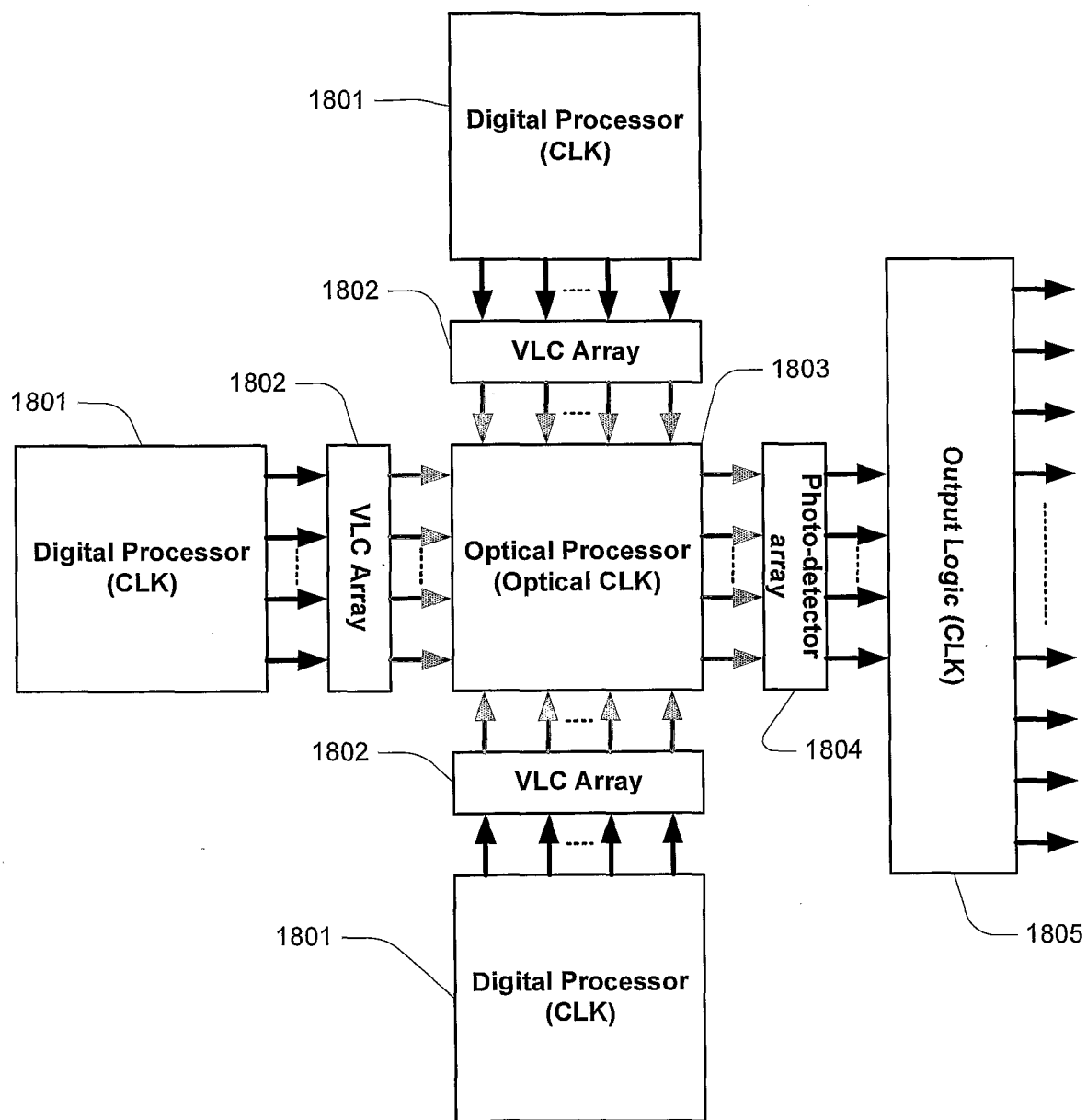


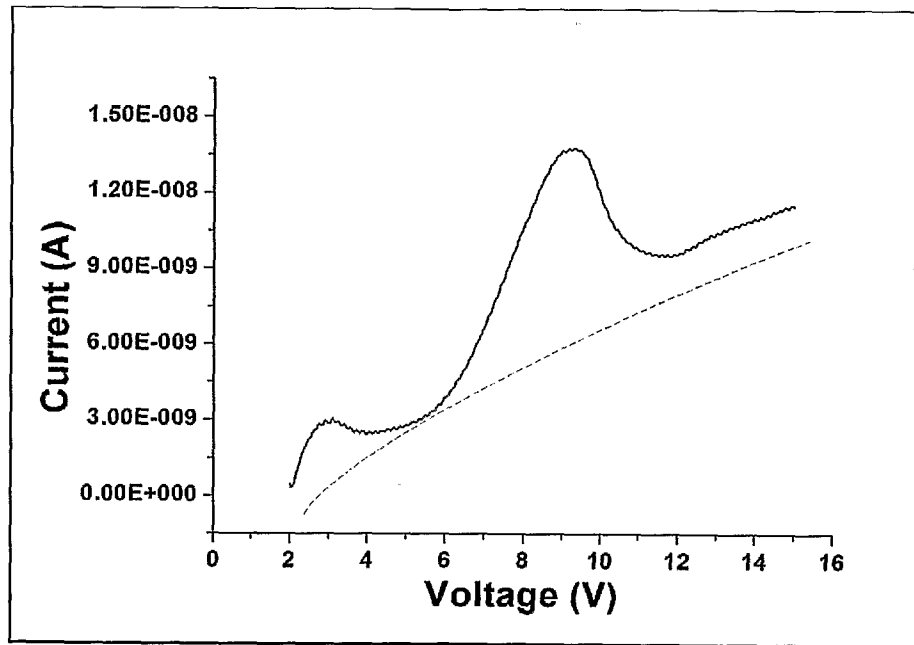
FIG. 16



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FIG. 17

**FIG. 18**

**FIG. 19**

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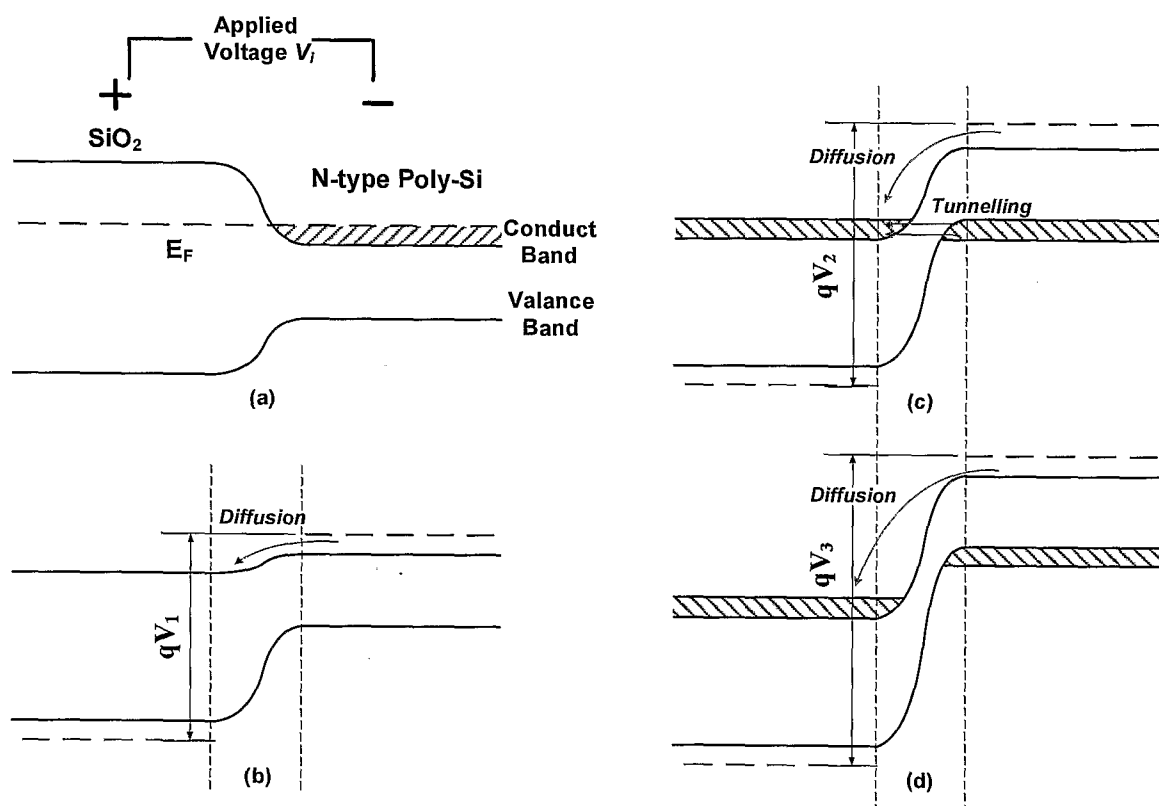
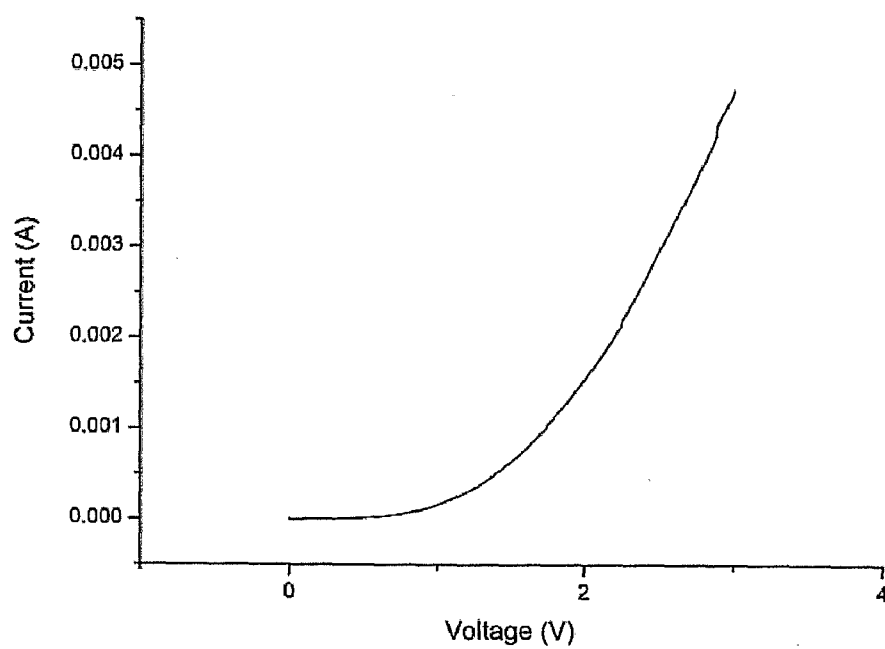
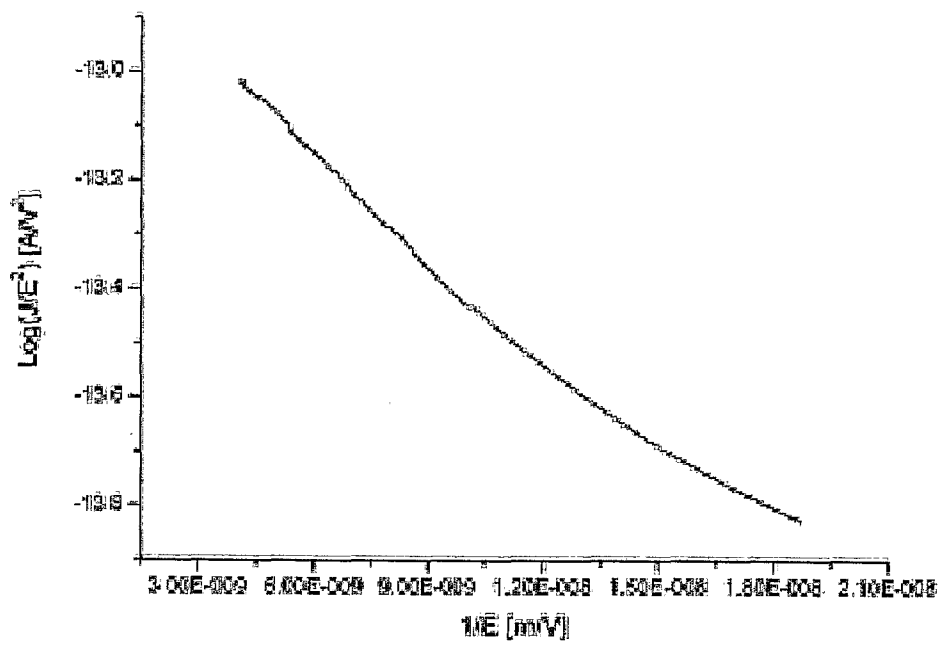


FIG. 20

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**FIG. 21A**

**FIG. 21B**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/NZ2009/000240

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H03K 19/14 (2006.01)

H01L 33/00 (2010.01)

G11C 11/42 (2006.01)

G02F 3/00 (2006.01)

H01L 33/28 (2010.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPOQUE-WPI, EPO keywords: optoelectronic, photonic, LED, OLED, light w emit+, primary, initial, driv+, first, source, input, signal, voltage, plural+, multi+, second+, auxiliary, control+, output, light, optical, radiat+, switch+, logic, gate?, potential, threshold, minimum, add+, combin+, sum+, +silicon, +crystal+

INSPEC: optoelectronic, logic, gate?, comput+, +silicon

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5233556 A (MATSUDA et al.) 3 August 1993 Figs. 1-5, 9, 10; col. 7 line 66-col. 8 line 19; col. 9 lines 26-58; col. 11 lines 35-44	1-12, 16, 36-38
Y	col. 7 lines 1-9	17-35
Y	US 5272355 A (NAMAVAR et al.) 21 December 1993 col. 2 lines 1-10, lines 37-56; col. 5 lines 7-27; col. 6 lines 3-24; col. 7 lines 7-22, 49-55	17-35

☒ Further documents are listed in the continuation of Box C

☒ See patent family annex

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 10 February 2010	Date of mailing of the international search report 17 FEB 2010
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustalia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer STEPHEN EDWARDS AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6225 6108

INTERNATIONAL SEARCH REPORT

International application No.

PCT/NZ2009/000240

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2007042973 A1 (KONIN-KLIJKE PHILIPS ELECTRONICS N.V.) 19 April 2007 See abstract, Fig. 3, 5	

INTERNATIONAL SEARCH REPORT

International application No.

PCT/NZ2009/000240

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: **41-43**
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
The claims do not comply with Rule 6.2(a) because they rely on references to the description and/or drawings.

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

(see additional sheet)

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.: **1-38**

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/NZ2009/000240

Supplemental Box

(To be used when the space in any of Boxes I to IV is not sufficient)

Continuation of Box No: III

This International Application does not comply with the requirements of unity of invention because it does not relate to one invention or to a group of inventions so linked as to form a single general inventive concept.

In assessing whether there is more than one invention claimed, I have given consideration to those features which can be considered to potentially distinguish the claimed combination of features from the prior art. Where different claims have different distinguishing features they define different inventions.

This International Searching Authority has found that there are different inventions as follows:

- Claims 1-38 are directed towards an optoelectronic component comprising a light emitting structure, and wherein a source voltage signal and at least one control voltage signal is applied to modify the overall voltage signal applied to the light emitting structure such that an optical output signal is generated under various operating states.

It is considered that *applying a source voltage and at least one control voltage to a light emitting structure in the manner described* comprises a first distinguishing feature.

- Claims 39 and 40 are directed towards an optical/electrical hybrid processor comprising a number of electrical processors generating electrical signals and which are coupled to an optical processor, wherein optical signals responsive to the electrical signals emitted are processed.

It is considered that *an optical/electrical hybrid processor with the defined configuration of multiple electrical processors and an optical processor* comprises a second distinguishing feature.

PCT Rule 13.2, first sentence, states that unity of invention is only fulfilled when there is a technical relationship among the claimed inventions involving one or more of the same or corresponding special technical features. PCT Rule 13.2, second sentence, defines a special technical feature as a feature which makes a contribution over the prior art.

Each of the abovementioned groups of claims has a different distinguishing feature and they do not share any feature which could satisfy the requirement for being a special technical feature. Because there is no common special technical feature it follows that there is no technical relationship between the identified inventions. Therefore the claims do not satisfy the requirement of unity of invention *a priori*.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/NZ2009/000240

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report				Patent Family Member			
US	5233556	JP	4245680	JP	4323708		
US	5272355	NONE					
WO	2007042973	CN	101283392	EP	1938301	KR	20080063303
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.							
END OF ANNEX							