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(54) **LAYOUT METHOD FOR SOFT-ERROR HARD ELECTRONICS, AND RADIATION HARDENED LOGIC CELL**

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(57) **ABSTRACT**

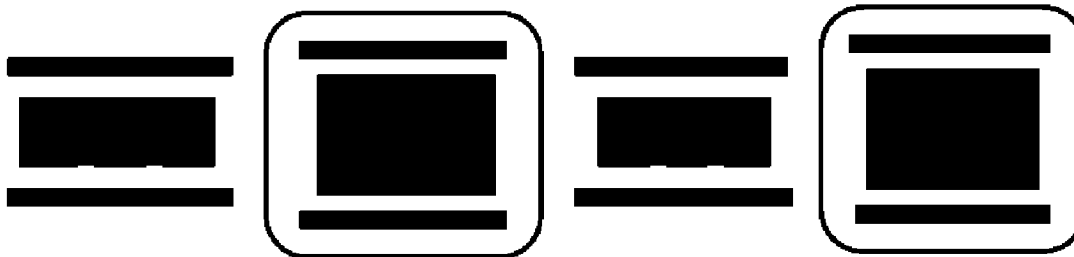
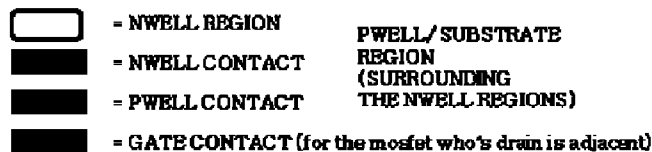
This invention comprises a layout method to effectively protect logic circuits against soft errors (non-destructive errors) and circuit cells, with layout, which are protected against soft errors. In particular, the method protects against cases where multiple nodes in circuit are affected by a single event. These events lead to multiple errors in the circuit, and while several methods exist to deal with single node errors, multiple node errors are very hard to deal with using any currently existing protection methods. The method is particularly useful for CMOS based logic circuits in modem technologies ( $\leq 90$  nm), where the occurrence of multiple node pulses becomes high (due to the high integration level). It uses a unique layout configuration, which makes the circuits protected against single event generated soft-errors.

(21) Appl. No.: **12/354,655**

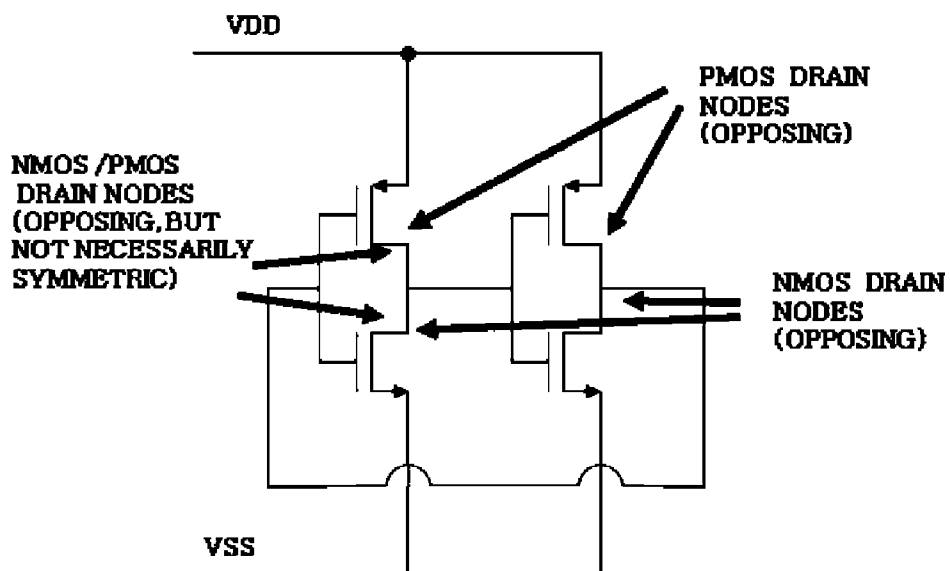
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**Related U.S. Application Data**

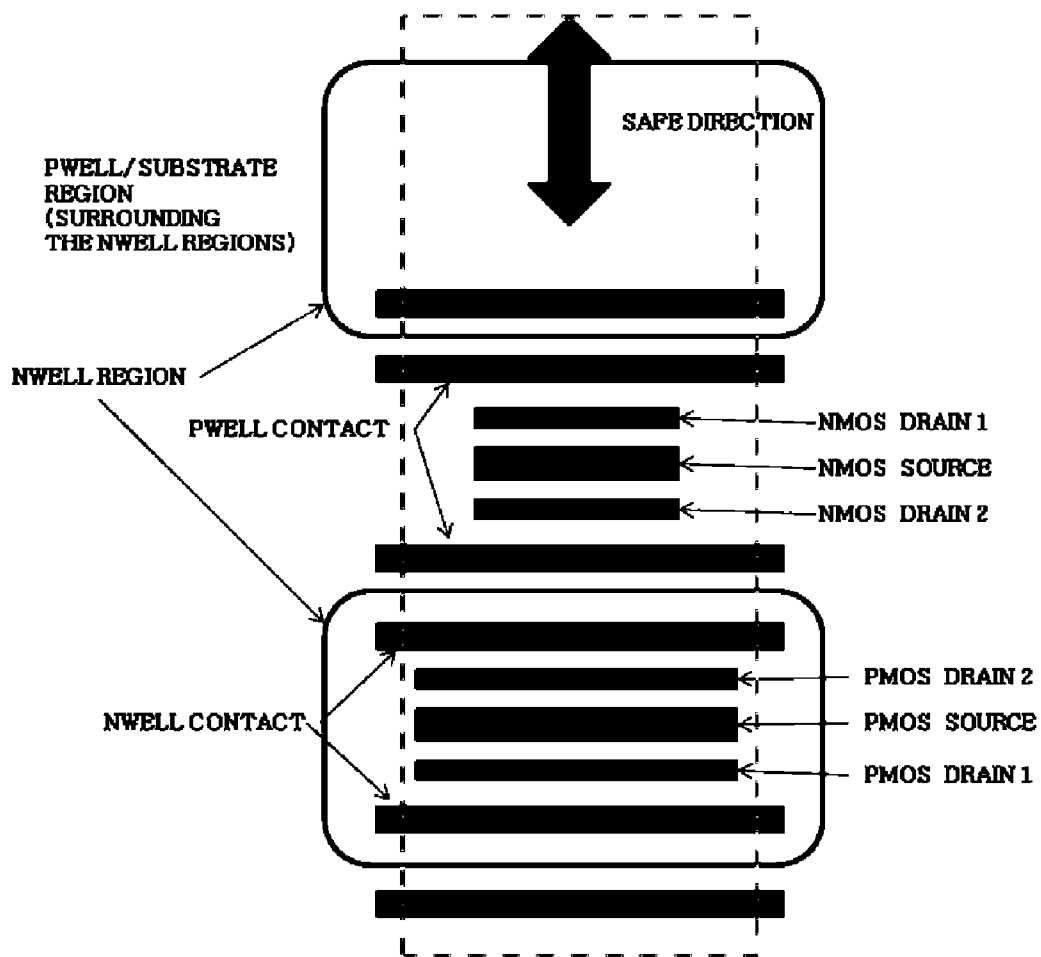
(60) Provisional application No. 61/011,599, filed on Jan. 17, 2008, provisional application No. 61/011,989, filed on Jan. 22, 2008, provisional application No. 61/068,483, filed on Mar. 7, 2008, provisional application No. 61/123,003, filed on Apr. 5, 2008.



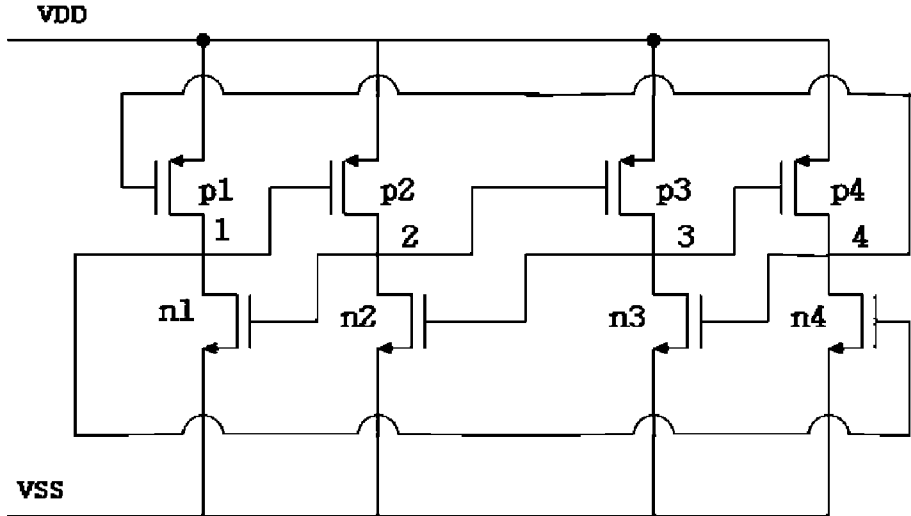
*A first preferred layout arrangement for the layout of the DICE latch cell. ns/ps are the source contacts for the two mosfets who's drains are adjacent. ). p1-p4 and n1-n4 are the pMOSFET drains and the nMOSFET drains of the 4 main storage nodes, respectively. Any cyclic simultaneous permutation of the n and p nodes will be equivalent (and part of the invention). The mosfets can be placed in separate active areas, or the adjacent n and p nodes can be placed in the same active area. The MOSFET sources can be placed in the line of the drains or in the direction vertical to the line of the drain nodes. The well contacts can be placed on either side only, or also surround the adjacent node pairs. The nodes can also be arranged in a different order subject to the following rules: two adjacent n-drains, or two adjacent p-drains are always an odd/even pair (e.g., p1 & p2, or n2 and n3), adjacent n-drain to p-drain are always an odd/odd or and even/even pair (e.g., n2 & p2, or p3 & n1).*



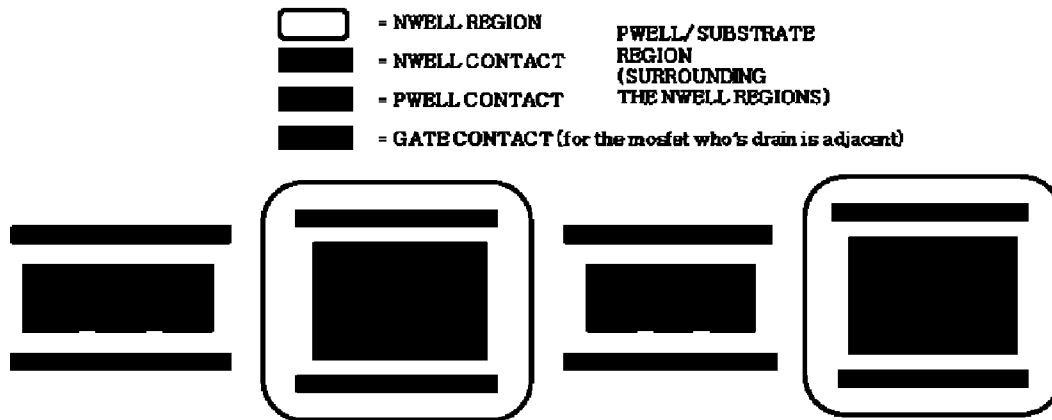
*Drawing 1. Primary opposing nodes, with respect to the state of the latch, in a latch cell.*



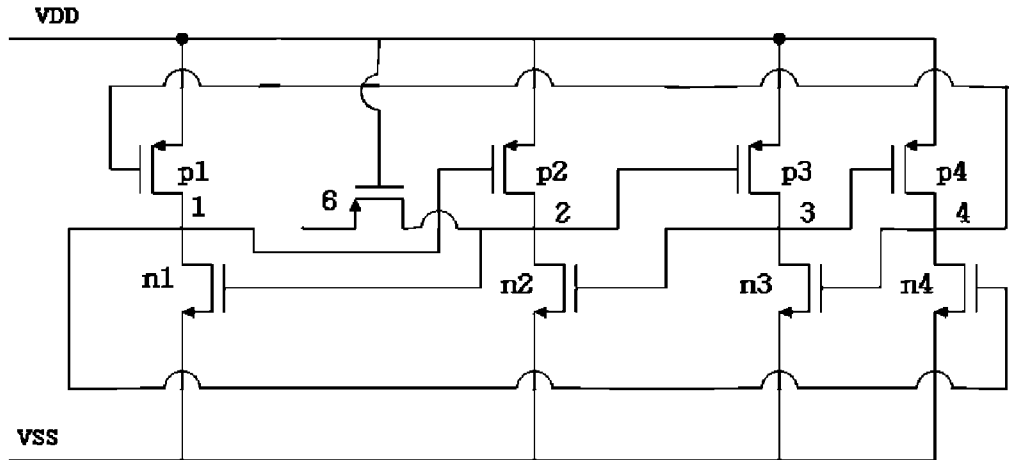
*Drawing 2. An example of a layout arrangement of opposing node of a latch circuit (the drain1's connected to one of the net, and the drain2's connected to the other net, which has the inverse voltage state of the first net).*



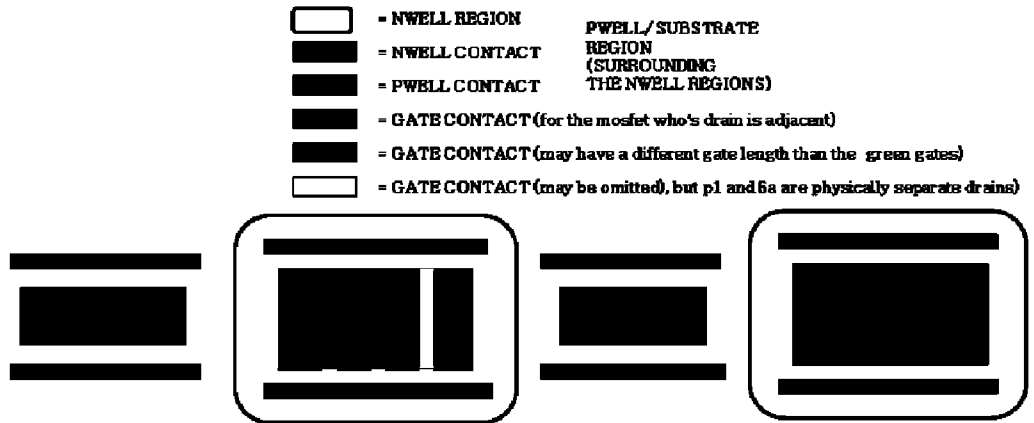
Drawing 3. Basic netlist for the DICE latch cell (prior art [Nic05]) with nodes 1-4. p1-p4 and n1-n4 are the pMOSFET drains and the nMOSFET drains, respectively.



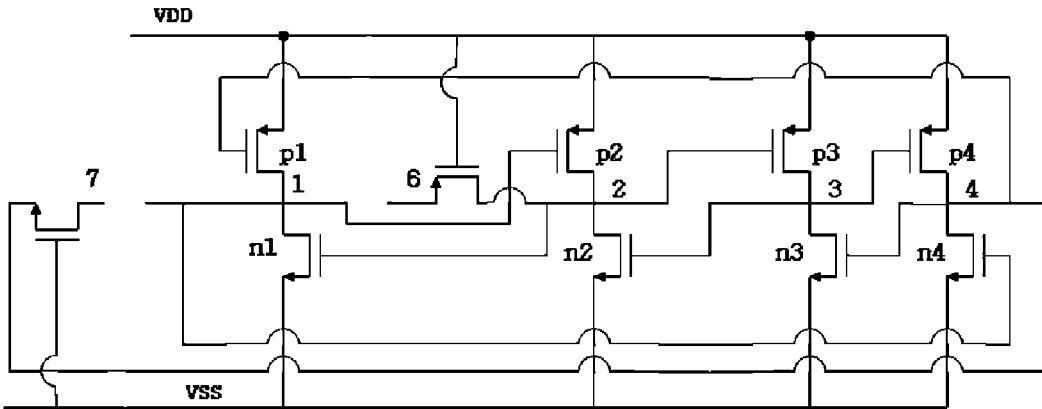
Drawing 4. A first preferred layout arrangement for the layout of the DICE latch cell. ns/ps are the source contacts for the two mosfets who's drains are adjacent. ). p1-p4 and n1-n4 are the pMOSFET drains and the nMOSFET drains of the 4 main storage nodes, respectively. Any cyclic simultaneous permutation of the n and p nodes will be equivalent (and part of the invention). The mosfets can be placed in separate active areas, or the adjacent n and p nodes can be placed in the same active area. The MOSFET sources can be placed in the line of the drains or in the direction vertical to the line of the drain nodes. The well contacts can be placed on either side only, or also surround the adjacent node pairs. The nodes can also be arranged in a different order subject to the following rules: two adjacent n-drains, or two adjacent p-drains are always an odd/even pair (e.g., p1 & p2, or n2 and n3), adjacent n-drain to p-drain are always an odd/odd or and even/even pair (e.g., n2 & p2, or p3 & n1).



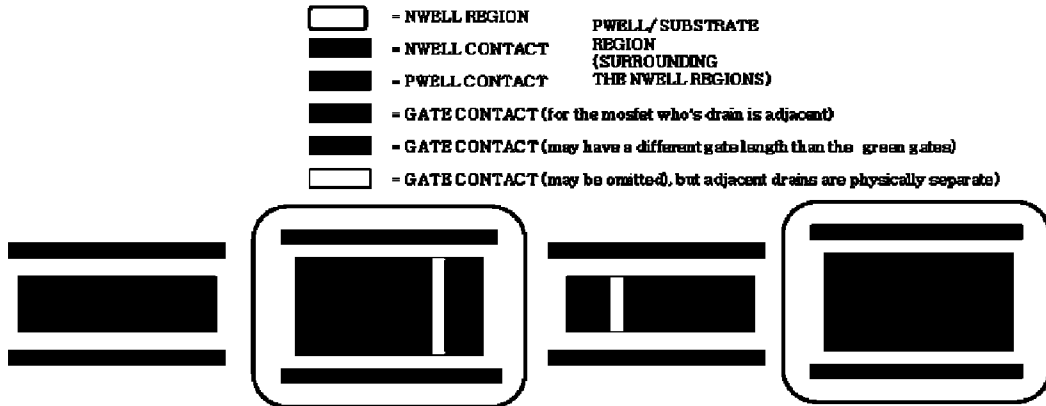
Drawing 5. Net-list corresponding to the second preferred arrangement. The yellow MOSFET may or may not be included, as long as node 6 is connected to drain 6a in drawing 5, and p1 and 6a are physically separate.



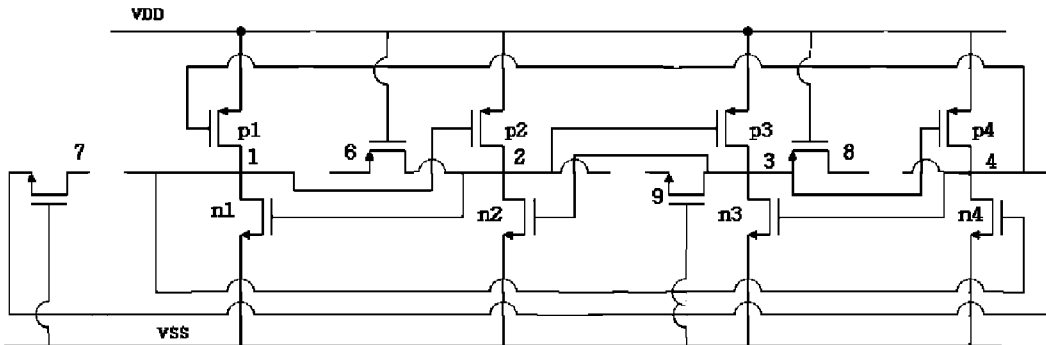
Drawing 6. A second preferred layout arrangement. ns/ps are the source contacts for the two mosfets who's drains are adjacent. Node 6a and 6b are connected. The yellow gate adjacent to node 6a may or may not be included (both variants included in the claims), but p1 and 6a are physically separate. The layout derives from the layout in drawing 1, and the same variants w.r.t. node permutations, active, source, and well contact arrangements apply.



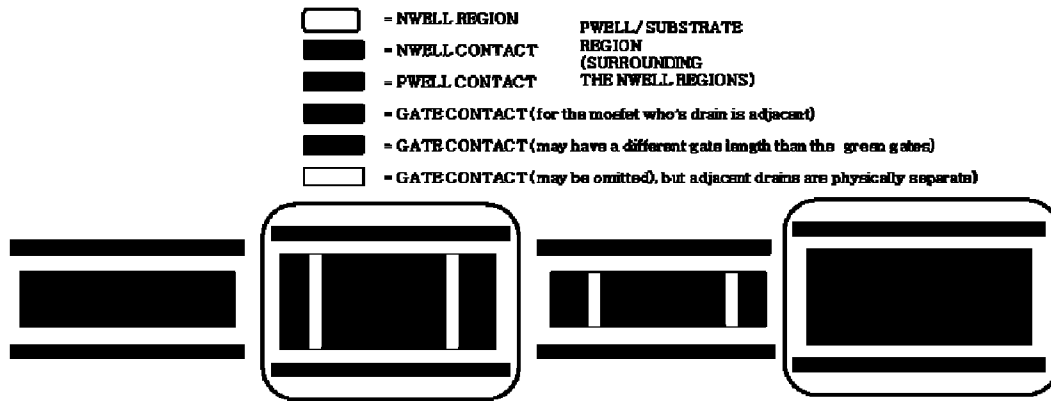
Drawing 7. Net-list corresponding to the third preferred arrangement. The yellow MOSFET may or may not be included, as long as node 6 is connected to drain 6a in drawing 4, and p1 and 6a are physically separate, and node 7 is connected to drain 7a in drawing 4, and n1 and 7a are physically separate.



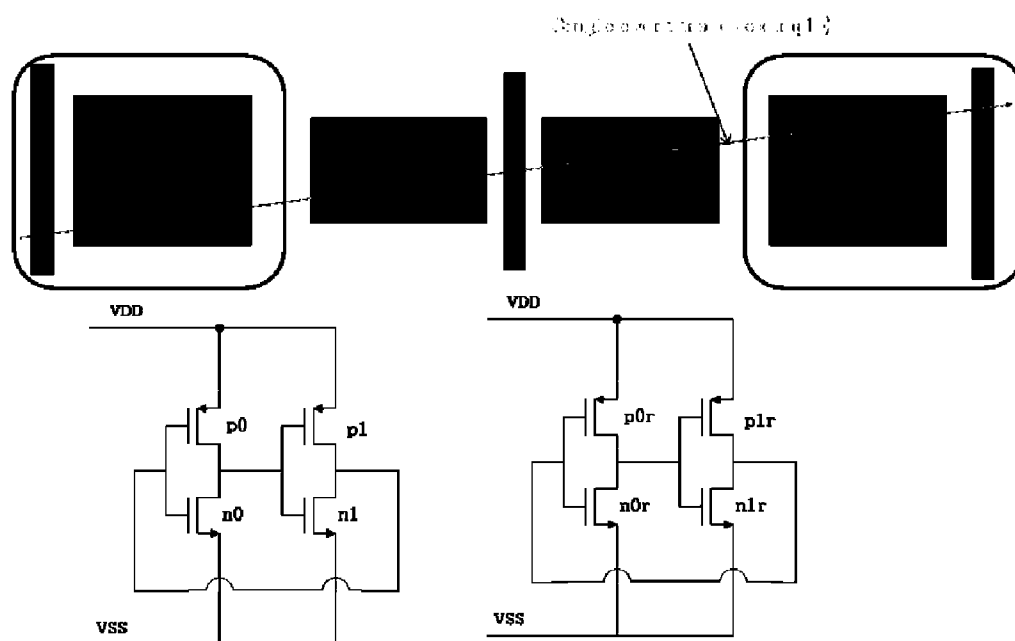
Drawing 8. A third preferred layout arrangement. ns/ps are the source contacts for the two mosfets who's drains are adjacent. Node 6a-6b are connected, as are node 7a/7b. The yellow gate adjacent to node 6a and 7a may or may not be included (both variants included in the claims), but the adjacent drain areas are physically separate. The layout derives from the layout in drawing 1, and the same variants w.r.t. node permutations, active, source, and well contact arrangements apply.



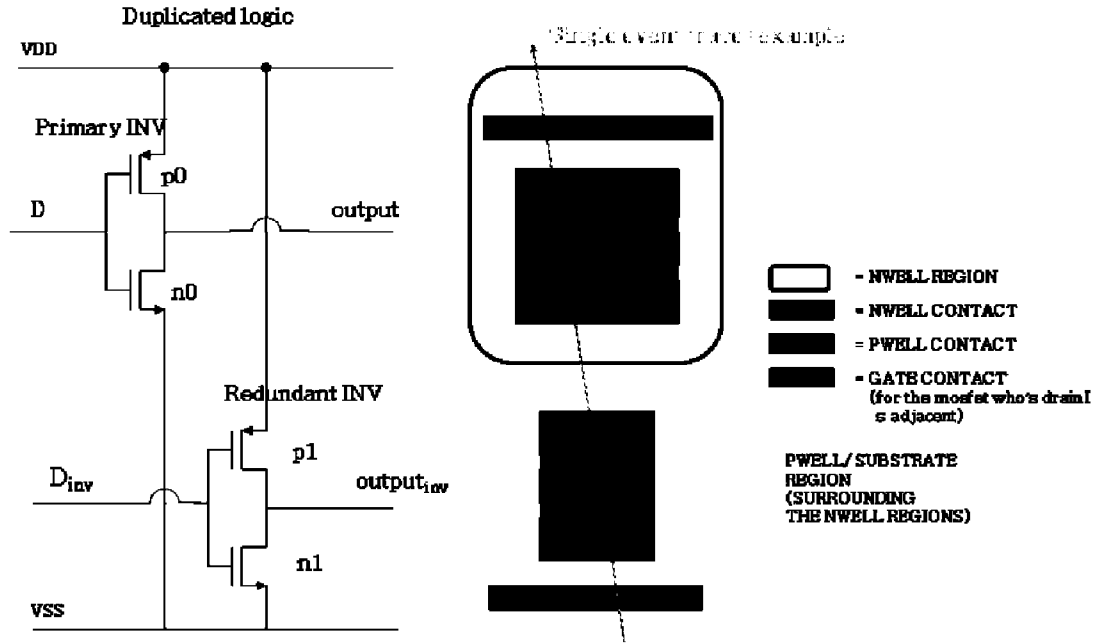
Drawing 9. Net-list corresponding to the fourth preferred arrangement. The yellow MOSFET may or may not be included, as long as node 6 is connected to drain 6a, 7 to 7a, 8 to 8a, and 9 to 9a in drawing 8, and 6a, 7a, 8a, 9a are physically separate from their adjacent main drain node.



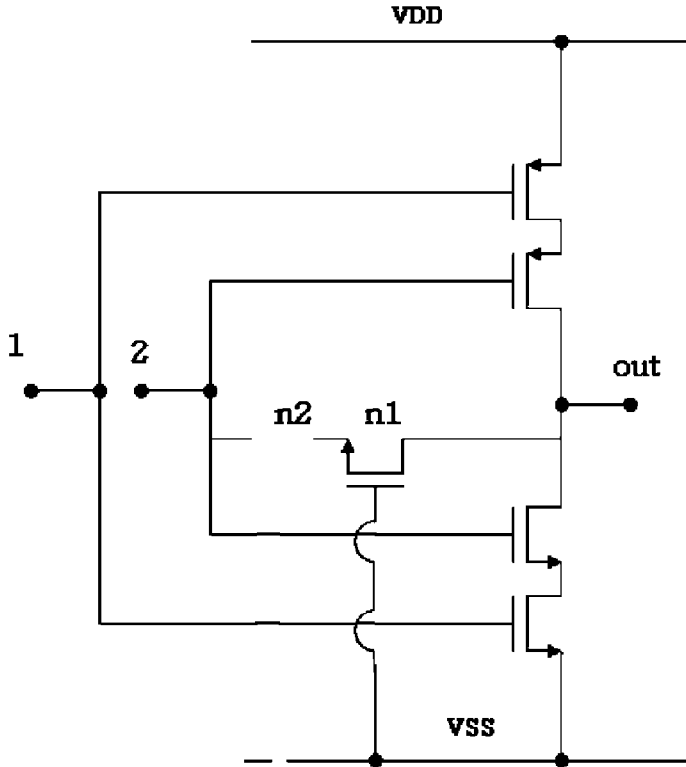
Drawing 10. A fourth preferred layout arrangement. ns/ps are the source contacts for the two mosfets who's drains are adjacent. Node 6a/6b, 7a/7b, 8a/8b, and 9a/9b are connected. The yellow gates adjacent to nodes 6a,7a, 8a, 9a may or may not be included (both variants included in the claims), but nodes 6a, 7a, 8a, 9a are physically separate from their adjacent MOSFET drains. The layout derives from the layout in drawing 1, and the same variants w.r.t. node permutations, active, source, and well contact arrangements apply. Naturally the claims also cover the various additional variants where and combination of the extra nodes 6a/6b, 7a/7b, 8a/8b, 9a/9b have been included or omitted.



Drawing 11. Circuit schematic and layout for duplicated latch cells (e.g. for BISR) using placement and sizing to ensure complete hardness against single and multiple node single event effects. For a single event affecting several nodes, the primary latch can only be upset when node 1 is HIGH, and the redundant latch can only be upset when node 1r is LOW. Hence, any single event that affects both latches, can only upset one of the two latches in the BISR configuration, and therefore, cannot generate an error in both latches at the same time.



*Drawing 12. Example of a duplicated circuit of claim 9 and 10. In a duplicated inverter where the redundant and primary nodes carry opposite states, error signals on both primary and redundant nodes can be generated if both ndrain0 and pdrain1 are affected (if D is high) or if both ndrain1 and pdrain0 are affected (D low). By placing the nodes such, that if a particle trace goes through two nodes that can cause an error transient on both primary and redundant output, then the trace also passes through the other nodes and the pulse on one of the nets are suppressed. For example, consider the trace in the figure; if node 0 is high, the charge collected on ndrain0 will pull node 0 low (error transient), the charge collected on node pdrain1 will pull node 1 high, however, the charge collected on node ndrain1 will pull node 1 low, opposing the effect on pdrain1, and keeping node 1 low (i.e., preventing the transient on node 1). If node 0 is low, the charge collected on node ndrain1, will pull node 1 low (error transient), however, the charge collected at ndrain0, will keep node 0 low (i.e., preventing a transient on node 0). It should be pointed out that in the general case there will be some pulses on all nodes, but that it will always hold true that a full swing pulse (a transient that can propagate) only can be generated on one, and one only, of the duplicated nodes.*



*Drawing 13. Example of a adding protective MOSFET devices to a c-element filter circuit. The ndrain of the output of the c-element (i.e., a net which becomes floating if the two inputs have different voltage states) is connected, via the protection MOSFET n1, either to an n-type contact area close to the ndrain of the input net 2, or via a second protective MOSFET, n2, to the ndrain of the input net 2. This protection would be adequate when the layout is such that the ndrain of the c-element output and the ndrain of the input node 2 are the most sensitive contact area pair (i.e., that other mutually sensitive contact areas are further apart, and/or have other opposing contact areas in between them). As in the case of the DICE circuit more protective MOSFET devices can be added to protect other mutually sensitive contact area pair, if required.*

**LAYOUT METHOD FOR SOFT-ERROR HARD  
ELECTRONICS, AND RADIATION  
HARDENED LOGIC CELL**

CROSS REFERENCE TO RELATED  
APPLICATIONS

**[0001]** This application claims the benefit of U.S. Provisional Application Nos. 61/011,599 filed Jan. 17, 2008; 61/011,989 filed Jan. 22, 2008; 61/068,483 filed Mar. 7, 2008; and 61/123,003 filed Apr. 5, 2008, which are incorporated herein by reference.

GOVERNMENT SUPPORT

**[0002]** This invention was made with Government support under W31P4Q-06-C-0097 awarded by DARPA and FA9451-06-C-0383 awarded by DTRA. The Government has certain rights in the invention.

BACKGROUND OF THE INVENTION

**[0003]** 1. Field of the Invention

**[0004]** This invention comprises a layout method to effectively protect logic circuits against soft errors (non-destructive errors) and circuit cells, with layout, which are protected against soft errors. In particular, the method protects against cases where multiple nodes in circuit are affected by a single event. These events lead to multiple errors in the circuit, and while several methods exist to deal with single node errors, multiple node errors are very hard to deal with using any currently existing protection methods. The method is particularly useful for CMOS based logic circuits in modern technologies ( $\leq 90$  nm), where the occurrence of multiple node pulses becomes high (due to the high integration level). It uses a unique layout configuration, which makes the circuits protected against single event generated soft-errors.

**[0005]** The problem of soft errors generated by single event transients (and single event upsets) is expected to increase drastically in ultra-deep submicron ( $\leq 90$  nm) technologies. Of particular significance is that logic circuits are expected to become much more sensitive to radiation generated soft-errors and possibly surpass memory as the major source of single event errors. Furthermore, the generation rate of multiple errors, multiple bit upsets (MBU), single-event multiple upset (SEMU) increases.

**[0006]** The main reason for this is that, with a higher feature integration and higher frequencies, the spatial distribution and pulse length of a single event transient (SET) becomes relatively larger, increasing the probability that an SET pulse is latched-in as a (soft-) error, or that SET pulses are generated simultaneously on several circuit nodes by one single event.

**[0007]** The problem with increasing soft-error rates is further complicated by the escalating cost of semiconductor design and manufacturing. The high cost involved in developing and maintaining a semiconductor FAB makes it highly desirable to use standard commercial semiconductor manufacturing also for applications that require a high radiation tolerance. Hence, there is a strong drive to develop efficient and robust radhard-by-design (RHBD) techniques for these applications.

**[0008]** Furthermore, the design process is also becoming very complex and expensive, and it would be highly desirable to be able to re-use standard design IP and libraries as much as possible for radhard applications.

**[0009]** 2. Prior Art

**[0010]** Current radhard-by-design technology for single event errors include triplication (triple mode redundancy, TMR) or duplication (e.g., built-in soft-error resilience, BiSER). These circuits carry two or more redundant copies of a signal, and use some form of voting, or filtering, circuitry to determine the correct signal among the redundant signals. Filtering preventing a signal to pass in the case that one of the redundant signals is wrong (by comparing the value of the redundant signals), and voting circuits selects the correct signal from the majority among several (3 or more) redundant signals.

**[0011]** These techniques generate undesirable power and area overhead, and current versions of these techniques cannot handle MBUs or SEMUs. Error correction codes, ECC, for memory, which also (loosely) could be classified as RHBD, is more efficient than duplication/triplication and can, with additional overhead, handle multiple errors in memory circuitry. However, the application of a corresponding error correction to logic circuits is very limited and application specific (e.g., selective parity check or insertion of specialized checking circuit IP).

**[0012]** State-of-the art for layout techniques for soft-error hard design mainly consist of simple spacing and sizing, and in adding additional contacts.

BRIEF SUMMARY OF THE INVENTION

**[0013]** A radiation generated single event (soft-) error (SEE) occurs when the charge, generated in the semiconductor material by one or more (e.g. secondary) charge particles, is collected by contact areas on the semiconductor substrate. This leads to current pulses on the circuit nets, connected to these contact areas, which, in their turn, cause voltage pulses in the circuit which can upset a sequential element (latch, flip-flop) or propagate through combinational logic and be latched in as errors at the next sequential element in the circuit.

**[0014]** This invention comprises a unique new layout method, which takes advantage of the overall circuit response to a single event effect, and, furthermore, comprises circuit cells, with layout, which are protected against soft errors. The method uses an arrangement of critical contact areas in such a way that single event pulses in the circuit, that are generated on multiple nodes, act to oppose each other and hence cancel (or greatly reduce the effect of the single event). In the case that a primary and secondary circuit is used to maintain, or process the signal in a circuit, addition rules, described in section 4, are used, so that no possibility remains that a error is generated in both primary and secondary circuit, and hence that the combination of primary and secondary circuit will be fully error free.

BRIEF DESCRIPTION OF THE DRAWINGS AND  
FIGURES

**[0015]** Table 1. The state for the nodes in a circuit that uses a primary (nodes n1,n2) and secondary (nodes n3,n4) circuit for storage or processing of the state.

**[0016]** Drawing 1. Primary opposing nodes in a latch cell.

**[0017]** Drawing 2. A principal arrangement of opposing node of a latch circuit.

**[0018]** Drawing 3. Basic netlist for the DICE latch cell (prior art [Nic05]) with nodes 1-4. p1-p4 and n1-n4 are the pMOSFET drains and the nMOSFET drains, respectively.

**[0019]** Drawing 4. A first preferred layout arrangement for the layout of the DICE latch cell. ns/ps are the source contacts for the two mosfets who's drains are adjacent.). p1-p4 and n1-n4 are the pMOSFET drains and the nMOSFET drains of the 4 main storage nodes, respectively. Any cyclic simultaneous permutation of the n and p nodes will be equivalent (and part of the invention). The mosfets can be placed in separate active areas, or the adjacent n and p nodes can be placed in the same active area. The MOSFET sources can be placed in the line of the drains or in the direction vertical to the line of the drain nodes. The well contacts can be placed on either side only, or also surround the adjacent node pairs. The nodes can also be arranged in a different order subject to the following rules: two adjacent n-drains, or two adjacent p-drains are always an odd/even pair (e.g., p1 & p2, or n2 and n3), adjacent n-drain to p-drain are always an odd/odd or and even/even pair (e.g., n2 & p2, or p3 & n1).

**[0020]** Drawing 5. Net-list corresponding to the second preferred arrangement. The yellow MOSFET may or may not be included, as long as node 6 is connected to drain 6a in drawing 5, and p1 and 6a are physically separate.

**[0021]** Drawing 6. A second preferred layout arrangement. ns/ps are the source contacts for the two mosfets who's drains are adjacent. Node 6a and 6b are connected. The yellow gate adjacent to node 6a may or may not be included (both variants included in the claims), but p1 and 6a are physically separate. The layout derives from the layout in drawing 1, and the same variants w.r.t. node permutations, active, source, and well contact arrangements apply.

**[0022]** Drawing 7. Net-list corresponding to the third preferred arrangement. The yellow MOSFET may or may not be included, as long as node 6 is connected to drain 6a in drawing 4, and p1 and 6a are physically separate, and node 7 is connected to drain 7a in drawing 4, and n1 and 7a are physically separate.

**[0023]** Drawing 8. A third preferred layout arrangement. ns/ps are the source contacts for the two mosfets who's drains are adjacent. Node 6a-6b are connected, as are node 7a/7b. The yellow gate adjacent to node 6a and 7a may or may not be included (both variants included in the claims), but the adjacent drain areas are physically separate. The layout derives from the layout in drawing 1, and the same variants w.r.t. node permutations, active, source, and well contact arrangements apply.

**[0024]** Drawing 9. Net-list corresponding to the fourth preferred arrangement. The yellow MOSFET may or may not be included, as long as node 6 is connected to drain 6a, 7 to 7a, 8 to 8a, and 9 to 9a in drawing 8, and 6a, 7a, 8a, 9a are physically separate from their adjacent main drain node.

**[0025]** Drawing 10. A fourth preferred layout arrangement. ns/ps are the source contacts for the two mosfets who's drains are adjacent. Node 6a/6b, 7a/7b, 8a/8b, and 9a/9b are connected. The yellow gates adjacent to nodes 6a, 7a, 8a, 9a may or may not be included (both variants included in the claims), but nodes 6a, 7a, 8a, 9a are physically separate from their adjacent MOSFET drains. The layout derives from the layout in drawing 1, and the same variants w.r.t. node permutations, active, source, and well contact arrangements apply. Naturally the claims also cover the various additional variants where and combination of the extra nodes 6a/6b, 7a/7b, 8a/8b, 9a/9b have been included or omitted.

**[0026]** Drawing 11. Circuit schematic and layout for duplicated latch cells (e.g. for BISER) using placement and sizing to ensure complete hardness against single and multiple node

single event effects. For a single event affecting several nodes, the primary latch can only be upset when node 1 is HIGH, and the redundant latch can only be upset when node 1 (r) is LOW. Hence, any single event that affects both latches, can only upset one of the two latches in the BISER configuration, and therefore, cannot generate an error.

**[0027]** Drawing 12. Example of a duplicated circuit of claim 9 AND 10. In a duplicated inverter where the redundant and primary nodes carry opposite states, error signals on both primary and redundant nodes can be generated if both ndrain0 and pdrain1 are affected (if D is high) or if both ndrain1 and pdrain0 are affected (D low). By placing the nodes such, that if a particle trace goes through two nodes that can cause an error transient on both primary and redundant output, then the trace also passes through the other nodes and the pulse on one of the nets are suppressed. For example, consider the trace in the figure; if node 0 is high, the charge collected on ndrain0 will pull node 0 low (error transient), the charge collected on node pdrain1 will pull node 1 high, however, the charge collected on node ndrain1 will pull node 1 low, opposing the effect on pdrain1, and keeping node 1 low (i.e., preventing the transient on node 1). If node 0 is low, the charge collected on node ndrain1, will pull node 1 low (error transient), however, the charge collected at ndrain0, will keep node 0 low (i.e., preventing a transient on node 0). It should be pointed out that in the general case there will be some pulses on all nodes, but that it will always hold true that a full swing pulse (a transient that can propagate) only can be generated on one, and one only, of the duplicated nodes.

#### DETAILED DESCRIPTION OF THE INVENTION AND HOW IT WORKS

**[0028]** This invention comprises a unique new layout method, which takes advantage of the overall circuit response to a single event effect. It also includes specific circuit cells with layout, which have been constructed in accordance with the new layout method.

**[0029]** A radiation generated single event (soft-) error (SEE) occurs when the charge, generated in the semiconductor material by one or more (e.g. secondary) charged particles, is collected by contact areas. The contact areas are the low resistivity regions on, or in, the semiconductor substrate, which are connected to a net in the circuit, e.g., the source and drain areas in a MOSFET technology. A circuit net (or node) refers to a part of the circuit, connected by low resistivity regions (metal), which maintains a certain voltage value (referred to as the voltage state of the net) throughout its' extent. A net can be connected to any number of contact areas.

**[0030]** The charge collected by contact areas during a single event, leads to current pulses in the circuit, which, in their turn, cause a change in the voltage of the circuit nets, connected to these contact areas, i.e. a voltage pulse in the circuit. These pulses can upset a sequential element (latch, flip-flop) or propagate through combinational logic (i.e., a set of digital logic gates) and be latched in as errors at the next sequential element in the circuit.

**[0031]** The effect of a single event on the voltage on the circuit net, is different for different contact areas, e.g., a single event can have the effect of increasing the voltage on the net connected to the contact area, or decreasing it, depending on where the contact areas are located in substrate, and how they are connected to the circuit. The method in this invention uses an arrangement of contact areas in such a way that single event generated pulses in the circuit, that occur on multiple

contact areas, acts to oppose each other, w.r.t. the effects they have on the voltage of the circuit nets, and hence cancel (or greatly reduce the effect of the single event).

**[0032]** The method also comprises an adjustment the strength of the effect a single event has on the voltage of the circuit nets, when this is desirable to achieve the desired total effect on the circuit. This adjustment can be achieved by changing the sizes of the contact areas, and by changing their positions relative to other components in the layout.

**[0033]** The method can be applied to sequential logic elements (latches, flip-flops, memory cells), to combinational logic (a connection of one or more digital logic gates), or to analog circuit cells.

**[0034]** In the following two section details of two specific ways to apply the method are described. The first, section 4.1, uses a placement, and strength adjustment, such that the single event effects, on several contact areas, cancel out each other, in terms of their effect on the circuit nets they are connected to. The second, section 4.2, uses a placement, and strength adjustment, such that two, or more, redundant nets in the circuit, are affected differently by a single event, in such a way that a single event cannot simultaneously change their voltage state on several of the redundant nets.

#### A. Layout Method Using Symmetric Arrangements—Method 1

**[0035]** The key steps in method one of the invention are:

**[0036]** 1. Identify which contact areas have opposing effects on the circuit nets when they are simultaneously affected by a single event

**[0037]** 2. Place these nodes in the layout next to each other, and in a fully symmetric way with respect to other adjacent contact areas

**[0038]** a. In particular in a CMOS technology the contact are configured in a symmetric (equivalent) position w.r.t. well junctions and well contacts

**[0039]** b. If the two contact areas are part of a sequential element (e.g., a latch), this arrangement ensures that these two nodes cannot be upset by a single event that affects both areas, i.e., an event which has an extended charge (e.g., as generated by a charged particle passing through) which is in such a direction that it affects both these nodes.

**[0040]** c. If nodes are part of a combinational element, the arrangement ensures that the generated output pulse is greatly suppressed, when the generation single event affects both nodes, i.e., an event which has an extended charge (e.g., as generated by a charged particle passing through) which is in such a direction that it affects both these nodes.

**[0041]** 3. In an element using additional protective circuitry (redundant nets), place the contact areas of the redundant nets in a direction, which is such that when the charge from one single event effects both primary, and redundant nets, it is in the direction which is such that it always also affects both opposing nodes in either the primary or the secondary circuit, or that it affects the opposing node of both primary and secondary circuit.

**[0042]** Specifically for CMOS technology, step one and two above would use the following to characterize the effect of a single event on a source or drain contact area:

**[0043]** a. When an n-drain (or source) is affected by a single event, the effect of the single event is to reduce the voltage on the net connected to this contact area, i.e., if

the node is high is will tend to switch the voltage, when the node is low, it will not tend to switch the voltage.

**[0044]** b. When an n-drain (or source) is affected by a single event, the effect of the single event is to reduce the voltage on the net connected to this contact area, i.e., if the node is high is will tend to switch the voltage, when the node is low, it will not tend to switch the voltage.

**[0045]** Also, specifically for a CMOS technology, step 3 above, would use the following rules for two nodes, each connected to a net carrying redundant signals (primary and secondary nets):

**[0046]** a. When two n-drains (or sources), one connected to the primary net and one to the secondary net, are affected by a single event, and they always have opposite voltage states, then only one of the primary/secondary nets can be upset (i.e., change its' voltage).

**[0047]** b. When two p-drains (or sources), one connected to the primary and one to the secondary net, are affected by a single event, and they always have opposite voltage states, then only one of the primary/secondary circuits can be upset.

**[0048]** c. When an n-drain (or source) from one net, and a p-drain (or source) from the other net is affected, are affected by a single event, and the nets connected to these drains (sources) always have the same voltage state, then only one of the primary/secondary nets can be upset.

#### B. Layout Method Using Asymmetric Arrangements—Method 2

**[0049]** For the case of an element that uses primary and redundant nets to store the state (i.e., the voltage or signal), an alternative to synthesizing a layout where single event effects cancel out each other, is to deliberately let one of the contact areas be stronger w.r.t. single event charge collection. This contact area will then always determine the outcome of a single event in on the connected net (e.g., for a p-drain it would always end up HIGH (at Vdd)). When there are four nets that store the state (2 primary nets, two redundant nets), and we make sure that net connected to the contact areas that is made dominant in the primary circuit part, stores the opposite state to the net connected to the contact area that is made dominant in the redundant circuit part, then only one of the two redundant circuit parts can be upset by an event that affects both circuit parts. Using this variant, the robust cell synthesis methodology would be as follows:

**[0050]** For designs that use primary and redundant nets to store a state:

**[0051]** a. Identify which contact areas have opposing circuit effects when they are simultaneously affected by a single event (in the primary as well as the redundant part)

**[0052]** b. Place these nodes in the layout next to each other, and make one of the nodes dominant w. r. t. a single event (e.g., by making the drain area larger, and changing the distance to the well-junction and the well-ties).

**[0053]** c. Make sure that the net connected to the dominant contact area of the primary circuit part, stores the opposite state to the net connected to the dominant contact area in the redundant circuit part.

**[0054]** d. Place the primary and redundant contact areas, relative to each other, in such a way that a single event the affects both the primary and redundant circuitry, also

always affects both the dominant and the non-dominant nodes in the primary and in the redundant part.

**[0055]** (i) In this way, either the primary or the redundant part will be in a state where the dominant node will make sure this circuit part cannot be upset (i.e. change its state or voltage). Hence, in any situation only ONE of the redundant parts can be upset by a single event.

C. Discussion, Clarification, and Specific Circuit Cells

**[0056]** In a basic sequential logic circuit element (latch, sram-type memory cell, etc.) there are two main nets that maintain the state. These will always have opposite state (voltage). FIG. 1 shows the schematics of the fundamental components of a latch circuit implemented in a CMOS technology. In this latch, each of the two (main) net is connected to two contacts areas in the layout (the nmos device drain and the pmos drain).

**[0057]** In this configuration the contact areas that will have opposing effects with respect to the state of the latch, when affected by the same single event, can be identified as (step 1 above):

**[0058]** a. A single event that affects both pmos drains will have opposing effects on the state of the latch

**[0059]** b. A single event that affects both nmos drains will have opposing effect on the state of the latch

**[0060]** b. A single event that affects both nmos and pmos drain of the same node will have opposing effect on the state of the latch

**[0061]** In the symmetric method, we arrange the layout such that drains, with opposing effects, are placed next to each other, in a symmetric arrangement (i.e. w.r.t. symmetric w.r.t the surrounding layout, and having the same shape). This is step 2 in the methodology number 1 above. FIG. 2 shows such an arrangement where we have utilized the first two of the opposing contact area identifications above. We now have a latch which cannot be upset if the single event has such a directions that it passes the two nets of the circuit.

**[0062]** Step 3 in methodology number 1, as well as method number 2, concerns the case when an additional (redundant) circuit (here a latch) is available. In a circuit configuration that uses two latches to maintain the states, there will be 4 main nodes, n1, n2, from the primary latch, and n3, n4, from the secondary latch. The nodes from one latch will be in opposite states, and, during correct circuit operation, each node in the primary latch will always have the same state as one node in the secondary latch. This situation is shown in table 1, where n1 and n3 maintain the same state, and n2 and n4 maintain the same state.

**[0063]** According to step 3, the nodes of the second latch are now placed, w.r.t. the first latch, such that when an extended event occurs that affects both latches, it will be in a direction which affects both opposing nodes in each individual latch, or at least in one of them. FIG. 11 shows such an arrangement, where the method with dominating nodes (methodology 2 above) has been used, and the two latches have been placed in such a way relative to each other that at the most, one of the latches can be upset, by any single event, but not both.

**[0064]** The same situation is the same also for other sequential elements (e.g., memory cells) and the method applies to these elements as well. The method also applies to elements

which uses more than 2 nodes to maintain the state, as well as non-sequential elements with a primary and secondary redundant net.

TABLE 1

The state for the nodes in a circuit that uses a primary (nodes n1, n2) and secondary (nodes n3, n4) circuit for storage or processing of the state.				
Node:	n1	n2	n3	n4
State 0	0	1	0	1
State 1	1	0	1	0

**[0065]** To extract the correct signal from the two, or more, redundant nets, a filtering, or voting circuit is used. The filtering ensuring that at any time where one of the redundant nets is wrong (e.g., for the redundant nets carrying the same voltage state; if the voltage states differ) the signal is not allowed to pass through the filtering circuit. The Built-In Soft Error (BISER) design [Mitra2005] is an example of such a configuration. A voting circuit, being used on at least 3 redundant circuit, performs a vote between the voltage states of the redundant nets. Triple mode redundancy (TMR) configurations use this type of redundancy.

**[0066]** This invention also comprises several specific DICE cells, created using the layout method. The DICE (Dual Interlocked Cell) latch [Nic2005], the circuit of which is shown in drawing 3, also uses four nets to store the circuit state, but as can be seen in drawing 3, they are not connected as two separate latches, but in an interlocked way.

**[0067]** The principal arrangement of the 4 storage nets, of the DICE cells in this inventions, is that the contact areas of the nets are placed along one direction (e.g., drawing 4), and that they have a certain order, than minimizes or removes the effect of the single event, and hence reduces or removes the possibility that the storage element can be upset by a single event. The first variant (variant 1) is shown in drawing 4. In this variant the MOSFET pairs have been placed in the same active area with a common MOSFET source contact in-between. However, they can also be placed in separate active areas, using separate sources contacts, and they can also be oriented so that the sources are perpendicular to the direction of the drain nodes.

**[0068]** In variants 2-4 (drawing 5-10) protective nodes have been added. They act to protect certain sensitive node-pairs and are not (necessarily) active during normal circuit operation. However, they can also be used as active devices connecting their gates to other storage nodes. For example, while variant 1 is much more robust than the normal layout (which does not have other nodes in between the sensitive node pairs), there are still some single event sensitivity remaining, the main being for the node pair p1-n2. By extending variant one as shown in drawings 5-6, the node pair p1-n2 is also protected. This is variant 2. The most sensitive node pair in variant 2 is the n1-p4 node pair, this pair is protected with the extension in variant 3 (drawings 7-8). Finally the latch can be made symmetric by adding additional protective nodes. A fully symmetric arrangement of protective nodes is shown in drawings 9-10 (third variant).

**[0069]** The addition of additional protective MOSFETs has a general application to circuits which uses redundant nets. In the same way as in the case of the DICE circuit, they can be used to keep the state of a circuit node which becomes floating (not connected to the power, i.e., to VSS or VDD) during a

single event. Floating nets become very sensitive to the single event charge, their voltage state can change very easily (i.e., even by very weak interaction with the single event). The additional protective devices, even if they just turn on partially during the single event, will make the nodes, that become floating during a single event, much more stable. Another (not DICE) example of the addition of such protective devices for a c-element filtering circuit is shown in drawing 13.

[0070] The invention also comprises a combinational circuit where all, or some of the nets have been duplicated, in such a way that there is one (primary) net that carries the signal, and a second (redundant) net carries the inverse of the signal on the primary net (i.e., when the voltage on the primary net is high, the voltage on the redundant net is always low, and vice versa), and where, in accordance with the layout method, the contact areas of the primary and redundant net, are placed in such a way that when a single event affects both nets, a voltage pulse can only be generated on one of the nets, but not on both. For this type of duplicated combinational circuit, a filtering also needs to be applied to the outputs (at some point before the signal is latched into a single sequential element), which prevents propagation of a signal, unless both nets have their correct state (i.e., one being the inverse of the other). Alternatively sequential elements can also be duplicated, and an error detection and correction added at some point in the circuit (an error being identified by comparing the signal on the two redundant nets). This type of duplicated combinational circuit is shown in drawing 12.

What is claimed is:

1. A method for laying out an electronic circuit wherein the electronic circuit comprises contact areas, said method comprising:

- a. determining the effect on the voltage state of one or more nets in the circuit, due to a single event occurring near each contact area, for each contact area in the circuit;
- b. categorizing the contact areas in such a way that contact areas for which a single event have opposing effects on the voltage state of the nets in the circuit, and for which a single event has a non-opposing effect on the voltage state of the nets in the circuit, are identified;
- c. placing these contact areas in such a way that when a single event has opposing effects on the voltage state of the circuit nets, the opposing first and second contact areas are placed as close to each other as permitted by the circuit and by the design rules;
- d. placing a first contact area and a second contact area, with non-opposing effects on the voltage state of the nets in the circuit, said non-opposing effects caused by a single event, wherein the first and second contact areas are non-adjointing, and placing a third contact area in between the first and second contact areas, wherein said third contact area has an effect on the voltage state of the nets in the circuit opposing those of the first and second contact areas, and wherein the third contact area's effect on the voltage state of the nets in the circuit is caused by a single event, and
- e. adjusting the strength of the effect of a single event on the placed contact areas in such a way that the opposing effects are of the same, but opposite, strength.

2. The method of claim (1), wherein the circuit has at least two nets carrying the same signal (or the signal and its' inverse), where each of these nets have at least two contact

areas for which a single event has an opposing effect on the voltage state of said two nets, comprising:

- a. placing a first contact area and a second contact area, each from a separate redundant net, for which a single event has the effect of changing the voltage state on the two redundant nets, wherein the first and second contact areas are non-adjointing, and placing a third contact area in between the first and second contact areas, said third contact area having an effect on the voltage state on at least one of the redundant nets, and wherein said effect of the third contact area is caused by a single event and opposes the effects of the first and second contact areas, and
- b. adjusting the strength of the effect of a single event on the placed contact areas in such a way that any single event that affects (passes through) the two redundant nets, at maximum can change the state of one of the nets, but never both nets.

3. The method of claim 1 or 2, wherein the circuit utilizes MOSFET devices, further comprising:

- a. identifying all MOSFET source (S) and drain (D) doping areas, which are not directly connected to the power-nets (VSS, VDD) as the contact areas of claim (1) and (2); and
- b. identifying the n-type MOSFET drains or sources, as contact areas for which a single event have the effect of pulling the voltage state, of the nets connected to this contact area, low, and the p-type MOSFET drains or sources, as contact areas for which a single event have the effect of pulling the voltage state, of the nets connected to this contact area, high.

4. The method of claim 3, further comprising:

- a. adding additional MOSFET devices between two nets, which at any time, carry opposite voltage states (high/low voltage level), in such a way that if one (first) of the nets is affected by a single event, such that its' voltage state is changed, then the additional MOSFET device turns on, connecting the two nets, and hence ensures that the state of the second net is not changed; and
- b. connecting the sources or drains of the p-type MOSFETs in the two nets by additional p-type MOSFETs with their gates connected to the high level power net (VDD), and connecting the sources or drains of the n-type MOSFETs in the two nets by additional n-type MOSFETs with their gates connected to the low level power net (VSS).

5. A sequential logic or memory cell and layout, which uses two or more latches to store the state of the element, each latch having at least one net that stores the voltage state and at least one net that stores the opposite value (inverse) of the voltage state, comprising:

- a. an arrangement of the contact areas of each net (which keep a certain voltage state or its' inverse), in the such a way that the contacts areas of at least 4 of these nets are positioned symmetrically along one line in the layout, and positioned relative to each other such that no two contact areas, which:
  - i. carry the same voltage state, and for which a single event have the same effect on the voltage state of the net; or
  - ii. carry different voltage states (i.e., a certain state and its' inverse), and for which a single event have opposite effect on the data (voltage) of the net are placed next to each other.

6. A sequential logic cell, which consist of four inverter circuits, each inverter circuit consisting of one p-type MOSFET and one n-type MOSFET, where the inverters have been connected as a Dual Interlocked Cell (DICE) by connecting the outputs of each inverter to the gate of a p-type MOSFET of another, second, inverter, and to the gate of an n-type MOSFET of another third inverter, each gate being connected to one output only, and hence having four nets, one connected to each inverter output and to two gates, two nets carrying the same voltage state and the two other carrying the inverse of the voltage state of the first two nets, each net having one p-type drain contact area and one n-type drain contact area, comprising:

- a. An arrangement where the contact areas of each of the four nets, are placed along a line in the layout; and
- b. In which two adjacent n-drain contact areas, or two adjacent p-drain contact areas, always belong to (are connected to) two nets which carry opposite voltage states, and where adjacent n-drain contact areas and p-drain contact areas always belong to nets that carry the same voltage state.

7. The sequential Dual Interlocked Cell (DICE) circuit of claim (6), wherein one or more, additional protective MOSFET devices, are added and connected in between two circuit nets of the sequential element of claim 6, comprising:

- a. a configuration where said additional devices are connected such that additional p-type devices having their gates connected to the high voltage level (VDD), and either drain or source being (shared with) the p-type contact area of a first circuit net in the sequential circuit of claim 6, and the other contact (drain or source) either being connected to a source or drain contact area of another second additional p-type MOSFET, said second additional MOSFET having its' other contact (drain or source) being (shared with) the p-type contact area connected to a second net in the sequential circuit, or to a contact area which is adjacent to the p-type drain of the second net of the sequential circuit but not connect to a net, said second net in the sequential circuit having the inverse voltage state of the first net, and, additional n-type devices having their gates connected to the low voltage level (VSS), and either drain or source being (shared with) the n-type contact area of a first circuit net in the sequential circuit of claim 6, and the other contact (drain or source) either being connected to a source or drain contact area of another second additional n-type MOSFET, said second additional MOSFET having its' other contact (drain or source) being (shared with) the n-type contact area connected to a second net in the sequential circuit, or to a contact area which is adjacent to the n-type drain of the second net of the sequential

circuit but not connect to a net, said second net in the sequential circuit having the inverse voltage state of the first net; and

- b. a configuration where any additional drain or source contact areas belonging to the additional MOSFET devices are placed in the same line in the layout as the contact areas of the sequential circuit of claim 6

8. The sequential logic or memory cell and layout of claim (5), wherein a filtering or voting circuit is connected to the output of redundant nets, said filtering circuit, being used in the case of two redundant nets, preventing a data signal to pass unless both nets have the correct data, said voting circuit used on three redundant nets, performing a vote between the states of the redundant nets, comprising:

- a. a layout where the strength of the response to a single event have been adjusted such that the total effect, caused by a single event, on one of the nets (primary) is opposite to the total effect, caused by a single event, on its' redundant counterpart, ensuring that when a single event affects both the primary and redundant nets, one and only one, of these nets can change its state.

9. A combinational circuit, where logic element have been duplicated (either throughout or in selected parts) and hence the data signal is carried by a primary net, and by a secondary net (carrying either the signal or it's inverse), and where either filtering circuits, preventing a signal to pass unless the two redundant nets carry the correct signal, have been place in front of each sequential elements, or the sequential elements also have been duplicated (the latter case requiring an error detection and/or correction at the end of the duplicated circuit chain), comprising:

- a. a layout where the contacts areas of two redundant nets (primary and secondary) are placed such that there is no straight line between a first and a second contact area, each from separate redundant nets, ad for which a single event has the effect of changing the voltage state in the net connected to the circuit area, unless there is, along this line, in between the first and second contact area, at least one third contacts area, for which a single event has an opposite effect, to that of the first and second contact areas, on the voltage state of at least one of the two redundant nets.

10. The combinational circuit of claim 9 comprising:

- a. a layout where the strength of the response to a single event have been adjusted such that the total effect, caused by a single event, on one of two redundant nets is opposite to the total effect, caused by a single event, on the other of the two redundant nets. ensuring that when a single event affects both of the two redundant nets, only one of these two nets can generate and error signal in the circuit.

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