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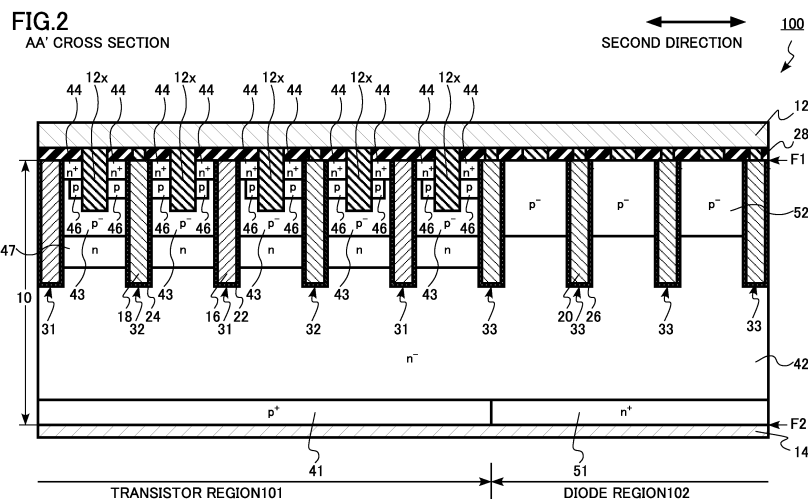
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(54) SEMICONDUCTOR DEVICE

(57) A semiconductor device of embodiments includes a transistor region and a diode region. The transistor region includes: a first conductive type first semiconductor region, a second conductive type second semiconductor region, a first conductive type third semiconductor region in this order in a semiconductor layer; a second conductive type fourth semiconductor region and a first conductive type fifth semiconductor region on the third semiconductor region and arranged alternately in a

first direction; a first conductive type sixth semiconductor region between the third and the fourth semiconductor region a first trench spaced from the sixth semiconductor region; a gate electrode in the first trench; a first electrode having a first portion, a bottom surface of the first portion being in contact with the third semiconductor region and side surfaces of the first portion being in contact with the fourth, the fifth, and the sixth semiconductor regions; and a second electrode.



DescriptionCROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2023-158094, filed on September 22, 2023, the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

[0003] An example of a power semiconductor device is an insulated gate bipolar transistor (IGBT). In the IGBT, for example, a p-type collector region, an n-type drift region, and a p-type base region are provided on a collector electrode. Then, in a trench that penetrates through the p-type base region to reach the n-type drift region, a gate electrode is provided with a gate insulating film interposed therebetween. In addition, an n-type emitter region connected to an emitter electrode is provided in a region adjacent to the trench on the surface of the p-type base region.

[0004] In recent years, a reverse-conducting IGBT (RC-IGBT) in which an IGBT and a freewheeling diode are formed in the same semiconductor chip has been widely developed and commercialized. The RC-IGBT is used, for example, as a switching element in an inverter circuit. The freewheeling diode has a function of making a current flow in a direction opposite to the on-current of the IGBT. Forming the IGBT and the freewheeling diode in the same semiconductor chip has many advantages, such as a reduction in chip size due to sharing the termination region and dispersion of heat generation locations.

[0005] In the RC-IGBT, there is a possibility that the operation of the IGBT and the operation of the diode will interfere with each other to degrade the element characteristics of the RC-IGBT. For example, when the diode is turned off, holes injected from the IGBT region at the boundary with the diode region may not be discharged to increase the reverse recovery current of the diode. When the reverse recovery current of the diode increases, the switching loss of the diode increases, and the switching loss of the RC-IGBT increases.

BRIEF DESCRIPTION OF THE DRAWINGS**[0006]**

Fig. 1 is a schematic diagram of a semiconductor device according to a first embodiment;

Fig. 2 is a schematic cross-sectional view of a part of the semiconductor device according to the first embodiment;

Fig. 3 is a schematic top view of a part of the semiconductor device according to the first embodiment;

Fig. 4 is a schematic cross-sectional view of a part of the semiconductor device according to the first embodiment;

Fig. 5 is a schematic cross-sectional view of a part of a semiconductor device according to a comparative example;

Fig. 6 is a schematic top view of a part of the semiconductor device according to the comparative example;

Fig. 7 is a schematic cross-sectional view of a part of the semiconductor device according to the comparative example;

Fig. 8 is an explanatory diagram of the problem of the semiconductor device according to the comparative example;

Fig. 9 is an explanatory diagram of the function and effect of the semiconductor device according to the first embodiment;

Fig. 10 is an explanatory diagram of the function and effect of the semiconductor device according to the first embodiment;

Fig. 11 is a schematic cross-sectional view of a part of a semiconductor device according to a first modification example of the first embodiment;

Fig. 12 is a schematic top view of a part of the semiconductor device according to the first modification example of the first embodiment;

Fig. 13 is a schematic cross-sectional view of a part of the semiconductor device according to the first modification example of the first embodiment;

Fig. 14 is a schematic cross-sectional view of a part of a semiconductor device according to a second modification example of the first embodiment;

Fig. 15 is a schematic top view of a part of the semiconductor device according to the second modification example of the first embodiment;

Fig. 16 is a schematic cross-sectional view of a part of the semiconductor device according to the second modification example of the first embodiment;

Fig. 17 is a schematic cross-sectional view of a part of a semiconductor device according to a second embodiment;

Fig. 18 is a schematic top view of a part of the semiconductor device according to the second embodiment; and

Fig. 19 is a schematic cross-sectional view of a part of the semiconductor device according to the second embodiment.

DETAILED DESCRIPTION

[0007] A semiconductor device of embodiment includes a transistor region and a diode region. The transistor region includes: a semiconductor layer having a first face and a second face opposite to the first face; a first semiconductor region of a first conductive type pro-

vided in the semiconductor layer; a second semiconductor region of a second conductive type provided in the semiconductor layer and provided between the first semiconductor region and the first face; a third semiconductor region of the first conductive type provided in the semiconductor layer and provided between the second semiconductor region and the first face; a fourth semiconductor region of the second conductive type and a fifth semiconductor region of the first conductive type provided in the semiconductor layer, provided between the third semiconductor region and the first face, and arranged alternately in a first direction parallel to the first face; a sixth semiconductor region of the first conductive type provided between the third semiconductor region and the fourth semiconductor region and having a first conductive type impurity concentration higher than that in the third semiconductor region and lower than that in the fifth semiconductor region; a first trench provided on the first face side in the semiconductor layer, extending in the first direction, repeatedly arranged in a second direction parallel to the first face and perpendicular to the first direction, in contact with the second semiconductor region, the third semiconductor region, the fourth semiconductor region, and the fifth semiconductor region, and spaced from the sixth semiconductor region; a gate electrode provided in the first trench; a gate insulating film provided between the gate electrode and the third semiconductor region; a first electrode provided on the first face side with respect to the semiconductor layer and having a first portion, a bottom surface of the first portion being in contact with the third semiconductor region and side surfaces of the first portion being in contact with the fourth semiconductor region, the fifth semiconductor region, and the sixth semiconductor region; and a second electrode provided on the second face side with respect to the semiconductor layer and in contact with the first semiconductor region. The diode region includes: the semiconductor layer; the second semiconductor region; a seventh semiconductor region of the second conductive type provided in the semiconductor layer, provided between the second semiconductor region and the second face, and having a second conductive type impurity concentration higher than that in the second semiconductor region; an eighth semiconductor region of the first conductive type provided in the semiconductor layer and provided between the second semiconductor region and the first face; the first electrode electrically connected to the eighth semiconductor region; and the second electrode in contact with the seventh semiconductor region.

[0008] Hereinafter, embodiments will be described with reference to the diagrams. In the following description, the same or similar members and the like will be denoted by the same reference numerals, and the description of the members and the like once described will be omitted as appropriate.

[0009] In this specification, when there are notations of n^+ -type, n -type, and n^- -type, this means that the n -type impurity concentration decreases in the order of n^+ -type,

n -type, and n^- -type. In addition, when there are notations of p^+ -type, p -type, and p^- -type, this means that the p -type impurity concentration decreases in the order of p^+ -type, p -type, and p^- -type.

[0010] In this specification, the n -type impurity concentration does not indicate the actual n -type impurity concentration, but indicates the effective n -type impurity concentration after compensation. Similarly, the p -type impurity concentration does not indicate the actual p -type impurity concentration, but indicates the effective p -type impurity concentration after compensation. For example, if the actual n -type impurity concentration is higher than the actual p -type impurity concentration, the n -type impurity concentration is obtained by subtracting the p -type impurity concentration from the actual n -type impurity concentration. The same applies to the p -type impurity concentration.

[0011] In this specification, the distribution and absolute value of the impurity concentration in a semiconductor region can be measured by using, for example, secondary ion mass spectrometry (SIMS). In addition, the relative magnitude relationship between the impurity concentrations in two semiconductor regions can be determined by using, for example, scanning capacitance microscopy (SCM). In addition, the distribution and absolute value of the impurity concentration can be measured by using, for example, spreading resistance analysis (SRA). By the SCM and the SRA, the relative magnitude relationship or absolute values of the carrier concentrations in semiconductor regions can be calculated. By assuming the activation rate of impurities, the relative magnitude relationship between the impurity concentrations in two semiconductor regions, the distribution of the impurity concentration, and the absolute value of the impurity concentration can be calculated from the measurement results of the SCM and the SRA.

(First Embodiment)

[0012] A semiconductor device according to a first embodiment includes a transistor region and a diode region. The transistor region includes: a semiconductor layer having a first face and a second face opposite to the first face; a first semiconductor region of a first conductive type provided in the semiconductor layer; a second semiconductor region of a second conductive type provided in the semiconductor layer and provided between the first semiconductor region and the first face; a third semiconductor region of the first conductive type provided in the semiconductor layer and provided between the second semiconductor region and the first face; a fourth semiconductor region of the second conductive type and a fifth semiconductor region of the first conductive type provided in the semiconductor layer, provided between the third semiconductor region and the first face, and arranged alternately in a first direction parallel to the first face; a sixth semiconductor region of the first conductive type provided between the third semiconductor

region and the fourth semiconductor region and having a first conductive type impurity concentration higher than that in the third semiconductor region and lower than that in the fifth semiconductor region; a first trench provided on the first face side in the semiconductor layer, extending in the first direction, repeatedly arranged in a second direction parallel to the first face and perpendicular to the first direction, in contact with the second semiconductor region, the third semiconductor region, the fourth semiconductor region, and the fifth semiconductor region, and spaced from the sixth semiconductor region; a gate electrode provided in the first trench; a gate insulating film provided between the gate electrode and the third semiconductor region; a first electrode provided on the first face side with respect to the semiconductor layer and having a first portion, a bottom surface of the first portion being in contact with the third semiconductor region and side surfaces of the first portion being in contact with the fourth semiconductor region, the fifth semiconductor region, and the sixth semiconductor region; and a second electrode provided on the second face side with respect to the semiconductor layer and in contact with the first semiconductor region. The diode region includes: the semiconductor layer; the second semiconductor region; a seventh semiconductor region of the second conductive type provided in the semiconductor layer, provided between the second semiconductor region and the second face, and having a second conductive type impurity concentration higher than that in the second semiconductor region; an eighth semiconductor region of the first conductive type provided in the semiconductor layer and provided between the second semiconductor region and the first face; the first electrode electrically connected to the eighth semiconductor region; and the second electrode in contact with the seventh semiconductor region.

[0013] The semiconductor device according to the first embodiment is an RC-IGBT 100 in which an IGBT and a freewheeling diode are formed in the same semiconductor chip. The RC-IGBT 100 has a trench gate type IGBT including a gate electrode in a trench formed in a semiconductor layer. Hereinafter, a case where the first conductive type is p-type and the second conductive type is n-type will be described as an example.

[0014] Fig. 1 is a schematic diagram of the semiconductor device according to the first embodiment.

[0015] Fig. 2 is a schematic cross-sectional view of a part of the semiconductor device according to the first embodiment. Fig. 2 is a cross-sectional view taken along the line AA' of Fig. 1.

[0016] Fig. 3 is a schematic top view of a part of the semiconductor device according to the first embodiment.

[0017] Fig. 3 is a top view on a first face F1. Fig. 2 is a cross-sectional view taken along the line AA' of Fig. 3.

[0018] Fig. 4 is a schematic cross-sectional view of a part of the semiconductor device according to the first embodiment. Fig. 4 is a cross-sectional view taken along the line BB' of Fig. 3.

[0019] The semiconductor device according to the first

embodiment is the RC-IGBT 100. The RC-IGBT 100 has a transistor region 101 and a diode region 102. The transistor region 101 operates as an IGBT. The diode region 102 operates as a freewheeling diode.

[0020] The RC-IGBT 100 according to the first embodiment includes a semiconductor layer 10, an upper electrode 12 (first electrode), a lower electrode 14 (second electrode), a gate electrode 16, a first conductive layer 18, a second conductive layer 20, a gate insulating film 22, a first insulating film 24, a second insulating film 26, an interlayer insulating layer 28, and a gate electrode pad 103.

[0021] The upper electrode 12 has a first trench contact portion 12x (first portion).

[0022] In the semiconductor layer 10, a gate trench 31 (first trench), a first dummy trench 32 (second trench), a second dummy trench 33 (third trench), a collector region 41 (first semiconductor region), a drift region 42 (second semiconductor region), a base region 43 (third semiconductor region), an emitter region 44 (fourth semiconductor region), a cell contact region 45 (fifth semiconductor region), a resistance reduction region 46 (sixth semiconductor region), a barrier region 47 (tenth semiconductor region), a cathode region 51 (seventh semiconductor region), an anode region 52 (eighth semiconductor region), and a diode contact region 53 (ninth semiconductor region) are provided.

[0023] The semiconductor layer 10 has a first face F1 and a second face F2 opposite to the first face F1. The first face F1 and the second face F2 are substantially parallel, for example.

[0024] The semiconductor layer 10 is, for example, single crystal silicon. The thickness of the semiconductor layer 10 is, for example, equal to or more than 40 μm and equal to or less than 700 μm .

[0025] In this specification, one direction parallel to the first face F1 is referred to as a first direction. In addition, a direction parallel to the first face F1 and perpendicular to the first direction is referred to as a second direction. In addition, in this specification, the "depth" is defined as a distance in a direction toward the second face F2 with the first face F1 as a reference.

[0026] The transistor region 101 includes the semiconductor layer 10, the upper electrode 12 (first electrode), the lower electrode 14 (second electrode), the gate electrode 16, the first conductive layer 18, the gate insulating film 22, the first insulating film 24, and the interlayer insulating layer 28.

[0027] In the semiconductor layer 10 of the transistor region 101, the gate trench 31 (first trench), the first dummy trench 32 (second trench), the collector region 41 (first semiconductor region), the drift region 42 (second semiconductor region), the base region 43 (third semiconductor region), the emitter region 44 (fourth semiconductor region), the cell contact region 45 (fifth semiconductor region), the resistance reduction region 46 (sixth semiconductor region), and the barrier region 47 (tenth semiconductor region) are provided.

[0028] The upper electrode 12 is provided on the first face F1 side of the semiconductor layer 10. In the transistor region 101, the upper electrode 12 functions as an emitter electrode of the IGBT.

[0029] The upper electrode 12 has the first trench contact portion 12x. The first trench contact portion 12x is formed in a trench provided in the semiconductor layer 10. The first trench contact portion 12x extends in the first direction.

[0030] The bottom surface of the first trench contact portion 12x is in contact with the base region 43. The side surfaces of the first trench contact portion 12x are in contact with, for example, the base region 43, the emitter region 44, the cell contact region 45, and the resistance reduction region 46. The first trench contact portion 12x is electrically connected to the base region 43, the emitter region 44, the cell contact region 45, and the resistance reduction region 46.

[0031] The contact between the first trench contact portion 12x and the base region 43 is, for example, a Schottky contact. The contact between the first trench contact portion 12x and the emitter region 44 and the cell contact region 45 is, for example, an ohmic contact. The contact between the first trench contact portion 12x and the resistance reduction region 46 is a Schottky contact or an ohmic contact. It is preferable that the contact between the first trench contact portion 12x and the resistance reduction region 46 is an ohmic contact.

[0032] The upper electrode 12 is, for example, a metal or a metal compound. The first trench contact portion 12x and portions other than the first trench contact portion 12x are formed of, for example, the same material. The first trench contact portion 12x and the portions other than the first trench contact portion 12x may be formed of different materials.

[0033] The lower electrode 14 is provided on the second face F2 side of the semiconductor layer 10. At least a part of the lower electrode 14 is in contact with the second face F2 of the semiconductor layer 10. In the transistor region 101, the lower electrode 14 functions as a collector electrode of the IGBT.

[0034] The lower electrode 14 is in contact with collector region 41 in transistor region 101. The lower electrode 14 is electrically connected to collector region 41 in transistor region 101.

[0035] The lower electrode 14 is, for example, a metal or a metal compound.

[0036] The collector region 41 is a p⁺-type semiconductor region. The collector region 41 is in contact with the second face F2. The collector region 41 is electrically connected to the lower electrode 14. The collector region 41 is in contact with the lower electrode 14. The collector region 41 serves as a source of holes when the IGBT is ON.

[0037] The collector region 41 contains p-type impurities. The p-type impurity is, for example, boron (B). The p-type impurity concentration in the collector region 41 is, for example, equal to or more than $1 \times 10^{18} \text{ cm}^{-3}$ and

equal to or less than $1 \times 10^{21} \text{ cm}^{-3}$.

[0038] The drift region 42 is an n⁻-type semiconductor region. The drift region 42 is provided between the collector region 41 and the first face F1.

[0039] The drift region 42 serves as an on-current path when the IGBT is ON. The drift region 42 has a function of being depleted when the IGBT is OFF to maintain the breakdown voltage of the IGBT.

[0040] The drift region 42 contains n-type impurities. The n-type impurity is, for example, phosphorus (P) or arsenic (As). The n-type impurity concentration in the drift region 42 is, for example, equal to or more than $1 \times 10^{15} \text{ cm}^{-3}$ and equal to or less than $1 \times 10^{18} \text{ cm}^{-3}$.

[0041] The base region 43 is a p⁻-type semiconductor region. The base region 43 is provided between the drift region 42 and the first face F1. The drift region 42 is interposed between the base region 43 and the collector region 41.

[0042] The depth of the base region 43 is, for example, equal to or less than 5 μm . In a region of the base region 43 facing the gate electrode 16, an n-type inversion layer is formed when the IGBT is ON. The base region 43 functions as a channel region of the IGBT.

[0043] The base region 43 contains p-type impurities. The p-type impurity is, for example, boron (B). The p-type impurity concentration in the base region 43 is, for example, equal to or more than $5 \times 10^{16} \text{ cm}^{-3}$ and equal to or less than $5 \times 10^{17} \text{ cm}^{-3}$.

[0044] The emitter region 44 is an n⁺-type semiconductor region. The emitter region 44 is provided between the base region 43 and the first face F1. The emitter region 44 is in contact with the first face F1.

[0045] The emitter region 44 is in contact with the gate trench 31 and the first dummy trench 32. The emitter region 44 is in contact with the gate insulating film 22 and the first insulating film 24.

[0046] The emitter region 44 is in contact with the first trench contact portion 12x of the upper electrode 12. The emitter region 44 is electrically connected to the upper electrode 12. The emitter region 44 serves as a source of electrons when the IGBT is ON.

[0047] The emitter region 44 contains n-type impurities. The n-type impurity is, for example, phosphorus (P) or arsenic (As). The n-type impurity concentration in the emitter region 44 is higher than the n-type impurity concentration in the drift region 42. The n-type impurity concentration in the emitter region 44 is, for example, equal to or more than $1 \times 10^{19} \text{ cm}^{-3}$ and equal to or less than $1 \times 10^{21} \text{ cm}^{-3}$.

[0048] The cell contact region 45 is a p⁺-type semiconductor region. The cell contact region 45 is provided between the base region 43 and the first face F1. The cell contact region 45 is in contact with the first face F1.

[0049] The cell contact region 45 is in contact with the gate trench 31 and the first dummy trench 32. The cell contact region 45 is in contact with the gate insulating film 22 and the first insulating film 24.

[0050] The cell contact region 45 is in contact with the

first trench contact portion 12x of the upper electrode 12. The cell contact region 45 is electrically connected to the upper electrode 12.

[0051] The cell contact region 45 contains p-type impurities. The p-type impurity is, for example, boron (B). The p-type impurity concentration in the cell contact region 45 is higher than the p-type impurity concentration in the base region 43. The p-type impurity concentration in the cell contact region 45 is, for example, equal to or more than $5 \times 10^{19} \text{ cm}^{-3}$ and equal to or less than $1 \times 10^{21} \text{ cm}^{-3}$.

[0052] As shown in Fig. 3, the emitter region 44 and the cell contact region 45 are alternately arranged in the first direction on the first face F1. The width of the emitter region 44 in the first direction on the first face F1 is smaller than the width of the cell contact region 45 in the first direction on the first face F1, for example.

[0053] The resistance reduction region 46 is a p-type semiconductor region. The resistance reduction region 46 is provided between the base region 43 and the emitter region 44. The resistance reduction region 46 is in contact with the base region 43 and the emitter region 44, for example.

[0054] The resistance reduction region 46 is provided between the base region 43 and the cell contact region 45, for example. The resistance reduction region 46 is in contact with the base region 43 and the cell contact region 45, for example. For example, the resistance reduction region 46 extends in the first direction.

[0055] The resistance reduction region 46 is in contact with the first trench contact portion 12x of the upper electrode 12. The resistance reduction region 46 is in contact with the side surfaces of the first trench contact portion 12x. The resistance reduction region 46 is electrically connected to the upper electrode 12.

[0056] The resistance reduction region 46 is spaced from the gate trench 31. The resistance reduction region 46 is spaced apart the gate insulating film 22. The resistance reduction region 46 is provided between the gate trench 31 and the first trench contact portion 12x, for example. For example, the base region 43 is provided between the resistance reduction region 46 and the gate trench 31. The base region 43 between the resistance reduction region 46 and the gate trench 31 functions as a channel region of the IGBT.

[0057] The resistance reduction region 46 is in contact with the first dummy trench 32. The resistance reduction region 46 is in contact with the first insulating film 24.

[0058] The depth of the resistance reduction region 46 is smaller than the depth of the first trench contact portion 12x.

[0059] The resistance reduction region 46 reduces the electrical resistance of the lower portion of the emitter region 44. The resistance reduction region 46 functions as a path for holes to escape to the upper electrode 12 when the IGBT is turned off. Since the resistance reduction region 46 is provided, the operation of the parasitic npn transistor is suppressed, so that the latch-up immu-

nity of the RC-IGBT 100 is improved. In addition, since the resistance reduction region 46 is in contact with the first dummy trench 32, the hole current is discharged along the sidewalls of the first dummy trench 32, so that the resistance reduction region 46 functions effectively. Therefore, the latch-up immunity can be improved compared to when the resistance reduction region 46 is not in contact with the first dummy trench 32.

[0060] The resistance reduction region 46 contains p-type impurities. The p-type impurity is, for example, boron (B). The p-type impurity concentration in the resistance reduction region 46 is higher than the p-type impurity concentration in the base region 43 and lower than the p-type impurity concentration in the cell contact region 45. The p-type impurity concentration of the resistance reduction region 46 is, for example, equal to or more than $5 \times 10^{17} \text{ cm}^{-3}$ and equal to or less than $1 \times 10^{19} \text{ cm}^{-3}$.

[0061] The barrier region 47 is an n-type semiconductor region. The barrier region 47 is provided between the drift region 42 and the base region 43.

[0062] The barrier region 47 has a function of promoting accumulation of carriers when the IGBT is ON to reduce the on-resistance.

[0063] The barrier region 47 contains n-type impurities. The n-type impurity is, for example, phosphorus (P) or arsenic (As). The n-type impurity concentration in the barrier region 47 is, for example, equal to or more than $5 \times 10^{15} \text{ cm}^{-3}$ and equal to or less than $5 \times 10^{18} \text{ cm}^{-3}$.

[0064] The gate trench 31 is provided on the first face F1 side of the semiconductor layer 10. The gate trench 31 is a groove provided in the semiconductor layer 10. The gate trench 31 is a part of the semiconductor layer 10.

[0065] As shown in Fig. 3, the gate trench 31 extends on the first face F1 in the first direction parallel to the first face F1. The gate trench 31 has a stripe shape. A plurality of gate trenches 31 are repeatedly arranged in the second direction perpendicular to the first direction.

[0066] The gate trench 31 is in contact with the drift region 42, the barrier region 47, the base region 43, the emitter region 44, and the cell contact region 45. The gate trench 31 is spaced from the resistance reduction region 46. This is because when the resistance reduction region 46 is in contact with the gate trench 31, the threshold voltage becomes higher than the desired value because the impurity concentration in the resistance reduction region 46 is higher than that in the base region 43, making driving difficult. The gate trench 31 passes through the base region 43 and the barrier region 47 to reach the drift region 42. The depth of the gate trench 31 is, for example, equal to or less than $8 \mu\text{m}$.

[0067] The gate electrode 16 is provided in the gate trench 31. The gate electrode 16 is, for example, a semiconductor or a metal. The gate electrode 16 is, for example, amorphous silicon or polycrystalline silicon containing n-type or p-type impurities. The gate electrode 16 is electrically connected to the gate electrode pad 103.

[0068] The gate insulating film 22 is provided between the gate electrode 16 and the semiconductor layer 10.

The gate insulating film 22 is provided between the gate electrode 16 and the drift region 42, between the gate electrode 16 and the base region 43, between the gate electrode 16 and the emitter region 44, and between the gate electrode 16 and the cell contact region 45. The gate insulating film 22 is, for example, a silicon oxide.

[0069] The first dummy trench 32 is provided on the first face F1 side of the semiconductor layer 10. The first dummy trench 32 is a groove provided in the semiconductor layer 10. The first dummy trench 32 is a part of the semiconductor layer 10.

[0070] As shown in Fig. 3, the first dummy trench 32 extends on the first face F1 in the first direction parallel to the first face F1. The first dummy trench 32 has a stripe shape. A plurality of first dummy trenches 32 are repeatedly arranged in the second direction perpendicular to the first direction. The first dummy trench 32 is provided between the two gate trenches 31 adjacent to each other.

[0071] The first dummy trench 32 is in contact with the drift region 42, the barrier region 47, the base region 43, the emitter region 44, the cell contact region 45, and the resistance reduction region 46. The first dummy trench 32 passes through the base region 43 and the barrier region 47 to reach the drift region 42. The depth of the first dummy trench 32 is, for example, equal to or less than 8 μm .

[0072] The first conductive layer 18 is provided in the first dummy trench 32. The first conductive layer 18 is, for example, a semiconductor or a metal. The first conductive layer 18 is, for example, amorphous silicon or polycrystalline silicon containing n-type impurities or p-type impurities.

[0073] The first conductive layer 18 is electrically connected to the upper electrode 12, for example. It is also possible to connect the first conductive layer 18 to an electrode other than the upper electrode 12 and apply a voltage different from the voltage for the upper electrode 12 to the first conductive layer 18. For example, the first conductive layer 18 may be electrically connected to the gate electrode pad 103.

[0074] The first insulating film 24 is provided between the first conductive layer 18 and the semiconductor layer 10. The first insulating film 24 is provided between the first conductive layer 18 and the drift region 42, between the first conductive layer 18 and the base region 43, between the first conductive layer 18 and the emitter region 44, between the first conductive layer 18 and the cell contact region 45, and between the first conductive layer 18 and the resistance reduction region 46. The first insulating film 24 is, for example, a silicon oxide.

[0075] The interlayer insulating layer 28 is provided between the gate electrode 16 and the upper electrode 12. The interlayer insulating layer 28 electrically isolates the gate electrode 16 and the upper electrode 12 from each other. For example, the first conductive layer 18 and the upper electrode 12 are electrically connected to each other by using an opening provided in the interlayer insulating layer 28. The interlayer insulating layer 28 is,

for example, a silicon oxide.

[0076] The diode region 102 includes the semiconductor layer 10, the upper electrode 12 (first electrode), the lower electrode 14 (second electrode), the second conductive layer 20, and the second insulating film 26.

[0077] In the semiconductor layer 10 of the diode region 102, the second dummy trench 33 (third trench), the drift region 42 (second semiconductor region), the cathode region 51 (seventh semiconductor region), the anode region 52 (eighth semiconductor region), and the diode contact region 53 (ninth semiconductor region) are provided.

[0078] In the diode region 102, the upper electrode 12 functions as an anode electrode of the diode. The upper electrode 12 is in contact with the anode region 52 and the diode contact region 53. The upper electrode 12 is electrically connected to the anode region 52 and the diode contact region 53.

[0079] The contact between the upper electrode 12 and the diode contact region 53 is, for example, an ohmic contact. In addition, the contact between the upper electrode 12 and the anode region 52 is, for example, a Schottky contact.

[0080] The upper electrode 12 and the anode region 52 are in contact with each other on the first face F1. The position where the upper electrode 12 and the anode region 52 are in contact with each other is shallower than the depth of the diode contact region 53.

[0081] In the diode region 102, the lower electrode 14 functions as a cathode electrode of the diode. The lower electrode 14 is in contact with the cathode region 51.

[0082] The cathode region 51 is an n⁺-type semiconductor region. The cathode region 51 is in contact with the second face F2. The cathode region 51 serves as a source of electrons when the diode is ON. The cathode region 51 is in contact with the lower electrode 14.

[0083] The drift region 42 is an n-type semiconductor region. The drift region 42 is provided between the cathode region 51 and the first face F1. The n-type impurity concentration in the drift region 42 is lower than the n-type impurity concentration in the cathode region 51.

[0084] The drift region 42 serves as an on-current path when the diode is ON.

[0085] The anode region 52 is a p-type semiconductor region. The anode region 52 is provided between the drift region 42 and the first face F1. The drift region 42 is interposed between the anode region 52 and the cathode region 51.

[0086] The anode region 52 serves as a source of holes when the diode is ON.

[0087] The diode contact region 53 is a p⁺-type semiconductor region. The diode contact region 53 is provided between the anode region 52 and the first face F1.

[0088] The diode contact region 53 is in contact with the upper electrode 12. The diode contact region 53 is electrically connected to the upper electrode 12.

[0089] The p-type impurity concentration in the diode contact region 53 is higher than the p-type impurity con-

centration in the anode region 52.

[0090] The second dummy trench 33 is provided on the first face F1 side of the semiconductor layer 10. The second dummy trench 33 is a groove provided in the semiconductor layer 10. The second dummy trench 33 is a part of the semiconductor layer 10.

[0091] As shown in Fig. 3, the second dummy trench 33 extends on the first face F1 in the first direction parallel to the first face F1. The second dummy trench 33 has a stripe shape. A plurality of second dummy trenches 33 are repeatedly arranged in the second direction perpendicular to the first direction.

[0092] The second dummy trench 33 is in contact with the drift region 42, the anode region 52, and the diode contact region 53. The second dummy trench 33 passes through the anode region 52 to reach the drift region 42. The depth of the second dummy trench 33 is, for example, equal to or less than 8 μm .

[0093] The second conductive layer 20 is provided in the second dummy trench 33. The second conductive layer 20 is, for example, a semiconductor or a metal. The second conductive layer 20 is, for example, amorphous silicon or polycrystalline silicon containing n-type impurities or p-type impurities.

[0094] The second conductive layer 20 is electrically connected to the upper electrode 12, for example. It is also possible to connect the second conductive layer 20 to an electrode other than the upper electrode 12 and apply a voltage different from the voltage for the upper electrode 12 to the second conductive layer 20.

[0095] The second insulating film 26 is provided between the second conductive layer 20 and the semiconductor layer 10. The second insulating film 26 is provided between the second conductive layer 20 and the drift region 42, between the second conductive layer 20 and the anode region 52, and between the second conductive layer 20 and the diode contact region 53. The second insulating film 26 is in contact with the drift region 42, the anode region 52, and the diode contact region 53. The second insulating film 26 is, for example, a silicon oxide.

[0096] The interlayer insulating layer 28 is provided between the second conductive layer 20 and the upper electrode 12. For example, the second conductive layer 20 and the upper electrode 12 are electrically connected to each other by using an opening provided in the interlayer insulating layer 28.

[0097] The gate electrode pad 103 is provided on the first face F1 side of the semiconductor layer 10. The gate electrode pad 103 is electrically connected to the gate electrode 16. The gate electrode pad 103 and the gate electrode 16 are connected to each other by using, for example, a metal wiring (not shown).

[0098] A gate voltage is applied to the gate electrode pad 103.

[0099] Next, the function and effect of the semiconductor device according to the first embodiment will be described.

[0100] In the RC-IGBT 100 according to the first em-

bodiment, it is possible to achieve both a reduction in switching loss and an improvement in latch-up immunity. The RC-IGBT 100 includes the first trench contact portion 12x and the resistance reduction region 46 in the transistor region 101. Then, the bottom surface of the first trench contact portion 12x is in contact with the base region 43. In particular, since the RC-IGBT 100 has the above configuration, it is possible to achieve both a reduction in switching loss and an improvement in latch-up immunity. Details description will be given below.

[0101] Fig. 5 is a schematic cross-sectional view of a part of a semiconductor device according to a comparative example. Fig. 5 is a cross-sectional view taken along the line XX' of Fig. 6. Fig. 5 is a diagram corresponding to Fig. 2 in the first embodiment.

[0102] Fig. 6 is a schematic top view of a part of the semiconductor device according to the comparative example.

[0103] Fig. 6 is a top view on the first face F1. Fig. 6 is a diagram corresponding to Fig. 3 according to the first embodiment.

[0104] Fig. 7 is a schematic cross-sectional view of a part of the semiconductor device according to the comparative example. Fig. 7 is a cross-sectional view taken along the line YY' of Fig. 6. Fig. 7 is a diagram corresponding to Fig. 4 in the first embodiment.

[0105] The semiconductor device according to the comparative example is an RC-IGBT 900. The RC-IGBT 900 is different from the RC-IGBT 100 according to the first embodiment in that the resistance reduction region 46 is not provided and a p-type region 55 is provided.

[0106] The p-type region 55 is a p-type semiconductor region. The p-type region 55 is provided between the base region 43 and the first trench contact portion 12x. The p-type region 55 is in contact with the bottom surface of the first trench contact portion 12x.

[0107] The p-type impurity concentration in the p-type region 55 is higher than the p-type impurity concentration in the base region 43. The contact between the first trench contact portion 12x and the p-type region 55 is, for example, an ohmic contact.

[0108] The RC-IGBT 900 according to the comparative example includes the p-type region 55 in contact with the bottom surface of the first trench contact portion 12x. Providing the p-type region 55 promotes the discharge of holes from the p-type region 55 to the upper electrode 12 when the IGBT is turned off. Therefore, the operation of the parasitic npn transistor in the transistor region is suppressed. As a result, the latch-up immunity of the RC-IGBT 900 is improved.

[0109] Fig. 8 is an explanatory diagram of a problem of the semiconductor device according to the comparative example. Fig. 8 is a diagram corresponding to Fig. 5. Fig. 8 is a diagram showing the flow of holes during steady operation of the diode.

[0110] As shown in Fig. 8, in the transistor region 101 near the boundary with the diode region 102, the amount of holes injected from the base region 43 into the drift

region 42 during steady operation of the diode is large. Therefore, during steady operation of the diode, the amount of holes injected from the transistor region 101 into the drift region 42 of the diode region 102 increases.

[0111] The reason why the amount of holes injected into the transistor region 101 of the RC-IGBT 900 according to the comparative example is large is considered to be that the amount of holes injected from the p-type region 55 at the bottom of the first trench contact portion 12x is large.

[0112] Fig. 9 is an explanatory diagram of the function and effect of the semiconductor device according to the first embodiment. Fig. 9 is a diagram corresponding to Fig. 2. Fig. 9 is a diagram showing the flow of holes during steady operation of the diode.

[0113] As shown in Fig. 9, the amount of holes injected into the transistor region 101 near the boundary with the diode region 102 is smaller than that in the comparative example. The RC-IGBT 100 according to the first embodiment does not include the p-type region 55 at the bottom of the first trench contact portion 12x. Therefore, it is considered that holes are not injected from the bottom of the first trench contact portion 12x.

[0114] In addition, in the RC-IGBT 100 according to the first embodiment, during steady operation of the diode, electrons are discharged to the upper electrode 12 through the contact surface between the bottom surface of the first trench contact portion 12x and the base region 43, which make a Schottky contact therebetween. Therefore, it is considered that the injection of holes from the base region 43 into the drift region 42 is suppressed.

[0115] Fig. 10 is an explanatory diagram of the function and effect of the semiconductor device according to the first embodiment. Fig. 10 is a diagram showing the current characteristics of diodes in the RC-IGBT 100 according to the first embodiment and the RC-IGBT 900 according to the comparative example.

[0116] As the amount of holes injected into the diode region 102 from the transistor region 101 near the boundary with the diode region 102 during steady operation of the diode increases, the amount of holes to be discharged to the upper electrode 12 when the diode is turned off increases. As the amount of holes to be discharged from the upper electrode 12 increases, the reverse recovery current of the diode increases. As the reverse recovery current of the diode increases, the switching loss of the diode increases.

[0117] In the RC-IGBT 100 according to the first embodiment, the amount of holes injected from the transistor region 101 into the diode region 102 during steady operation of the diode is smaller than that in the RC-IGBT 900 according to the comparative example. Therefore, as shown in Fig. 10, the reverse recovery current of the diode in the RC-IGBT 100 according to the first embodiment is smaller than that in the RC-IGBT 900 according to the comparative example. As a result, in the RC-IGBT 100 according to the first embodiment, the switching loss of the diode is reduced.

[0118] The RC-IGBT 100 according to the first embodiment does not include the p-type region 55 at the bottom of the first trench contact portion 12x. However, the RC-IGBT 100 includes the p-type resistance reduction region 46 between the base region 43 and the emitter region 44. The p-type resistance reduction region 46 is in contact with the side surfaces of the first trench contact portion 12x.

[0119] Since the RC-IGBT 100 according to the first embodiment includes the resistance reduction region 46 in contact with the side surfaces of the first trench contact portion 12x, the discharge of holes from the resistance reduction region 46 to the upper electrode 12 when the IGBT is turned off is promoted. Therefore, the operation of the parasitic npn transistor in the transistor region 101 is suppressed. As a result, the latch-up immunity of the RC-IGBT 100 is improved.

[0120] As described above, according to the RC-IGBT 100 according to the first embodiment, it is possible to achieve both a reduction in switching loss and an improvement in latch-up immunity.

[0121] From the viewpoint of promoting the discharge of holes from the resistance reduction region 46 to the upper electrode 12, it is preferable that the p-type impurity concentration in the resistance reduction region 46 is high. The p-type impurity concentration in the resistance reduction region 46 is higher than the p-type impurity concentration in the base region 43. The p-type impurity concentration in the resistance reduction region 46 is preferably equal to or more than $5 \times 10^{17} \text{ cm}^{-3}$, more preferably equal to or more than $1 \times 10^{18} \text{ cm}^{-3}$, and even more preferably equal to or more than $5 \times 10^{18} \text{ cm}^{-3}$.

[0122] From the viewpoint of stabilizing the threshold voltage of the IGBT, it is preferable that the p-type impurity concentration of the resistance reduction region 46 adjacent to the channel region of the IGBT is low. The p-type impurity concentration of the resistance reduction region 46 is lower than the p-type impurity concentration of the cell contact region 45. The p-type impurity concentration of the resistance reduction region 46 is preferably equal to or less than $1 \times 10^{19} \text{ cm}^{-3}$.

[0123] From the viewpoint of facilitating the formation of the resistance reduction region 46, it is preferable to provide the first dummy trench 32 in contact with the resistance reduction region 46. Since the width of the resistance reduction region 46 in the second direction can be increased, it becomes easy to form the resistance reduction region 46.

[0124] From the viewpoint of improving the latch-up immunity, it is preferable to provide the first dummy trench 32. In particular, since the first conductive layer 18 in the first dummy trench 32 is electrically connected to the upper electrode 12, holes easily flow along the side surfaces of the first dummy trench 32 when the IGBT is turned off. Therefore, the discharge of holes from the resistance reduction region 46 to the upper electrode 12 is promoted. As a result, the latch-up immunity of the RC-IGBT 100 is improved.

[0125] From the viewpoint of improving the latch-up immunity, it is preferable that the width of the emitter region 44 in the first direction is small. From the viewpoint of improving the latch-up immunity, it is preferable that the width of the emitter region 44 in the first direction on the first face F1 is smaller than the width of the cell contact region 45 in the first direction on the first face F1. In addition, by adjusting the width of the emitter region 44 and the width of the cell contact region 45 to adjust the transconductance, it is possible to increase the short circuit withstand time.

[0126] From the viewpoint of promoting the discharge of electrons to the upper electrode 12 during steady operation of the diode and suppressing the injection of holes into the drift region 42, it is preferable that the base region 43 is in contact with the side surfaces of the first trench contact portion 12x.

[0127] In addition, although the case where there are one transistor region 101 and one diode region 102 has been exemplified in Fig. 1, each of the transistor region 101 and the diode region 102 may be divided into a plurality of regions and arranged alternately. By dividing each of the transistor region 101 and the diode region 102 into a plurality of regions, the generation of heat in the IGBT and the diode can be made uniform.

(First Modification Example)

[0128] A semiconductor device according to a first modification example of the first embodiment is different from the semiconductor device according to the first embodiment in that the diode region further includes a tenth semiconductor region between the second semiconductor region and the eighth semiconductor region.

[0129] Fig. 11 is a schematic cross-sectional view of a part of the semiconductor device according to the first modification example of the first embodiment. Fig. 11 is a cross-sectional view taken along the line CC' of Fig. 12. Fig. 11 is a diagram corresponding to Fig. 2 in the first embodiment.

[0130] Fig. 12 is a schematic top view of a part of the semiconductor device according to the first modification example of the first embodiment. Fig. 12 is a top view on the first face F1. Fig. 12 is a diagram corresponding to Fig. 3 in the first embodiment.

[0131] Fig. 13 is a schematic cross-sectional view of a part of the semiconductor device according to the first modification example of the first embodiment. Fig. 13 is a cross-sectional view taken along the line DD' of Fig. 12. Fig. 13 is a diagram corresponding to Fig. 4 according to the first embodiment.

[0132] The semiconductor device according to the first modification example of the first embodiment is an RC-IGBT 110. The RC-IGBT 110 is different from the RC-IGBT 100 according to the first embodiment in that the diode region 102 includes the barrier region 47.

[0133] The barrier region 47 is an n-type semiconductor region. The barrier region 47 is provided between the

drift region 42 and the anode region 52.

[0134] The barrier region 47 contains n-type impurities. The n-type impurity is, for example, phosphorus (P) or arsenic (As). The n-type impurity concentration in the barrier region 47 is, for example, equal to or more than $5 \times 10^{15} \text{ cm}^{-3}$ and equal to or less than $5 \times 10^{18} \text{ cm}^{-3}$.

[0135] The barrier region 47 has a function of suppressing the injection of holes into the drift region 42 when the diode is ON. Therefore, the amount of holes to be discharged to the upper electrode 12 when the diode is turned off is reduced. As the amount of holes to be discharged from the upper electrode 12 decreases, the reverse recovery current of the diode decreases. As the reverse recovery current of the diode decreases, the switching loss of the diode decreases.

[0136] Therefore, according to the RC-IGBT 110 according to the first modification example of the first embodiment, it is possible to further reduce the switching loss.

(Second Modification Example)

[0137] A semiconductor device according to a second modification example of the first embodiment is different from the semiconductor device according to the first embodiment in that the diode region further includes an eleventh semiconductor region of the first conductive type having a first conductive type impurity concentration higher than that in the eighth semiconductor region, the first electrode of the diode region includes a second portion, side surfaces of the second portion are in contact with the eighth semiconductor region, a bottom surface of the second portion is in contact with the eleventh semiconductor region, and the eleventh semiconductor region is provided between the eighth semiconductor region and the second portion.

[0138] Fig. 14 is a schematic cross-sectional view of a part of a semiconductor device according to a second modification example of the first embodiment. Fig. 14 is a cross-sectional view taken along the line EE' of Fig. 15. Fig. 14 is a diagram corresponding to Fig. 2 in the first embodiment.

[0139] Fig. 15 is a schematic top view of a part of the semiconductor device according to the second modification example of the first embodiment. Fig. 15 is a top view on the first face F1. Fig. 15 is a diagram corresponding to Fig. 3 in the first embodiment.

[0140] Fig. 16 is a schematic cross-sectional view of a part of the semiconductor device according to the second modification example of the first embodiment. Fig. 16 is a cross-sectional view taken along the line FF' of Fig. 15. Fig. 16 is a diagram corresponding to Fig. 4 in the first embodiment.

[0141] The semiconductor device according to the second modification example of the first embodiment is an RC-IGBT 120. The RC-IGBT 120 is different from the RC-IGBT 100 according to the first embodiment in that the diode region 102 includes a trench bottom p-type

region 56 (eleventh semiconductor region) and the upper electrode 12 of the diode region 102 has a second trench contact portion 12y (second portion).

[0142] The second trench contact portion 12y is formed in a trench provided in the semiconductor layer 10. The second trench contact portion 12y extends in the first direction.

[0143] The bottom surface of the second trench contact portion 12y is in contact with the trench bottom p-type region 56. The side surfaces of the second trench contact portion 12y are in contact with the anode region 52. The second trench contact portion 12y is electrically connected to the trench bottom p-type region 56 and the anode region 52.

[0144] The trench bottom p-type region 56 is a p-type semiconductor region. The trench bottom p-type region 56 is provided between the anode region 52 and the second trench contact portion 12y. The trench bottom p-type region 56 is in contact with the second trench contact portion 12y.

[0145] The p-type impurity concentration in the trench bottom p-type region 56 is higher than the p-type impurity concentration in the anode region 52. The contact between the second trench contact portion 12y and the trench bottom p-type region 56 is, for example, an ohmic contact.

[0146] According to the RC-IGBT 120 according to the second modification example of the first embodiment, for example, the first trench contact portion 12x of the transistor region 101 and the second trench contact portion 12y of the diode region 102 can be manufactured through a common process.

[0147] As described above, according to the first embodiment and its modification examples, it is possible to provide semiconductor devices that can achieve both a reduction in switching loss and an improvement in latch-up immunity.

(Second Embodiment)

[0148] A semiconductor device according to a second embodiment is different from the semiconductor device according to the first embodiment in that the transistor region does not include the second trench. Hereinafter, the description of a part of the content overlapping the first embodiment may be omitted.

[0149] The semiconductor device according to the second embodiment is an RC-IGBT 200 in which an IGBT and a freewheeling diode are formed in the same semiconductor chip. The RC-IGBT 200 has a trench gate type IGBT including a gate electrode in a trench formed in a semiconductor layer. Hereinafter, a case where the first conductive type is p-type and the second conductive type is n-type will be described as an example.

[0150] Fig. 17 is a schematic cross-sectional view of a part of the semiconductor device according to the second embodiment. Fig. 17 is a cross-sectional view taken along the line GG' of Fig. 18. Fig. 17 is a diagram corre-

sponding to Fig. 2 in the first embodiment.

[0151] Fig. 18 is a schematic top view of a part of the semiconductor device according to the second embodiment.

[0152] Fig. 18 is a top view on the first face F1. Fig. 18 is a diagram corresponding to Fig. 3 in the first embodiment.

[0153] Fig. 19 is a schematic cross-sectional view of a part of the semiconductor device according to the second embodiment. Fig. 19 is a cross-sectional view taken along the line HH' of Fig. 18. Fig. 19 is a diagram corresponding to Fig. 4 in the first embodiment.

[0154] The semiconductor device according to the second embodiment is the RC-IGBT 200. The RC-IGBT 200 has a transistor region 101 and a diode region 102.

[0155] The transistor region 101 operates as an IGBT. The diode region 102 operates as a freewheeling diode.

[0156] The RC-IGBT 200 according to the second embodiment includes a semiconductor layer 10, an upper electrode 12 (first electrode), a lower electrode 14 (second electrode), a gate electrode 16, a second conductive layer 20, a gate insulating film 22, a second insulating film 26, an interlayer insulating layer 28, and a gate electrode pad 103.

[0157] The upper electrode 12 has a first trench contact portion 12x (first portion).

[0158] In the semiconductor layer 10, a gate trench 31 (first trench), a second dummy trench 33 (third trench), a collector region 41 (first semiconductor region), a drift region 42 (second semiconductor region), a base region 43 (third semiconductor region), an emitter region 44 (fourth semiconductor region), a cell contact region 45 (fifth semiconductor region), a resistance reduction region 46 (sixth semiconductor region), a barrier region 47 (tenth semiconductor region), a cathode region 51 (seventh semiconductor region), an anode region 52 (eighth semiconductor region), and a diode contact region 53 (ninth semiconductor region) are provided.

[0159] In the RC-IGBT 200 according to the second embodiment, it is possible to achieve both a reduction in switching loss and an improvement in latch-up immunity, as in the RC-IGBT 100 according to the first embodiment.

[0160] In addition, in the RC-IGBT 200 according to the second embodiment, the occupation rate of the gate trench 31 in the transistor region 101 is higher than that in the RC-IGBT 100 according to the first embodiment. Therefore, for example, it is possible to realize the RC-IGBT 200 with lower on-resistance and higher on-current than the RC-IGBT 100 according to the first embodiment.

[0161] As described above, according to the second embodiment, it is possible to provide a semiconductor device that can achieve both a reduction in switching loss and an improvement in latch-up immunity.

[0162] In the first and second embodiments, the case where the semiconductor layer is single crystal silicon has been described as an example. However, the semiconductor layer is not limited to the single crystal silicon. For example, other single crystal semiconductors, such as single crystal silicon carbide, may be used.

[0163] In the first and second embodiments, the case where the first conductive type is p-type and the second conductive type is n-type has been described as an example. However, the first conductive type can be n-type and the second conductive type can be p-type. 5

[0164] In the first and second embodiments, the case where the second dummy trench 33 is provided in the diode region 102 has been described as an example. However, it is also possible not to provide the second dummy trench 33 in the diode region 102. 10

[0165] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the semiconductor device described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the devices and methods described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions. 15 20

[0166] It is explicitly stated that all features disclosed in the description and/or the claims are intended to be disclosed separately and independently from each other for the purpose of original disclosure as well as for the purpose of restricting the claimed invention independent of the composition of the features in the embodiments and/or the claims. It is explicitly stated that all value ranges or indications of groups of entities disclose every possible intermediate value or intermediate entity for the purpose of original disclosure as well as for the purpose of restricting the claimed invention, in particular as limits of value ranges. 25 30 35

Claims

1. A semiconductor device (100,110,120,200), comprising: 40
 - a transistor region (101) including:
 - a semiconductor layer (10) having a first face (F1) and a second face (F2) opposite to the first face (F1); 45
 - a first semiconductor region (41) of a first conductive type provided in the semiconductor layer (10);
 - a second semiconductor region (42) of a second conductive type provided in the semiconductor layer (10) and provided between the first semiconductor region (41) and the first face (F1); 50
 - a third semiconductor region (43) of the first conductive type provided in the semiconductor layer (10) and provided between the second semiconductor region (42) and the 55

first face (F1);

a fourth semiconductor region (44) of the second conductive type and a fifth semiconductor region (45) of the first conductive type provided in the semiconductor layer (10), provided between the third semiconductor region (43) and the first face (F1), and arranged alternately in a first direction parallel to the first face (F1);

a sixth semiconductor region (46) of the first conductive type provided between the third semiconductor region (43) and the fourth semiconductor region (44) and having a first conductive type impurity concentration higher than a first conductive type impurity concentration in the third semiconductor region (43) and lower than a first conductive type impurity concentration in the fifth semiconductor region (45);

a first trench (31) provided on a first face side in the semiconductor layer (10), extending in the first direction, repeatedly arranged in a second direction parallel to the first face (F1) and perpendicular to the first direction, in contact with the second semiconductor region (42), the third semiconductor region (43), the fourth semiconductor region (44), and the fifth semiconductor region (45), and spaced from the sixth semiconductor region (46);

a gate electrode (16) provided in the first trench (31);

a gate insulating film (22) provided between the gate electrode (16) and the third semiconductor region (43);

a first electrode (12) provided on the first face side with respect to the semiconductor layer (10) and having a first portion (12x), a bottom surface of the first portion (12x) being in contact with the third semiconductor region (43) and side surfaces of the first portion (12x) being in contact with the fourth semiconductor region (43), the fifth semiconductor region (45), and the sixth semiconductor region (46); and

a second electrode (14) provided on a second face side with respect to the semiconductor layer (10) and in contact with the first semiconductor region (41); and

a diode region including (102):

the semiconductor layer (10);

the second semiconductor region (42);

a seventh semiconductor region (51) of the second conductive type provided in the semiconductor layer (10), provided between the second semiconductor region (42) and the

- (42) and the second face (F2), and having a second conductive type impurity concentration higher than a second conductive type impurity concentration in the second semiconductor region (42);
 an eighth semiconductor region (52) of the first conductive type provided in the semiconductor layer (10) and provided between the second semiconductor region (42) and the first face (F2);
 the first electrode (12) electrically connected to the eighth semiconductor region (52); and
 the second electrode (14) in contact with the seventh semiconductor region (51).
2. The semiconductor device (100,110,120,200) according to claim 1,
 wherein the sixth semiconductor region (46) extends in the first direction, and the fifth semiconductor region (45) is provided between the sixth semiconductor region (46) and the first face (F1).
 3. The semiconductor device (100,110,120,200) according to claim 1 or 2,
 wherein the sixth semiconductor region (46) is provided between the first trench (31) and the first portion (12x).
 4. The semiconductor device (100,110,120) according to any one of claims 1 to 3,
 wherein the transistor region (101) further includes:
 a second trench (32) provided on the first face side in the semiconductor layer (10), provided between two adjacent first trenches (31), extending in the first direction, and in contact with the second semiconductor region (42), the third semiconductor region (43), the fourth semiconductor region (44), the fifth semiconductor region (45), and the sixth semiconductor region (46);
 a first conductive layer (18) provided in the second trench (32); and
 a first insulating film (24) provided between the first conductive layer (18) and the third semiconductor region (43).
 5. The semiconductor device (100,110,120) according to claim 4,
 wherein the first conductive layer (18) is electrically connected to the first electrode (12).
 6. The semiconductor device (100,110,120,200) according to any one of claims 1 to 5,
 wherein a width of the fourth semiconductor region (44) in the first direction is smaller than a width of the fifth semiconductor region (45) in the first direction.
 7. The semiconductor device (100,110,120,200) according to any one of claims 1 to 6,
 wherein the diode region (102) further includes a ninth semiconductor region (53) of the first conductive type provided in the semiconductor layer (10), provided between the eighth semiconductor region (52) and the first face (F1), and having a first conductive type impurity concentration higher than a first conductive type impurity concentration in the eighth semiconductor region (52), and
 the first electrode (12) is in contact with the ninth semiconductor region (53).
 8. The semiconductor device (100,110,120,200) according to any one of claims 1 to 7,
 wherein the transistor region (101) further includes a tenth semiconductor region (47) of the second conductive type provided between the second semiconductor region (42) and the third semiconductor region (43) and having a second conductive type impurity concentration higher than a second conductive type impurity concentration in the second semiconductor region (42).
 9. The semiconductor device (110) according to claim 8,
 wherein the diode region (102) further includes the tenth semiconductor region (47) provided between the second semiconductor region (42) and the eighth semiconductor region (52).
 10. The semiconductor device (120) according to any one of claims 1 to 9,
 wherein the diode region (102) further includes an eleventh semiconductor region (56) of the first conductive type having a first conductive type impurity concentration higher than a first conductive type impurity concentration in the eighth semiconductor region (52),
 the first electrode (12) of the diode region (102) includes a second portion (12y), side surfaces of the second portion (12y) are in contact with the eighth semiconductor region (52), and a bottom surface of the second portion (12y) is in contact with the eleventh semiconductor region (56), and
 the eleventh semiconductor region (56) is provided between the eighth semiconductor region (52) and the second portion (12y).
 11. The semiconductor device (100,110,120,200) according to any one of claims 1 to 10,
 wherein the diode region (102) further includes:
 a third trench (33) provided on the first face side

in the semiconductor layer (10), extending in the first direction, and in contact with the second semiconductor region (42) and the eighth semiconductor region (52);
a second conductive layer (20) provided in the third trench (33); and
a second insulating film (26) provided between the second conductive layer (20) and the eighth semiconductor region (52).

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- 12.** The semiconductor device (100,110,120,200) according to claim 11,
wherein the second conductive layer (20) is electrically connected to the first electrode (12).

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- 13.** The semiconductor device (100,110,120,200) according to any one of claims 1 to 12,
wherein the side surfaces of the first portion (12x) are in contact with the third semiconductor region (43).

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- 14.** The semiconductor device (100,110,120,200) according to any one of claims 1 to 13,
wherein a depth of the sixth semiconductor region (46) is smaller than a depth of the first portion (12x).

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FIG.1

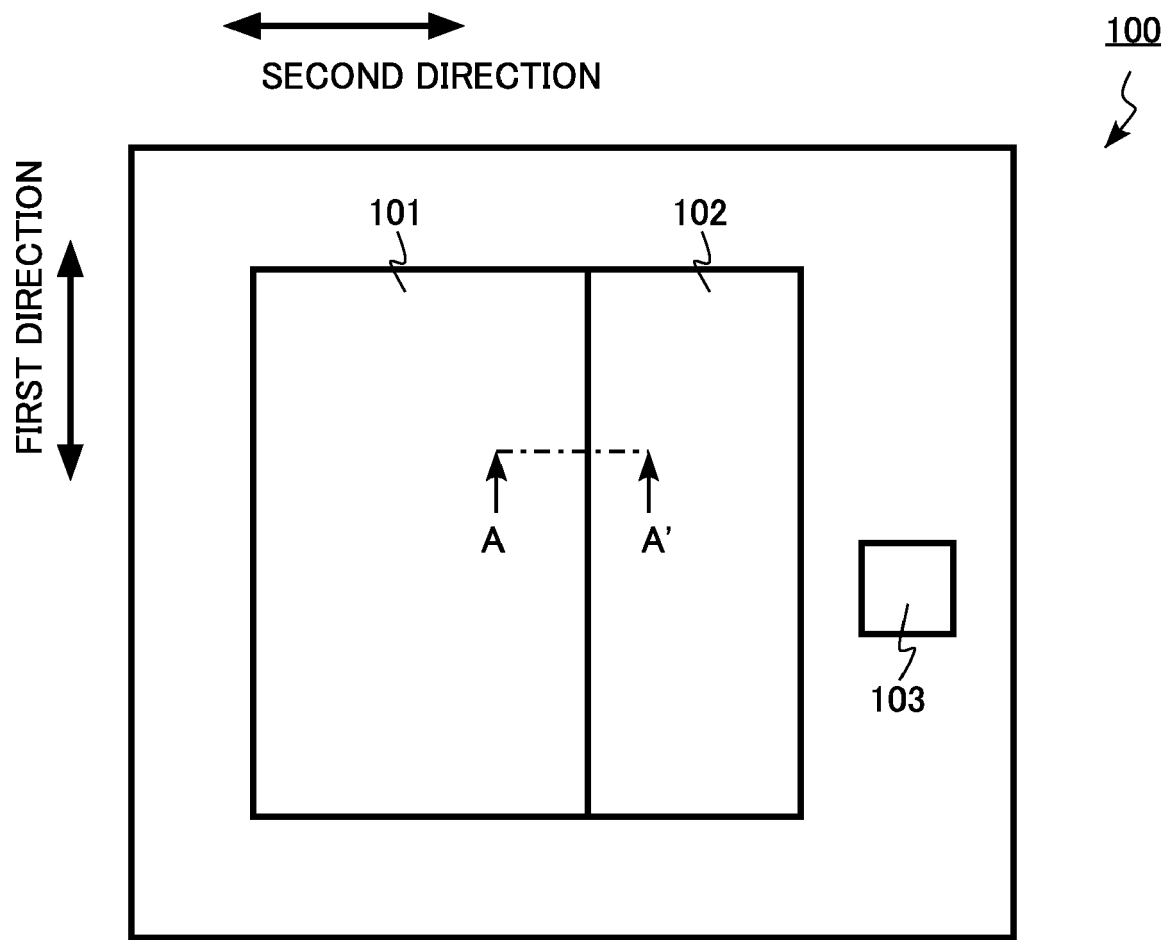
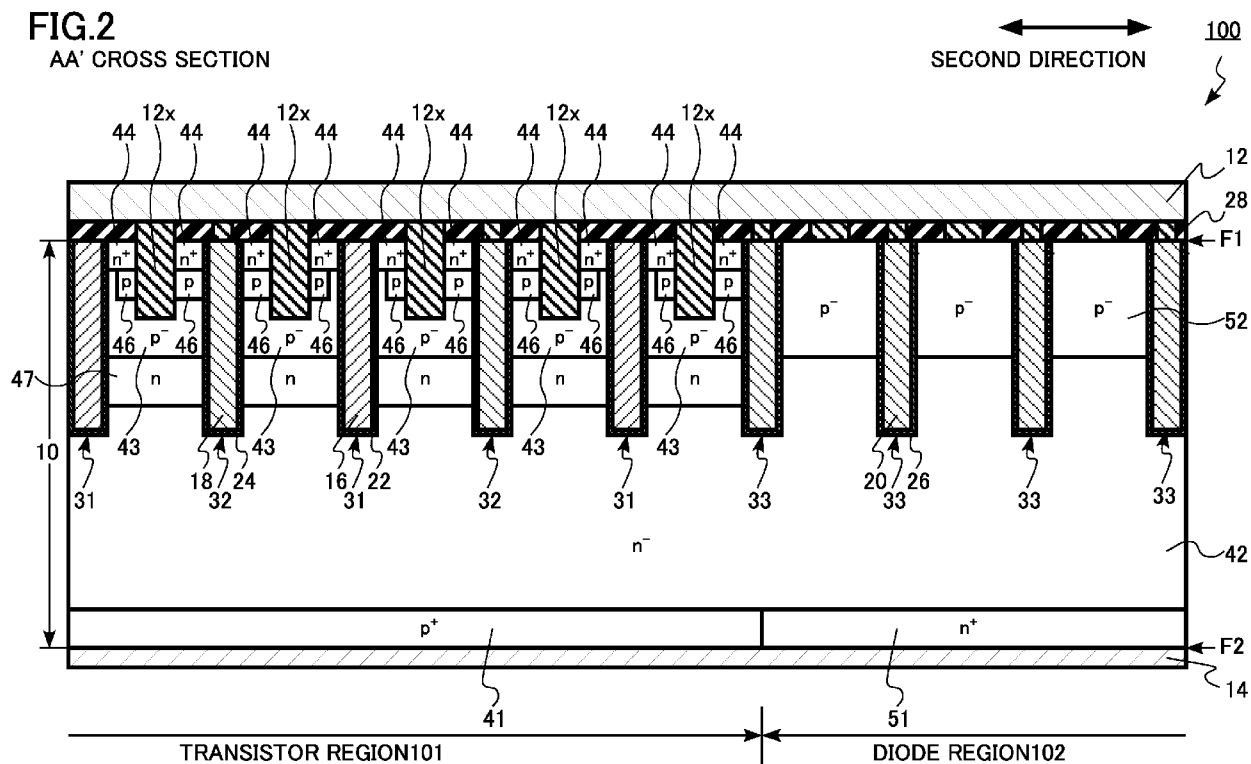


FIG.2
AA' CROSS SECTION



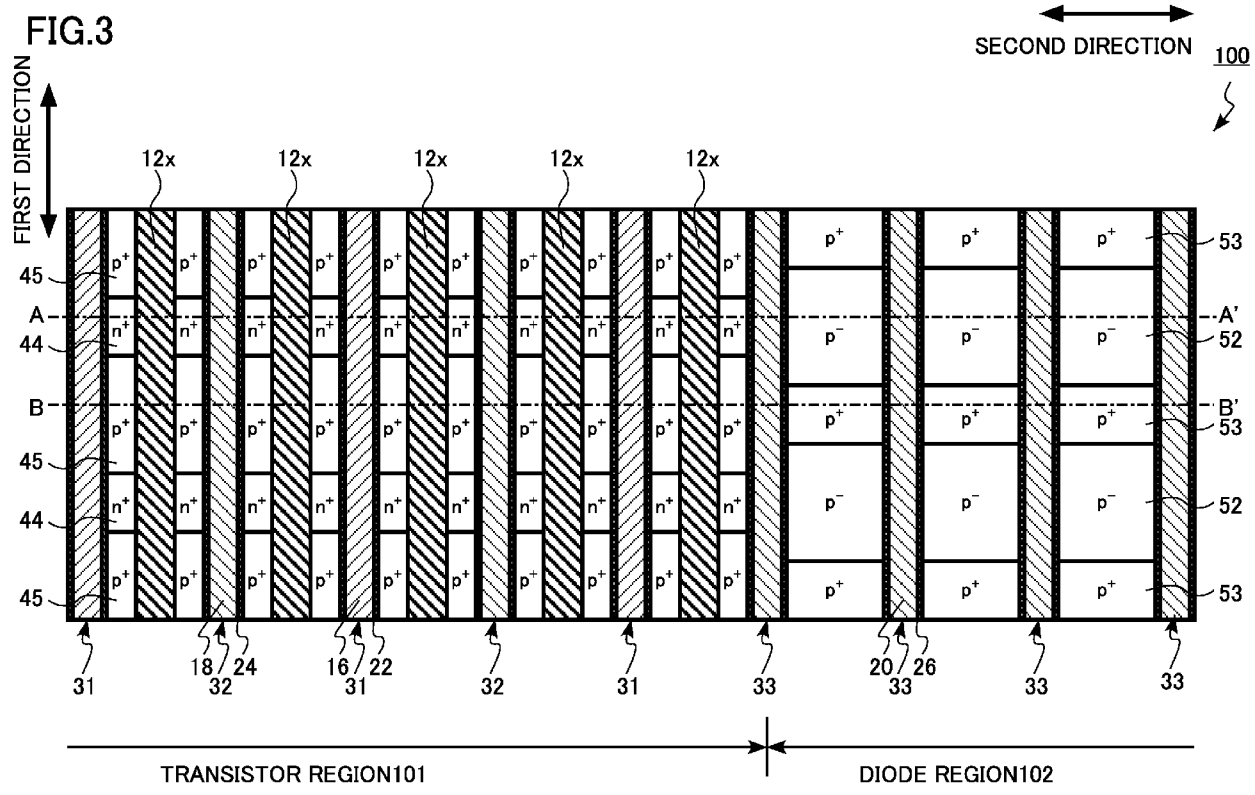


FIG.4
BB' CROSS SECTION

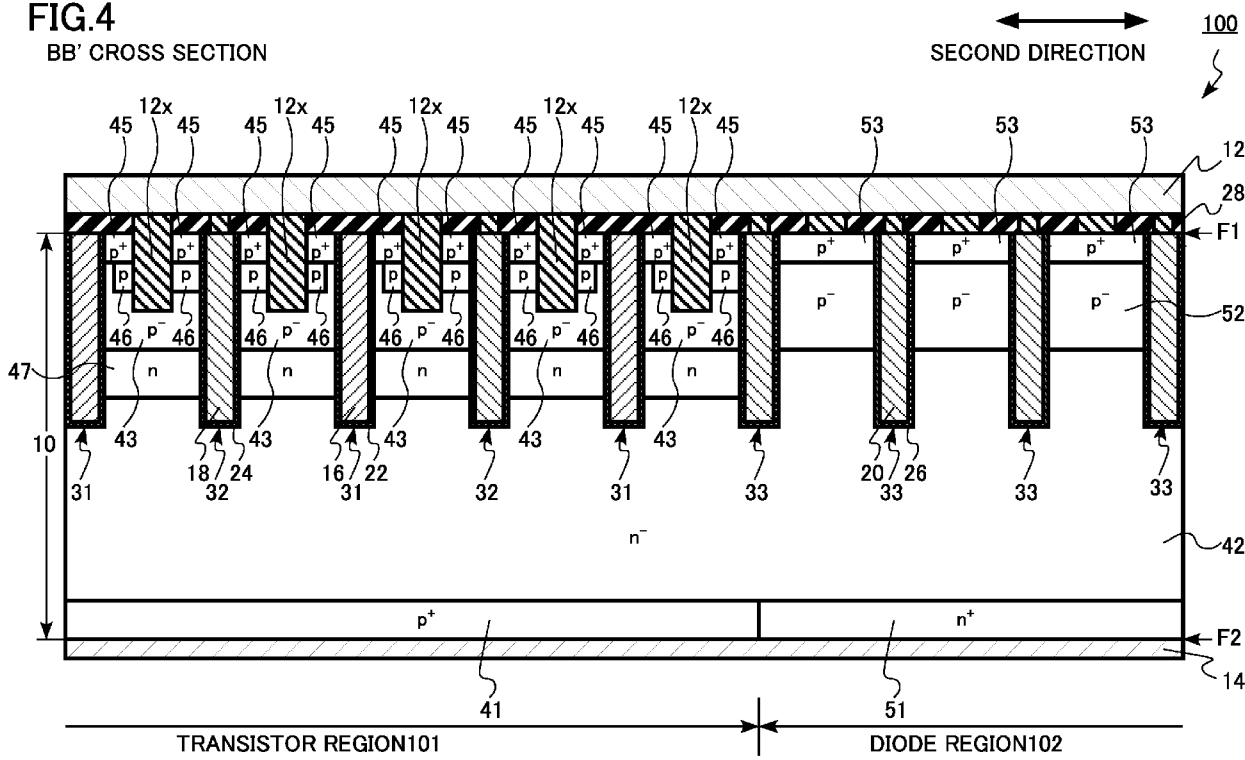


FIG.5
XX' CROSS SECTION

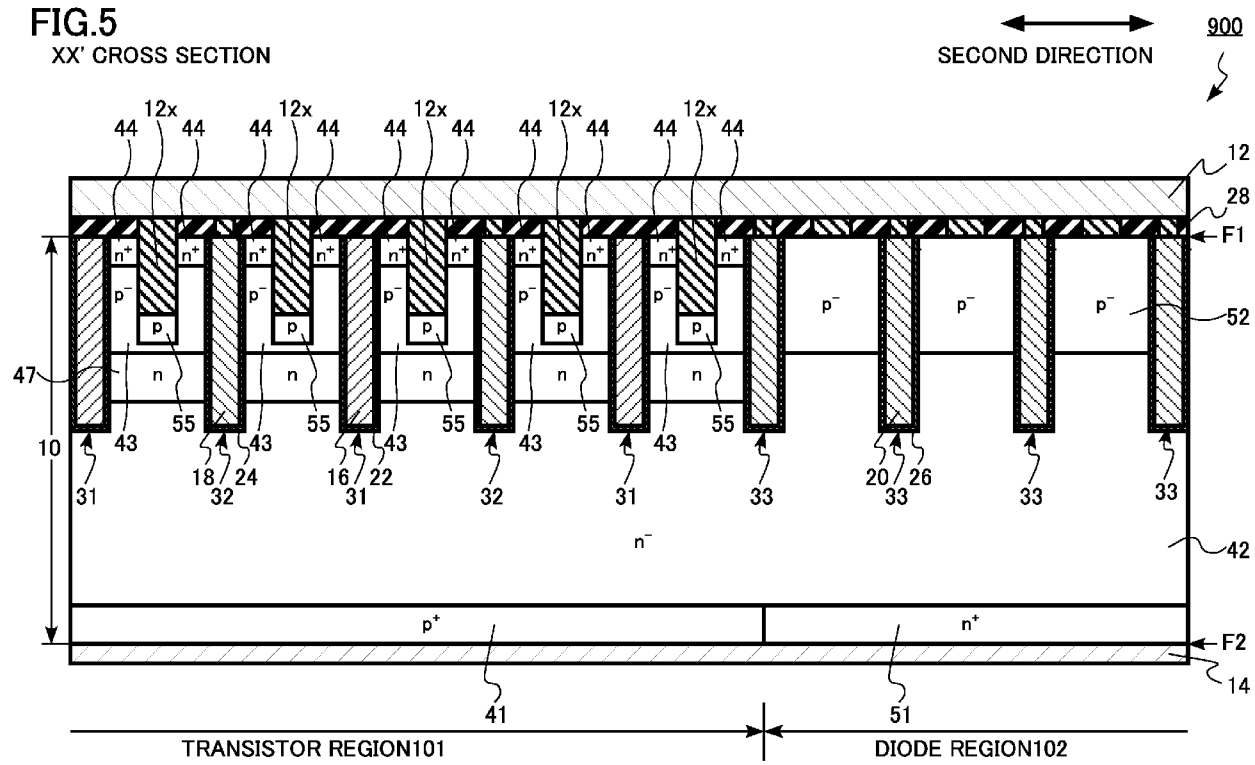


FIG.6

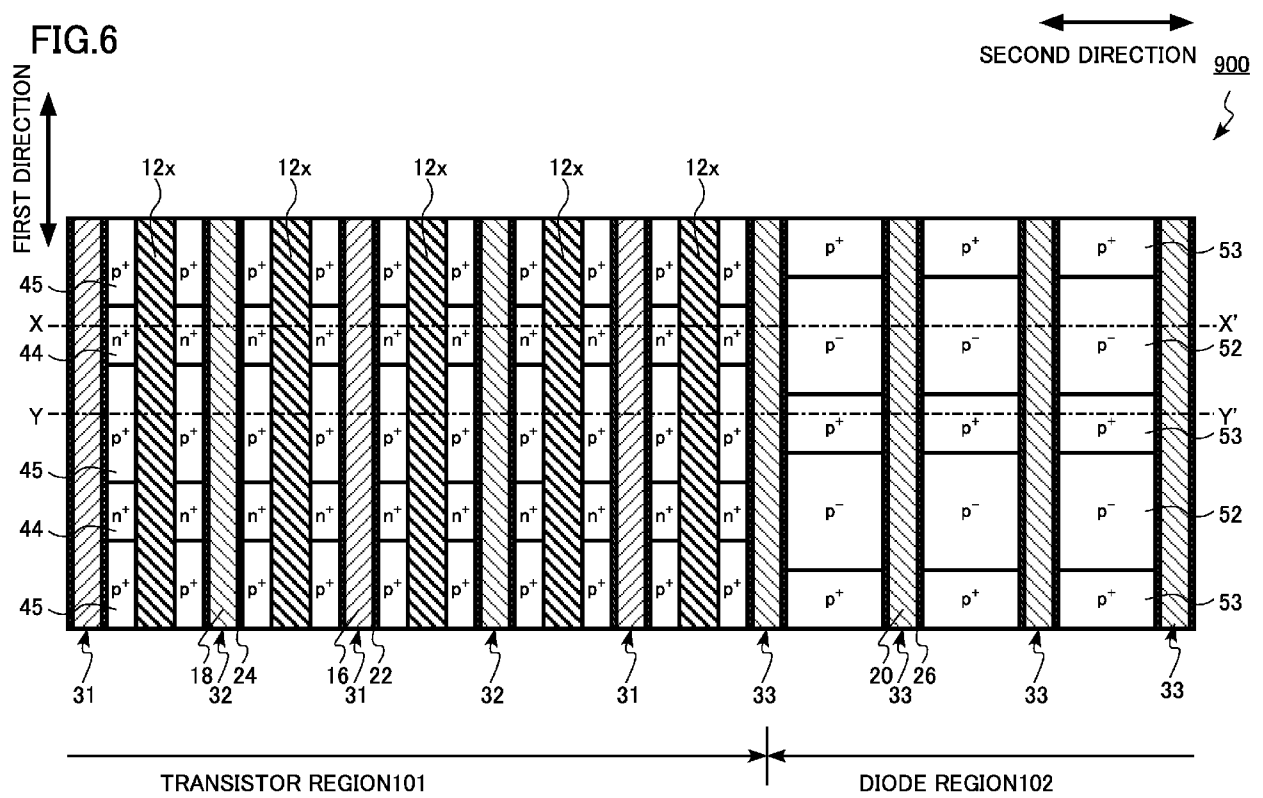


FIG.7
YY' CROSS SECTION

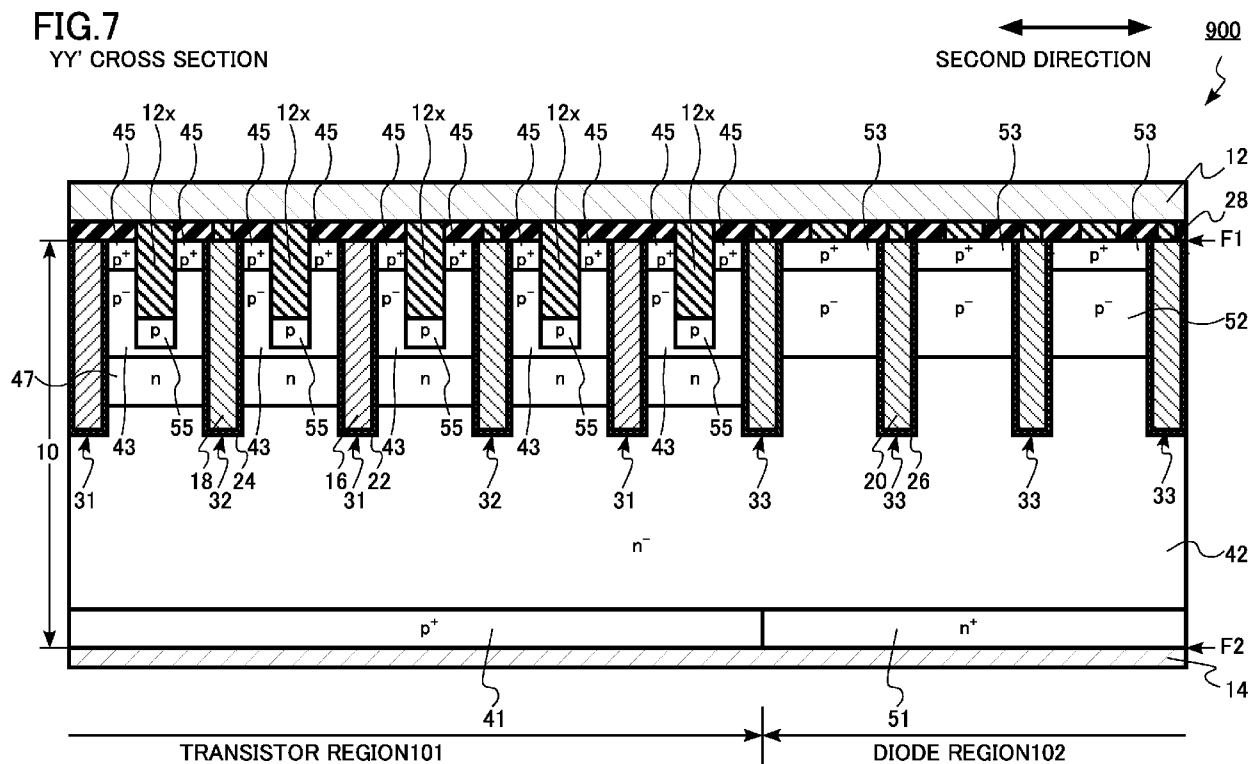


FIG.8
XX' CROSS SECTION

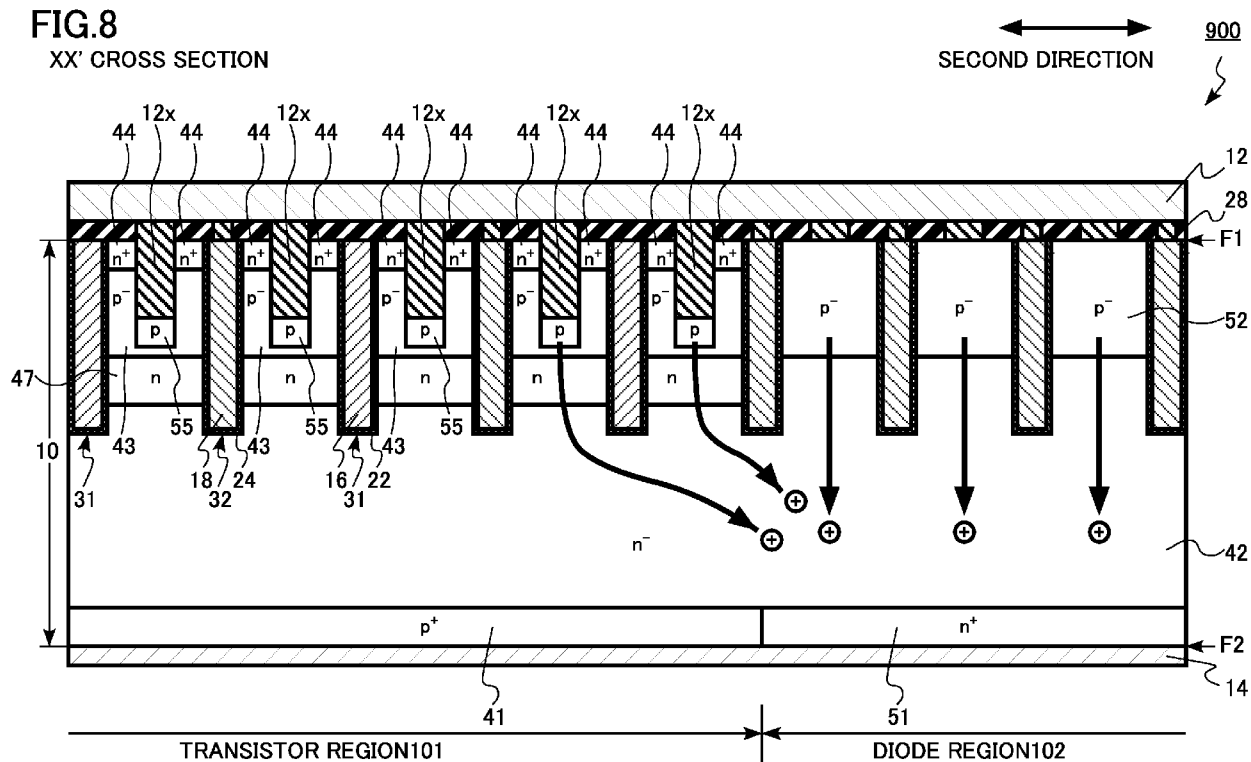


FIG.9
AA' CROSS SECTION

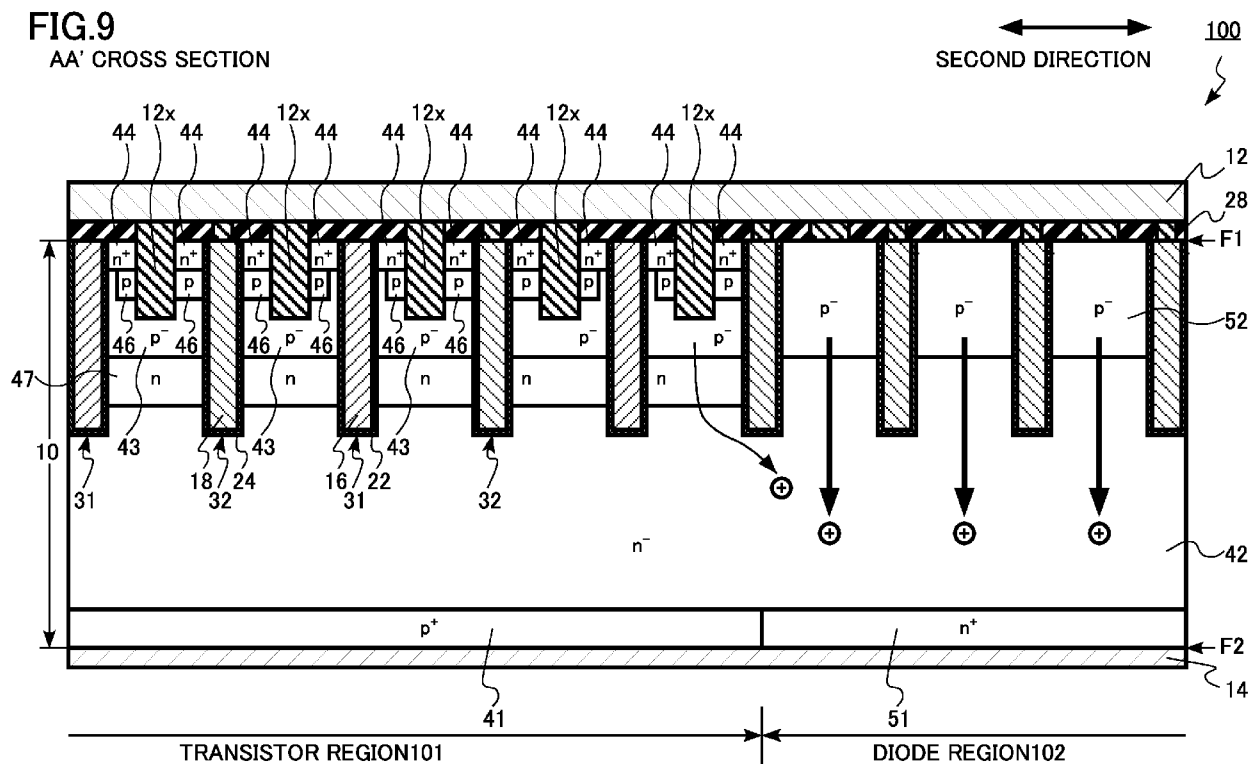


FIG.10

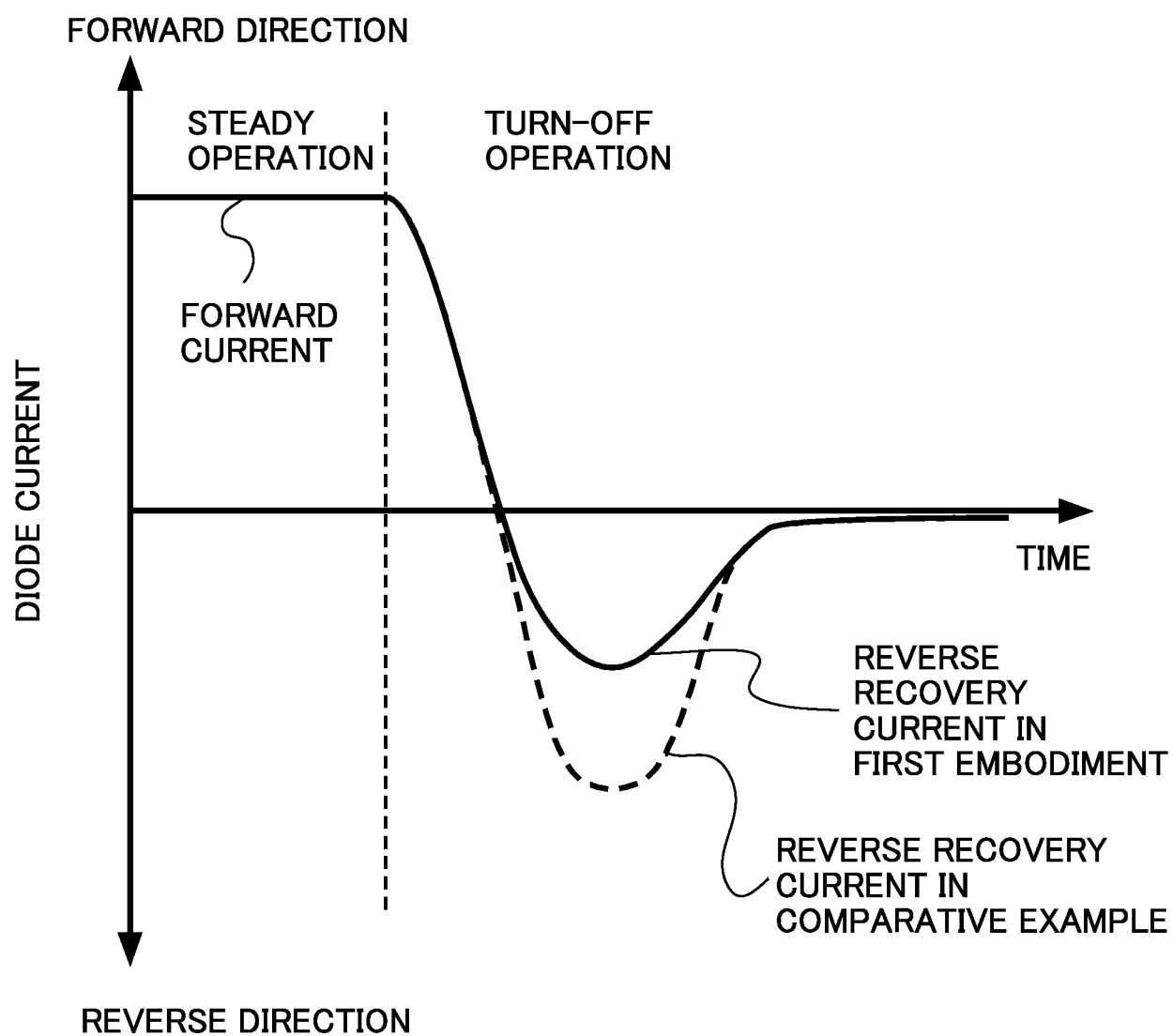
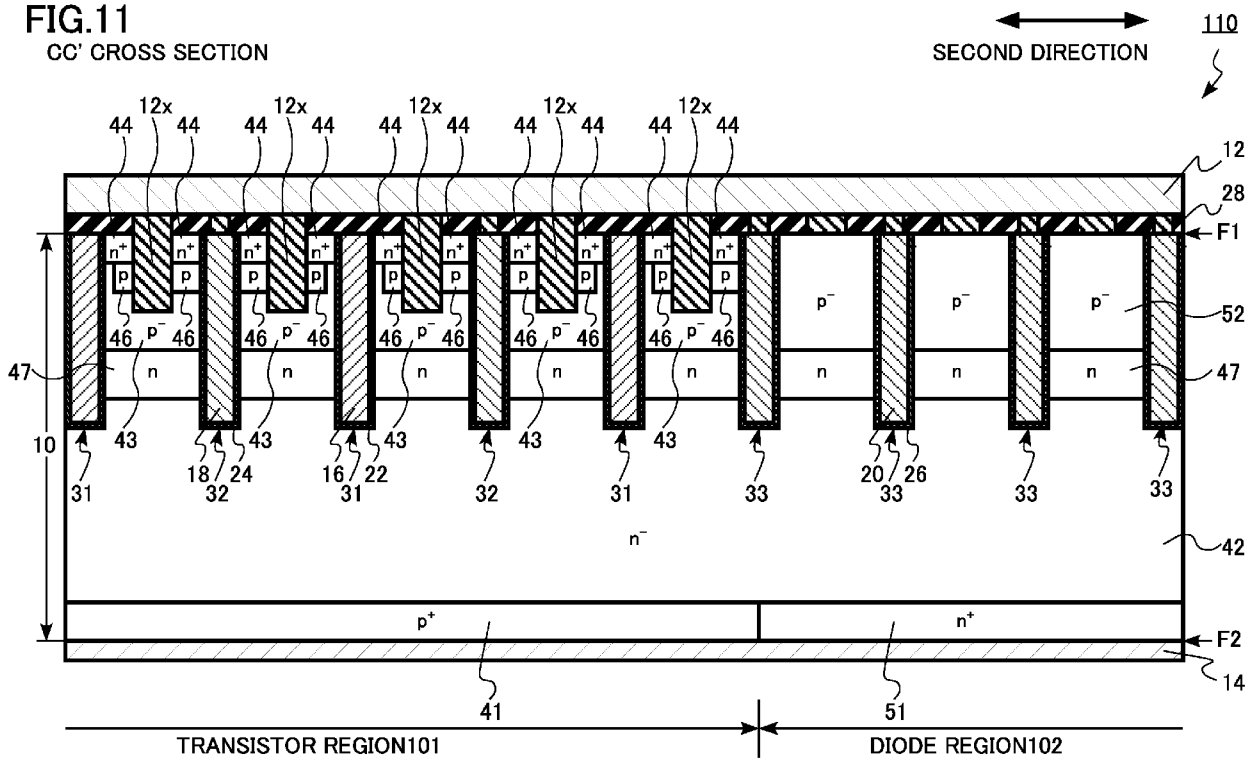


FIG.11
CC' CROSS SECTION



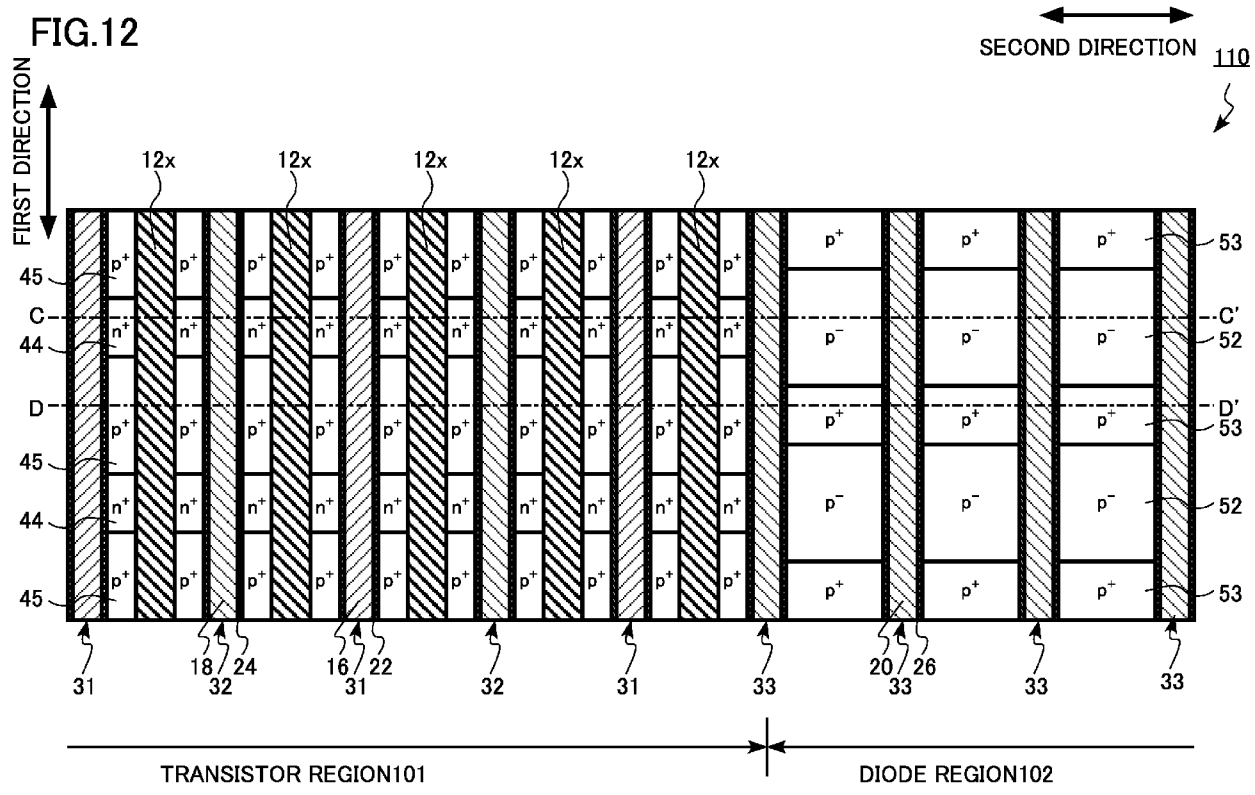


FIG.13
DD' CROSS SECTION

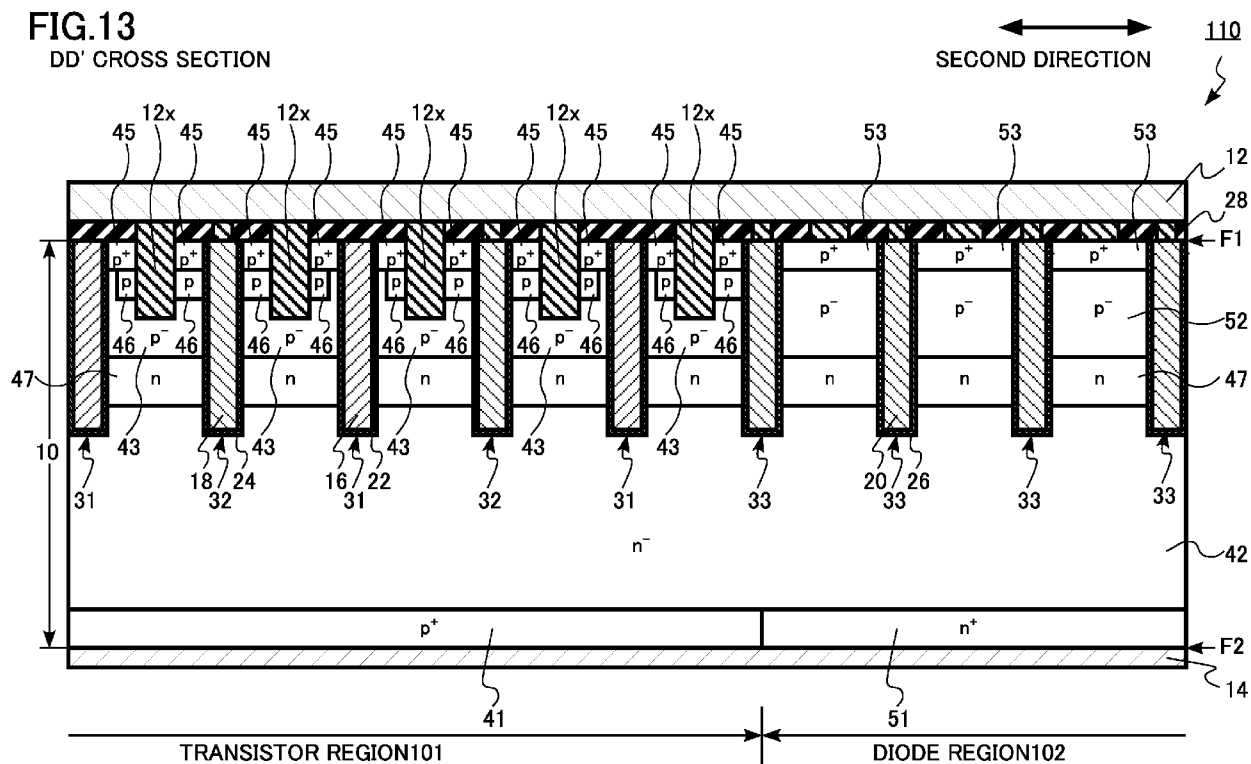
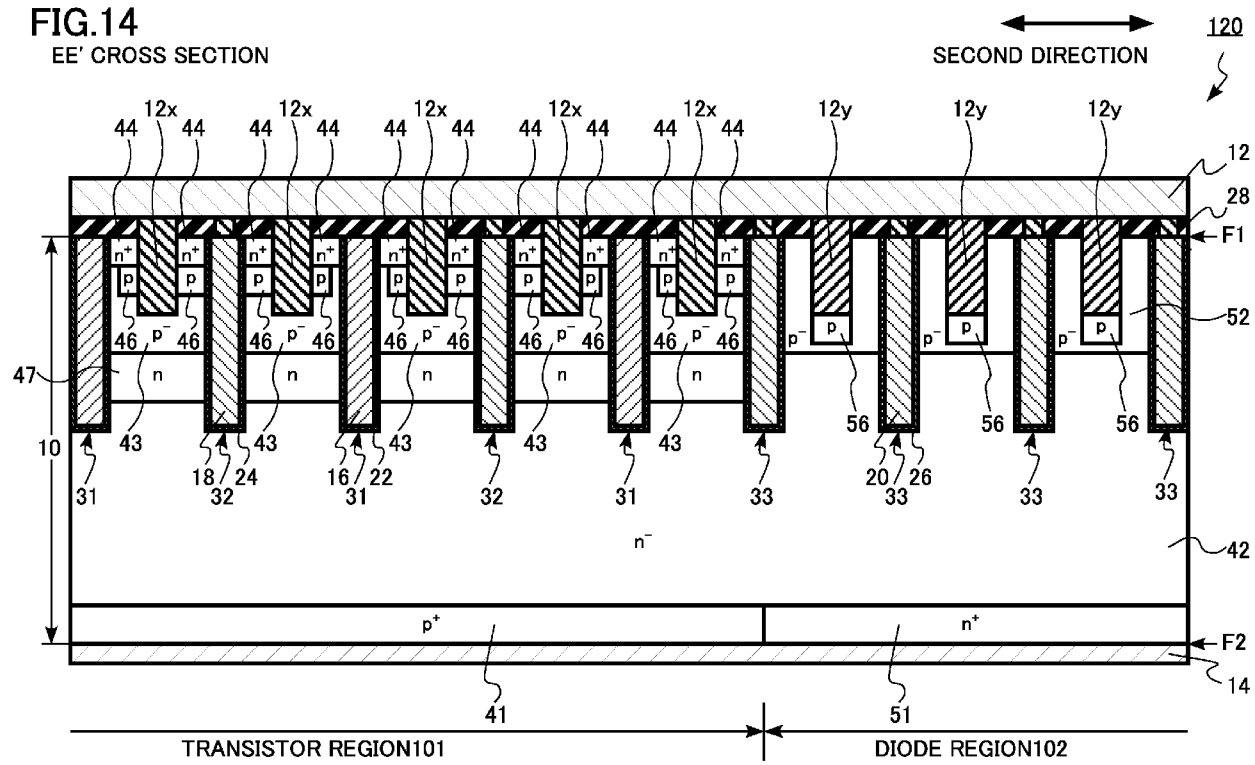


FIG.14
EE' CROSS SECTION



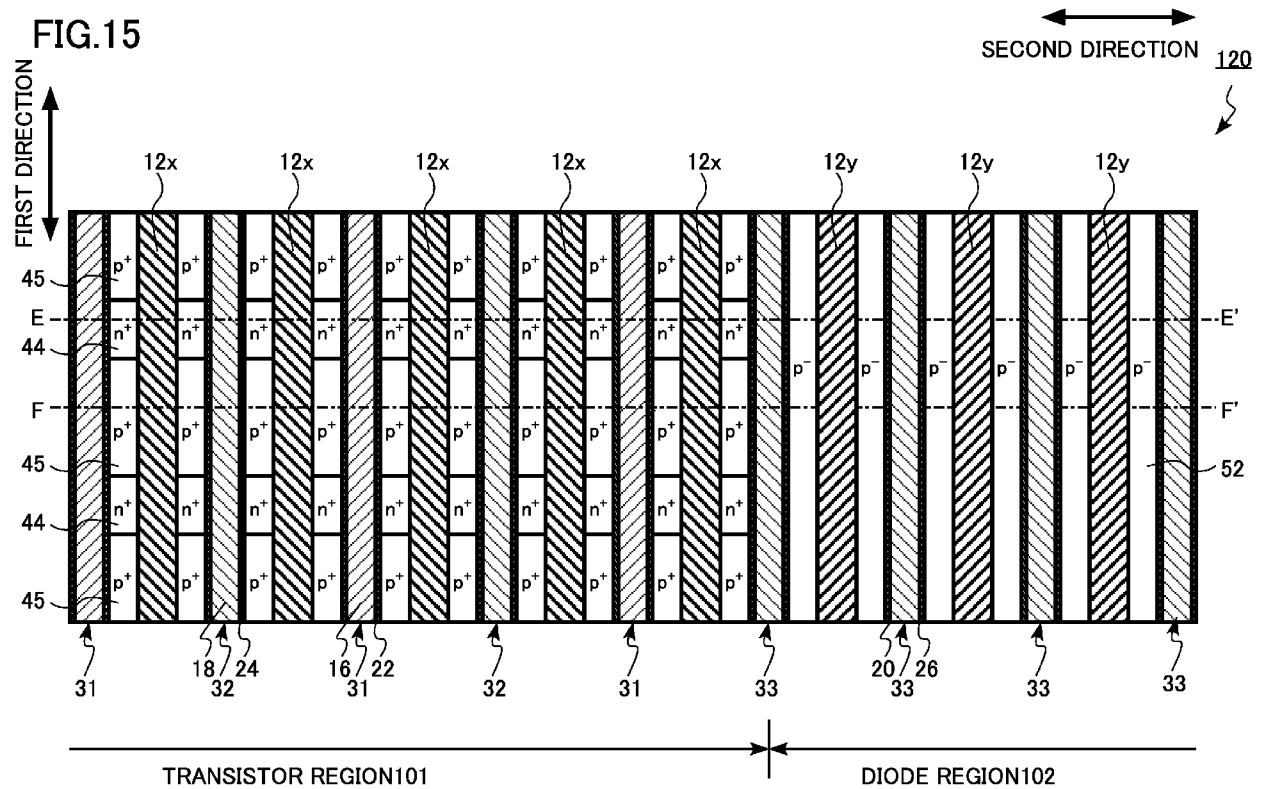


FIG.16
FF' CROSS SECTION

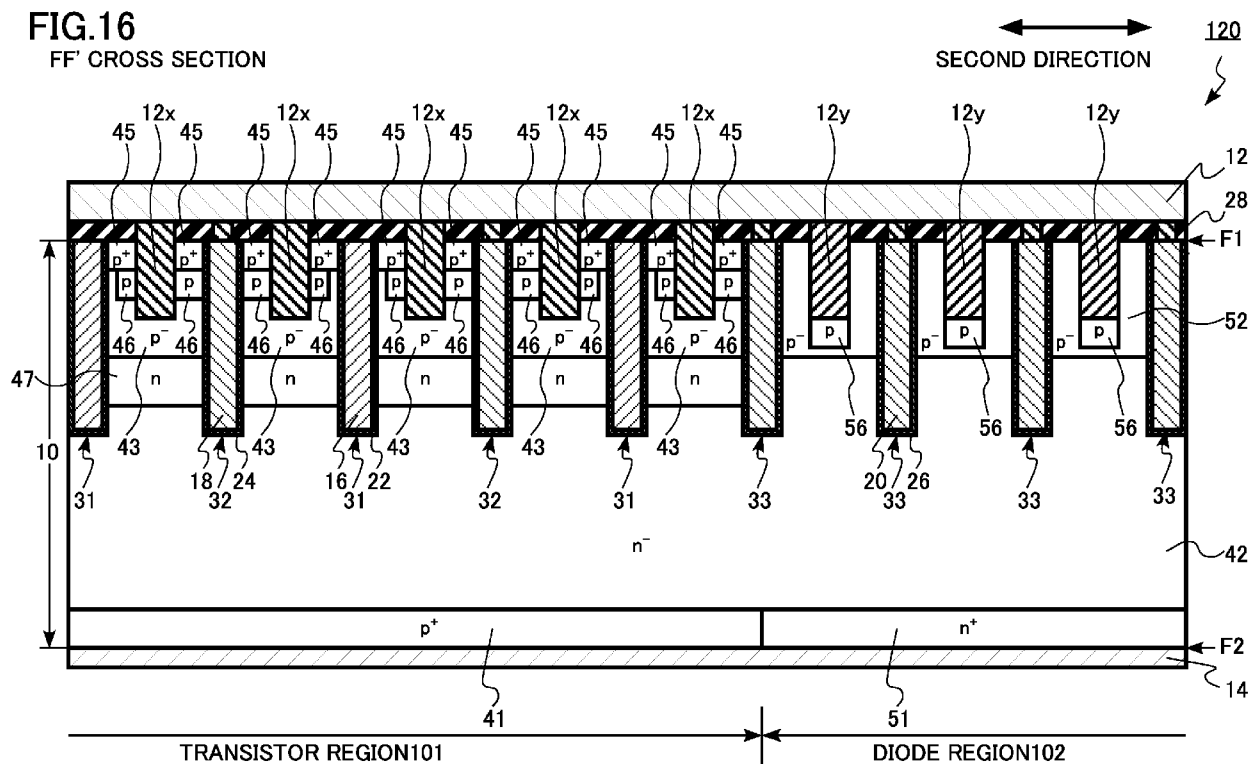
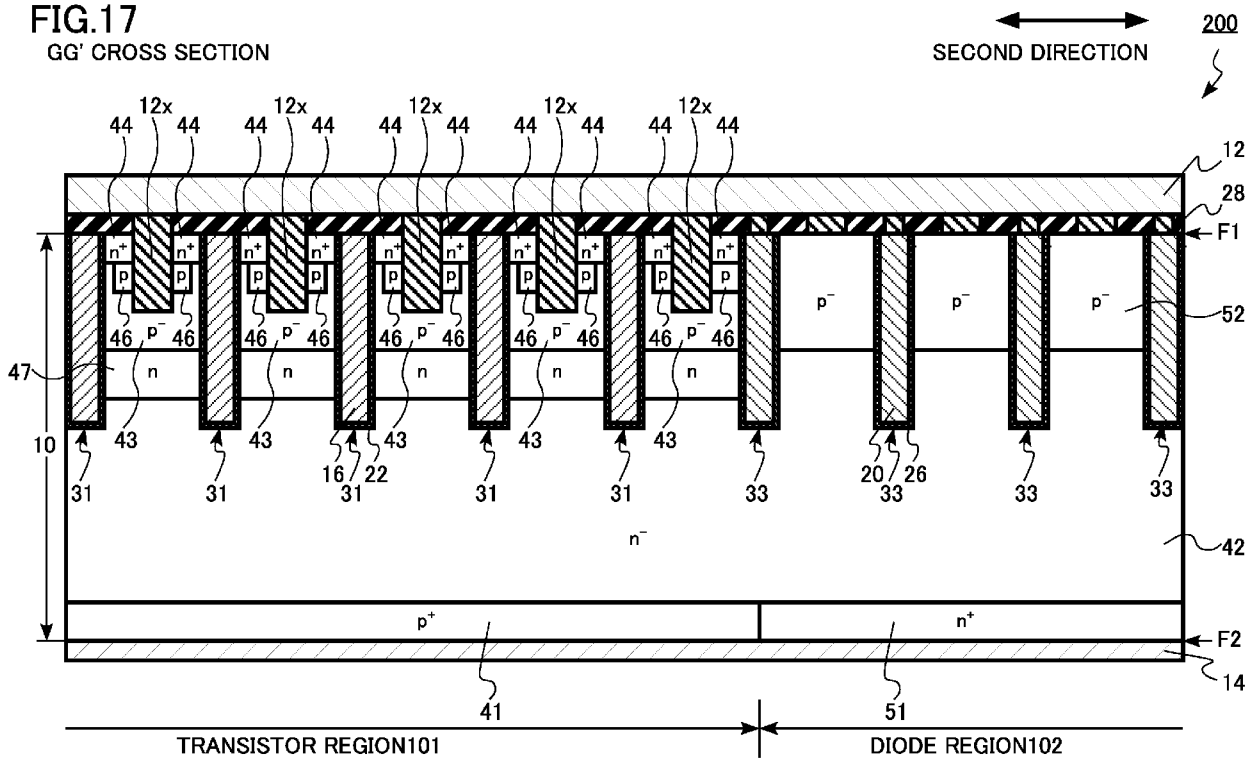


FIG.17
GG' CROSS SECTION



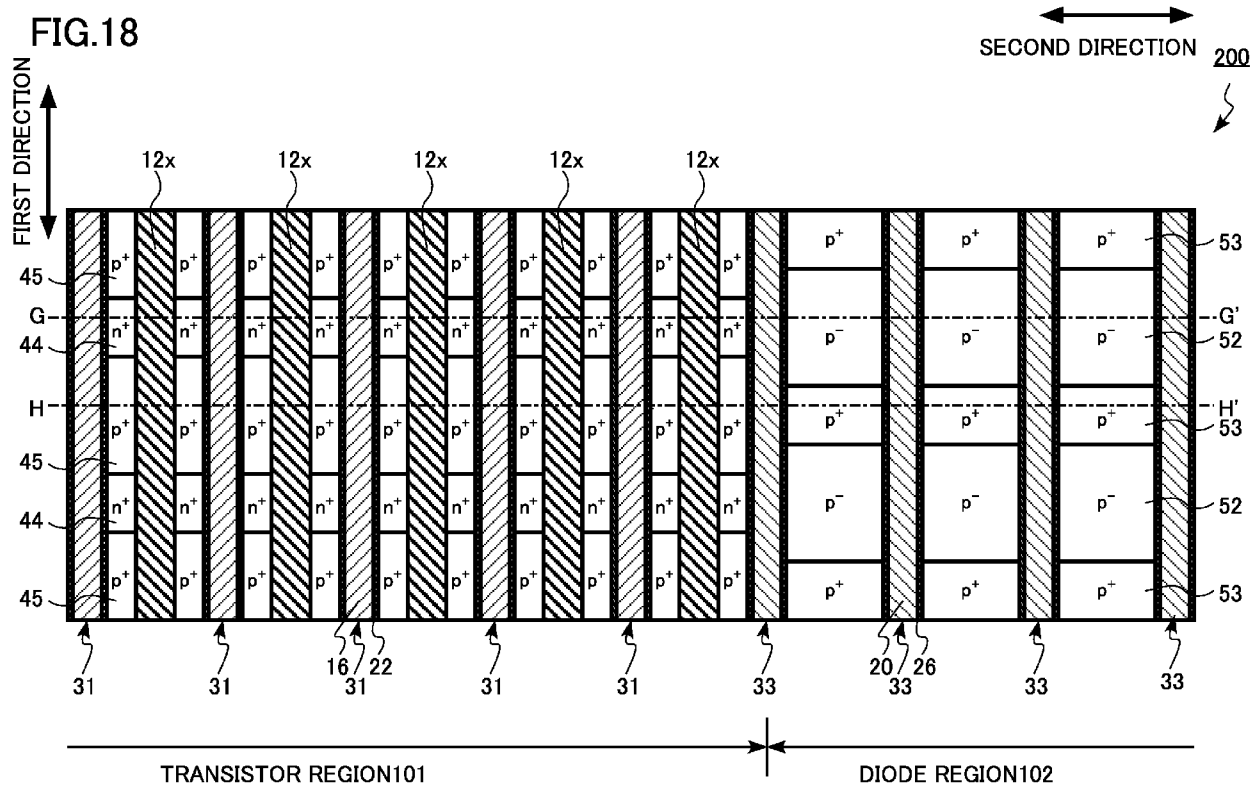
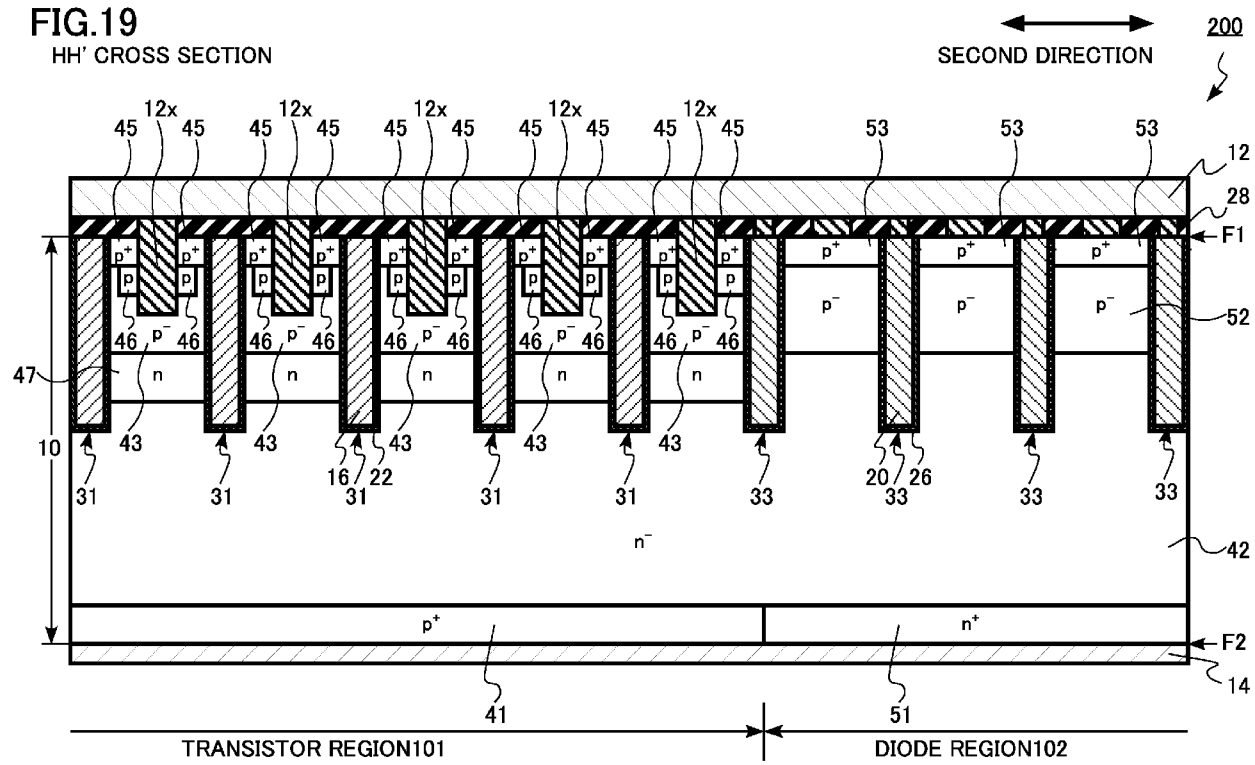


FIG.19
HH' CROSS SECTION





EUROPEAN SEARCH REPORT

Application Number

EP 24 16 0265

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Y	US 2023/207674 A1 (KUBOUCHI MOTOYOSHI [JP] ET AL) 29 June 2023 (2023-06-29) * paragraph [0135] - paragraph [0155] * * figures 3A-3E * -----	1-14	ADD. H01L29/47
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