(12) UK Patent (19) GB (11) 2 197 127 (13) B

(54) Title of Invention

# A method for fabricating a Bicmos device

(51) INT CL[5]; H01L 27/06

(21) Application No
8725477.7

(22) Date of filing
30 Oct 1987

(30) Priority data

(31) 869286

(32) 4 Nov 1986

(33) KR

(43) Application published
11 May 1988

(45) Patent published
4 Jul 1990

(73) Proprietor(s)
Samsung Electronics
Co Ltd

(Incorporated in Rep Korea)

416 Maetan-Dong
Suwon-City
Kyungki-do
Republic of Korea

(72) Inventor(s)
Suk-Gi Choi
Sung-ki Min
Chang-Won Kahng

(74) Agent and/or
Address for Service
Langner Perry
52/54 High Holborn
London WC1V 6RR

(52) Domestic classification
(Edition K)
H1K KGAK K1AA9 K1CA
K11B3 K11D K4C11 K4C14
K9B1 K9B1A K9C1 K9D1
K9N2 K9R2

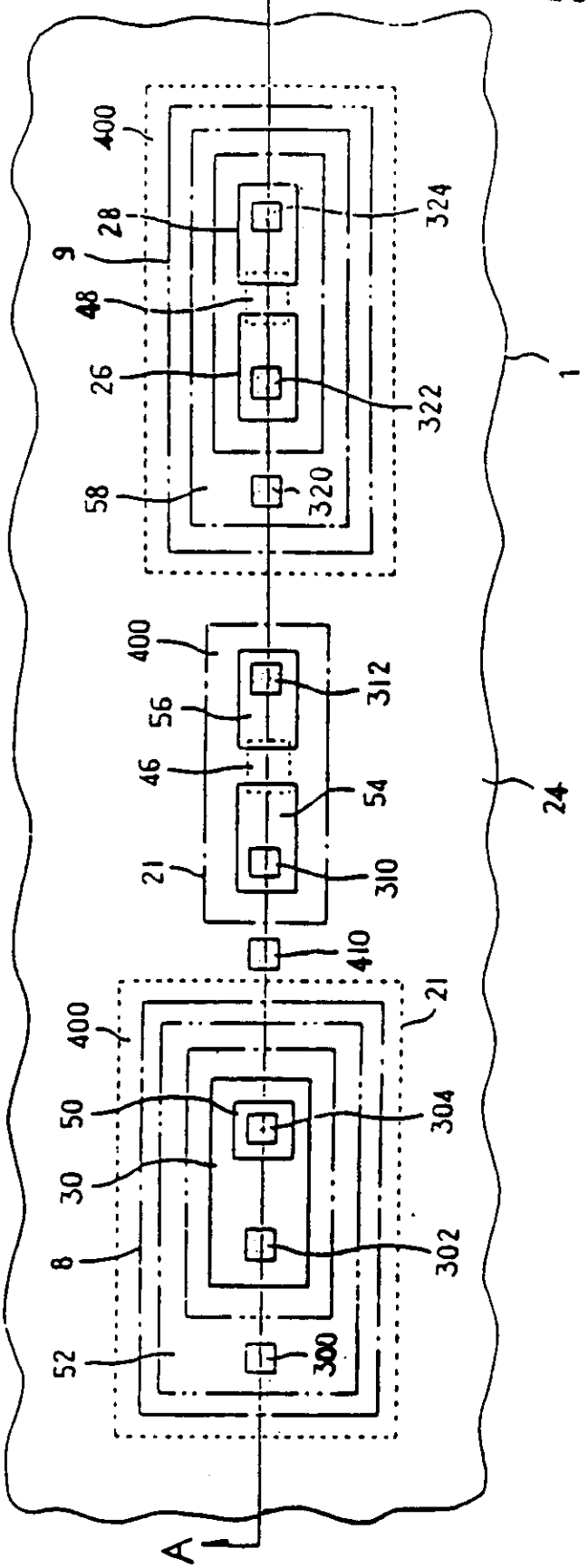
(56) Documents cited
US 4326189 A
US 4046250 A
US 3920484 A

(58) Field of search

As for published application
2197127 A *viz:*
UK CL H1K
INT CL[4]
H01L
updated as appropriate

2197127

Fig 1



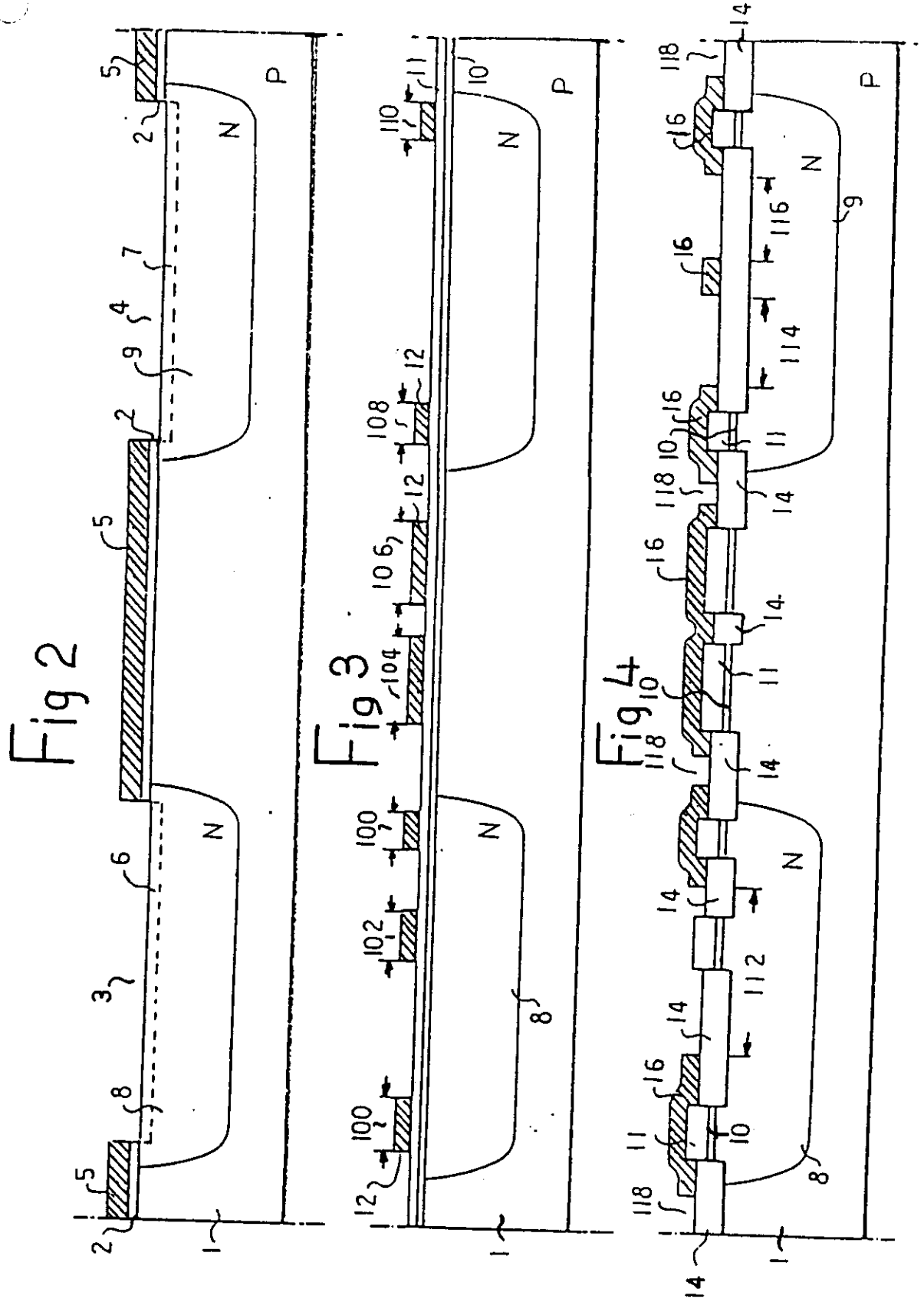


Fig 2
Fig 3
Fig 4
P
N
1
2
3
4
5
6
7
8
9
10
11
12
14
16
100
102
104
106
108
110
112
114
116
118

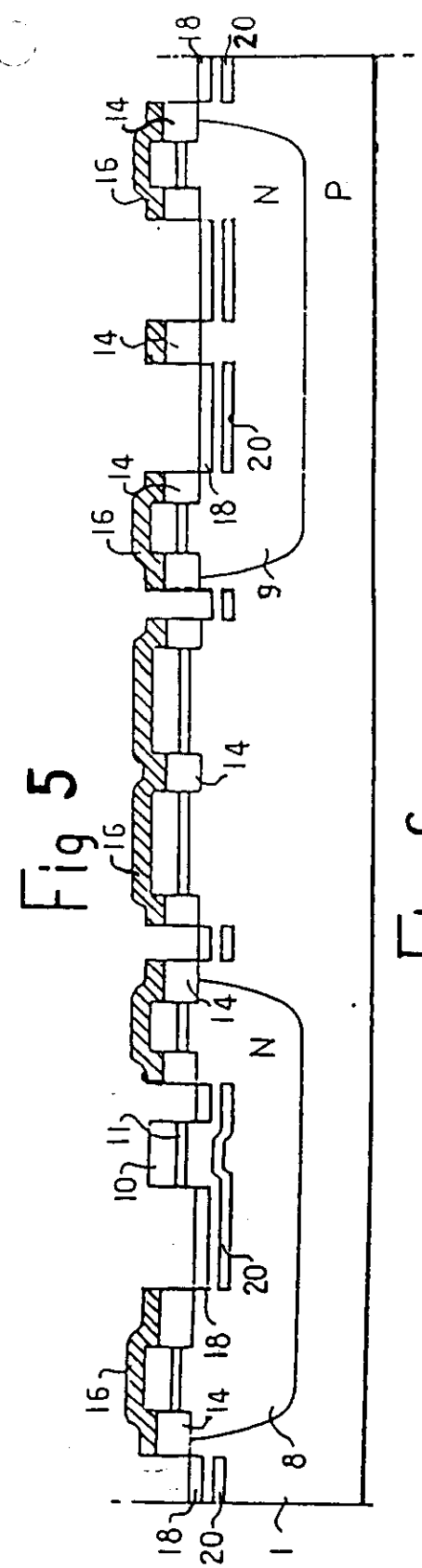



Fig 5

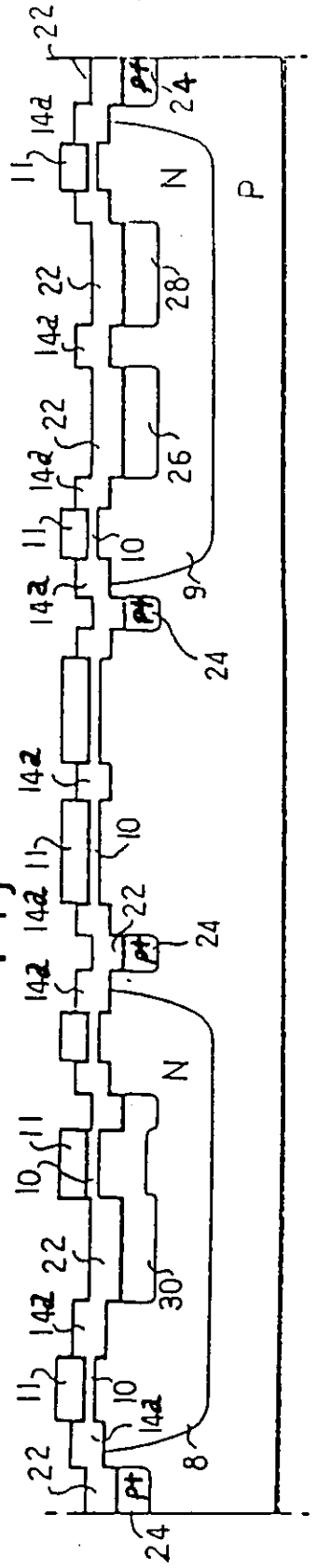



Fig 6

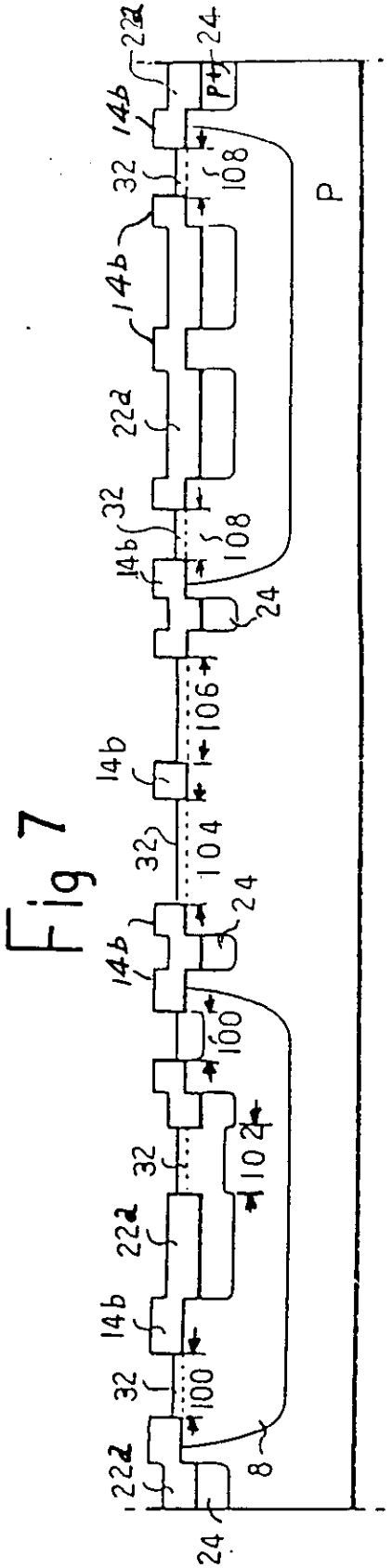



Fig 7

Fig8

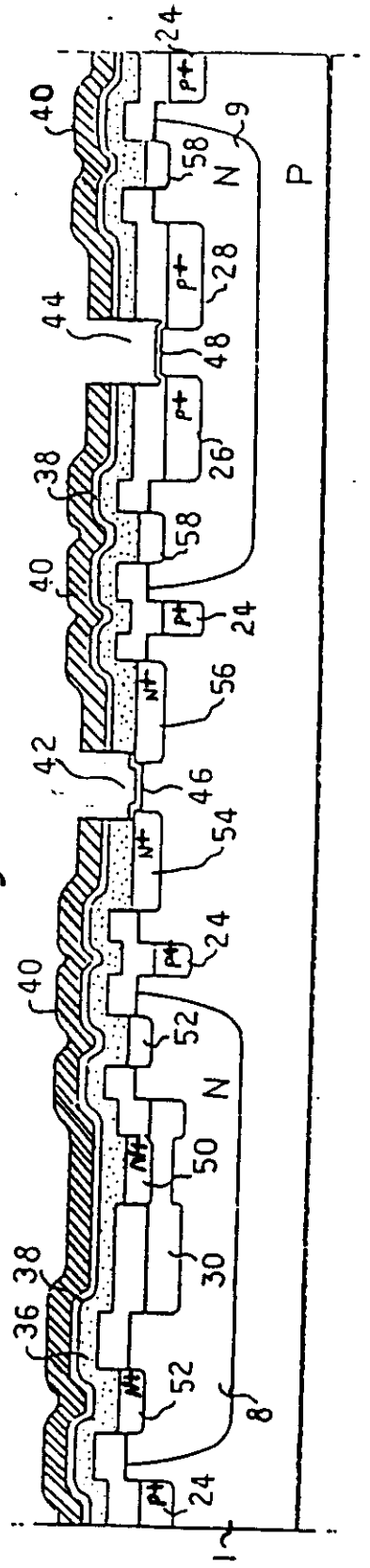

24
40
58
9
N
P
28
44
48
38
26
58
40
24
56
42
46
54
24
40
52
N
50
30
36 38
52
8
24
1

Fig9

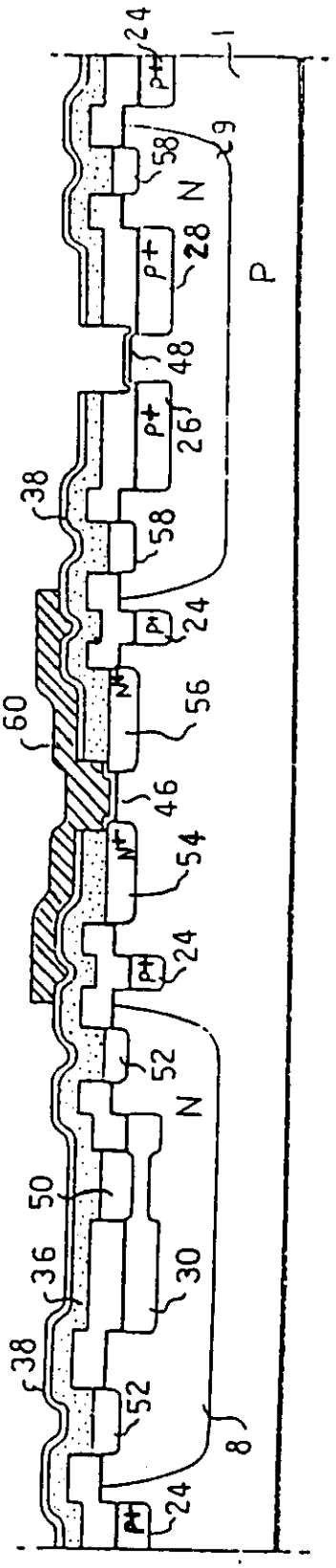

24
1
58
9
N
28
P
48
26
38
58
24
56
60
46
54
24
52
N
50
36
30
38
52
8
24

Fig 10

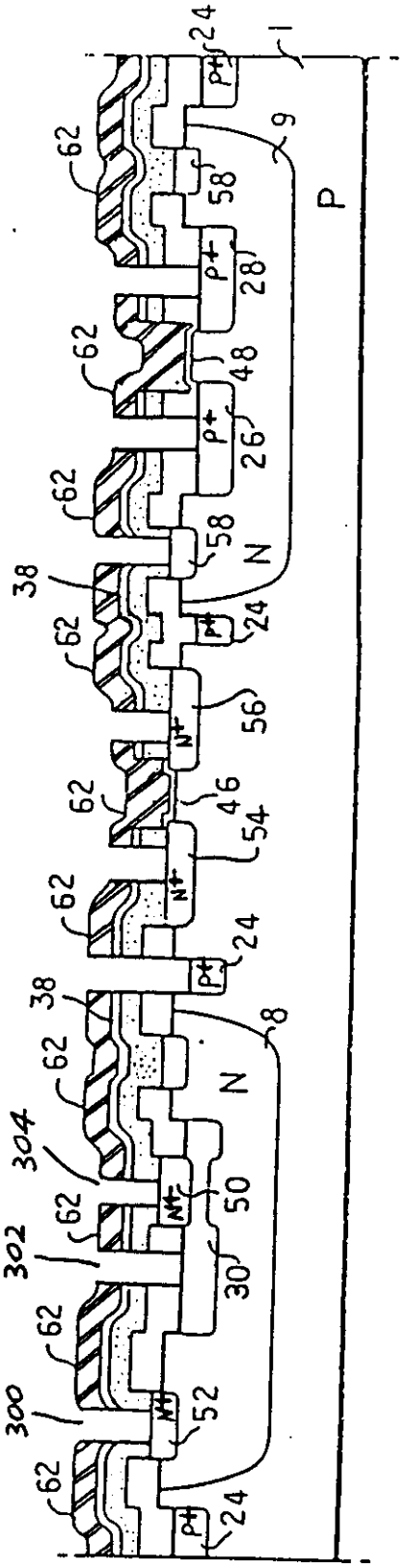
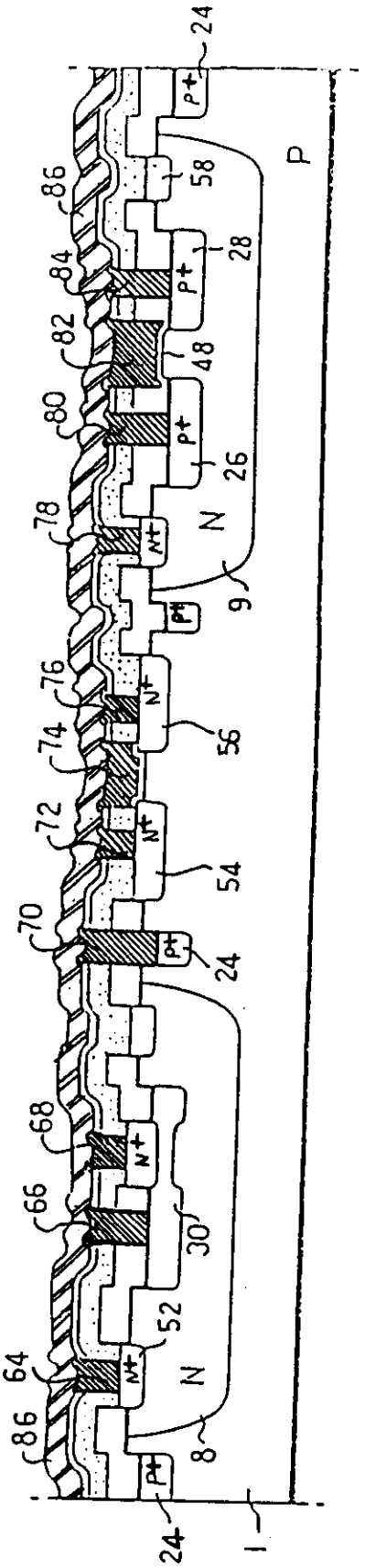

24
1
62
9
58
P
28
48
26
N
38
56
46
54
8
304
50
302
30
300
52

Fig 11


24
86
58
P
84
28
82
48
80
26
78
N
9
76
56
74
72
54
70
24
68
66
30
64
52
N
86
8
24
1

2197127

# A METHOD FOR FABRICATING A BiCMOS DEVICE

This invention relates to a method for fabricating a semiconductor device with bipolar transistors and N and P channel MOS field effect transistors on the same Si substrate.

A semiconductor device which has bipolar transistors and CMOS transistors is generally called as a BiCMOS device.

A method for frabricating a BiCMOS device on a Si substrate of a first conductivity, is disclosed in, e.g. U.S. Patent No. 4,503,603. This method is based on the fabricating steps that use a part of the first dielectric layer as the gate oxide of the FETs, which remains unchanged throughout the whole process and forms a part of the masking layer composed of the first dielectric, $SiO_2$ and the second dielectric nitrides over the substrates after defining the substrate regions (wells) of a second conductivity type (the reverse of the first conductivity) to fabricate bipolar transistors and P channel MOSFETs on the Si substrate of the first conductivity.

Thus this convention process needs the following 8 mask steps;

(1) the first mask step defines the substrate region (well region) of the second conductivity on the substrate of the first conductivity;

(2) the second mask step makes the above masking layer over the whole substrate after the first mask and leaves the masking layers of the emitter region and collector contact region of bipolar transistor and the gate region of P channel MOSFET and the part of source and drain adjacent to the gate and the contact region to provide the back bias to the substrate of the PMOS FET and the NMOS FET region; (3) the third mask step masks against the ion implantation to form the base region of the bipolar transistor and the source and drain of the PMOS FET, and the contact region of the substrate in the first conductivity; (4) the fourth mask step masks against the ion implantation to form the collector region and the emitter region of the bipolar transistor and the contact region of the substrate of the PMOS and the source and drain of the NMOS; (5) the fifth mask step provides ion implantation for the source and drain of the NMOS FET adjacent to the gate to form the channel region; (6, 7) the sixth and the seventh mask steps define the electrode and the interconnections; and (8) the eighth mask step interconnects the pads after masking the passivation layer to protect the surface.

Thus, with the traditional method,

(1) there are problems of unstable threshold voltages caused by the non-uniform distribution of impurity after successive etching and oxidation processes because the gate insulator of the CMOSFET is covered by the second nitride layer as a mask against the oxidation processes,

(2) there is the disadvantage that the electrical characteristics of the MOSFETs are controlled by the condition of the bipolar transistor fabrication process,

(3) many mask steps are needed, which, if ion implantation is performed additionally to control the threshold voltage of the PMOS and NMOS transistors, amounts to a total of 10 separate masking steps.

The object of this invention is to provide a method for fabricating BiCMOS device having a stable MOSFET using the good insulator as the gate dielectric of the CMOSFET.

Another object of this invention is to provide a method which enables easy control of the threshold voltages of CMOSFET.

A further object of this invention is to minimize the number of mask steps and to provide economic ways of fabrication of a BiCMOS.

According to this invention there is provided a method for fabricating a BiCMOS device, in which said device has a Si substrate of a first conductivity in which there is formed a first substrate region of a second conductivity for a bipolar transistor, a second substrate region of said second conductivity for a first MOSFET having a source and drain of the first conductivity, and in which a part of said Si substrate is to be formed to provide a second MOSFET which has a source and drain of the second conductivity, including the steps of:-

(a) providing a masking layer formed by a first oxide layer and a nitride layer over the Si substrate of first conductivity;

(b) providing a mask over said masking layer to mask a collector contact region and an emitter region of the bipolar transistor, and the source and drain of the second MOSFET, and the contact region of the first MOSFET;

(c) removing portions of the masking layer which are not masked during the step (b);

(d) removing the mask over the masking layer;

(e) forming a second oxide layer on the first substrate region revealed during the previous steps and on the second substrate region and on the Si substrate;

(f) forming a mask on the second oxide layer to produce a channel stopper region on said Si substrate of the first conductivity and a base of the bipolar transistor and the source and drain of the first MOSFET;

(g) removing the unmasked portion of the second oxide layer;

(h) ion implanting through the region revealed in step (f) to form the base, the source, drain and the channel stopper region;

(i) removing the mask and forming a third oxide layer on the region without said masking layer and simultaneously activating the inplanted impurities;

(j) performing ion implantation on the collector contact and emitter of the bipolar transistor and a contact region of the first MOSFET and the source and drain of the second MOSFET after removing the masking layer therefrom;

(k) depositing an oxide layer over the substrate surface;

(l) forming a mask and removing the oxide layer on the gate region of the first and second MOSFET;

(m) depositing a gate oxide in the exposed gate region after removing the mask of step (l);

(n) providing a thermal treatment for activating the implanted impurities and for increasing the density of the oxide layer deposited during the step (k);

(o) making openings for the contacts of the emitter, base and collector of the bipolar transistor and the contacts of the sources and drains of the first and second MOSFET, and the body contact for the channel stopper;

(p) interconnecting the openings by a conductor; and

(q) forming a passivation layer and making an opening therein to form a pad for wire bonding thereto.

The invention will now be described by way of example with reference to the accompanying drawings in which:-

Figure 1 is a plan view of a BiCMOS fabricated in accordance with the invention; and

Figures 2 to 11 are cross-sectional views of the process steps used in accordance with this invention taken along with line A-A of Figure 1.

Referring to Figure 1, the starting material is a p-type <111> Si substrate 1 of a first conductivity with resistivity 1-20 Ω-cm. It

should be noted that Figure 1 represents a part of NPN transistors and PMOSFETs and NMOSFETs on the Si wafer.

In Figure 1, there is a first N-type substrate region 8 in which NPN transistors are formed, a region 21 in said substrate 1 in which NMOSFETs are formed and a second N-type substrate region 9 in which PMOSFETs are formed. Also there are $P^+$ channel stopping regions 24 outside a surface 400 of the substrates 8 and 9 which are to prevent the formation of channels between the devices, and openings 410 which are the ohmic contacts for channel stopping regions 24. The first substrate region 8 is the collector area of NPN transistors, in which the collector contact region 52 and the base region 30 and the emitter region 50 are formed. The collector contact region 52 of proper depth covers around the base regions 30 at a certain distance on the surface within the substrate 8. The $N^+$ emitter regions 50 are defined in the base region 30. The openings 300, 302, 304 are those for contact regions of collector, base and emitter. A gate insulator 46 in the region 21 in which the NMOSFET is fabricated is formed on the upper surface between a source region 54 and the drain region 56 and the openings 310, 312 are the contact openings for the source 54 and drain 56. An $N^+$ contact area in the second substrate region 9 for PMOSFET, which is to apply the bias for the second substrate region 9, covers separately around the $P^+$ source 26 and $P^+$ drain 28. Over these separated regions, between the source 26 and drain 28, a gate insulator 48 is formed. Opening 320 is for contact to area 58 and openings 322, 324 define contact regions for the source 26 and drain 28.

Figures 2 to 11 are cross-sectional views of the process steps in accordance with the invention taken along with line A-A shown in the Figure 1 and the process steps of constructing a BiCMOS will now be explained.

After forming a $SiO_2$ layer 2 by the conventional oxidation method over the surface of the Si substrate 1 as is shown in Figure 2, a photoresist 5 is coated thereon and the openings 3, 4 for the NPN transistor and the substrate regions of the PMOSFET are made by conventional photolithography techniques and the N type implanted regions 6, 7 are made after high energy ion implantation of phosphorous with dose of $10^{12}$ - $10^{14}$ ions/$cm^2$.

After removing the photoresist 5 used for the mask against ion implantation, N type implanted regions are activated at about 1200°C in

nitrogen gas ambient and form the first N substrate region 8 and the second N substrate region 9 with a diffusion depth of about 2.5μm. A thin oxide layer 10 is formed on the substrate 1 as shown in Figure 3 after removing the oxide layer 2 from the substrate 1. A thin $Si_3N_4$ layer 11 is formed by conventional LPCVD (Low Pressure Chemical Vapor Deposition) over the oxide layer 10. The masking layer composed of the oxide layer 10 and the nitride layer 11 prevents the substrate 1 under said masking layer from oxidising during the following oxidation processes. A second photoresist mask 12 on the nitride layer 11 is made over the masking layer 10, 11. The mask 12 covers the collector region 100 and the emitter region 102 in the first substrate region 8 which is to form the NPN transistor, the source and drain 104, 106 which are to form NMOSFET and a contact region 108, 110 of the second substrate region 9 which is to form PMOSFET.

After etching the unmasked nitride layer 11 using the second mask 12 as an etch mask and removing the second mask 12, the second oxide layer 14 is formed as in Figure 4 for the third photolithography. In this oxidation process, the oxide is not grown on the Si substrate under the masking layer 10, 11 but it is grown on the region unmasked by the masking layer 10, 11.

After the growth of the oxide layer 14, the regions except those to form the base 112 of NPN transistor, the source and drain 114, 116 of PMOSFET and region 118 that is to form the channel stopper, are covered by a third photoresist mask 16 as shown in Figure 4.

A portion of the substrate region 1 and the first and second substrate regions 8, 9 are revealed after etching the second oxide layer 14 with the third oxide etch mask 16.

After this, boron implantation is performed using the third mask 16 and oxide layer 14 and the masking layers 10, 11 to mask against the ion implantation. This boron implantation is performed twice with differing energy levels. The first implantation is performed with high dose at energy less than 100 KeV and the second is performed with dose $2 \times 10^{12} - 5 \times 10^{13}$ ions/cm$^2$ at an energy level high enough to penetrate the oxide 10 and the nitride 11 into the substrate and to make the junction depth about 0.5μm. The above process sequence can be reversed. The implantation with relatively low energy cannot penetrate the masking layer 10, 11 on the emitter region 102 of the NPN transistor which is

unmasked by the third mask and the implantation with high energy penetrates it and the energy can be varied so that the boron concentration of the base region under the emitter region can be controlled. Then as shown in Figure 5, $P^+$ region 18 implanted with low energy and high concentration and P region 20 implanted with high energy and low concentration are formed.

After the third mask 16 is etched out by plasma etching, an oxidizing process, such as the conventional method using masks 10, 11 as the oxide mask as shown in Figure 6, forms a third oxide layer 22 on silicon surfaces exposed by the above etching process and the second oxide layer 14 in Figure 5 is formed by an oxide layer 14a of the prescribed thickness. During this process, $P^+$ region 18 of high concentration and P region 20 of low concentration which are boron-implanted regions as in Figure 5 are also activated so that channel formation between devices is prohibited as shown in Figure 6, and $P^+$ channel stop region surrounding the NPN transistor, N channel and P channel FET devices are also formed, and source and drain regions 26, 28 of P channel FET are also formed in said second substrate layer 9, and also the activated base region 30 is formed in the first substrate region 8. The base region 30 outside the emitter region 102 is deeper in depth and has higher concentration than that of the base region under the emitter 102 so that it is easy to reduce the base resistance and to improve the electical characteristics of the NPN transistor.

After removing the nitride layer 11 by the conventional method of etching the nitride without any mask, the thin oxide layer 10 is etched by HF solution without any mask so as to reveal the surface of the substrate 1 and the first and second substrate region 8, 9 under the masking layer 10, 11 in Figure 5 (Figure 7). Then the second oxide layer 14a and the third oxide layer 22 of Figure 6 become the new oxide layers 14b, 22a etched by the thicknesses of the first oxide layer.

After that, as shown in Figure 7, an As implantation with dose $10^{15}$ - $10^{16}$ ions/$cm^2$ is performed by using the above new oxide layers 14b, 22a as a mask. The As implanted layer with junction depth about 0.3$\mu$m in the collector region 100 and the emitter region 102 of the NPN transistor and the source and drain regions 104, 106 of NMOSFET and the contact area 108 of PMOSFET in the second substrate region are formed so that the high emitter efficiency and the low ohmic resistance can be obtained.

An oxide layer 36 in Figure 8 is deposited by the conventional CVD technique over the surface of the substrate 1 and a nitride 38 is deposited over the oxide 36 by LPCVD and a fourth photoresist coating 40 is provided, openings 42, 44 being made by the conventional photolithography and etching of the oxide and the nitride to form the gate insulators of NMOSFET and PMOSFET.

After this, the fourth photoresist mask 40 is removed in plasma and the gate oxide of about 400Å thickness is formed by pyrogenic oxidation at about 850°C in $H_2$ and $O_2$ ambient to keep the shallow junction depth of the emitter and base of NPN transistor. In this process, if the base and emitter junctions are deep, the gate oxide layers 46, 48 can be formed by the conventional dry oxidation process.

Here, the purpose of covering the oxide 36 with the nitride 38 is to prevent the growth of oxide by protection of the oxide 36 and the emitter 50 of NPN transistor during the oxidation process for the gate insulator of NMOSFET and PMOSFET, and it will be understood that it is useful for making the high frequency transistor whose emitter depth is extremely shallow. It should be noted that, if the emitter junction is relatively deep, it is possible for the fourth photoresist mask 40 to be formed over the oxide layer 36 without the nitride layer 38, and the openings 42, 44 for the gate insulator of NMOSFET and PMOSFET to be formed.

Moreover, the activation of the As implanted region 32 in Figure 7 is performed by the above processing steps for the gate oxides 46, 48. Thus, as shown in Figure 8, the $N^+$ collector contact 52 and $N^+$ emitter 50 of NPN transistor formed in said first substrate region 8 and the contacts 58 for feeding back bias to the PMOSFET and the source and drain 54, 56 of NMOSFET are formed. The contact areas 58 are formed by opening the oxide outside the source and drain 26, 28 of PMOSFET surrounding the regions 26, 28 and are formed in the second substrate region 9.

After forming the gate oxide layers 46, 48 as stated above, the process steps for controlling the threshold voltages of PMOSFET and NMOSFET can be made, if needed. That is to say, after forming the gate oxide layers 46, 48, boron implantation with energy about 30 KeV and dose about $10^{11}$ ions/$cm^2$ through the openings 42, 44 is performed as in Figure 8, and after removing the fourth photoresist mask 40, a fifth

photoresist mask 60 is formed over the channel region of the NMOSFET, and the boron implantation is performed again and sequentially with energy about 30KeV and dose about $10^{11}$ ions/$cm^2$.

After removing the fifth photoresist mask 60, a thermal treatment is performed to activate the implanted boron and to increase the density of CVD oxide layer 36. This treatment is performed at about 920°C in $N_2$ ambient for about 120 minutes. After this, the threshold voltages of PMOSFET and NMOSFET are -0.75 volt and +0.75 volt respectively. After removing the fifth photoresist mask 60 and coating a sixth photoresist 62 over the surface the contact openings for the collector 52, base 30 emitter 50 of NPN transistor, the source and drain 54, 56 of NMOSFET, the body contact 58 and source and drain 26, 28 of PMOSFET, the channel stopper 24 are formed by photolithography using the sixth photoresist mask 62 as an etching mask.

After the sixth photoresist mask is removed and Al is deposited in vacuum and electrodes formed by the photolithography, sequentially, as in Figure 10, the collector electrode 64 and emitter electrode 68 and base electrode 66 of NPN transistor, the electrode 70 to feed the back bias to the substrate 1, the source electrode 72 and gate electrode 74 and drain electrode 76 of NMOSFET, the electrode 78 to feed the back bias to the second substrate region 9 and the source electrode 80 and gate electrode 82 and drain electrode 84 of PMOSFET are formed. A passivation layer 86 of PSG to protect the above semiconductor system is formed as shown in Figure 11.

As explained above, the method for fabricating a BiCMOS of this invention introduces the advantage of a decrease in the number of process steps, a decrease in the production cost and a stabilization of the threshold voltage by the clean gate oxide. Through the minimization of the number of masks required, only total of 8 masks are necessary which include those additionally required for forming the electrode and revealing pads for bonding after forming the passivation layer and another mask for the process for controlling the threshold voltage.

CLAIMS:

1. A method for fabricating a BiCMOS device, in which said device has a Si substrate of a first conductivity in which there is formed a first substrate region of a second conductivity for a bipolar transistor, a second substrate region of said second conductivity for a first MOSFET having a source and drain of the first conductivity, and in which a part of said Si substrate is to be formed to provide a second MOSFET which has a source and drain of the second conductivity, including the steps of:-

(a) providing a masking layer formed by a first oxide layer and a nitride layer over the Si substrate of first conductivity;

(b) providing a mask over said masking layer to mask a collector contact region and an emitter region of the bipolar transistor, and the source and drain of the second MOSFET, and the contact region of the first MOSFET;

(c) removing portions of the masking layer which are not masked during the step (b);

(d) removing the mask over the masking layer;

(e) forming a second oxide layer on the first substrate region revealed during the previous steps and on the second substrate region and on the Si substrate;

(f) forming a mask on the second oxide layer to produce a channel stopper region on said Si substrate of the first conductivity and a base of the bipolar transistor and the source and drain of the first MOSFET;

(g) removing the unmasked portion of the second oxide layer;

(h) ion implanting through the region revealed in step (f) to form the base, the source, drain and the channel stopper region;

(i) removing the mask and forming a third oxide layer on the region without said masking layer and simultaneously activating the inplanted impurities;

(j) performing ion implantation on the collector contact and emitter of the bipolar transistor and a contact region of the first MOSFET and the source and drain of the second MOSFET after removing the masking layer therefrom;

(k) depositing an oxide layer over the substrate surface;

(l) forming a mask and removing the oxide layer on the gate region of the first and second MOSFET;

(m) depositing a gate oxide in the exposed gate region after removing the mask of step (l);

(n) providing a thermal treatment for activating the implanted impurities and for increasing the density of the oxide layer deposited during the step (k);

(o) making openings for the contacts of the emitter, base and collector of the bipolar transistor and the contacts of the sources and drains of the first and second MOSFET, and the body contact for the channel stopper;

(p) interconnecting the openings by a conductor; and

(q) forming a passivation layer and making an opening therein to form a pad for wire bonding thereto.

2. A method as claimed in claim 1 in which a nitride layer is formed on the oxide layer after the step (k).

3. A method as claimed in claim 1 in which the ion implantation is performed for adjusting the threshold voltages after the step (m).

4. A method as claimed in claim 3 in which said ion implantation process is provided for adjusting the threshold voltage of the NMOSFET and the PMOSFET, and the ion implantation for adjusting the threshold voltage of PMOSFET is thereafter processed.

5. A method of fabricating a BiCMOS device substantially as herein described with reference to and as shown in the accompanying drawings.

REGISTER ENTRY FOR GB2197127

Form 1 Application No GB8725477.7 filing date 30.10.1987

Priority claimed:
04.11.1986 in Republic of Korea - doc: 869286

Title A METHOD FOR FABRICATING A BICMOS DEVICE

Applicant/Proprietor
SAMSUNG SEMICONDUCTOR AND TELECOMMUNICATIONS CO LTD, Incorporated in the Republic of Korea, 259 Gongdan-Dong, Gumi-City, Kyungsangbuk-Do, Republic of Korea [ADP No. 00702456003]

Inventors
SUK-GI CHOI, 2-903 Woosung Apt, 63 Daichi 3-Dong, Kangnam-ku, Seoul, Republic of Korea [ADP No. 00124842001]

SUNG-KI MIN, 157-1 Kanseok-Dong, Nam-Ku, Inchon, Republic of Korea [ADP No. 00124859001]

CHANG-WON KAHNG, 91-209 Sinsoo-Dong, Mapo-Ku, Seoul, Republic of Korea [ADP No. 00124867001]

Classified to
H1K
H01L

Address for Service
LANGNER PARRY, High Holborn House, 52-54 High Holborn, London, WC1V 6RR, United Kingdom [ADP No. 00001032001]

Publication No GB2197127 dated 11.05.1988

Patent Granted with effect from 04.07.1990 (Section 25(1)) with title A METHOD FOR FABRICATING A BICMOS DEVICE

---

17.11.1988 Section 32 Application filed
Entry Type 10.1 Staff ID. BAE1 Auth ID. BACK

29.12.1988 SAMSUNG ELECTRONICS CO.LTD, 416,Maetan-Dong, Suwon-City, Kyungki-do, Republic of Korea [ADP No. 05529870001] registered as Applicant/Proprietor in place of SAMSUNG SEMICONDUCTOR AND TELECOMMUNICATIONS CO LTD, Incorporated in the Republic of Korea, 259 Gongdan-Dong, Gumi-City, Kyungsangbuk-Do, Republic of Korea [ADP No. 00702456003] by virtue of deed of assignment dated 24.10.1988. Certified copy filed on GB2202703
Entry Type 8.4 Staff ID. BAE1 Auth ID. BACK

**** END OF REGISTER ENTRY ****