

[54] **ELECTRONIC FEEDBACK
CONTROLLED TIME-DIVISION
MULTIPLIER AND/OR DIVIDER**
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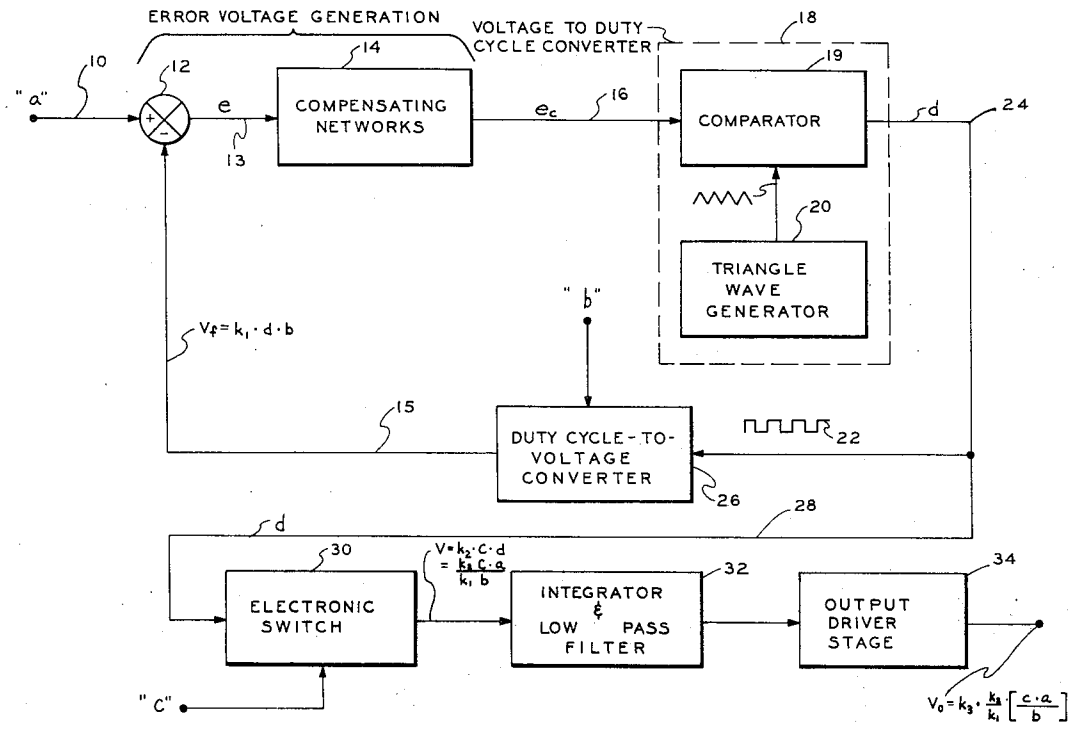
[56] **References Cited**
UNITED STATES PATENTS
3,569,688 3/1971 Brendle.....235/194

2,966,306	12/1960	Isabeau	235/194
3,466,460	9/1969	Connolly	235/194 X
3,492,471	1/1970	Crowell.....	235/194
3,610,910	10/1971	Udall.....	235/194

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[57] **ABSTRACT**
An electronic system for simultaneously multiplying and dividing analog signals which comprises a closed loop circuit in which the division is accomplished by introducing the dividend signal into the main signal translating portion of the circuit and the divisor signal into the feedback portion of the circuit. The output signal of this closed loop circuit has a varying duty cycle which is proportional to the quotient of these signals, and this quotient is multiplied by a third signal in an electronic switch which is connected to the output of the above closed loop circuit.

21 Claims, 2 Drawing Figures



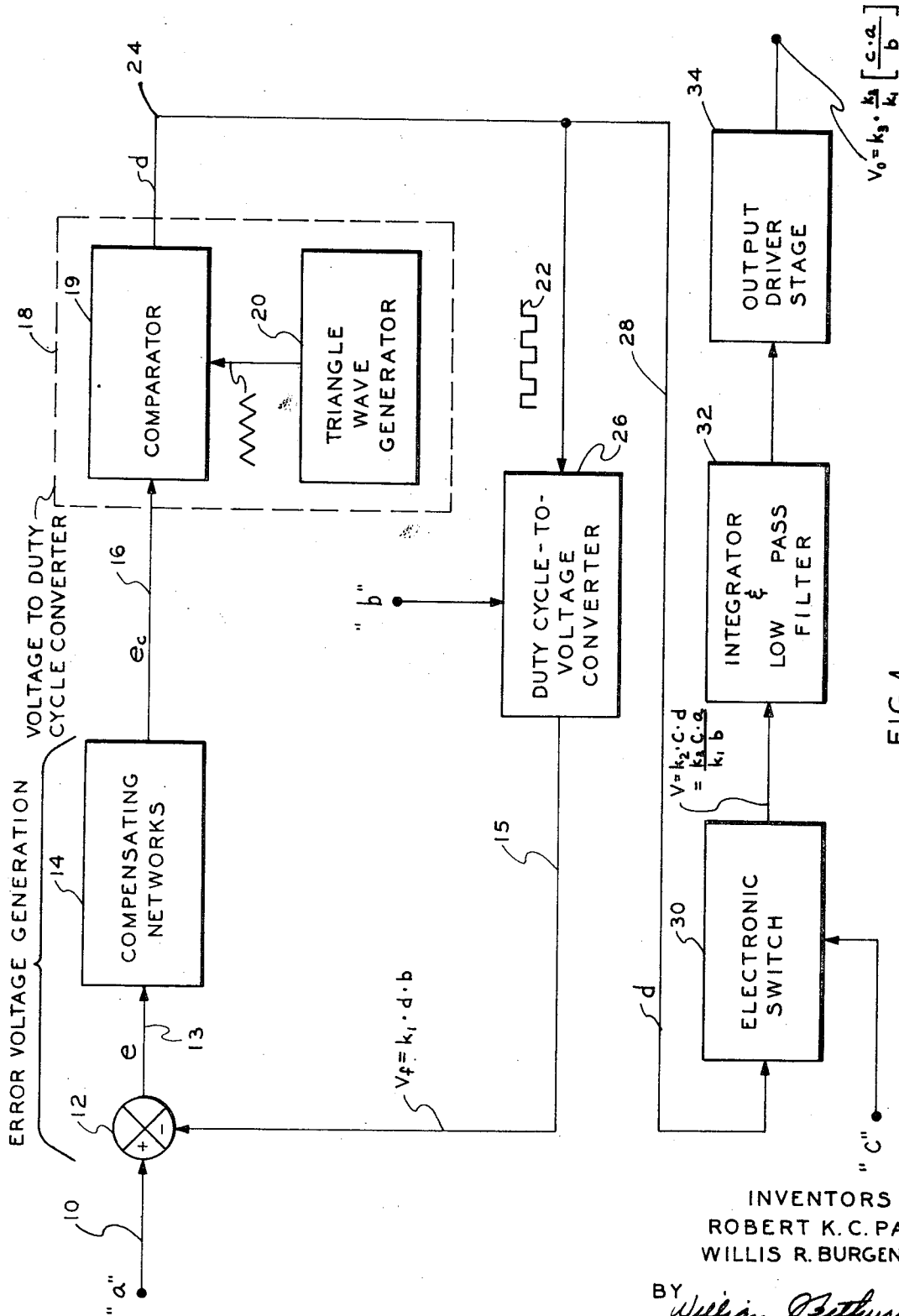
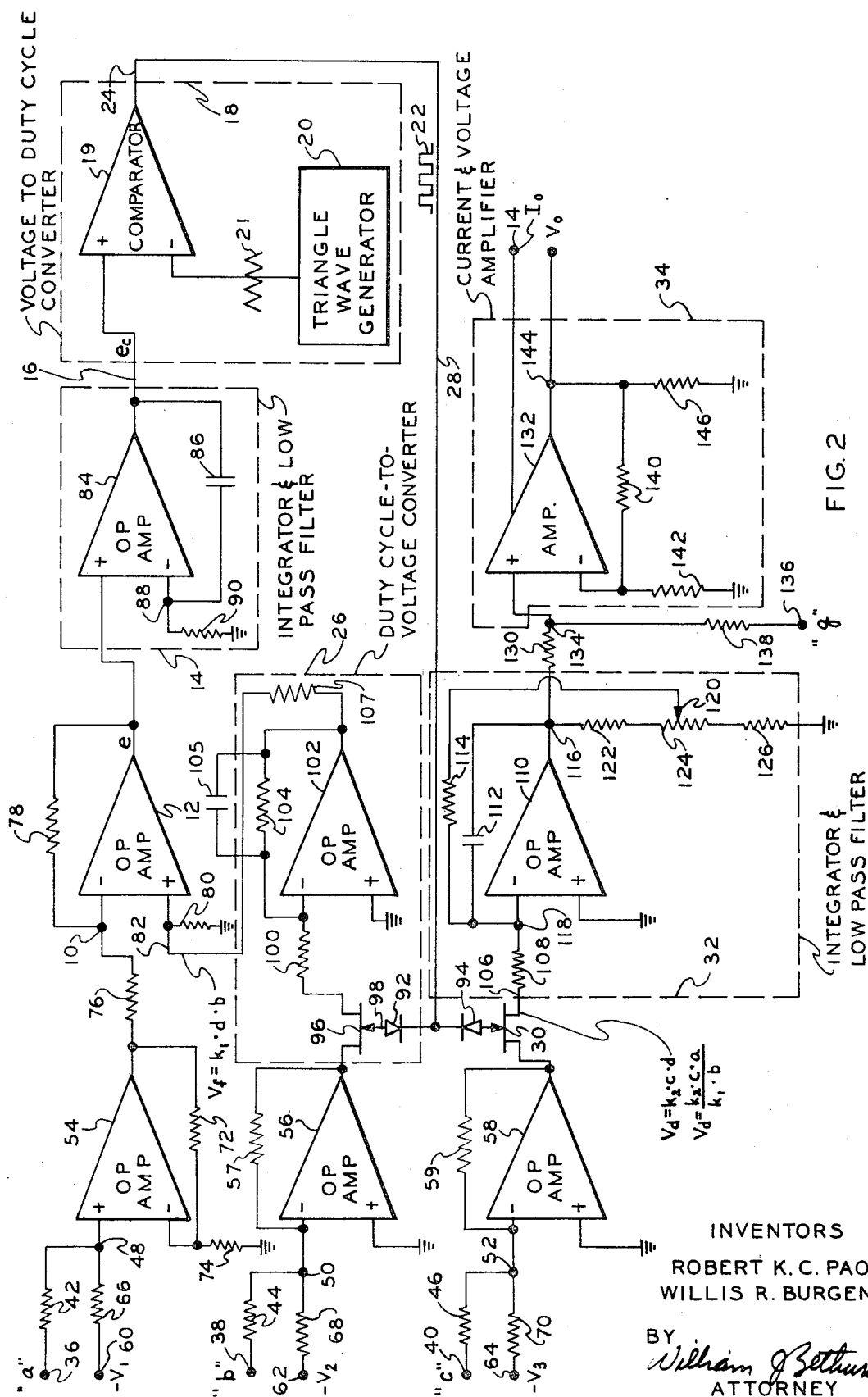


FIG. 1

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ELECTRONIC FEEDBACK CONTROLLED TIME-DIVISION MULTIPLIER AND/OR DIVIDER

FIELD OF THE INVENTION

This invention relates generally to electronic computing circuitry and more particularly to electronic circuitry capable of simultaneously multiplying and dividing three separate input variables.

BACKGROUND

Various types of time division multipliers and dividers have been employed in the prior art, and these electronic circuits are operable to generate an output voltage which is equal to some gain constant, k , times ac/b where a and c are the two independent input variables to be multiplied and b is the third independent input variable which is the divisor. For example, one type of known prior art circuit for performing the above algebraic function utilizes an operational amplifier to which is connected a first input variable a , and a separate multiplier stage is connected in the operational amplifier's feedback loop for receiving the divisor input variable b . When properly connected and biased, this closed-loop feedback system is operative to generate an output voltage which is proportional to the quantity a/b . The output of the operational amplifier may then be further connected to a second multiplier stage which is connectable to receive a third input variable c , so that the output of this second multiplier stage is an output voltage proportional to the quantity ac/b .

For a high degree of accuracy, the above type of prior art multiplier-divider system commonly utilizes a time division (pulse width modulation) technique which requires a precisely shaped clock waveform, such as a triangular waveform, to drive one or both of the above multiplier stages at some preselected clock frequency. While these prior art systems have operated satisfactorily in the past as long as the clock generators therefor produce this waveform or waveforms of a precise shape, these systems are subject to error where the shape of the above clock or time base generator waveform varies slightly from a precise chosen waveform shape. For example, this clock signal may be applied to one of two inputs of a differential comparator amplifier within the system and the independent variable signal voltage may be applied to the other input of the comparator amplifier and chopped or modulated in accordance with the precise shape of the periodic clock signal. When the shape of this clock signal varies slightly from its desired shape, then the switching threshold of the comparator amplifier will also vary as a result of the latter and thereby introduce error into the multiplying or dividing function of the system.

THE INVENTION

The general purpose of this invention is to provide a new and useful time division electronic multiplier and divider system having all of the advantages of the afore-described and other prior art time division multipliers and dividers, while at the same time providing true and accurate division and multiplication of three separate input variables independent of the precise shape of the waveform of the driving clock signal. To attain this, the multiplier-divider according to the present invention has been constructed to include a duty cycle controlled, closed-loop circuit servo system wherein a first analog input signal a is applied to the main or primary

signal translating portion of the servo loop and therein compared to a feedback signal V_f . A second analog divisor signal b is applied to the feedback circuit i.e. feedback loop of the system, and therein modulated by a variable duty cycle output signal at the output of the main signal translating portion to thereby produce the above feedback signal V_f . The main signal translating portion of the system includes means for generating an error signal which is a function of the difference between the feedback signal, V_f , and the a signal, and this error signal is modulated in a voltage-to-duty cycle converter to produce the variable duty cycle output signal proportional to a/b . This signal continuously forces V_f toward a , so that the a/b output signal is independent of the shape of the clock (modulating) signal used to chop the error voltage. This error voltage is the integral of the comparison difference signal of V_f and a , so that the system is provided with a good reset response, and additionally includes a desirable high D.C. gain and a high frequency stability. The a/b variable duty cycle output voltage may be utilized to modulate a third input signal variable c . This modulated signal V_d is proportional to $(a.c)/b$ and is then filtered and amplified for driving a final control element or the like in a process control system.

Accordingly, an object of the present invention is to provide a new and improved electronic multiplier-divider system for accurately generating the product and quotient of three independent input variables.

Another object of the invention is to provide a system of the type described whose error-free operation is independent of the precise shape of the waveform of the main clock generator of the system.

Another object of this invention is to provide new and useful electronic multiplier/divider circuitry of the type described which is particularly adaptable for use in the field of process control and which has a high static accuracy and a stable closed-loop response.

A further object of this invention is to provide a new and improved multiplier/divider system of the type described which may be simply and easily constructed using individually known, commercially available and relatively inexpensive operational amplifiers and solid-state electronic switches.

These and other objects and features of this invention will become apparent in the following description thereof.

DRAWINGS

FIG. 1 is a functional block diagram of a preferred embodiment of the electronic computing system according to the present invention, and

FIG. 2 is a detailed schematic diagram of the system shown in FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIG. 1, a first input signal a is received on input terminal 10 and is processed through a comparator 12 and through compensating networks 14 where it controls the generation of a compensates error voltage e_c on line 16 and at the input of the voltage-to-duty cycle converter stage 18. Stages 12 and 14 provide a means for generating the error signal e_c , and as will be described in detail below, the networks 14 provide integral reset action which continuously forces the output difference signal e of the comparator 12 to zero

during the generation of the variable duty cycle output signal 22. The converter stage 18 includes an operational amplifier comparator 19 which is driven by a clock pulse triangle waveform generator 20. The output signal of the comparator 19 has a duty cycle, d , is proportional to the analog value of e_c which determines the switching threshold of the comparator 19. Thus, comparator 19 and generator 20 provide a voltage-to-duty cycle converter functioning as means for receiving and modulating the error signal e_c . The stages described thus far are within the main or primary signal translating portion 13 of the system.

The variable duty-cycle signal 22 at the output terminal 24 of the stage 18 is fed directly into a duty-cycle-to-voltage converter 26 in the feedback portion 15 of the system, and the converter 26 is also simultaneously driven by a second independent divisor voltage b to generate a feedback signal V_f . The feedback voltage, V_f , which is returned to the comparator 12, may be expressed as

$$V_f = k_1 \cdot d \cdot b$$

(1)

where k_1 is the gain constant for the converter stage 26. When this servo loop is operating in its null condition, then the input signal $a = V_f$, the error difference signal e at the output of comparator 12 equals zero, and the compensated error signal e_c is constant. However, when e is any value other than zero, then the networks 14 continuously generate, by reset action, an integral error signal e_c which, by closed loop feedback control, forces V_f toward a and thereby produces the signal 22 proportional to a/b , and independent of the shape of the triangular waveform of generator 20.

The chopped signal 22 of duty cycle d on line 28 is provided as one input to an electronic switch 30, such as a field-effect transistor (FET), and this switch 30 is also simultaneously driven by a third independent variable input voltage c which is chopped or modulated in the switch 30 at the frequency of the variable duty-cycle signal 22 on line 28. Thus, the output voltage V_d of the electronic switch 30 may be expressed as

$$V_d = k_2 \cdot c \cdot d$$

(2)

where k_2 is equal to the gain constants associated with the incoming signal c . This voltage V_d at the output of switch 30 is filtered and integrated in the integrator and filter stage 32 and then amplified in the current amplifier stage 34 which includes both current and voltage outputs as shown in FIG. 2.

The multiplying and dividing functions accomplished by the present invention may be explained as follows with reference to FIG. 1, and this multiplying and dividing action will also be further discussed below with reference to FIG. 2.

For a null condition and with the error signal $e=0$, the incoming signal a is equal to the feedback voltage, V_f , so that

$$V_f = a = k_1 \cdot d \cdot b$$

(3)

Therefore, the variable duty-cycle signal 22 which is applied to the electronic switch 30 may be expressed as

$$d = (1/k_1) \cdot (a/b)$$

(4)

Since the variable duty-cycle signal 22 on line 28 modulates the input signal voltage c in the electronic switch 30, the output voltage V_d of the electronic switch 30 may, by combining equations (2) and (4) above, be expressed as

$$V_d = (k_2 k_1) \cdot (c \cdot a / b)$$

(5)

Thus, the output voltage, V_o , at the output of stage 34 may be expressed as

$$V_o = k_3 (k_1 / k_2) \cdot (c \cdot a) / b$$

(6)

where k_3 is the gain constant associated with stages 32 and 34. Therefore, from the equation 6 above, it can be seen that the output voltage, V_o , is independent of the precise shape of the triangular waveform at the output of the triangular wave generator 20 which drives the operational amplifier comparator 19, and this is an extremely significant feature of the present invention.

Referring now to FIG. 2 in detail, there are shown the a , b and c input terminals 36, 38, and 40, respectively, and the three input signals a , b and c are connected through their respective series input resistors 42, 44, and 46 to the summing junctions 48, 50, and 52 of the three isolation operational amplifiers 54, 56, and 58. A plurality of negative D.C. offset voltages $-V_1$, $-V_2$ and $-V_3$ are applied respectively to input terminals 60, 62, and 64 as shown, and these offset range setting voltages are connected through series resistors 66, 68 and 70 to the above identified summing junctions 48, 50 and 52. The isolation operational amplifier 54 has its inverting input terminal grounded through resistor 74 and also has a feedback resistor 72 connected as shown between the output and input of operational amplifier. The analog signal a is processed through the unity gain operational amplifier 54 and through the series resistor 76 into the summing junction 10 of the comparator or deviation operational amplifier 12. The isolation operational amplifiers 56 and 58 are further connected with feedback resistors 57 and 59, respectively and are also connected to drive the FET switches 30 and 96 as will be described further below.

The op amp comparator 12 has a feedback resistor 78 connected between its output node and the summing junction 10, and the noninverting input 82 of the comparator operational amplifier 12 is grounded through resistor 80. The operational amplifier input 82 is also connected to receive the feedback signal designated V_f which will be described in more detail below.

The output signal of the comparator operational amplifier 12 is an error signal e which is the difference between the analog input signal a and the servo loop feedback signal V_f . The error signal e is coupled through the compensating network 14 which comprises an integrator and low pass filter constructed using an operational amplifier 84 having a feedback capacitor 86 connected between the output thereof and the inverting input 88 of operational amplifier 84. The inverting input 88 of operational amplifier 84 is grounded as shown through resistor 90, and the integrator and low pass filter com-

compensating network 14 provides a desired high D.C. gain and a high frequency stability for the servo system described above. Furthermore, this network 14 continuously integrates the difference error signal e to generate e_c and thus provide a highly responsive reset action which continuously forces V_f to equal a .

The compensated (integrated and filtered) error signal e_c at the output node 16 of the operational amplifier 84 is connected to the noninverting input terminal of comparator 19 in the voltage-to-duty-cycle converter stage 18. The inverting input terminal of comparator 19 is connected to the output of a triangular wave generator 20 which provides the driving triangular waveform 21 for the comparator 19. When the triangular waveform 21 rises and falls above and below the analog level of the compensated analog signal e_c applied to the noninverting input of the comparator 19, the output of comparator 19 is switched between two discrete D.C. levels; and the duty cycle, d , of this rectangular wave output signal at the output 24 of the comparator 19 is proportional to the analog signal level of the compensated error signal e_c . This variable duty cycle signal 22 is independent of the exact shape of waveform 21 and is applied via feedback line 28 simultaneously to the cathodes of a pair of steering diodes 92 and 94, respectively. For example, if the slope of the triangular wave clock signal 21 should vary slightly from a preselected value, then momentarily the duty cycle, d , of feedback signal 22 will change as a result of operational amplifier 19 now switching at a different point in time within the period of the clock signal. This variation will momentarily produce a change in the level of V_f , and this change in V_f will in turn produce a corresponding change in e_c . This latter change compensates for the slope variation in the triangular waveform 21 and forces the duty cycle d to return to the value which causes V_f to equal a . Thus the duty cycle d varies only in accordance with the value of a/b and remains independent of the precise slope of the triangular clock waveform 21. Thus, this extremely important feature of the present invention substantially reduces the tolerance requirements for the circuit design of the triangular waveform generator 22, and this clock generator 20 is not required to provide an output triangular waveform 21 having a constant shape at all times. That is, the clock waveform is not required to have either a constant slope or a constant linearity at all times and may even undergo DC level shifts without affecting the duty cycle d of the output signal 22 of the comparator 19.

The b divisor signal which is processed through isolation operational amplifier 56 and applied to the source electrode of a first FET switch 96 is modulated in this switch by the negative going pulses 22 which are coupled through the steering diode 92, and this diode passes only the negative going pulses 22 to the gate electrode 98 of the N-channel FET 96. Thus, the b divisor signal is modulated in the FET 96 and has a duty cycle equal to the duty cycle of the rectangular wave feedback voltage 22. This modulated b signal is applied through an input resistor 100 to the inverting input of the integrating operational amplifier 102 within the duty cycle-to-voltage converter stage 26. The noninverting input of the op amp 102 is grounded, and the feedback resistor 104 and the input resistor 100 set the voltage gain of the converter stage 26. Operational amplifier 102, which also has an integrating feedback ca-

pacitor 105, provides the smoothing and filtering action for the chopped signal at the FET 96 and also provides the desired level of analog feedback signal V_f .

The feedback output voltage V_f of operational amplifier 102 is equal to $k_1 d \cdot b$ as set forth in equation (1), and this voltage V_f is coupled through output resistor 107 into the differential op amp 12 where it is compared to the analog signal a . The feedback voltage V_f continuously drives the error voltage e at the output of the operational amplifier 12 towards zero during variations of the a and b signals, and it is seen from equation (4) above that the duty cycle d of the rectangular wave signal 22 is proportional to a/b and independent of the shape of the triangular wave clock signal 21.

The feedback signal 22 is also coupled through a steering diode 94 into the gate of a second FET switch 30 to modulate the multiplier analog signal c which is fed into the source of FET 30. The output voltage V_d on the drain 106 of the FET 30 is given in equation (5) above, so it is seen that the system embodying the present invention simultaneously multiplies the first analog a input signal by the third analog c input signal and divides this product by the second analog b input signal.

The V_d signal on the FET drain 106 is coupled through an input resistor 108 to the inverting input of the operational amplifier 110 within the integrator and low pass filter stage 32. The noninverting input of the operational amplifier 110 is grounded, and a feedback capacitor 112 and a feedback resistor 114 are connected as shown to the input summing junction 118 of operational amplifier 110. A variable tap 120 on potentiometer 124 and the fixed output resistors 122 and 126 are utilized to set the scale factor of the system, and this stage 32 filters and smooths the chopped signal coupled from the FET 30 to the summing junction 118. The gain of the integrator and low pass filter stage 32 is established in accordance with the values of the input and feedback resistors 108 and 114 and also output resistors 122, 124 and 126.

The output node 116 of operational amplifier 110 is coupled through an input resistor 130 to the noninverting input of the output current and voltage amplifier 132, and if desired, an additional offset voltage g may be applied as shown via resistor 138 to the summing junction 134 of the amplifier 132. The gain of the amplifier 132 is set in accordance with the values of feedback resistor 140, and the grounded input resistor 142 which is connected to the inverting input of the amplifier 132.

The amplifier stage 132 may advantageously be constructed with a differential operational amplifier "front end" (not shown) and with a Darlington output stage (not shown), and these stages may be connected in cascade in a well known manner to provide the desired current and voltage gains for the integrated and filtered signal at node 134. For improved stability in the output, it is desirable to provide feedback via resistor 140 around both the operational amplifier and Darlington stages within the amplifier 132, and the amplifier network 34 has both a voltage output V_o and a current output I_o . The output resistor 146 is the Darlington series output resistor which establishes the relationship between the output current I_o and output voltage V_o .

In view of the foregoing, it will be seen that the several objects of the invention are achieved and other advantageous results attained.

As various changes could be made in the construction herein described without departing from the scope of the invention, it is intended that all matter contained in the above description are shown in the accompanying drawings be interpreted as illustrative rather than in a limiting sense.

e claim:

1. A system for dividing a first or a analog input signal by a second or b analog input signal including, in combination:

- a. a closed loop circuit comprising a main signal translating portion and a feedback portion,
- b. means in said main signal translating portion for receiving said a analog input signal,
- c. error signal generating means in said main signal translating portion, connected to said receiving means, for comparing said a analog input signal with a feedback signal, V_f , generated in said feedback loop portion thereby to generate an error signal,
- d. means in said main signal translating portion and coupled to said error signal generating means for modulating said error signal by a selected waveform to produce a variable duty cycle output signal, and
- e. means in said feedback portion for modulating said b analog signal by said variable duty cycle output signal for generating said feedback signal, V_f , whereby said error signal continuously forces V_f to equal a , and the variable duty cycle output signal at the output of said modulating means has a duty cycle which is proportional to a/b and is substantially independent of the precise shape of the waveform utilized to modulate said error signal.

2. The system defined in claim 1 wherein said error signal generating means includes a differential comparator having one input thereof connected to receive said a analog input signal and a second input thereof connected to said feedback portion to receive said feedback signal, V_f , and to generate an output signal proportional to the difference between a and V_f .

3. The system defined in claim 2 wherein said error signal generating means further includes means connected between said differential comparator and said modulating means for integrating said output signal from said differential comparator and continuously changing when said output signal is not zero to force V_f towards a and force the output of said modulating means to be proportional to a/b .

4. The system defined in claim 1 wherein said modulating means comprises a voltage-to-duty cycle converter including a differential comparator connected to receive said error signal at one input thereof and further connected to a triangular wave generating means, whereby said error signal and a triangular wave clock signal from said generating means drive said differential comparator between two D.C. levels at a duty cycle proportional to a/b .

5. The system defined in claim 1 wherein said means in said feedback portion for modulating said b analog signal includes:

- a. switch means having an input electrode connected to receive said b analog signal and a control electrode connected to receive said variable duty cycle output signal from said modulating means, whereby said b analog signal is modulated in accordance

with the duty cycle of said output signal from said modulating means, and

- b. amplifier means interconnecting an output electrode of said switch means to an input of said differential comparator thereby to convert said modulated b signal to said feedback voltage, V_f .

6. The system defined in claim 5 which further includes a second switch means having an input electrode thereof connected to receive a c multiplying analog signal and having a control electrode connected to receive said variable duty cycle output signal from said modulating means, whereby the output signal of said second switch means is proportional to $a \cdot c/b$, whereby said system operates to simultaneously multiply and divide said a , b and c analog signals.

7. The system defined in claim 3 wherein said modulating means includes a voltage-to-duty cycle converter electrically coupled to the output of said comparing means to generate said variable duty cycle output signal which is proportional to the amplitude of said error signal.

8. The system defined in claim 7 wherein said voltage-to-duty cycle converter includes a differential comparator for receiving said error signal at one input thereof and for receiving a triangular wave clock pulse at the other input thereof for switching the output of said last named differential comparator at a duty cycle proportional to the amplitude of a/b .

9. The system defined in claim 8 wherein said means in said feedback portion for modulating said b analog signal includes:

- a. switch means having an input electrode connected to receive said b analog signal and a control electrode connected to receive said variable duty cycle output signal from said modulating means, whereby said b analog signal is modulated in accordance with the duty cycle of said output signal from said modulating means, and
- b. amplifier means interconnecting an output electrode of said switch means to an input of said differential comparator thereby to convert said modulated b signal to said feedback voltage, V_f .

10. The system defined in claim 9 which further includes a second switch means having an input electrode thereof connected to receive a c multiplying analog signal and having a control electrode connected to receive said variable duty cycle output signal from said modulating means, hereby the output signal of said second switch means is proportional to $a \cdot c/b$, and said system operates to simultaneously multiply and divide said a , b and c analog signals.

11. The system defined in claim 10 wherein said integrating means includes an integrator and low pass filter interconnecting the output of said first named differential comparator and one input of said second named differential comparator for integrating the differential output signal at the output of said first named comparator and providing reset action in the generation of said error signal, said integrator and low pass filter further providing a high DC gain and a high frequency stability for said system.

12. The system defined in claim 11 which further includes:

- a. a first input isolation amplifier connected between said first named differential comparator and an a analog input voltage terminal for summing said a analog input voltage with a first offset voltage,

- b. a second isolation amplifier interconnected between the input electrode of said first named switch means and a *b* analog input terminal, and said *b* analog signal being summed at the input of said second isolation amplifier with a second offset voltage, and
- c. a third isolation amplifier interconnected between the input electrode of said second named switch means and a *c* analog voltage input terminal, hereby said *c* analog signal may be summed with a third offset voltage at the input of said third isolation amplifier, whereby the ranges of currents and voltages at the outputs of said output stage may be varied in accordance with said first, second and third offset voltages which are summed with said *a*, *b* and *c* analog input signals, respectively.

13. The system defined in claim 12 wherein said first and second switch means are field-effect transistors each having source, gate and drain electrodes, with the gate electrodes thereof interconnected through first and second blocking diodes, respectively, to the output of said voltage-to-duty cycle converter, whereby said first and second blocking diodes unidirectionally pass said variable duty cycle output signal to the respective gate electrodes of said first and second field-effect transistors to control the signal modulation therein.

14. A system for dividing a first analog signal by a second analog signal and for multiplying their quotient by a third analog signal, said system including, in combination:

- means for receiving a first analog signal,
- means connected to said receiving means for comparing said first analog signal with a feedback signal and for generating from the comparison an error signal which is dependent upon variations in said first analog or feedback signals,
- first conversion means coupled to said error signal generating means for pulse modulating said error signal and producing a variable duty cycle output signal proportional thereto, and
- feedback means connected to the output of said first conversion means and including second conversion means connected to receive both said variable duty cycle output signal and said second analog signal and responsive thereto to generate said a feedback signal, whereby said error signal continuously forces said feedback signal toward said first analog signal toward and forces the duty cycle of the output signal of said first conversion means to be proportional to a/b , and
- means for modulating said third analog signal by said variable duty cycle signal to produce an output signal proportional to said quotient multiplied by said third analog signal.

15. The system defined in claim 14 wherein said error signal generating means includes comparator means connected to both said receiving means and to said second conversion means for comparing said feedback signal and said first analog signal and for generating an output signal representing the difference between the

latter two signals.

16. The system defined in claim 15 wherein

- said error signal generating means further includes an integrating amplifier coupled to the output of said comparator means for providing reset action and a continuously varying output error signal when said first analog signal and said feedback signal are not equal to zero, said integrating amplifier also providing a high D.C. gain and a high frequency stability for said system and
- said first conversion means includes differential comparator means having a first input thereof connected to receive the integrated error signal from said integrating amplifier and having a second input thereof connected to receiving a triangular waveform clock signal, whereby said differential comparator means is switched to provide a pulse width modulated output signal having a varying duty cycle determined by relative levels of said integrated error signal and said triangular waveform clock signal.

17. The system defined in claim 16 wherein said second conversion means includes:

- switching means having one input thereof connected to receive said variable duty cycle output signal from said first conversion means and having a second input thereof connected to receive said second analog signal, whereby said second analog signal is modulated in accordance with the duty cycle of said output signal from said first conversion means, and
- said second conversion means further includes amplifier means interconnecting the output of said stitching means to an input of said comparator means for continuously driving the signal output voltage of said comparator means towards zero during variations of said first and second analog input signals.

18. The system defined in claim 17 wherein said means for modulating said third analog input signal comprises a second switching means having one input thereof connected to receive said variable duty cycle output signal from said first conversion means and a second input thereof connected to receive a said third analog input signal.

19. The system defined in claim 18 which further includes amplifier and filter means connected to the output of said second switching means for amplifying and filtering the modulated output signal of said second switching means and providing a high gain and the required filtering for the output of said system.

20. The system defined in claim 19 which further includes an output bias and current driver stage connected to output of said amplifier and filter means and providing a desired range of output currents and voltages suitable for driving transducer type final control elements in a process control system.

21. The system defined in claim 20 herein said first and second switching means are field-effect transistors.

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