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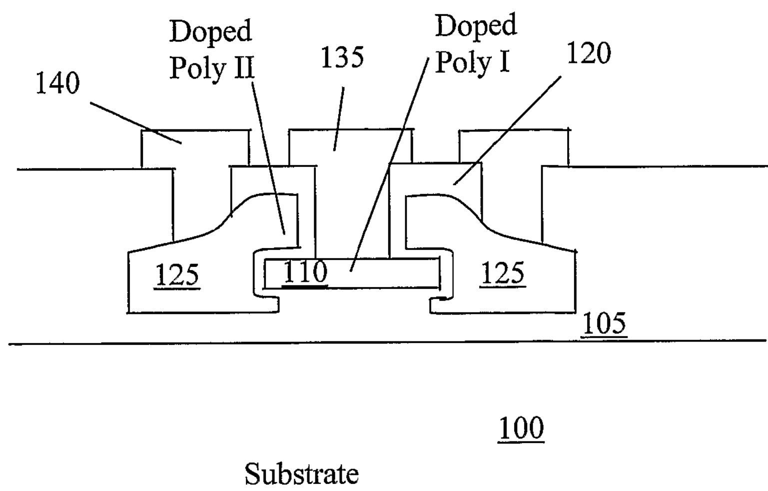
(54) Title: ONE TIME PROGRAMMABLE MEMORY CELL



(57) Abstract: This invention discloses a one-time programmable (OTP) memory cell. The OTP memory cell includes a dielectric layer disposed between two conductive polysilicon segments wherein the dielectric layer is ready to change from a non-conductive state to a conductive state through an induced voltage breakdown. In a preferred embodiment, one of the conductive polysilicon segments further includes an etch undercut configuration for conveniently inducing the voltage breakdown in the dielectric layer. In a preferred embodiment, the dielectric layer is further formed as sidewalk covering the edges and corners of a first polysilicon segments to conveniently induce a voltage breakdown in the dielectric layer by the edge and corner electrical field effects.

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ONE TIME PROGRAMMABLE MEMORY CELL

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

The invention disclosed herein relates generally to the structure and manufacturing process of a memory cell. More particularly, this invention relates to a novel cell structure and manufacturing process of a write once
10 programmable memory.

2. Description of the Prior Art

In order to reduce cost and to shorten the time-to-market of integrated
15 circuit (IC) products, the design houses are increasingly relying on the readily available foundry processes to carry out the prototyping and manufacturing. However, the device features that are tailored for post-package trimming require additional intellectual property (IP) modules or fuse. These IP modules may include one time programmable (OTP) memory or the electrical
20 erasable programmable read only memory (EEPROM) provided by the foundry with additional costs. In the case of fuse, fuse-trimming using dedicated testing equipment with specific test configuration setup and high current is required. All these extra processing or testing requirements cause delays for shipping the products to the market and also increase the
25 production costs. For these reasons, it is desirable to reduce as much as possible the requirements for post-packaging trimming and testing of these device features.

However, conventional techniques of configuring and designing such
30 OTP memory or EEPROM cell for IC devices require complex processing.. In US Patent 4,698,900 a method for making a non-volatile memory with dielectric filled trenches was disclosed. The invention provides a cross point EPROM array that has trenches to provide improved isolation between adjacent buried N+ bit-lines at locations where the adjacent buried N+ bit-
35 lines are not separated by a FAMOS transistor. This results in improved leakage current, improved punch-through voltage characteristics, and in improved programmability for the cell. In another US Patent 6,215,140,

Reisinger, et al. disclosed an electrically programmable non-volatile memory cell configuration. The semiconductor substrate is of the first conductivity type. Trenches are aligned to be parallel to one another and are incorporated in the semiconductor substrate, and first address lines run along the sidewalls of the trenches. Second address lines are formed on the semiconductor substrate, transversely with respect to the trenches. Semiconductor substrate regions, in which a diode and a dielectric whose conductivity can be changed are arranged, are located between the first address lines and the second address lines. A suitable current pulse can be used to produce a breakdown in the dielectric, with information thus being stored in the dielectric. US Patent 6,584,029 disclosed a one-time programmable memory using fuse/anti-fuse and a vertically oriented fuse unit memory cell. The one-time programmable ("OTP") memory includes one or more memory arrays stacked on top of each other. The OTP memory array is a cross-point array where unit memory cells are formed at the cross-points. The unit memory cell may include a fuse and an anti-fuse in series with each other or may include a vertically oriented fuse. Programming the memory may include the steps of selecting unit memory cells, applying a writing voltage such that critical voltage drop across the selected cells occur. This causes the anti-fuse of the cell to break down to a low resistance. The low resistance of the anti-fuse causes a high current pulse to be delivered to the fuse, which in turn melts the fuse to an open state. Reading the memory may include the steps of selecting unit memory cells for reading, applying a reading voltage to the selected memory cells and measuring whether current is present or not.

The above patented memory cell configurations however does not provide a solution to allow for application of standard foundry processes to enable low-cost post-packaging trimming requirements. Therefore, a need still exists in the art to provide an improved memory configuration and manufacturing methods to provide the one-time programmable memory cells using standard foundry process such that the above discussed difficulties as now encountered in the prior art can be resolved.

SUMMARY OF THE PRESENT INVENTION

It is therefore an object of the present invention to provide a new and improved one-time programmable (OTP) memory cell by using standard IC

manufacturing processes commonly implemented in the foundries such that the above discussed difficulties and limitations may be resolved.

Specifically, it is an object of the present invention to provide a one-time programmable (OTP) memory cell by taking advantage of the sidewall and corner breakdown features of a thin oxide layer overlying a polysilicon segment. The phenomena of etch undercut prior to the gate oxidation further degrades the breakdown property of the thin oxide. In general, special attention needs to be paid to avoid the inter-poly oxide low breakdown issues in conventional IC poly-poly capacitors or flash/EEPROM memory interpoly coupling layers (for example, high quality oxide-nitride-oxide composite layers are commonly used). However in this invention disclosure, the weakness of the inter-poly sidewall oxide breakdown is utilized to our advantage as a programming mechanism for the OTP cell. As a breakdown and conductivity between two polysilicon layers can be more conveniently generated, this undesirable poly segment sidewall configuration is implemented for inducing a breakdown and for changing the conductivity state to perform the one-time program function.

Briefly in a preferred embodiment this invention discloses a one-time programmable (OTP) memory cell. The OTP memory cell includes a dielectric layer disposed between two conductive polysilicon segments wherein the dielectric layer is ready to change from a non-conductive state to a conductive state through an induced voltage breakdown. In a preferred embodiment, one of the conductive polysilicon segments further includes an etch undercut configuration for conveniently inducing the voltage breakdown in the dielectric layer. In another preferred embodiment, one of the conductive polysilicon segments further includes an etch undercut configuration for conveniently inducing the voltage breakdown in the dielectric layer via a corner electrical field effect. In another preferred embodiment, the dielectric layer constituting a sidewall covering one of the conductive polysilicon segments with an etch undercut configuration for inducing the voltage breakdown in the dielectric layer via an edge electrical field effect. In another preferred embodiment, one of the conductive polysilicon segments further includes a corner for conveniently inducing the voltage breakdown in the dielectric layer via a corner electrical field effect. In another preferred embodiment, the OTP memory cell further includes a

semiconductor substrate having an insulating layer disposed on a top surface of the substrate for supporting the OTP memory cell thereon. In another preferred embodiment, the OTP memory cell further includes an insulating passivation layer covering the OTP memory cell and the insulating passivation layer further includes contact opening for depositing electrode metal therein to for electrically contacting the conductive polysilicon segments to function as electrodes. In another preferred embodiment, the conductive polysilicon segments are conductive impurity doped polysilicon segments. The conductive polysilicon segments can be a P-type impurity doped or N-type impurity doped polysilicon segment.

This invention further discloses a method for manufacturing a one-time programmable (OTP) memory cell. The method includes a step of disposing a dielectric layer between two conductive polysilicon segments for readily inducing a voltage breakdown in the dielectric to change from a non-conductive state to a conductive state for carrying out a one-time program operation. In another preferred embodiment, the method further includes a step of forming one of the conductive polysilicon segments with an etch undercut configuration for conveniently inducing the voltage breakdown in the dielectric layer. In another preferred embodiment, the method further includes a step of forming one of the conductive polysilicon segments with an etch undercut configuration with a corner for conveniently inducing the voltage breakdown in the dielectric layer via a corner electrical field effect. In another preferred embodiment, the method further includes a step of forming one of the dielectric layer as a sidewall covering one of the conductive polysilicon segments with an etch undercut configuration for inducing the voltage breakdown in the dielectric layer via an edge electrical field effect. In another preferred embodiment, the method further includes a step of forming one of the conductive polysilicon segments with a corner for conveniently inducing the voltage breakdown in the dielectric layer via a corner electrical field effect.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment, which is illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a side cross sectional view of a one-time programmable memory cell of this invention.

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Figs. 2A to 2G are a serial of side cross sectional views for illustrating the processing steps for manufacturing the OTP memory cell of Fig. 1.

DETAILED DESCRIPTION OF THE METHOD

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Referring to Fig. 1 for a one-time programmable memory cell of this invention supported on a thick field oxide layer 100 formed on a top surface of a semiconductor substrate 100. The thick field oxide layer 105 insulates the cell from the substrate 100. A first doped poly region 210 is insulted with a

15 thin layer low voltage gate oxide 120 from a second doped polysilicon region 125. Each poly region has an electrode, e.g., electrodes 135 and 140 respectively, connected for data recording and reading. The thin gate oxide layer 120 between the two doped poly regions blocks the conductivity between the two doped poly regions 110 and 125. However, the conducting

20 status between the two doped poly regions 110 and 125 may be changed for the purpose of programming the memory. In the process of programming the memory cell as shown in Fig. 1, a high voltage may be applied to the electrodes between doped poly regions 110 and 125. When the voltage is high enough, a breakdown is induced in the single crystal thin gate oxide layer 120

25 and becomes conductive. The high voltage therefore changes the conductance between the two doped poly regions 110 and 125 and is employed to store a binary bit in the cell. The threshold voltage is related to the thickness as well as the micro microstructure of the oxide layer 120.

30 The key features as that shown in Fig.1 are the relative positions of the second polysilicon poly-2 segment 125 over the first polysilicon poly-1 segment. The sidewall overlaying the poly-1 segment 110 includes a corner undercut. With the undercut and edge effects of the thin oxide layer 120 as sidewall covering the poly-1 segment 110, a breakdown can be conveniently

35 induced and the state of conductivity can be more easily changed for writing a binary bit into the memory cell by applying a high voltage over the electrodes 135 and 140.

Referring to Figs. 2A to 2F for a serial of side cross sectional views for the illustration of the processing steps to fabricate the one-time programmable memory cell of Fig. 1. In Fig. 2A, a field oxide layer 205 of approximately three to eight Angstrom thickness is formed on top of a semiconductor substrate 200 by using a thermal oxidation process. In Fig. 2B, a polysilicon layer 210 of approximately 500 to 2000 Angstroms in layer thickness is deposited on top of the field oxide layer 205. A N-type or P-type ion implant with an ion flux intensity of approximately $1X10^{14}$ to $1X10^{15}$/cm2 is then carried out over the polysilicon layer 210 to make the poly-1 more conductive. A mask is then applied to etch and pattern the polysilicon layer 210 to form a poly-1 segment 210 as shown. A high voltage oxide layer 215 is grown over the poly-1 segment.

In Fig. 2C, the high voltage oxide layer 215 is etched off in the active cell area and maintaining the high voltage oxide layer in the peripheral region to support the high voltage recording operation. The etch process produces an undercut 218 below the edge of the poly-1 segment 210. In Fig. 2D, a thin layer of low voltage oxide 220 of approximately 120 Angstroms in thickness is grown over the poly-1 segment 210. In Fig. 2E, a second polysilicon layer 225 is deposited. An ion implant is carried out on the second polysilicon layer 225 with a similar dopant concentration with either a N-type or P-type ions. Then a mask is applied to etch and pattern the second polysilicon layer 225 as that shown in Fig. 2E. In Fig. 2F, an oxide or BPSG layer 230 is deposited over the top to cover the entire top surface. Then in Fig. 2G, a contact mask is applied to open contact holes in the BPSG layer 230 and the metal contact is then deposited into the contact openings to form the electrodes 235 and 240 for establishing electric contacts to the doped poly-1 and poly 2 layers 210 and 225 respectively.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alterations and modifications will no doubt become apparent to those skilled in the art after reading the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alterations and modifications as fall within the true spirit and scope of the invention.

CLAIMS

We claim:

1. A one-time programmable (OTP) memory cell comprising:

5

a dielectric layer disposed between two conductive polysilicon segments wherein said dielectric layer is ready to change from a non-conductive state to a conductive state through an induced voltage breakdown.

10

2. The one-time programmable (OTP) memory cell of claim 1 wherein:

one of said conductive polysilicon segments further includes an etch undercut configuration for conveniently inducing said

15 voltage breakdown in said dielectric layer.

3. The one-time programmable (OTP) memory cell of claim 1 wherein:

one of said conductive polysilicon segments further includes an

20 etch undercut configuration for conveniently inducing said voltage breakdown in said dielectric layer via a corner electrical field effect.

4. The one-time programmable (OTP) memory cell of claim 1

25 wherein:

said dielectric layer constituting a sidewall covering one of said conductive polysilicon segments with an etch undercut configuration for inducing said voltage breakdown in said dielectric layer via an edge electrical field effect.

30

5. The one-time programmable (OTP) memory cell of claim 1 wherein:

one of said conductive polysilicon segments further includes a corner for conveniently inducing said voltage breakdown in

35 said dielectric layer via a corner electrical field effect.

6. The one-time programmable (OTP) memory cell of claim 1 further comprising:

5 a semiconductor substrate having an insulating layer disposed on a top surface of said substrate for supporting said OTP memory cell thereon.

7. The one-time programmable (OTP) memory cell of claim 1 further comprising:

10

an insulating passivation layer covering said OTP memory cell and said insulating passivation layer further includes contact opening for depositing electrode metal therein to for electrically contacting said conductive polysilicon segments to function as

15 electrodes.

8. The one-time programmable (OTP) memory cell of claim 1 wherein:

said conductive polysilicon segments comprising conductive

20 impurity doped polysilicon segments.

9. The one-time programmable (OTP) memory cell of claim 1 wherein:

at least one of said conductive polysilicon segments comprising

25 N-type impurity doped polysilicon segments.

10. The one-time programmable (OTP) memory cell of claim 1 wherein:

at least one of said conductive polysilicon segments comprising

30 P-type impurity doped polysilicon segments.

11. A method for manufacturing a one-time programmable (OTP) memory cell comprising:

5 disposing a dielectric layer between two conductive polysilicon segments for readily inducing a voltage breakdown in said dielectric to change from a non-conductive state to a conductive state for carrying out a one-time program operation.

12. The method of claim 11 further comprising:

10

forming one of said conductive polysilicon segments with an etch undercut configuration for conveniently inducing said voltage breakdown in said dielectric layer.

15 13. The method of claim 11 further comprising:

forming one of said conductive polysilicon segments with an etch undercut configuration with a corner for conveniently inducing said voltage breakdown in said dielectric layer via a

20 corner electrical field effect.

14. The method of claim 11 further comprising:

forming one of said dielectric layer as a sidewall covering one of

25 said conductive polysilicon segments with an etch undercut configuration for inducing said voltage breakdown in said dielectric layer via an edge electrical field effect.

15. The method of claim 11 further comprising:

30

forming one of said conductive polysilicon segments with a corner for conveniently inducing said voltage breakdown in said dielectric layer via a corner electrical field effect.

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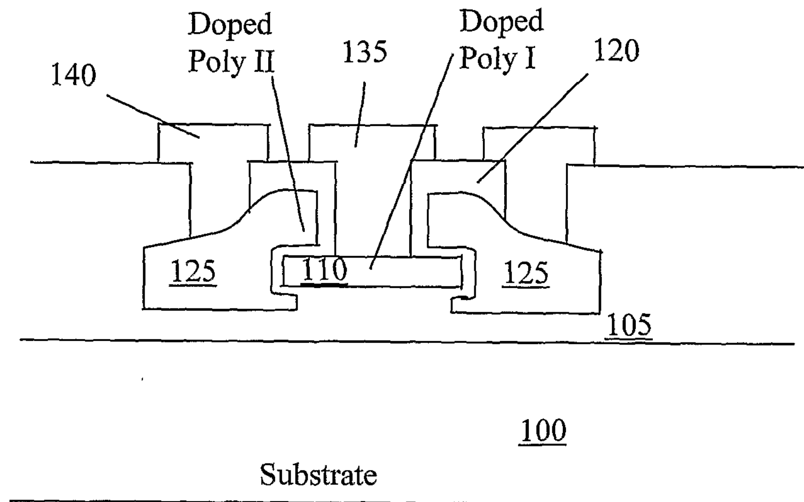

Fig. 1

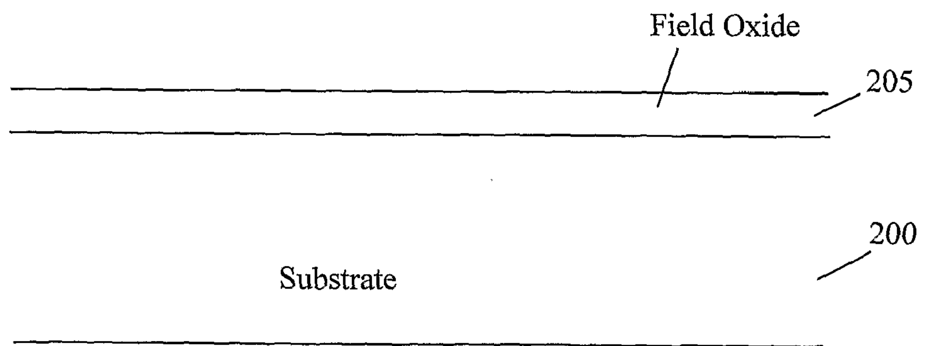

Fig. 2A

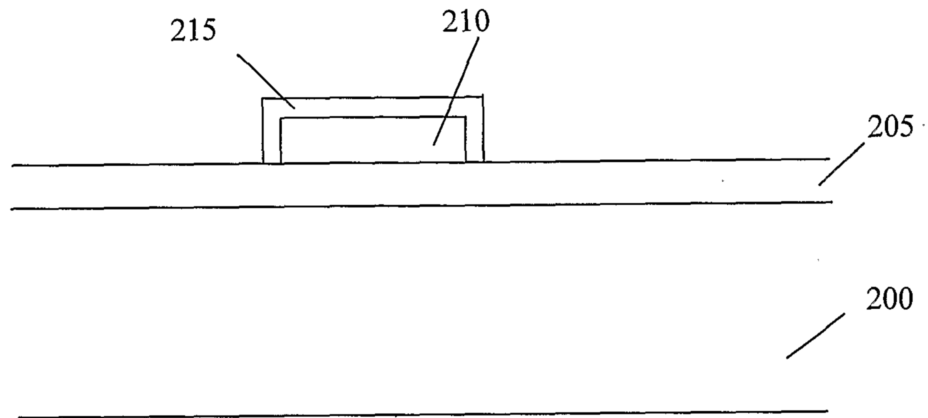

Fig. 2B

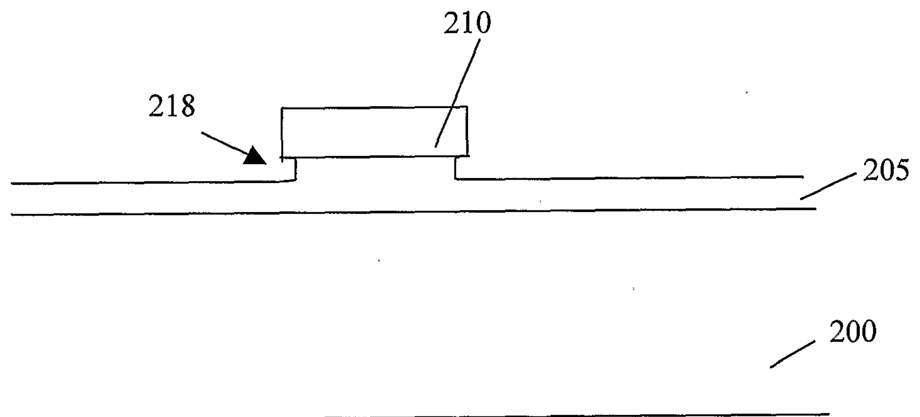

Fig. 2C

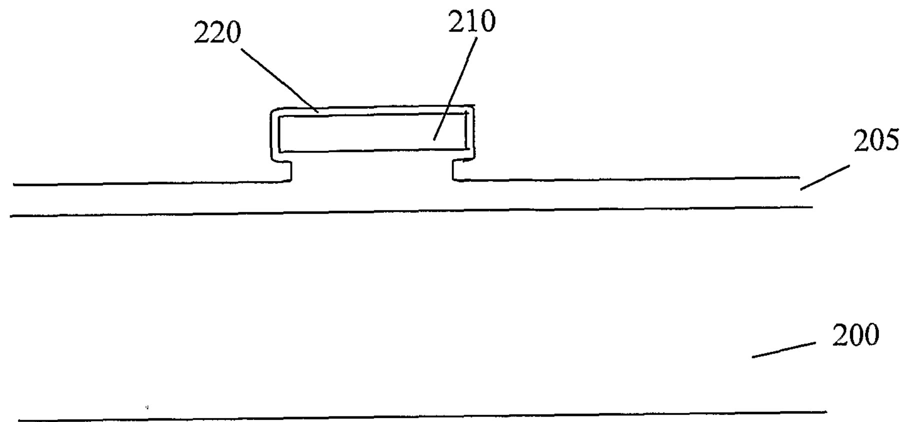

Fig. 2D

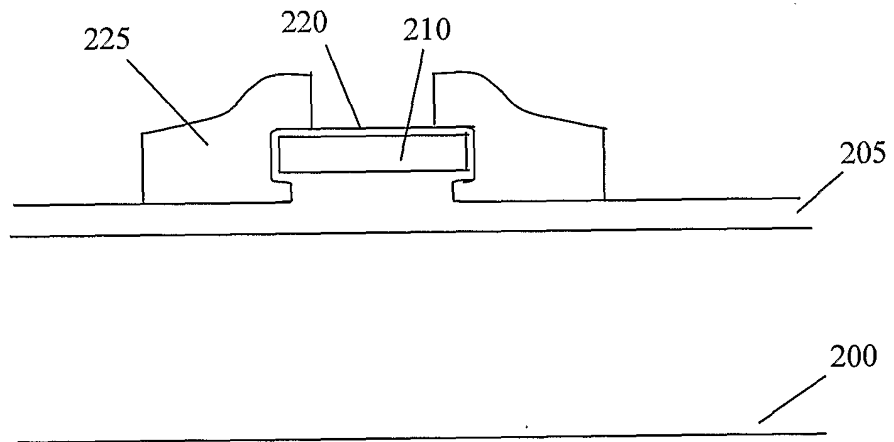

Fig. 2E

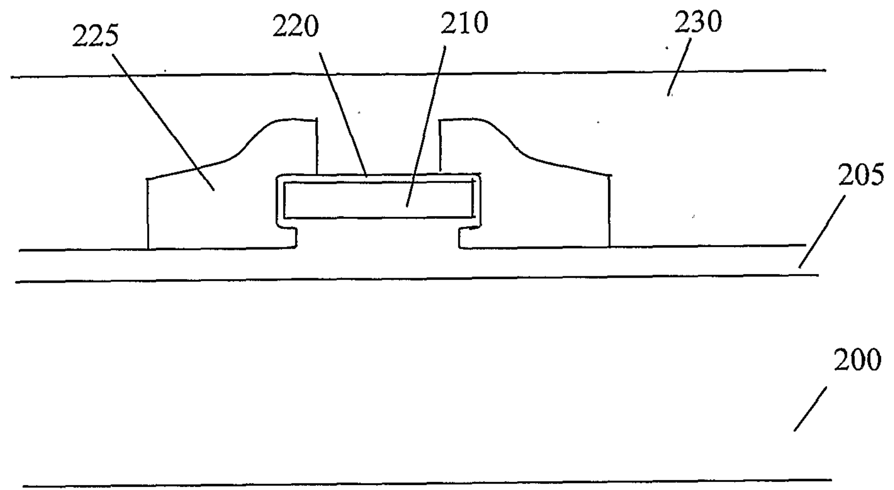

Fig. 2F

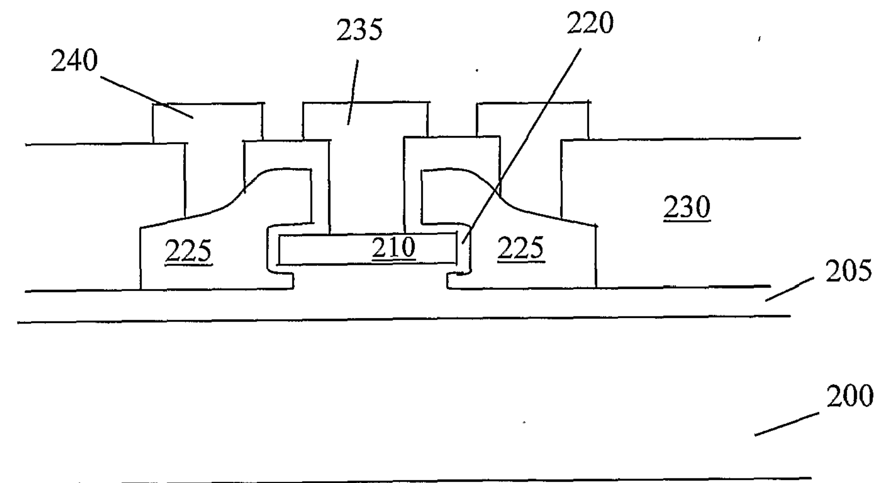

Fig. 2G