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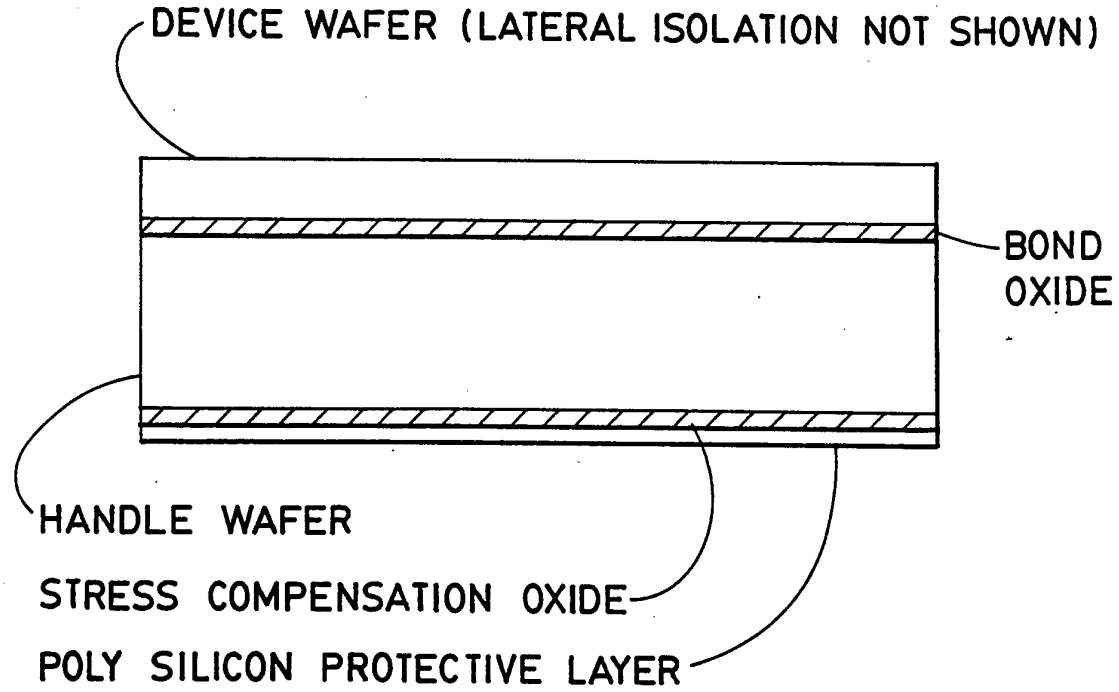
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(54) Title: BONDED WAFER PROCESSING



(57) Abstract

Warpage in a bonded wafer is limited by maintenance of a stress compensation layer on the backside of the bonded wafer during device fabrication processing. One embodiment applies a sacrificial polysilicon layer over a stress compensation silicon dioxide layer for bonded silicon wafers. The fabrication processing consumes the polysilicon layer but not the stress compensation silicon dioxide.

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BONDED WAFER PROCESSING

BACKGROUND AND SUMMARY OF THE INVENTIONS

The present invention relates to electronic integrated circuits and methods of fabrication, and, more particularly, to dielectrically isolated semiconductor integrated circuits and related fabrication methods.

Silicon-on-insulator substrates

Integrated circuits fabricated in silicon-on-insulator substrates offer performance advantages including freedom from latchup for CMOS structures, high packing density, low parasitic capacitance, low power consumption, radiation hardness, high voltage operation, and the possibility of three dimensional integration. Indeed, isolation trenches extending through the silicon layer down to the insulation provide a simple approach to dielectric isolation of integrated circuit devices. The sidewalls of such trenches are coated with an insulator, usually silicon dioxide ("oxide"), and the remaining portion of trench opening, if any, is filled with a filler which is usually polycrystalline silicon. Diffused PN junctions can also be used for lateral isolation.

Additionally, silicon-on-insulator technology using very thin films offers special advantages for submicron devices. Scaling bulk devices tends to degrade their characteristics because of small-geometry effects, such as punch-through, threshold voltage shift, and subthreshold-slope degradation. The use of silicon-on-insulator devices suppresses these small-geometry effects. Therefore, even in the submicron VLSI era, silicon-on-insulator technology can offer even higher device performance than can bulk technology, along with the inherent advantages of silicon-on-insulator.

Silicon-on-insulator substrates may be fabricated in various ways: a crystalline silicon layer may be formed over an

existing oxide layer either by laser or strip heater recrystalization of polysilicon deposited on the oxide or by selective epitaxial silicon growth over the oxide. However, the quality of such a silicon layer is generally inferior to that normally associated with bulk silicon. Other approaches form an oxide layer beneath an existing high quality silicon layer either by oxidizing a buried porous silicon layer or by oxygen ion implantation; however, such oxide is low quality and the silicon top layer may be damaged during the oxide layer formation.

Another approach to silicon-on-insulator is wafer bonding as described by J. Lasky et al., Silicon-On-Insulator (SOI) by Bonding and Etch-Back, 1985 IEDM Tech. Deg. 684. This wafer bonding process proceeds as follows: a lightly doped epitaxial layer of silicon is grown on a heavily doped silicon substrate, oxide is thermally grown on the epilayer, a second lightly doped silicon substrate is thermally oxidized, the two oxidized surfaces are pressed together. See Figure 1a. The pressed together wafers are inserted into an oxidizing atmosphere at 1,100°C to bond them as illustrated in Figure 1b. Lastly, a preferential etch is used to remove the heavily doped substrate, leaving the thin, lightly doped epitaxial layer above the bonded thermally grown oxides which are now on the second substrate as shown in Figure 1c. The resulting thin silicon layer above the thermally grown oxide has high quality and the oxide also retains its quality and may be thick, as might be desired for CMOS or high voltage devices, or then, as might be desired for shared element applications. Figure 1d heuristically illustrates trench isolation with poly filled trenches isolating MOSFET and bipolar devices.

Conceptually, this process may meet all the desired goals for the ultimate silicon-on-insulator material (a specular finished crystalline silicon layer without dislocations and a back interface with the insulator of quality equal to the interface of thermally grown silicon dioxide on

silicon; both the crystalline silicon layer and the insulator of variable thickness).

Another wafer bonding method, illustrated in Figures 2a-c and described in copending U.S.Patent Application Serial No. _____, filed _____, proceeds as follows. Start with a device wafer having a lightly doped epilayer on a heavily doped substrate and a handle wafer with a thick (4,000 A) oxide layer. Activate the surface of the device wafer with an acid or peroxide wash to enhance hydroxyl group formation. Place a drop of oxidant such as water plus hydrogen peroxide on the oxide, and squeeze the wafers together. See Figure 2a. The drop of oxidant has a volume in the range of 0.8 to 8.0 microliters per square inch of wafer surface. Dry the squeezed wafers at room temperature for a day and then heat the squeezed wafers to 1150 degrees C for two hours. The heating drives an oxidation of the device wafer and the silicon-oxygen bonds formed fuse the two wafers. See Figure 2b. Lastly, grind and etch back the device wafer until exposure of the device epilayer. This completes the silicon-on-insulator substrate as shown in Figure 2c.

However, bonded wafers have problems including warpage. In particular, the oxide (or other dielectric) used to bond the two wafers together is usually formed in a stressed condition. For example, when the wafers are silicon and the oxide is formed by thermal oxidation, the oxide is in compressive stress and causes the bonded wafer to warp. Indeed, the device epilayer may be quite thin (1 μm) and the handle wafer of typical wafer thickness (500 μm), so the epilayer-oxide stress can be accommodated by elastic deformation of the epilayer, but the handle-oxide stress will produce warpage. The greater the stress, the greater the warpage. The bonding process produces a compressive oxide on the device wafer as in thermal oxidation. However, even for thicker epilayers (e.g., 15-50 μm thick for high voltage

applications) the handle-oxide stress dominates and warpage may occur.

The wafers cannot be handled by manufacturing equipment such as aligner chucks when the warpage is too large. This causes manufacturing yield loss and limits the maximum bond oxide thickness which can be used. Thus there is a need to reduce the warpage induced by stress in bonded wafer dielectric films.

Features

The present invention provides bonded wafer processing with a stress compensation layer to deter warpage and during processing the stress compensation layer is protected. Other embodiments deter warpage by reduction of stress in the bonding layer within the bonded wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described with reference to the accompanying drawings, which are schematic for clarity:

Figures 1a-d and 2a-c illustrate in cross sectional elevation views known wafer bonding methods and integrated circuits;

Figures 3a-f are cross sectional elevation views of a first preferred embodiment method of warpage control in bonded wafer processing;

Figures 4a-c further illustrate the first preferred embodiment method;

Figures 5a-i are cross sectional elevation views of a fourth preferred embodiment; and

Figures 6 and 7a-e illustrate another preferred embodiment method.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Warpage Control Method

Figures 3a-e illustrate in cross sectional elevation view a first preferred embodiment method of warpage control in bonded wafer processing. The bonded wafer processing proceeds as follow:

(a) Begin with a 4-inch diameter silicon wafer 302 of doping type and resistivity (e.g., N type and 20 ohm-cm resistivity) desired for eventual device fabrication and with standard wafer thickness of about 500 μm as illustrated in Figure 3a. Thermally oxidize wafer 302 to form oxide layers 304 and 306. Oxide 306 will become the bottom oxide, so the oxide is grown to the desired bottom oxide thickness; for example, 4 μm. If a buried layer in the final device structures is desired, then prior to the thermal oxidation of wafer 302, the eventual buried layer would be formed by doping wafer 302 on the face to be oxidized to bottom oxide 306.

(b) Press handle wafer 312 and device wafer 302 together with a drop of oxidizer on the surface of oxide 306 to bond in a furnace cycle with oxidizing ambient which will grow about 2 μm of backside oxide 316 on handle wafer 312. See Figure 3b.

(c) After bonding, remove the bulk of device wafer 302 by grinding, lapping, and polishing to leave the desired device island thickness; for example, 35-40 μm. This thinning of device wafer 302 proceeds without any etchstop, so the final thickness of device wafer 302 depends upon process control. See Figure 3c.

(d) Thermally grow mask oxide 326 on device wafer 302 to a thickness of about 4 μm, thisincreases backside oxide 316 on handle wafer 312 to about 4.5 μm. Mask oxide 326 will be used as a trench etch mask. See Figure 3d.

(e) Print a trench pattern into photoresist spun onto mask oxide 326. Note that the bottom oxide 306 (4 μm),

the mask oxide 326 (4 μm) and the backside oxide 316 (4.5 μm) are all fairly closely matched in thickness during the photoresist patterning. Use the patterned photoresist as etch mask to wet etch (HF) the trench pattern in oxide 326. The wet etch removes 4 μm from backside oxide 316 to leave only 0.5 μm. Then strip the photoresist and use the patterned oxide 326 to plasma reactive ion etch (RIE) device wafer 302 to form silicon islands 322, 323, . . . on bottom oxide 306. See Figure 3e.

(f) Strip patterned oxide 326 with a wet etch. This etch also removes the remaining backside oxide 316 on the back of handle wafer 312. Then thermally grow oxide to a thickness of 4 μm to form isolation oxide 336 on the sides of islands 322, 323, . . . This also forms 4 μm of oxide 338 on the island surfaces and 4 μm of oxide 346 on handle wafer 312. This also thickens the portions of bottom oxide 306 exposed at the trench bottoms. Next, deposit polysilicon 348 to fill the trenches. Lastly, planarize to remove the polysilicon except from the trenches. See Figure 3f. Note that again the island surface oxide 338, bottom oxide 306, and backside oxide 346 all have the same thickness (4 μm).

(g) Fabricate devices in islands 322, 323, . . . with repeated cycles as follows: (1) thermally grow oxide layer, (2) spin on photoresist using a spinner vacuum chuck, (3) pattern the photoresist using an aligner vacuum chuck, (4) wet etch the oxide using the patterned photoresist as etch mask, (5) and diffuse or implant or etch silicon using the patterned oxide as diffusion/implant/etch mask. The patterned oxides may remain from cycle to cycle. Wet etches provide better throughput if line width is not a problem, and thus high voltage processes often use wet etches. However, wet etches attack backside oxide 346, and the thermal growth of oxide does not restore backside oxide 346 as quickly as it is removed due to the parabolic growth rate of thermal oxide. That is, when step (1) grows an oxide of thickness T μm, backside oxide 346 increases in thickness less than T μm; but the wet etch to etch

the grown oxide will remove at least T μm from backside oxide 346. Thus backside oxide 346 would suffer net removal while bottom oxide 306 would not be affected. This would lead to an increasing thickness differential and warpage and processing failure. However, coating the backside with a sacrificial layer which is partially or completely consumed during subsequent manufacturing steps can protect the stress compensation backside oxide 346. A polycrystallyne or amorphous silicon film can be used as a sacrificial layer. Its thickness should be chosen such that the oxidations and etches to which the back of the wafer is subjected do not remove the entire protective layer until the underlying oxide alone can maintain sufficient stress compensation through the remainder of the warpage sensitive part of the manufacturing process. It may be desirable to adjust the thickness of backside oxide 346 so that the net stress of oxide and polysilicon matches that of bottom oxide 306.

An example of the method is a bonded wafer dielectric isolation (DI) process for high voltage ICs. The bottom oxide is 4 μm thick grown by conventional furnace thermal oxidation. The islands are isolated by polysilicon filled lateral trench isolation with oxide separating the poly trench fill from the islands. The stress compensation layer is a 4 μm thermal grown oxide. The protective layer is a 2-3 μm layer of polysilicon. The thickness of polysilicon is chosen such that the sequence of thermal oxidations and subsequent wet (buffered HF) oxide etches performed during wafer processing does not remove the entire polysilicon protective layer. Typically, the processing will include five or six repeated cycles of wet etch openings in frontside oxide with a patterned photoresist mask, introduction of dopants through the oxide openings, and thermal drive-in of the dopants while growing oxide. Such cycles will also grow oxide from the polysilicon during the drive-ins and remove this oxide during the wet etches. Consequently, the polysilicon removal rate can be easily computed.

Wafers with and without the stress compensation plus protection layers are schematically illustrated in Figures 4a and 4b, respectively.

Experimentally, when the thickness difference between bottom oxide 306 and the stress compensation backside oxide 346 is less than about 2 μm for 4 inch starting wafers of thickness about 500 μm, then the warpage can be tolerated by most vacuum chucks used. This implies that backside oxide 346 need not be protected at every possible occurrence of an oxide etch as long as protection is used to insure that the magnitude of the thickness difference remains less than about 2 μm. Indeed, Figure 4c graphically illustrates the warpage (in mils) of a 4-inch bonded wafer with a device layer thickness of about 20 μm and a bottom oxide thickness of 4 μm as a function of the thickness difference. Note that Figure 4c includes both positive and negative thickness differences which correspond to the bottom oxide being thicker and thinner than the backside oxide, respectively. For the positive thickness differences the bonded wafer had convex warpage as in Figure 4a.

With more sensitive vacuum chucks than used so far, the maximum difference would need to be smaller.

Second Warpage Control Method

Protection of the stress compensation backside oxide 346 of the first method can also be achieved by coating the oxide with a layer of material such as silicon nitride which is not removed by processes to which the backside is exposed until all warpage sensitive process steps have been completed. In this case, the oxide 346 thickness may be adjusted so that the combined stress of the oxide and its permanent protective layer (such as nitride) match the stress of the bottom oxide 306. For example, 3000 A of nitride on 3 μm of oxide could be used in place of backside oxide 346. Further, the backside oxide 346 could be completely replaced by nitride, although this would require the oxide and nitride formations be controllable

to produce at least approximately matching stressed layers. The thicknesses of the bottom oxide and a backside nitride could be almost invariant throughout the processing.

Third Warpage Control Method

Another way to protect stress compensation oxide layer 346 of the first method is to coat backside oxide 346 with photoresist prior to a wet etch and remove it after the wet etch. This can protect backside oxide 346 and keep its thickness comparable to that of bottom oxide 306 to prevent warpage. Once devices and interconnections have been formed in islands 322, 323, . . . and other warpage sensitive steps completed, then backside oxide 346 can be removed.

Fourth Warpage Control Method

Figures 5a-i show in cross sectional elevation view a fourth preferred embodiment method of warpage control in bonded wafer processing. The bonded wafer processing proceeds as follow:

(a) Begin with two 4-inch diameter silicon wafers of thickness about 500 μm as illustrated in Figure 5a. Wafer 502 is the device wafer and wafer 504 is the handle wafer. Device wafer 502 has lightly doped device epilayer 510 of thickness about 35 μm and heavily doped etchstop layer 512. Device epilayer 510 has only a native oxide on its surface. Handle wafer 504 has 4 μm thick oxides 520 and 522 on its surfaces; oxide 520 will become the bottom oxide in the final bonded wafer, and oxide 522 will just be a backside oxide. For high voltage products the bottom oxide must be several μm thick. These oxides may be formed simultaneously such as by thermal oxidation in steam. Oxides 520 and 522 have the same compression/tension and thus provide balanced stresses on handle wafer 504 and will deter warpage of the bonded wafer. Indeed, the purpose of backside oxide 522 is warpage deterrence by providing a stress approximately balancing that of bottom

oxide 520. Figure 5a also shows a drop 530 of water plus hydrogen peroxide which are silicon oxidizers.

(b) Press wafers 502 and 504 together. Drop 530 wets the surface of bottom oxide 520 and migrates throughout the contact interface of pressed-together wafers 502-504. The theoretical average thickness of such liquid layer is about 6 μm for a drop of volume 0.05 milliliters (about 4 microliters/square inch). After drying for a day, the pressed-together wafers are heated to about 1150 degrees C for two hours which drives the oxidation of the surface region of device epilayer 510. This oxidation forms silicon-oxygen bonds which effectively extend bottom oxide 520 to device epilayer 510 and thereby fuse wafers 502-504 to form bonded wafer 500. The heating may be performed in an oxidizing ambient and thus grow oxide 506 and thicken oxide 522. However, bottom oxide 520 thickens based on the amount of oxidizer in drop 530 and typically ends up being about 4 μm thick. Ideally, the thicknesses of bottom oxide 520 and backside oxide 522 remain roughly equal. See Figure 5b. Also, the growth of bottom oxide 520 consumes a portion of device epilayer 510. Typically, device epilayer 510 has a final thickness of about 35 μm.

(c) Remove oxide 506 and the bulk of former device wafer 502 by grinding and then etching down to etchstop 512 with KOH and propanol. Then remove etchstop 512 with HF, HNO_3, and acetic acid which preferentially etches the heavily doped etchstop layer 512 and stops on lightly doped device epilayer 510. This leaves bonded wafer 500 as illustrated in Figure 5c.

(d) Form isolation trenches in device epilayer 510 by plasma etching with an oxide etch mask. This proceeds by first forming an oxide coating on device epilayer 510, patterning photoresist on the oxide coating, etching the oxide using the patterned photoresist as etch mask, and then etching device epilayer 510 using the etched oxide as etch mask. Thus,

first thermally oxidize device epilayer 510 to form oxide 514 of thickness 4 μm. This oxidation also increases the thickness of oxide 522 to about 4.5 μm, although the growth is parabolic and not nearly so fast as that of oxide 514 due to the existing thickness of oxide 522. Figure 5d shows bonded wafer 500 after this oxidation.

(e-f) Place bonded wafer 500 on a vacuum chuck and spin on photoresist and harden the photoresist. Then place the photoresist-covered wafer on an aligner vacuum chuck in a projection aligner and expose the photoresist to the trench isolation pattern. If bonded wafer 500 were warped on the magnitude of 5 mils deviation from flat at the center, then a vacuum chuck may be unable to hold the wafer down and the photoresist application or patterning may be impossible to perform. However, for bonded wafer 500 the thickness of bottom oxide 520 differs from the thickness of backside oxide 522 by only about 0.5 μm, and this keeps the warpage of bonded wafer 500 within tolerable limits. Oxides 520 and 522 are both compressive and under similar stress, then bottom oxide 520 being thicker than backside oxide 522 implies a warpage as shown (exaggerated) in Figure 5e. Figure 5e also heuristically indicates vacuum chuck 550 and the direction of vacuum pull. Conversely, if bottom oxide 520 were thinner than backside oxide 522, then the warpage would be as shown in Figure 5f. Because a vacuum chuck pulls at the center of a wafer, warpage as in Figure 5e can be more easily tolerated than that shown in Figure 5f.

(g) After photoresist exposure, develop the photoresist and bake. Then use the patterned photoresist to wet etch oxide layer 514. This wet etch also attacks backside oxide 522 and thins it. An overetch of oxide 514 (thickness 4 μm) removes at least 4 μm of backside oxide 522. However, this removal of backside oxide 522 is prevented by spinning photoresist onto backside oxide 522 just prior to the wet etch. This extra photoresist protects the backside oxide during the

wet etch. After the wet etch, remove the backside photoresist along with the patterned photoresist on oxide 514. See Figure 5g.

(h) Plasma etch trenches in device epilayer 510 using patterned oxide 514 as the etch mask. The trenches extend down into bottom oxide 520 and leave device epilayer 510 in the form of islands 511 of silicon on bottom oxide 520. Next, form oxide on the sidewalls of the trenches by thermal oxide growth to a thickness of about 4 μm; this a lateral isolation oxide formation. The oxidation also increases the thickness of the oxide 514 already on the tops of islands 511 plus thickens backside oxide 522. Then fill the trenches by deposition of polysilicon. One may use either LPCVD or epitaxial deposition; LPCVD covers both front and back of bonded wafer 500. Then planarize with a chemical and mechanical polish back which stops on oxide. See Figure 5h.

(i) Fabricate devices in islands 511 with repeated cycles as follows: (1) thermally grow oxide layer, (2) spin on photoresist using spinner vacuum chuck, (3) pattern the photoresist using an aligner vacuum chuck, (4) wet etch the oxide using the patterned photoresist as etch mask, (5) and diffuse or implant or etch silicon using the patterned oxide as diffusion/implant/etch mask. The patterned oxides may remain from cycle to cycle. As previously noted, wet etches attack backside oxide 522, and the thermal growth of oxide does not restore backside oxide 522 as quickly as it is removed due to the parabolic growth rate of thermal oxide. Thus backside oxide 522 would suffer net removal while bottom oxide 520 would not be affected; and this would lead to a thickness differential and warpage and processing failure. However, coating backside oxide 522 with photoresist 552 prior to a wet etch and removal after the wet etch can protect backside oxide 522 and keep its thickness comparable to that of bottom oxide 520 to prevent warpage. See Figure 5i. Once devices and interconnections have been formed in islands 511 and other

warpage sensitive steps completed, then the backside oxide 522 can be removed.

Differential Stresses

It may be desirable to have the stresses of the bottom oxide and the backside oxide not quite equal so that the net residual stress causes a small warpage which is always in the same direction. As an example, one might want the center of the bottom to be above the circumference so that the perimeter of the wafer back makes first contact with wafer chucks thereby providing good sealing action when vacuum is applied. Figure 5e illustrates this situation.

Unprotected Stress Compensation Layer

In some cases, the stress compensation layer can be used without protection. This occurs when the thickness removed in subsequent process steps is small enough that the remaining part of the stress compensation layer keeps warpage within acceptable limits during all warpage sensitive processing steps. Thus in any of the methods the protection could be foregone in all steps following some cutoff step.

Bottom Oxide Breakup

Warpage in bonded wafers may also be reduced by breaking up the sheet of bottom oxide which extends across the entire surface of the handle wafer. When broken up in small areas, the stress is reduced because there is less stressed oxide present and the oxide that is present may relax by expanding into the edges of non-oxide areas.

The bottom oxide can be broken up by removing it from the bottoms of the areas taken up by lateral trench isolation as shown in Figure 6. Alternatively, or as an additional area of bottom oxide removal, the bottom oxide can be removed from the areas surrounding each circuit which are provided as areas

to be cut (scribed or sawed) to separate the circuits from one another when wafer processing is complete.

The bottom oxide can be patterned using the following process sequence. Oxide is formed on the wafer to be laterally isolated after it has been thinned and otherwise processed into final form. The oxide is patterned and used as a silicon trench etch mask. The silicon is etched preferably by reactive ion etching to form trenches with nearly vertical side walls. The silicon etch preferably undercuts the oxide so that the oxide mask overhangs the sides of the trenches. Oxide and or other insulator is formed on the sides (and optionally the bottom) of the trenches by thermal oxidation and or conformal oxide deposition by chemical vapor deposition.

Finally the bottom oxide is removed by reactive ion etching with the side oxide being protected by the top oxide overhang (if present) and by the fact that the side walls are nearly vertical and the reactive ion etch process attacks horizontal surfaces only due to the direction of ion motion (vertical). This is somewhat similar to forming oxide spacers on the sides of polysilicon gates. The process sequence is illustrated in Figures 7a-e. Of course, the mask oxide must be thicker than the bottom oxide to be an effective mask.

Wafer Size

The stress in an oxide (or other material) layer on a silicon (or other material) wafer is proportional to layer thickness, thus a thicker layer will lead to more warpage. Conversely, a thicker wafer will have greater strength against bending and lead to less warpage for the same layer stress. Now, increasing wafer diameters leads to increasing wafer thicknesses for handling reasons, so 6 inch wafers will likely show less warpage than 4 inch wafers with similar stress layers. Also, the vacuum chucks for 6 inch wafers will exert much greater pull on the wafer than will the chuck for a 4 inch wafer because the pull is proportional to the area of the

vacuum chuck. Indeed, the force is proportional to the chuck area times atmospheric pressure assuming that the chuck can reduce pressure under the wafer to a small fraction of atmospheric pressure. This will also make 6 inch wafers likely easier to handle than 4 inch wafers. Note that the uniform stress of a layer on a wafer leads to a constant curvature warpage, so with the same wafer strength and same layer stress, and thus the same warpage curvature, a larger wafer will have a greater center deflection due to its larger size. The deflection will depend approximately quadratically on wafer diameter for small deflections.

Modifications and Variations

The preferred embodiment methods may be varied in many ways while retaining one or more of the features of bonded wafer processing with stress compensation backside layer during processing or with breakup of the bottom oxide for warpage control. For example, the bottom oxide could vary from 2 μm to 6 μm in thickness and accommodate devices operating up to 1000 volts. Similarly, the thickness of the silicon islands could vary from 10 μm to 60 μm for junction breakdown voltages of 100 to 1000 volts, although alternative approaches could provide high breakdown voltages with islands as thin as 1 μm. The original bottom oxide could have initially been partially on both the device wafer and the handle wafer if a different bonding process were used. The backside oxide for stress compensation could be formed after the bonding of the two wafers. Other materials could be used, such as bonding gallium arsenide to silicon.

CLAIMS

What is claimed is:

1. A method of bonded wafer processing, comprising the steps of:

(a) providing a bonded wafer with a stress compensation layer; and

(b) protecting said layer during a processing step applied to said wafer, wherein said processing step would affect the stress of said layer.

2. The method of claim 1, wherein:

(a) said wafer includes silicon bonded to silicon by silicon oxide; and

(b) said layer includes silicon oxide.

3. The method of claim 1, wherein:

(a) said step of protecting includes applying photoresist to said layer.

4. The method of claim 1, wherein:

(a) said step of protecting includes applying silicon nitride to said layer.

5. The method of claim 1, wherein:

(a) said step of protecting includes applying polysilicon to said layer.

6. The method of claim 1, wherein:

(a) said step of protecting includes applying a material to said layer and retaining said material on said layer through a plurality of processing steps applied to said wafer.

7. The method of claim 6, wherein:

(a) said material is partially removed by said processing steps.

8. The method of claim 7, wherein;

(a) said material is polysilicon.

9. A method of bonded wafer processing, comprising the steps of:

(a) providing a bonded wafer;

(b) accessing a bonding layer within said bonded wafer;

(c) reducing stress in said accessed bonding layer by removal of a portion of said bonding layer; and then

(d) applying processing steps to said wafer.

10. The method of claim 9, wherein:

(a) said bonded wafer includes silicon oxide bonding silicon to silicon; and

(b) said bonding layer includes silicon oxide.

11. The method of claim 9, wherein:

(a) said accessing is part of formation of an isolation structure in said bonded wafer.

12. A method of bonded wafer processing, comprising the steps of:

(a) providing a silicon bonded wafer with a silicon oxide bonding layer and a silicon oxide stress compensation layer, said bonding layer of thickness at least about 4 μm; and

(b) maintaining the thickness of said compensation layer to within 2 μm of the thickness of said bonding layer during a plurality of processing steps applied to said wafer.

13. The method of claim 12, wherein:

(a) said maintaining includes formation of a polysilicon layer on said compensation layer.

14. The method of claim 13, wherein:

(a) said polysilicon layer has a thickness greater than the thickness of silicon removed by said plurality of processing steps.

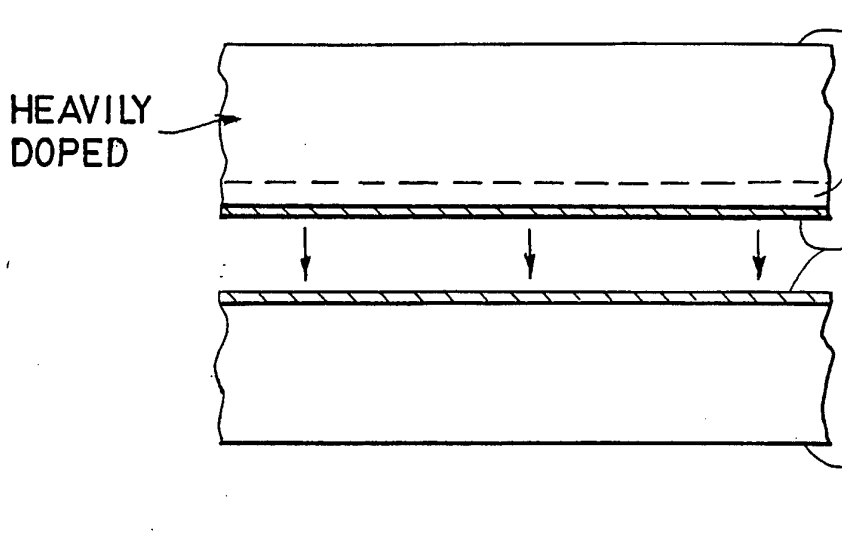


FIG.1a
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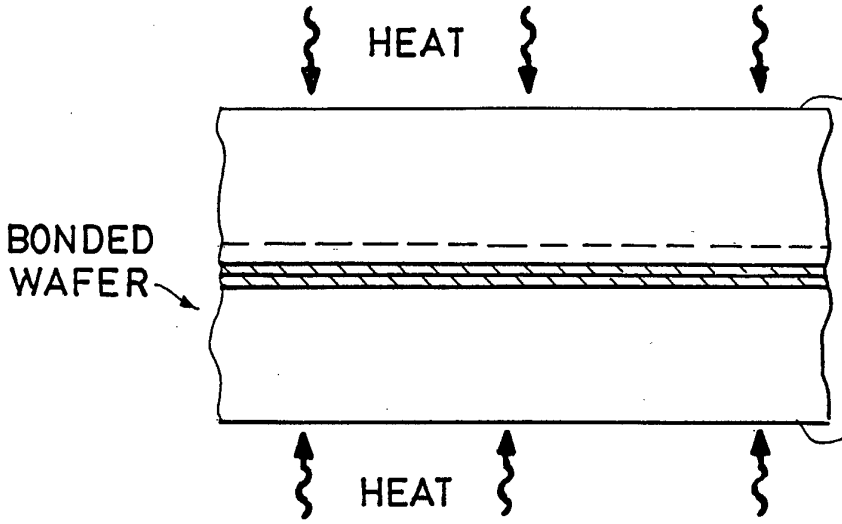


FIG.1b
PRIOR ART

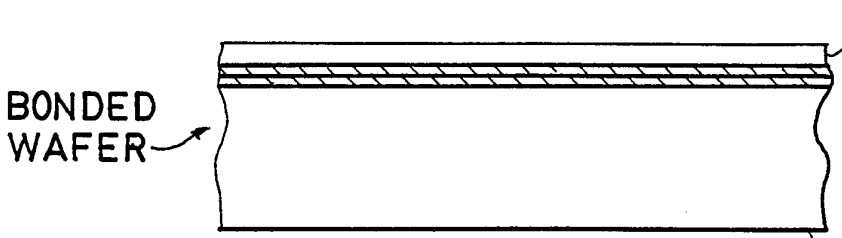


FIG.1c
PRIOR ART

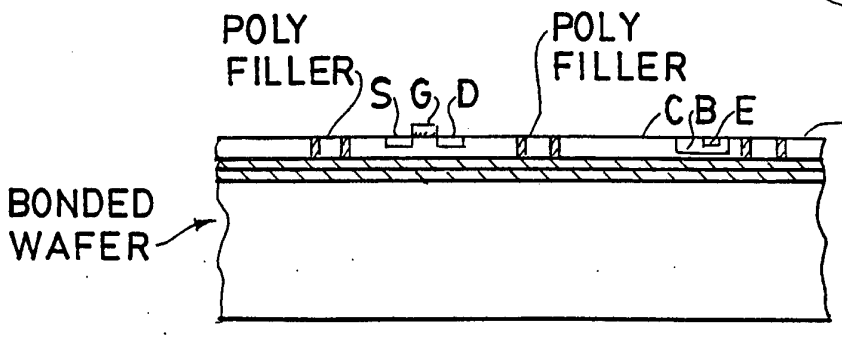


FIG.1d
PRIOR ART

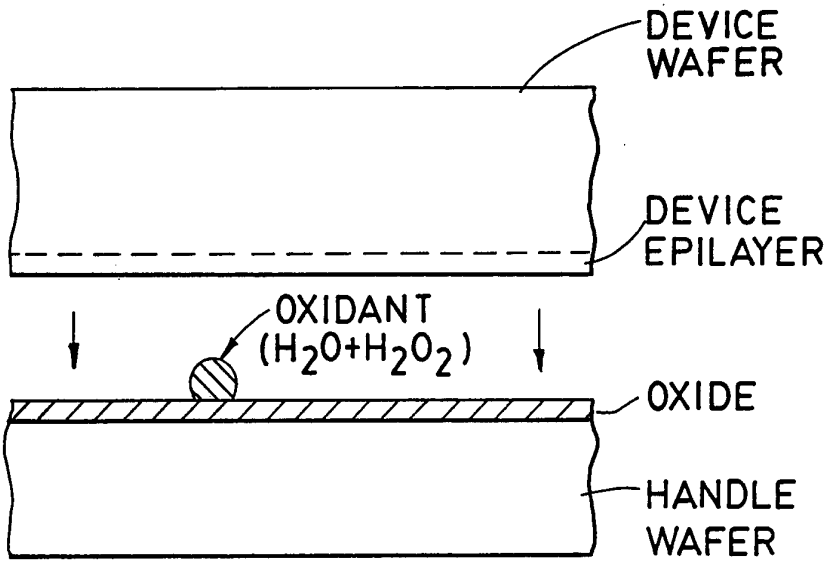


FIG. 2a

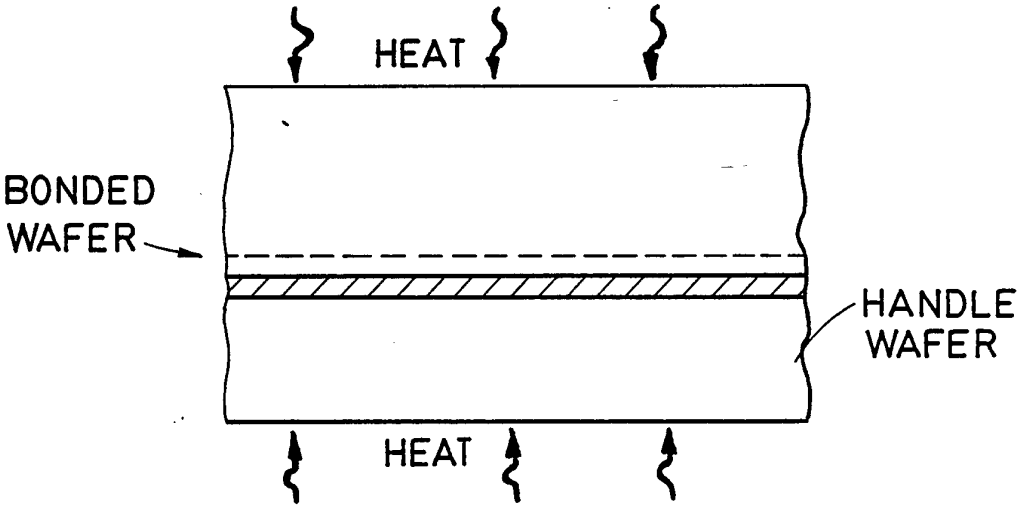


FIG. 2b

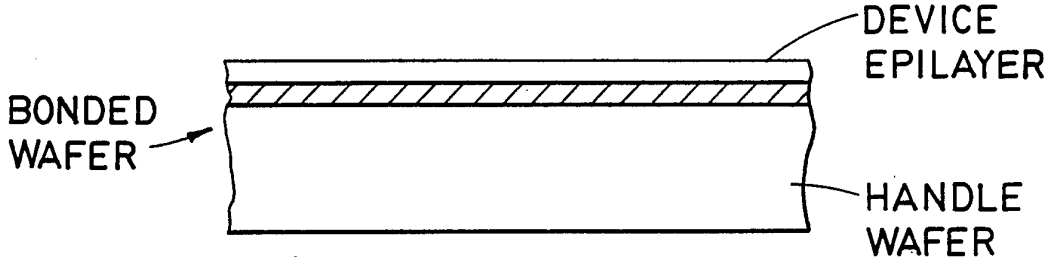
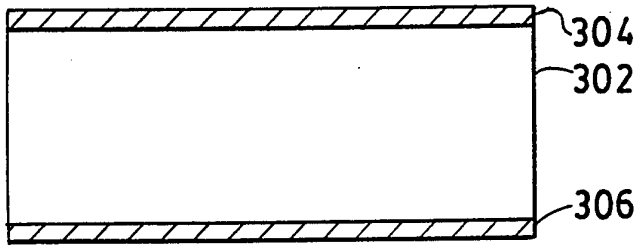
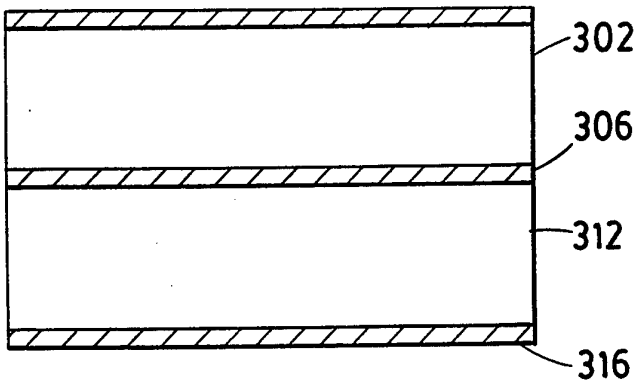


FIG. 2c



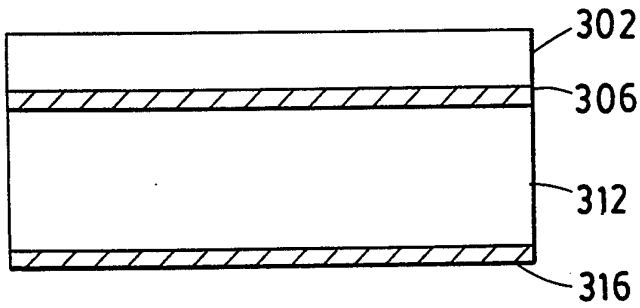
OXIDIZE WAFER

FIG. 3a



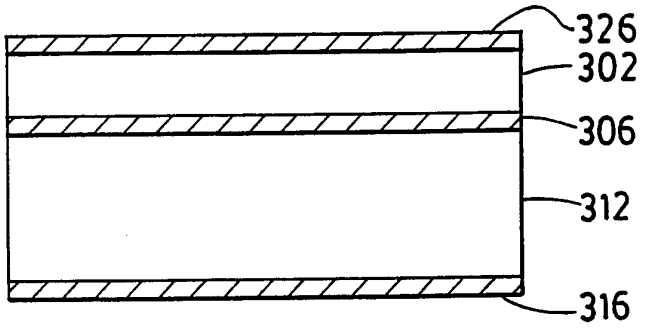
BOND DEVICE WAFER
TO HANDLE WAFER

FIG. 3b



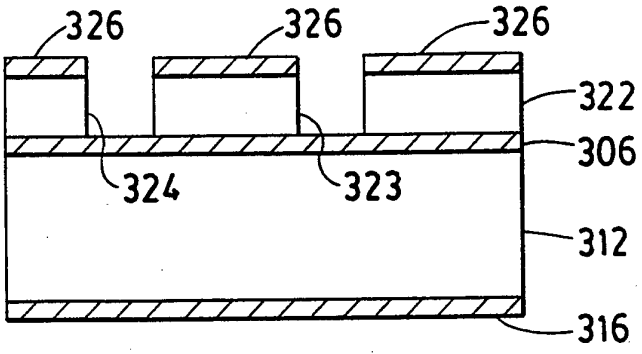
THIN DEVICE WAFER

FIG. 3c



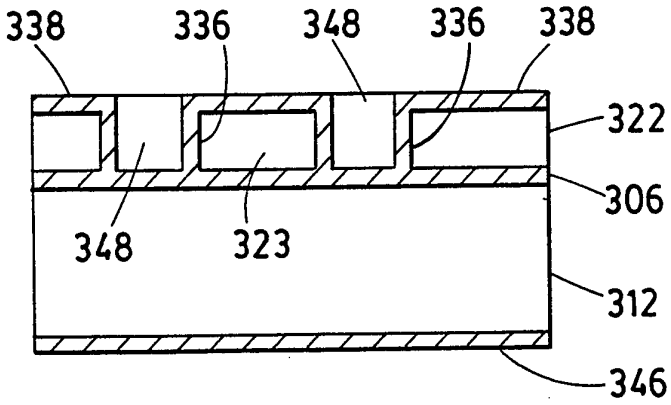
TRENCH MASK OXIDE

FIG. 3d



TRENCH PR
AND ETCH

FIG. 3e



SIDE+TOP OXIDE,
TRENCH FILL (POLY)
AND PLANARIZATION

FIG. 3f

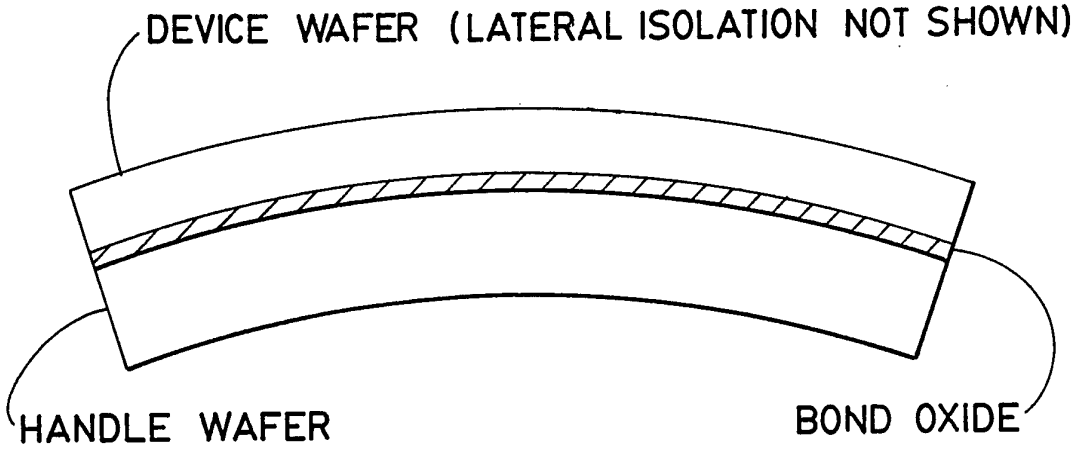

DEVICE WAFER (LATERAL ISOLATION NOT SHOWN)
HANDLE WAFER
BOND OXIDE

FIG. 4a

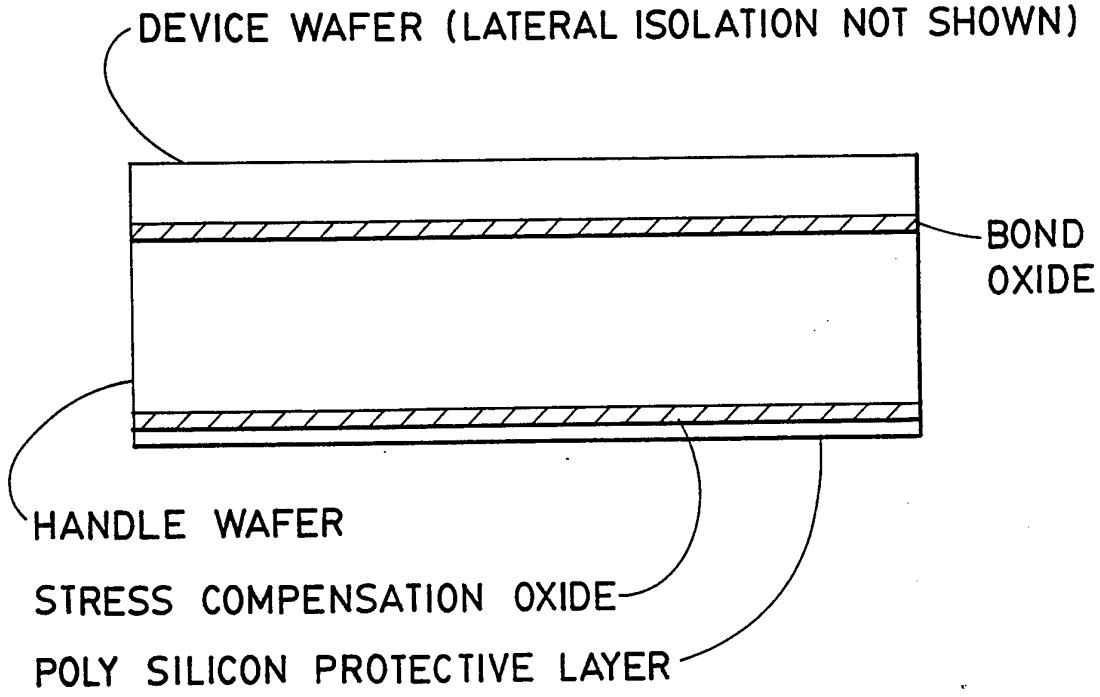

DEVICE WAFER (LATERAL ISOLATION NOT SHOWN)
BOND OXIDE
HANDLE WAFER
STRESS COMPENSATION OXIDE
POLY SILICON PROTECTIVE LAYER

FIG. 4b

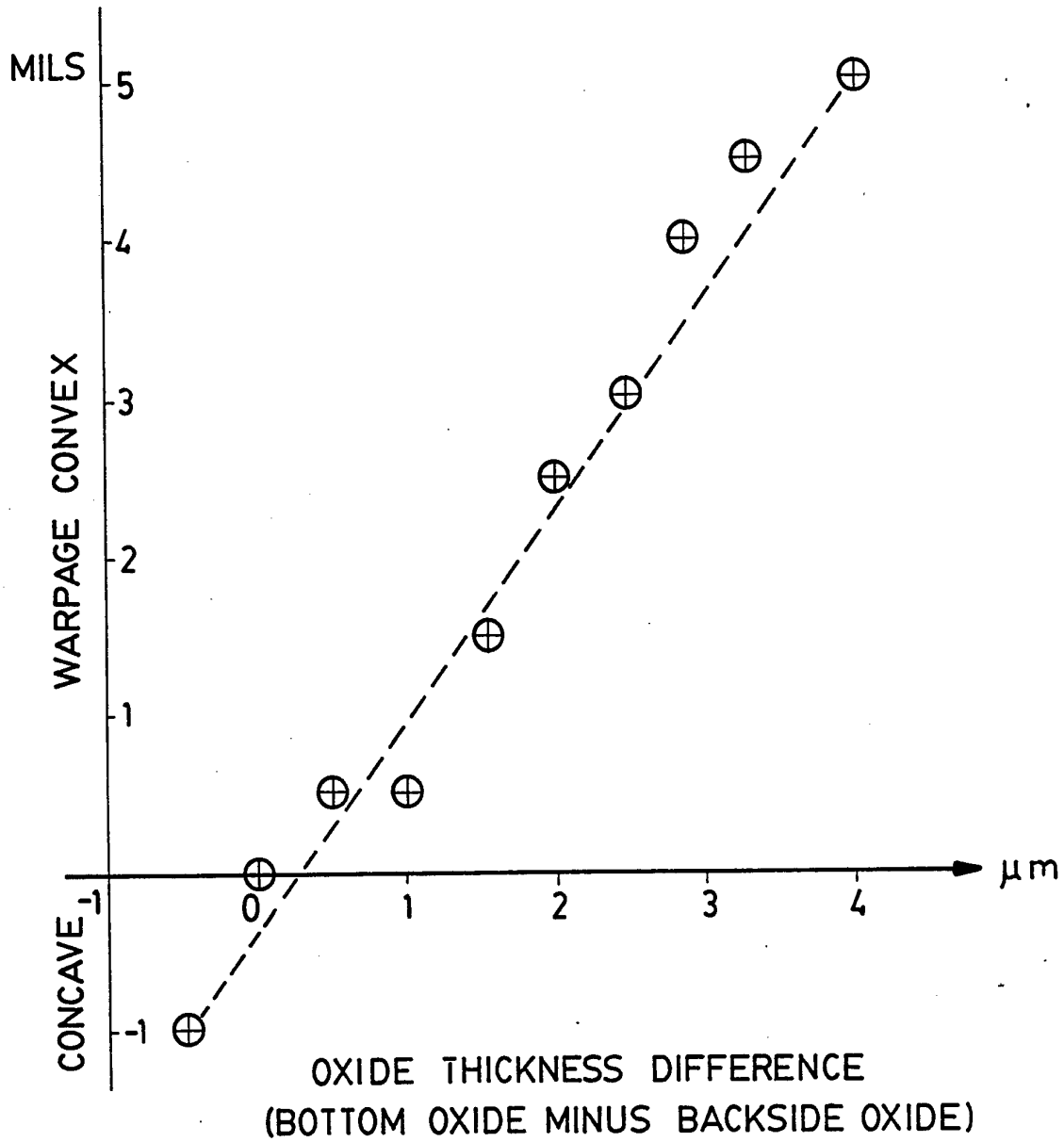

MILS
5
4
3
2
1
-1
WARPAGE CONVEX
CONCAVE
-1
0
1
2
3
4
μm
OXIDE THICKNESS DIFFERENCE
(BOTTOM OXIDE MINUS BACKSIDE OXIDE)

FIG 4c

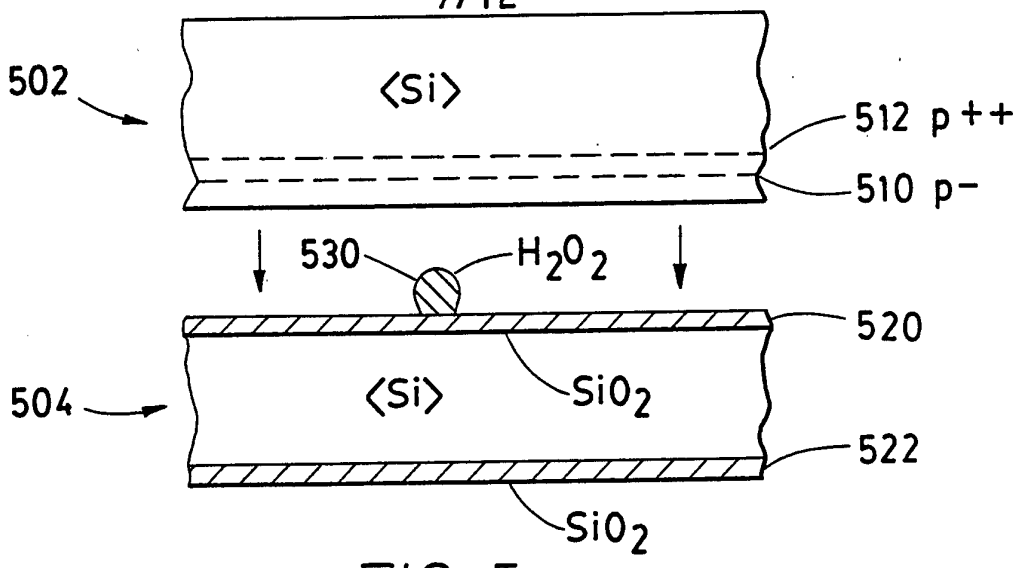


FIG. 5a

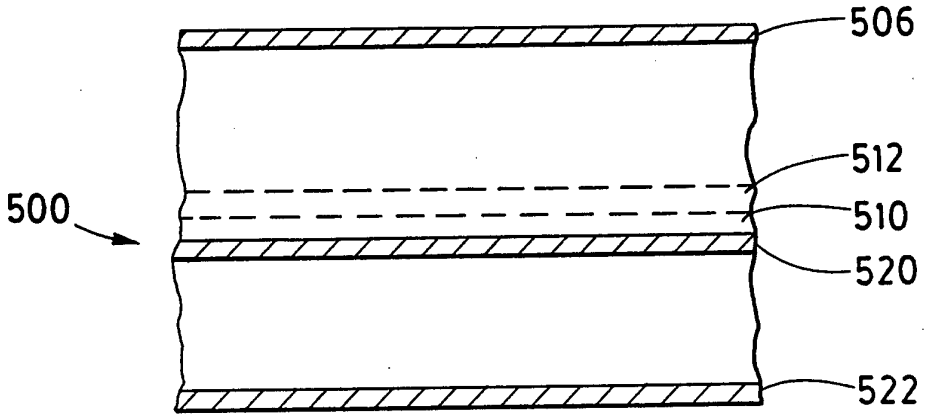


FIG. 5b

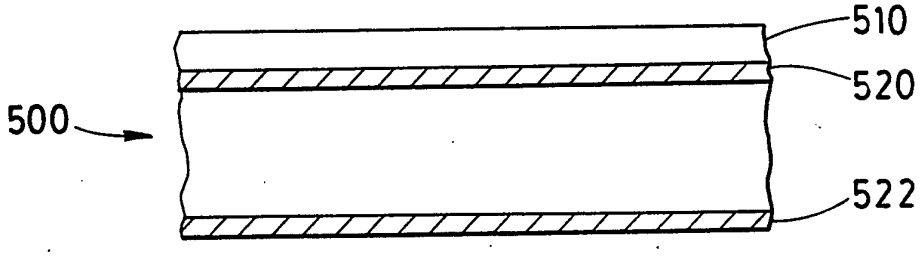


FIG. 5c

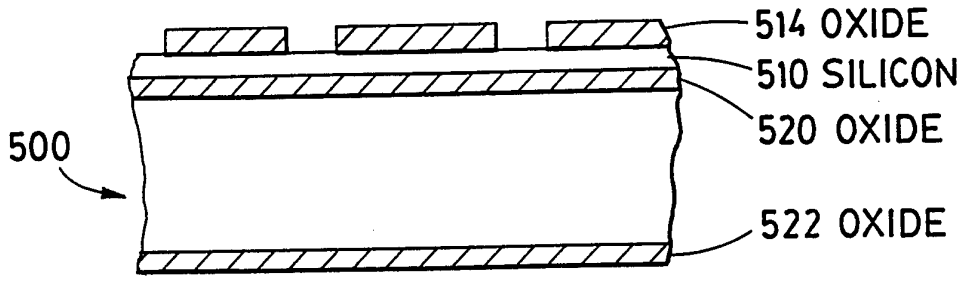


FIG. 5g

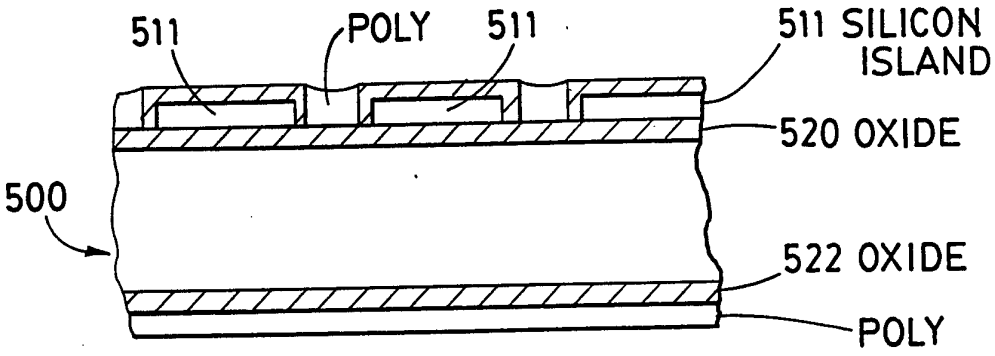


FIG. 5h

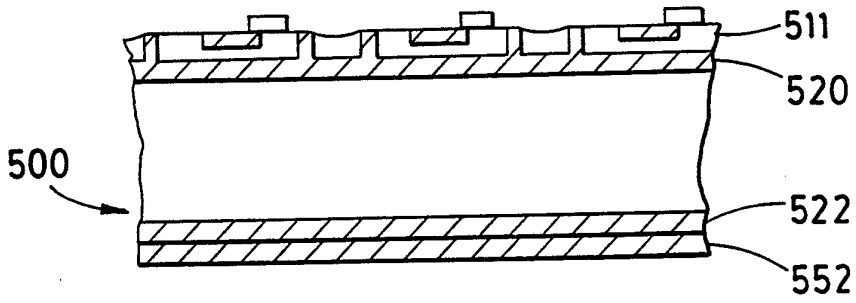


FIG. 5i

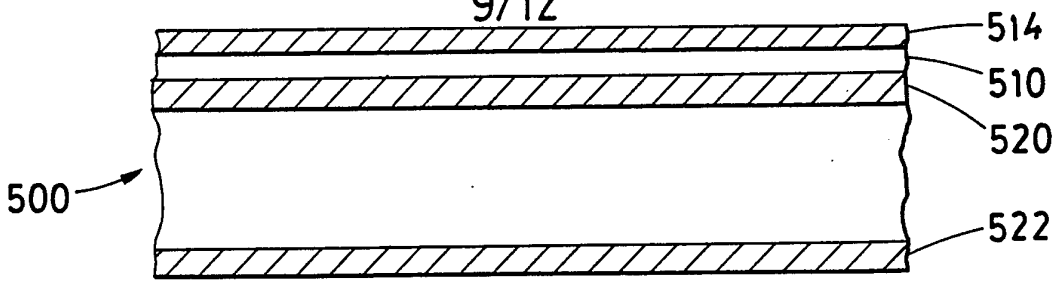


FIG. 5d

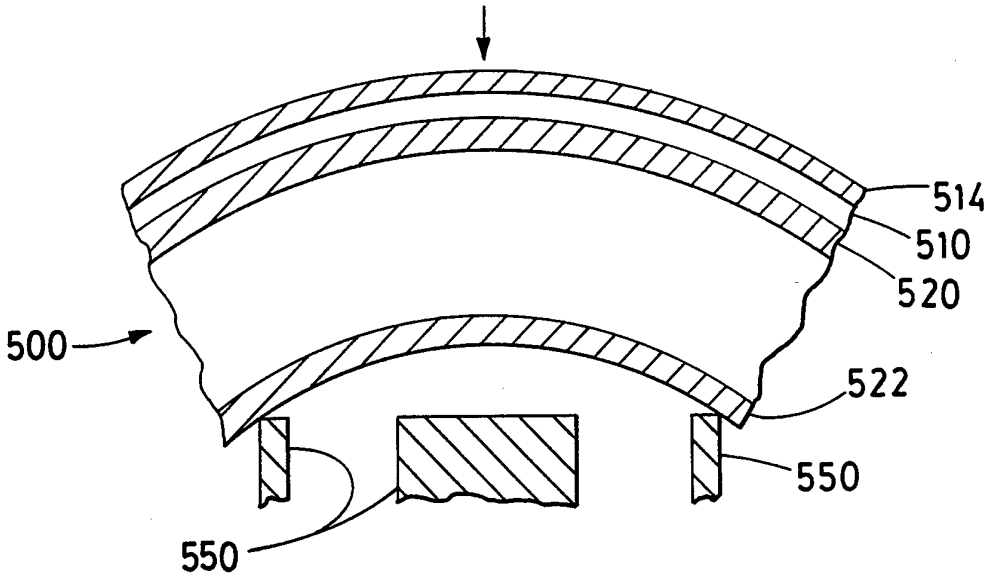


FIG. 5e

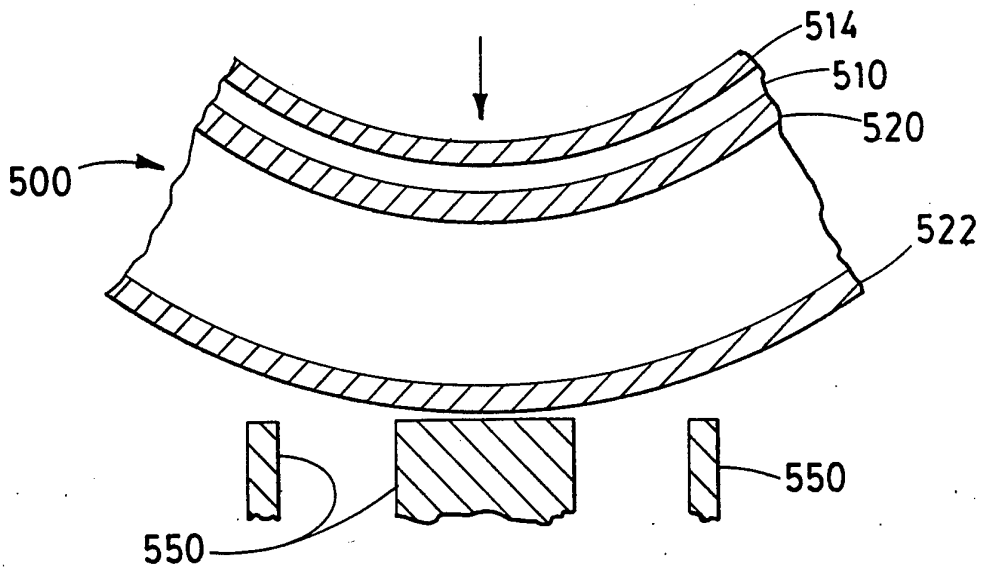


FIG. 5f

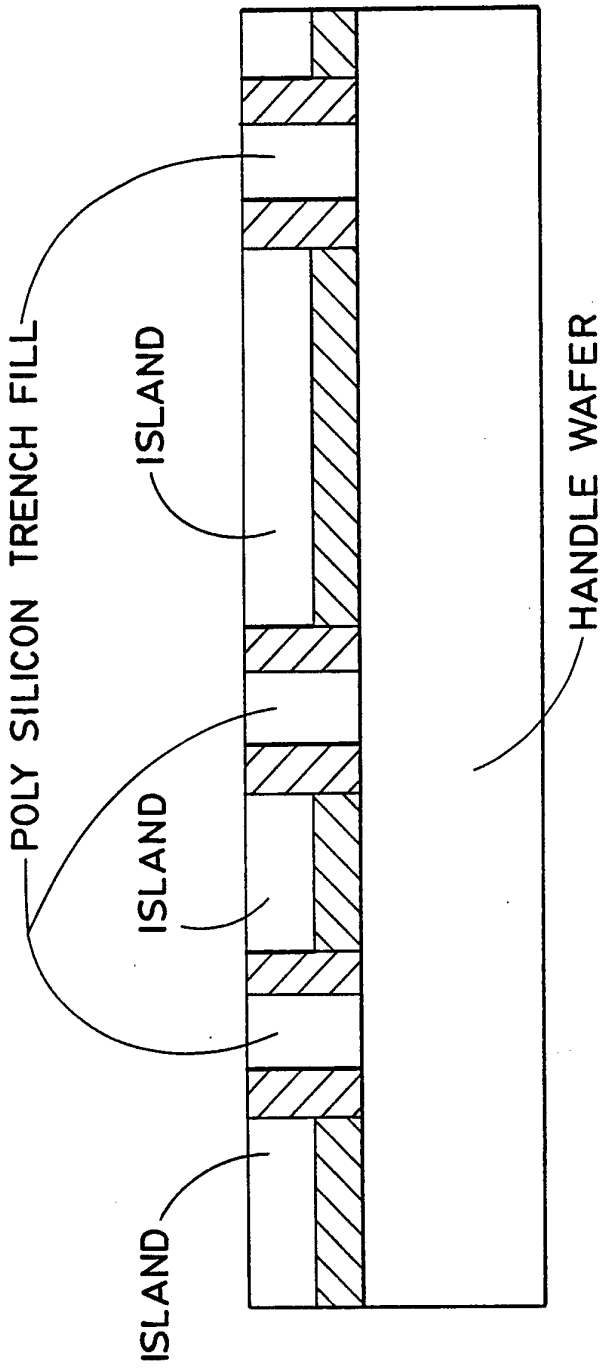
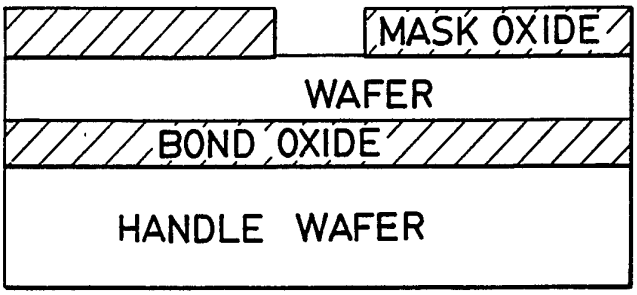
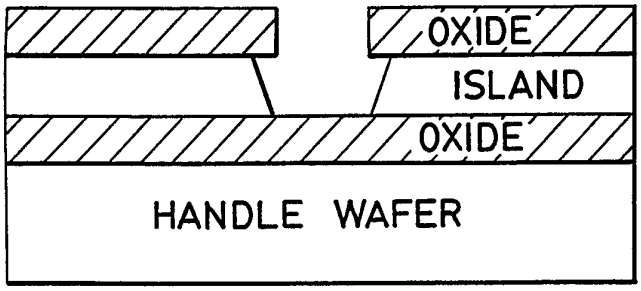

POLY SILICON TRENCH FILL
ISLAND
ISLAND
ISLAND
HANDLE WAFER
= BOND OXIDE
= LATERAL ISOLATION OXIDE

FIG. 6



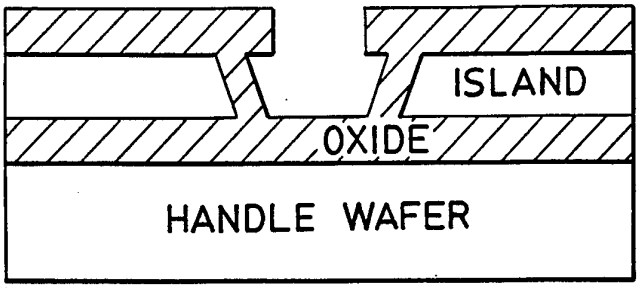
AFTER MASK OXIDE ETCH

FIG. 7a



AFTER RIE SILICON TRENCH ETCH

FIG. 7b



AFTER LATERAL ISOLATION OXIDE FORMATION

FIG. 7c

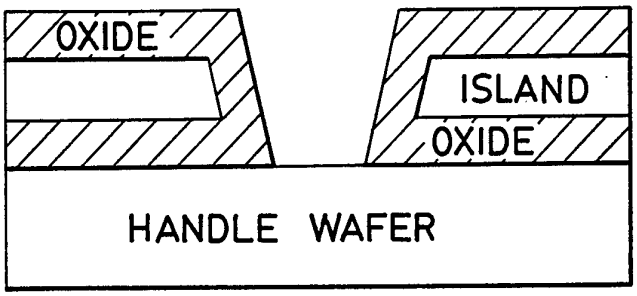

OXIDE
ISLAND
OXIDE
HANDLE WAFER
AFTER RIE
BOTTOM OXIDE
ETCH

FIG. 7d

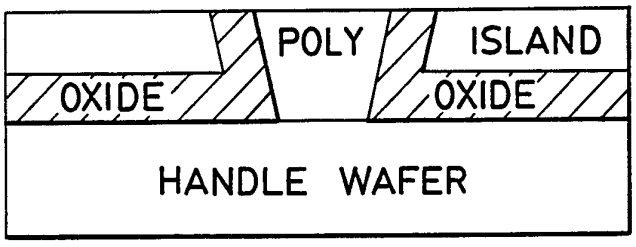

POLY
ISLAND
OXIDE
OXIDE
HANDLE WAFER
AFTER POLY TRENCH
FILL AND
PLANARIZATION

FIG. 7e

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 93/05828

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H01L21/76; H01L21/20

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H01L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category °	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
X	EP,A,0 469 583 (TOSHIBA K.K.) 5 February 1992 see column 2, line 5 - column 3, line 13; claims 12-19; figures 1A-1F,7 ---	9-11
X	PATENT ABSTRACTS OF JAPAN vol. 014, no. 099 (E-0893)22 February 1990 & JP,A,13 02 740 (TOSHIBA K.K.) 6 December 1989 see abstract ---	1,2,5-8
X	EP,A,0 464 837 (TOSHIBA K.K.) 8 January 1992 see column 8, line 18 - column 9, line 15; claims 1,5-8; figures 4,6,8	1-3,6,7
A	see column 4, line 45 - column 5, line 34 --- -/--	12

° Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
07 OCTOBER 1993	18. 10. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	VANCRAEYNEST F.H.

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 007, no. 013 (E-153)19 January 1983 & JP,A,57 170 539 (FUJITSU LTD) 20 October 1982 see abstract	1,4
A	EP,A,0 444 943 (SHIN-ETSU HANDOTAI CY) 4 September 1991 see column 5, line 33 - column 6, line 33	12
A	IEEE TRANSACTIONS ON ELECTRON DEVICES vol. 38, no. 7, July 1991, NEW YORK US pages 1650 - 1654 A. NAKAGAWA ET AL. 'BREAKDOWN VOLTAGE ENHANCEMENT FOR DEVICES ON THIN SILICON LAYER/SILICON DIOXIDE FILM' see page 1652, column 1, paragraph 5 - column 2, paragraph 2; figures 1,7	12

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO.

US 9305828
SA 76069

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 05/10/93

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0469583	05-02-92	JP-A- 4088657	23-03-92
EP-A-0464837	08-01-92	JP-A- 4065126	02-03-92
EP-A-0444943	04-09-91	JP-A- 3250615	08-11-91
		JP-A- 3250617	08-11-91