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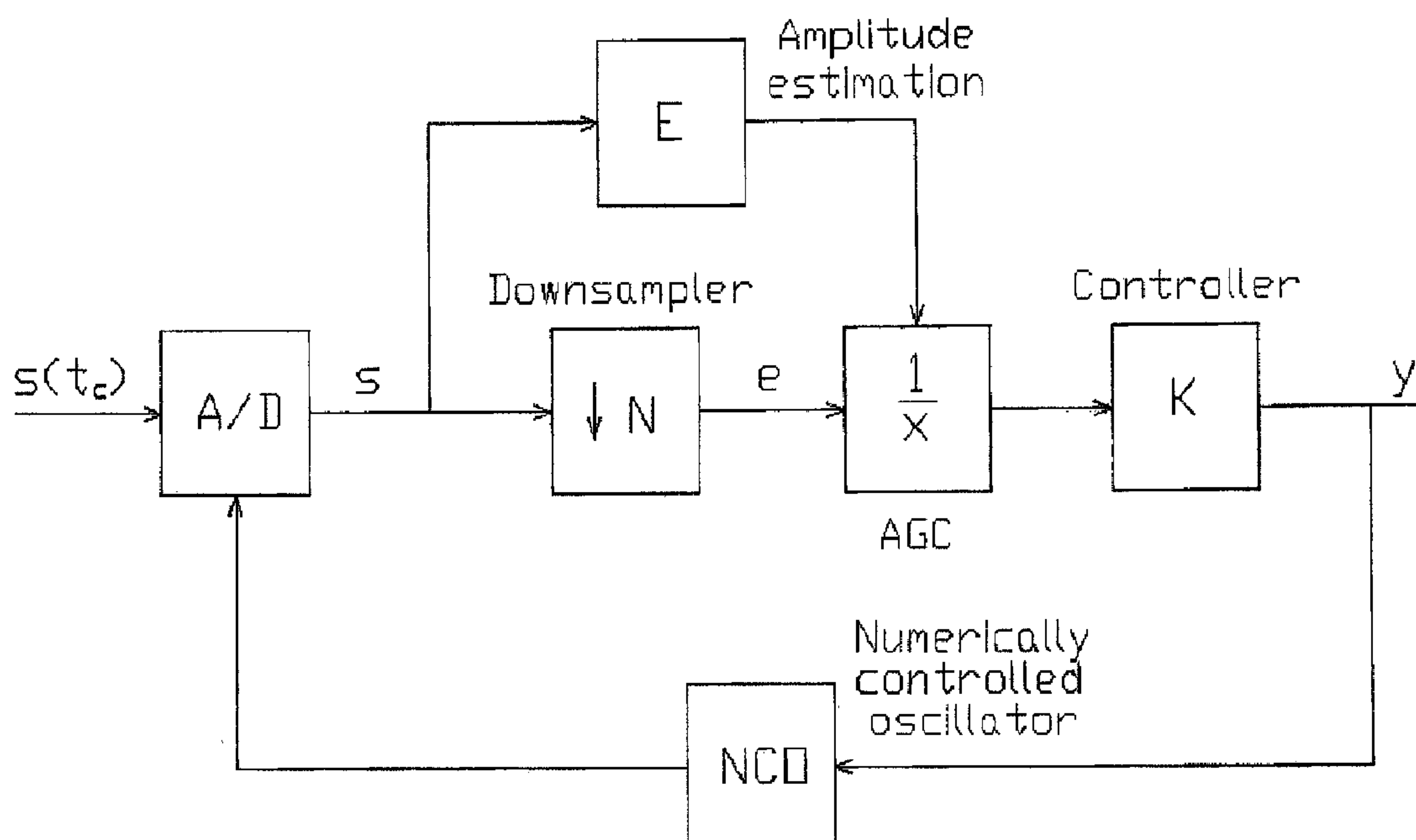
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(54) Titre : BOUCLE NUMERIQUE DE VERROUILLAGE DE PHASE A TAUX MULTIPLES PERMETTANT LA
SYNCHRONISATION SUR DES SIGNAUX PERTURBES

(54) Title: MULTIRATE DIGITAL PHASE-LOCKED LOOP FOR SYNCHRONIZATION TO DISTURBED SIGNALS



PLL with Automatic Gain Control (AGC)

(57) Abrégé/Abstract:

This invention relates to a method and system for synchronization in applications where the synchronization signal is severely disturbed and where the signal frequency and amplitude are variable. The system is based on a multirate phase-locked loop (PLL). With respect to the operation of the system, blocks in the proposed system operate at different sample rates and the sample rates are variable. The system sample rates are a multiple of the fundamental frequency of the input signal and they are forced to vary synchronously with the fundamental frequency through the system feedback action.

ABSTRACT

This invention relates to a method and system for synchronization in applications where the synchronization signal is severely disturbed and where the signal frequency and amplitude are variable. The system is based on a multirate phase-locked loop (PLL).

- 5 With respect to the operation of the system, blocks in the proposed system operate at different sample rates and the sample rates are variable. The system sample rates are a multiple of the fundamental frequency of the input signal and they are forced to vary synchronously with the fundamental frequency through the system feedback action.

MULTIRATE DIGITAL PHASE-LOCKED LOOP FOR SYNCHRONIZATION TO DISTURBED SIGNALS

FIELD OF THE INVENTION

This invention relates to a method and system for real time synchronization to disturbed utility network signals using a multi-rate digital zero crossing sampling phase-locked loop. The expression 'synchronization to disturbed signals' stands for the synchronization to the fundamental harmonic of the disturbed signal. More specifically, this invention relates to a robust digital multi-rate phase locked loop that provides synchronous sampling of the input signal at a multiple of the input signal frequency.

10 BACKGROUND

Stand-alone equipment such as relays, meters and static power converters mainly utilize the fundamental component of power system signals. All of these applications usually require some type of signal processing associated with network signals.

The increasing use of nonlinear loads and devices has resulted in an increased level of disturbances injected into the power system. These disturbances cause several problems for metering, control and protective devices. Such problems include measurement errors, control system instability or relay misoperation.

The needs for phase synchronization in power electronics and power engineering applications are numerous. Typical examples are: synchronization of inverters to an AC utility network, control of parallel connected inverters, synchronization of active filters, synchronization of line-commutated phase-controlled converters, synchronized signal processing, etc. In applications where the noise level of the signal is low, phase synchronization can be realized by using an ordinary analog or digital phase-locked loop (PLL). The PLL is one part of the synchronization system. A particular type of digital PLL known as the zero crossing sampling phase-locked loop (ZC-PLL) has the known advantages that implementation, modelling and analysis of this type of PLL are easier than for other types of digital PLLs. In cases where the input signal is corrupted with strong disturbances, performance of an ordinary PLL may be unsatisfactory. The

PLL output signal can contain jitter or it even may happen that the PLL cannot track the input signal at all.

Earlier approaches using adaptive filtering to the problem of detecting zero-crossings of disturbed signals are known. In an adaptive filtering based approach, the question of the system design and the system dynamics is solved in a basically trial and error manner. As a result the corresponding design process can be difficult and uncertain.

SUMMARY OF THE INVENTION

To help overcome the deficiencies of the prior art we introduce a synchronization method based on a multirate digital PLL, where the system blocks operate at two different sample rates. One sample rate is much higher than the input signal (carrier) frequency and is referred to as the fast sample rate (frequency). The other sample rate is equal to (or double) the carrier frequency and is referred to as the slow sample rate. The input signal is sampled at the fast sample rate in order to alleviate the implementation of the antialiasing filter and enable synchronization to disturbed signals. Other system blocks (apart from the antialiasing filter and possibly an amplitude estimation and a gain control block) are implemented using the slow sample rate, which reduces the overall computational burden of the system.

An advantage of the proposed approach is that it enables phase synchronization to signals containing a high level of disturbances. The antialiasing filter automatically adapts to the input signal frequency through the system's variable sample rate operation. The system's control aspects are derived from a transfer function model. According to the invention, an all digital system can be implemented to track realistic signals such as a sinusoidal signal containing notch type disturbance and noise and an arc furnace voltage signal. The system can be implemented using any available method for implementation of digital systems. For example, the proposed system can be implemented using a digital signal processor, field programmable gate array (FPGA), an application specific integrated circuit (ASIC) or a system on a chip architecture (SoC).

It is an objective of this invention to provide means for digital tracking of disturbed signals under conditions where the signal frequency and amplitude are variable. The proposed system enables the tracking of signals contaminated with a wide class of

disturbances. Some examples of disturbances are: random noise, notch type disturbances, an electric arc disturbances etc. The signal supposed to be tracked is typically an ac signal associated with a power engineering or power electronics application.

5 Further objectives of the invention are to:

- i) enable an all digital implementation of the system;
- ii) offer a better rejection of signal disturbances compared to the adaptive filtering based approach;
- iii) enable an easier and more flexible system design; and
- 10 iv) enable the design of all system blocks in a straight forward manner according to a well formulated design procedure.

A zero crossing sampling phase-locked loop (PLL) digital signal processing unit using an integer or rational valued oversampling rate is designed as a building block for a phase synchronization system. On the basis of models derived herein, two different system
 15 controllers are designed and the system transient response for the two cases is compared. The first controller is of a proportional-integral (PI) type and the second controller is the minimum response time (MRT) controller. The MRT controller is also known as a finite settling time controller or deadbeat controller. While it is generally known that the PI controller is robust and simple to implement and MRT controller gives
 20 the fastest system response, the present invention discloses means to design and implement these controllers in the context of the multirate PLL.

The functionality of the digital signal processing system is implemented in a preferred embodiment on AC utility network signals containing a high level of disturbances. The system is based on a multirate digital phase-locked loop (PLL). The main advantages of
 25 the multirate approach are that it simultaneously simplifies the implementation of the anti-aliasing filter while enabling the system to accommodate input signals of varying amplitude. The antialiasing filter, in the proposed system, is implemented as a high order bandpass filter. The anti-aliasing filter automatically adapts to the input signal frequency through the system's variable sample rate operation. The system's control aspects are
 30 derived from a transfer function model. According to the invention, an all digital system is

implemented to track realistic signals such as a sinusoidal signal containing notch type disturbance and noise and an arc furnace voltage signal.

The purpose is to track frequency changes in the fundamental frequency of an input signal in the presence of background noise or other disturbances to amplitude or phase.

- 5 An analog to digital converter samples an input signal at a fast sample rate. In the steady-state, the fast sample rate is a multiple (integer or rational) of the fundamental frequency of the input signal. The resulting digital sequence is fed to a digital bandpass filter and an amplitude estimation block. The digital bandpass filter has a centre frequency equal to the fundamental frequency of the input signal in the steady-state.
- 10 The amplitude estimation block may operate at any rate between the fast sample rate and the slow sample rate to determine a scaling factor for the digital bandpass filter output.

- The bandpass filter output signal is downsampled and scaled and the resulting signal, which represents the PLL error signal, is fed to the system controller. The
- 15 downsampling and scaling may occur at any point between the digital bandpass filter and the controller, but for efficiency of computation, the downsampling is performed before scaling, so that scaling can be performed at the slow sample rate as well. In the case where the phase-locked loop algorithm is based only on positive or negative going zero crossings of the signal, the slow sample rate is equal to the fundamental frequency
- 20 of the input signal. In the case where the PLL algorithm is based on both positive and negative going zero crossings, the slow sample rate is equal to two times the fundamental frequency of the input signal. In the steady-state, the error sequence is zero because the downsampling occurs exactly at the zero crossings of the input signal. The output of the system controller determines frequency of the numerically controlled
- 25 oscillator. During a transient i.e. a change of the input signal fundamental frequency, the error signal is not zero therefore the controller modifies the frequency of the numerically controlled oscillator in order to achieve a zero error signal. The numerically controlled oscillator determines sampling instants of the analog to digital converter. The ratio between the fast sample rate and the slow sample rate remains constant during
- 30 operation of the loop.

With these new developments as a backbone, the system and method is readily portable to other systems where accurate synchronization with a disturbed input signal is needed or where the input signal synchronously oversampled digital sequence is needed.

DETAILED DESCRIPTION

- 5 Figure 1 is a block diagram showing the connections of the three primary components of the zero-crossing phase-locked loop.

Figure 2 is a graphical representation of the locking process of a zero crossing PLL after a step change in the frequency of the input signal at time 0. Converging estimates of positive going zero crossings are denoted with 'o' and converging estimates of both
10 positive going and negative going zero crossings are denoted with 'x'.

Figure 3 is a block diagram showing the connections of the necessary components of a multi-rate zero crossing sampling digital phase-locked loop.

Figure 4 is a graphical representation of the frequency response of the anti-aliasing filter used in a preferred embodiment of the multi-rate phase-locked loop.

- 15 The block diagram in Figure 5 represents the state-space model of the multi-rate PLL.

Figure 6 is a block diagram of a linearized state-space model of the multi-rate PLL shown in Figure 5.

Figure 7 is the Z -domain representation of the multi-rate digital phase-locked loop shown in Figure 6.

- 20 Figure 8 is the single rate block diagram of the multi-rate digital phase-locked loop in the Z -domain.

Figure 9 is a flow chart for a software implementation of the multi-rate digital phase-locked loop.

- 25 Figure 10 can serve for the purpose of comparison between the system response with PI and MRT control. This figure shows the response of the multirate digital PLL to a step frequency perturbation from 60Hz to 61Hz, occurring at the time $t=0$. The waveforms in

the figure represent the PLL error signal. The PLL response with PI control is shown by the solid line and the PLL response with MRT control is shown with the dashed line.

Figure 11 is the block diagram of the multi-rate digital phase-locked loop of Figure 5 with automatic gain control. The purpose of the automatic gain control is to accommodate
5 varying amplitude of input signals.

Figures 12 to 14 show the operation of the multirate digital phase-locked loop as it tracks zero crossings of various disturbed signals.

GENERAL DESCRIPTION OF PREFERRED EMBODIMENTS

The operation of the single rate zero crossing PLL is discussed with the aid of Figure 1.

10 The system input is the continuous time sinusoidal signal $s(t_c)$, where t_c stands for the continuous time. The PLL may consist of three blocks: an analog to digital converter (ADC), a controller and a numerically controlled oscillator (NCO). The sampling rate of the ADC is defined by the NCO frequency. The simplicity of the implementation of a zero crossing sampling PLL stems from the fact that it does not use a phase detector in the
15 ordinary sense. The role of the phase detector is played by the ADC, *i.e.* sampler. The loop interprets the samples of the input signal as the phase error. On the basis of the phase error, the controller modifies the frequency of the NCO. As a consequence, the ADC sampling instants are modified accordingly. The feedback action is such that the phase error is forced to zero. When zero error is achieved, the input signal is sampled
20 exactly at zero crossings and the PLL is locked. The locking process of the PLL is shown in Figure 2. The input continuous time signal is represented by the dashed line. Samples of the input signal are denoted by the circles.

Notice that the zero crossing sampling PLL is, by its nature, a variable sample rate system. In the steady state operation, the sample rate is equal to the input signal
25 frequency. The operation principle can be slightly modified so that the PLL steady state sample rate is equal to two times the input signal frequency (William C. Lindsey, Chak Ming Chie, "A Survey of Digital Phase-Locked Loops", Proceedings of the IEEE, Vol. 69, No. 4, pp. 410-431, April 1981). This is achieved by sampling the input signal on both positive and negative going zero crossings. The input signal samples in this type of PLL
30 are denoted with the 'x' sign in Figure 2.

A multirate PLL (Figure 3) has some features similar to the single rate zero crossing sampling PLL above. It contains an analog to digital converter (ADC), a controller and a numerically controlled oscillator (NCO). The sampling rate of the ADC is defined by the NCO frequency. The PLL error signal, on the basis of which the controller modifies the NCO frequency and, ultimately, sampling instants of the ADC is derived from the input signal samples. The PLL feedback action is such that the error is forced to zero. When zero error is achieved, the input signal is sampled exactly at zero crossings and the PLL is locked.

The multirate PLL is, by its nature, a variable sampling rate system. The principal difference compared to the single rate PLL is that blocks of the multirate PLL operate at two different sample rates. One sample rate is much higher than the input signal (carrier) frequency and is referred to as the fast sample rate (frequency). The other sample rate is equal to the carrier frequency (or double the carrier frequency if both positive going and negative going zero crossings are employed) and is referred to as the slow or fundamental sample rate. The relationship between the fast sample rate ν and the slow sample rate f is $\nu = N f$, where N is an integer. In general, the ratio between the fast and slow sample rate can be a rational number. The use of a rational ratio of the fast and slow sample rates can be beneficial, for example, in cases where the synchronization system is based on a Nyquist rate phase locked loop. However, in this preferred embodiment an integer ratio is used to benefit from the simplicity of the zero-crossing sampling phase-locked loop implementation.

The multirate PLL input signal is sampled at the fast sampling frequency. The fast sampling frequency is high enough so that no analog antialiasing filter in front of the ADC is necessary. Instead, it can be implemented as a digital filter in the digital part of the system.

This technique is, in digital signal processing (DSP), referred to as oversampling. The main advantage of having the antialiasing filter in the digital part of the system comes from the fact that in some applications it would be difficult, or impossible, to implement a practical analog antialiasing filter. To avoid aliasing in the part of the system operating at the slow sample rate, the antialiasing filter must precede the sample rate reduction block (downsampler).

The antialiasing filter is denoted by the letter B in Figure 3. Two points should be noticed in regard to the antialiasing filter. First, in the case of the PLL, it is a bandpass filter. Second, its centre frequency automatically tracks the carrier signal frequency. This feature is a benefit of the variable sample rate operation of the PLL. To obtain the error signal e , the bandpass filter output signal is downsampled by N in the downsampler block. In practical applications it is computationally more efficient to implement filtering and downsampling simultaneously rather than as separate operations. In this preferred embodiment, we use the Blackman window based finite impulse response bandpass filter of order 512. The filter frequency response is shown in Figure 4. The bandpass filter is implemented using a modified version of the efficient downsampling algorithm. The computation of the filter response, in our implementation, is distributed throughout the program execution loop. As a result, the program execution time is reduced.

Next, we formulate models of the multirate PLL. First, a nonlinear state-space model is formulated (Figure 5) and then it is linearized to obtain a linear state-space model (Figure 6). The transfer function model is obtained by applying the Z -transform methods to the linear state-space model. The block diagrams corresponding to Z -domain models are shown in Figures 7 and 8.

Nonlinear State-space Model

We will derive the model of the PLL under the assumption that the input signal frequency variation is a step function. We assume an input signal in the form of

$$s(t_c) = \begin{cases} S \sin(\Omega_q t_c) & , \quad t_c < 0 \\ S \sin(\omega t_c + \phi) & , \quad t_c \geq 0 \end{cases} \quad (1)$$

where: $\Omega_q = 2\pi f_q$ is the PLL nominal frequency and ϕ is a constant phase shift. We assume that for $t_c < 0$ the PLL is in a locked state. We will derive a model which describes the system behaviour for $t_c \geq 0$. To make the derivation easier to follow, we first consider a multirate PLL without an antialiasing filter and with a proportional controller. Once the transfer function model is derived, we will see that an antialiasing filter and a controller can then be incorporated into the model in a straightforward manner. The fast sample rate signals are indexed with n and the slow sample rate

signals are indexed with k . The discrete time $t(n)$ is a state variable and, to avoid confusion, we adopt $x(n) = t(n)$.

The sampled-data version of the input signal is

$$s(n) = S \sin \theta(n) = S \sin[\omega(n)x(n) + \phi]. \quad (2)$$

5 We use θ to denote the signal phase, namely

$$\theta(n) = \omega(n)x(n) + \phi. \quad (3)$$

The error signal is obtained through downsampling s by N . Therefore,

$$\begin{aligned} e(k) &= s(Nk) = S \sin \theta(Nk) = \\ &= S \sin[\omega(Nk)x(Nk) + \phi]. \end{aligned} \quad (4)$$

The signal at the output of the proportional controller is

$$10 \quad y(k) = Ke(k) = KS \sin[\omega(Nk)x(Nk) + \phi]. \quad (5)$$

The NCO frequency ν^o is given by $\nu^o(Nk) = \nu_q + Q y(k)$, where Q is the slope of the NCO transfer characteristic and $\nu_q = N f_q$. The ADC sampling period is

$$\begin{aligned} \tau(Nk) &= \frac{1}{\nu^o(Nk)} = \\ &= \frac{1}{\nu_q + KQS \sin[\omega(Nk)x(Nk) + \phi]}. \end{aligned} \quad (6)$$

15 Notice that $\tau(Nk)$ depends nonlinearly on $y(k)$. To emphasise this we can write $\tau(Nk) = \gamma(y(k))$. The NCO operates in such a way that N consecutive samples of τ , starting with $\tau(Nk)$, are equal to $\tau(Nk)$ i.e.

$$\tau(Nk+i) = \tau(Nk), \quad i = 0, 1, 2, \dots, N-1. \quad (7)$$

The next N sampling instants are given by

$$\begin{aligned} x(Nk+i+1) &= x(Nk+i) + \tau(Nk+i), \\ i &= 0, 1, 2, \dots, N-1. \end{aligned} \quad (8)$$

Equations (8) and (5) represent the state-space model of the PLL. The state variable is the sampling time $x(n)$, the system inputs are $\omega(n)$ and ϕ and the system output is $y(k)$.

On the basis of Eq.(3)-(8) we can draw a block diagram as shown in Fig.5. The block denoted by d represents a delay of one fast sampling period. It is used to implement Eq.(7).

Linear State-space Model

- 10 A linear model can be obtained through the linearization of the nonlinear model. The linearization is done in the neighborhood of a known solution of the system. If we take $\omega = \Omega_q$ and $\phi = 0$ in Eq.(1), the steady state solution is $x(n) = n\tau_q$. We will denote this solution by q , namely

$$q = nT_q. \quad (9)$$

- 15 The linearized form of Eq.(2) reads

$$\hat{s}(n) = P[\Omega\hat{x}(n) + q\hat{\omega}(n) + \hat{\phi}]. \quad (10)$$

where

$$P = S \cos(\Omega_q \cdot q) = S \cos\left(\frac{2\pi n}{N}\right). \quad (11)$$

- 20 The hat sign over variables denotes the perturbation of the variable. Notice that for $n = Nm$, and m an integer, we have $P = S$. Therefore, the linearized version of Eq.(4) reads

$$\hat{e}(k) = \hat{s}(Nk) = S[\Omega\hat{x}(Nk) + q\hat{\omega}(Nk) + \hat{\phi}]. \quad (12)$$

Linearization of Eq.(5)-(8) results in the following equations

$$\hat{y}(k) = K\hat{e}(k) = KS[\Omega\hat{x}(Nk) + q\hat{w}(Nk) + \hat{\phi}] \quad (13)$$

$$\hat{\tau}(Nk) = -\frac{1}{v_q^2} Q\hat{y}(k) = -J\hat{y}(k), \quad J = \frac{Q}{v_q^2}; \quad (14)$$

$$\hat{\tau}(Nk+i) = \hat{\tau}(Nk), \quad i = 0, 1, 2, \dots, N-1; \quad (15)$$

5 and

$$\hat{x}(Nk+i+1) = \hat{x}(Nk+i) + \hat{\tau}(Nk), \quad i = 0, 1, 2, \dots, N-1. \quad (16)$$

Equations (16) and (13) represent the linear state-space model of the PLL. The corresponding block diagram is shown in Figure 6. There are 3 time-varying blocks in the system. These are $n\tau_q$, $S\cos(2\pi n/N)$ and the downsampler block. The block $n\tau_q$ is a consequence of the relationship between the signal's angular frequency and phase and the fact that the frequency variation is a step function. The time varying block $S\cos(2\pi n/N)$ is due to the fact that the input sinusoidal signal is sampled at the fast sampling frequency. The time-varying nature of the system introduces difficulties in the analysis and design, in particular the treatment of the $S\cos(2\pi n/N)$ and downsampler blocks. Block $n\tau_q$ does not generate a difficulty because we can consider its output as an equivalent system input.

Transfer Function Model

In the general case, Z -transform methods are not applicable to time-varying systems. However, it is possible to extend the applicability of the Z -transform methods to the class of multirate systems where the ratio of sample rates is a rational number. The time-varying model of the multirate PLL, derived in the previous section, belongs to this class since the ratio of sample rates is an integer. Analytical techniques exist to enable the extension of the conventional Z -transform methods to multirate sampled-data systems. A novel aspect of this invention comes by applying these techniques to the linearized model given above to obtain the block diagrams shown in Figure 7 and Figure 8. This combination of techniques is new to the problem of PLL design. The letter z

denotes the complex variable in the Z -transform of the slow sample rate signals. To avoid confusion, the complex variable in the Z -transform of the fast sample rate signals is denoted by the letter p . The relationship between the two complex variables is $p^N = z$. The equivalent system input, for an input signal step frequency variation, is

5 $U(p) = p\omega_0\tau_g / (p-1)^2$, where ω_0 represents the value of the frequency step. The bandpass filter is represented by the transfer function $B(p)$ and the controller is represented by the transfer function $K(z)$. The time-varying block $S\cos(2\pi n/N)$ and the downsampler are denoted by M and D , respectively.

The input-output relationship of these blocks cannot be represented in the form of a
10 transfer function. However, it can be represented in the form of a complex mapping. Block M multiplies the incoming signal by $S\cos(2\pi n/N)$. The input to the block is phase $\hat{\theta}(n)$ and its output is the signal $\hat{s}(n)$. The Z -transforms of $\hat{\theta}(n)$ and $\hat{s}(n)$ are denoted by $\Theta(p)$ and $s(p)$, respectively. The input-output relationship of the block M can be represented in the form of the mapping $s(p) = M(\Theta(p))$. It is known that the
15 mapping M has the form

$$s(p) = \frac{S}{2} \left[\Theta \left(p e^{j\frac{2\pi}{N}} \right) + \Theta \left(p e^{-j\frac{2\pi}{N}} \right) \right]. \quad (17)$$

Block D downsamples the incoming signal by a factor N . Its output is the error signal $\hat{e}(k)$. Let us denote the Z -transform of $\hat{e}(k)$ by $E(z)$. The block can be described by the mapping $E(z) = D(s_f(p))$. Applying multirate Z -transform methods the mapping
20 has the form

$$E(z) = \frac{1}{N} \sum_{i=0}^{N-1} s_f \left(p e^{j\frac{2\pi i}{N}} \right). \quad (18)$$

There is a subtlety in Eq.(18) with respect to the complex variables z and p . By application of the mapping, $s_f(p)$ is mapped into $E(p^N)$ but since $p^N = z$, the end result is $E(z)$.

The NCO transfer function can be derived with the aid of the following observations. The sample rate of the NCO input signal $\hat{y}(k)$ is equal to the slow sample rate and the sample rate of its output signal $\hat{r}(n)$ is equal to the fast sample rate. For each input sample, the NCO generates N equal output samples (see Eq.(14) and (15)). If we
 5 assume that the input is the unit delta function it follows that the NCO response, and therefore its transfer function, is

$$G(p) = -J(1 + p^{-1} + p^{-2} + \dots + p^{-(N-2)} + p^{-(N-1)}) \quad (19)$$

The minus sign in Eq.(19) is extracted to the feedback summing node in Figure 7. The NCO response to an arbitrary signal $Y(z)$ reads $\tau(p) = G(p)Y(z) = G(p)Y(p^N)$. Using
 10 Z-transform methods which are applicable to multirate systems, the multirate block diagram from Figure 7 can be transformed into an equivalent single rate block diagram shown in Figure 8. The equivalent system input is $U(z) = z\omega_0 T_q / (z-1)^2$ and $A(z)$ is a transfer function obtained in the process of transformation. Notice that the bandpass filter response is incorporated in $A(z)$. The block diagram in Figure 8 can be used for
 15 the system stability analysis and the PLL controller design. Since it is a single rate system, all conventional Z-transform methods can be applied.

Software Implementation of the PLL

One issue in the realization of the PLL is the implementation of variable sample rate signal processing. In the realizations based on a digital signal processor, variable
 20 sample rate processing can be efficiently implemented using the processor timer. The timer may be comprised of a period register and a counter. The period register holds the desired value of the sampling period and the counter counts the processor clock. When the counter content is equal to the content of the period register, the timer interrupt is generated and the timer is reset and started again. It is possible to modify the period
 25 register once the counter is started. To that purpose it is necessary to hold the counter while the content of the period register is modified.

The flow chart of a PLL implementation algorithm is shown in Figure 9. The fast sample rate signal processing is done in the inner program loop and the slow sample rate signal processing is done in the outer loop. At the beginning of the outer loop, the processor

timer is initialized with the value corresponding to the maximum value of the fast sampling period. The actual value of the fast sampling period is written into the timer later, when it becomes available. While the timer counts towards the value equal to the maximum sampling period, the remaining part of the loop is executed. It consists of
 5 reading the ADC, bandpass filtering, controller output computation and the fast sampling period computation.

Once the actual value of the sampling period is computed, it is written into the timer. After finishing the remaining operations, such as writing the system outputs, the processor enters an idle state, waiting for the timer interrupt. When the content of the
 10 timer counter is equal to the content of the period register it means that the current fast sampling period has elapsed. The timer generates an interrupt and the execution of the inner loop begins. When all operations in the inner loop are done, the processor again enters an idle state. Upon arrival of the next timer interrupt, the inner loop is repeated. The inner loop is repeated a total of $N - 1$ times. After that, the program execution is
 15 repeated from the beginning of the outer loop. Two facts should be noticed with regard to the timer operation. First, the length of the time interval between successive timer interrupts is equal to the fast sample period. Therefore, the timer sets the fast sample rate. The slow sample period is obtained simply by counting a total of N fast sample periods. Second, all N fast sample periods which make one slow sample period are
 20 equal. Alternatively, the PLL algorithm can be implemented in an interrupt service routine. This approach has an advantage that the processor is available to execute non real time tasks during the time intervals when it does not execute real time tasks. With regard to the bandpass filter implementation, we would like to point out that in this preferred embodiment we use a modified version of the efficient downsampling algorithm
 25 presented in Ronald E. Crochiere, Lawrence R. Rabiner, *Multirate Digital Signal Processing*, (Prentice-Hall Inc.: Englewood Cliffs, New Jersey, 1983). In our implementation of the efficient downsampling algorithm, the computation of the bandpass filter response is distributed in all N fast sample periods. This modification results in the reduction of the execution time.

Control of the PLL

The control aspects and the tracking properties of the PLL may be examined in relation to a preferred embodiment, where the system is employed for frequency tracking of 60Hz AC utility network signals. The parameters of the PLL are as follows.

- 5 Input signal amplitude: $S = 1.0$
 Nominal frequency: $f_q = 60 \text{ Hz}$
 Upsampling ratio: $N = 128$
 Antialiasing filter: As specified above.

NCO:

- 10 Nominal frequency: $\nu_q = 7.680 \text{ kHz}$
 Minimum frequency: $\nu_{\min} = 6.144 \text{ kHz}$
 Maximum frequency: $\nu_{\max} = 9.216 \text{ kHz}$
 Negative saturation level: $V_{s2} = -2.0$
 Positive saturation level: $V_{s1} = 2.0$

- 15 We consider a proportional-integral (PI) controller and the minimum response time (MRT) controller. The MRT controller is often referred to as the deadbeat controller.

The PLL with PI control tracks the step input signal frequency variation with zero steady state error. This can be proved by applying the final value theorem to the expression for $E(z)$ obtained from Figure 8. The controller parameters can be found by a Nyquist
 20 criterion based trial and error method. The loop gain phase margin of 45 degrees is obtained with the following controller

$$K(z) = 0.222 \frac{z - 0.937}{z - 1.000} \quad (20)$$

- The response of the PLL to a step frequency perturbation from 60 Hz to 61 Hz, occurring at time $t = 0$, is shown with the solid line in Fig.10. The figure shows the PLL error
 25 signal.

For polynomial system inputs (step, ramp, quadratic function etc.) there is a formal design approach to design a controller which gives the minimum system response time (see John R. Ragazzini, Gene F. Franklin, *Sampled-Data Control Systems* (McGraw-Hill, New York, 1958). Using this approach we obtained the 5th order controller whose coefficients are given in Table 1. The numerator and denominator coefficients of the transfer function are given in the 2nd and 3rd row of the table, respectively. In the 1st row are given powers of z to which the coefficients relate.

	z^5	z^4	z^3	z^2	z^1	z^0
n_k	9.034	-6.538	0.000	0.000	0.000	0.000
d_k	1.000	1.475	0.269	-1.787	-0.909	-0.047

Table 1. Coefficients of the MRT controller transfer function.

The practical implementation of the controller would normally contain an anti wind up and the loop gain control feature.

Feedback loops containing a controller with an integrator (summer) and a block with a saturating characteristic can experience an undesired operating mode known as integrator wind up. Both, the PI controller and the minimum response time controller, as described above, contain an integral term. The block with a saturating characteristic, in the case of the PLL, is the NCO. The final effect of the integrator wind up is that the output of the saturating block bounces between saturation levels and the whole system oscillates in the form of large signal oscillations. The integrator wind up is prevented by incorporating saturation in the controller implementation. In our implementation, we use the direct form I of digital filters (A. V. Oppenheim, R. W. Schaffer, *Digital Signal Processing*. Englewood Cliffs, New Jersey: Prentice-Hall Inc., 1975.) to implement the controller and we incorporate saturation at the controller output.

An undesirable characteristic of the ZC-PLL is that its dynamic properties depend on the input signal amplitude. This can be explained by the fact that the signal amplitude appears as a gain block in the block diagram shown in Figure 7. The present invention helps solve this problem by incorporating automatic gain control (AGC) into the PLL.

The basic idea in the AGC is to modify the system loop gain with the estimated value of the input signal amplitude. This can be accomplished as shown in Figure 11. The solution shown in this figure is based on the multirate nature of the system. The input

signal is sampled at a rate which is N times higher than the carrier signal frequency. As a result, at the output of the ADC there are a total of N signal samples per period of the input signal. These samples are used to estimate the signal amplitude in the estimator block E . The amplitude estimate is obtained by the computation of the fundamental harmonic in the discrete-time Fourier series. The PLL error signal is obtained by downsampling the antialiasing (bandpass) filter output signal by N . The downsampled error signal is modified with the amplitude estimate so that the PLL loop gain is independent of the signal amplitude. An approach to design the PLL with the AGC is first to design the PLL without the AGC and then simply add the AGC. The output of the amplitude estimation block can be at any rate between the fast sample rate and the slow sample rate. This preferred embodiment uses the slow rate for computational efficiency. Other applications may require a faster response to a variation of the amplitude of the input signal. The ability to obtain an amplitude estimate at any rate between the fast and slow sample rate including the fast and slow sample rate should also be considered as an element of this invention.

PLL Tracking Properties

One goal of the present invention is to track disturbed network signals. In order to test the ability of the invention to track disturbed signals, we used the test signal shown by the solid line in Figure 12.

It is a sinusoidal signal with superimposed notch type disturbance and noise. We assume that the notch type disturbance is produced by a line-commutated phase-controlled converter operating with delay angle of 90 degrees. The notch width is 300us. For the noise component we use a random signal with a uniform probability density function. The maximum peak to peak noise value is equal to 50% of the signal fundamental harmonic amplitude. In addition to the disturbances, we assume that the frequency and amplitude of the signal fundamental harmonic are variable. We use a step or ramp frequency variation and a step amplitude variation. The desired output of the synchronization system is represented in the form of the rectangular signal drawn with the dashed line in Figure 12. We can see that the signal zero crossings are correctly estimated regardless of the disturbances.

The PLL tracking properties are tested using the disturbed signal from Figure 12 under the conditions where the signal frequency and the signal amplitude are variable. We assume that the frequency and amplitude of the signal are variable as shown in Figure 13a. The frequency variation is in the form of a ramp function with the rate of change of 1 Hz/s. The amplitude variation is in the form of a step function with the step value equal to 50% of the signal amplitude. The response of the PLL with a PI control to this test signal is shown in Figure 13b. The figure shows the PLL error signal. We can see that, apart from the relatively small jitter, the tracking error during the intervals with constant signal frequency is zero. During the frequency ramping intervals, the tracking error has a constant value.

The PLL tracking properties are also tested using an arc furnace voltage as the input signal. Arc furnaces are known for their ability to generate disturbances onto the AC utility network. A typical waveform of an arc furnace voltage is shown by the solid line in Figure 14. The PLL estimate of the arc furnace voltage zero crossings is shown in the form of the rectangular signal drawn by the dashed line.

According to the invention described, phase synchronization to disturbed utility network signals can be efficaciously achieved using the proposed multirate PLL based synchronization system. The system comprises an antialiasing filter for signal disturbance rejection. The multirate nature of the system enables the implementation of the antialiasing filter in the digital part of the system. A software implementation algorithm is presented, and the industrial applicability is verified by addressing the system's control requirements and by demonstrating the expected response using a sinusoidal signal containing a notch type disturbance and noise and an arc furnace voltage signal.

A practical consideration in designing the system is the choice of the oversampling rate for the input signal. The oversampling rate must be high enough to avoid aliasing, but low enough to allow the real time implementation of the algorithm. The ratio of the oversampling (the fast) rate and the input signal fundamental frequency is denoted by N . With analog to digital converters now available, the value of N as high as 20,000 can easily be achieved.

The present invention has been described with respect to three-phase networks and 60 Hz power signals as particular embodiments. It will be appreciated by those of ordinary skill in the art that, in light of the present disclosure, the system and methods described allow for synchronization to disturbed signals at other frequencies and in other contexts, without departing from the intended scope of the invention. All such modifications are intended to be included within the scope of this disclosure.

CLAIMS

We claim:

1. A digital multirate zero-crossing phase-locked loop, for synchronization to an input signal having a variable fundamental frequency or variable amplitude, comprising:

an analog to digital converter for sampling the input signal at a fast sample rate and for generating a digital sequence, the fast sample rate being sufficiently large to avoid aliasing and being a multiple of a slow sample rate;

a digital bandpass filter for filtering the digital sequence and for outputting a filter output sequence, the digital bandpass filter having a centre frequency which tracks the input signal fundamental frequency;

an amplitude estimation block for generating an amplitude estimate of the fundamental harmonic of the input signal based on the digital sequence;

a gain control block for scaling the filter output sequence, or a subsequence thereof, by the inverse of the amplitude estimate and for outputting a scaled sequence;

a controller for receiving an error sequence at the slow sample rate and for outputting a controller output with anti-wind up protection to a numerically controlled oscillator, the controller controlling the numerically controlled oscillator in order to track the variable fundamental frequency of the input signal according to a phase-locked loop algorithm, the error sequence being the scaled sequence, or a subsequence thereof, and the phase-locked loop algorithm operating on the error sequence to force the error sequence to zero;

the numerically controlled oscillator for receiving the controller output, for generating a clock signal frequency based on the controller output and

where the clock signal frequency determines the fast sample rate of the analog to digital converter,

whereby the fast sample rate and slow sample rate are modified by phase-locked loop feedback action to force the error sequence to zero at which point the fast sample rate and the slow sample rate are synchronized to the fundamental frequency of the input signal.

2. The digital multirate zero-crossing phase-locked loop of claim 1 further comprising a downsampler for sampling the filter output sequence of the digital bandpass filter at the slow sample rate.

10 3. The digital multirate zero-crossing phase-locked loop of claim 1 further comprising a downsampler for sampling the output of the gain control block at the slow sample rate.

4. The digital multirate zero-crossing phase-locked loop of claims 1 to 3 wherein the ratio of the fast sampling rate and slow sampling rate is an integer N .

15 5. The digital multirate zero-crossing phase-locked loop of claim 4 wherein the integer N is a power of 2.

6. The digital multirate zero-crossing phase-locked loop of claims 1 to 5 wherein the anti-wind up protection is obtained by using saturation at the controller output.

20 7. The digital multirate zero-crossing phase-locked loop of claim 6 wherein the controller is a proportional integral controller.

8. The digital multirate zero-crossing phase-locked loop of claim 6 wherein the controller is a minimum response time controller.

25 9. The digital multirate zero-crossing phase-locked loop of claims 1 to 8, wherein the slow sample rate in steady-state is equal to the fundamental frequency of the input signal.

10. The digital multirate zero-crossing phase-locked loop of claims 1 to 8, wherein the slow sample rate in steady-state is equal to two times the fundamental

frequency of the input signal and the phase-locked loop algorithm uses both negative going and positive going zero-crossings.

11. The digital multirate zero-crossing phase-locked loop of claims 1 to 10 wherein the digital bandpass filter is a Blackman window based finite impulse response bandpass filter of order 512.

12. The digital multirate zero-crossing phase-locked loop of claims 1 to 11 wherein the amplitude estimation block generates the amplitude estimation at any rate between the fast sample rate and the slow sample rate by computing the fundamental harmonic of the input signal using the discrete-time Fourier series of the digital sequence, or a subsequence thereof,

13. A method for synchronization to a input signal with a variable fundamental frequency and/or variable amplitude comprising:

sampling the input signal at a fast sample rate to generate a digital sequence, the fast sample rate being sufficiently high to avoid aliasing and being a multiple of a slow sample rate;

filtering the digital sequence using a digital bandpass filter to output a filter output sequence, the digital bandpass filter having a centre frequency which tracks the input signal fundamental frequency;

estimating the amplitude of the fundamental harmonic of the input signal based on the digital sequence;

scaling the filter output sequence, or a subsequence thereof, by the inverse of the amplitude of the fundamental harmonic of the input signal and outputting a scaled bandpass filter output sequence;

performing a phase-locked loop control algorithm on an error sequence at the slow sample rate and generating a controller output, the error sequence being the scaled bandpass filter output sequence, or a subsequence thereof, and the controller output controlling the fast sample rate in order to obtain a sampling of the input signal which results in zero error sequence;

whereby the fast sample rate and slow sample rate are modified by phase-locked loop feedback action to force the error sequence to zero at which point the fast sample rate and the slow sample rate are synchronized to the fundamental frequency of the input signal.

- 5 14. The method of claim 13 further comprising a downsampler for sampling the filter output sequence of the digital bandpass filter at the slow sample rate.
15. The method of claim 13 further comprising a downsampler for sampling the scaled filtered output sequence at the slow sample rate.
- 10 16. The digital multirate zero-crossing phase-locked loop of claims 13 to 16 wherein the controller output is obtained using a proportional integral controller with anti-wind up protection, the anti-wind up protection obtained by using saturation at the controller output.
- 15 17. The method of claims 13 to 16 wherein the controller output is obtained using a minimum response time controller with anti-wind up protection, the anti-wind up protection obtained by using saturation at the controller output.
18. The digital multirate zero-crossing phase-locked loop of claims 1 to 8, wherein the slow sample rate in steady-state is equal to the fundamental frequency of the input signal.
- 20 19. The digital multirate zero-crossing phase-locked loop of claims 1 to 8, wherein the slow sample rate in steady-state is equal to two times the fundamental frequency of the input signal and the phase-locked loop algorithm uses both negative going and positive going zero-crossings.
- 25 20. A method for estimating the amplitude of the fundamental harmonic of an input signal with a variable fundamental frequency or variable amplitude comprising:

sampling the input signal at a fast sample rate to generate a digital sequence, the fast sample rate being sufficiently high to avoid aliasing and being a multiple of a slow sample rate;

filtering the digital sequence using a digital bandpass filter to output a filter output sequence, the digital bandpass filter having a centre frequency which tracks the disturbed signal fundamental frequency;

5

computing the fundamental harmonic of the input signal using the discrete-time Fourier series of the digital sequence, or a subsequence thereof, to estimate an amplitude estimate of the fundamental harmonic of the input signal, and where the amplitude estimate sample rate can be in the range between the slow sample rate and the fast sample rate;

10

scaling the filter output sequence, or a subsequence thereof, by the inverse of the amplitude of the fundamental harmonic of the input signal and outputting a scaled bandpass filter output sequence;

15

performing a phase-locked loop control algorithm on an error sequence at the slow sample rate and generating a controller output, the error sequence being the scaled bandpass filter output sequence, or a subsequence thereof, and the controller output controlling the fast sample in order to obtain a sampling of the input signal which results in zero error sequence.

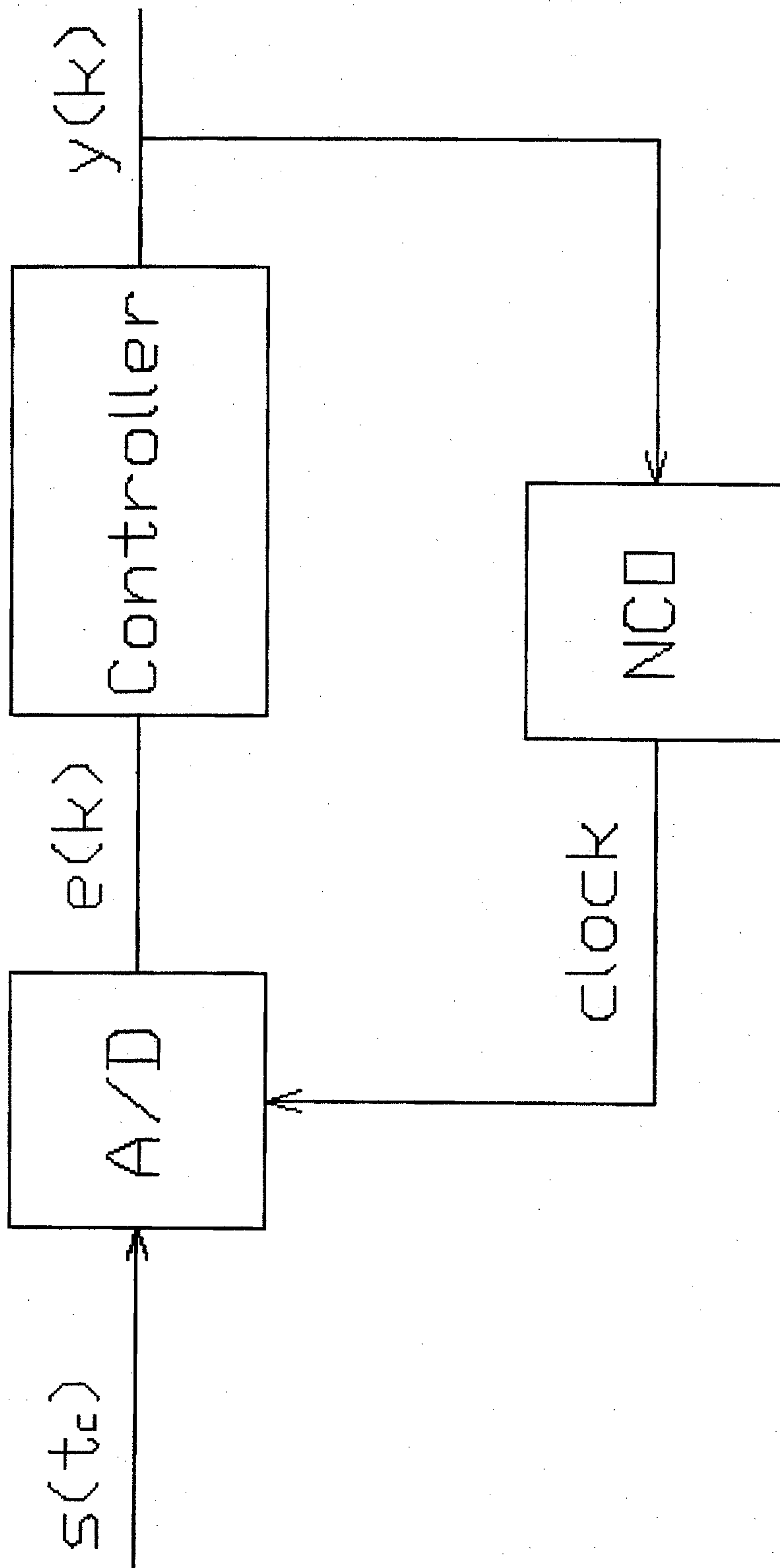


Figure 1. Zero crossing sampling digital PLL.

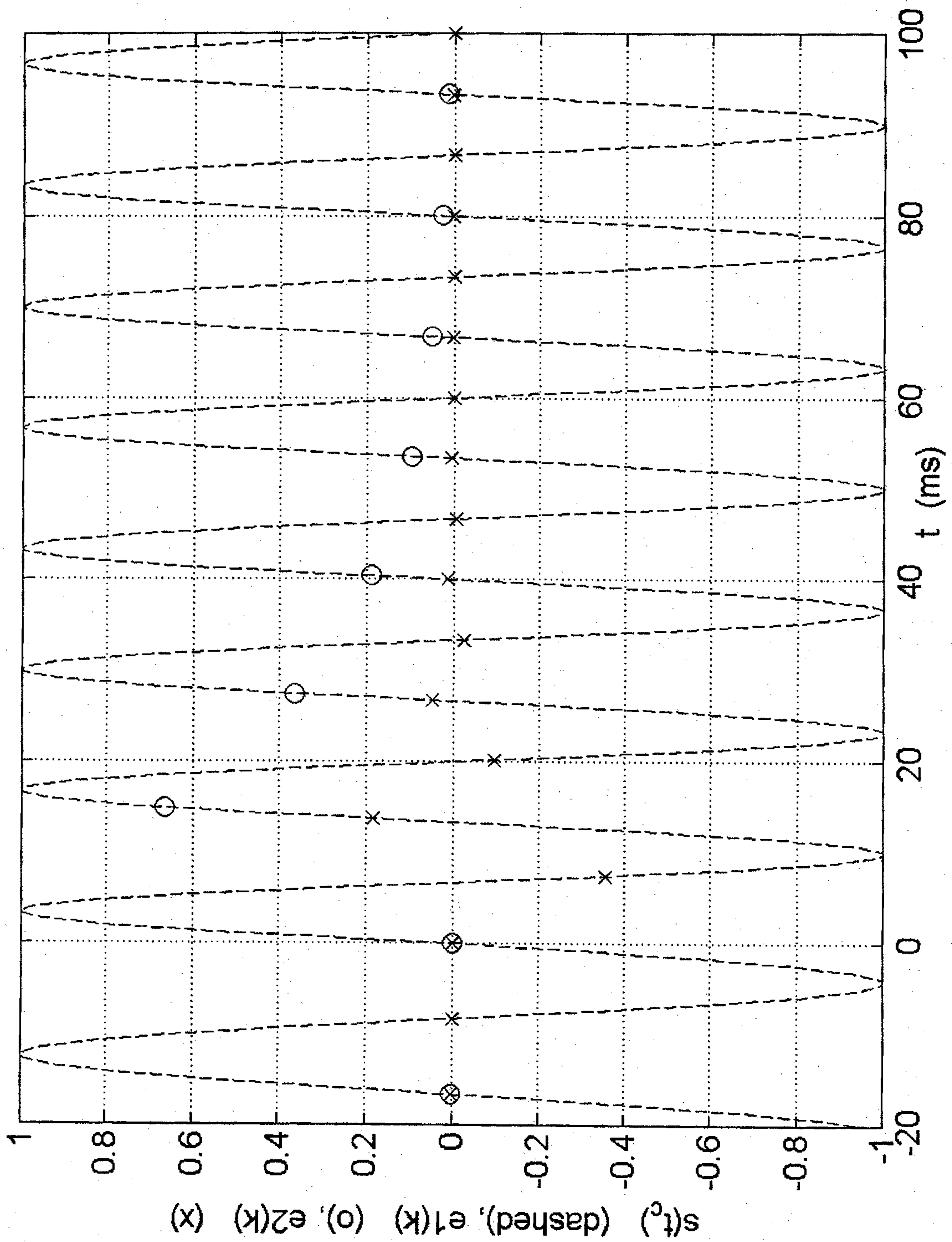


Figure 2: Locking Process of Type 1 PLL ('o') and Type 2 PLL ('x')

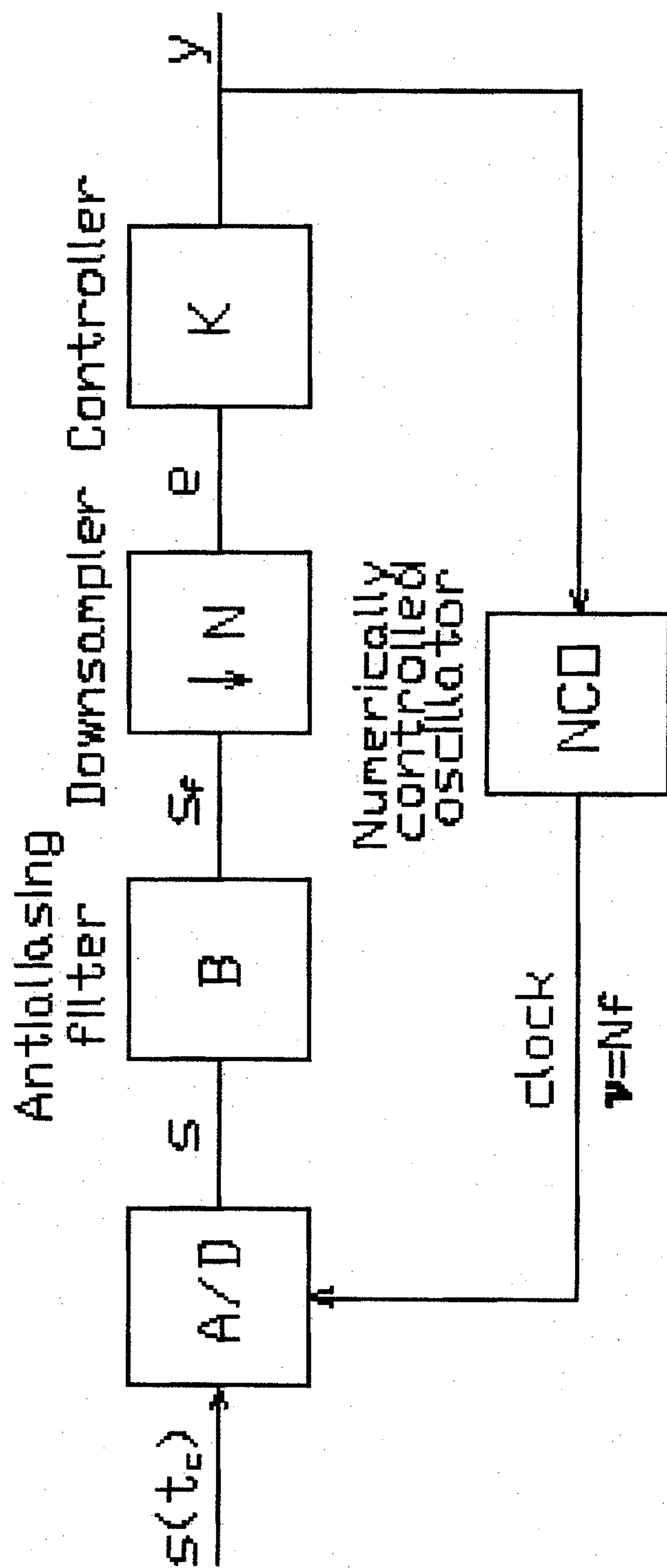


Figure 3. Multirate zero crossing sampling digital PLL.

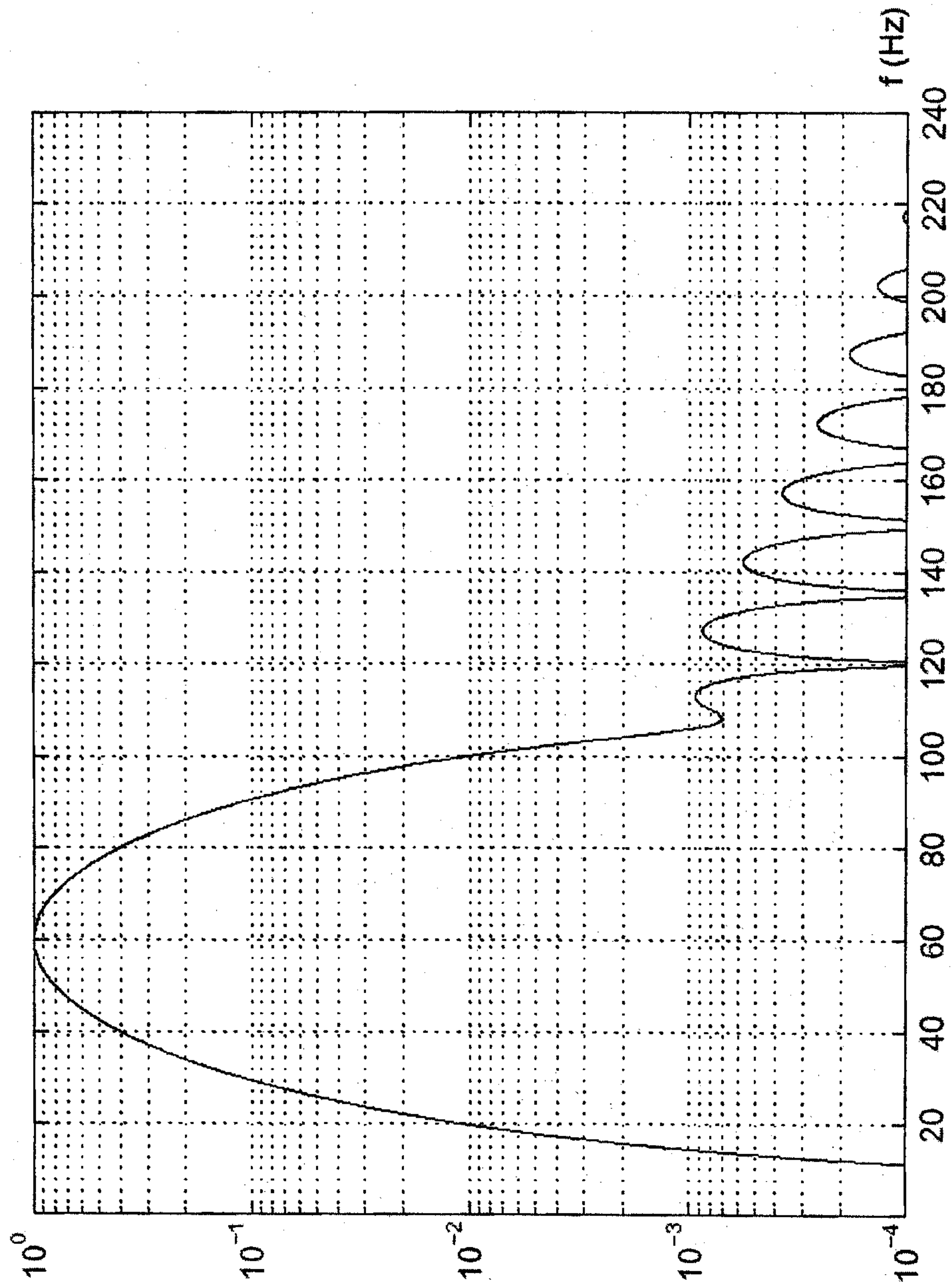


Figure 4. Frequency response of the antialiasing filter.

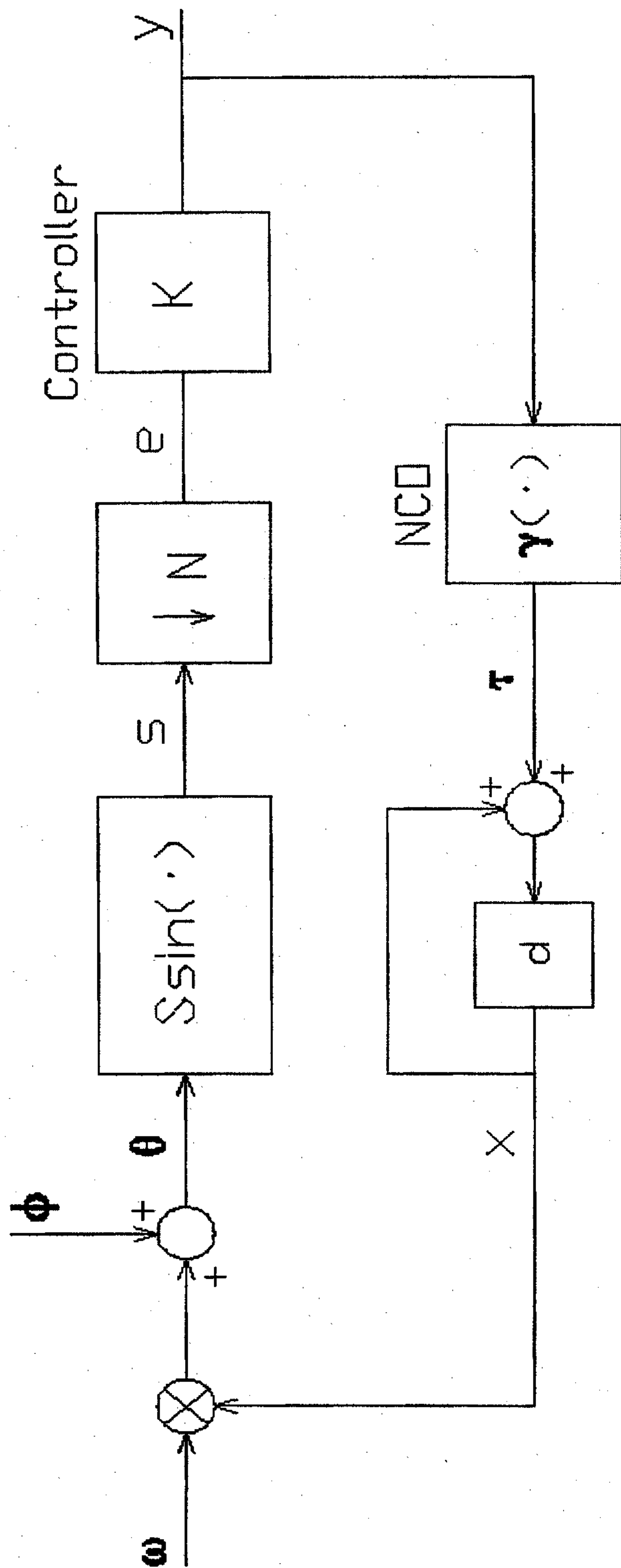


Figure 5. Block diagram of the PLL.

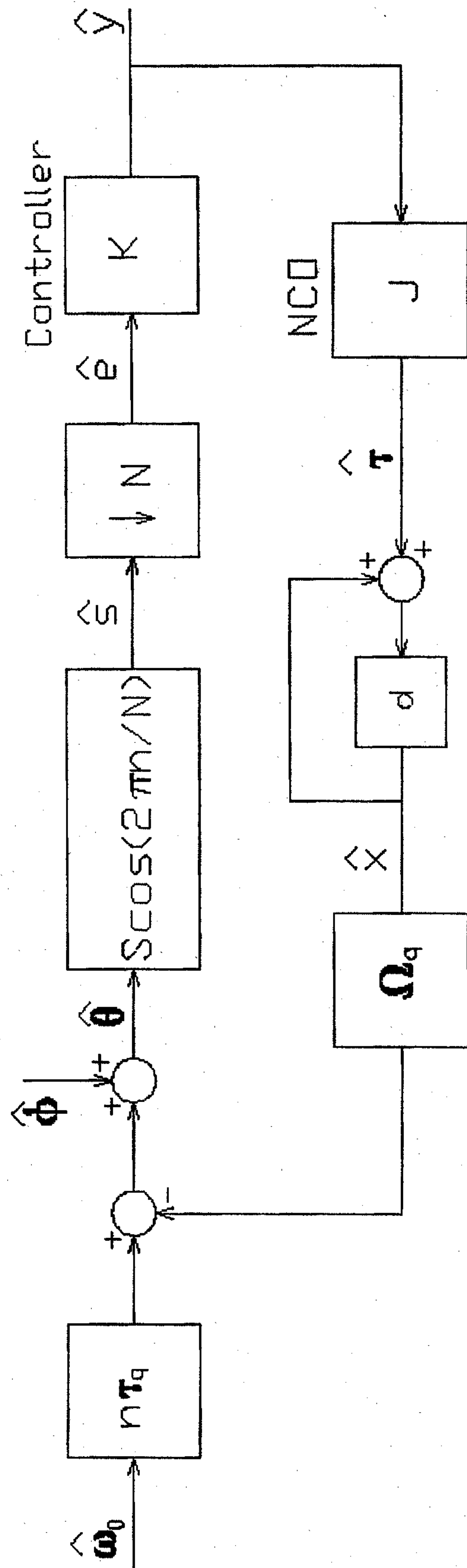


Figure 6. Block diagram of the linear model of the PLL.

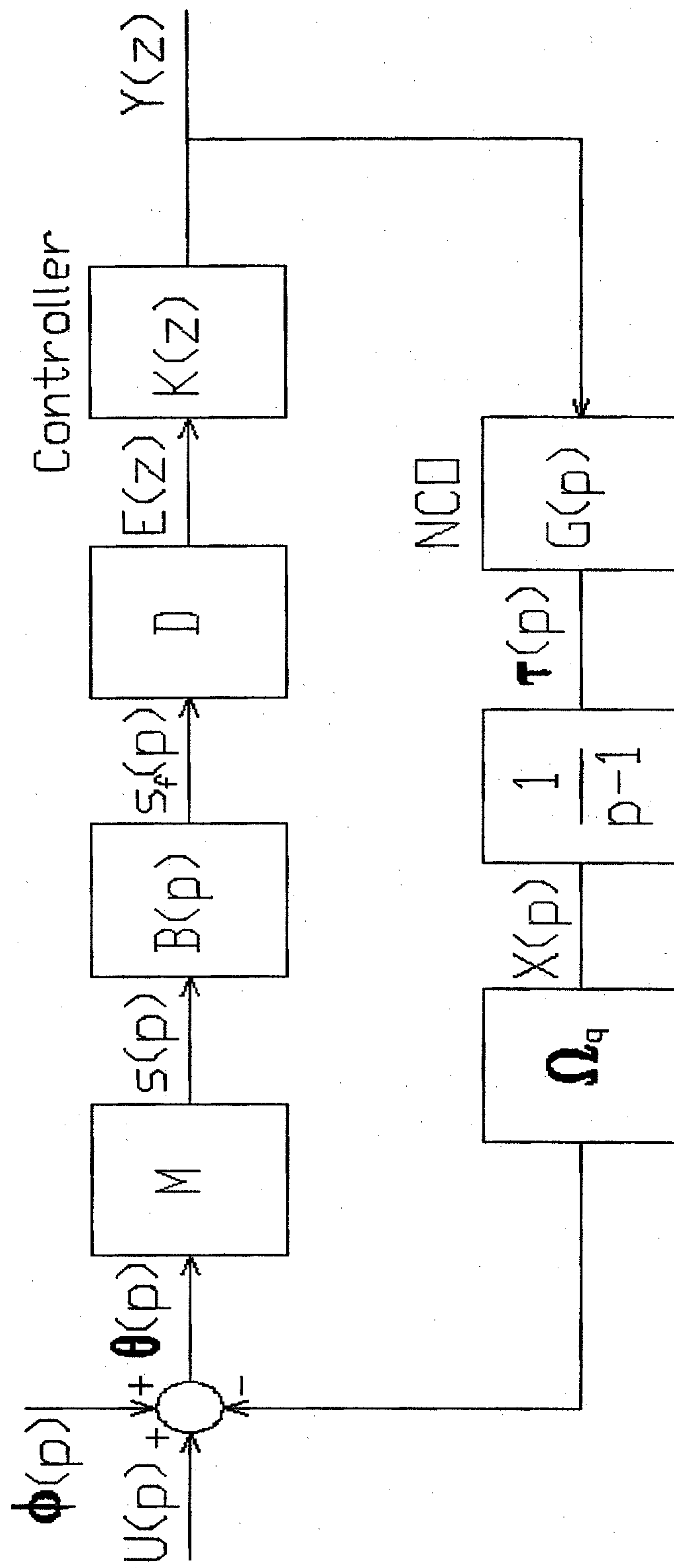


Figure 7. Z-domain block diagram of the PLL.

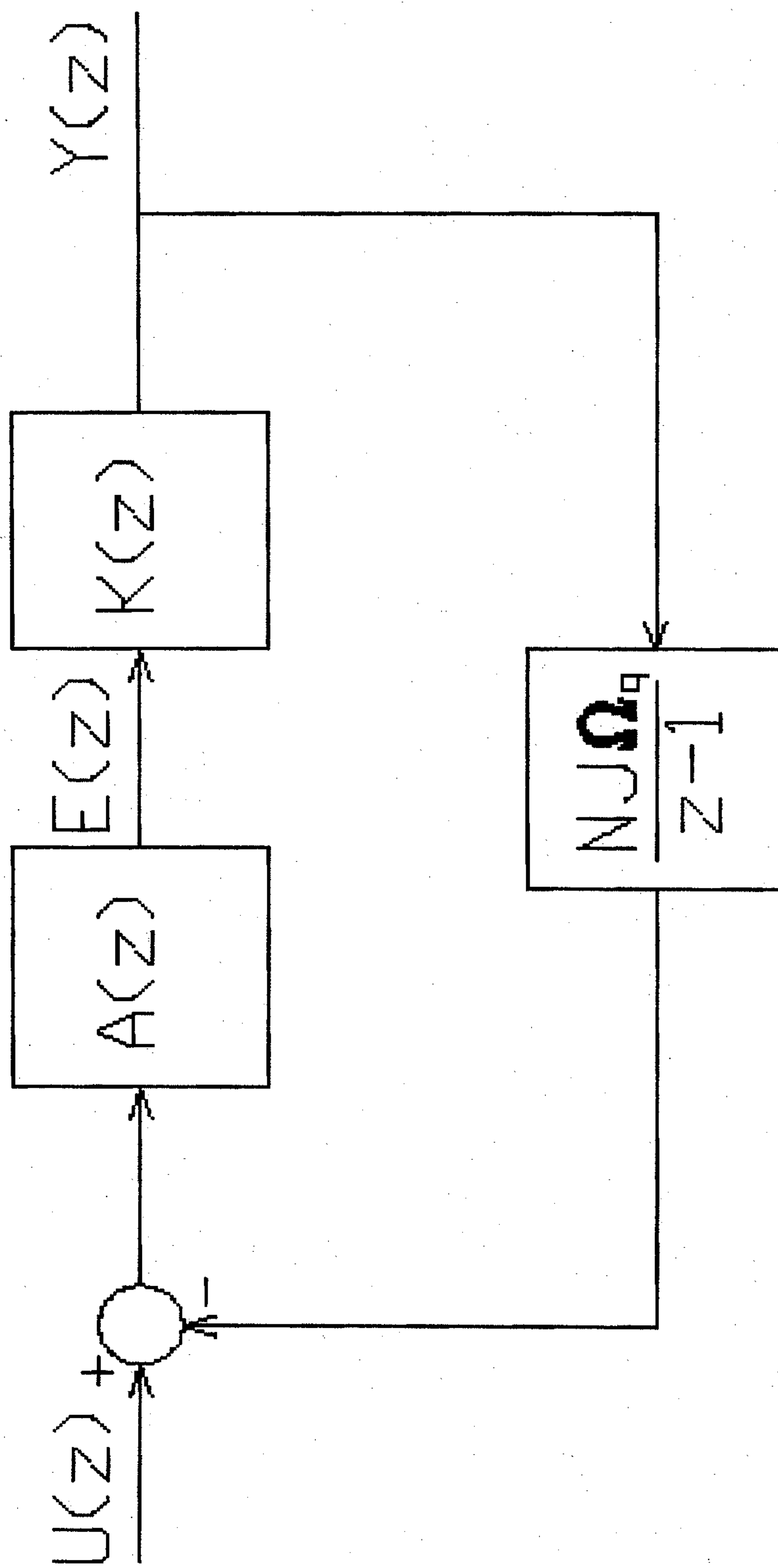


Figure 8. Single rate block diagram of the PLL.

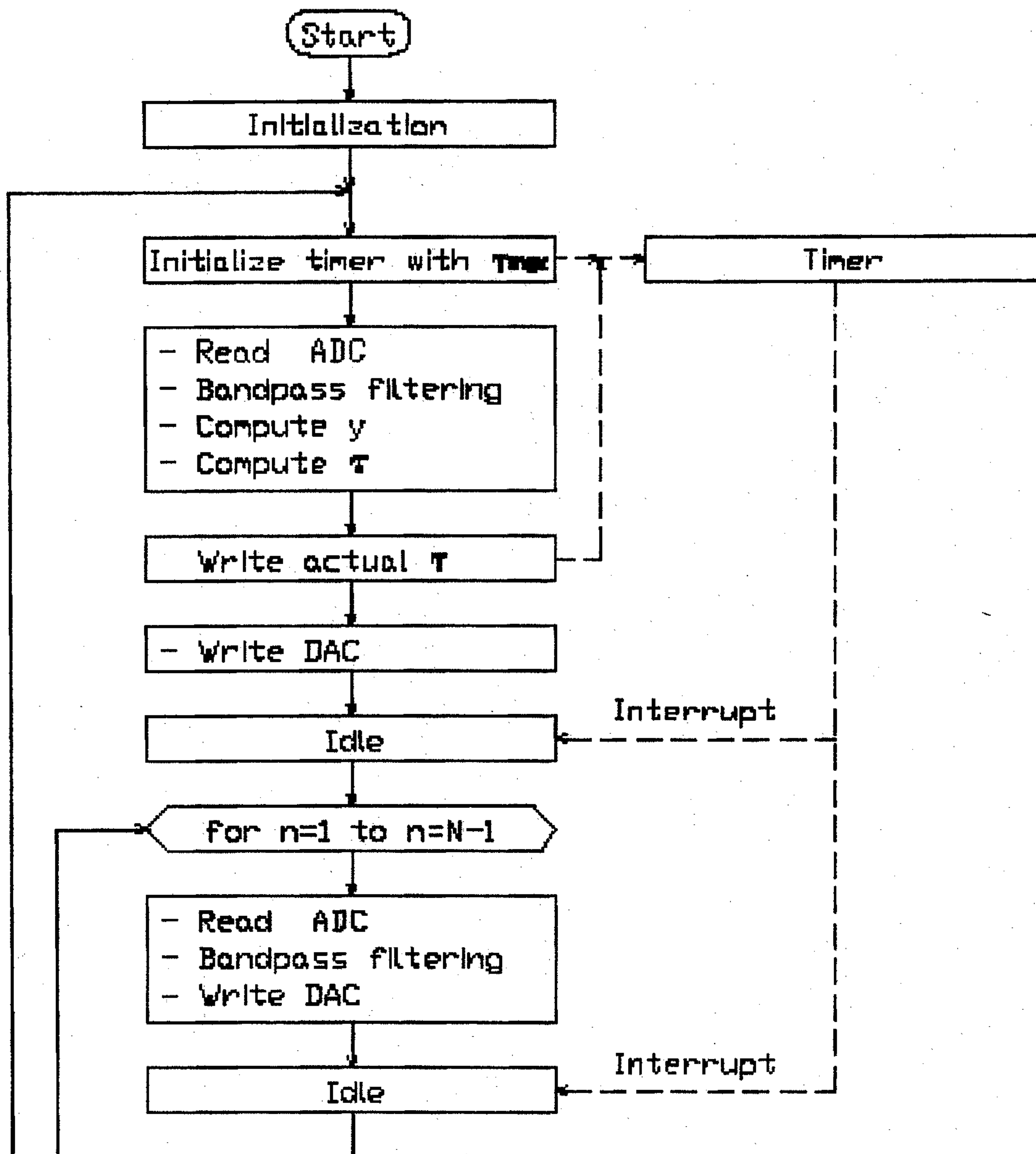


Figure 9. Multirate PLL program flowchart.

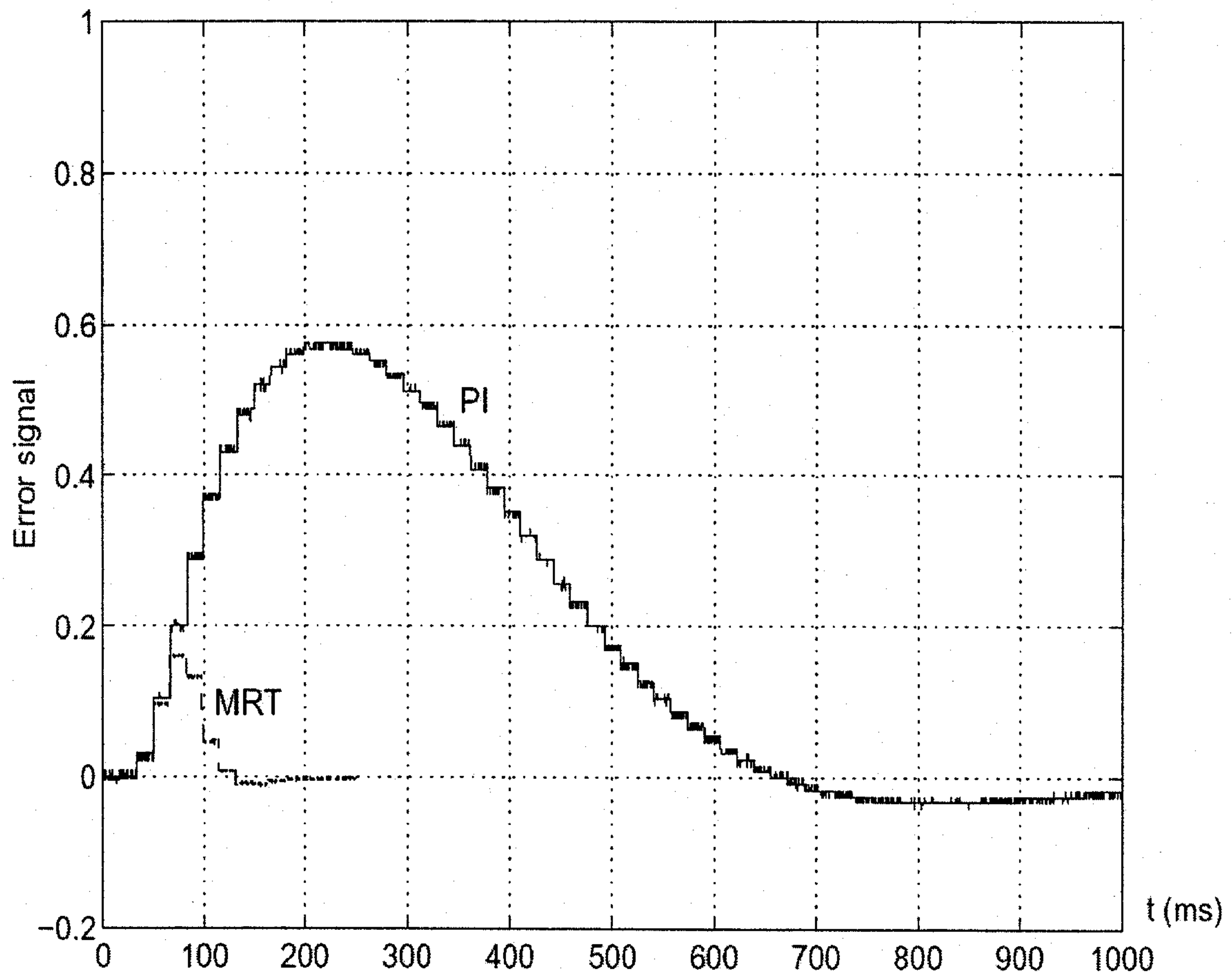


Figure 10. The PLL response to the step frequency variation.

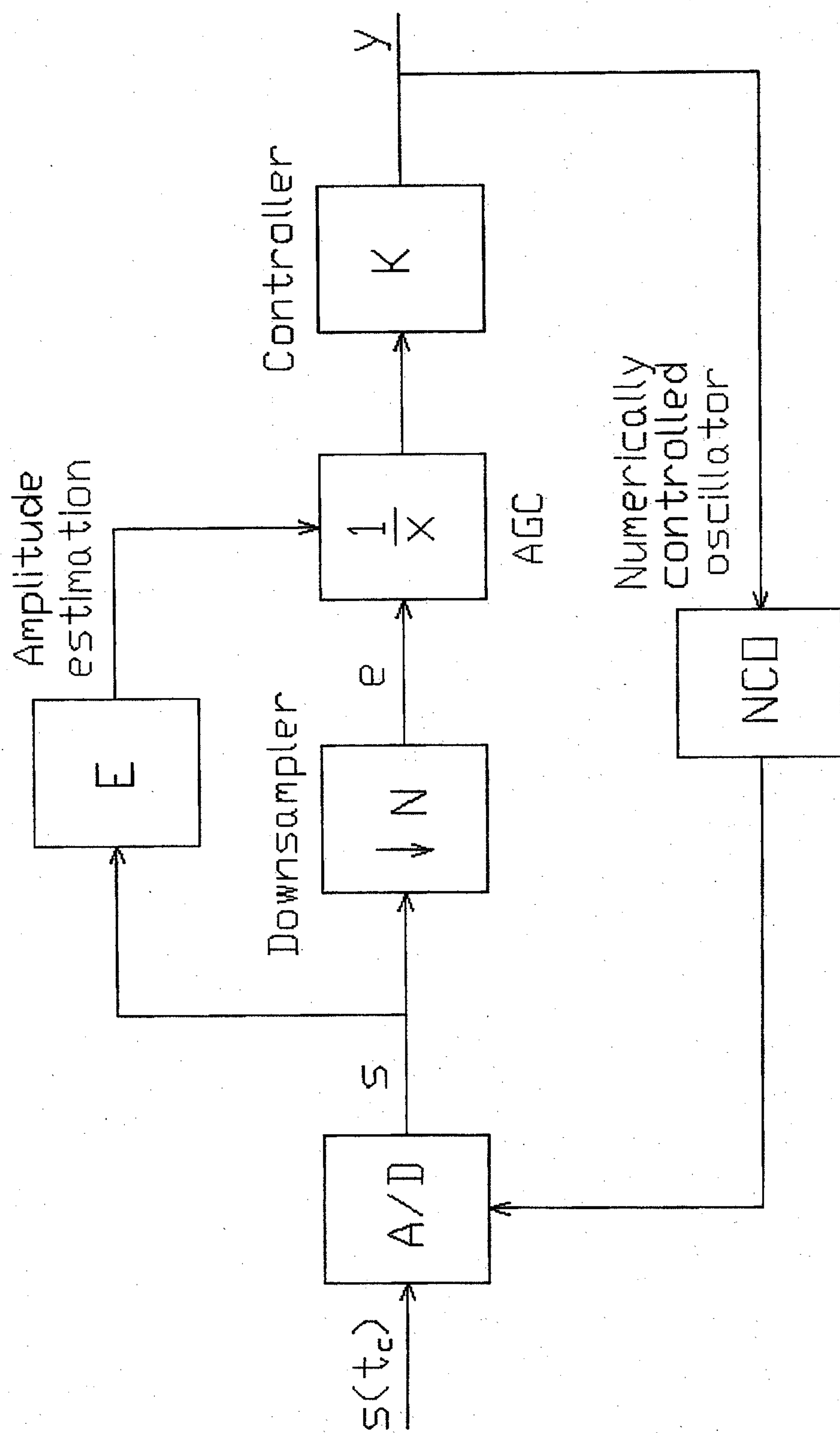


Figure 11. PLL with Automatic Gain Control (AGC)

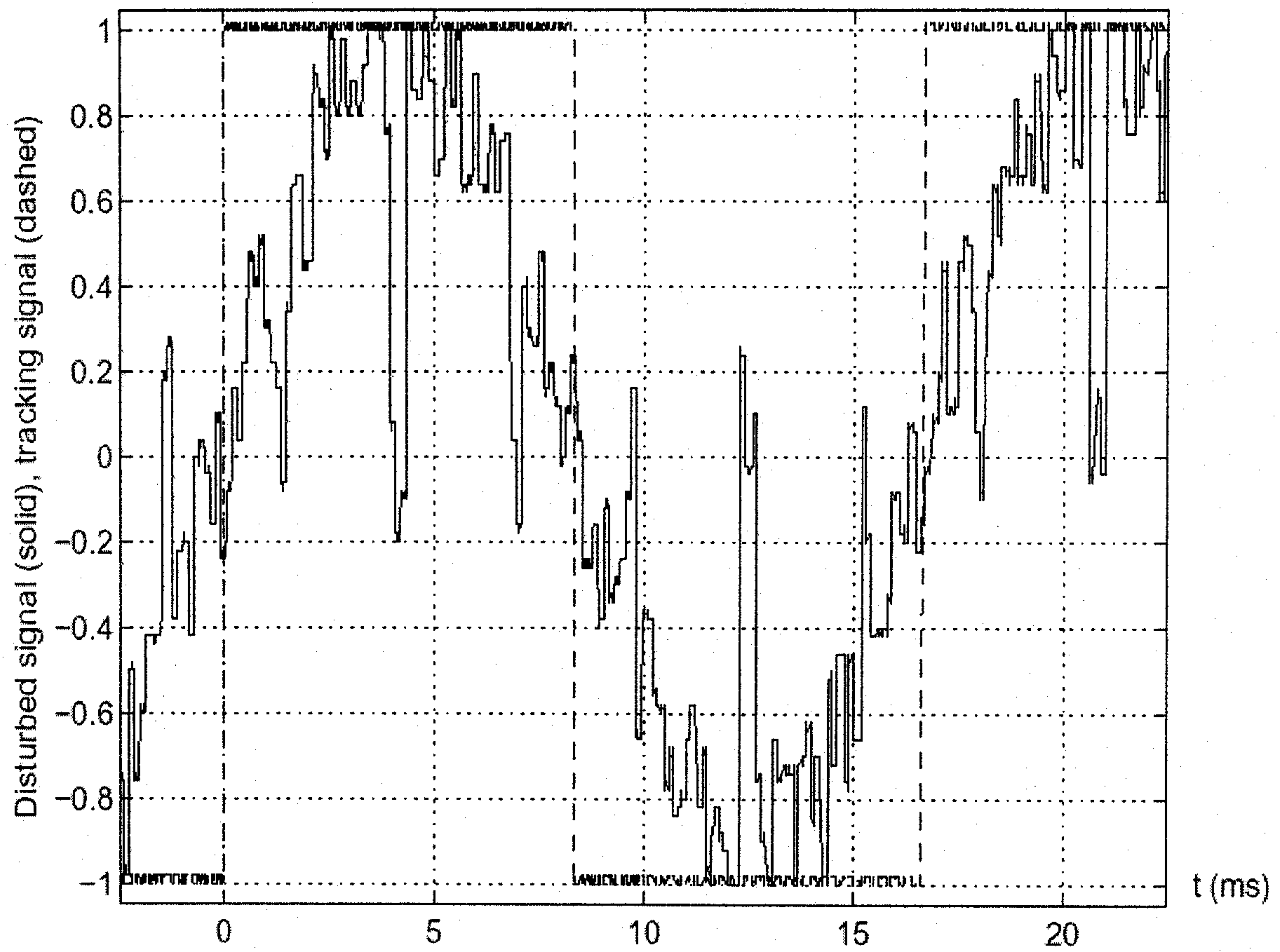


Figure 12. Network voltage with notch-type disturbance and noise.

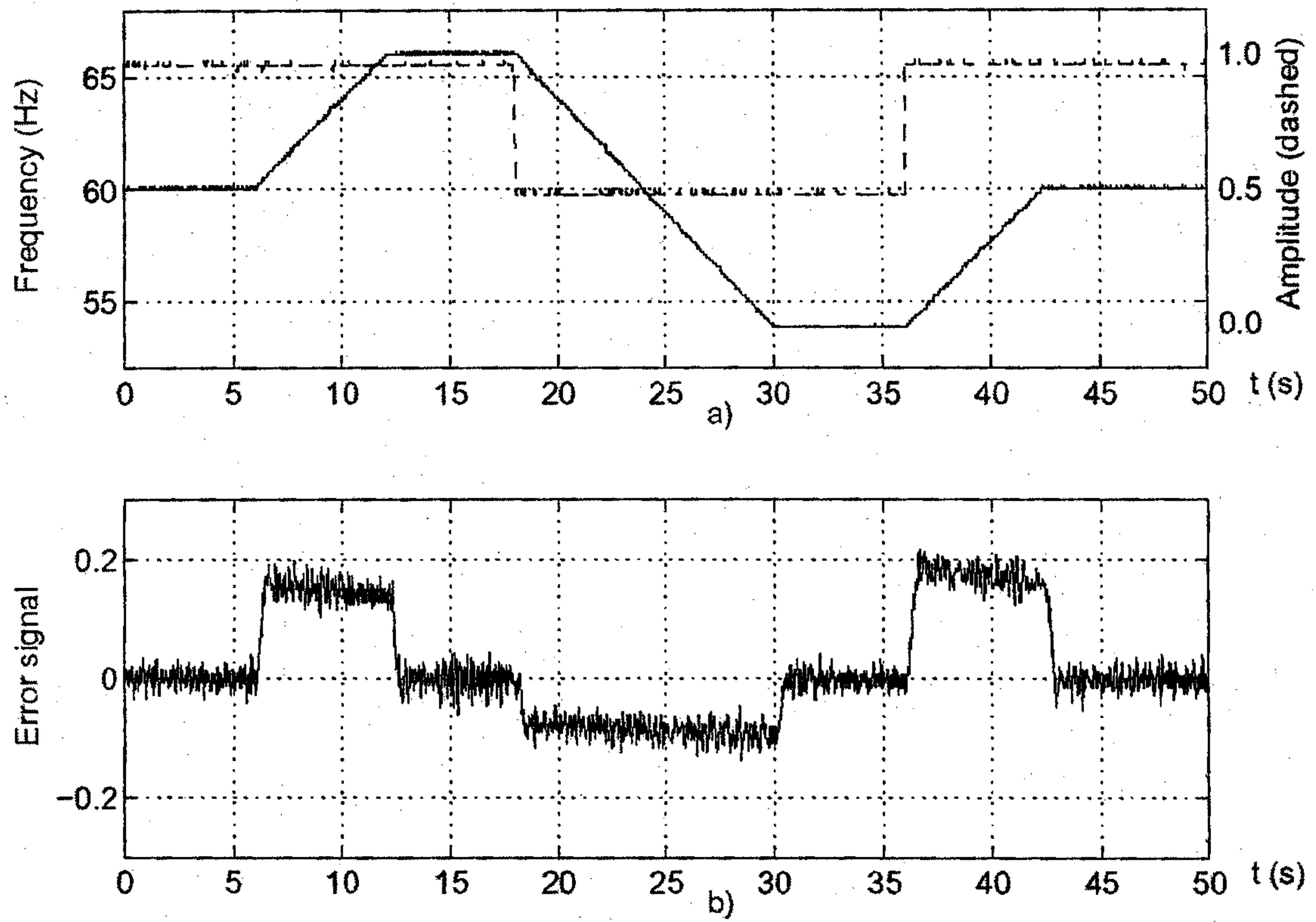


Figure 13(a) & 13(b). PLL tracking error.

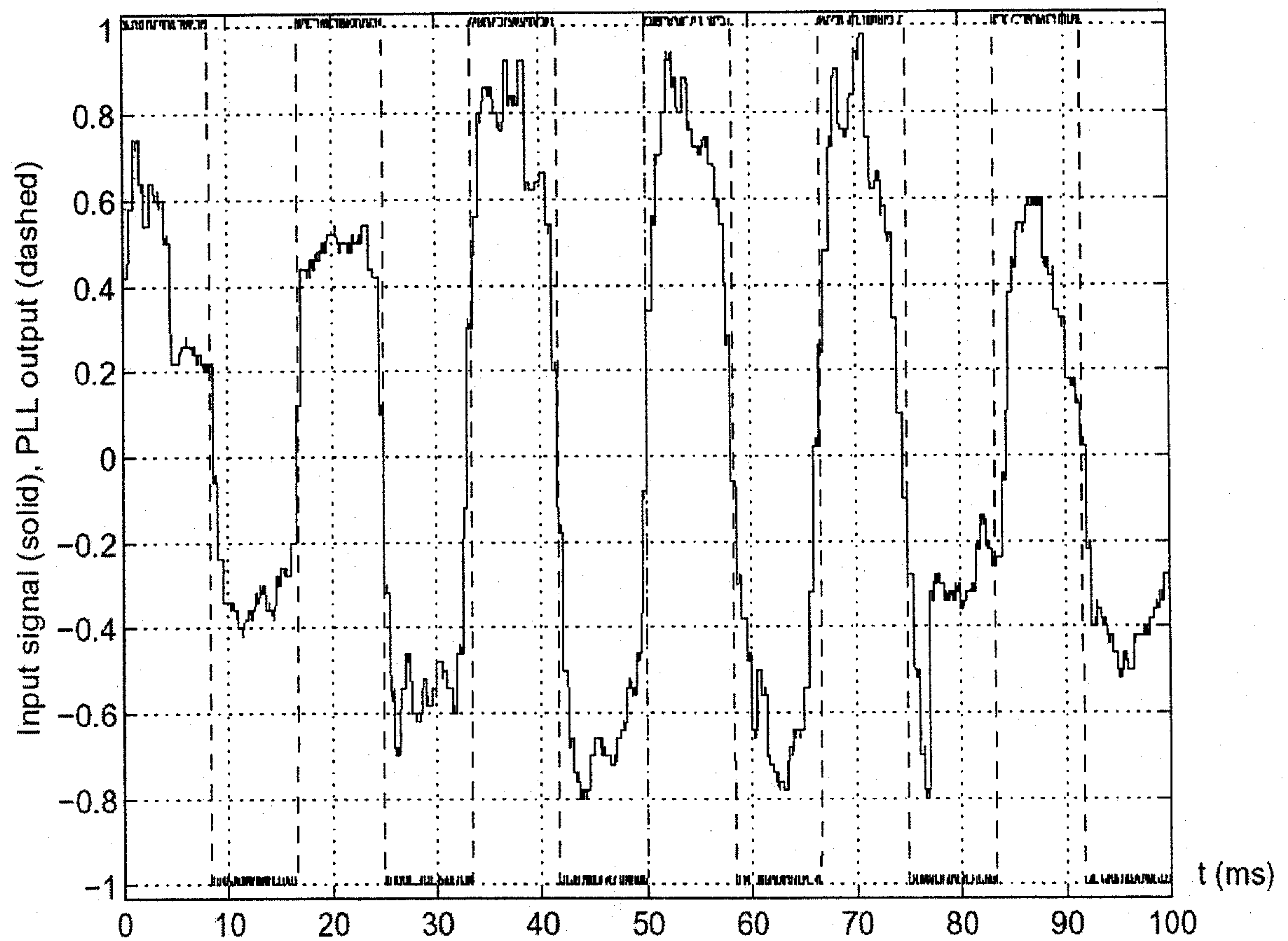
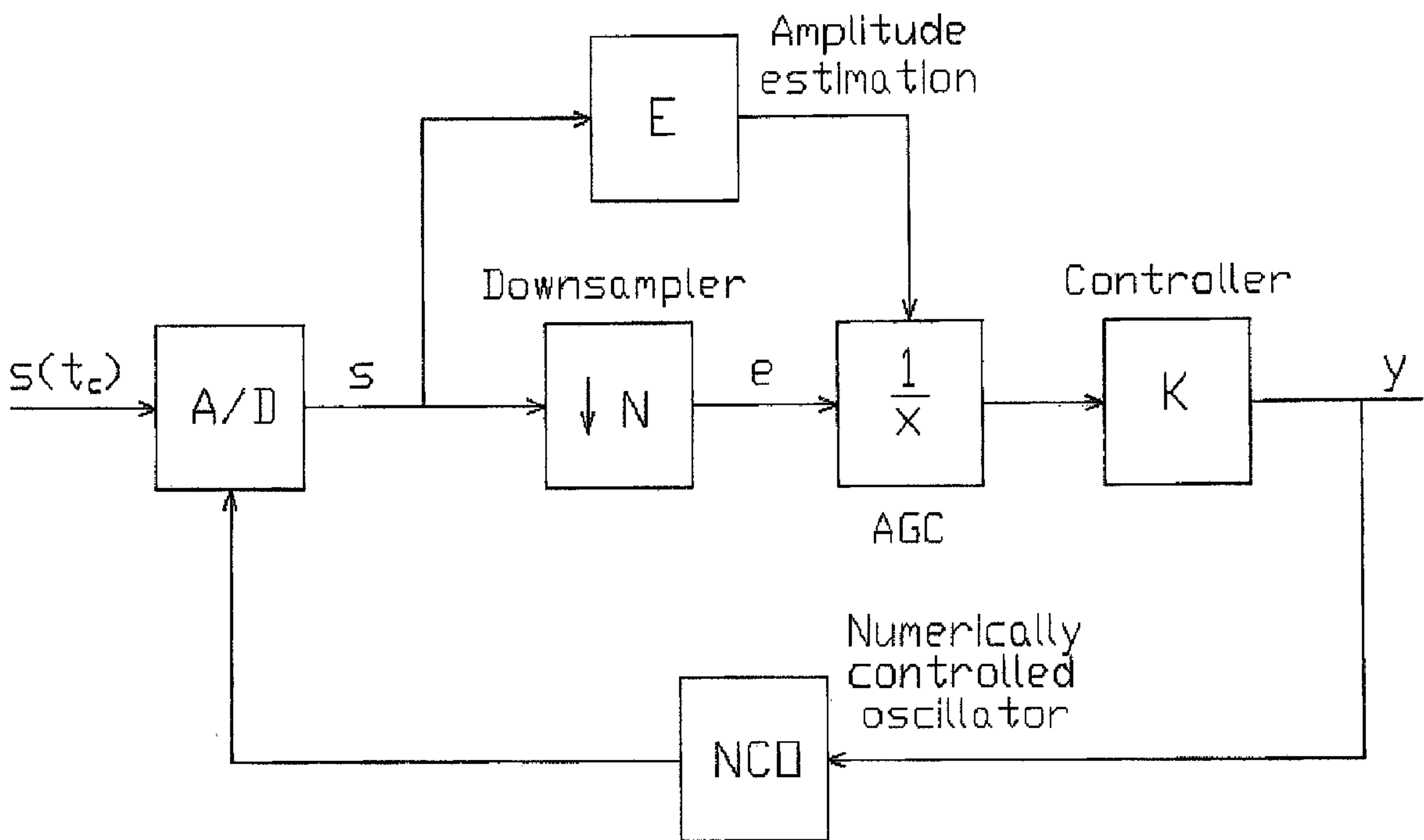


Figure 14. Estimation of the arc furnace voltage zero crossings.



PLL with Automatic Gain Control (AGC)