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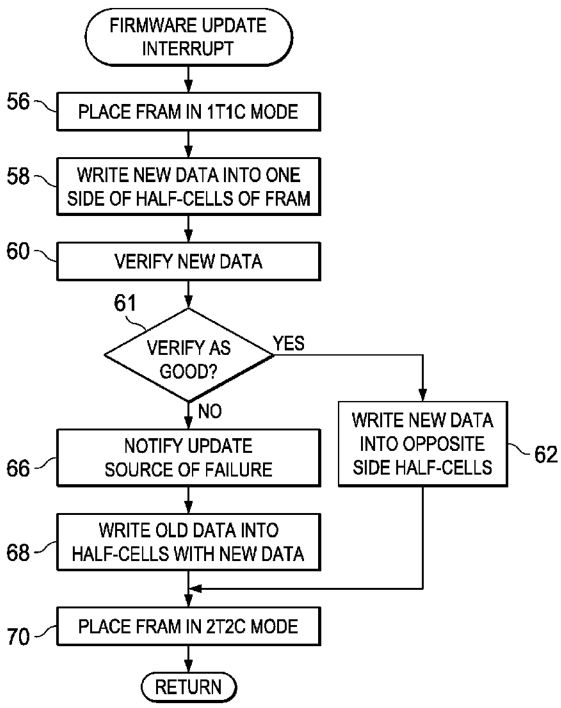

FIG. 6

(57) Abstract: In described examples, an integrated circuit includes a ferroelectric random access memory (FRAM) for storing firmware. The FRAM is constructed to selectively operate as a 2T2C FRAM memory in a normal operating mode, and as a 1T1C FRAM memory in an update mode. Updating of the stored firmware is performed by placing the FRAM in its update (1T1C) mode (56) and writing the updated code into alternate rows of the 1T1C half-cells at each of multiple memory locations (58), while the other 1T1C half-cells in the other alternate rows retain the original data. Following verification of the updated contents (60), the original data in the other half-cells are overwritten with the verified updated data (62), and the operating mode is changed back to the normal (2T2C) operating mode (70).

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FERROELECTRIC MEMORY EXPANSION FOR FIRMWARE UPDATES

BACKGROUND

[0001] This relates generally to electronic systems incorporating embedded ferroelectric memory resources, and more particularly to systems and methods of operating the same to update contents of those embedded memory resources.

[0002] Conventional metal-oxide-semiconductor (MOS) and complementary MOS (CMOS) logic and memory devices are prevalent in modern electronic systems, as they provide an excellent combination of fast switching times and low power dissipation, along with their high density and suitability for large-scale integration. However, those devices are essentially volatile, in that logic and memory circuits constructed according to these technologies do not retain their data states upon removal of bias power. Especially in mobile and miniature systems, the ability to store memory and logic states in a non-volatile fashion is desirable. As a result, various technologies for constructing non-volatile devices have recently been developed.

[0003] A recently developed technology for realizing non-volatile solid-state memory devices involves the construction of capacitors in which the dielectric material is a polarizable ferroelectric material, such as lead zirconate titanate (PZT) or strontium-bismuth-tantalate (SBT), rather than silicon dioxide or silicon nitride as typically used in non-ferroelectric capacitors. Hysteresis in the charge-vs.-voltage (Q-V) characteristic, based on the polarization state of the ferroelectric material, enables the non-volatile storage of binary states in those capacitors. In contrast, conventional MOS capacitors lose their stored charge on power-down of the device. It has been observed that ferroelectric capacitors can be constructed by processes that are largely compatible with modern CMOS integrated circuits, such as by placing the capacitors above the transistor level, between overlying levels of metal conductors.

[0004] FIG. 1 illustrates an example of a Q-V characteristic of a conventional ferroelectric capacitor. As shown, the charge (Q) stored across the conductive plates depends on the voltage applied to the plates (V), and also on the recent history of that voltage. If the voltage V applied across the capacitor plates exceeds a "coercive" voltage $+V_{\alpha}$, the capacitor polarizes into the "+1" state. According to this characteristic, after being polarized to the "+1" state, so long as voltage V remains above coercive voltage $-V_\beta$, the capacitor exhibits a stored charge of $+Q_1$. Conversely, if the voltage V applied across the capacitor plates is more negative than coercive voltage $-V_\beta$, the capacitor is polarized into the "-1" state, and will exhibit a stored charge of $-Q_2$ for applied voltage V below $+V_\alpha$.

[0005] An important characteristic of ferroelectric capacitors, for purposes of non-volatile storage in integrated circuits, is the difference in capacitance exhibited by a ferroelectric capacitor between its polarized states. The capacitance of an element refers to the ratio of stored charge to applied voltage. In the context of a ferroelectric capacitor, the change in polarization state that occurs upon application of a polarizing voltage is reflected in charge storage. For example, referring to FIG. 1, the polarization of a ferroelectric capacitor from its "-1" state to its "+1" state is reflected in a relatively high capacitance C(-1), by which polarization charge involved in the change of polarization state is retained within the capacitor as the voltage exceeds its coercive voltage V_α. By comparison, a capacitor already in its "+1" state exhibits little capacitance C(+1) due to polarization, because its ferroelectric domains are already aligned before the application of the voltage. In each case, the ferroelectric capacitor also has a linear capacitance, by virtue of its construction as parallel plates separated by a dielectric film (*i.e.*, the ferroelectric material). As will be evident from the following description, a stored logic state is read by interrogating the capacitance of ferroelectric capacitors to discern its polarized state.

[0006] Ferroelectric technology is now used to realize non-volatile solid-state read/write random access memories (RAMs). These memory resources, commonly referred to as "ferroelectric RAM", or "FeRAM", or "FRAM", are now commonplace in many electronic systems, particularly portable electronic devices and systems. FRAMs are especially attractive in implantable medical devices, such as pacemakers, defibrillators, and monitoring devices, due to the ultra-low power consumption of FRAM memory.

[0007] One approach to the implementation of FRAMs is the two-transistor, two-capacitor (2T2C) ferroelectric memory cell, in which the two ferroelectric capacitors in a cell are polarized to complementary states. FIG. 2a schematically illustrates memory cell $2_{j,k}$ of conventional 2T2C construction. In this example, cell $2_{j,k}$ resides in a row *j* and a column *k* of a memory array, and includes two ferroelectric capacitors 4a, 4b and two metal-oxide semiconductor (MOS) transistor 5a, 5b. Ferroelectric capacitors 4a, 4b are parallel-plate capacitors with ferroelectric material, such as PZT, as the dielectric; one or both of the plates may be formed in semiconductor material (e.g., a diffused region in the substrate, polysilicon) or in a metal or conductive metal compound material (e.g., a silicide, or conductive nitride). One plate of each of ferroelectric capacitors 4a, 4b is connected to plate line PL_j for row *j*. The other plate of ferroelectric capacitor 4a is connected to bit line BLT_k for column *k* via the source/drain path of p-channel transistor 5a; similarly, the second plate of ferroelectric capacitor 4b is connected to bit line BLC_k via the source/drain path of n-channel transistor 5b. The gates of transistors 5a, 5b are driven by word line WL_j for row *j* of the memory array.

[0008] In operation, ferroelectric capacitors 4a, 4b store complementary polarization states that are reflected as a differential voltage or current between bit lines BLT_k, BLC_k when read. Accordingly, in a write operation to conventional memory cell $2_{j,k}$, complementary levels are applied to bit lines BLT_k, BLC_k at a polarity corresponding to the desired data state, while word line WL_j is driven active high to turn on transistors 5a, 5b; a pulse at plate line PL_j during this state causes opposite polarization voltages to polarize capacitors 4a, 4b into the corresponding complementary polarization states. In a read operation, bit lines BLT_k, BLC_k are precharged to a selected voltage and then float, after which word line WL_j is asserted active high. A pulse at plate line PL_j causes the complementary polarization states of capacitors 4a, 4b to be reflected as a differential signal across bit lines BLT_k, BLC_k, respectively, for sensing and amplification by sense amplifier 6_k for column *k*.

[0009] FIG. 2b illustrates, in block form, a simplified arrangement of conventional memory array 5 of memory cells 2 such as constructed according to FIG. 2a. Memory arrays in actual integrated circuits are much larger than that shown in FIG. 3, so this small (4 by 4) example is provided for illustration only. In array 5 of FIG. 3, each row of cells 2 in the array is associated with a corresponding one of word lines WL_0 through WL_3 and one of plate lines PL_0 through PL_3. Each column of cells 2 share a pair of bit lines, with column 0 coupled to bit lines BLT_0, BLC_0; column 1 coupled to bit lines BLT_1, BLC_1, and so on. Sense amplifier 6_0 receives bit lines BLT_0, BLC_0, sense amplifier 6_1 receives bit lines BLT_1, BLC_1, sense amplifier 6_2 receives bit lines BLT_2, BLC_2, and sense amplifier 6_3 receives bit lines BLT_3, BLC_3. Accordingly, the energizing of word line WL_j and plate line PL_j for row *j* of cells 2 will cause the read or write (as the case may be) of data from or to cells $2_{j,0}$ through $2_{j,3}$, via bit lines pairs BLT_0, BLC_0 through BLT_3, BLC_3, respectively.

[0010] The conventional 2T2C arrangement of FIGS. 2a and 2b has been observed to provide good long term data retention because of the robust read margin resulting from the differential sense arrangement. Even if one of ferroelectric capacitors 4a, 4b in a given cell $2_{j,k}$ is weak when manufactured, or suffers a significant loss of polarization during the operating life of the device, the cell can still return the correct data state so long as the opposing capacitor retains a stronger polarized state.

[0011] In contrast, ferroelectric cells constructed in a 1T1C (one transistor, one capacitor) arrangement, similar to conventional dynamic RAM memory cells, are attractive because of their small chip area. FIG. 2c illustrates an example arrangement of a conventional 1T-1C FRAM cell 12_{jk}, which represents a single cell residing in a row *j* and a column *k* of an array of similar cells 12. Cell 12_{jk} includes ferroelectric capacitor 14 and n-channel pass transistor 15. The source/drain path of transistor 15 is connected between bit line BL_k for column *k* of the array, and the top plate of ferroelectric capacitor 14; the gate of transistor 15 is controlled by word line WL_j for row *j* of the array. The bottom plate of ferroelectric capacitor 14 is connected to plate line PL for the row, or which may be in common for all cells 12 in the array or array portion, depending on the architecture. Accordingly, 1T-1C FRAM cells are constructed similarly as conventional dynamic RAM memory cells. Sense amplifier 16_k is coupled to bit line BL_k, and operates to compare the bit line voltage developed by read current i_R to a reference voltage V_{REF} generated by a reference voltage generator, or at a "dummy" bit line as may be produced by a reference capacitor. This reference voltage V_{REF} is usually at an intermediate level between the expected voltages for the "0" and "1" data states.

[0012] In comparing the 1T1C and 2T2C FRAM cell architectures, the 1T1C cell has the advantage of increased bit density but the disadvantage of reduced read margin because of its single-ended sense relative to a reference voltage, while the 2T2C cell provides the advantage of robust data retention from complementary data storage and differential sensing, but at only about one-half the bit density.

[0013] As mentioned above, FRAM non-volatile memory has become popular for use in many electronic systems. So-called "system-on-a-chip" (SoC) devices, such as the MSP430 family of microcontrollers available from Texas Instruments Incorporated, now often include FRAM resources, particularly when used to realize sensors and controllers deployed in remote locations and thus in which power consumption is a particular concern. Zwerg et al., "An 82 mA/MHz Microcontroller with Embedded FeRAM for Energy-Harvesting Applications", *Digest of*

Technical Papers, 2011 Int'l Solid-State Circ. Conf., paper 19.2 (IEEE), pp. 334 – 36, incorporated herein by this reference, describes an example of such a microcontroller-based SoC. The networking of these and similar SoC devices according to the so-called "Internet of Things" (IoT) is becoming widespread.

[0014] Particularly in those networked implementations, FRAM is often used to store the microcontroller "firmware", including executable program code according to which the particular sensor or controller carries out its desired function. Considering the expected system life of these remotely-deployed IoT devices, SoC architectures typically include some provision for updating that system firmware, including the ability to verify the newly-received updated firmware before its installation to ensure post-update operability. In conventional architectures, a buffer in the memory space is necessary to store the updated firmware during this verification, before overwriting the existing firmware image in FRAM. This buffer requires additional memory in the SoC device, which increases the device's chip area and manufacturing cost, and potentially impacts the SoC's power consumption. In some system architectures, an additional memory device (e.g., RAM), external to the SoC device, is provided as a buffer for storing updated firmware before validation. While avoiding the cost of implementing the additional buffer in the SoC device, this external buffer increases cost and complexity of the overall system.

[0015] As further background, conventional FRAM architectures exist in which the memory cells can be selectively operated in either of the 2T2C or 1T1C modes. An example of such an architecture is described in Patent No. U.S. 5,571,628, incorporated herein by reference. In the example of Patent No. U.S. 5,571,628, a control signal selects whether an additional row address line is to be decoded, in which case the FRAM cells are operated (*i.e.*, written and read) as 1T1C cells. For a read cycle in the 1T1C mode, a dummy word line is activated to couple a reference memory cell capacitor to the opposite bit line from that to which the addressed 1T1C cell is coupled; the sense amplifier then senses the data state of the addressed 1T1C cell by comparison with the bit line voltage produced by the reference memory cell capacitor. Conversely, for a read cycle in the 2T2C mode, the dummy word line is not activated; rather, two word lines are activated to couple cells in adjacent rows and the same column to opposing bit lines, for differential sensing by the sense amplifier.

SUMMARY

[0016] In described examples, a large-scale integrated circuit includes programmable logic whose firmware is able to be updated without requiring an additional buffer. In a method of updating the firmware of such integrated circuit, the method is performed in a manner that does not require use of an additional buffer to store the updated content before verification. Such circuit and method provides the ability to so update the firmware using non-volatile read/write memory.

[0017] In described examples, an integrated circuit includes a ferroelectric random access memory (FRAM) resource for storing executable code for the programmable logic, and contents of the FRAM are updated by logic circuitry and a corresponding method. The FRAM is constructed to selectively operate as a 2T2C FRAM memory in a normal operating mode and as a 1T1C FRAM memory in an update mode. To update the FRAM contents, its operating mode is changed to the update (1T1C) mode by the memory controller logic, and updated data are written into one of the 1T1C half-cells at each of multiple memory locations, while the original data are stored in the other 1T1C half-cell at each of those memory locations. Following verification of the updated contents, the original data in the complementary half-cells are overwritten with the verified updated data, and the operating mode is changed back to the normal (2T2C) operating mode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1 is a plot of a charge-vs.-voltage characteristic of a conventional ferroelectric capacitor.

[0019] FIG. 2a is an electrical diagram, in schematic and block form, illustrating a conventional 2T-2C ferroelectric memory cell and its operation.

[0020] FIG. 2b is an electrical diagram, in block form, of the architecture of a conventional ferroelectric random access memory (FRAM) array.

[0021] FIG. 2c is an electrical diagram, in schematic and block form, illustrating a conventional 1T-1C ferroelectric memory cell and its operation.

[0022] FIG. 3 is an electrical diagram, in block form, of the architecture of an SoC device constructed according to embodiments.

[0023] FIG. 4 is an electrical diagram, in block form, of the architecture of an FRAM subsystem in the SoC device of FIG. 3, constructed according to embodiments.

[0024] FIG. 5 is an electrical diagram, in schematic and block form, illustrating an arrangement of a portion of the FRAM array in the architecture of FIG. 3, according to an embodiment.

[0025] FIG. 6 is a flow diagram illustrating the operation of updating the contents of the FRAM array according to an embodiment.

[0026] FIGS. 7a through 7f are block diagrams illustrating contents of the FRAM array in the architecture of FIG. 3 at various stages during the process of FIG. 6 according to that embodiment.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0027] Example embodiments may be implemented into a large-scale integrated circuit, such as a so-called “system on a chip” or “SoC”. Also, example embodiments may be beneficially implemented in other applications and for other uses.

[0028] FIG. 3 illustrates, in block diagram form, the generalized architecture of SoC 400 constructed according to these embodiments. In this example, programmable logic serving as the central processing unit (CPU) of SoC 400 is provided by CPU 430, which may be a microprocessor, such as an ARM processor, or a 16-bit RISC processor core as used in the MSP430 family of microcontrollers available from Texas Instruments Incorporated. SoC 400 may be constructed to include multiple CPUs 430, which may be of the same type as one another or which may be processors of other types such as generic programmable processors, digital signal processors (DSPs) or other application-specific or customized logic, including fixed sequence generators, as appropriate for the particular function of SoC 400. As shown in FIG. 3, CPU 430 may include one or more banks of registers, including control registers 431.

[0029] Memory resources in SoC 400 are provided by ferroelectric random access memory (FRAM) 410, read-only memory (ROM) 432, and random access memory 412, a portion of each of which is accessible to CPU 430 through main address bus MAB and main data bus MDB. FRAM 410, ROM 432, and RAM 412 are shown in FIG. 3 as unitary blocks, but these memory resources may alternatively be realized as multiple memory blocks or arrays. For example, RAM 412 may be realized by any one or more of a number of memory cell types and arrangements, such as static RAM (SRAM) and dynamic RAM (DRAM). FRAM 410 in this embodiment is coupled to buses MAB, MDB via FRAM controller logic 411, the function and operation of which in connection with the updating of the contents of FRAM 410 will be described in detail below. Because of non-volatility and low power consumption, FRAM 410 is well-suited for storing the "firmware" of SoC 400, such firmware constituting the executable program code for one or more applications carried out by SoC 400 in its normal operation. This firmware will be updated in the examples described in this specification, illustrating the operation of these embodiments. ROM 432 in this architecture serves as "bootloader" memory ("BSL"), and as such stores program code that is executable by CPU 430.

[0030] In addition to the various memory resources 410, 412, 432 that are accessible via address bus MAB and data bus MDB, many of the circuit functions within SoC 400 may themselves include local memory resources that are not directly accessible to CPU 430. As noted above in connection with control registers 431, CPU 430 itself may also include local memory resources, such as one or more levels of cache memory.

[0031] Various peripheral functions of SoC 400 may be also coupled to buses MAB, MDB, to be accessible to CPU 430 and one another. In the architecture of FIG. 3, these peripherals include direct memory access (DMA) engine 433 for providing DMA access to and from the various memory resources of SoC 400, various signal processing functions such as analog-to-digital (ADC) and digital-to-analog (DAC) converters, communications ports, timers, serial and other interface functions. These various peripheral functions may be within the address space of SoC 400, as suggested by their accessibility via buses MAB, MDB; alternatively, one or more of these or other functions may be accessible to CPU 430 directly or via other functional circuitry. Security features may also be realized within SoC 400, such as by secure state machine 448 in combination with stored security parameters in one or more secure memory resources, to execute features such as preventing data reads or writes to areas of memory that are specified to be secure areas unless a secure mode is enabled. SoC 400 also includes other functions, such as its clock system, and emulation system 420 and JTAG interface 421 for debug and emulation.

[0032] SoC 400 may include additional or alternative functions to those shown in FIG. 3, or may have its functions arranged according to a different architecture from that shown.

[0033] FIG. 4 shows the architecture of an FRAM subsystem according to an embodiment, such as incorporated into the architecture of SoC 400 of FIG. 3. This architecture includes those functions involved in the updating of the contents of FRAM 410, particularly for the example of the updating of firmware stored in FRAM 410. FRAM 410 in this architecture is coupled to receive memory addresses from FRAM controller 411, and to communicate data and control signals to and from FRAM controller 411. FRAM controller 411 is coupled to receive addresses from CPU 430 via main address bus MAB, and to communicate data with CPU 430 via main data bus MDB. CPU 430 may also communicate control information to FRAM controller 411 via buses MAB, MDB, such as by writing that control information to memory addresses corresponding to control registers within FRAM controller 411. As will be described further below, FRAM controller 411 may also include internal memory in the form of cache 411c, as shown in FIG. 4. This cache 411c may be used in the updating of FRAM 410 and a higher-level cache in SoC 400 during its normal operation (e.g., as an instruction cache for firmware instructions already retrieved by FRAM controller 410 from FRAM 410).

[0034] According to this embodiment, the control signals communicated from FRAM controller 411 to FRAM 410 include one or more control signals indicating the particular operating mode of FRAM 410. FRAM 410 includes an array of ferroelectric memory cells arranged in rows and columns in the conventional fashion, such as discussed above relative to FIG. 2b, along with sense amplifiers, address decoders, and other conventional peripheral circuitry (to the extent not included within FRAM controller 411 in this example). However, in this embodiment, FRAM 410 is constructed so that its memory cells can operate either as two-transistor two-capacitor (2T2C) ferroelectric cells or as one-transistor one-capacitor (1T1C) ferroelectric cells. In a general sense, as will be discussed in more detail below, FRAM 410 will operate as a 2T2C ferroelectric memory in a normal operating mode of SoC 400 to obtain the data retention and excellent read margin provided by that cell architecture, and will operate as a 1T1C memory in an update mode to temporarily enjoy the doubled capacity provided by that cell architecture.

[0035] As mentioned hereinabove, conventional FRAM array and peripheral circuitry can selectively operate in either the 2T2C or 1T1C mode. FIG. 5 illustrates an example following the approach of the above-incorporated Patent No. U.S. 5,751,628, which has a construction useful in connection with this embodiment. The ability to select between the two operating modes may be implemented in various ways. In this example, FIG. 5 illustrates a portion of a column *k* in an array of *m* rows and *n* columns of 2T2C FRAM cells $2_{j,k}$, where *j* indicates the one of the *m* 2T2C rows in which a given cell $2_{j,k}$ resides. The full array will include other columns of similarly arranged FRAM cells. Each 2T2C cell $2_{j,k}$ is shown as having first and second half-cells, each including a ferroelectric capacitor coupled between plate line PL and a pass transistor in the conventional manner. These two half-cells in this example will be referred to as left and right half-cells $2_{j,k}$[L] and $2_{j,k}$[R], respectively. Complementary (in the 2T2C sense) bit lines BLT_k, BLC_k are coupled to the pass transistor of the left-hand and right-hand cells 2 in column k, and to sense amplifier 46_k for column k. Sense amplifier 46_k is a conventional differential sense amplifier, which in a read operation from column k forwards a data state signal (not shown) responsive to the comparison of the voltages at its bit lines BLT_k, BLC_k. The writing of data into cells 2 of FRAM 410 is performed in the conventional manner, according to the particular mode (2T2C or 1T1C) of operation.

[0036] In this construction, the pass transistors of the left half-cell $2_{j,k}$[L] and the right half-cell $2_{j,k}$[R] receive separate word lines at their gate electrodes. For example, left half-cell $2_{0,k}$[L] receives word line WL_0 from row decoder 40, while right half-cell $2_{0,k}$[R] receives word line WL_0. Similarly, the left half-cells $2_{j,k}$[L] receive even-numbered word lines WL_2, WL_4, …, WL_{2m-4}, WL_{2m-2}, while the right half-cells $2_{j,k}$[R] receive odd-numbered word lines WL_3, WL_5, …, WL_{2m-3}, WL_{2m-1} from row decoder 40. FRAM controller 411 provides to row decoder 40 a row address selecting one of the m rows of 2T2C cells, and having an additional, least significant, bit that can selects between the left half-cell and right half-cell of the selected 2T2C row. FRAM controller 411 also provides, to row decoder 40 in this example, a control signal $1T1C/\overline{2T2C}$ indicating whether FRAM 410 is to operate in its 1T1C or 2T2C modes. The configuration of the FRAM subsystem of FIG. 4 is set by CPU 430 storing the appropriate values in control registers of FRAM controller 411, in response to which FRAM controller 411 issues the appropriate logic state of control signal $1T1C/\overline{2T2C}$ to FRAM 410 for the desired operating mode. Responsive to control signal $1T1C/\overline{2T2C}$ indicating operation in the 2T2C mode, an LSB mask 41 is set in row decoder 40 such that the least significant bit of the row address is ignored in the generation of the word line signals, and both word lines (e.g., word lines WL_0 and WL_1 for the first row j=0) are energized in the access cycle. Conversely, in the 1T1C mode, LSB mask 41 will not be enabled, and the least significant bit of the row address will be included in the selection of a single word line. The desired configuration and operating mode of FRAM 410 will be readily selectable in this manner, or according to other conventional approaches.

[0037] FRAM 410 according to this example implementation also includes reference voltage generator 44 for use in the 1T1C mode. Reference voltage generator 44 may be a conventional reference voltage circuit that produces a stable output voltage at a level between the expected "0" bit line voltage and the expected "1" bit line voltage of FRAM 410; alternatively, as described in the above-incorporated Patent No. U.S. 5,751,628, reference voltage 44 may be constructed as a pair of ferroelectric capacitors, either sized or polarized to produce a bit line voltage at the desired reference level. Pass transistors 42_0, 42_1 couple reference voltage generator 44 to bit lines BLT_k, BLC_k, respectively, when turned on by dummy word lines DWL0, DWL1, respectively, from row decoder 40. In this example, row decoder 40 energizes dummy word line DWL0 to connect reference voltage generator 44 to bit line BLT_k responsive to the LSB of the row address selecting a right half-cell $2_{j,k}$[R] (*i.e.*, LSB = 1), and energizes dummy word line DWL1 to connect reference voltage generator 44 to bit line BLC_k responsive to the LSB of the row address selecting a left half-cell $2_{j,k}$[L] (*i.e.*, LSB = 0). In this way, sense amplifier 46_k performs single-ended sensing of a selected half-cell in column *k* with FRAM 410 in the 1T1C mode.

[0038] Referring to FIGS. 6 and 7a through 7f, the operation of an FRAM subsystem in an SoC device, such as SoC 400, according to an embodiment will now be described. In particular, this example of the operation of this FRAM subsystem will be described in the context of the updating of firmware for SoC 400 as stored in FRAM 410, because this embodiment is especially beneficial when used in such an application. Also, this same process and operation are useful in updating contents of the FRAM memory other than the system firmware. In the architecture of FIG. 4, this updating process will be executed and controlled largely by FRAM controller 411, at the initiation and direction of CPU 430, such as in an interrupt handler routine that is invoked by an interrupt corresponding to the communication of an update. The particular logic circuits responsible for specific tasks and processes involved in the update may vary from this implementation, depending on the particular architecture of the device and its FRAM resource. This embodiment is readily adaptable to such applications and alternative architectures.

[0039] In the firmware update context, an original or other prior version of the SoC firmware is initially stored in FRAM 410, and is used for normal system operation in which application software is executed or otherwise carried out by SoC 400, under that original firmware or earlier update. Usually, this normal operation of SoC 400 is performed with FRAM 410 in its 2T2C mode, by FRAM controller 411 issuing control signal $1T1C/\overline{2T2C}$ at the appropriate level in response to CPU 430 having set the contents of the appropriate control register in FRAM controller 411 accordingly. As mentioned above, the operation of FRAM 410 in its 2T2C mode is suitable for long-term storage, with optimal read margin and robust data retention performance.

[0040] FIG. 7a illustrates an example of the contents of a portion of FRAM 410 containing the original firmware contents, and during its normal operation before receipt of a firmware update. In this example, eight rows of 2T2C cells in FRAM 410 are shown as storing the original firmware code. In the 2T2C mode of FRAM 410 constructed as described above relative to FIG. 5, these eight rows correspond to the 2T2C row addresses 000x through 111x, where the "x" indicates that the least significant bit that selects between the left half-cells and right-half cells is ignored (*i.e.*, "masked" by LSB mask 41 of row decoder 40). Because of the differential operation of 2T2C FRAM cells as described above, the polarization state of each right half-cell $2_{j,k}$[R] will be the logical complement of the state of its corresponding left half-cell $2_{j,k}$[L]. Accordingly, the original firmware code may be stored as two copies in FRAM 410, so that: one copy is stored in the left half-cells; and the other copy is stored as complementary data in the right half-cells.

[0041] Conventionally, SoC 400 is able to receive updated software, including updates to the firmware stored in FRAM 410, either asynchronously or upon initiation of a firmware update ("flash") by a user or from a host network node. In this embodiment, upon SoC 400 receiving an indication of updated firmware, a firmware update interrupt is invoked, and the interrupt handler routine of FIG. 6 according to this embodiment is executed.

[0042] According to this embodiment, the firmware update interrupt handler begins with process 56, in which FRAM controller 411 places FRAM 410 into its update mode. In these embodiments, the update mode entered in process 56 causes FRAM 410 to consider and operate its cells 2 as 1T1C FRAM cells, and operate row decoder 40, sense amplifiers 46, and other peripheral circuitry of FRAM 410 as appropriate for a 1T1C FRAM. For example, in the architecture of FIG. 5, LSB mask 41 in row decoder 40 is disabled, allowing the activation of one of dummy word lines DWL0, DWL1 in each cycle in response to the value of the row address least significant bit. Referring to FIG. 7b, the 2T2C rows of FRAM 410 as shown in FIG. 7a are now considered as pairs of half-rows, or 1T1C rows that are selectable based on the state of the least significant row address bit, and that store complementary data relative to one another. For example, 1T1C row address 0000 corresponds to the left half-cells $2_{0,k}$[L] of the first 2T2C row j=000x, and 1T1C row address 0001 corresponds to the right half-cells $2_{0,k}$[R] of that first 2T2C row j=000x. The data stored in 1T1C row 0001 is the logical complement of that stored in 1T1C row 0000; this complementary data by alternating 1T1C rows continues throughout FRAM 410 as shown in FIG. 7b. Essentially, the memory capacity of FRAM 410 is doubled in this 1T1C mode as compared with the 2T2C mode, but at this point in the process is storing two copies of the same data.

[0043] Optionally, before the placing of FRAM 410 into the 1T1C mode in process 56, the original data stored in FRAM 410 may be "refreshed" by reading and then rewriting the same data back into each cell in the array. This refreshing of the contents of FRAM 410 may be useful to re-establish a full polarization state for each bit of the stored data, considering that subsequent operations will be reading these stored contents of single-ended sensing in the 1T1C mode. If desired, this refreshing may be performed at an elevated power supply voltage, such as used in some FRAM test operations and modes, to boost the polarization states for the stored data.

[0044] In process 58, the new data corresponding to the updated firmware for SoC 400 are received and written into the half-cells on one side of each FRAM cell 2 in FRAM 410. In this example, these updated data are stored in the right half-cells of FRAM 410, in the 1T1C rows having a "1" in the least significant row address bit (*i.e.*, at row addresses $a_3a_2a_1$1), as shown in FIG. 7c. The effective doubling of the capacity of FRAM 410 by the switching into the 1T1C mode provides essentially a full-size buffer to receive firmware updates and other new data, without requiring additional memory cells in SoC 400 for that buffer. The updated firmware does not necessarily fill the available buffer provided by the alternate 1T1C rows.

[0045] The writing of the updated data into the alternate 1T1C rows in process 58 may be performed in various ways. In this example, because the updated data are written into the right half-cells associated with the complementary bit line BLC_k of each column k, these updated data may be written as the logical complement of the actual updated data. Alternatively, the data may be written into the right half-cells as the true data states (*i.e.*, as received). The updated data may instead be written into the left half-cells in process 58, and the earlier version retained in the right half-cells. In any case, subsequent processes will comprehend the true or complement states of these data. Also, the actual write cycles of process 58 may be performed at an elevated power supply voltage, such as used in some FRAM test operations and modes, to boost the polarization states for the stored data in light of the reduced read margin inherently provided by 1T1C FRAM cells relative to 2T2C cells.

[0046] Following the writing of the updated data (e.g., firmware) to alternate 1T1C rows in process 58, these updated data are then verified by CPU 430 in the appropriate manner in process 60 to ensure that the updated data were accurately received and stored. According to this embodiment, verification process 60 will be performed by CPU 430 or another logic circuit in SoC 400 executing some type of numerical data verification routine on the stored updated data. Various conventional numerical data verification techniques (such as evaluation of a cyclic redundancy check (CRC), hashes, cryptographic hashes, and check sums) are useful in process 60. This verification will usually involve the retrieval by FRAM controller 411 of the updated data from the alternate rows (row addresses $a_3a_2a_11$ of FIG. 7c) in which it was stored in process 58, along with the execution of the appropriate verification calculations by CPU 430 or other computational logic in SoC 400, as desired.

[0047] Decision 61 determines whether the verification of process 60 was successful, indicating that the updated data written into the alternate rows of FRAM 410 is free of errors (or at least may be corrected using conventional error correction) and may be trusted as true and accurate. If so (decision 61 is "yes"), these updated data are copied into the paired alternate rows of FRAM 410 in process 62, overwriting the original data in those locations. FRAM 410 is still in its 1T1C update mode for this process 62. As shown in FIG. 7d, the overwriting of process 62 retrieves the data stored in the right half-cells of a given 2T2C row (e.g., row address 0001) and writes those same data into the left half-cells of the same 2T2C row (e.g., into row address 0000). This overwriting of process 62 is performed for all of the other rows in FRAM 410 that contain the updated firmware or other data. In this example, the contents at each row address $a_3a_2a_11$ are copied into the cells at its paired row address $a_3a_2a_10$. Preferably, the overwriting of process 62 writes the logical complement of the updated data into the corresponding alternate 1T1C row, such that the data stored in row $a_3a_2a_10$ are the logical complement of the data stored in its companion row $a_3a_2a_11$. For the architecture of FIG. 5, it will be convenient for the polarity of the complement stored data to be consistent with the convention that the left half-cells are associated with the "true" bit lines BLT_k and the right half-cells are associated with the "complement" bit lines BLC_k. Also, the actual write cycles of process 62 may be performed at an elevated power supply voltage, such as used in some FRAM test operations and modes, to boost the polarization states for the stored data, considering the reduced read margin inherently provided by 1T1C FRAM cells relative to 2T2C cells.

[0048] The copying of the updated data from the alternate 1T1C rows (e.g., addresses $a_3a_2a_1 1$) into the paired alternate row addresses ($a_3a_2a_1 0$) in process 62 may be performed by hardware functions in SoC 400. For example, referring to the architecture of FIG. 4, one hardware approach for performing this overwriting is to use FRAM controller 411 to read FRAM 410 and rewrite the complementary data back into FRAM 410 without involving CPU 430. In this approach, cache 411c may be used to temporarily store the contents retrieved from FRAM 410 in process 62, thus allowing the read and write of larger blocks of data from and to FRAM 410. Another hardware-based approach may use DMA engine 433 to retrieve the contents from the alternate 1T1C rows (e.g., addresses $a_3a_2a_1 1$) of FRAM 410 and then rewrite those contents into the paired alternate row addresses ($a_3a_2a_1 0$), without involving CPU 430. Alternatively, process 62 may be performed by CPU 430 executing software instructions, such as fetched from BSL ROM 432 or from FRAM 412 itself, to carry out the reads and writes involved in copying the contents from alternate rows into their corresponding paired rows. The appropriate one of these and other approaches will be readily implementable, including hybrids of these and other hardware and software-based techniques, as appropriate for particular applications and architectures.

[0049] Following the copying of updated data performed in process 62, the updating process completes according to this embodiment by FRAM controller 411 issuing control signal $1T1C/\overline{2T2C}$ at the appropriate level to place FRAM 410 into the 2T2C mode in process 70, following which a return from the interrupt is performed, and operation in the normal operating mode commences, under the updated firmware. Again, with FRAM 410 in the 2T2C mode, its cells 2 are then accessed on a row-by-row basis by row addresses $a_3a_2a_1x$, in which the least significant bit is masked by LSB mask 41 of row decoder 40, and thus ignored in the decoding of the row address in this 2T2C mode. Execution of the appropriate applications of SoC 400 are then again carried out.

[0050] By comparison, if the verification of the updated data (e.g., firmware) performed in process 60 is unsuccessful, decision 61 returns a “no” result, indicating the detection of one or more uncorrectable errors in the updated firmware. Such errors may occur in either the communication of the update over a network link, or in the storage or retention of the updated data by FRAM 410. In this event, process 66 is then executed to notify the source of the update of this failure, so that the update may be retransmitted if desired. The updated data stored in alternate rows of FRAM 410 are then considered as invalid, and will not be copied over from the alternate 1T1C rows (e.g., addresses $a_3a_2a_1 1$) of FRAM 410 into the paired alternate row addresses ($a_3a_2a_1 0$). Rather, the old data are copied over from the 1T1C rows of FRAM 410 storing that earlier version (e.g., from row addresses $a_3a_2a_1 0$) into the cells at the alternate row addresses ($a_3a_2a_1 1$) that received the failed update, in process 68. FRAM 410 remains in the 1T1C update mode for this process 68. The particular data states written in process 68 will again be complementary to those of the corresponding addresses from which the old data is retrieved, consistent with the differential data storage and sensing of 2T2C FRAMs described above. This overwriting of process 68 may be performed at an elevated voltage, as described above, to optimize reliability of the stored data, and may be performed by either particular hardware or DMA logic in SoC 400 or by CPU 430 or other logic circuitry executing software routines for performing this process 68. FIG. 7f illustrates the overwriting of the old data in this process 68. Following the replacement of the earlier version of the stored data as performed in this process 68, FRAM controller 411 issues the control signal $1T1C/\overline{2T2C}$ at the appropriate level to place FRAM 410 into the 2T2C mode in process 70, and a return from the firmware update interrupt handler is carried out. Normal operation of SoC 400 can then continue, awaiting a resend of the updated firmware or other data from the source end if such is performed.

[0051] These embodiments provide the ability to efficiently receive and verify updated firmware and other program code or data in an integrated circuit including embedded non-volatile memory. This ability is provided by temporarily reconfiguring ferroelectric memory from its 2T2C operating mode into a double-capacity, but less robust, 1T1C operating mode, for the time required to verify and copy the received updated data. This approach retains the robust read margin performance and excellent data retention provided by the differential data storage and sensing of 2T2C FRAM memory, which is well-suited for storing system software routines commonly contained within system firmware, while the doubled bit density of 1T1C FRAM memory is used to advantage in the update and verify process. Additional buffers, either in the integrated circuit itself or as an external memory device in the overall system, for receiving firmware updates through verification are therefore not necessary, reducing the cost and power consumption of the large-scale integrated circuit and the system in which it is implemented.

[0052] As evident from this specification, these embodiments are described above as constructed using ferroelectric memory technology. Alternatively, these embodiments may alternatively be implemented in memories of a similar structure, but using a non-volatile storage technology other than the polarization of ferroelectric material. For example, these embodiments may be realized using memory cells that include a pair of magnetorestrictive random access memory (MRAM) storage elements coupled to separate conductors (e.g., bit lines) for differential sensing in one mode, but that in another operating mode may be separately written and sensed via those bit lines.

[0053] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A method of updating content stored in a ferroelectric random access memory (FRAM) array in an integrated circuit, the FRAM array including memory cells arranged in rows and columns, each memory cell of the FRAM array operable as two-transistor two-capacitor (2T2C) memory cells in a normal operating mode, and as first and second one-transistor one-capacitor (1T1C) half-cells in an update mode, the method comprising:

storing a first data set as complementary polarization states in each of a plurality of the memory cells;

placing the FRAM array into the update mode;

writing a second data set in the second half-cell of each of a selected plurality of the memory cells;

verifying the second data set;

responsive to successfully verifying the second data set, writing the second data set into the first half-cell of each of the selected plurality of memory cells; and

then placing the FRAM array into the normal operating mode.

2. The method of claim 1, further comprising: responsive to the verifying step indicating an error in the second data set, writing the first data set into the second half-cell of each of the selected plurality of memory cells.

3. The method of claim 2, wherein the verifying step includes: reading the second data set from the second half-cells of the selected plurality of memory cells; and executing a numerical data verification on the second data set as read.

4. The method of claim 2, further comprising: receiving the second data set from an update source over a network link; and responsive to the verifying step indicating an error in the second data set, notifying the update source of a failed verification.

5. The method of claim 1, further comprising: in the normal operating mode, selecting a row of memory cells responsive to a row address; and sensing the contents of one or more memory cells in the selected row.

6. The method of claim 5, wherein: for each row of memory cells, the first half-cells in the row are associated with a first row address value, and the second half-cells in the row are associated with a second row address value differing from the first row address value by a single

row address bit; and the single row address bit is masked in the selecting step in the normal operating mode.

7. The method of claim 6, wherein the sensing step includes: sensing a differential signal between first and second bit lines coupled to the first and second half-cells, respectively, of the one or more memory cells in the selected row.

8. The method of claim 6, wherein:

the verifying step includes: reading the second data set from the second half-cells of the selected plurality of memory cells; and executing a numerical data verification on the second data set as read; and

the reading step includes: selecting the second half-cells in a row of memory cells corresponding to a row address including the single row address bit; and comparing a signal at a second bit line coupled to the second half-cell of one or more of memory cells in the selected row with a reference voltage.

9. The method of claim 5, wherein contents of the FRAM memory correspond to executable program instructions, and further comprising: operating programmable logic to execute a program instruction corresponding to the sensed contents of the one or more memory cells.

10. An integrated circuit, comprising:

a ferroelectric random access memory (FRAM) operable as a two-transistor two-capacitor (2T2C) memory in a normal operating mode, and as a one-transistor one-capacitor (1T1C) memory in an update mode, including: an array of memory cells arranged in rows and columns, the memory cells in each column coupled to first and second bit lines, and each memory cell in the array including first and second half-cells, each including a ferroelectric capacitor and a pass transistor; and a plurality of sense amplifiers, each associated with a column of memory cells and coupled to the first and second bit lines for that column; and

logic circuitry for controlling the FRAM to update its contents by performing a sequence of operations including: storing a first data set as complementary polarization states in each of a plurality of the memory cells; placing the FRAM array into the update mode; writing a second data set in the second half-cell of each of a selected plurality of the memory cells; verifying the second data set; responsive to successfully verifying the second data set, writing the second data set into the first half-cell of each of the selected plurality of memory cells; and then placing the FRAM array into the normal operating mode.

11. The integrated circuit of claim 10, wherein:

the FRAM further includes decode circuitry for decoding a row address value and energizing a word line for a row of the array of memory cells responsive to the row address value;

for each row of memory cells, the pass transistor of each of the first half-cells in that row couples a plate of its ferroelectric capacitor to the first bit line responsive to a first word line signal, associated with a first row address value, shared among the first half-cells of the memory cells in the row;

for each row of memory cells, the pass transistor of each of the second half-cells in that row couples a plate of its ferroelectric capacitor to the second bit line responsive to a second word line signal, associated with a second row address value, shared among the second half-cells of the memory cells in the row; and

the first and second row address values for the same row differ from one another by a single row address bit.

12. The integrated circuit of claim 11, wherein the logic circuitry controls the FRAM, in the normal operating mode, to read the contents of one or more memory cells by a sequence of operations including:

applying a row address to the decode circuitry;

controlling the decode circuitry to select a row of the array of memory cells corresponding to the row address while masking the single row address bit; and

operating one or more of the plurality of sense amplifiers to sense a differential signal between the first and second bit lines;

wherein, in the update mode, the verifying operation includes reading the second data set from the second half-cells of the selected plurality of memory cells by: applying a row address to the decode circuitry; controlling the decode circuitry to select a row of the array of memory cells corresponding to the row address including the single row address bit; and operating one or more of the plurality of sense amplifiers to compare a signal at the second bit line with a reference voltage.

13. The integrated circuit of claim 12, wherein the FRAM further includes: circuitry for coupling a reference voltage to one of the first and second bit lines of each of the columns in the update mode, responsive to the single row address bit.

14. The integrated circuit of claim 10, further comprising programmable logic, for executing program instructions stored in and retrieved from the FRAM; wherein the logic circuitry includes memory controller logic for controlling the FRAM to update its contents, and for storing and retrieving data in and from the FRAM in the normal operating mode.

15. The integrated circuit of claim 10, wherein the sequence of operations further includes: responsive to the verifying operation indicating an error in the second data set, writing the first data set into the second half-cell of each of the selected plurality of memory cells.

16. The integrated circuit of claim 15, wherein the verifying operation includes: reading the second data set from the second half-cells of the selected plurality of memory cells; and executing a numerical data verification on the second data set as read.

17. An integrated circuit, comprising:

a non-volatile memory, including: an array of memory cells arranged in rows and columns, each memory cell including first and second half-cells that each include a non-volatile memory element, the first half-cell coupled to a first bit line when accessed, and the second half-cell coupled to a second bit line when accessed, the first and second bit lines shared by memory cells in the same column of the array; and a plurality of sense amplifiers, each associated with a column of memory cells and coupled to the first and second bit lines for that column; and

logic circuitry for controlling the memory to update its contents by performing a sequence of operations including: storing a first data set as complementary data states in each of a plurality of the memory cells; placing the memory into an update mode in which the first and second half-cells of each memory cell are separately accessed; writing a second data set in the second half-cell of each of a selected plurality of the memory cells; verifying the second data set; responsive to successfully verifying the second data set, writing the second data set into the first half-cell of each of the selected plurality of memory cells; and then placing the memory into a normal operating mode in which the first and second half-cells of an accessed memory cell are coupled to the first and second bit lines, respectively, for the corresponding column.

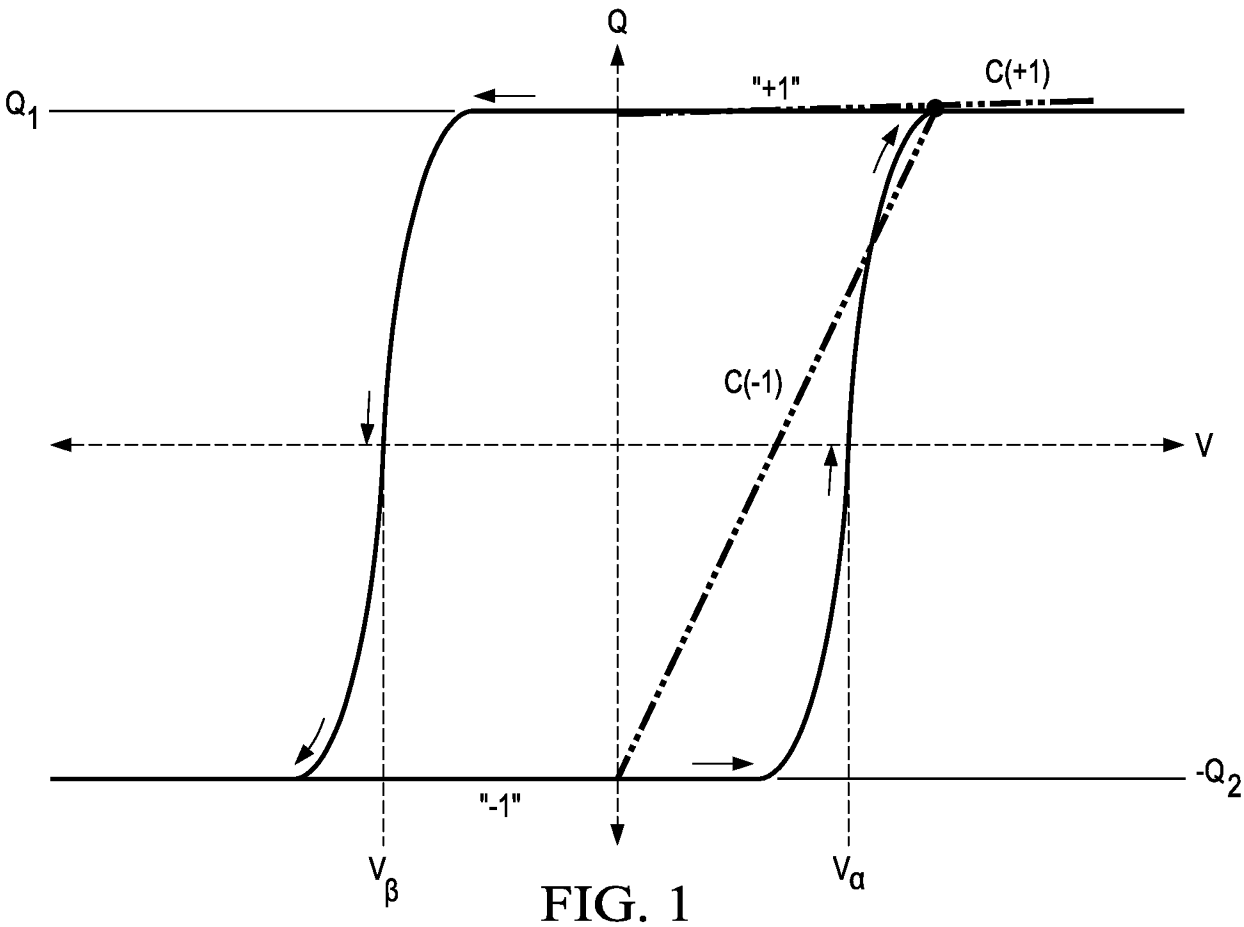

FIG. 1
(PRIOR ART)

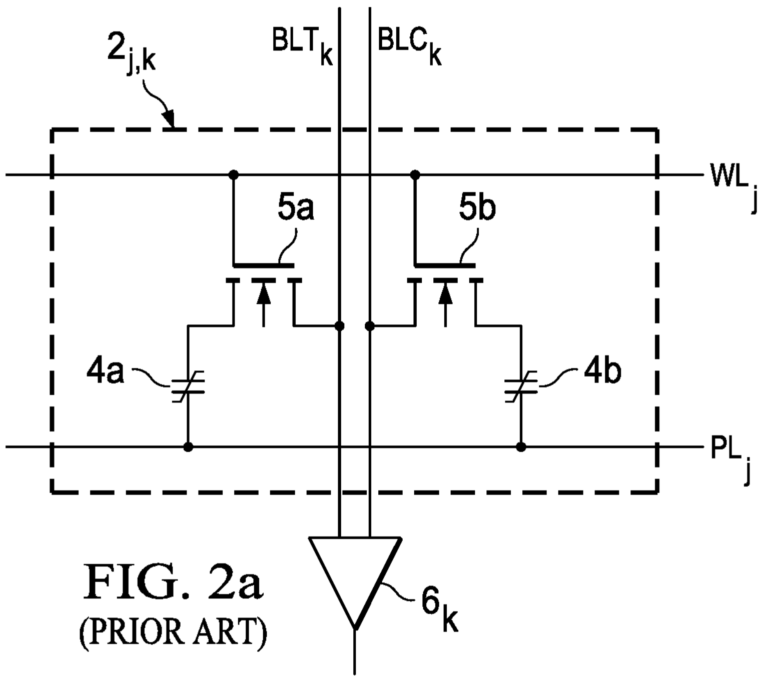

FIG. 2a
(PRIOR ART)

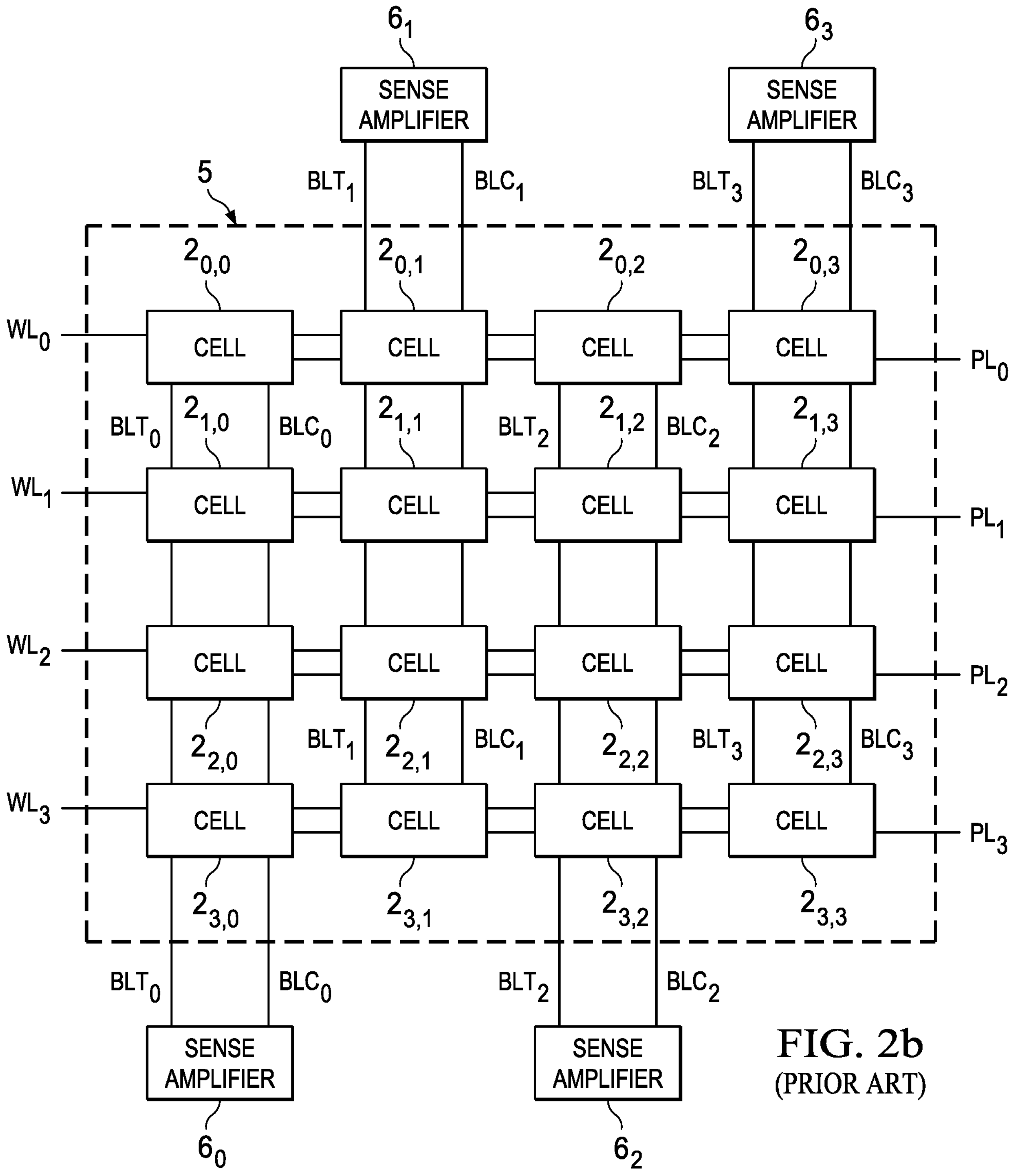

FIG. 2b
(PRIOR ART)

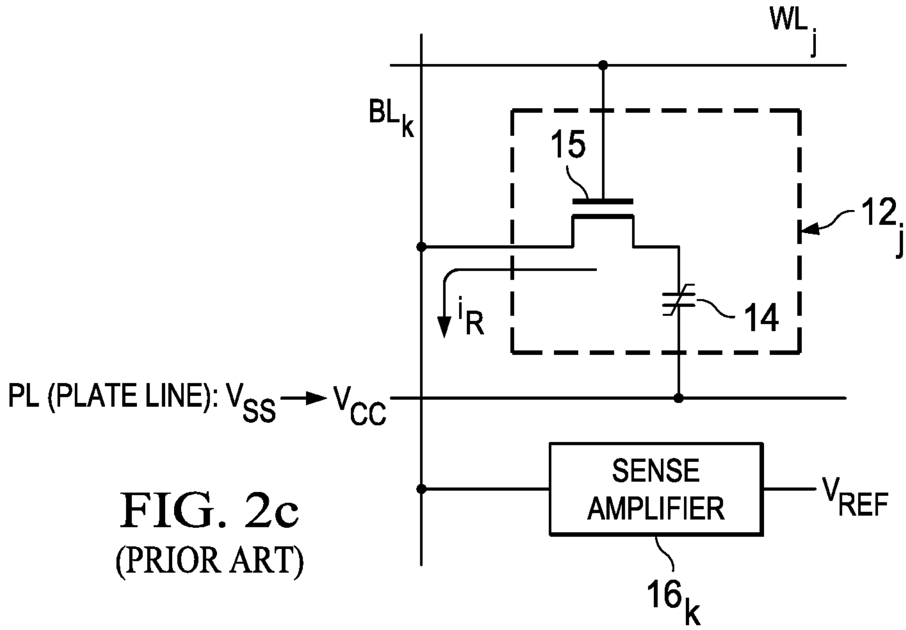

FIG. 2c
(PRIOR ART)

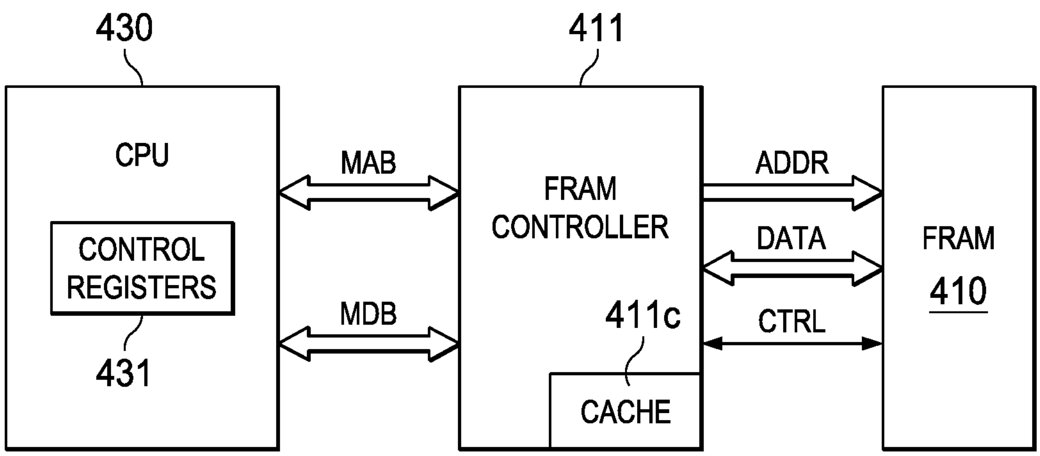

FIG. 4

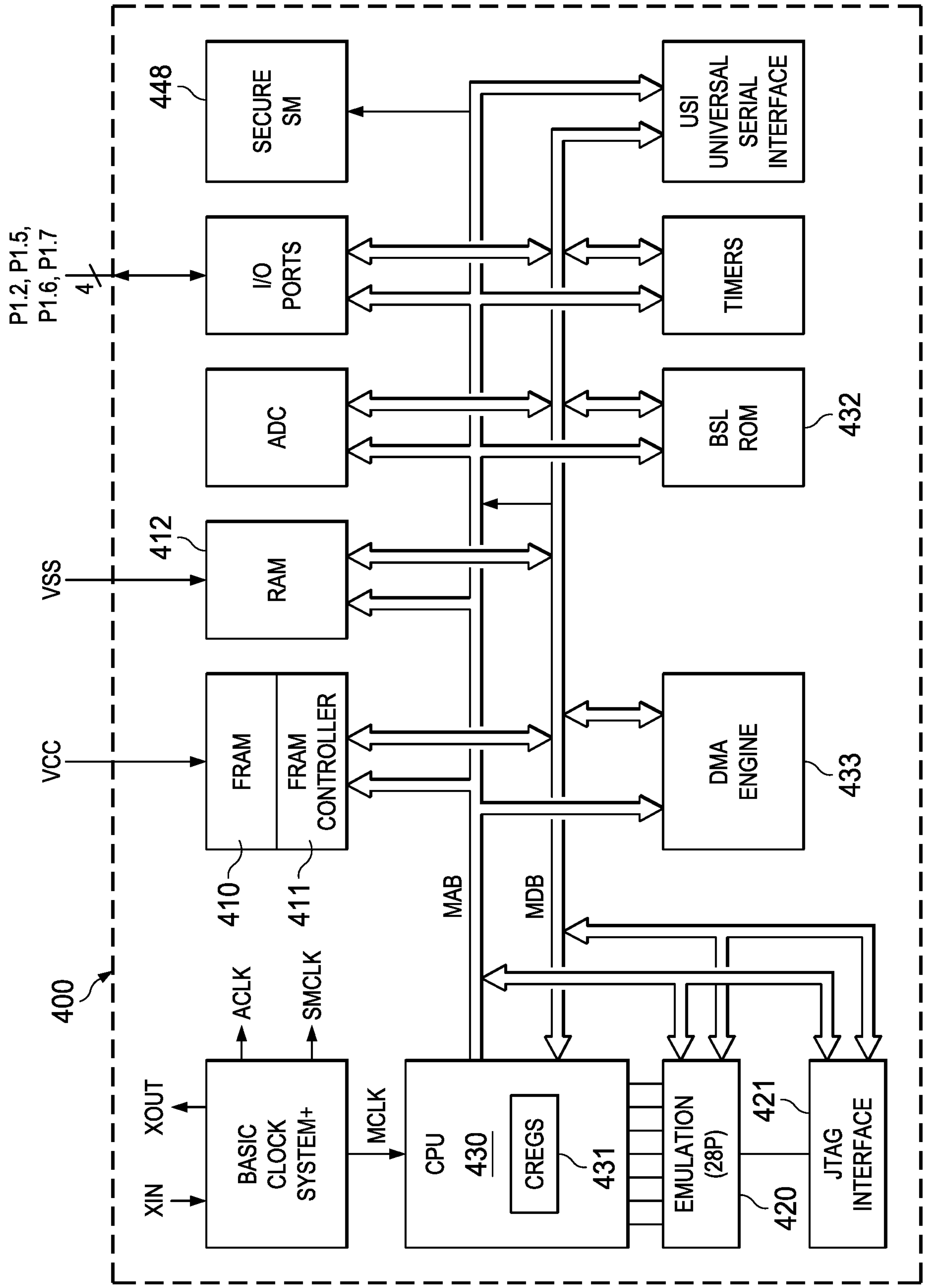
400
XIN
XOUT
BASIC CLOCK SYSTEM+
ACLK
SMCLK
MCLK
CPU
430
CREGS
431
EMULATION (28P)
420
JTAG INTERFACE
421
MAB
MDB
FRAM
410
FRAM CONTROLLER
411
VCC
RAM
412
VSS
ADC
I/O PORTS
P1.2, P1.5, P1.6, P1.7
4
SECURE SM
448
USI UNIVERSAL SERIAL INTERFACE
TIMERS
BSL ROM
432
DMA ENGINE
433

FIG. 3

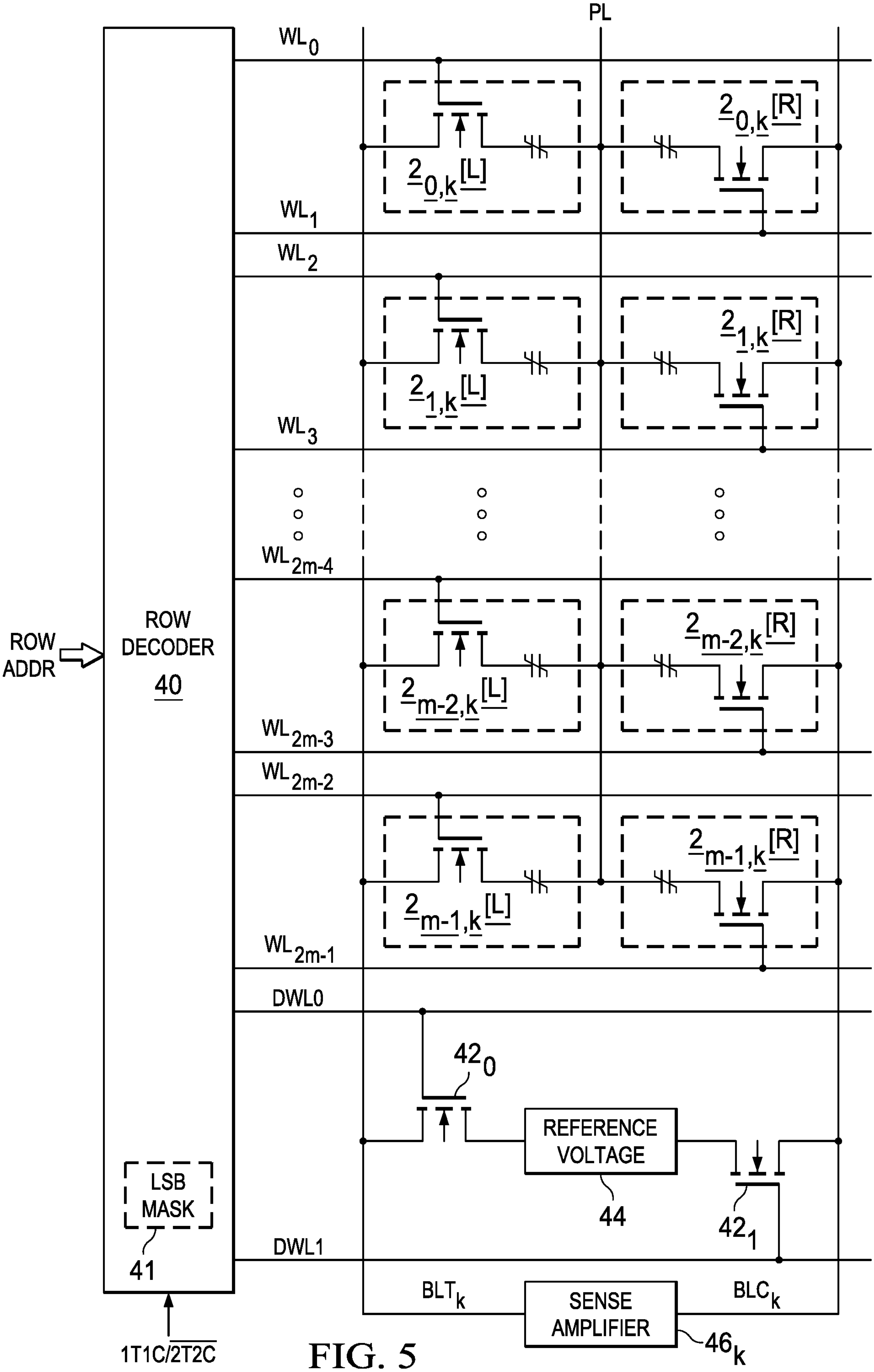
PL
WL0
WL1
WL2
WL3
WL2m-4
WL2m-3
WL2m-2
WL2m-1
DWL0
DWL1
20,k[L]
20,k[R]
21,k[L]
21,k[R]
2m-2,k[L]
2m-2,k[R]
2m-1,k[L]
2m-1,k[R]
ROW ADDR
ROW DECODER
40
LSB MASK
41
1T1C/2T2C
420
421
REFERENCE VOLTAGE
44
BLTk
BLCk
SENSE AMPLIFIER
46k

FIG. 5

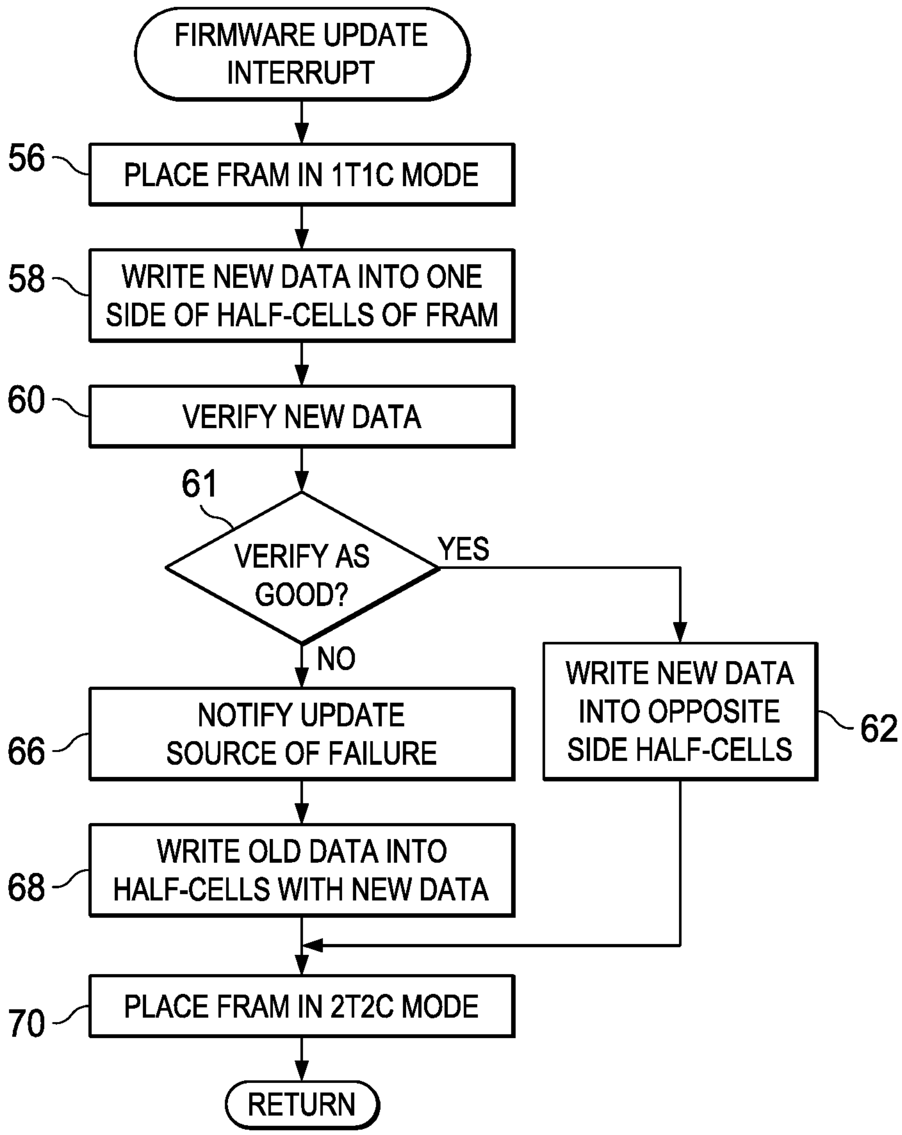
FIRMWARE UPDATE INTERRUPT
56
PLACE FRAM IN 1T1C MODE
58
WRITE NEW DATA INTO ONE SIDE OF HALF-CELLS OF FRAM
60
VERIFY NEW DATA
61
VERIFY AS GOOD?
YES
NO
WRITE NEW DATA INTO OPPOSITE SIDE HALF-CELLS
62
NOTIFY UPDATE SOURCE OF FAILURE
66
WRITE OLD DATA INTO HALF-CELLS WITH NEW DATA
68
PLACE FRAM IN 2T2C MODE
70
RETURN

FIG. 6

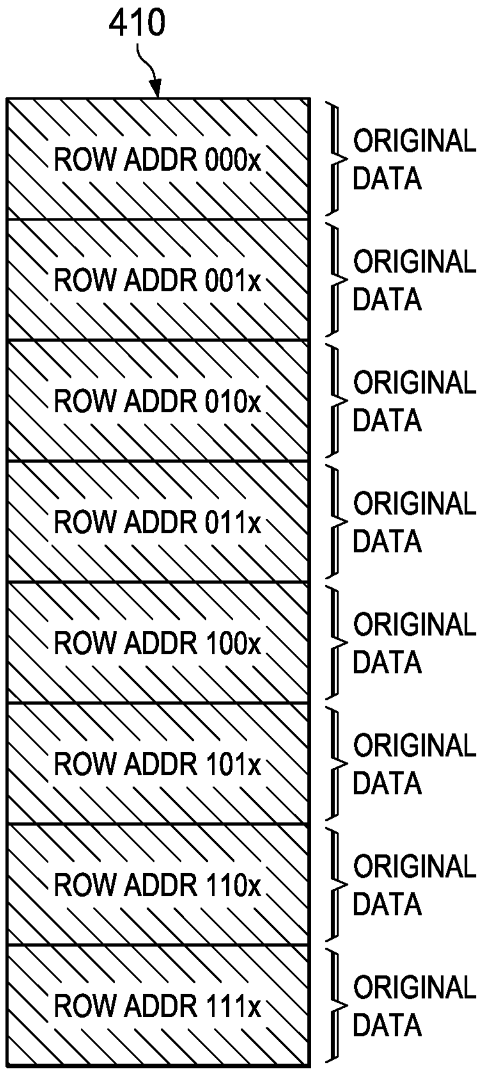
410
ROW ADDR 000x
ORIGINAL DATA
ROW ADDR 001x
ORIGINAL DATA
ROW ADDR 010x
ORIGINAL DATA
ROW ADDR 011x
ORIGINAL DATA
ROW ADDR 100x
ORIGINAL DATA
ROW ADDR 101x
ORIGINAL DATA
ROW ADDR 110x
ORIGINAL DATA
ROW ADDR 111x
ORIGINAL DATA

FIG. 7a

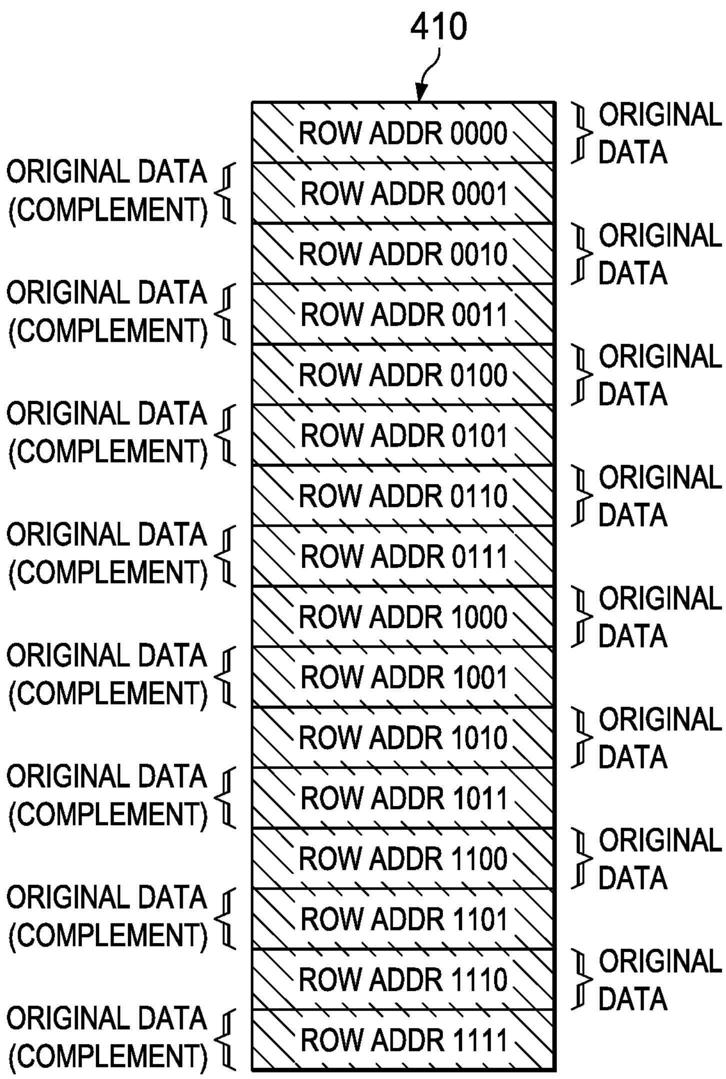
410
ROW ADDR 0000
ORIGINAL DATA
ROW ADDR 0001
ORIGINAL DATA (COMPLEMENT)
ROW ADDR 0010
ORIGINAL DATA
ROW ADDR 0011
ORIGINAL DATA (COMPLEMENT)
ROW ADDR 0100
ORIGINAL DATA
ROW ADDR 0101
ORIGINAL DATA (COMPLEMENT)
ROW ADDR 0110
ORIGINAL DATA
ROW ADDR 0111
ORIGINAL DATA (COMPLEMENT)
ROW ADDR 1000
ORIGINAL DATA
ROW ADDR 1001
ORIGINAL DATA (COMPLEMENT)
ROW ADDR 1010
ORIGINAL DATA
ROW ADDR 1011
ORIGINAL DATA (COMPLEMENT)
ROW ADDR 1100
ORIGINAL DATA
ROW ADDR 1101
ORIGINAL DATA (COMPLEMENT)
ROW ADDR 1110
ORIGINAL DATA
ROW ADDR 1111
ORIGINAL DATA (COMPLEMENT)

FIG. 7b

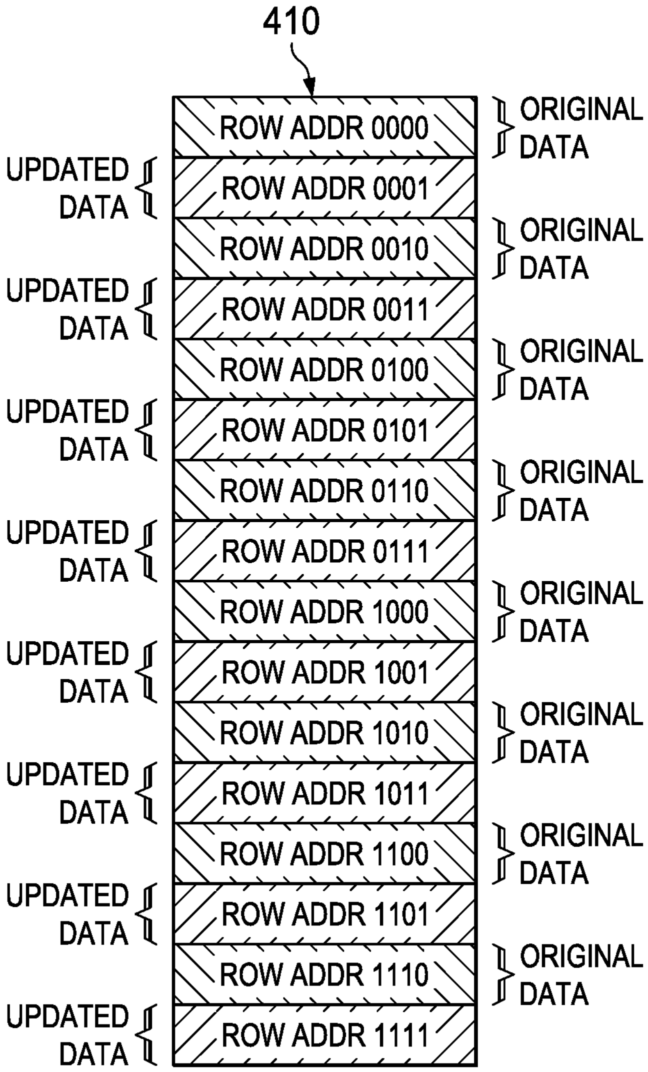
410
ROW ADDR 0000
ROW ADDR 0001
ROW ADDR 0010
ROW ADDR 0011
ROW ADDR 0100
ROW ADDR 0101
ROW ADDR 0110
ROW ADDR 0111
ROW ADDR 1000
ROW ADDR 1001
ROW ADDR 1010
ROW ADDR 1011
ROW ADDR 1100
ROW ADDR 1101
ROW ADDR 1110
ROW ADDR 1111
ORIGINAL DATA
UPDATED DATA

FIG. 7c

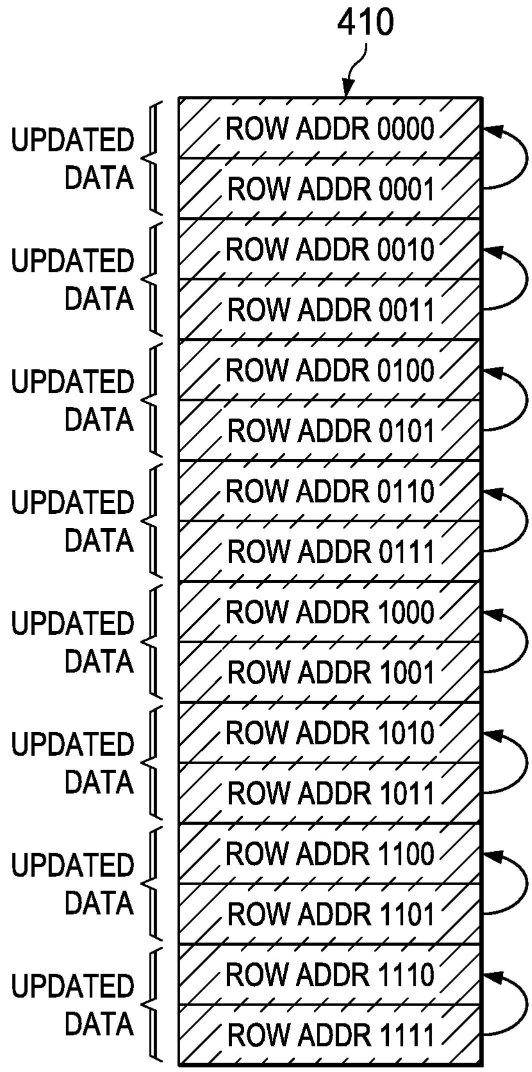
410
ROW ADDR 0000
ROW ADDR 0001
ROW ADDR 0010
ROW ADDR 0011
ROW ADDR 0100
ROW ADDR 0101
ROW ADDR 0110
ROW ADDR 0111
ROW ADDR 1000
ROW ADDR 1001
ROW ADDR 1010
ROW ADDR 1011
ROW ADDR 1100
ROW ADDR 1101
ROW ADDR 1110
ROW ADDR 1111
UPDATED DATA

FIG. 7d

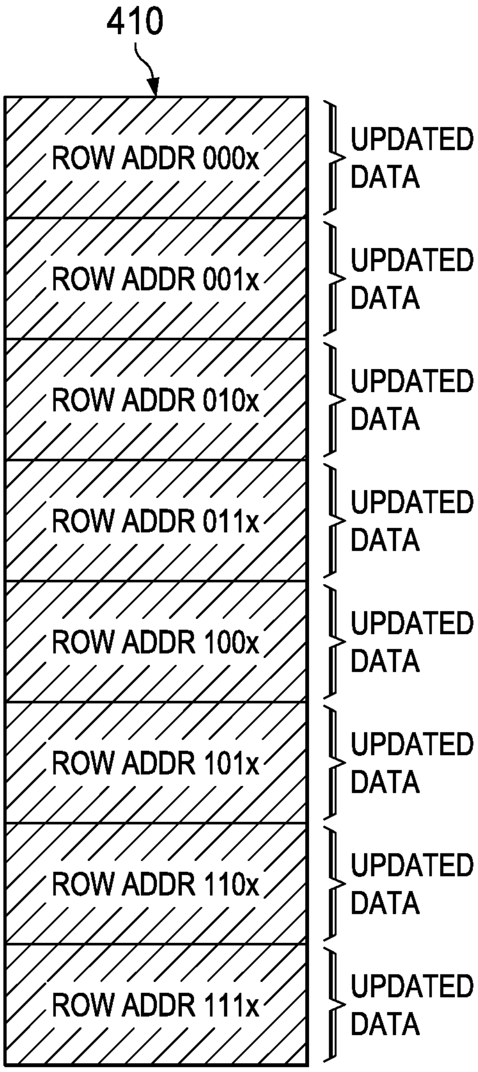
410
ROW ADDR 000x
UPDATED DATA
ROW ADDR 001x
UPDATED DATA
ROW ADDR 010x
UPDATED DATA
ROW ADDR 011x
UPDATED DATA
ROW ADDR 100x
UPDATED DATA
ROW ADDR 101x
UPDATED DATA
ROW ADDR 110x
UPDATED DATA
ROW ADDR 111x
UPDATED DATA

FIG. 7e

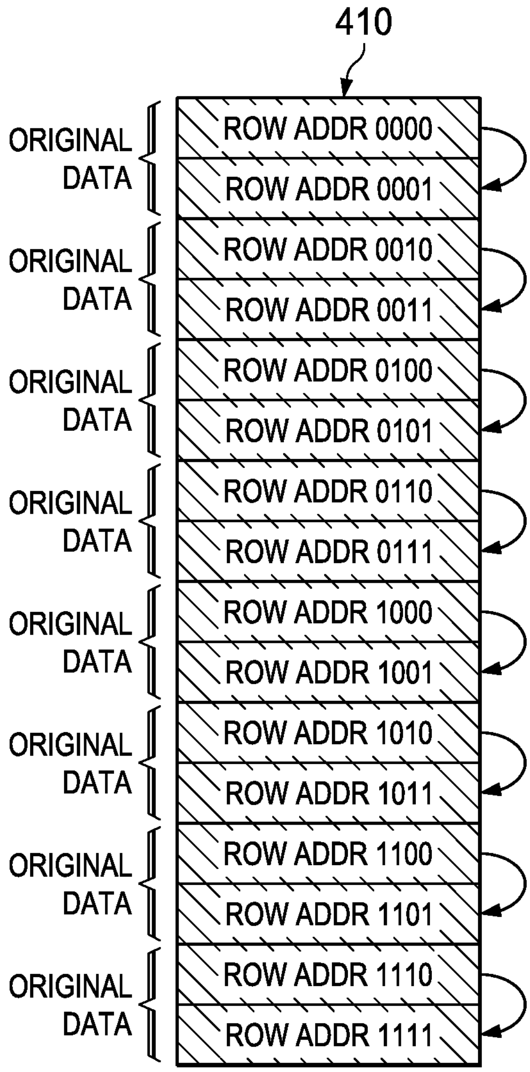
410
ORIGINAL DATA
ROW ADDR 0000
ROW ADDR 0001
ORIGINAL DATA
ROW ADDR 0010
ROW ADDR 0011
ORIGINAL DATA
ROW ADDR 0100
ROW ADDR 0101
ORIGINAL DATA
ROW ADDR 0110
ROW ADDR 0111
ORIGINAL DATA
ROW ADDR 1000
ROW ADDR 1001
ORIGINAL DATA
ROW ADDR 1010
ROW ADDR 1011
ORIGINAL DATA
ROW ADDR 1100
ROW ADDR 1101
ORIGINAL DATA
ROW ADDR 1110
ROW ADDR 1111

FIG. 7f

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/035578

A. CLASSIFICATION OF SUBJECT MATTER

G11C 11/22 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 11/00, 11/21, 11/22, 11/34, 11/40, 11/401, 11/4063, 11/407, 11/409, 11/4099, 16/00,16/02,16/06,16/10, H03K 19/00,19/02,19/185, H01G 7/00, 7/06, G11B 9/00,9/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, K-PION, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2011/0044087 A1 (KABUSHIKI KAISHA TOSHIBA) 24.02.2011, abstract, paragraphs [0020], [0061], [0073], claim 1	1-17
A	US 2012/0127777 A1 (TEXAS INSTRUMENTS INCORPORATED) 24.05.2012, abstract, paragraphs [0003], [0006], [0007], [0024], [0026], [0031], [0032], [0042]-[0044], [0048], [0060], [0062]	1-17
A	US 2010/0006942 A1 (HAN-BYUNG PARK et al.) 14.01.2010, paragraphs [0044], [0087], [0091], [0124]	1-17
A	US 2003/0210584 A1 (JUDITH E. ALLEN et al.) 13.11.2003, paragraphs [0013], [0144]	1-17

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 August 2016 (17.08.2016)	25 August 2016 (25.08.2016)

Name and mailing address of the ISA/RU:	Authorized officer
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