

ASSEMBLY LEVEL ENCAPSULATION LAYER WITH MULTIFUNCTIONAL PURPOSE, AND METHOD OF PRODUCING THE SAME

FIELD OF INVENTION

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The present invention generally relates to the field of electronic packaging and in particular to the packaging of optoelectronic components, modules and devices, e.g. Light Emitting Devices (LED), ultra-violet LEDs, white light LEDs, Superluminescent LEDs (SLED), Laser Diodes (LD), semiconductor photo detectors or photovoltaic devices. More particularly, embodiments of the present invention include multifunctional ultra-thin protective layers used for assembly level encapsulation (ALE), and having applications e.g. in LED light engine modules.

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BACKGROUND OF THE INVENTION

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Electronic or optoelectronic components must be protected from environment to prevent detrimental effects due to humidity, oxygen and corrosion due to ions and non-neutral substances.

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Different failure modes terminate component's functionality abruptly or by gradually degrading performance. The root causes of the failure modes can be roughly divided into internal and external ones. Internal ones refer to e.g. material defects, electromigration, material diffusion inside semiconductor devices, and e.g. design related failures. External ones are induced by environmental stresses that alone cause failures or trigger internal ones to develop up-to a point of failure.

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With properly designed and manufactured packaging it is possible to reduce the effect of environment and enhance the component's reliability. Hermetic sealing is a good choice to improve reliability of electronic and optoelectronic components and prevent their premature end-of-life. Without hermetic protection to external stresses the background defects can develop and cause a premature failure originating typically from chip attach, wire bonding, wire bonding joints, chip's metal-semiconductor contact, or chip's top surface passivation. Hermetic sealing can substantially increase the mean time to failure as

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typical failure mechanisms are related to moisture leaking into the package and corroding the contacts or active areas e.g. the facets of the laser diodes.

External stress is caused for example by oxygen, water vapor, corrosive gases, ions and chemically active radical groups attacking the package surfaces. External stress can cause e.g. mechanical deformation through absorption and desorption of humidity, change in electrical circuitry, galvanic corrosion, delamination, and oxidation of metal surfaces. For example humidity can chemically attack aluminum based top electrode contact pads, breaking the electrical connection between the wire bonding and the contact pad.

Semiconductor dies have normally a top surface layer, typically a thin nitride or oxide thin film that passivates the die electrically but also acts as a first buffer against corrosion due to environment. However, such passivation thin films are grown on wafer level prior the die singulation step. After dies are separated, the dies' vertical sidewalls become exposed to air and corrosive oxygen, and harmful compounds in the air. Furthermore, such chip's top surface passivation layers are open on the electrical contact pads, exposing these areas directly to stress from environment.

US 2007/0215998 discloses a LED package where a LED is attached to a substrate. A protective layer, disposed by plasma chemical vapor deposition surrounds the chip (the LED), the upper side of the substrate and electrically conductive humps. The protective layer consists of several sub-layers which have different refractive index. However, D1 does not disclose any protective layer consisting of sub-layers with different electrical conductivity.

US 2012/0326178 concerns an optoelectronic component comprising a semiconductor protected by a sealing material applied by atomic layer deposition.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an encapsulated optoelectronic component. The encapsulation is introduced at assembly level to provide an optically transparent hermetical sealing layer and electrically insulating layer on all surfaces of the

said component. The encapsulation, which is in direct contact with the surface of the component, provides a zero cavity structure.

It is an aspect of certain embodiments to provide an optoelectronic component comprising;
5 a substrate, at least one light emitter device mounted on the substrate, and electrical contacts, with all surfaces coated with the protective layer. The substrate material can be ceramic, but is not limited to, e.g. Alumina (Al_2O_3) or Aluminum Nitride (AlN). The substrate can be semiconductor material, but is not limited to, e.g. Silicon. The substrate material can be a typical printed circuit board material, but is not limited to, e.g. FR4, FR5,
10 or epoxy laminate material.

The protective layer can be a material layer deposited with ALD or other similar means. The protective layer can be a multi-layer coating formed of two or more materials, such as Al_2O_3 and SiO_2 .

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The protective layer's function is to provide hermetic sealing of all surfaces. The protective layer is deposited with a conformal coating process so that vertical sidewalls, edges, and shadowed areas are covered. The protective layer is formed at least on the front surface of the said component. According to certain embodiments the protective layer could be
20 deposited on all surfaces of the component including the back side of the substrate and substrate's vertical sidewalls.

According to certain embodiments the protective layer could be deposited on top of mechanical package and transparent covering.

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The protective layer is physically in contact with the active optical chips, and electrical parts, so that no cavity is formed between component and protective layer.

Embodiments of the present invention aim to solve issues associated with multichip
30 modules and their hermetic sealing in a cost effective way. A common problem in packaging is that the layouts and dimensions of the units or chips to be packaged are changing due to rapid technical advancement and process changes, as in the field of LED technology. A flexible packaging approach is thus required that can accommodate

frequently changing units without being modified despite changes in the actual LED processing or LED chips. An approach that is cost effective and, for example, which does not apply fixed mask sets is desired.

- 5 The Atomic Layer Deposition (ALD) technique is well suited for this task. The ALD method can be applied on any 3D geometry and packaging material. ALD offers wide selection of materials to choose most suitable to form the said protective layer. The flexibility of the present invention has a substantial advantage over other packaging methods such as WLP.

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It is a further object of the present invention to provide a method for manufacturing a hermetically sealed optoelectronic component according to the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

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Figure 1 shows schematic cross-section of optoelectronic component with a substrate, a semiconductor die with electrical contact pad layer on top of surface of the die, die attach layer, electrical conductive layer on top surface of the substrate, and a wire bond to form electrical contact between the die and the electrical conductive layers.

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Figure 2 shows schematic cross-section of optoelectronic component with a substrate, a semiconductor die with electrical contact pad layer on top of surface of the die, die attach layer, electrical conductive layer on top surface of the substrate, a wire bonding to form electrical contact between the die and the electrical conductive layers, and a protective

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layer covering the component surface excluding the back side of the substrate.

Figure 3 shows assembly flow for a typical component comprising a step to form the said protective layer.

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EMBODIMENTS

In the present context, the following terms are interchangeably used:

- “die” and “chip”; and

- “protection layer”, “encapsulation”, “coating” and “barrier layer”.

The verbs “to comprise” and “to include” are used in this document as open limitations that neither exclude nor require the existence of also un-recited features. The features
5 recited in dependent claims are mutually freely combinable unless otherwise explicitly stated. Furthermore, it is to be understood that the use of "a" or "an", i.e. a singular form, throughout this document does not exclude a plurality.

The present invention discloses means to provide a protective layer after or during the assembly phase to improve the component's reliability. In order to protect all surfaces
10 susceptible to environmental stresses, the protective layer is deposited after the basic assembly steps have been completed including the die separation, die attachment to substrate and wire bonding steps. The protective layer is made as a final step of the assembly, or just prior a mechanical enclosure is done. After the protective layer has been deposited, only the contact areas or the soldering pads for a printed circuit board assembly
15 are left un-protected.

Such protective layers are ultra-thin optically transparent, conformal and uniform in nature. They provide a moisture resistance and improved electrical insulation with a typical application in LED light engine modules.
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Referring to Figure 3:

For example in case of a LED package comprising of a semiconductor die made of III-V semiconductor material mounted with conductive adhesive on an alumina substrate having
25 on its top surface electrically conductive tracks made of silver alloy, and copper wire bonding to form electrical contacts between the semiconductor die and the electrical layer of the substrate.

After the die attach and wire bonding the assembled component can be coated with a
30 protective layer formed of two dielectric materials of 10 nm of Al_2O_3 and 5 nm of SiO_2 and these sub-layers could be deposited post-assembly e.g. with an atomic layer deposition method. Such a protection layer would be optically transparent and innocuous. The thickness of the protection layer can be optimized for the transmission at the said

wavelength in interest. For example one quarter wavelength thick anti-reflection coating for an emission wavelength of 405 nm would be $(405 \text{ nm}/4/1.8) \sim 59 \text{ nm}$.

According to one embodiment of the present invention, a method of making a solid state light emitting and/or light detecting device, comprises the steps of:

- providing a first substrate;
- providing on the first substrate a plurality of solid state light emitting and/or light detecting chips;
- wire bonding the solid state chips to the first substrate;
- 10 – providing a conformal sealing layer to the solid state chips, wire bonds and any exposed first substrate between the solid state chips;
- providing a second substrate that is transmissive to the wavelength of light to be emitted and/or detected by the solid state chips; and
- 15 – providing a sealing layer between the first and second substrates and bonding the first and second substrates together so as to seal the solid state chips therebetween.

In one embodiment, the protective layer comprises at least one material selected from the group of oxide materials consisting of Al_2O_3 , TiO_2 , ZnO , HfO_2 , HfSiO , SiO_2 , MgO , Ta_2O_5 , ZrO_2 .

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In another embodiment, the protective layer comprises at least one material selected from the group of nitride materials consisting of AlN , HfN , SiN_x , Si_3N_4 , TaN , TiN .

In a third embodiment, the protective layer consists of electrically conductive material of Indium Tin Oxide.

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The protective layer manufacturing with the atomic layer deposition can take place at relatively low temperature. A high quality Al_2O_3 layer can be grown at 120 to 150 °C.

30 Low temperatures are often preferred as typical electronic packaging materials can withstand only 150 °C. A plasma-assisted ALD can be used for depositing low-temperature silicon dioxide as a top sub-layer at temperature of 150 °C. Alternatively, it

has been also proposed to use a low temperature thermal ALD process can be used for depositing a high quality silicon dioxide.

As the protection layer deposition takes place after the assembly i.e. the semiconductor die
5 has been attached to the substrate and electrical connections have been made by wire bonding, all surfaces including die attach layer and wire bonding become protected as well and improve the reliability of the component. The substrate or module has typically electrical contact pads used to make the connections to an external circuitry in the printed circuit board assembly phase. Such electrical contact pads on the substrate can be
10 selectively protected during the deposition of the protective layer with e.g. a Kapton tape, which can be removed after the deposition of the protective layer.

Described herein is a hermetically sealed optoelectronic component. According to an embodiment, there are optoelectronic components comprising; a substrate, at least one
15 optoelectronic chip bonded, soldered or glued on the substrate, an electrically conductive track on the substrate, and a wire bonding making electrical connection from the said chip to electrical conductive track on the top surface of the substrate,.

Examples of optoelectronic components are Light Emitting Diode (LED) components,
20 Laser Diode (LD) components, Superluminescent LEDs (SLED), and other non-emitting types of components such as semiconductor detectors or imaging arrays. Light emitter components according to the present invention should not be limited to those emitting visible light but also include other forms of electromagnetic radiation. Further examples of light emitter components include those which comprises an In-, Ga-, Al-, and/or N-
25 containing compound, for instance an InGaN or AlGaN diode.

In one embodiment, the present invention comprises a component formed of a substrate, semiconductor chip(s), electrical contact wire(s), electrical contact layer(s), electrically conductive track(s), and a protective layer, which is a conformal layer forming a uniform
30 coating on the said component's surface. The protective layer is further hermetic and optically transparent. Preferably the protective layer comprises sub-layers of two or more different materials, wherein one sub-layer is electrically conductive in order to avoid charge accumulation in the coating.

None of the above-mentioned references discloses any component or solid state device based on such a component, where the component has a protective layer in which one sub-layer is electrically conductive in order to avoid charge accumulation in the coating.

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Optical performance

In some embodiments of the present invention, the protective coating acts also as a functional layer to improve optical performance e.g. it can act as an anti-reflection coating, or provide optimized transmission of the electromagnetic radiation in certain wavelength in interest.

In another embodiment the protective layer functions as an optical layer providing means to create selective or custom reflection or transmission bands at a wavelength in interest. Such a protective layer could be formed of several alternating high refractive index and low refractive index materials. Thus the said protection layer provides means to optimize e.g. sensor sensitivity for a specified wavelength range.

Electrical insulation

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Carbonization of materials within the component package can lead to accumulation of materials on top of the active surfaces, possibly causing undesired conductive paths causing leakage currents and short-circuit failures. Typically electrical contacts are made with wire bonding, which have non-insulated metal surfaces. Also the conductive paths on top surface of the substrates are non-insulated. Both of these are susceptible to leakage currents and short-circuit type failures. If protection layer material is dielectric the said passivation layer acts as electrical insulation layer formed on all electrical conductors prohibiting unwanted current paths and thus improves electrical performance and reliability.

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In one embodiment, the protective layer has a sheet resistance lower than 1000 ohm, or preferably, lower than 100 ohm, or even more preferably lower than 10 ohm.

The said protective layer that forms conformal coating around wire bonding would enable use of other materials than Au and leading to a more economical component.

Humidity absorbed on the component's surface can cause leakage currents and even cause short circuits. Thus a dielectric protective layer forming uniform insulation layer on all surfaces protects device from such electrical failures.

Furthermore the said dielectric protective layer acting would prevent galvanic corrosion mechanism to erode metallic surfaces.

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A conformal passivation layer manufactured post module assembly provides convenient way to passivate all package surfaces susceptible to degradation under corrosive environment. In case of porous package surfaces it is likely that humidity absorbed causes deformation and stress leading to early failure. A conformal passivation layer provides means to prevent absorption of humidity inside porous surfaces.

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In some embodiment of this invention the protective layer can be made hydrophobic to further increase the resistance to humidity.

20 The protective layer typically has a water vapor transmission rate lower than 1×10^{-2} g/m²/day, or preferably lower than 1×10^{-3} g/m²/day, as measured at 25 °C, and at 50% relative humidity.

The protective layer typically has an oxygen transmission rate lower than 1×10^{-2} cm³/m²/atm/day, or preferably lower than 1×10^{-3} cm³/m²/atm/day.

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It is foreseen that in some applications it is beneficial to have the said protective layer comprise conductive sub-layers to enable electrical functions. For example to avoid charge accumulation in the coating, an Indium Tin Oxide (ITO) sub-layer could be used as part of the protective layer.

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Barrier against oxidation

Typically used materials Ag, Al, Cu suffer oxidation. Commonly used reflector materials in LED packages are Ag or Ag based alloys. In another embodiment of the disclosed invention the protection layer covers the package surfaces coated with reflective thin films comprising Ag or Al based alloys. These alloys are susceptible to tarnishing and easily lose their reflectivity due to oxidation if applied without appropriate protective layer. The said protective layer shields such reflector layers from oxidation and lengthens the life-time of the LED.

Manufacturing

The said protective layer can be manufactured with a wide range of standard deposition methods applied in the semiconductor industry. Such standard methods include for example atomic layer deposition, plasma enhanced chemical vapor deposition, and sputtering. As it is often a requirement to have a conformal layer to protect shadowed areas, the ALD is the most preferred manufacturing method. A thermal, plasma-assisted or spatial ALD can be used for manufacturing the layers, or any combination of those. The structure of the said protective layer is such that it can be processed with a one loading step providing economical solution for the encapsulation.

Turning now to Figures 1 and 2:

Figure 1 shows an example of an optoelectronic component 100. The component has a substrate 101 having one chip 105 mounted on the substrate. The chip is solder or adhesive mounted on the substrate. A thin material layer 102 of solder or adhesive is between chip and substrate. The chip and substrate both have electrical contact layers 104, 110 on top surfaces. The chip is electrically connected from a chip's bonding pad 107 with a wire bonding 108 to the substrate's electrical contact pad 110.

Figure 2 shows an example of an optoelectronic component 200 with a protective conformal coating layer 211 forming uniform and homogeneous hermetical seal covering all surfaces of the component.

The other components 201 to 210 are analogous to the ones mentioned above in connection to optoelectronic component 100.

REFERENCE SIGNS LIST

- 5
- 101 substrate
 102 solder/adhesive material layer on top of electrical contact layer on substrate's surface
 103 chip vertical edge
 104 electrical contact layer on top surface of the chip
 10 105 chip
 106 top surface of the chip
 107 wire bonding bump on top of electrical contact layer on chip's top surface
 108 bonding wire
 109 wire bonding bump on top of electrical contact layer on substrate's surface
 15 110 electrical contact layer on substrate's surface
 201 substrate
 202 contact material layer on top of electrical contact layer on substrate's top surface
 203 chip vertical edge
 204 electrical contact layer on top surface of the chip
 20 205 chip
 206 top surface of the chip
 207 wire bonding bump on top of electrical contact layer on chip's top surface
 208 bonding wire
 209 wire bonding bump on top of electrical contact layer on substrate's surface
 25 210 electrical contact layer on substrate's top surface
 211 conformal protection layer
 301 Wafer Cutting – Die Singulation
 302 Die Attachment to Substrate
 303 Electrical Contact Making - Wire Bonding
 30 304 Protective Layer Deposition
 305 Mechanical Protection

LIST OF REFERENCES

- 35 US 2007/0215998
 US 2012/0326178

CLAIMS

1. A component formed of
 - a substrate,
 - 5 – semiconductor chip(s),
 - electrical contact wire(s), electrical contact layer(s),
 - electrically conductive track(s), and
 - a protective layer.
- 10 2. A component according to claim 1, wherein the said protective layer
 - is a conformal layer forming a uniform coating on the said component's surface,
 - is hermetic,
 - is optically transparent, and/or
 - comprises sub-layers of two or more different materials.
- 15 3. A component according to any of the preceding claims, wherein the said protective layer's thickness is preferably below 100 nm, or below 20 nm, or below 5 nm.
- 20 4. A component according to any of the preceding claims, wherein the said protective layer is made with a method selected from the group comprising the atomic layer deposition method, the chemical vapor deposition method, plasma enhanced chemical vapor deposition method, physical vapor deposition, electron sputtering, ion beam sputtering, magnetron reactive sputtering and a combination thereof.
- 25 5. A component according to any of the preceding claims, wherein the said protective layer comprises at least one material selected from the group of oxide materials consisting of Al_2O_3 , TiO_2 , ZnO , HfO_2 , HfSiO , SiO_2 , MgO , Ta_2O_5 , ZrO_2 , and/or comprises at least one material selected from the group of nitride materials consisting of AlN , HfN , SiN_x , Si_3N_4 , TaN , TiN .
- 30 6. A component according to any of claims 1 to 4, wherein the said protective layer comprises or consists of electrically conductive material(s) of Indium Tin Oxide.

7. A component according to any of the preceding claims, wherein the said protective layer has water vapor transmission rate lower than 1×10^{-2} g/m²/day, or preferably lower than 1×10^{-3} g/m²/day, as measured at 25 °C, and at 50% relative humidity.
- 5 8. A component according to any of the preceding claims, wherein the said protective layer has oxygen transmission rate lower than 1×10^{-2} cm³/m²/atm/day, or preferably lower than 1×10^{-3} cm³/m²/atm/day
9. A component according to any of the preceding claims, wherein the said protective layer
10 forms uniform electrically non-conductive top layer.
10. A component according to any of claims 1 to 9, wherein the said protective layer is electrically conductive, preferably having sheet resistance lower than 1000 ohm, or preferably lower than 100 ohm, or preferable lower than 10 ohm.
- 15 11. A component according to any of the preceding claims, wherein the said protective layer has optical transmission higher than 80 % and preferably higher than 85 %.
12. A component according to any of the preceding claims, wherein the said protective
20 layer is transparent for the required electromagnetic wavelengths for the said component.
13. A component according to any of the preceding claims, wherein the refractive index profile of the said protective layer is optimized for light output extraction from the surface of the said component.
- 25 14. A component according to any of the preceding claims, wherein the said protective layer forms an anti-reflection coating for the required wavelength range of the said component said anti-reflection coating preferably having a thickness of one quarter wavelength.
- 30 15. A component according to any of the preceding claims, wherein the said semiconductor die is an optoelectronic component, preferably emitting electromagnetic radiation, for example a light emitting diode.

16. A component according to any of claims 1 to 14, wherein the said component detects electromagnetic radiation *e.g.* a photodiode or a light sensitive sensor array.

5 17. A component according to any of the preceding claims, formed of

- a substrate,
- semiconductor chip(s),
- electrical contact wire(s), electrical contact layer(s),
- electrically conductive track(s), and

10 – a protective layer, which

- is a conformal layer forming a uniform coating on the said component's surface,
- is hermetic,
- is optically transparent, and

15 ○ comprises sub-layers of two or more different materials, wherein one sub-layer is electrically conductive in order to avoid charge accumulation in the coating.

18. A method of making a solid state light emitting and/or light detecting device, in particular based on the use of a component according to any of the claims 1 to 17, comprising:

- providing a first substrate;
- providing on the first substrate a plurality of solid state light emitting and/or light detecting chips;
- 25 – wire bonding the solid state chips to the first substrate;
- providing a conformal sealing layer to the solid state chips, wire bonds and any exposed first substrate between the solid state chips;
- providing a second substrate that is transmissive to the wavelength of light to be emitted and/or detected by the solid state chips; and
- 30 – providing a sealing layer between the first and second substrates and bonding the first and second substrates together so as to seal the solid state chips therebetween, said sealing layer being an atomic layer deposition (ALD) layer preferably comprising Al_2O_3 , SiNO_x , ZrO_2 , HfO_2 , $(\text{Ba}, \text{Sr})\text{TiO}_3$, Hf_3N_4 , Zr_3N_4 , HfO_xN_y and

ZrO_xN_y and/or Ta₂O₅, in particular the ALD layer is Al₂O₃ or SiNO_x or an organic layer, preferably a silicone or epoxy layer.

19. The method of claim 18, further comprising depositing a silicon nitride, oxide or oxynitride layer prior to the ALD layer for coating the solid state chips, wire bonds and any exposed first substrate between the solid state chips, with the ALD layer having a thickness of from 5 to 50 nm deposited thereafter.
20. The method of any of claims 18 or 19, wherein the sealing layer is a metal or ceramic layer, preferably an oxide, nitride or oxynitride of a metal or metalloid, or the sealing layer is a glass frit layer.
21. The method of any of claims 18 to 20, further comprising bonding a second substrate to the first substrate for sealing the light emitting or light detecting chips therebetween, wherein the second substrate is a glass, quartz or sapphire substrate, and preferably the second substrate is a substantially planar substrate.
22. The method of any of claims 18 to 21, wherein the second substrate comprises material selected from the group of an organic polymeric material, a hybrid organic-inorganic polymeric material, a phosphor and combinations thereof.
23. The method of any of claims 18 to 22, wherein the solid state chips comprise both light emitting and light detecting chips, preferably LED chips.
24. The method of any of claims 18 to 23, wherein the conformal layer is a hermetic layer, preferably further comprising a self-assembled monolayer.
25. The method of any of claims 18 to 24, wherein the ALD layer comprises an nitride, oxide, or oxynitride of aluminum, silicon, zirconium, titanium and/or hafnium.
26. The method of any of claims 18 to 25, further comprising depositing a silicon nitride, oxide or oxynitride layer after the ALD layer for further coating the solid state chips, wire bonds and any exposed first substrate between the solid state chips.

27. The method of any of claims 17 to 25, wherein the ALD layer is an oxide layer preferably comprising CaO, ZnO, Er₂O₃, Sc₂O₃, La₂O₃, HfO₂, Ta₂O₅, SiO₂, V_xO_y, Ga₂O₃, Y₂O₃, TiO₂, CuO, Nb₂O₅, Yb₂O₃, Al₂O₃, MgO and/or ZrO₂ or a nitride layer, preferably comprising AlN, TiN_x TaN_x, and/or TiAlN or an oxynitride layer, preferably comprising SiNO_x, HfO_xN_y and/or ZrO_xN_y.
28. A solid state device, comprising:
- a first substrate;
 - on the first substrate a plurality of solid state light emitting and/or light detecting chips, such as light emitting diodes, which are electrically connected to the first substrate; and
 - a conformal sealing layer, which is optionally a hermetic layer and optionally further comprises a self-assembled monolayer, disposed on the solid state chips, wire bonds and any exposed first substrate between the solid state chips, said sealing layer optionally being an organic layer, preferably a silicone or epoxy layer, or an atomic layer deposition (ALD) layer, preferably having a thickness of from 5 to 50 nm, preferably comprising an nitride, for example a nitride layer comprising AlN, TiN_x TaN_x, and/or TiAlN, an oxide, for example an oxide layer comprising CaO, ZnO, Er₂O₃, Sc₂O₃, La₂O₃, HfO₂, Ta₂O₅, SiO₂, V_xO_y, Ga₂O₃, Y₂O₃, TiO₂, CuO, Nb₂O₅, Yb₂O₃, Al₂O₃, MgO and/or ZrO₂, or oxynitride, particularly preferably comprising Al₂O₃, SiNO_x, ZrO₂, HfO₂, (Ba,Sr)TiO₃, Hf₃N₄, Zr₃N₄, HfO_xN_y and ZrO_xN_y or Ta₂O₅, in particular Al₂O₃ or SiNO_x, optionally further comprising a self-assembled monolayer, and/or a metal or ceramic layer, such as an oxide, nitride or oxynitride of a metal or metalloid, or the sealing layer is a glass frit layer, said sealing layer optionally having a water vapor transmission rate lower than 1×10^{-2} g/m²/day, as measured at 25 °C, and at 50% relative humidity, further optionally having oxygen transmission rate lower than 1×10^{-2} cm³/m²/atm/day, preferably further optionally having sheet resistance lower than 1000 ohm, or preferably lower than 100 ohm,

particularly further optionally having optical transmission higher than 80%, in particular higher than 85%,
said sealing layer optionally being provided at a thickness so as to act as an anti-reflection coating at a wavelength of light at which the light emitting or light
5 detecting chips operate.

29. The device of claim 28, wherein a second substrate is provided to connect directly or indirectly to the first substrate for sealing the light emitting or light detecting devices therebetween, and preferably the second substrate is a substantially planar glass, quartz or
10 sapphire substrate, optionally comprising an organic or hybrid organic-inorganic polymeric material, and/or comprising a phosphor, preferably comprising multiple phosphors that emit light at different wavelengths.

30. The device of any of claims 28 to 29, wherein the solid state chips comprise both light
15 emitting and light detecting chips, preferably LED chips.

31. The device of any of claims 28 to 30, further comprising a silicon nitride, oxide or oxynitride layer deposited after the ALD layer for further coating the solid state chips, wire bonds and any exposed first substrate between the solid state chips.

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32. The device of any of claims 28 to 31, further comprising:

- a second substrate bonded to the first substrate that is transmissive to the wavelength of light to be emitted and/or detected by the solid state chips.

25 33. The device of any of claims 28 to 32 further comprising:

- a sealing layer between the first and second substrates for bonding the first and second substrates together so as to seal the solid state chips therebetween, wherein the sealing layer is optionally a glass frit layer, or a metal solder layer, and optionally further comprising an organic polymeric coating on top of the sealing
30 layer, wherein the organic coating comprises at least one phosphorescence material and/or is an epoxy coating or a silicone coating.

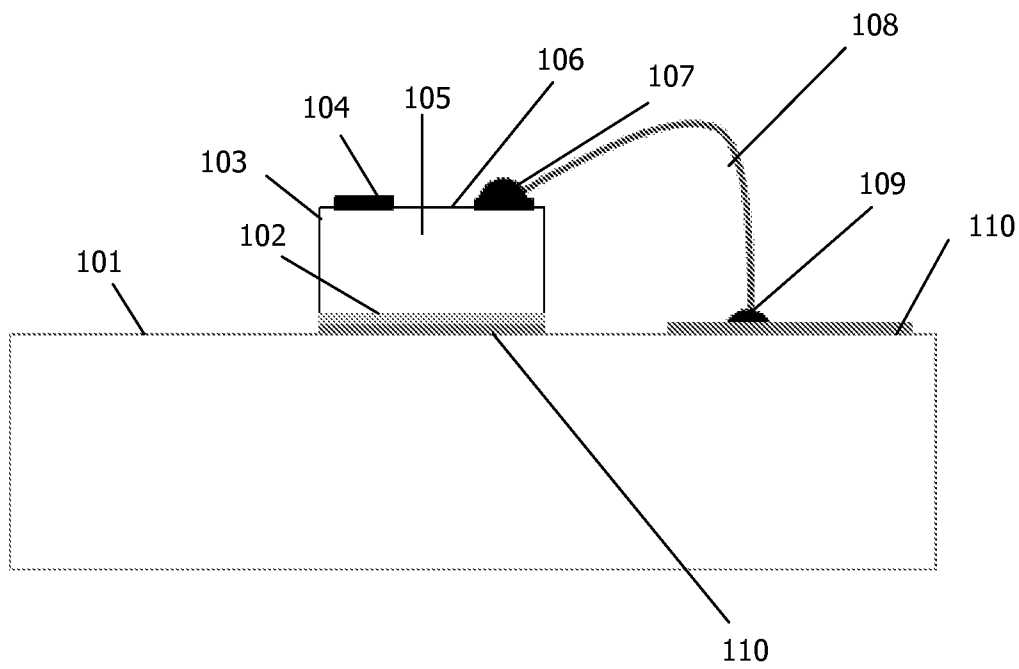


Fig. 1

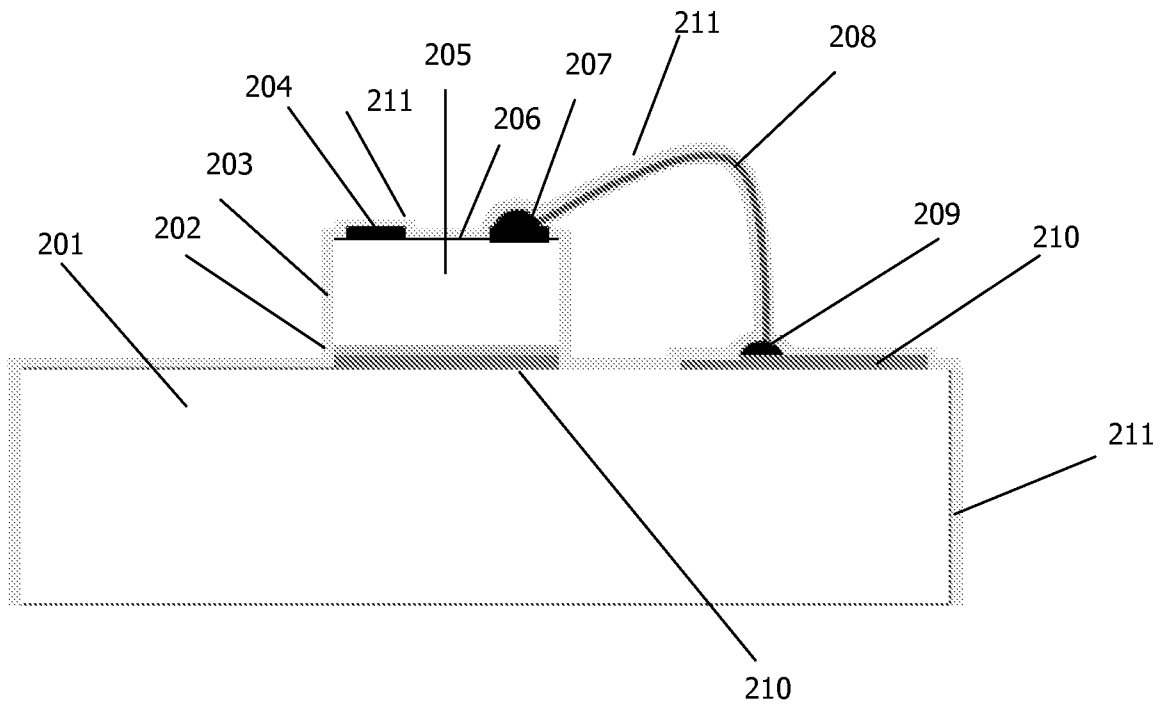
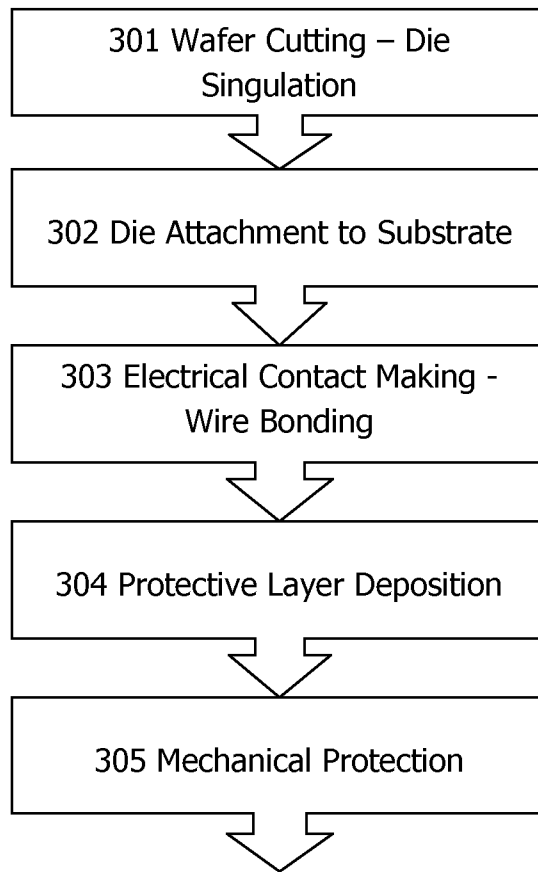


Fig. 2

2/2

**Fig. 3**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI2014/050741

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

FI, SE, NO, DK

Electronic data base consulted during the international search (name of data base, and, where practicable, search terms used)

EPO-Internal, WPI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2007215998 A1 (HU CHEN-ZE [TW] et al.) 20 September 2007 (20.09.2007) paragraphs [0004]-[0006], [0015], [0016]; Fig. 2E paragraphs [0004]-[0006], [0015], [0016]; Fig. 2E	1-18, 20-33 19
X Y	US 2013161658 A1 (LIN SHAOW B D [US] et al.) 27 June 2013 (27.06.2013) [0015], [0040], [0041], [0049], [0091]; Figs. 7 [0015], [0040], [0041], [0049], [0091]; Figs. 7	1-18, 20-33 19
Y	WO 2011073027 A1 (OSRAM OPTO SEMICONDUCTORS GMBH [DE]) 23 June 2011 (23.06.2011) paragraphs [0034], [0038]	19
A	WO 2009061704 A2 (HCF PARTNERS L P [US]) 14 May 2009 (14.05.2009)	

☒ Further documents are listed in the continuation of Box C.
☒ See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
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Date of the actual completion of the international search 29 January 2015 (29.01.2015)	Date of mailing of the international search report 30 January 2015 (30.01.2015)
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INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI2014/050741

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007004080 A1 (OUYANG MIKE X [US]) 04 January 2007 (04.01.2007)	
A	EP 2381491 A1 (LG INNOTEK CO LTD [KR]) 26 October 2011 (26.10.2011)	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2014/050741

CLASSIFICATION OF SUBJECT MATTER

IPC
H01L 33/52 (2010.01)
H01L 31/0203 (2014.01)

INTERNATIONAL SEARCH REPORT
Information on Patent Family Members

International application No.
PCT/FI2014/050741

Patent document cited in search report	Publication date	Patent family members(s)	Publication date
US 2007215998 A1	20/09/2007	CN 101047221 A CN 100464439 C JP 2007258701 A	03/10/2007 25/02/2009 04/10/2007
US 2013161658 A1	27/06/2013	CN 103782402 A CN 104247055 A CN 104247060 A EP 2786429 A1 EP 2791982 A1 JP 2014525146 A KR 20140038553 A TW 201312807 A US 2013020590 A1 US 2013214298 A1 WO 2013013154 A2 WO 2013082445 A1 WO 2013101385 A1	07/05/2014 24/12/2014 24/12/2014 08/10/2014 22/10/2014 25/09/2014 28/03/2014 16/03/2013 24/01/2013 22/08/2013 24/01/2013 06/06/2013 04/07/2013
WO 2011073027 A1	23/06/2011	CN 102668140 A DE 102009058796 A1 EP 2513984 A1 JP 2013514642 A KR 20120114311 A TW 201143162 A TW I446594 B US 2012326178 A1	12/09/2012 22/06/2011 24/10/2012 25/04/2013 16/10/2012 01/12/2011 21/07/2014 27/12/2012
WO 2009061704 A2	14/05/2009	None	
US 2007004080 A1	04/01/2007	US 7348193 B2 CN 101523586 A CN 103318835 A JP 2009500848 A JP 5374150 B2 KR 20080028984 A KR 101304662 B1 WO 2007005228 A2	25/03/2008 02/09/2009 25/09/2013 08/01/2009 25/12/2013 02/04/2008 06/09/2013 11/01/2007
EP 2381491 A1	26/10/2011	CN 102237460 A JP 2011233881 A	09/11/2011 17/11/2011

International application No.
PCT/FI2014/050741

Form PCT/ISA/210 (patent family annex) (January 2015)